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SILICON-ON-CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet Task of the Low-Cost Solar Array Project

Annual Report No. 5

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A. B. Whitehead, J. D. Zook, B. L. Grung,
J. D. Heaps, F. Schmit, S. B. Schuldt, and P. W. Chapman

Period Covered: 9/29/79 - 9/30/80

Published: 5 January 1981

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NOTICE

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SUMMARY

The objective of this research is to investigate the technical feasibility of producing solar-cell-quality sheet silicon to meet the DOE 1986 cost goal of 70¢/watt. The silicon-on-ceramic approach is to coat a low-cost ceramic substrate with large-grain polycrystalline silicon by unidirectional solidification of molten silicon.

Results and accomplishments which occurred during the past year can be summarized as follows:

- A new silicon-coating system, SCIM-II, was designed and constructed (at Honeywell expense) during the first part of the year. This machine has demonstrated reliable operation, and has coated 10cm x 100cm slotted substrates.
- A design strategy to avoid buckling and breaking of substrates has been formulated, implemented, and verified. Thermal stress was not a problem at high speeds, but the coatings at high speeds have been very thin.
- Detailed thermal modeling of the heating and cooling zones has been performed, and the results have been compared with experiment. The qualitative as well as the qualitive results have been useful in making desirable modifications of the SCIM-II coater.
- A number of modifications have been made in SCIM-II to implement the strategy to minimize thermal stress and to improve reproducibility of coating conditions.
- Dip-coating has been continued in order to supply material for cell fabrication, since impure carbon parts have been used in the SCIM-coater while changes were still being made.
- The best cell had a total-area efficiency of 10.5% (AM1, AR) for a cell area of 5 cm^2. For 74 recent AR-coated cells, this average efficiency was 9.6% with a standard deviation of 0.5%

- The highest efficiencies were produced with a PH_3 diffusion at 850°C, followed by a slow cooldown at about 5°C/min.

- Theoretical modeling of SOC solar cells shows that present cell performance is limited by diffusion length, and that 13% SOC cells are possible with a diffusion length of 50 μm.

- The average diffusion length in SOC material is 15 to 25 μm. The diffusion length within good grains is three times the average diffusion length, $\bar{L}$. Closely spaced grain boundaries, high dislocation densities, and subsurface grain boundaries have been identified as structural causes of the reduction in $\bar{L}$.

- Cost estimates of the SOC process are $\$13/m^2$ added value, or $\$17.25/m^2$ including silicon at \$14/kg. Based on 11% module efficiency, this corresponds to a sheet cost of $16.6¢/W_p$. The analysis shows that the cost of ceramic is the largest cost driver in the SOC process.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 11% or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be made to wet only the graphite-coated face and produce uniform, thin layers of a large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous-coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 23 cm^2 in area have been achieved with single-crystal grains as large as 4mm in width and several cm in length. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Because SOC cell structure is on an insulating substrate, special consideration must be given to electrical contact to the base region. The preferred method uses slots in the substrate perpendicular to the crystalline growth direction. Electrical contact to the base region

is made by metallizing the silicon exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results to date indicate a 10.5% conversion efficiency (AR-coated) on a 5-cm^2 (total area) cell. Average conversion efficiencies, η, of about 10%, with antireflection (AR) coating have been achieved. Such cells typically have open-circuit voltages, V_{oc}, and short-circuit current densities, J_{sc}, of 0.57 V and 23.6 mA/cm^2, respectively.

The best SOC layers for solar cells have been produced by the dip-coating process. However, this process has two limitations if scaled up to a production method: 1) The melt becomes progressively contaminated by the mullite substrate. 2) The coating throughput in terms of area per unit time is limited. For these reasons, an alternative method of applying the silicon is being developed, which is termed SCIM (for Silicon Coating by Inverted Meniscus). The first SCIM-coating facility has successfully coated 5-cm-wide mullite sheets with uniform silicon layers by passing the sheets, carbonized surface down, over a trough of molten silicon. The current objective of this task is to uniformly coat slotted substrate sheets 5 inches wide. An improved SCIM coater was designed and built during the past year and has successfully demonstrated coating of ceramic substrates 10 cm wide by 100 cm long.

TECHNICAL DISCUSSION

CONTINUOUS COATING

SCIM-II Coater Description (J.D. Heaps and E. Masterson)

During the past year, a second continuous coating system (designated SCIM-II) was designed, constructed, and made operational. Its primary function is to demonstrate the capability of producing silicon sheet at a throughput rate of 14 cm/min (0.233 cm/sec).

To achieve this goal, the coater was designed as shown in Fig. 1 to simultaneously coat (side-by-side) two 12.5-cm-wide x 100-cm-long mullite substrates. The coating experience acquired using the original SCIM coater (SCIM-I) was a valuable asset in the design of SCIM-II. The design of this new coater is shown schematically in Fig. 2. There are several key features which are different from the SCIM-I system. They are:

1) All assemblies within the coater are attached to a common water-cooled chassis (see Fig. 3). This assures us that proper alignment of key parts will be maintained irrespective of operating temperature.

2) All metallic parts within the coater are water-cooled to improve the purity of the silicon layer and the majority of the remaining parts are fabricated from graphite which can be purified prior to assembly.

3) The melt crucible and trough are contained in a graphite cradle assembly which permits convenient adjustment of trough-to-substrate distance during operation.

4) Side heaters powered by a separate power supply were installed to improve the transverse temperature uniformity in the substrate preheater. These side heaters, however, have proven so far not to be a necessary feature.

5) The substrate transport mechanism consists of aluminum rollers which are fitted with several silicone rubber "O"-rings. The upper roller as well as the lower roller is driven by a loosely

coupled spur gear. The entrance and exit rollers are positioned external to the cover containing the inert atmosphere needed for growth. In operation, they have proven to be very effective in performing the transport function. With this method of substrate transport, however, the substrate used must be at least as long as the distance (97 cm) between the rollers. This can be a problem if a substrate breaks during coating. In this respect, the multiple roller method used in the SCIM-I is superior. However, the numerous rollers in SCIM-I, some of which are operating at temperatures as high as 1400°C, have been found to be only marginally dependable.

6) The water-cooled cover on SCIM-II serves only the function of containing the inert gas. As such, when this cover is removed, the inner walls are easy to clean. Likewise, when removed, the entire interworkings of the coater are easily accessable for maintenance.

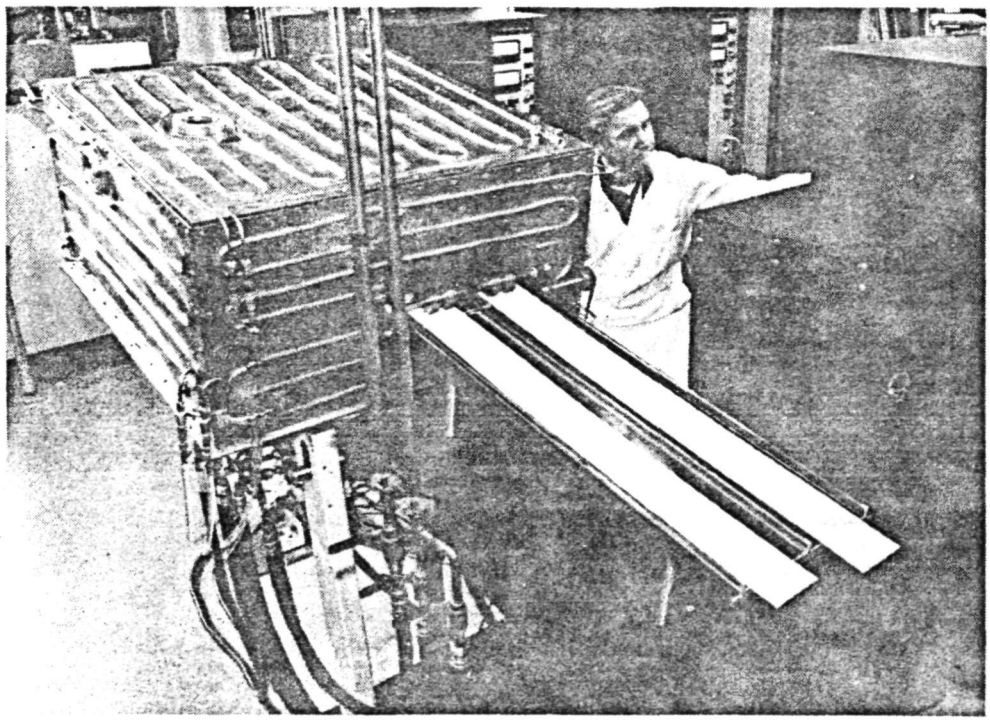

Figure 1. Photograph of SCIM-II exterior showing two side-by-side substrates entering the coater. So far, simultaneous coatings have not been achieved.

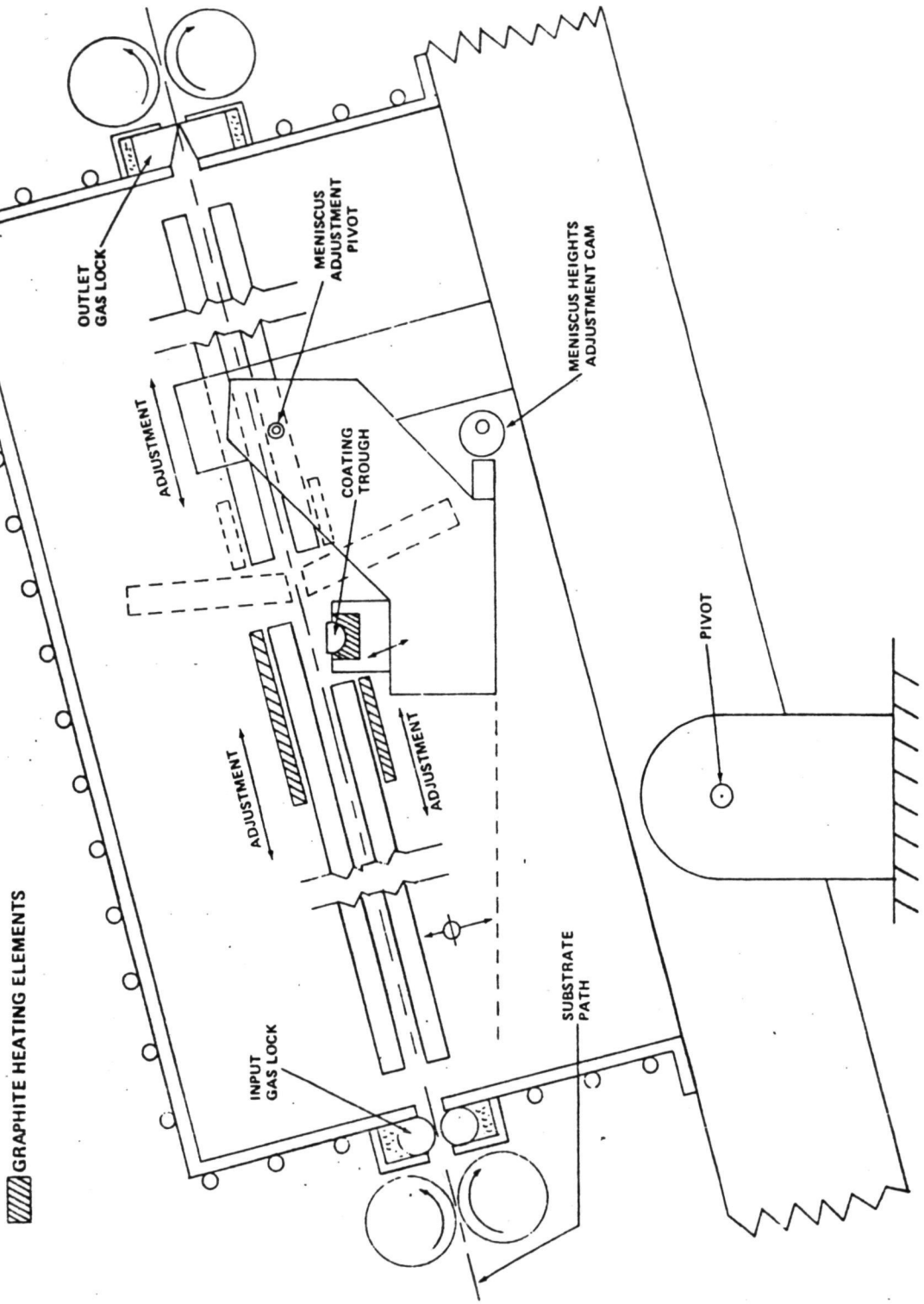

Figure 2. Schematic cross section of SCIM-II.

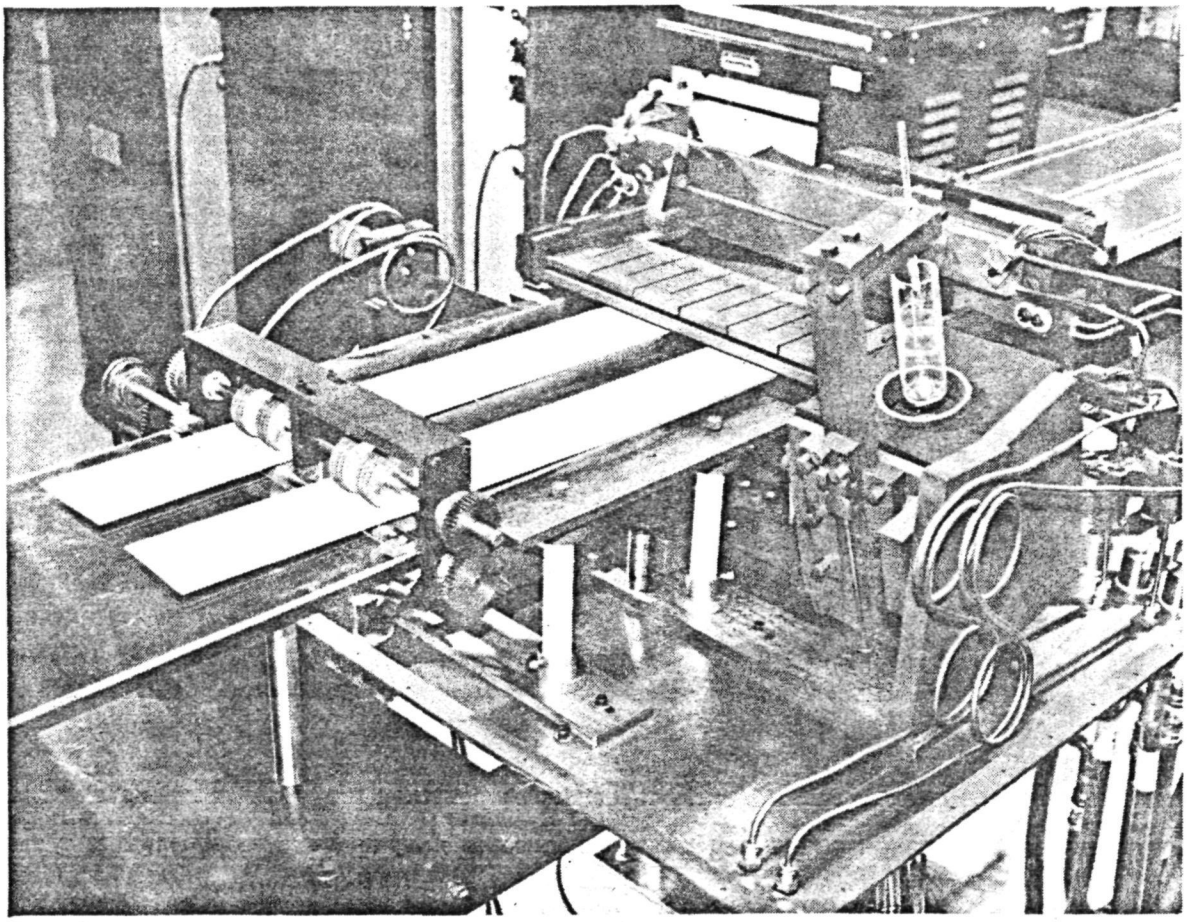

Figure 3. Photograph of SCIM-II interior showing water-cooled base and substrates emerging from preheater.

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The preheater and postheater design used in SCIM-II was fashioned after that of SCIM-I. This design was used because these functions in SCIM-I performed well. The purpose of the preheater is to bring the substrate from room temperature to the melting point of silicon in a manner which neither fractures nor warps the substrate. This is done by using a narrow graphite tunnel through which the substrate passes. One end of the tunnel is heated by a graphite resistance heater, and thermal conduction along the tunnel creates the needed temperature gradient. The postheater is similarly constructed. It, however, is a passive element deriving its heat from the preheater and the coating trough. This coating configuration produces a temperature profile with a rapid fall in temperature immediately downstream from the coating trough, thus creating the required thermal environment for solidification. To ensure that the coated substrate will emerge from the machine at a temperature of less than 232°C (the maximum operating temperature of the silicone rubber "O"-rings), a water-cooled heat sink is attached to the downstream end of the postheater. The thermal modeling contributing to this design is discussed in the next subsection of this report. In order to achieve a uniform transverse temperature, the preheater and postheater are substantially wider than the width of the side-by-side substrates being coated.

The trough heater and the fused-silica trough-crucible assembly is also fashioned after the design used in SCIM-I. The quartz trough nestles in an electrically active trough heater. The cross section of this heater is reduced at the electrode end in order that additional power can be generated to offset losses by conduction to the water-cooled copper electrodes and by radiation through the viewing port. The trough heater is also made purposely long for temperature uniformity reasons.

As with SCIM-I, SCIM-II can also be tilted to coating angles up to 20 degrees for the purpose of providing the necessary meniscus stability. To date, 10-cm-wide substrates have been coated at 10- to 20-degree coating angles and these results are also described in the next subsection of this report.

Thermal Profile Design to Avoid Thermal Stress (D. Zook)

The most obvious problem during the initial operation of SCIM-II (in March, 1980) was the buckling and/or breakage of the coated substrates. Experiments were performed without silicon in the system to clarify the situation. Initial experiments quickly showed that at high speed (15 cm/min) there was only

minor buckling, but at lower speeds the buckling became more severe, and below 6 cm/min the substrates broke. The results were qualitatively the same regardless of the silicon coating and regardless of whether one side of the substrate was carbon-coated.

The original design of the entrance and exit tunnels was based on a design speed of 15 cm/min, which is the 1980 program goal. The most interesting result is that at this high speed there has been little warping and no cracking of any substrates. This is true of the original design as well as all subsequent modifications.

The problem is that without forced convective cooling or use of any asymmetric growth mode, there is no chance of getting the desired silicon thickness at the high speed. The thickness is needed to demonstrate slot coverage and cell performance. Thus, we want to do initial coatings in the range of 4 to 6 cm/min. At these lower speeds, the substrates have warped, buckled, or cracked. The proposed explanation is that the longitudinal temperature profile must be the cause of the problem. At high speeds, the longitudinal profile is smoother than at low speeds because the heat capacity of the substrate causes a temperature lag. Thus, the purpose of the changes in tunnel design has been to linearize the temperature profile. Fortunately, this has reduced the problem at low speeds, and has not created any problem at high speeds.

The explanation in terms of thermal stresses caused by longitudinal temperature gradients is the same as that proposed by Surek for EFG ribbon growth.[1] The origin of thermal stress and the strategy to avoid it are discussed in the most recent SOC Quarterly Report (July, 1980).

As discussed by Surek,[1] the equation for the stress is

$$\sigma_{xx} = \frac{\alpha_E b^2}{6}\left(1 - \frac{3y^2}{b^2}\right)\frac{d^2T}{dx^2} \qquad (1)$$

in the case where only the second derivative of the temperature is significant. Here, α is the expansion coefficient, E is Young's modulus, and b is

[1] A.D. Morrison, et al., "Large-Area Silicon Sheet by EFG," Mobile Tyco Energy Corporation Annual Progress Report, September 15, 1976.

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one-half the substrate width. The solution is positive at the center (y = 0) and negative at the edges (y = ± b), indicating tension and compression, respectively, when d^2T/dx^2 is positive. At the ends of the substrate the solution is not valid, since $\sigma_{xx} = 0$. Thus, in the vicinity of the end, there are σ_{yy} and σ_{xy} stresses which can also be derived analytically.[1]

It is obvious that the temperature profile cannot be entirely linear in any substrate which is heated and then cooled and that both types of nonlinearities must be encountered, as shown in Fig. 4. Thus, thermal stress must always exist. However, there is a strategy which, at least in principle, can reduce the residual thermal stress to zero.[1] This strategy is detailed in Fig. 4. The idea is to have the concave portions of the profile in regions with high yield stress, and to maintain d^2T/dx^2 sufficiently low that $(\sigma_{xx})_{max}$ does not exceed the yield stress. Thus, thermal stresses do exist, but they result only in elastic deformation so that when the sample is again in a $d^2T/dx^2 = 0$ region, the residual thermal stress is zero.

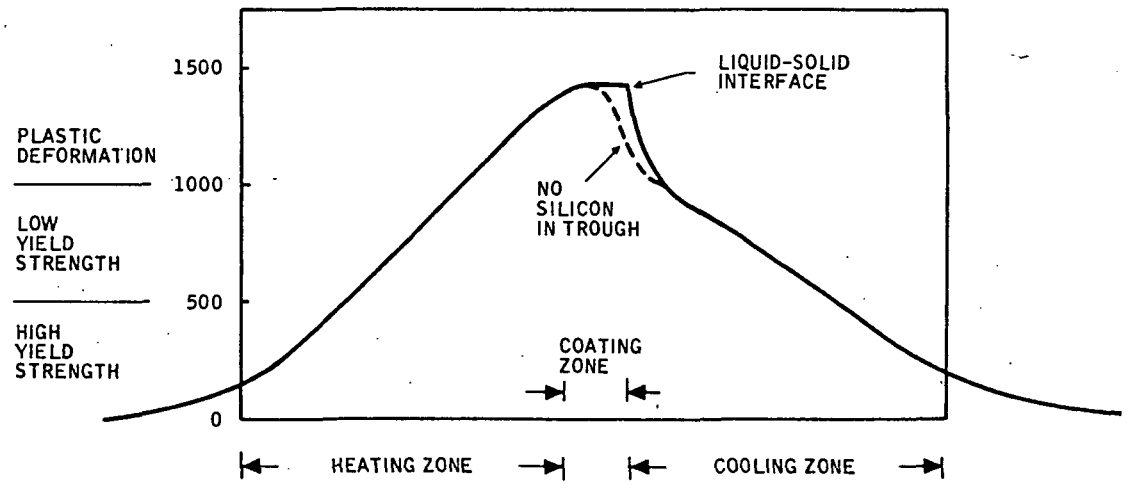

Figure 4. Strategy to eliminate effects of thermal stress. In the high-temperature regions, the ceramic can deform without buckling or cracking, and stress in the silicon is annealed as it is generated. At low temperatures, only elastic deformation occurs. The intermediate temperature ranges are critical, and the temperature profile must be linear.

At sufficiently high temperatures, the yield strength of both the ceramic and the silicon is low so that the sample can undergo plastic deformation with no buckling or cracking. Stress relaxation studies in silicon[1] show that at 1000°C the stress relaxation time is a few seconds. The assumption is that the plastic flow occurs by diffusion-controlled climb of dislocations, and that the presence of the dislocations is not deleterious to the

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solar cell performance.[1] Thus, in the vicinity of the trough and especially of the liquid-solid interface, the presence of large nonlinearities in the temperature gradient will not have harmful effects.

In summary, the strategy is to consider the problems in terms of three temperature zones. The following strategy applies to both the heating and cooling zones:

a) The high-temperature zone ($T \gtrsim 1000^{o}C$) can tolerate large nonlinearities in the temperature profile.

b) The intermediate temperature zone ($1000^{o}C \gtrsim T \gtrsim 500^{o}C$) must have a very linear profile.

c) The low temperature zone ($500^{o}C \gtrsim T$) can tolerate large nonlinearities such that the thermal stress does not exceed the elastic limit of silicon on ceramic.

Thermal Modeling for SCIM-II (S. Schuldt)

Thermal stresses have continued to be a problem in the substrate heating and cooling chambers of SCIM-II, but a combined experimental and theoretical approach is making good progress toward solving the problem. According to the design strategy based on stress analysis (Fig. 4), a linear longitudinal temperature profile is sought for the temperature range of low yield strength, from 500 to $1000^{o}C$. The linear profile is necessary in both heating and cooling in order to eliminate or at least greatly reduce residual stresses in the coated ceramic panels. A second requirement is to provide rapid initial cooling of the coated substrate, as prescribed by heat balance at the silicon liquid-solid interface. The second requirement will not be in conflict with the first one if rapid cooling is restricted to the plastic deformation region, as indicated in Fig. 4.

It is expected that the thermal design of a production coater can be optimized for a given fixed feed rate. In the experimental growth system, thermal design is complicated by the need to accommodate more than one feed rate; an ideal temperature profile is difficult to maintain over a wide range of feed rates. At low speeds, the substrate is likely to heat up over-rapidly on first entering the heating chamber. At higher speeds, this is moderated by the thermal inertial time lag. On the other hand, high-speed panels tend

to emerge from the cooling chamber insufficiently cooled. The first problem can be eliminated by heat-sinking at the entrance to the heating chamber, whereas the second problem is relieved by heat-sinking at the exit from the cooling chamber. A more flexible means of accommodating different speeds is to vary the amount of insulation placed in the respective chambers.

A great deal of insight into these and other aspects of the thermal design problem has been provided by a mathematical analysis of the heating and cooling chambers. A brief thermal description of the mathematical models follows.

The substrate panels are transported at ambient temperature to the heating chamber, which is shown in schematic cross section in the left half of Fig. 5. This is made up of pairs of active heaters, carbon guides (also functioning as the passive heaters), and insulating layers. The 1mm-thick ceramic panels move left to right between the guides, acquiring heat by radiation from the guides, so that they reach 1693 K when they arrive at the right end of the tunnel. At this temperature, the melting point of silicon, they are ready for silicon coating in the chamber immediately to the right. It will be noted that the moving panels extract a total of $\rho Cwt\Delta T$ joules of heat per centimeter of length, where ρ and C are the density and specific heat, w and t are panel width and thickness, and ΔT is the temperature rise. If the panel feed rate is v cm/sec, the active heaters then must supply energy at a rate greater than $\rho Cwt\Delta T$ watts. The "greater than" may be made to approach "equal to" if wasted heat is minimized; that is, the quantity and placement of insulation are such as to prevent significant losses to the water-cooled case.

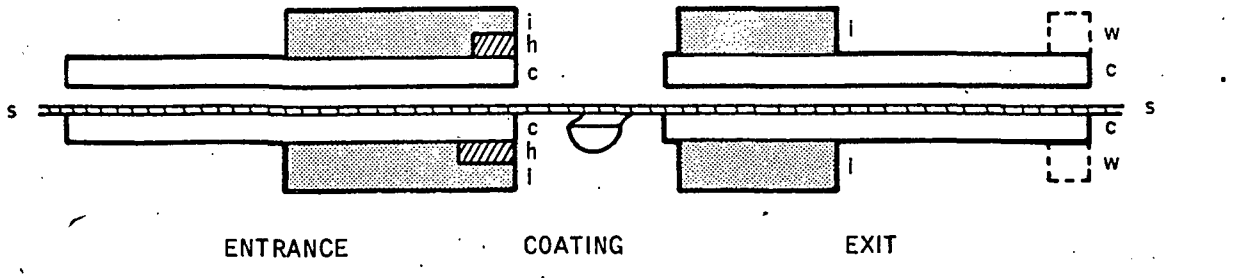

Figure 5. Schematic cross section of SCIM-II showing simplified arrangement of various thermal elements used in the modeling. h = resistive heater; c = carbon (guide); i = insulation; w = heat sink (when present).

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After the silicon-coating step, the panels traverse a cooling chamber (right half of Fig. 5) of similar geometry to the entrance tunnel. The important difference is the omission of the active heaters. However, the water-cooled case and variable insulation are essential. Inasmuch as cooling is passive with the case being the heat sink, the carbon guides are a hindrance to cooling though needed for mechanical support. The guides act like heat shields interrupting the radiative transfer from silicon-coated panels to the case. The important heat escape path is vertical from panel to guide to case, with a lesser contribution by way of longitudinal conduction through the guides.

The need for design flexibility is reflected in the variable structure of the mathematical models; provisions are included also for experimental calibration:

- The amount of insulation used in the heating and cooling chambers can be varied. Adjusting insulation may be the quickest and easiest way to set up different substrate speeds.
- The far ends of the cooling chamber guides have tended to reach excessively high temperatures in both theory and practice. The theoretical model includes an optional heat sink at these ends.
- "Standby" versions of the models have been provided. These represent heating and cooling chamber with heaters active but no substrate present. The main purpose for these versions is to calibrate the models against temperature measurements, which are normally taken with the chambers empty.

Only longitudinal temperature profiles are being analyzed, since these are believed to be associated with warping and breakage. Transverse temperature variations also occur and are discussed elsewhere. The main problem caused by transverse variations is coating nonuniformity, and this is being successfully attacked by heater redesign.

The physical relationships upon which the thermal models are based will next be summarized. All temperature profiles are assumed to be one-dimensional; thus, variations in the transverse direction are ignored. Several thermal elements interact with one another (Fig. 5) so that as many as five coupled heat equations must be solved. Basically, the electrical input produces heat in the resistive heaters (h), and this heat spreads along both heating chamber guides (c) by thermal conduction. In the steady state, the heated

guides release part of this energy by radiation to the entering substrate(s) and the rest is lost by radiation and conduction to the ambient. The model includes a convective heat transfer coefficient, but this has been set equal to zero in the calculations reported here. A significant portion of the heat loss takes place from insulated surfaces due to the limited thicknesses of carbon felt. The substrate(s) acquires heat from the guides so that its temperature increases from approximately ambient at the left to the coating temperature (1420°C).

In the cooling chamber, the process is essentially reversed. The substrate is progressively cooled by radiation to the cooling chamber guides and by conduction in the downstream direction. Because of the heat-shield effect, the cooling rate is lower than it would be in the case of direct radiation to the 300 K ambient. The cooling problem is further aggravated at the far (right) end because thermal conduction within the guides tends to elevate the temperature at that end. This effect can be greatly relieved by heat-sinking (w).

End effects are found to be significant and are included both at the external ends facing the cool environment, and the internal ends facing the coating chamber. Not only the actual end surfaces are affected but also parts of the internal surfaces close to the ends. The moving substrate is not completely cooled when it emerges from the cooling chamber. It is important that enough cooling has taken place at this point in order to avoid a further precipitous temperature drop outside ofthe chamber. In the numerical calculations, a practical approximation is required for the boundary condition at infinity. We use $T = T_o$ (room temperature) at a point some distance (a few cm) beyond the tunnel end. Over this distance, the radiation environment is assumed to be at temperature T_o. It is easily verified that the approximate boundary condition does not affect the numerical solutions for the temperature within the chamber. Figure 6 shows calibration of model against measurements taken by placing a thermocouple instead of the substrate.

The finite-difference grid for the heating chamber represents 1-cm increments in longitudinal position, or 41 points for a 40-cm tunnel. Since there are five coupled layers (two heater-insulation layers, two guides, and one substrate), there are 5 x 41 = 205 nodal equations which are solved by a direct-inversion method for sparse matrices. The matrix has a bandwidth of 11 and is asymmetric due to the moving substrate. Since the radiation law is nonlinear and thermal conductivities are temperature-dependent, the equations are

resolved iteratively with updated coefficients for the nodal equations. Convergence occurs in about 20 iterations. For the cooling chamber, a finer grid (0.33 cm) is used, but heater-insulation layers are not required.

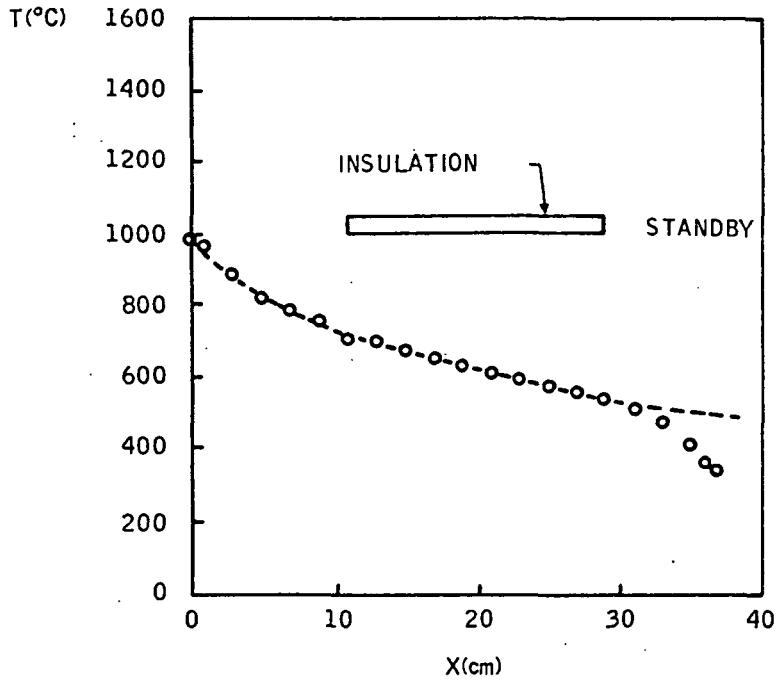

Figure 6. Calculated versus experimental exit tunnel temperature with no substrate in chamber.

Heating Chamber (Entrance Tunnel) Results -- Calculated temperature profiles are shown in Fig. 7 for two substrate speeds. The solid curve gives the substrate temperature and the dashed curve gives the mean guide temperature. (The two guides may differ up to 20°C from each other at any x position.) The dotted curve represents mean guide temperature under standby conditions--the same electrical input but no substrate. The high-speed substrate profile is nearly linear, indicating optimum design for high speed. Electrical input is 135 W/cm of width, of which 92 W/cm heats the substrate, the rest being absorbed by the ambient environment. The standby profile is considerably elevated because the entire 135 watts is wasted to the environment, thus requiring a higher average radiation temperature.

The low-speed profile demonstrates some of the difficulties encountered in trying to optimize the basic chamber design for a range of substrate speeds. With all the insulation in place, the initial temperature rise in the

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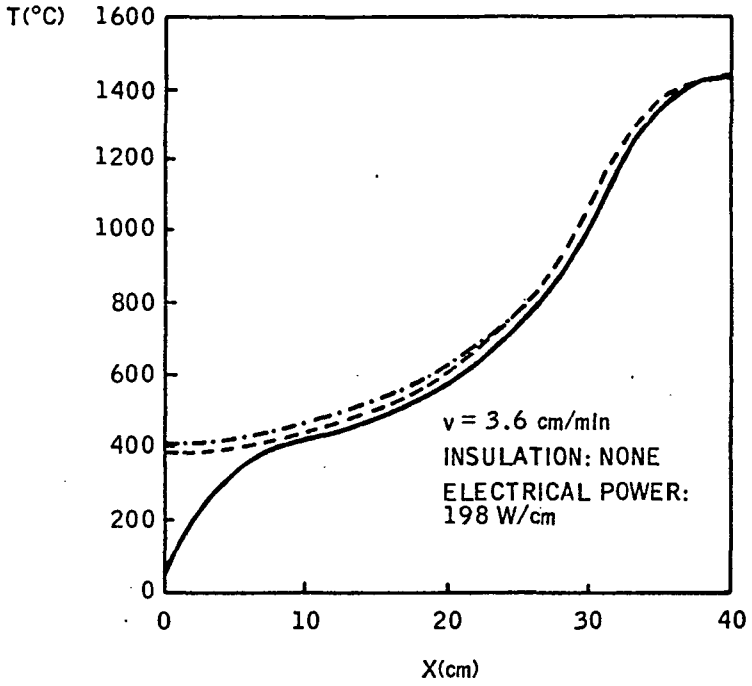

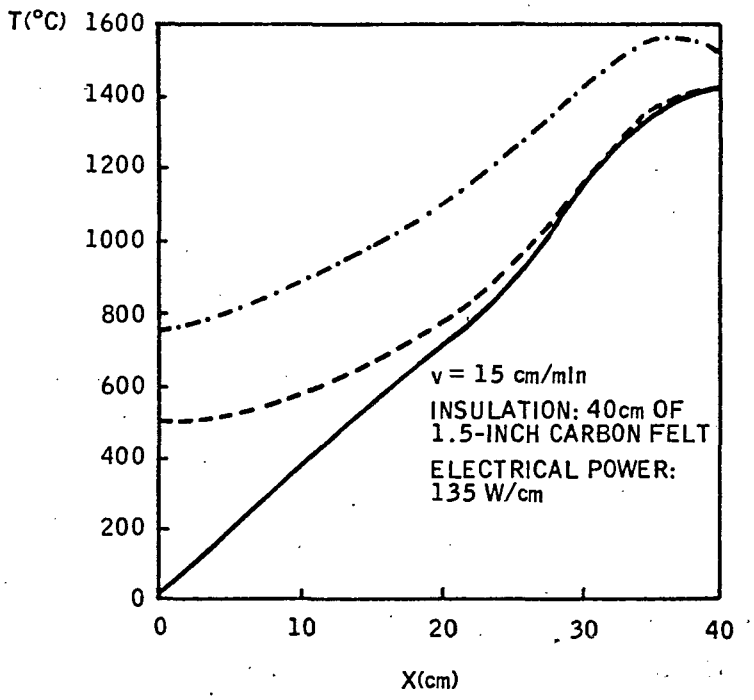

Figure 7. Calculated entrance tunnel profiles corresponding to slow and fast operation. Guides are 0.5 inch thick and the channel height is 0.5 inch. Solid profile corresponds to the substrate; dashed, to the guides under operating conditions; and dotted, to guides in standby conditions with same electrical input.

substrate is extremely rapid. This is moderated by removing all of the insulation, giving the indicated profile, which is still somewhat too steep and has excessive curvature. The curvature is initially convex but becomes concave in the middle due to the large radiation losses from the guides. It becomes convex once again the heater region at the end. The electrical input, 198 W/cm, is almost totally wasted, with only 12 W/cm required to heat the substrate. As discussed in SOC Quarterly Report No. 13 (January, 1980), the theoretical profile for the low-speed case is best improved by increasing the thermal resistance of the guides--for example, reducing their thickness. A compromise solution is being investigated experimentally; carbon has been removed in transverse grooves at the ends of the guides.

Cooling Chamber (Exit Tunnel) Results -- The substrate temperature distribution in the cooling chamber should satisfy two requirements: (1) a large initial gradient to carry off the latent heat of fusion of the grown silicon layer; (2) a nearly constant gradient from 1000°C to 500°C. As previously explained, these requirements are different to satisfy simultaneously under all conditions. The location of the insulation is critical; since the cooling curve has the greatest curvature at high temperatures, the insulation should be placed fairly close to the beginning of the chamber. On the other hand, the first requirement demands a fast initial cooling, and this dictates leaving a finite uninsulated gap at the very beginning. A 1-centimeter gap was found to be sufficient to retain the full initial cooling rate. The next $\sim$ 18 cm of both guides are insulated for present experimental work, and the same insulation interval (1 to 19 cm) was used in the numerical calculations plotted in Fig. 8. The effects of this insulation are readily observed by comparison with Fig. 9 which represents the uninsulated case.

As discussed above, the high exit temperatures are intolerable. A water-cooled heat sink was recently added at each guide end, and according to calculations (Fig. 10), a substantial lowering of the exit temperature was expected. As discussed below, this was indeed the result.

SCIM-II Coating Results (F. Schmit, D. Zook, R. Hegel, H. Burke, and V. Harris)

The SCIM-coating activity has continued to receive heavy emphasis and high priority in the program. The primary goal has been to achieve uniform coatings without substrate breakage or warpage. A second goal has been to achieve shutdown without breakage of carbon parts, especially heater elements.

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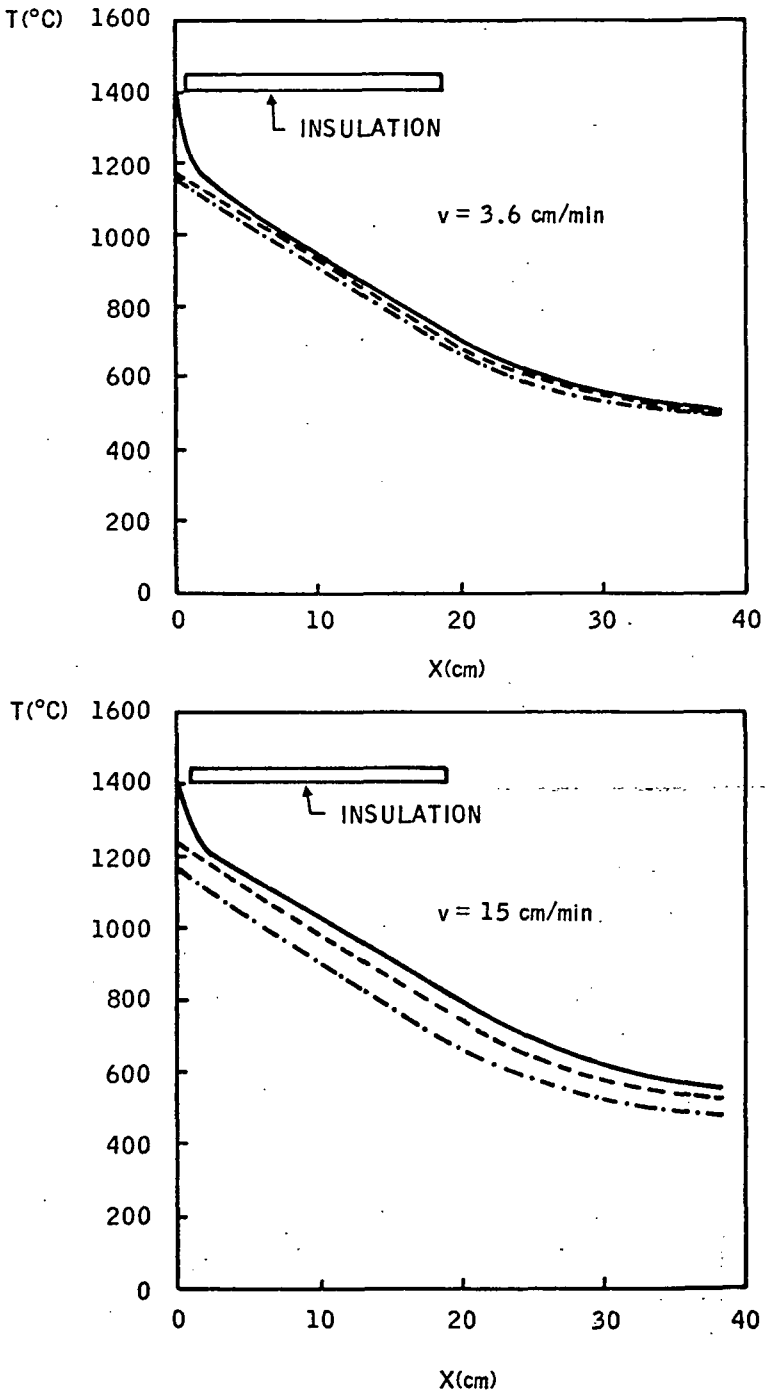


Figure 8. Calculated exit tunnel profiles at different speeds with insulation located as indicated (carbon guides are not heat-sunk). Solid profile corresponds to guides under operating conditions, and dotted profiles to guides in standby conditions.

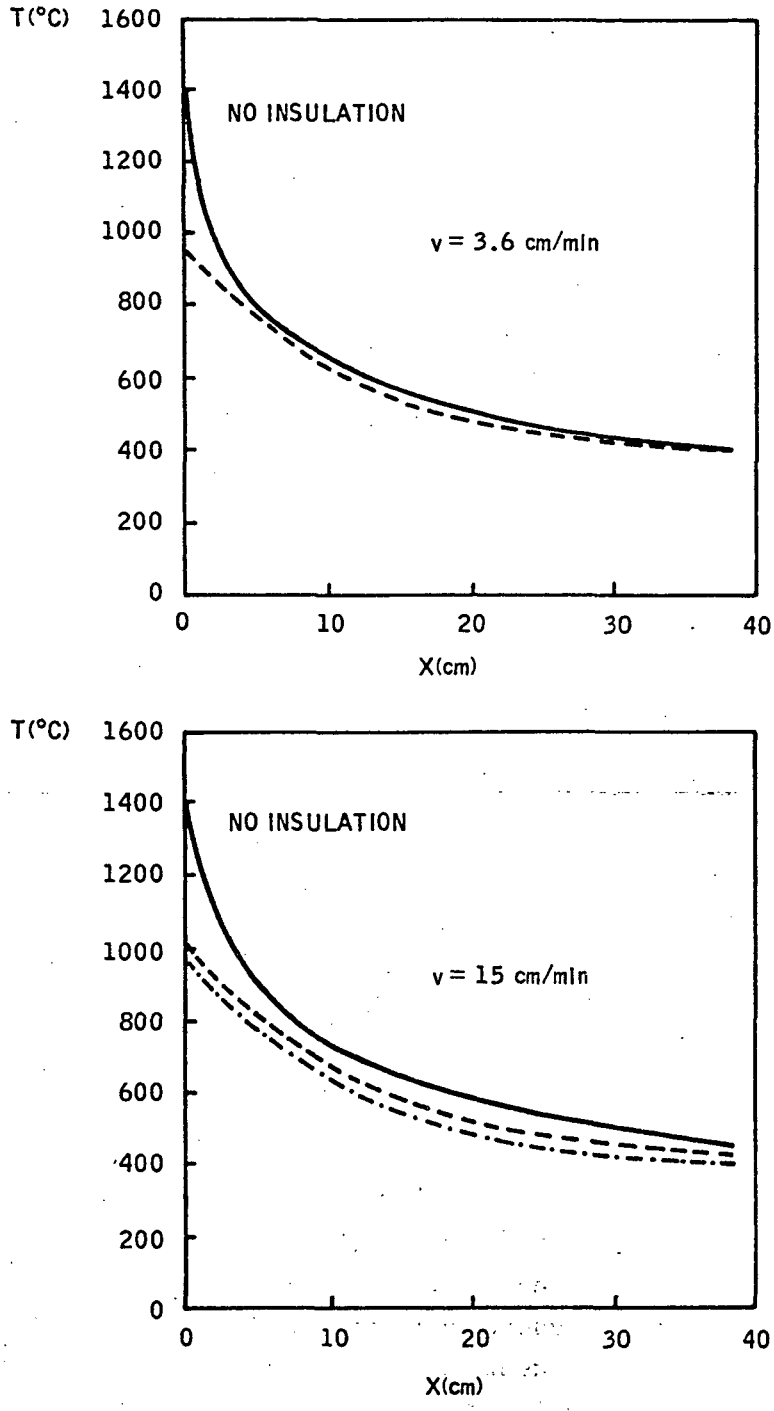


Figure 9. Calculated exit tunnel profiles at different speeds without insulation. Carbon guides are not heat-sunk. Solid profile corresponds to substrate; dashed profile corresponds to guides under operating conditions; and dotted profile corresponds to guides in standby conditions.

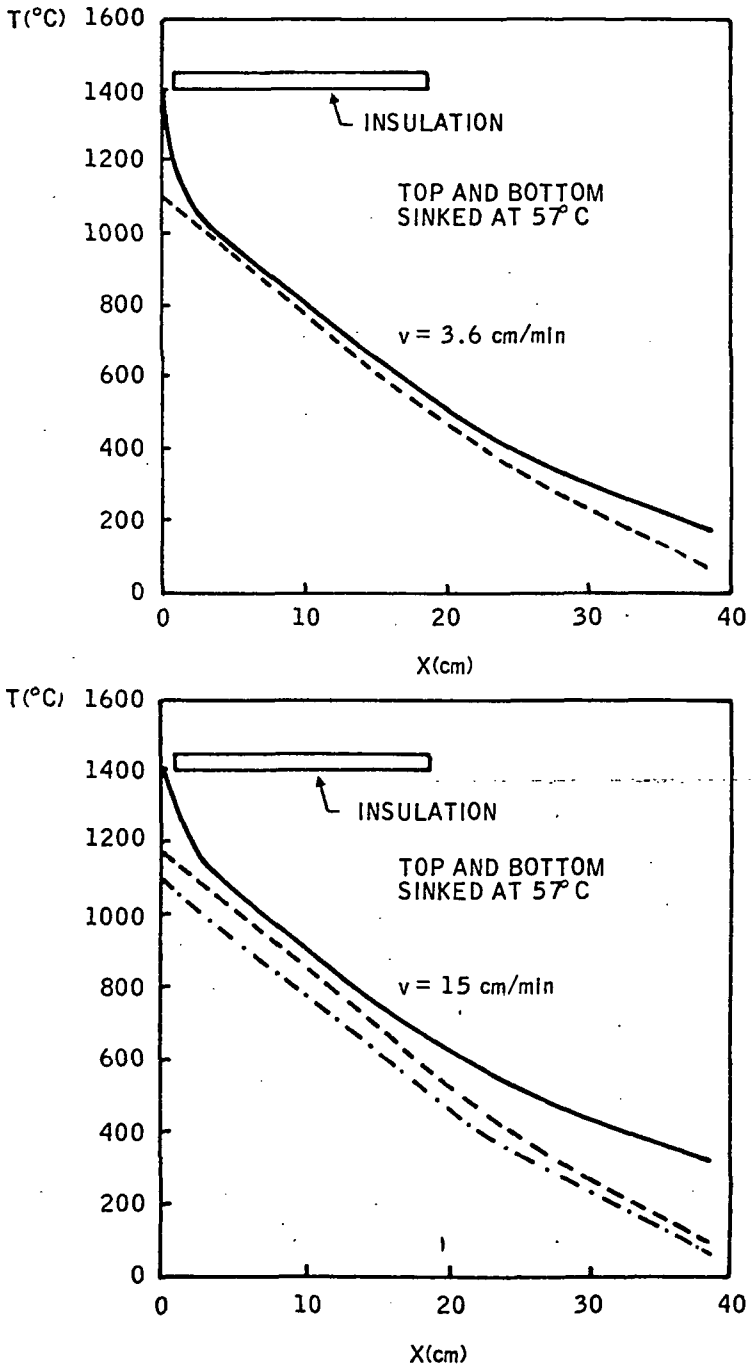


Figure 10. Calculated exit tunnel profiles with heat sink at exit end.

To achieve these goals, a large number of modifications were made in the system:

- Entrance tunnel heaters were simplified and moved forward.
- The side heaters were found to be unnecessary with the new entrance tunnel heaters.
- Insulation was added and removed at various times.
- The trough heater was designed to compensate for unavoidable conduction and radiation heat loss nonuniformities.
- The exit tunnel was connected to a water-cooled heat sink as indicated by modeling and by measurements.
- The method of measuring temperature profiles was changed several times.
- Closed-loop control of the temperature in the trough was implemented.
- The angle of the quartz trough was changed so that it tilts backwards in operation.

These and other changes have given much improved operation. A summary of coating results is given in Table 1. The results and current status are described below in some detail. It is to be noted that further changes are anticipated, but not major ones involving carbon parts, so that the purified carbon parts have now been ordered.

Temperature Profile Measurement -- A note on the measurement of the temperature profile is in order. Careful measurement shows that when the thermocouple is inserted from the entrance port, the reading is different from when the same thermocouple is at the same position from the exit port of the coater. The discrepancy is opposite to that expected on the basis of conduction of heat along the thermocouple. For example, the temperature above the trough is 30 degrees hotter when measured from the exit port, where heat is conducted away from the probe. The only reasonable explanation for the discrepancy is that the thermocouple is responding to the direct radiative environment and that the presence of the ceramic probe blocks the radiation. Thus, in the above example, the probe is pointed toward the hot

Table 1. SCIM-II coating runs during the past quarter.

Run No.	Date	Results
19	7/1/80	Six 10 x 100-cm substrates coated at speeds from 4 to 20 cm/min. Slow ones cracked and fast ones were thin, all-solid substrates.
20	7/17/80	Profile run. Drag T/C through.
21	7/19/80	Profile run. Tried H-shape and a "pusher" substrate.
22	7/24/80	Profile run with water-cooled exit tunnel.
23	8/1/80	Two 10 x 100-cm substrates coated at 10 cm/min. Too high a trough temperature gradient. Lots of SiO. Silicon hung up on side of crucible. Carbon frame around trough heater.
24	8/11/80	Profile run. Insulation on trough heater. Trough heater at 10-deg angle. Reduce entrance tunnel height to <5mm. Cut quartz trough parallel to heater.
25	8/14/80	Two substrates 10 x 100 cm. Cracked lengthwise. Trough freeze-up at crucible end.
26	8/25/80	Profile with 6 T/C's in exit tunnel plate showed exit tunnel temperature goes down when substrate goes through. Profile also showed exit tunnel 200°C cooler than previous measurement.
27	8/26/80	Profile run. No insulation on exit tunnel.
28	8/28/80	Mounting bolt arcing - abort run.
29	9/5/80	Profile run with substrate at 5 cm/min.
30	9/9/80	Profile run with substrate at 5 cm/min.
31	9/11/80	Silicon leak - abort run.
32	9/15/80	Nine substrates coated, all solid; 7 of them 10 x 100 cm, 2 of them 5 x 100 cm; looked good.
33	9/18/80	Eight substrates coated. Dendritic growth and breakup. Entrance tunnel cutback 1 cm may have been too much.
34	9/25/80	Profile run.
35	9/29/80	Seven substrates coated. Five were 10 x 100 cm and one was partially slotted. The other two were 5 x 60-cm slotted substrates. Some areas thin or cracked, other areas thick over slots and good looking.

entrance tunnel and reads hotter than when it is pointed at the cold exit tunnel. We now use a differnt method of reading the temperature profiles. A series of thermocouples was installed by drilling holes into the half-inch plates and cementing a thermocouple into each hole. The results of recent measurements are discussed in the following paragraphs.

The temperature of the exit-tunnel plates as indicated by the type K thermocouples, shows a sharp discontinuity at the edge of the insulation. This result also follows from the thermal modeling (see Fig. 10). Figure 11 plots this profile and sketches the insulation position. The function of these carbon plates is to take the sample from a high temperature where the ceramic is soft smoothly down to a low temperature where the sample is strong enough to withstand the strains (Fig. 4). There is a change in slope at the end of the insulation. In this case, breakage of substrates occurred, presumably due to the sizeable second derivative in the profile. Figure 12 shows the case where there was no insulation at all, and the profile is quite linear. Obviously, no insulation is not very energy efficient. It also prevents bringing the leading edge of the exit tunnel up to the 1000°C temperature range required by the mullite. We then covered the exit tunnel with a uniform layer of graphite felt from the leading edge of the carbon all the way back to overlap the water-cooled copper plates. Figure 13 shows the profile of the present exit tunnel and shows the position of the insulation and water-cooling. A similar set of thermocouples was mounted in the entrance tunnel to provide a profile of the entire SCIM-II coater. Figure 14 is a plot of the profile of the entrance and exit tunnels at two different input power levels. Considerable crosstalk between the trough heater temperature and the entrance tunnel heaters is indicated by the fact that the trough heater cannot reach 1400°C with 400 A, and when the entrance tunnel heaters are at 500 A the trough heater is able to maintain 1400°C. Also note the 900°C temperature at the leading edge of the exit tunnel corresponding to 400 A. Under these conditions, thermal stresses were excessive. We have concluded that at 900°C the exit tunnel is too low to begin cooldown on the substrate, whereas at 1000°C or more the 10-cm x 100-cm samples do not buckle at low or high speeds.

The data in Figures 11 through 14 all have been taken without samples or silicon in the trough. Figure 15 is the operating profile of SCIM-II, including all of the following cases:

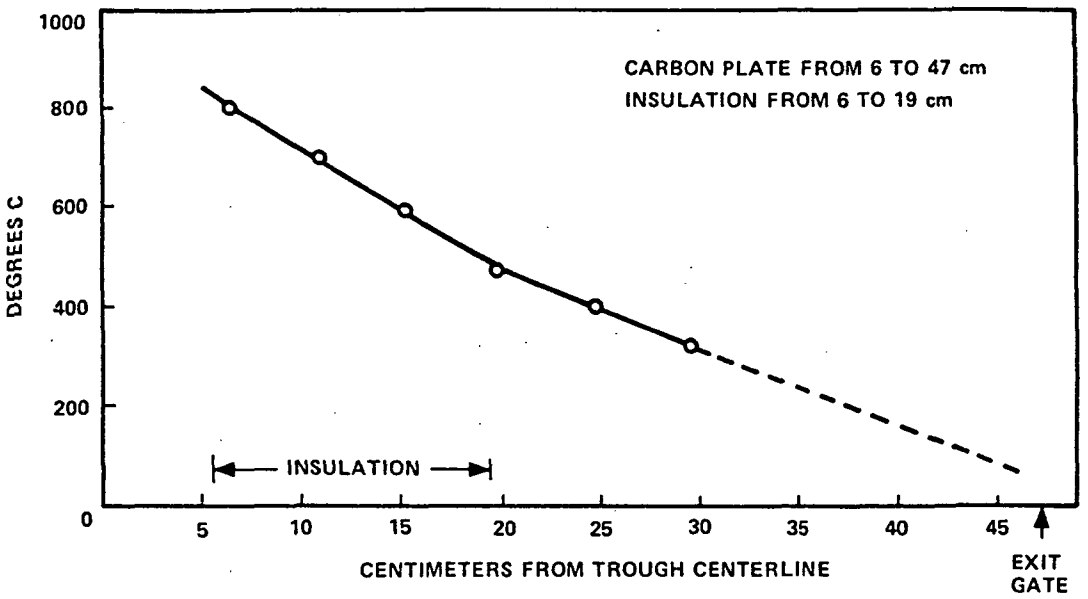


Figure 11. Temperature profile of partially insulated exit tunnel. The horizontal scale is measured in cm from the center of the trough. The data were taken with thermocouples imbedded in the carbon plates to avoid radiative coupling problems.

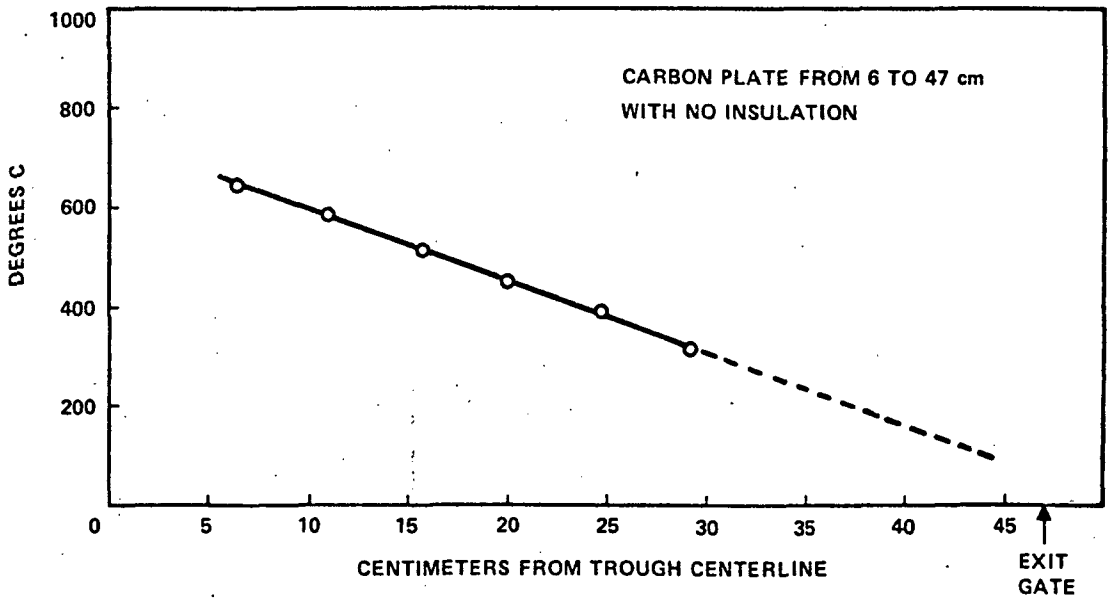


Figure 12. Measured profile of uninsulated exit tunnel.

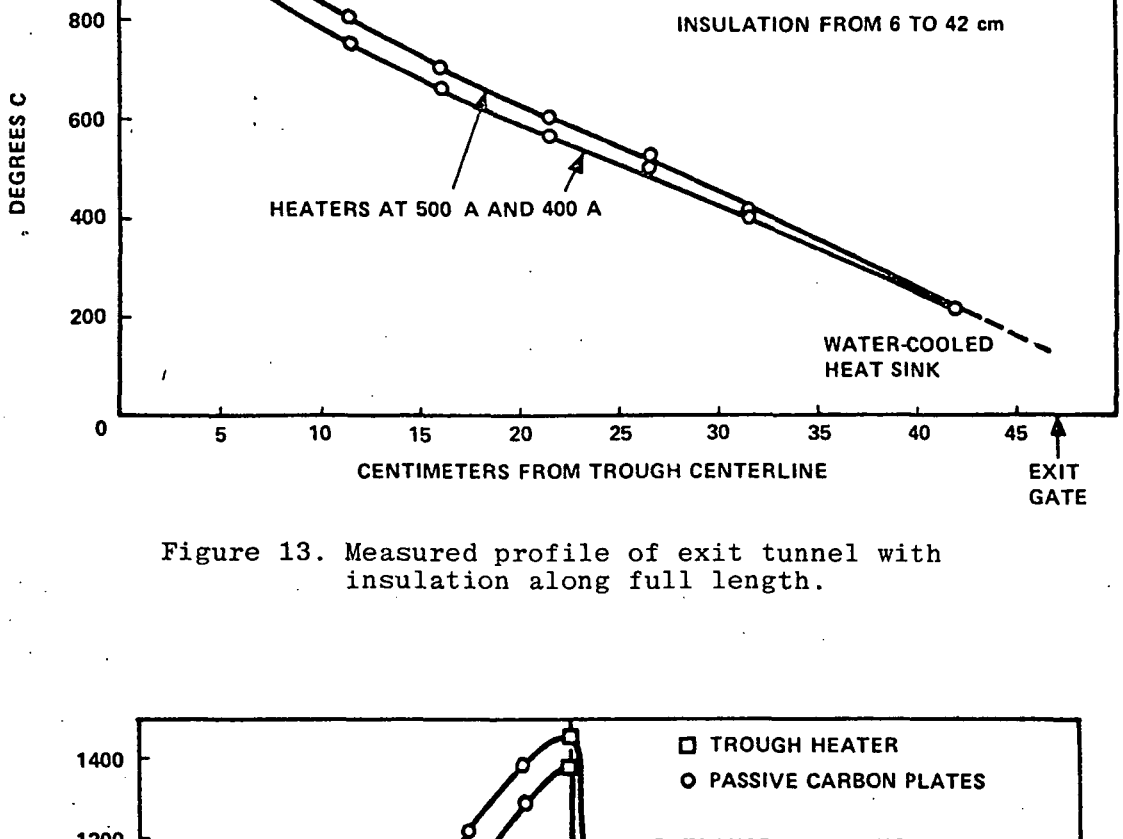


Figure 13. Measured profile of exit tunnel with insulation along full length.

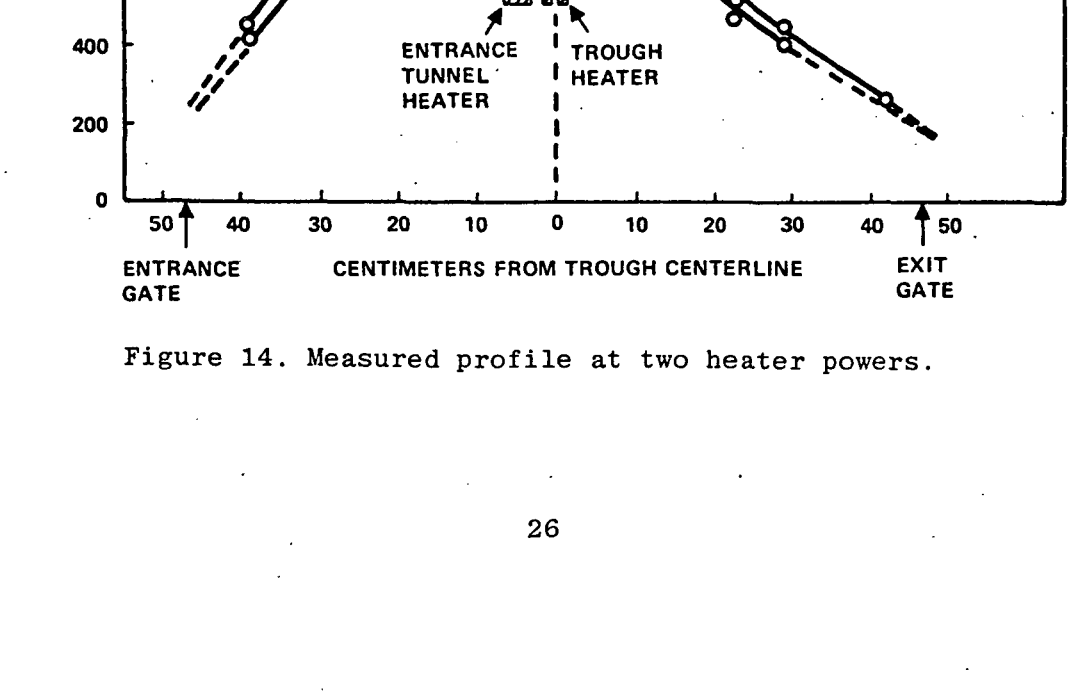


Figure 14. Measured profile at two heater powers.

- Substrates going through from 3 to 10 cm/min
- No substrates at all
- Silicon in the trough
- No silicon in the trough
- Coating SOC at 5 cm/min.

The height of the error bars shows the total variation in temperature under these conditions. This variation was only ±20°C at the most critical point (at the leading edge of the exit tunnel). With these conditions, the system can coat silicon on 10-cm x 100-cm ceramic substrates without buckling or cracking due to thermal stress.

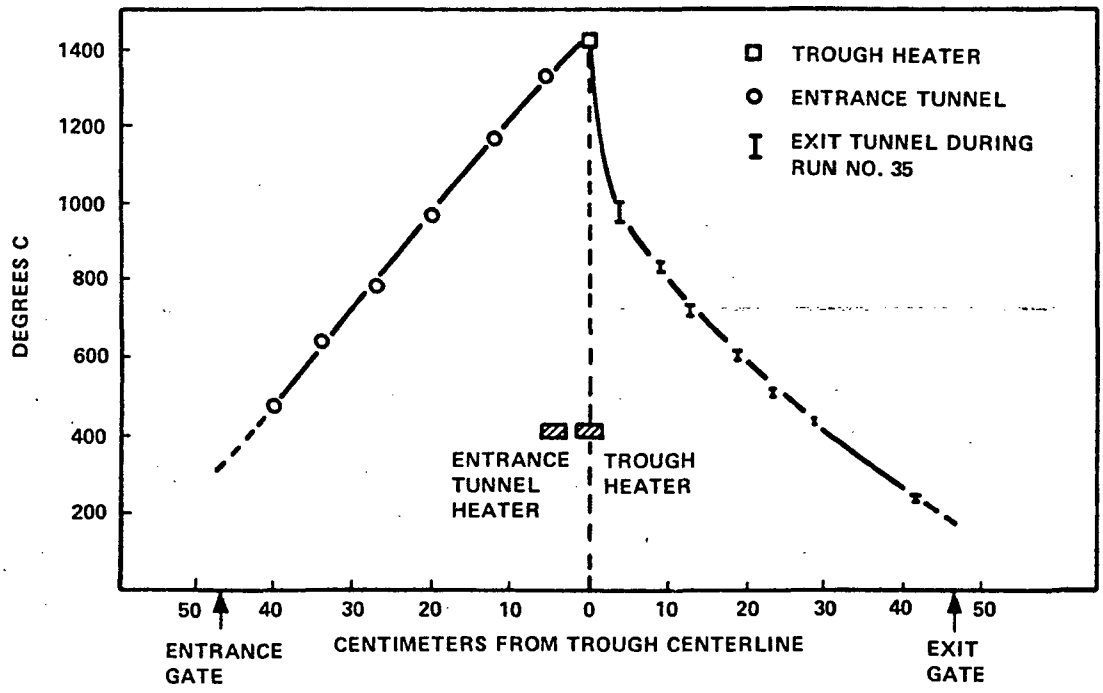


Figure 15. Measured profile during a run.

Heater Insulation -- Resistive carbon heaters are designed and built to surround the crucible or trough as much as possible. For the entrance tunnel, the heaters are adjacent to the carbon plate to be heated. In these cases, only one side of the heater sees the material to be heated, whereas the other side (outside, backside) radiates into some free-standing insulated structure which should act as a radiation shield. As the element to be heated approaches operating temperature, e.g., 1400°C in our system, it no longer requires a great deal of power from the heater, whereas the box between the heater

and the insulation that is holding the insulation continues to drain power from the system.

Three of our four heaters have been modified to minimize this loss and focus the radiation in the direction intended, by simply attaching the insulation directly to the electrically active heater element. The structure to hold the insulation is now the heater itself and no longer need be the elaborate structure previously used. The hottest part of the heater is now in contact with the insulation with reduced radiation, convection, or conduction losses on that side. The bare portion of the heater still radiates directly into the intended heat sink.

The insulation on the top entrance tunnel heater is simply a straight flat blanket cemented on top of the heater. The bottom heater is identical except for the insulation being underneath. The trough heater is somewhat more elaborate in that three sides of the heater are insulated at the end where the current connections are made, two sides are insulated along the coating length of the trough, and no sides are insulated where the heater reaches into the crucible container and nearly touches the crucible heater. There is a small stretch of three-side insulation between the crucible box and the coating area as well. All along the trough heater, the insulation is divided, since there is a voltage drop between the two sides. The 2mm gap in the heater is sufficient to maintain separation of both heater and insulation. Figure 16 gives a cross-sectional view of heaters, plates, and insulation.

Patent disclosures have been filed on the idea of putting the insulation directly on the heater and on a method of preparing the graphite felt for cementing onto a heater.

Observations of Meniscus Shape -- Having now coated many meter-long substrates, a few comments on the observed shape of the menisci seem in order. Figure 17 sketches the coating menisci. It shows the trough maniscus is controlled by the displacer as well as the inverted meniscus which is also affected by tilt angle, trough meniscus, and the thermal conditions which position the liquid-solid interface (LSI).

When the tilt angle is 20 degrees and the trough meniscus is horizontal, the inverted meniscus comes up from the trough with its center of curvature on the exit tunnel side of the trough and the LSI is above point A in Fig. 17.

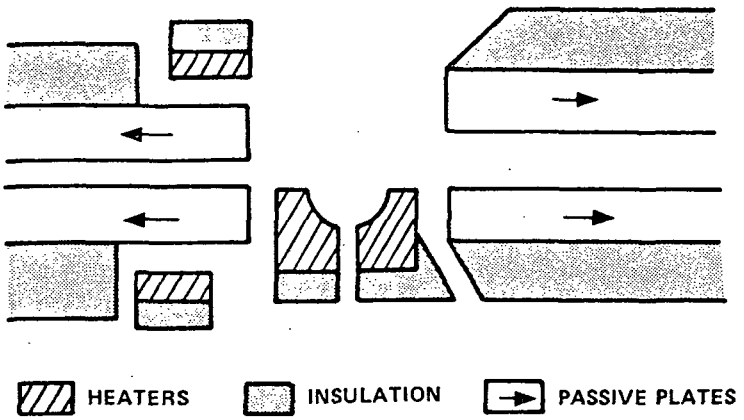


Figure 16. Schematic cross section of coating zone, including heaters, insulation, and passive plates.

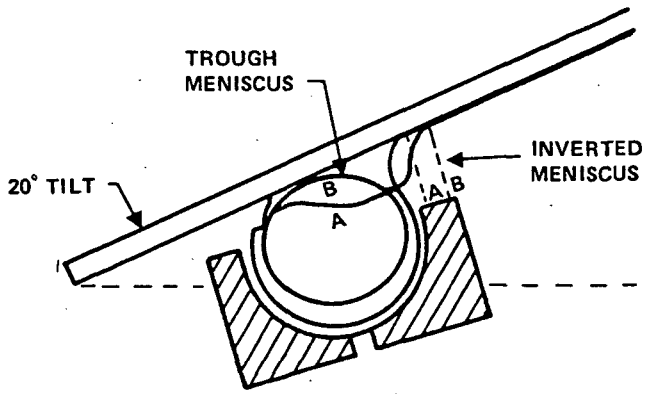


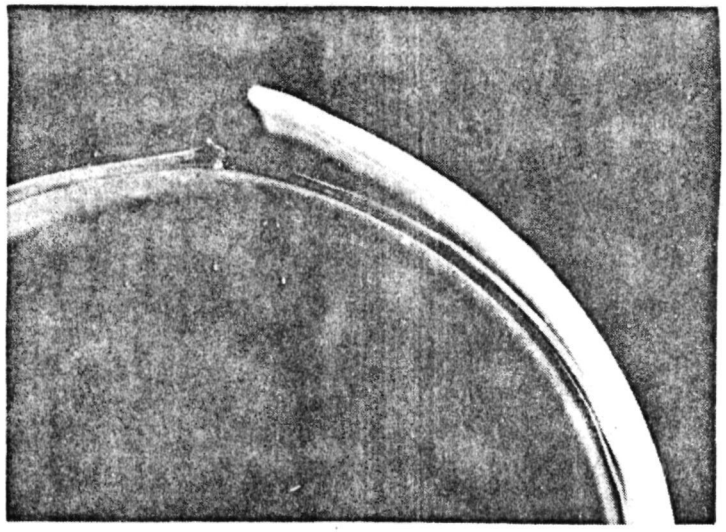
Figure 17. Meniscus shape during coating. The lettered trough meniscus produces a liquid-solid interface (LSI) at the lettered position. The LSI at "A" and "B" are <2mm apart. "B" can grow layers 100 μm thicker than "A" but the inverted meniscus at "B" is unstable at 20 degrees tilt.

At this same tilt angle, when the trough meniscus is pushed up above the trough, the inverted meniscus goes through a flip-flop condition and becomes S-shaped. The lower portion of the S hangs out over the outside of the trough and threatens to spill onto the heater. Under these threatening conditions, the LSI moves out 1 to 2mm so that it is above point B in Fig. 17. This condition of instability of the inverted meniscus is in a very narrow range of trough maniscus height, whereas the stable (concave) inverted meniscus does not apparently change over a wide range of trough meniscus positions. We have coated SOC at 10-, 15-, and 20-degrees tilt angles, but mostly at 20 degrees. It is not obvious at this time which is the optimal angle. It should be noted that the above observations are in complete agreement with the calculated shapes given in Quarterly Report No. 13 (January, 1980).

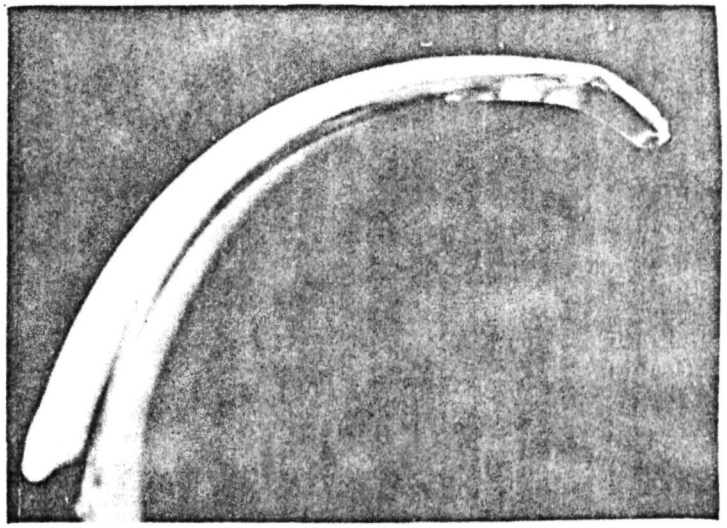
Safety Considerations -- The viewing ports on SCIM-II have been fitted with externally mounted metallized windows to prevent inadvertant eye damage. These also relieve the operator or observer of the bother of wearing welders' goggles. This not only saves one from looking in without eye protection, but also allows the operator more freedom to do the coating well. The external fitting of the metallized window allows swinging it away for room temperature viewing during loading or internal component alignment when the system is cold.

Impure Carbon Elements -- Heating the quartz trough with nonpurified carbon heaters shortens the life of the quartz dramatically. The impure carbon is not intended as a long-term condition from the viewpoint of melt contamination; however, purity is also important to maintain the life of the quartz. The cross-sectional views shown in Fig. 18(a), (b), and (c) show the attack of the quartz by the calcium driven from the carbon. An EDAX trace of the devitrified quartz shows the calcium in Fig. 18(d). Note the vitreous portions of the quartz that were not in contact with the heater; i.e., both the lips (close up in Fig. 18(b) and the central piece in the bottom corresponding to the center cut in the trough heater (close up in Fig. 18(c)).

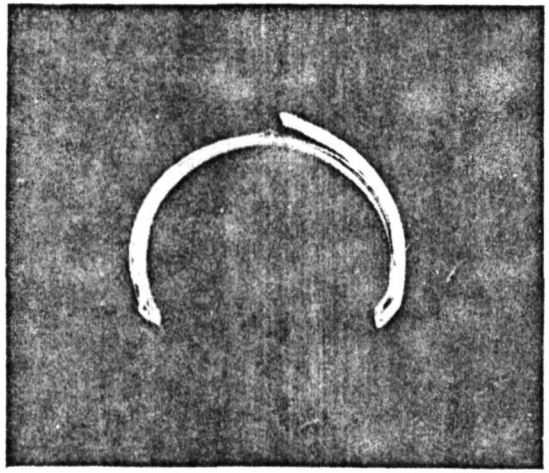
Coating Results on Slotted Substrates -- SOC layers on 10-cm x 100-cm solid substrates were produced late in September. A portion of a 10-cm x 100-cm fully slotted sample that was SCIM-coated was delivered in October. The fully-slotted substrate design is quite fragile without the silicon, so a more realistic design ($\sim$ 30% hole area instead of 40%) has been ordered that will fulfill our goals of slotted substrates as well as getting them out in one piece. Dentritic crystal growth along the entire length exists on many



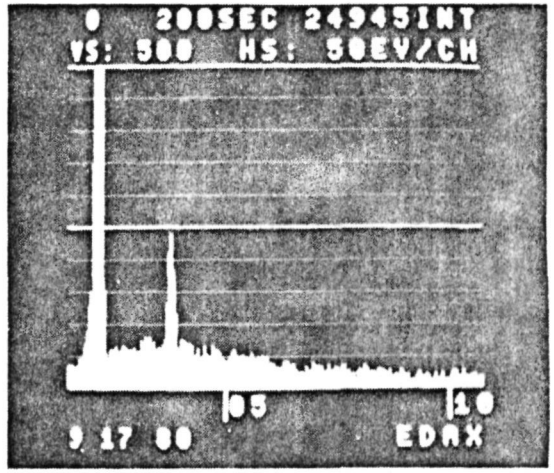
(a) ABOVE-HEATER CUT



(b) TIP OUT OF HEATER



(c) CROSS SECTION



(d) EDAX: CALCIUM AND SILICON

Figure 18. Cross section of quartz trough after 16-hour run.

samples. The driving mechanism is not yet known, but in one instance, blowing on the inverted meniscus with a turbulent argon flow smoothed out the dendritic growth. When the flow was interrupted, the dendritic growth did not immediately resume, so the correlation is still weak. Samples with dimensions 5 x 50 cm have been coated as well as 5 cm x 100 cm. The shorter samples are accommodated by a thin carbon piece slotted to fit the ends of the short sample and a meter-long sample that follows it as a "pusher." Any number of short samples can be coated as long as the last one is a meter long. The coating process is simply interrupted by lowering the trough assembly and breaking the meniscus. As soon as the attaching piece has passed the trough, the meniscus is raised again to contact the following substrate. It is not necessary to change the trough meniscus height to do this, since the displacer mechanism maintains its position relative to the crucible when the trough position is changed. Some slotted 5-cm-wide substrates have been coated with results similar to the 10-cm-wide samples in that the coating is not yet smooth and continuous along the entire length of the sample. Some of the slotted areas have been coated with 250 μm thick.

The foremost impediment to thick, uniform coatings is the transverse temperature gradient in the melt. The most obvious problem with a transverse gradient would be nonuniform thickness across the SOC and this is indeed observed. However, a more difficult situation has developed, in which the trough can freeze shut during operation. The reason is that between the crucible and the coating area there is a 3-cm length of trough heater (and quartz trough) that performs a bridge - the space between the crucible and the coater. This span has the greatest heat loss and is therefore subject to freeze-up when the coater is operated near minimum coating temperature. This freeze-up no only limits the supply of silicon from the crucible/displacer area, but it also propagates crystal growth along the trough due to the increased cooling from the higher-emissivity solidified silicon. Plans are to shape the heater and improve the insulation in that area.

DIP-COATING (K.D. McHenry, D.J. Sauve, and O.V. Harris)

During 1980, the main objectives of the dip-coating effort were to:

1) Provide material for solar-cell fabrication at Honeywell
2) Provide material for evaluation by JPL
3) Identify problems or potential problems and solutions associated with the yield in the supported growth of silicon.

As a result of objective No. 3, some experimetal dip-coating was performed in 1980 in addition to the normal dip-coating production efforts associated with objectives 1 and 2. All experimental runs were performed in the experimental dip-coater, while production runs have been performed in both dip-coaters.

Production runs for third quarter 1980 are summarized in Table 2. A total of 70 production-oriented runs were performed this year. Previous quarterly reports contain tables summarizing earlier runs. In Table 2, runs 256 through 258 were performed on the production dip-coater and runs 474 through 495 were performed on the experimental dip-coater.

During the past year, the ceramic substrate has been standardized to Type "O" material. This material, supplied by the Coors Porcelain Co., has a superior thermal shock resistance to those of materials tried previously. In addition, the thermal expansion coefficient of the Type "O" mullite appears to be more closely matched to that of silicon and the substrates do not warp too severely.

The dip-coating effort has also demonstrated or implemented several features during the past year. These include:

1) The use of a carbon afterheater to minimize thermal shock of the ceramic substrates during growth at high speeds
2) The feasibility of a system whereby granular silicon could be fed into the crucible to replenish the melt as the run progresses
3) The possibility that dendritic formation of silicon may be related to SiO contamination of the carbon-coated ceramic substrate prior to dipping.

Table 2. Dip-coating runs during the past quarter.

Run No.	Number Dipped	Comments
257	18	44% yield - dendritic growth.
258	15	40% yield - dendritic growth.
474	15	53% yield - new crucible support.
475	14	
476	19	New dip sequence attempted. See Monthly Progress Report No. 40.
477	16	63% yield using new sequence.
478	18	75% yield - some open slots.
479	4	Substrate broke and froze in melt.
480	11	Experimental - cooling shoe (He) and after-heater.
481	2	Substrate broke, fell in and splashed silicon onto heater.
482	10	Experimental - similar to run 480.
483	0	Erratic control of new heater.
484	8	Sample fell into melt.
485	6	50% yield.
486	15	
487	6	Experimental gas environment using Ar/H_2 (approx. 25% H_2).
488	12	Experimental gas environment using $Ar/CO_2/CO$. Noticeable "scum" formation on melt surface.
489	11	Experimental gas environment using $Ar/CO_2/CO$. Noticeable "scum" formation on melt surface.
490	8	Specimen broke and fell in melt.
491	12	Production run.
492	16	Production run.
493	17	Production run.
494	6	Production run - sample fell into melt.
495	12	Production run - sample fell into melt.

*All SOC substrates were grown at 3.60 cm/min and were boron-doped at $5 \times 10^{16}/cm^3$.

CELL FABRICATION AND DEVELOPMENT (B. Grung, T. Heisler, and S. Znameroski)

During this year, we fabricated approximately 250 solar cells from dip-coated SOC material. The best cell has a total-area conversion efficiency of 10.5% (AM1, AR), for a cell area of 5 cm^2. For 74 recent AR-coated cells, the average efficiency was 9.6%, with a standard deviation of 0.5%.

Tables 3 and 4 give the primary cell characteristics for 74 recent AR-coated cells, which will be called the 1980 baseline cells. All cells have a base doping concentration of 5 x $10^{16}/cm^3$ and a silicon thickness of approximately 250 μm. The current-voltage characteristics of the 10.5% cell are shown in Figs. 19 and 20. Before AR-coating, the cell had an efficiency of 7.58% and a fill-factor of 0.772. With the initial AR coating, the efficiency increased to 10.21% and the fill-factor decreased to 0.731. This decrease indicated that the AR-coating was shunting the cell. After baking the coating, the efficiency increased to 10.26% and the fill-factor increased to 0.752. At this point, the initial AR coating was deposited. Figure 20 shows that the resulting efficiency was 10.48%.

The cell information given in Table 4 is displayed graphically in Figs. 21 and 22. Figure 21 contains four distribution graphs for conditions before AR coating. The upper left-hand graph is for the open-circuit voltage, V_{oc}, and the others are for the fill-factor, FF, the short-circuit current density, J_{sc}, and the conversion efficiency, η. Figure 22 contains four similar graphs for conditions after AR coating. As can be seen, the average efficiency of the AR-coated cells is 9.6%, with a standard deviation of 0.5%.

The following three subsections discuss: (1) the optimum diffusion conditions, (2) variations in processing, and (3) modeling. The most important results of these subsections can be summarized as follows:

First, the highest cell efficiencies are obtained at a diffusion temperature of 850°C for 80 minutes. The diffusion cycle is divided into a 10-minute preheat time, a 60-minute source time and a 10-minute postheat. Second, the cell performance is significantly improved by using a slow-cooldown after the phosphorus diffusion. A cooling rate of approximately 5°C/min is used. Finally, the theoretical modeling indicates that the base diffusion length must be increased from approximately 25 μm to approximately 50 μm to increase substantially the conversion efficiencies of SOC cells.

Table 3. Conversion efficiencies of the 1980 baseline SOC cells.

item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/[])	Total Area Conversion Efficiencies Before AR (%)	After AR (%)	
1	226 - 3-111	4.7e+016	0.06	0.7	24.0	6.45	9.28	
2	226 - 3-211	4.7e+016	0.06	0.8	24.0	6.93	9.62	
3	238 - 8-111	5.0e+016	0.06	1.0	29.0	6.95	9.56	
4	238 - 8-211	5.0e+016	0.06	0.8	29.0	5.95	8.51	
5	241 - 4-111	5.0e+016	0.06	0.7	29.0	6.40	8.77	
6	241 - 4-211	5.0e+016	0.06	0.8	29.0	5.57	8.17	
7	244 - 3-111	5.0e+016	0.06	0.6	18.0	5.73	8.40	
8	244 - 3-211	5.0e+016	0.06	0.8	18.0	7.15	9.75	
9	244 -11-111	5.0e+016	0.06	0.7	22.0	6.03	8.43	
10	244 -11-211	5.0e+016	0.06	0.8	22.0	7.08	9.79	
11	244 -12-111	5.0e+016	0.06	0.7	21.0	6.70	9.42	
12	244 -12-211	5.0e+016	0.06	0.8	21.0	5.71	8.50	
13	248 - 1-111	5.0e+016	0.06	0.6	25.0	5.92	8.61	
14	248 - 1-211	5.0e+016	0.06	0.8	25.0	6.82	9.62	
15	248 - 2-111	5.0e+016	0.06	0.7	24.0	6.71	9.42	
16	248 - 2-211	5.0e+016	0.06	1.0	24.0	3.93	6.60	
17	248 - 4-111	5.0e+016	0.06	0.7	30.0	6.81	9.41	
18	248 - 4-211	5.0e+016	0.06	0.9	30.0	7.02	9.94	
19	249 - 7-111	5.0e+016	0.06	0.7	20.0	7.07	10.07	
20	249 - 7-211	5.0e+016	0.06	0.8	20.0	5.24	8.39	
21	251 - 3-111	5.0e+016	0.06	0.9	15.0	7.06	9.90	
22	251 - 3-211	5.0e+016	0.06	0.9	15.0	6.28	9.12	
23	251 - 8-111	5.0e+016	0.06	0.8	21.0	6.48	9.26	
24	251 - 8-211	5.0e+016	0.06	0.7	21.0	6.81	9.78	
25	252 - 3-111	5.0e+016	0.06	0.8	14.0	6.89	9.56	
26	252 - 3-211	5.0e+016	0.06	0.7	14.0	6.61	9.78	
27	252 - 4-111	5.0e+016	0.06	0.8	19.0	6.92	9.87	
28	252 - 4-211	5.0e+016	0.06	0.9	19.0	7.06	9.96	
29	252 - 6-111	5.0e+016	0.06	0.7	21.0	7.11	9.80	
30	252 - 6-211	5.0e+016	0.06	0.7	21.0	7.26	10.12	
31	252 - 7-111	5.0e+016	0.06	0.6	25.0	7.00	9.96	
32	252 - 7-211	5.0e+016	0.06	0.7	25.0	6.59	9.48	
33	252 - 9-111	5.0e+016	0.06	0.8	19.0	7.05	9.80	
34	252 - 9-211	5.0e+016	0.06	0.9	19.0	7.16	10.22	
35	253 - 3-111	5.0e+016	0.06	0.7	18.0	7.22	10.42	
36	253 - 3-211	5.0e+016	0.06	0.7	18.0	7.17	10.38	
37	253 - 4-111	5.0e+016	0.06	0.8	22.0	7.19	9.97	
38	253 - 4-211	5.0e+016	0.06	1.0	22.0	7.22	9.82	
39	254 - 1-111	5.0e+016	0.06	1.4	21.0	6.62	9.15	
40	254 - 1-211	5.0e+016	0.06	0.6	21.0	6.92	9.97	
41	254 - 6-111	5.0e+016	0.06	0.7	21.0	6.78	10.19	
42	254 - 6-211	5.0e+016	0.06	0.7	21.0	6.98	10.11	
43	254 - 9-111	5.0e+016	0.06	0.6	26.0	7.08	10.03	
44	254 - 9-211	5.0e+016	0.06	0.6	26.0	6.85	9.96	
45	255 - 2-111	5.0e+016	0.06	0.6	21.0	6.90	9.58	
46	255 - 2-211	5.0e+016	0.06	0.6	21.0	7.09	9.82	
47	255 - 5-111	5.0e+016	0.06	0.6	22.0	7.08	9.87	
48	255 - 5-211	5.0e+016	0.06	0.7	22.0	7.58	10.21	(10.5%)*
49	255 - 7-111	5.0e+016	0.06	0.6	27.0	6.97	9.91	

*See text and Figures 19 and 20.

Table 3. Conversion efficiencies of the 1980 baseline SOC cells (concluded).

Item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/[])	Total Area Conversion Efficiencies Before AR (%)	After AR (%)
50	255 - 7-211	5.0e+016	0.06	0.7	27.0	6.92	10.03
51	256 - 6-111	5.0e+016	0.06	1.3	52.0	6.92	9.77
52	256 - 6-211	5.0e+016	0.06	1.4	52.0	7.00	9.90
53	257 -13-111	5.0e+016	0.06	0.9	29.0	6.70	9.64
54	257 -13-211	5.0e+016	0.06	1.6	29.0	6.80	9.35
55	258 - 7-111	5.0e+016	0.06	0.9	22.0	6.94	9.52
56	258 - 7-211	5.0e+016	0.06	0.7	22.0	7.16	10.13
57	258 - 8-111	5.0e+016	0.06	1.1	35.0	6.78	9.76
58	258 -12-111	5.0e+016	0.06	0.9	36.0	6.67	9.58
59	258 -12-211	5.0e+016	0.06	1.0	36.0	6.37	9.13
60	473 - 7-211	5.0e+016	0.06	0.8	30.0	7.14	9.82
61	474 - 8-111	5.0e+016	0.06	0.8	23.0	7.10	9.88
62	474 - 8-211	5.0e+016	0.06	0.9	23.0	6.87	9.58
63	474 -10-111	5.0e+016	0.06	1.0	27.0	6.92	9.60
64	474 -10-211	5.0e+016	0.06	1.2	27.0	6.73	9.52
65	474 -11-111	5.0e+016	0.06	0.7	31.0	7.02	10.20
66	474 -11-211	5.0e+016	0.06	0.8	31.0	6.79	9.64
67	475 - 5-111	5.0e+016	0.06	1.5	31.0	6.97	9.73
68	475 - 5-211	5.0e+016	0.06	1.2	31.0	7.36	10.10
69	477 - 7-111	5.0e+016	0.06	0.9	46.0	6.89	9.47
70	477 - 7-211	5.0e+016	0.06	0.9	46.0	6.88	9.33
71	477 -11-111	5.0e+016	0.06	0.9	37.0	6.85	9.75
72	477 -11-211	5.0e+016	0.06	0.9	37.0	7.21	9.86
73	478 -11-111	5.0e+016	0.06	0.9	29.0	6.59	9.72
74	478 -11-211	5.0e+016	0.06	0.8	29.0	6.98	9.86

Table 4. Characteristics of recent AR-coated SOC cells.

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)	
1	226 - 3-111-0	80.40	0.551	0.728	16.08	6.45	
1	226 - 3-111-1	114.80	0.570	0.709	22.96	9.28	(AR)
2	226 - 3-211-0	83.70	0.554	0.747	16.74	6.93	
2	226 - 3-211-1	117.30	0.570	0.719	23.46	9.62	(AR)
3	238 - 8-111-0	82.60	0.556	0.757	16.52	6.95	
3	238 - 8-111-1	114.10	0.570	0.735	22.82	9.56	(AR)
4	238 - 8-211-0	82.10	0.546	0.664	16.42	5.95	
4	238 - 8-211-1	114.20	0.560	0.665	22.84	8.51	(AR)
5	241 - 4-111-0	78.40	0.554	0.737	15.68	6.40	
5	241 - 4-111-1	107.40	0.566	0.721	21.48	8.77	(AR)
6	241 - 4-211-0	77.70	0.536	0.669	15.54	5.57	
6	241 - 4-211-1	110.00	0.551	0.674	22.00	8.17	(AR)
7	244 - 3-111-0	81.50	0.552	0.673	16.30	5.73	
7	244 - 3-111-1	114.20	0.559	0.658	22.84	8.40	(AR)
8	244 - 3-211-0	82.30	0.563	0.772	16.46	7.15	
8	244 - 3-211-1	114.90	0.565	0.751	22.98	9.75	(AR)
9	244 -11-111-0	81.60	0.557	0.663	16.32	6.03	
9	244 -11-111-1	110.70	0.568	0.670	22.14	8.43	(AR)
10	244 -11-211-0	83.00	0.562	0.759	16.60	7.08	
10	244 -11-211-1	113.60	0.572	0.753	22.72	9.79	(AR)
11	244 -12-111-0	79.60	0.560	0.752	15.92	6.70	
11	244 -12-111-1	117.20	0.565	0.711	23.44	9.42	(AR)
12	244 -12-211-0	81.10	0.552	0.638	16.22	5.71	
12	244 -12-211-1	117.90	0.560	0.644	23.58	8.50	(AR)
13	248 - 1-111-0	81.00	0.546	0.669	16.20	5.92	
13	248 - 1-111-1	111.20	0.561	0.690	22.24	8.61	(AR)
14	248 - 1-211-0	82.40	0.550	0.753	16.48	6.82	
14	248 - 1-211-1	113.90	0.567	0.745	22.78	9.62	(AR)
15	248 - 2-111-0	79.40	0.556	0.760	15.88	6.71	
15	248 - 2-111-1	115.50	0.568	0.718	23.10	9.42	(AR)
16	248 - 2-211-0	79.60	0.526	0.469	15.92	3.93	
16	248 - 2-211-1	116.50	0.548	0.517	23.30	6.60	(AR)
17	248 - 4-111-0	81.30	0.550	0.761	16.26	6.81	
17	248 - 4-111-1	111.50	0.563	0.750	22.30	9.41	(AR)
18	248 - 4-211-0	83.50	0.552	0.761	16.70	7.02	
18	248 - 4-211-1	115.80	0.566	0.758	23.16	9.94	(AR)
19	249 - 7-111-0	84.10	0.560	0.753	16.82	7.07	
19	249 - 7-111-1	121.10	0.575	0.723	24.22	10.07	(AR)

Table 4. Characteristics of recent AR-coated SOC cells (continued).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)	
20	249 - 7-211-0	78.50	0.540	0.618	15.70	5.24	
20	249 - 7-211-1	120.00	0.560	0.624	24.00	8.39	(AR)
21	251 - 3-111-0	84.40	0.566	0.739	16.88	7.06	
21	251 - 3-111-1	120.20	0.575	0.716	24.04	9.90	(AR)
22	251 - 3-211-0	84.80	0.560	0.661	16.96	6.28	
22	251 - 3-211-1	121.10	0.570	0.661	24.22	9.12	(AR)
23	251 - 8-111-0	80.00	0.564	0.718	16.00	6.48	
23	251 - 8-111-1	120.40	0.568	0.677	24.08	9.26	(AR)
24	251 - 8-211-0	81.60	0.563	0.741	16.32	6.81	
24	251 - 8-211-1	122.70	0.567	0.703	24.54	9.78	(AR)
25	252 - 3-111-0	80.20	0.566	0.759	16.04	6.89	
25	252 - 3-111-1	117.30	0.572	0.713	23.44	9.56	(AR)
26	252 - 3-211-0	80.10	0.562	0.734	16.02	6.61	
26	252 - 3-211-1	120.20	0.570	0.714	24.04	9.78	(AR)
27	252 - 4-111-0	82.30	0.569	0.739	16.46	6.92	
27	252 - 4-111-1	118.40	0.575	0.725	23.68	9.87	(AR)
28	252 - 4-211-0	82.90	0.565	0.754	16.48	7.06	
28	252 - 4-211-1	120.10	0.571	0.726	24.02	9.96	(AR)
29	252 - 6-111-0	83.50	0.569	0.748	16.70	7.11	
29	252 - 6-111-1	119.50	0.579	0.708	23.90	9.80	(AR)
30	252 - 6-211-0	83.80	0.567	0.764	16.76	7.26	
30	252 - 6-211-1	119.40	0.578	0.733	23.88	10.12	(AR)
31	252 - 7-111-0	80.70	0.566	0.767	16.14	7.00	
31	252 - 7-111-1	120.50	0.577	0.716	24.10	9.96	(AR)
32	252 - 7-211-0	80.20	0.558	0.736	16.04	6.59	
32	252 - 7-211-1	120.00	0.570	0.693	24.00	9.48	(AR)
33	252 - 9-111-0	82.60	0.570	0.749	16.52	7.05	
33	252 - 9-111-1	116.20	0.580	0.727	23.24	9.80	(AR)
34	252 - 9-211-0	83.60	0.570	0.751	16.72	7.16	
34	252 - 9-211-1	122.30	0.578	0.723	24.46	10.22	(AR)
35	253 - 3-111-0	84.80	0.565	0.754	16.96	7.22	
35	253 - 3-111-1	123.60	0.573	0.736	24.72	10.42	(AR)
36	253 - 3-211-0	84.80	0.564	0.750	16.96	7.17	
36	253 - 3-211-1	125.10	0.572	0.725	25.02	10.38	(AR)
37	253 - 4-111-0	84.30	0.563	0.757	16.86	7.19	
37	253 - 4-111-1	119.10	0.578	0.724	23.82	9.97	(AR)

Table 4. Characteristics of recent AR-coated SOC cells (continued).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)	
38	253 - 4-211-0	84.80	0.560	0.760	16.96	7.22	
38	253 - 4-211-1	121.10	0.574	0.706	24.22	9.82	(AR)
39	254 - 1-111-0	80.30	0.560	0.736	16.06	6.62	
39	254 - 1-111-1	118.20	0.569	0.680	23.64	9.15	(AR)
40	254 - 1-211-0	79.00	0.563	0.778	15.80	6.92	
40	254 - 1-211-1	119.10	0.570	0.734	23.82	9.97	(AR)
41	254 - 6-111-0	83.40	0.564	0.721	16.68	6.78	
41	254 - 6-111-1	119.40	0.572	0.746	23.88	10.19	(AR)
42	254 - 6-211-0	81.40	0.562	0.763	16.28	6.98	
42	254 - 6-211-1	117.40	0.567	0.760	23.48	10.11	(AR)
43	254 - 9-111-0	82.70	0.565	0.758	16.54	7.08	
43	254 - 9-111-1	117.90	0.580	0.733	23.58	10.03	(AR)
44	254 - 9-211-0	80.90	0.561	0.755	16.18	6.85	
44	254 - 9-211-1	119.30	0.575	0.726	23.86	9.96	(AR)
45	255 - 2-111-0	80.20	0.564	0.763	16.04	6.90	
45	255 - 2-111-1	112.80	0.573	0.741	22.56	9.58	(AR)
46	255 - 2-211-0	82.80	0.565	0.758	16.56	7.09	
46	255 - 2-211-1	114.70	0.573	0.747	22.94	9.82	(AR)
47	255 - 5-111-0	82.30	0.569	0.756	16.46	7.08	
47	255 - 5-111-1	119.50	0.575	0.718	23.90	9.87	(AR)
48	255 - 5-211-0	86.00	0.571	0.772	17.20	7.58	
48	255 - 5-211-1	120.60	0.579	0.731	24.12	10.21	(AR) (10.5%)*
49	255 - 7-111-0	81.70	0.565	0.755	16.34	6.97	
49	255 - 7-111-1	116.50	0.571	0.745	23.30	9.91	(AR)
50	255 - 7-211-0	82.10	0.563	0.748	16.42	6.92	
50	255 - 7-211-1	116.70	0.573	0.750	23.34	10.03	(AR)
51	256 - 6-111-0	86.00	0.561	0.717	17.20	6.92	
51	256 - 6-111-1	126.10	0.574	0.675	25.22	9.77	(AR)
52	256 - 6-211-0	87.80	0.557	0.716	17.56	7.00	
52	256 - 6-211-1	125.70	0.573	0.687	25.14	9.90	(AR)
53	257 -13-111-0	83.50	0.551	0.732	16.70	6.70	
53	257 -13-111-1	116.10	0.563	0.737	23.22	9.64	(AR)
54	257 -13-211-0	85.40	0.551	0.723	17.08	6.80	
54	257 -13-211-1	117.30	0.563	0.708	23.46	9.35	(AR)
55	258 - 7-111-0	83.00	0.560	0.746	16.60	6.94	
55	258 - 7-111-1	117.00	0.569	0.715	23.40	9.52	(AR)

*See text and Figures 19 and 20.

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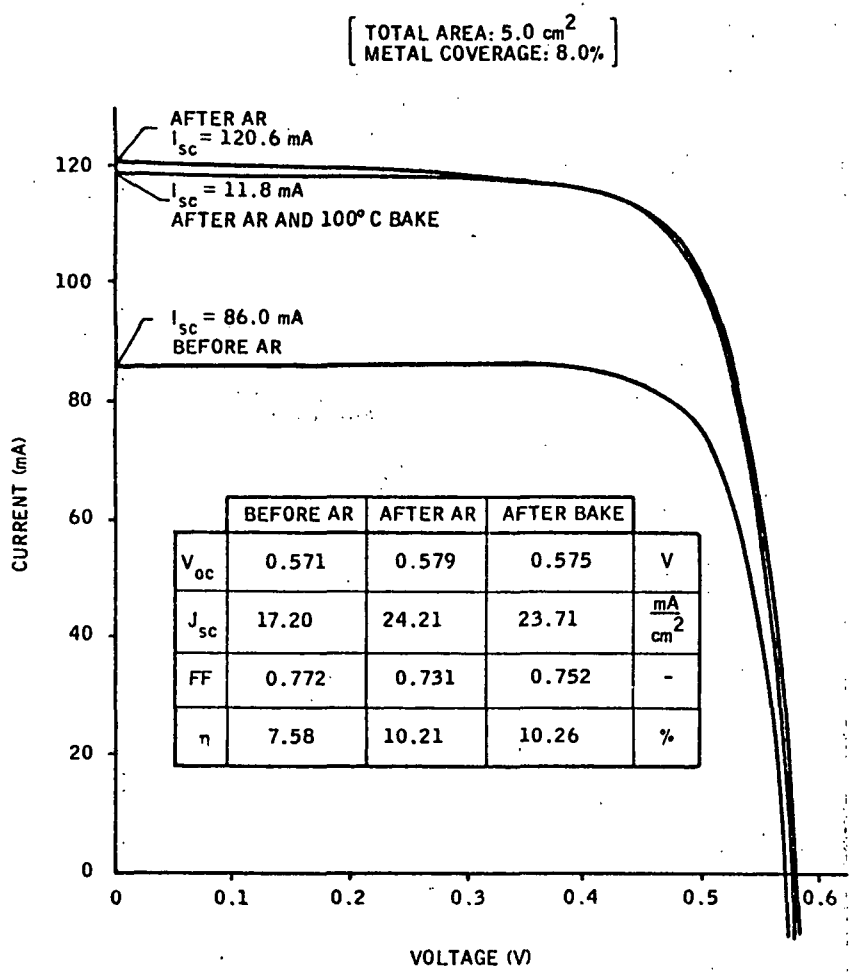
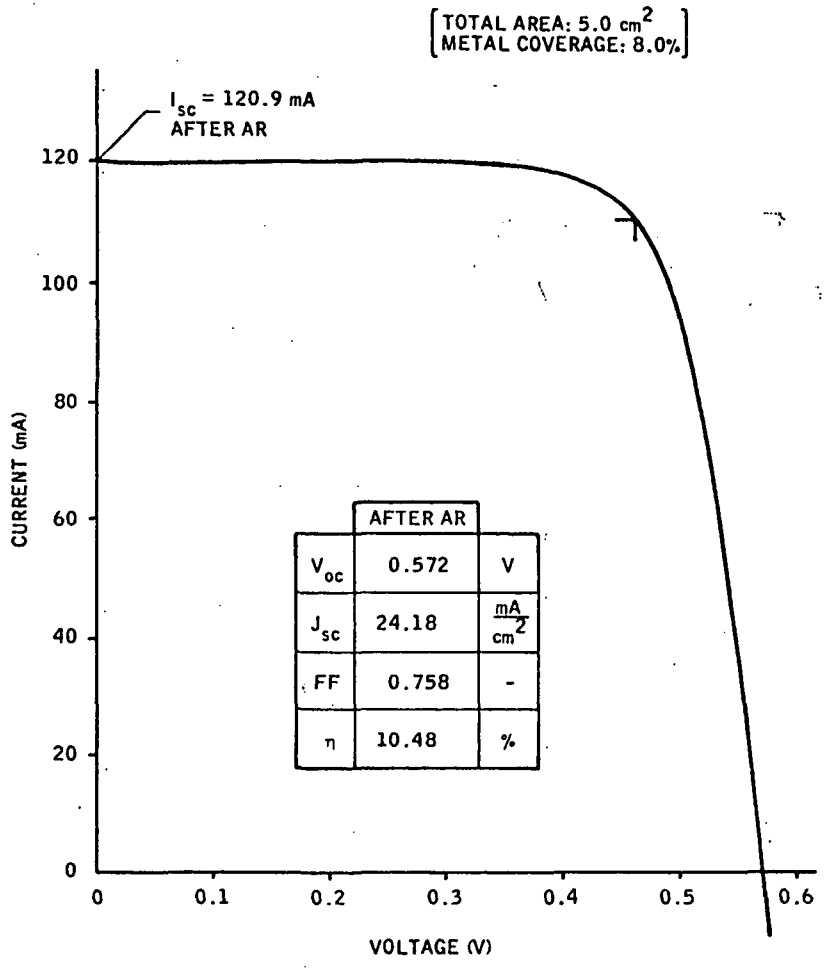
Table 4. Characteristics of recent AR-coated SOC cells (concluded).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff (%)	
56	258 - 7-211-0	84.00	0.561	0.760	16.80	7.16	
56	258 - 7-211-1	117.10	0.570	0.759	23.42	10.13	(AR)
57	258 - 8-111-0	83.50	0.560	0.725	16.70	6.78	
57	258 - 8-111-1	119.40	0.571	0.716	23.88	9.76	(AR)
58	258 -12-111-0	85.00	0.555	0.707	17.00	6.67	
58	258 -12-111-1	119.30	0.567	0.708	23.86	9.58	(AR)
59	258 -12-211-0	84.00	0.549	0.691	16.80	6.37	
59	258 -12-211-1	118.00	0.559	0.692	23.60	9.13	(AR)
60	473 - 7-211-0	85.10	0.563	0.745	17.02	7.14	
60	473 - 7-211-1	121.20	0.574	0.706	24.24	9.82	(AR)
61	474 - 8-111-0	83.60	0.565	0.752	16.72	7.10	
61	474 - 8-111-1	120.80	0.569	0.719	24.16	9.88	(AR)
62	474 - 8-211-0	81.30	0.561	0.753	16.26	6.87	
62	474 - 8-211-1	119.70	0.565	0.708	23.94	9.58	(AR)
63	474 -10-111-0	82.10	0.560	0.752	16.42	6.92	
63	474 -10-111-1	119.70	0.568	0.706	23.94	9.60	(AR)
64	474 -10-211-0	82.50	0.559	0.730	16.50	6.73	
64	474 -10-211-1	120.30	0.569	0.695	24.06	9.52	(AR)
65	474 -11-111-0	82.10	0.562	0.761	16.42	7.02	
65	474 -11-111-1	116.50	0.573	0.764	23.30	10.20	(AR)
66	474 -11-211-0	80.10	0.559	0.758	16.02	6.79	
66	474 -11-211-1	114.30	0.570	0.749	22.86	9.64	(AR)
67	475 - 5-111-0	87.10	0.564	0.709	17.42	6.97	
67	475 - 5-111-1	119.50	0.575	0.708	23.90	9.73	(AR)
68	475 - 5-211-0	86.50	0.568	0.749	17.30	7.36	
68	475 - 5-211-1	121.10	0.574	0.726	24.22	10.10	(AR)
69	477 - 7-111-0	82.30	0.558	0.750	16.46	6.89	
69	477 - 7-111-1	113.60	0.564	0.739	22.72	9.47	(AR)
70	477 - 7-211-0	84.50	0.558	0.729	16.90	6.88	
70	477 - 7-211-1	114.30	0.563	0.725	22.86	9.33	(AR)
71	477 -11-111-0	82.80	0.557	0.743	16.56	6.85	
71	477 -11-111-1	118.70	0.571	0.719	23.74	9.75	(AR)
72	477 -11-211-0	85.90	0.557	0.753	17.18	7.21	
72	477 -11-211-1	121.00	0.570	0.715	24.20	9.86	(AR)
73	478 -11-111-0	81.90	0.555	0.725	16.38	6.59	
73	478 -11-111-1	116.20	0.570	0.734	23.24	9.72	(AR)
74	478 -11-211-0	82.90	0.559	0.753	16.58	6.98	
74	478 -11-211-1	117.00	0.568	0.742	23.40	9.86	(AR)



	BEFORE AR	AFTER AR	AFTER BAKE	
V_{oc}	0.571	0.579	0.575	V
J_{sc}	17.20	24.21	23.71	$\frac{mA}{cm^2}$
FF	0.772	0.731	0.752	-
η	7.58	10.21	10.26	%

Figure 19.
Current-voltage characteristics of SOC cell No. 255-5-211. The lower curve corresponds to measurements before AR coating; the upper two curves, to measurements after AR coating.



	AFTER AR	
V_{oc}	0.572	V
J_{sc}	24.18	$\frac{mA}{cm^2}$
FF	0.758	-
η	10.48	%

Figure 20.
Current-voltage characteristics of the same cell as for Fig. 19. For this curve, the initial AR coating was removed and a new AR coating deposited.

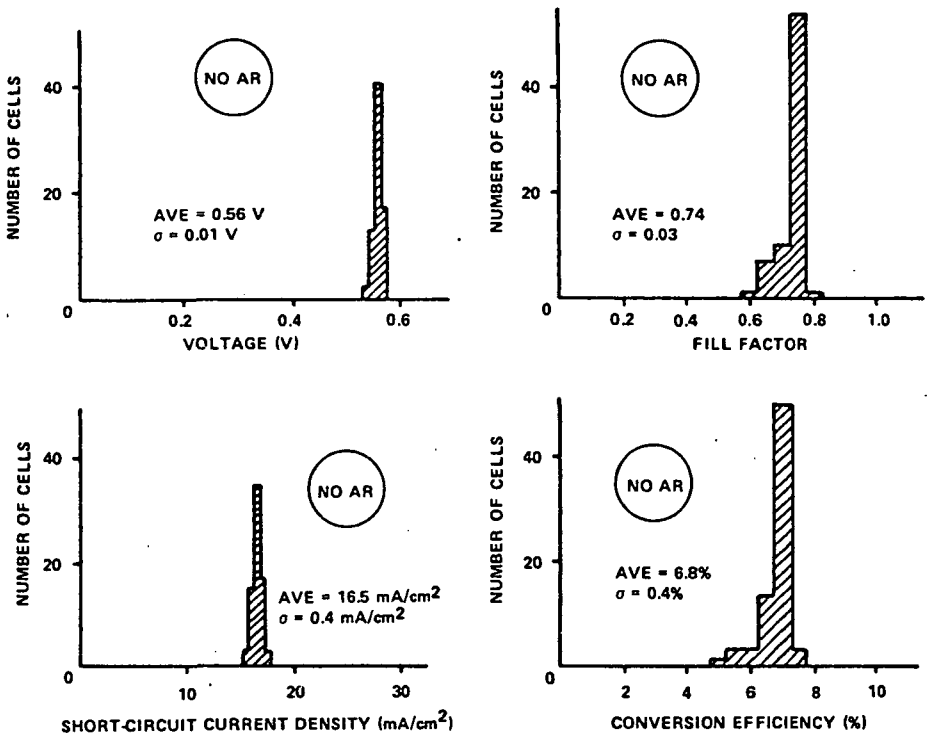


Figure 21. Distribution graphs for the 1980 baseline SOC cells for conditions before the AR coating.

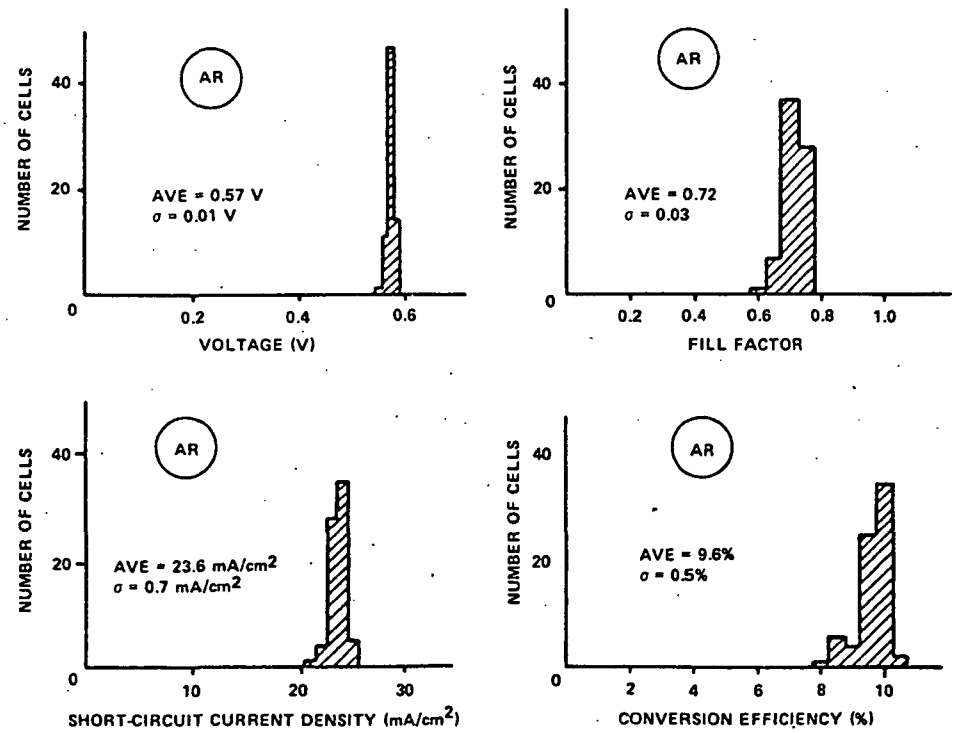


Figure 22. Distribution graphs for the 1980 baseline SOC cells for conditions after the AR coating.

Optimum Diffusion Conditions -- In Quarterly Report No. 13, results of experiments to determine the optimum diffusion conditions were reported. A total of 120 cells were fabricated using various diffusion conditions. Two figures were given, showing cell performance as a function of emitter sheet resistance. From these graphs, it was concluded that the optimum diffusion conditions were 850°C for 80 minutes. The present cell fabrication process uses these conditions, along with a slow cooldown after the phosphorus diffusion (see below).

Variation in Processing -- To improve cell performance, a number of experiments have been investigated and the principal ones are listed in Table 5. The major results of these experiments were discussed in Quarterly Reports No. 14 and 15. These results are summarized below, along with some more recent results:

1) Melt-Current Experiment -- Eight SOC cells were fabricated to determine the effect of an electric current through the melt during dip-coating. It was hoped that this current might reduce melt contamination by influencing the transport of impurities from the substrate into the melt. Based on the results of the eight cells, an electric current does not seem to have an effect on melt contamination.

2) No-Doping Experiment -- Four SOC cells were fabricated to determine the effects of progressive melt contamination on the sheet resistance of the dip-coated SOC material. For the ninth and twelfth substrates dipped in run no. 228, the sheet resistance was 770 and 550 ohms per square, respectively. Cells fabricated using these SOC substrates had efficiencies in the range from 4.3 to 6.1% (AM1, no AR). This indicates that the mullite progressively contaminated the melt with a p-type dopant, shown to be aluminum in earlier experiments. Such contamination is a basic problem for the dip-coating technique. A similar problem should not exist for the SCIM-coating technique, since the mullite will not be in direct contact with the silicon melt.

3) Aluminum-Doping Experiment -- Eleven SOC cells were fabricated to determine if aluminum doping could produce higher values of J_{sc}, for a given doping concentration. The highest J_{sc} is 14.68 mA/cm^2 (AM1, no AR) for an aluminum-doping concentration of

$2.2 \times 10^{16}/cm^3$. This value is low compared with an average value of 17 mA/cm^2 for boron-doped samples. Thus, aluminum doping does not seem to produce high values of J_{sc}.

4) Heavy-Doping Experiment -- Eight solar cells were fabricated using SOC material with a boron doping concentration of $10^{18}/cm^3$, as compared with the normal concentration of $5 \times 10^{16}/cm^3$. Our objective was to extend the experimental results given in Fig. 4 of Quarterly Report No. 14 in order to determine the upper limit for the base doping concentration. The fabricated cells were of poor quality and only the J_{sc} results were of value. The most interesting result was that the average J_{sc} was 19 mA/cm^2, as compared with 21 mA/cm^2, the value associated with the linear regression line given in Fig. 4 of the just-noted report. The 19 mA/cm^2 value indicates that Auger recombination begins to limit the performance of SOC cells for base doping concentrations greater than $10^{18}/cm^3$, as expected.

5) Carbon-Substrate Experiment -- Several carbon substrates were dipped first in a run in order to learn more about melt contamination from the ceramic substrate. We had planned to make photodiodes on the resulting silicon layers and to compare the performance of these diodes with the performance of corresponding diodes on SOC material. Unfortunately, the grain structure of the silicon layers on the carbon substrates was rather poor and, as a result, we did not complete this experiment.

6) Ion-Implant Experiment -- Eight SOC cells were fabricated using ion implantation and thermal anneal to form the n^+ emitter region. Arsenic was used as the dopant. For one set of SOC cells, the annealing temperature was $850^{\circ}C$ for 60 minutes. The emitter sheet resistance was approximately 32 ohms per square and the efficiency of one ion-implant/anneal cell was 5.6%, as compared with the 6.7% efficiency of a corresponding cell used for a control. More work needs to be done to determine the proper annealing conditions.

7) Hydrogenation Experiment -- Results for this experiment are discussed in the material evaluation sections of this report.

8) Two-Step Experiment -- Eighteen solar cells were fabricated to determine the effects of a two-step diffusion process. The best two-step cell had a total-area conversion efficiency of 10.26% (AM1, AR) for a cell area of 5 cm^2. For one group of cells, the two-step process was similar to the process described by DiStefano and Cuomo,[2] as well as by Lindmayer.[3] This two-step process basically is as follows: First, a low-temperature phosphorus diffusion is used to diffuse phosphorus atoms down grain boundaries using a spin-on diffusion source and diffusion conditions of 600°C for 60 minutes. Second, the initial diffusion source is then removed and the normal high-temperature phosphorus diffusion is used to form the p-n junction. For a second group of cells, the initial spin-on source was used for both the low- and high-temperature diffusion. For a third group, the order of the two diffusions was interchanged. The latter process seems to produce the highest efficiencies but more work must be done to determine if this is so.

9) Slow-Cooldown Experiment -- Twenty-seven SOC cells were fabricated using a slow cooldown after the phosphorus diffusion. Typically, the cooling rate was approximately 3°C/min from the diffusion temperature of 850°C to 700°C. The slow cooldown seems to produce a significant increase in cell performance.

10) Etching Experiment -- Nineteen cells were fabricated from SOC material that was etched before the phosphorus diffusion. The main idea is to determine if cell performance can be improved by removing impurities that segregate to the silicon surface during growth. Various etches have been used, including KOH etch, Sirtl etch, CP4 etch, and plasma etch. In all cases, we have removed approximately 3 μm of material from the surface of the SOC material. So far, none of the etches have produced a noticeable increase in cell performance.

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[2]DiStefano and Cuomo, Appl. Phys. Lett. 30, 351 (1977).

[3]Lindmayer, 13th IEEE Photovoltaic Specialist's Conf., p. 1096.

Table 5. Experiments for increasing cell performance.

Item	Experiment	Objectives	Results
1	Melt current	Reduce impurities.	No effect.
2	No doping	Determine rate of contamination.	Graph of ρ vs N.
3	Aluminum doping	Determine if aluminum doping improves J_{sc}.	Reduces J_{sc}.
4	Heavy doping	Determine effect of heavy doping.	Reduces J_{sc}.
5	Carbon substrate	Measure melt quality.	Poor structure.
6	Ion-implantation	Increase J_{sc}.	Preliminary results.
7	Hydrogenation	Increase J_{sc}.	Some improvements.
8	Two-step	Increase J_{sc}.	Some improvements.
9	Slow-cool	Increase J_{sc}.	Significant improvements.
10	Etching	Increase J_{sc}.	No improvements.

Modeling -- This subsection will be divided into two parts, one concerning empirical modeling and the other theoretical modeling. The objective of both parts is to increase our understanding of the SOC cell.

In Quarterly Report No. 14, we presented a figure showing cell performance as a function of the base doping concentration for the 1979 baseline cells. This figure, which is based on 136 SOC cells, is reproduced here as Fig. 23. The experimental results are indicated by the vertical lines; the calculated results, by the solid curves. These empirical curves can be calculated as follows: First, linear regression is used to determine a relationship between J_{sc} and N_B. The result is

$$J_{sc} = 1.48 \log \left(\frac{9.7 \times 10^{31}}{N_B} \right). \qquad (2)$$

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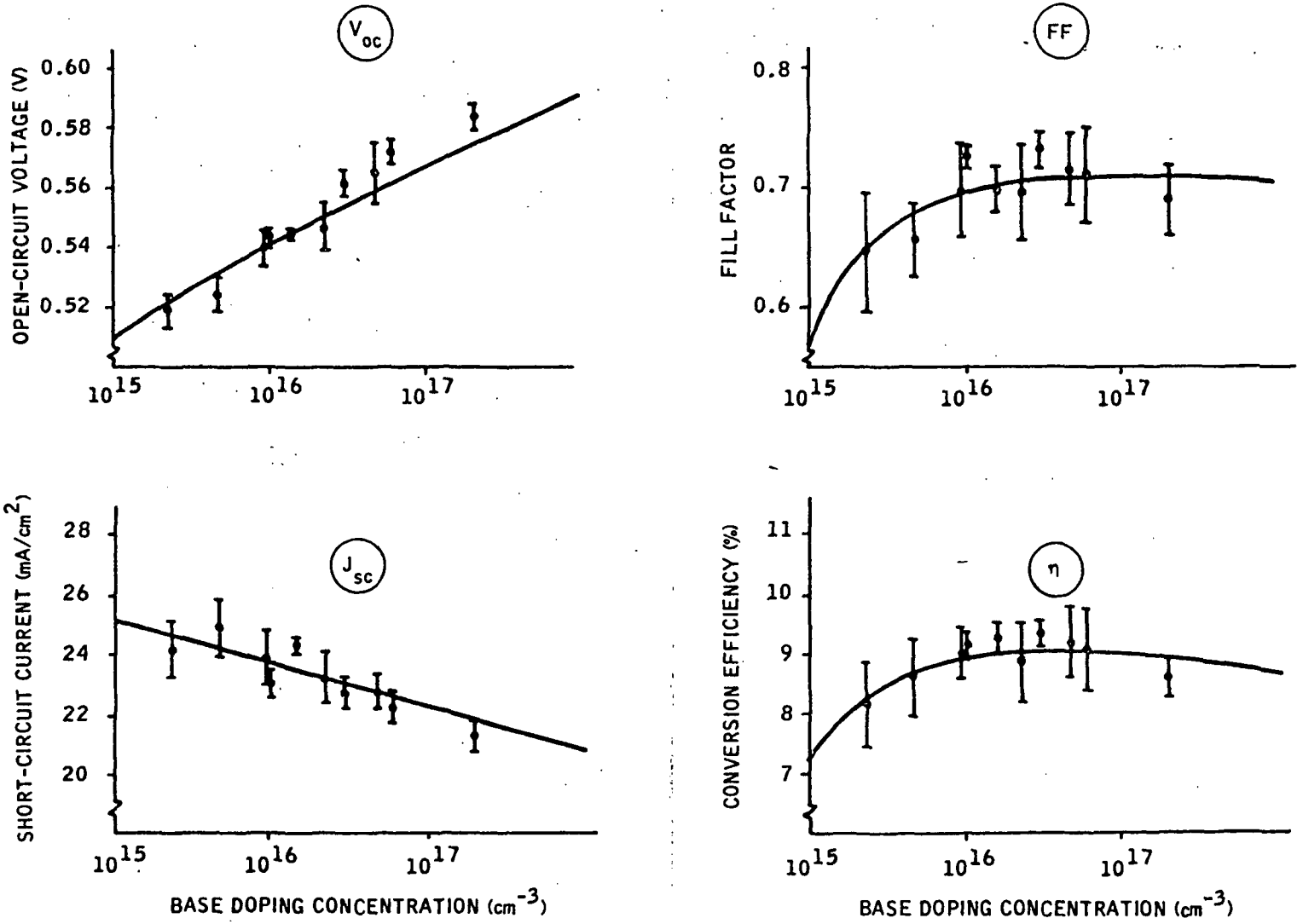

Figure 23. Cell performance as a function of base doping concentration, for the 1979 baseline cells, the characteristics of which were reported in Annual Report No. 4 and in Quarterly Report No. 14. Vertical lines are experiment results; solid curves are calculated results.

where J_{sc} is in units of mA/cm^2 and N_B is in units of cm^{-3}. Second, linear regression is used to determine an empirical relationship between J_{01} and N_B. For the data given in Table 4 of Monthly Report No. 34, the result is

$$J_{01} = \frac{9.6}{N_B^{0.54}} \tag{3}$$

where J_{01} is in units of mA/cm^2. Third, the theoretical expression for the specific series resistance, R_sA, as given in Quarterly Report No. 12, is used, with an empirical constant of 1.75 added to approximate the measured results. The resulting expression is

$$R_sA = 2.25 + \frac{3.35 \times 10^{15}}{N_B} \tag{4}$$

where R_sA is in units of ohm-cm^2. For Eq. (4), a growth velocity of 3.6 cm/min is assumed. Finally, the current density is assumed to be given by

$$J = J_{01}\left[\exp\frac{q(V - JR_sA)}{kT} - 1\right] + J_{02}\left[\exp\frac{q(V - JR_sA)}{nkT} - 1\right] + \left(\frac{V - JR_sA}{R_{sh}}\right) - J_{sc} \tag{5}$$

where J_{02} is 10^{-4} mA/cm^2 and n is 2. Equations (2) through (5) give the empirical curves of Fig. 23. Clearly, the empirical curves approximate the experimental result.

Now we turn from empirical modeling to theoretical modeling. Our objective is to understand more completely the performance limitations of SOC cells. In particular, we want to determine a relationship between the short-circuit current, J_{sc}, and the minority-carrier diffusion length, L_{nB}, assuming AM1 conditions.

To begin, we consider only generation in the base region and monochromatic light. These restrictions will be removed as we progress. Moreover, we will assume that the geometry is one-dimensional and that the effects of the grain boundaries can be neglected. In other words, we initially consider an SOC cell structure that approximates a one-dimensional, single-crystal cell structure having a base diffusion length corresponding to that of SOC material. The basic cell configuration is shown in Fig. 24, along with a

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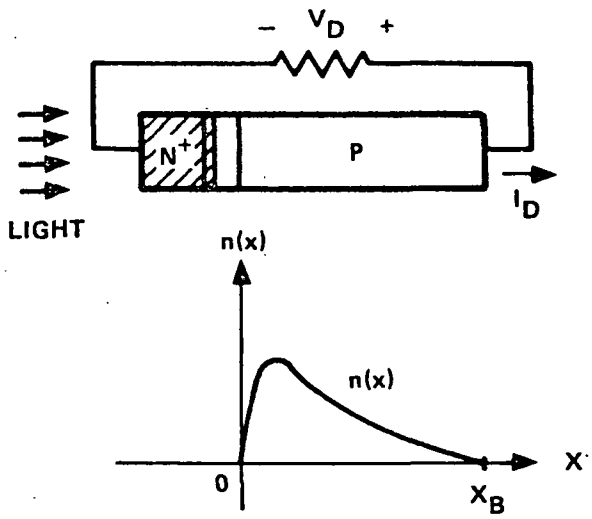

VALUES OF CONSTANTS

$N_{DE} = 10^{20}/cm^3$	$N_{AB} = 5 \times 10^{16}/cm^3$
$\frac{D_{pE}}{L_{pE}} = 2.3 \times 10^4$ cm/sec	$D_{nB} = 23.3$ cm^2/sec
$A = 1$ cm^2	$L_{nB} = 0.005$ cm
$q = 1.6 \times 10^{-19}$ coul	$X_B = 0.02$ cm
$n_i = 1.45 \times 10^{10}/cm^3$	$b_B = 3.06$
$kT/q = 0.0259$ V	

Figure 24. Solar cell configuration and values of constants used in the analysis. The distribution of minority carriers, n(x), is shown at the maximum power point.

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list of the various parameter values. A list of notation is given in Table 6. With the noted assumptions, conventional semiconductor theory yields the following five equations for low-level conditions:

$$p(0) = \frac{n_i^2}{N_{DE}} \exp \frac{q(-V_{jE})}{kT} \tag{6}$$

$$n(0) = \frac{n_i^2}{N_{AB}} \exp \frac{q(-V_{jE})}{kT} \tag{7}$$

$$V_D = -V_{jE} + R_S I_D \tag{8}$$

$$I_D = qA \frac{D_{pE}}{L_{pE}} p(0) + I_n(0) \tag{9}$$

$$I_n(0) = qAF(1 - R) \frac{\alpha L_{nB}}{(\alpha^2 L_{nB}^2 - 1)} \left\{ \alpha L_{nB} - \frac{\cosh(X_B/L_{nB}) - \exp(-\alpha X_B)}{\sinh(X_B/L_{nB})} \right\} - qA \frac{D_{nB}}{L_{nB}} n(0) \tag{10}$$

For monochromatic light having a wavelength of 0.882 μm, these equations given the I-V characteristics shown in Fig. 25. (Also shown are the corresponding I-V characteristics for AM1 light conditions, which will be discussed below.) For monochromatic light, the minority carrier profile in the base region is given by

$$\frac{n(x)}{N_{AB}} = \left\{ \frac{I_n(0)}{qA(D_{nB}/L_{nB})N_{AB}} - \alpha L_p Y \right\} \sinh \left(\frac{x}{L_{nB}} \right) + \left\{ \frac{n(0)}{N_{AB}} + Y \right\} \cosh \left(\frac{x}{L_{nB}} \right) - Y \sinh(-\alpha x) \tag{11}$$

where

$$Y \equiv \frac{\alpha F(1 - R) \tau_{nB}}{(\alpha^2 L_{nB}^2 - 1)N_{AB}} \tag{12}$$

Table 6. Notation used for modeling of the SOC cell structure.

Notation	Definition
A	Total surface area, cm^2.
b_B	Defined as D_{nB}/D_{pB}.
D_{nB}	Electron diffusivity in base region, cm^2/sec.
D_{pE}/L_{pE}	Empirical constant for emitter region, cm/sec.
I_D	Total current, mA.
I_{sc}	Short-circuit current, mA.
$I_p(x)$	Hole current, mA.
kT/q	Thermal voltage, V.
L_{nB}	Electron diffusion length in base region, cm.
N_{DE}	Donor concentration in the emitter region, cm^{-3}.
N_{AB}	Acceptor concentration in the base region, cm^{-3}.
n_i	Intrinsic concentration, cm^{-3}.
n(x)	Electron concentration, cm^{-3}.
q	Electrical charge, coul.
V_D	Diode voltage, V.
V_{oc}	Open-circuit voltage.
V_{jE}	Electrostatic potential drop across the emitter-base space-charge region minus the corresponding drop at equilibrium, V.
x	Distance from the boundary between the space charge region and the base region, cm.
X_B	Thickness of the base region, cm.
α	Absorption coefficient, cm^{-1}.

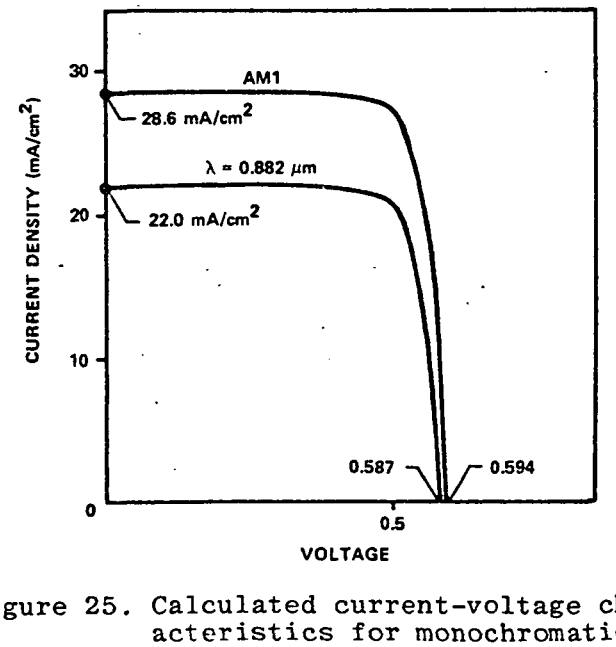

Figure 25. Calculated current-voltage characteristics for monochromatic light of wavelength of 0.882 μm and for AM1 light.

Equation (11) is plotted in Fig 26 for three values of wavelength. The figures demonstrate the following: As the wavelength increases, the slope at x = 0 decreases, indicating a decrease in collection efficiency. The latter decrease is approximately given by

$$\eta_{col} = \frac{\alpha L_{nB}}{1 + \alpha L_{nB}} \tag{13}$$

which is a well-known approximation. In particular, Eq. (13) is used to evaluate the diffusion length from LBIC measurements of η_{col}.

Now we turn to AM1 conditions. Our primary objective is to calculate a theoretical upper limit for J_{sc} and to compare this value with the measured values of J_{sc} for SOC cells. For AM1 conditions, we must solve the following standard differential equation by numerical methods:

$$\frac{d^2n}{dx^2} - \frac{n(x)}{L_{nB}^2} + \frac{G(x)}{D_{nB}} = 0 \tag{14}$$

where

$$G(x) = \frac{1}{hc} \int_0^\infty \lambda\alpha P(\lambda) \exp\left[-\alpha x\right] \, d\lambda \tag{15}$$

Here $P(\lambda)$ is the AM1 solar power spectral density given as a function of the photon wavelength, λ. For Eq. (15), we have assumed that the AR coating is perfect (i.e., R = 0) and that the thickness of the emitter region is negligible. Both these simplifying assumptions will be removed in a later report. The boundary conditions for Eq. (15) are

$$n(x) = n(0) \text{ at } x = 0 \tag{16}$$

and

$$n(x) = 0 \text{ at } x = X_B \tag{17}$$

Using numerical methods and Eqs. (10) through (13), we can determine a relationship between $I_n(0)$ and $n(0)$, which is the generalization of the monochromatic result expressed by Eq. (10). The generalized relationship can then be used with Eqs. (6) through (10) to give the AM1 current-voltage curve shown in Fig. 25. Figure 27 shows the corresponding minority-carrier profiles for J_{sc}, P_{max}, and V_{oc}.

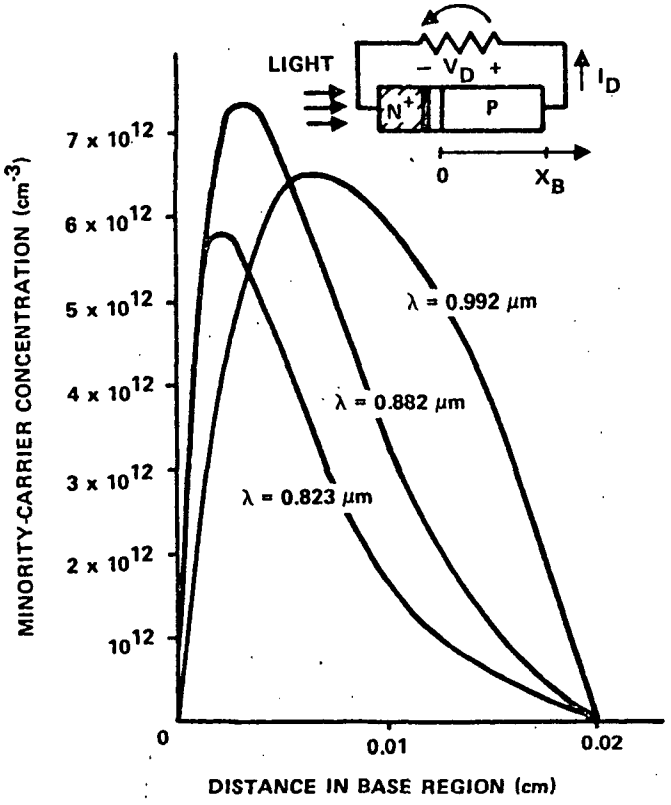

Figure 26.
Minority-carrier profiles in the base region for three values of wavelength: 0.823, 0.882, and 0.982 μm. The profiles were calculated at the maximum power point.

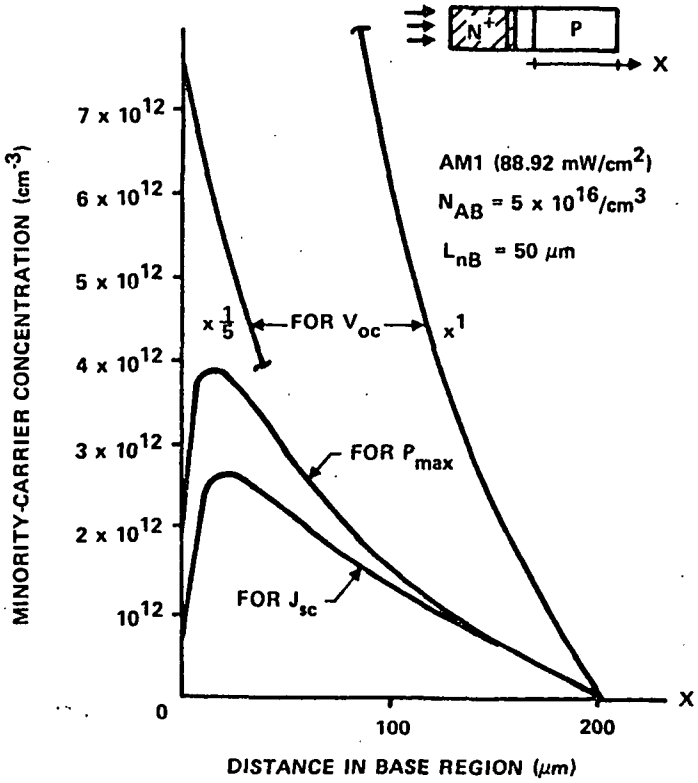

Figure 27.
Minority-carrier profiles for J_{sc}, P_{max} and V_{oc}. The profiles correspond to the AM1 curve given in Fig. 25.

For all calculations, the incident power density, P_{in}, is 88.92 mW/cm^2, which is the generally accepted value for AM1 sunlight. This value is about 10% lower than the 100 mW/cm^2 value generally used for cell measurements with an ELH lamp. For the figure, the metallization coverage was neglected, which means the J_{sc} is about 10% higher than possible with a typical metallization pattern. The low value of P_{in} approximately compensates for the neglect of the metallization coverage. Thus, AM1 results shown in Fig. 25 approximately represent measurement conditions using an ELH lamp with an incident power density of 100 mW/cm^2.

So for all calculations, we have assumed a diffusion length of 50 μm and negligible series resistance. Figure 28 shows the calculated cell characteristics for values of L_{nB} in the range from 10 μm to 100 μm, where the solid lines correspond to a specific series resistance of 1 Ω-cm^2 and where the dotted lines correspond to negligible series resitance. For the 1 Ω-cm^2 case, the calculated maximum efficiency is 11.2% for L_{nB} = 25 μm, 13.3% for L_{nB} = 50 μm, and 14.5% for L_{nB} = 100 μm. The measured characteristics of the SOC cell shown in Fig. 20 are indicated by squares in Fig. 28. For this cell, there is fair agreement between theory and experiment.

Recently, we have begun calculations to determine the maximum short-circuit current density as a function of diffusion length, assuming a perfect AR coating, a silicon monoxide AR coating, and no AR coating. The preliminary results are shown in Fig. 29.

MATERIAL EVALUATION (D. Zook, R. Hegel, C. Wensman, S. Parsons, and J. Dennis)

During the past year, there has been significant progress in assessing the relative importance of grain boundaries and impurities in limiting the performance of SOC solar cells.

We find that the average diffusion length is 15 to 25 μm, and that diffusion length within grains is about three times the average value. We can therefore say with some confidence that the structure (grain boundaries and dislocations) is responsible for the present efficiency, limit of 10.5%. The limitation due to impurities within grains would be 12.5 to 13% efficiency, corresponding to the factor of three increase in diffusion length.

This subsection summarizes development in our theoretical understanding of the relationship between grain boundary recombination and short-circuit

current (especially as related to LBIC measurements). Also, two different methods of determining an average diffusion length are compared; the effect of hydrogen passivation (performed at Sandia Labs) is discussed; and the relationship between structure and average diffusion length is discussed.

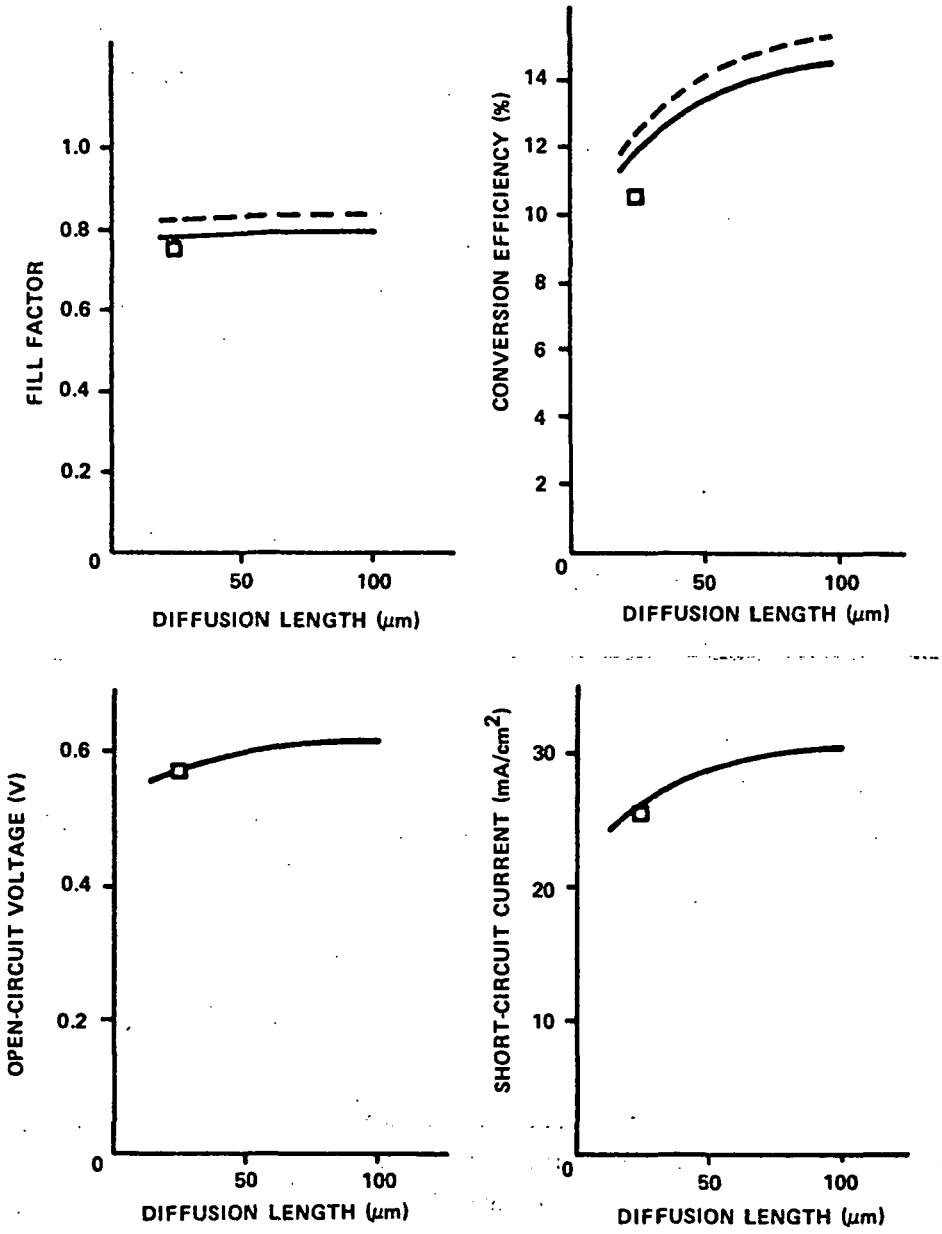

Figure 28. Solar cell characteristics as a function of base diffusion length, for a base thickness of 200 μm. Dotted lines assume no series resistance, solid lines include 1 Ω/cm^2 specific resistance. The squares in the latter correspond to cell no. 255-5-211-1.

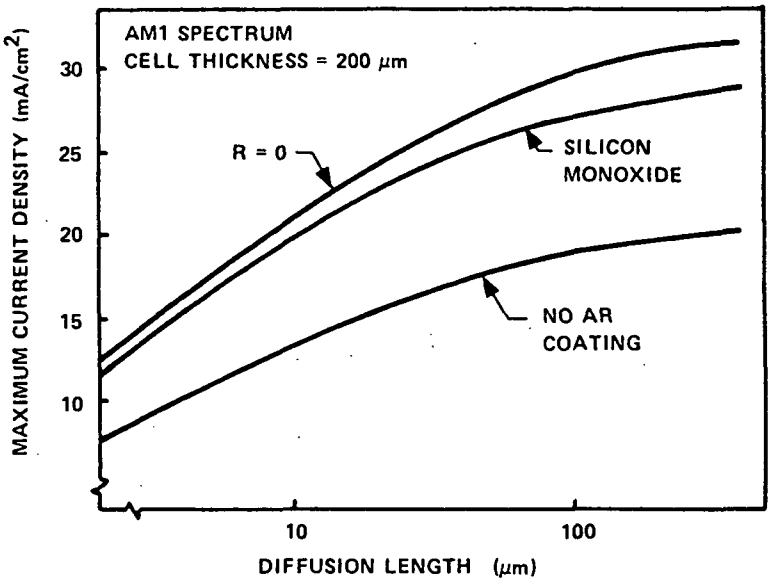

Figure 29. Calculated values of maximum current density as a function of diffusion length.

Theoretical Model of Grain Boundary Effects

An important assumption of our theoretical model is that the concept of a grain boundary recombination velocity, s, can be applied. This assumes a linear boundary condition at the grain boundary and means that analytical methods can be used to solve the differential equations. Several researchers[4,5] have predicted nonlinear effects at grain boundaries, based on the model of a potential barrier at the grain boundary. It is not clear, however, at what illumination levels the nonlinearities become important.

In order to clarify the role of grain boundaries in SOC material, LBIC (light-beam-induced current) measurements of quantum efficiency were made within grains and at grain boundaries. These measurements have been made on

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[4]H.C. Card and E.S. Yang, IEEE Trans. Elec. Devices ED-24, 397 (1977)

[5]J.G. Fossum and F.A. Lindholm IEEE Trans. Elec. Devices ED-27, 692 (1980)

several samples and in several different ways. The preferred method was to use a large slit opening (0.2mm) in the monochromator so that an intensity of about 10 suns could be attained in a 12-μm-diameter spot. Then neutral density filters were inserted into the beam to attenuate the light without changing the spot size or moving the sample.

The results of measurements are shown in Fig. 30. These were taken at the long wavelength where the effect of grain boundary recombination is assumed to be most severe. It is clear from these and other similar results that the dependence on intensity is quite small. We conclude that, in the range of interest, the concept of a constant recombination velocity at a grain boundary is valid, and that the theoretical model presented in Annual Report No. 4 should be appliable to SOC material.

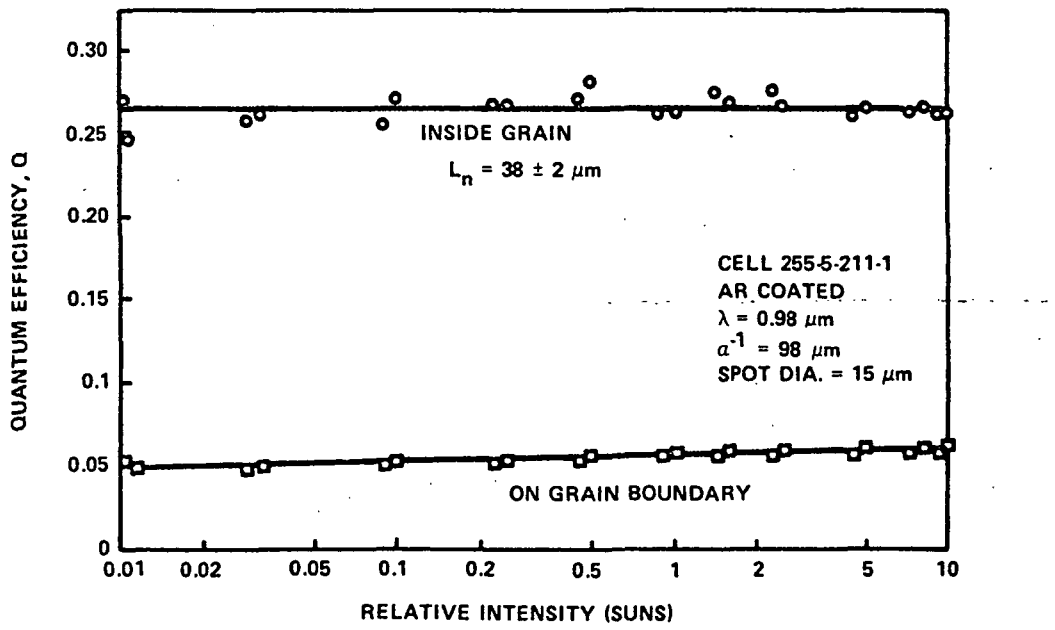

Figure 30. Quantum efficiency as a function of light-beam intensity at 0.98 μm.

The loss of short-circuit current due to a grain boundary is of particular interest to solar-cell performance. The LBIC quantum efficiency, Q, is a function of A, S and X, where A = αL, S = sL/D, X = x/L, and x is the distance from a grain boundary which is perpendicular to the junction. The total short-circuit current of a solar cell is simply the sum of the currents due to all such rays. The total loss in current due to an isolated grain boundary can be expressed as a loss in quantum efficiency:

$$W = 2\int_0^\infty \frac{Q_\infty - Q(A,S,X)}{Q_\infty}\, dx \qquad (18)$$

Here W is an effective width of a grain boundary in the sense that an opaque strip of width W on the surface of the length of the boundary would cause the same loss in current. The parameter $Q_\infty = Q(A,S,\infty) = A/(1 + A)$ is the usual quantum efficiency. This effective grain boundary width is plotted in Fig. 31 for all values of A and S. It can be seen that W decreases as A (or the absorption coefficient) increases; thus, W decreases as wavelengths decreases. This certainly agrees with experimental observations. The circles in Fig. 31 represent data points taken from LBIC data on SOC grain boundaries (sample 179-4). It is clear that the experimental values are in fair agreement with a surface recombination velocity S ≈ 20.

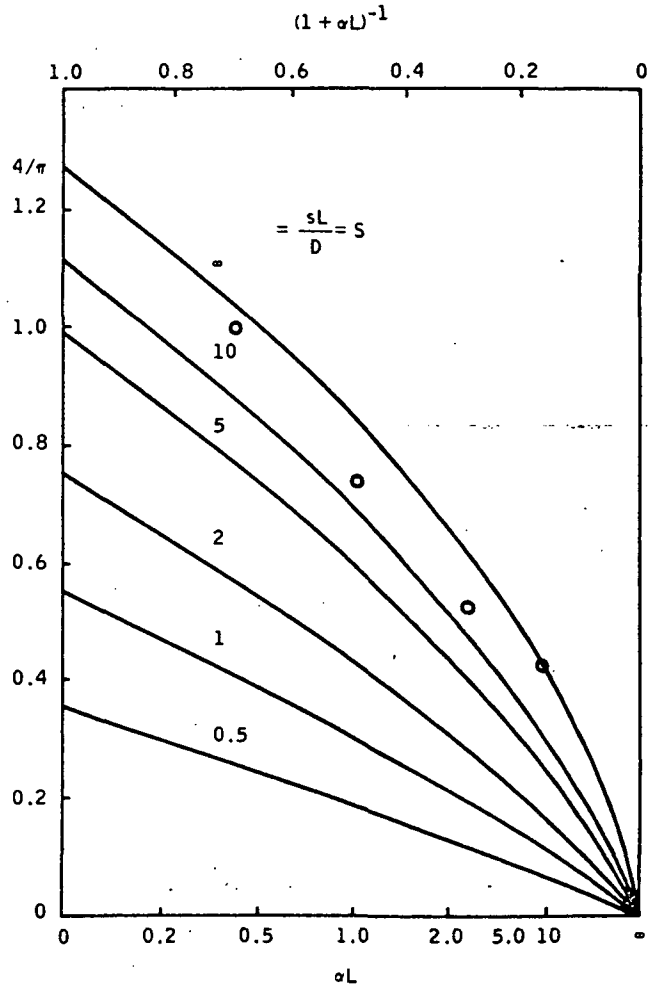

Figure 31. Calculated effective grain boundary width, W, as a function of wavelength for different values of surface recombination velocity, s, at the grain boundary. The wavelength dependence enters through the absorption coefficient, α.

The above discussion shows that out theoretical understanding of LBIC response in quite good. Experimentally, we have obtained LBIC scans on a

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large number of SOC solar cells, photodiodes, and unprocessed substrates (using, for the latter, the electrolyte technique). At best, we can make two generalizations, as follows:

1) There usually is a characteristic maximum diffusion length, L_{max}. This is evident from the good LBIC, response at 0.98 μm, and generally occurs in the largest visible grains (greater than 400 μm wide). Cross sections of samples at lines where the LBIC scan is known show that the best diffusion lengths occur in grains having high densities of twin boundaries and few dislocations.

2) There usually is a characteristic minimum diffusion length, characteristic of the most active grain boundaries. Surprisingly, the depth of the minimum LBIC response at 0.98 μm does not depend strongly on the spot size or the focus of the light beam. The minima of the LBIC response tend to be constant, even if the substrate is bowed, so that part of the scan is out-of-focus. Varying the spot size from 5 to 15 μm does not significantly affect the value of the minima. Thus, a "minimum diffusion length" is a fairly well-defined experimental quality for a given SOC cell.

Figure 32 shows values of $\bar{L}$, L_{max}, and L_{min} for a number of recent LBIC measurements. The average value of $\bar{L}$ is determined from the integrated average across the entire cell, corrected for metallization. The integration was performed electronically while scanning at 0.98 μm. A uniform region within a grain was selected and spectral response at all wavelengths was measured. The procedure described in Annual Report No. 4 was used to fit the long-wavelength spectral response (six data points between 0.823 μm and 0.994 μm), to give a value of L, 1 - R, and an rms deviation ΔL/L. The values of L_{max} and L_{min} were then determined from the 0.98 μm scan, and represent averages of the highest and lowest response at half a dozen points.

The values of L in Fig. 32 are shown as a function of doping. The three lines represent approximate fits for the diffusion length within grains, average diffusion lengths, and diffusion lengths at grain boundaries, respectively.

The data points labeled H and S were ignored in construcing these lines. In spite of the large scatter in the data, there is clear tendency for the diffusion length to decrease with the doping level. The reason for this

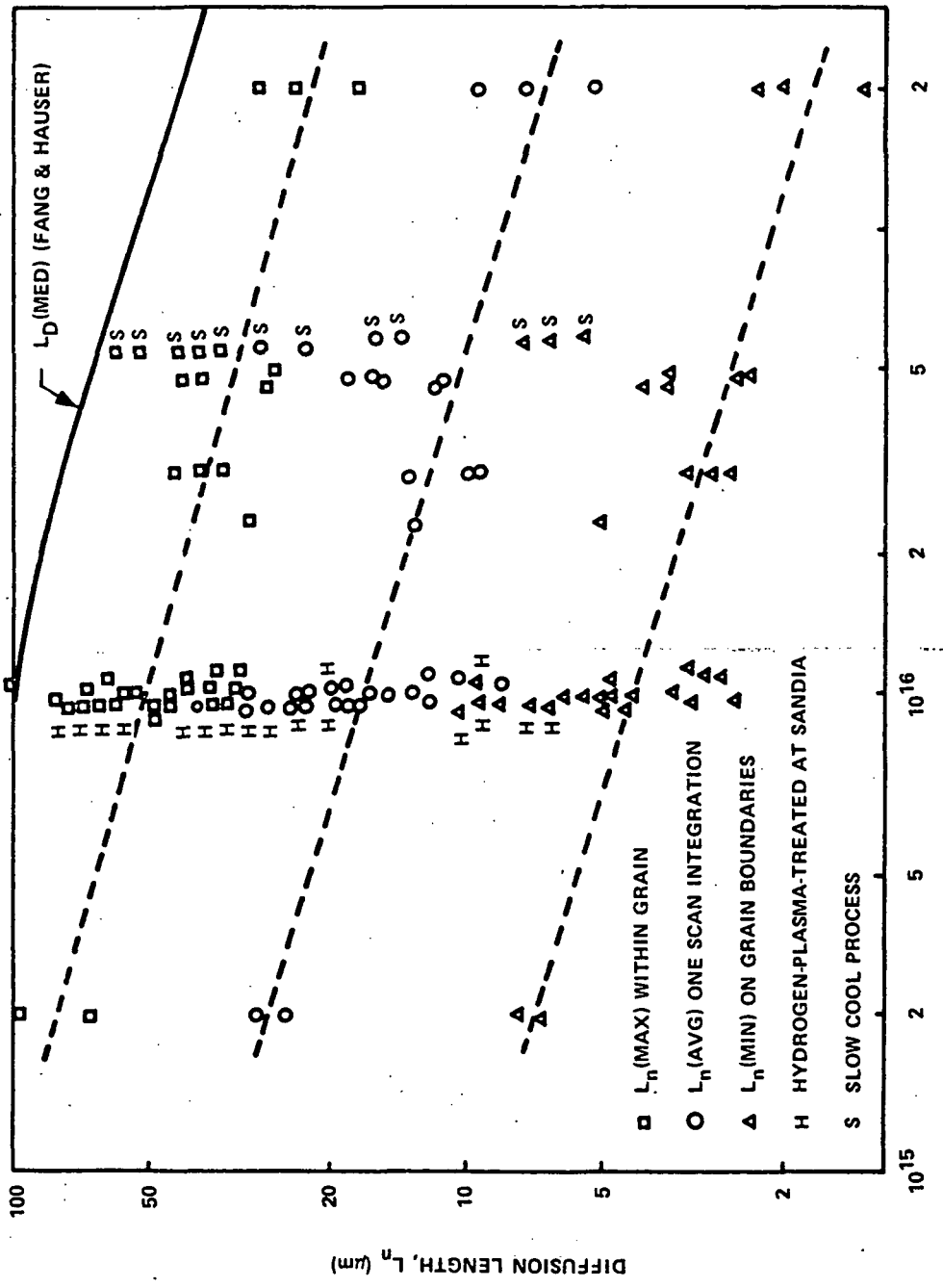

Figure 32. Diffusion length as a function of doping and cell processing.

decrease is not clear, since the boron itself does not produce recombination centers. However, single-crystal silicon does show behavior that is consistent with the behavior within a grain. The solid line is an average diffusion length for Czochralski cells taken from the literature.[6]

The decrease with doping is not understood. A possible explanation for the decrease is Auger recombination, but this mechanism would only become significant at higher doping levels. An alternative explanation is that boron forms complexes with carbon or oxygen, and that these function as recombination centers. If this effect could be prevented, the diffusion length and therefore the short-circuit current, would be significantly higher at a doping level of 5×10^{16}, and the efficiency of SOC cells would be about 10% higher. The slow-cool process gives such an increase, as discussed below.

Whole-Cell Diffusion Length Measurements

The LBIC method has certain advantages, but it is not a fast or simple method of determining an average length for a whole cell. A new system was constructed to quickly measure the whole-cell quantum efficiency at five different wavelengths. This system uses ELH lamp source and narrowband filters at 0.8, 0.85, 0.9 and 1.0-μm wavelengths. The intensity of each wavelength is about 0.1 suns. The signal is compared with that of a single-crystal cell. The single-crystal cell was calibrated against the reference EG&G photodiode that is used in the LBIC measurements. The LBIC measurements are at about one sun intensity and use a small spot size (5 x 12 μm).

Results of the correlation between the two types of measurements are shown in Fig. 33. It is clear that the correlation is not particularly good. The whole-cell illumination gave higher value of L_n than the values determined from the integrated LBIC scan. The reason for the discrepancy has not yet been determined.

The correlation between J_{sc} and L_n is shown in Fig. 34. In this case, two theoretical lines are shown. Both are special cases of the calculations in Fig. 29 and were obtained using the model developed by B. Grung. As pointed

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[6] C.R. Fang, and J.R. Hauser, 13th Photovoltaic Specialist's Conf. (1978) p. 1318. The orginal data are from S.I. Soclof and P. Iles, 11th IEEE Photovoltaic Specialist's Conf. (1975), p. 56.

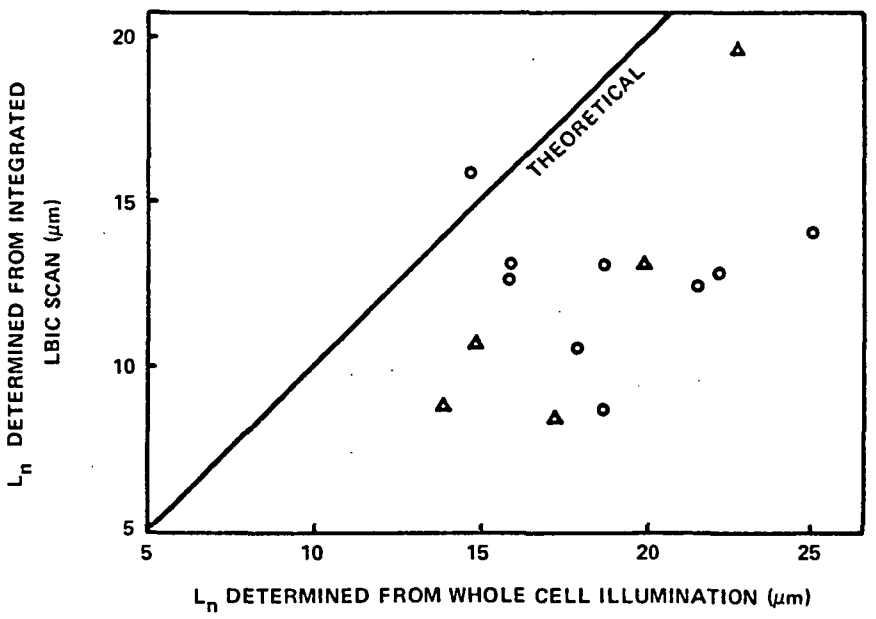

Figure 33. Correlation between two different measurements of average diffusion length.

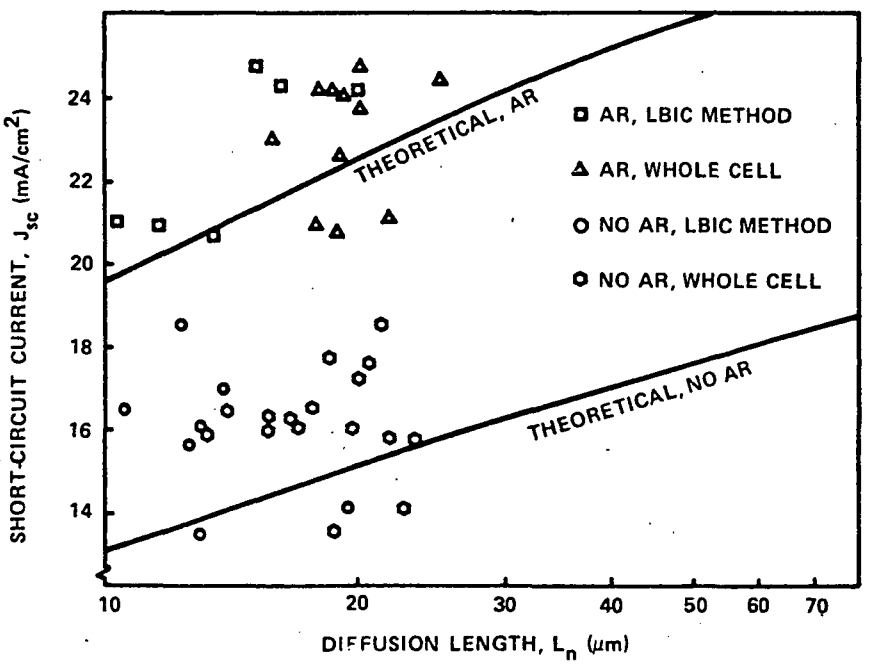

Figure 34. Correlation between short-circuit current density and diffusion length. The theoretical curves are from Fig. 29.

out previously, the non-AR measurements have a wider range of J_{sc} values because of inadvertent AR coatings. Again, there is a lot of scatter in the relationship between J_{sc} and L_n. For the AR-coated results, the LBIC method appears to give better correlation with J_{sc} than the whole-cell method.

One possible reason for the discrepancy in the two measurement techniques could be dependence of the recombination on light intensity. The whole-cell measurement is at a lower intensity than the LBIC measurements. However, the measurements as a function of intensity (Fig. 30) do not support this idea. There is also some discrepancy between the theoretical lines and the experimental values, since the theoretical lines should represent an upper limit to J_{sc} for a given L_n. The sources of the discrepancies will be investigated further.

Effects of Hydrogen Plasma Treatment

During the past year, two significant effects of cell processing on diffusion length were observed. The effects of hydrogen plasma treatment at Sandia Laboratories were described in the Quarterly Report No. 15 (July 31, 1980). The conclusions are:

- Most grain boundaries can be passivated to a considerable degree. However, some grain boundaries are not affected by the treatment.
- Uniformity within good grains is also improved. Correlations of LBIC response with metallographic cross-sections have shown that the nonuniformities within grains are due to variations in dislocation densities. Thus, hydrogenation apparently also reduces recombination at dislocations.

Effect of Slow-Cool Process

The slow-cool processing gives a significant improvement in efficiency, due to an increase in short-circuit current. The LBIC technique can be useful in determining whether the improvement was due to diffusion length within grains or at grain boundaries. Diffusion length data from LBIC scans (see Fig. 32, shows that the values of L_n (max), L_n (min), and L_n (avg.) are all improved compared with cells at the same doping level.

Since the slow-cool processing also improves diffusion lengths in single-crystal cells, it is unlikely that accumulation of impurities of grain

boundaries is the mechanism of improvement. Thus, the grain boundary recombination velocity, s, may not be affected. The dimensionless parameter $S = sL/D$ is actually increased when L increases, but since $S \gtrsim 20$ initially, this increase is not significant. The effective width, w, of a grain boundary is thus approximately proportional to L, and as L increases, grain boundary recombination becomes a larger fraction of the total loss.[7]

Relative Importance of Structural Defects and Chemical Defects

The reasons for regions with poor diffusion lengths were discussed in the Quarterly Report No. 15 (31 July 1980). Closely spaced grain boundaries, high dislocation densities, and subsurface grain boundaries have been identified as factors in reducing the value of L from L_{max} to L. The amount of the reduction may be estimated from the theoretical relationship between L and J_{sc} or between L and efficiency discussed in the "Modeling" section of this report.

Let us assume, for the sake of argument, that L_{max} is determined by chemical defects (i.e., isolated impurities within grains). The value of $\bar{L}$ is a factor of two to four less than L_{max} in SOC material because of structural defects (grain boundaries and dislocations). In order to increase the short-circuit current from the best present values (25 mA/cm^2) to the best values for single-crystal samples (30 mA/cm^2), both have to be reduced considerably. Elimination (or complete passivation) of grain boundaries would increase J_{sc} to about 28 mA/cm^2, and then increasing L_{max} from 50 to 200 μm would increase J_{sc} to about 30 mA/cm^2. Thus, both types of defects are important in limiting the performance of present SOC solar cells, with structural defects being slightly more important.

ECONOMIC ANALYSIS (S. Schuldt)

Cost estimates for SOC panels have been recalculated as new cost input data or new price estimation guidelines were made available. The latest estimates, which we summarize here, differ from those reported in April, 1980,[8] in the following respects:

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[7] J.D. Zook, Appl. Phys. Lett. 37, 223 (1980).

[8] DDE/JPL 954356/12 Quarterly Contract Report No. 14, 21, April 1980.

- A recent (September, 1980) independent cost analysis gave $\$5.78/m^2$ ceramic cost instead of $\$3.97/m^2$ (1980 dollars). This value may be lowered in the future, but is used in the present analysis.
- Yield is 87%, panel-to-module, instead of 83% previously used (sheet fabrication yield is 92%; cell yield, 95%; and module yield, 99.5%).
- The revised (IPEG2) estimation formula is now used.

The entries in Table 7 are direct costs for an annual production of 2.5 million square meters of sheet SOC, not adjusted for yield in cell fabrication and subsequent module manufacturing steps. Projected low-cost technology is postulated, as summarized by the listed assumptions. The 85% plant efficiency (15% downtime) represents loss of production time for all causes, including equipment repairs and replacement, preventive maintenance, and crucible replacement. A detailed analysis of the downtime factor is not possible at this time due to our limited data. We estimate crucible replacement times including cooldown and startup, will be on the order of 12 hours per week per machine, or 7%.

Table 7. Cost data for target technology.

Major Assumptions

- 2.5 million m^2 production
- 0.25-cm/sec pull speed
- Two 12.5-cm tracks per coating machine
- $50,800 cost for silicon coating machine
- 1/12 operator per coating machine; 4.7 shifts
- Operator labor $13,150/year without fringe benefits
- Coating machines stacked six high (24 ft^2 prorated floor space per machine)
- $\$5.78/m^2$ ceramic cost
- 85% plant efficiency
- 92% process yield

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	34,358	649	61,805	687,800(a) 15,706,500(b)	14,131
Silicon coating	8,405,947	3969	851,827	1,378,350(c) 8,881,464(d)	252,987
Inspect	501,500	2396	862,491	---	7,345
Total	8,941,805	7014	1,776,123	16,531,650(e) 25,413,114(f)	274,463

(a) Carbon, (b) substrates, (c) argon, crucibles, furnaces, insulation, (d) polysilicon, (e) excluding silicon, (f) including silicon.

Manufacturing price estimates are based on the IPEG2 formula:

$$\text{PRICE} = \begin{Bmatrix} 0.57 \\ 0.52 \end{Bmatrix} \text{EQPT} + 109\ \text{SQFT} + 2.8\ \text{DLAB} + 1.2\ (\text{MATS} + \text{UTIL}) \qquad (19)$$

In our case, the EQPT coefficient, 0.52, applies to INSPECT, where the anticipated equipment life is 10 years; the coefficient 0.57 applies to the other two tasks, for which equipment life is 7 years. We have also applied the DLAB coefficient of 2.8, because our direct labor costs do not include fringe benefits. Reduced to price per square meter, the projected technology estimates are

$\$12.99/m^2$ added value
$\$17.25/m^2$, including silicon

For an assumed 11% encapsulated cell efficiency and subsequent processing yields (cell and module fabrication) totaling 94.5%, the respective costs on a peak watt basis are

$12.5¢/W_p$ added value
$16.6¢/W_p$, including silicon

The price estimation formula can also be used to calculate price-sensitivity data, or price changes resulting from a change in any cost input parameter. For illustration purposes, it is convenient to denote the cost input changes in terms of percent of nominal values. For example, a polysilicon price of \$16/kg would be expressed as

$$\Delta\%_{SIL} = 100 \times \frac{16 - 14}{14} = +\ 14.3\%, \qquad (20)$$

since the nominal price is \$14/kg. The price sensitivity is given relative to ceramic (CER) and silicon (SIL) costs, silicon coating time (SCT), coating machine cost (CMC), coating operator load (COL), and argon cost (ARG):

$$\begin{aligned} \$ = 17.25 &+ 0.0754\ \Delta\%_{CER} + 0.0426\ \Delta\%_{SIL} \\ &+ 0.0353\ \Delta\%_{SCT} + 0.0192\ \Delta\%_{CMC} \\ &+ 0.00954\ \Delta\%_{COL} + 0.00083\ \Delta\%_{ARG} \end{aligned} \qquad (21)$$

The sensitivities are the coefficients in Eq. (21), or the slopes of the corresponding graphs in Fig. 35. These graphs, of course, intersect at 0%, giving the nominal sheet value, $\$17.25/m^2$. The largest theoretically possible cost saving is represented by negative 100%, meaning that a particular parameter has zero cost value. Hence, the intercepts on the left-hand vertical axis give the hypothetical sheet price in the zero-cost limit (e.g., the "added-value" is seen as the silicon graph intercept) $12.99.

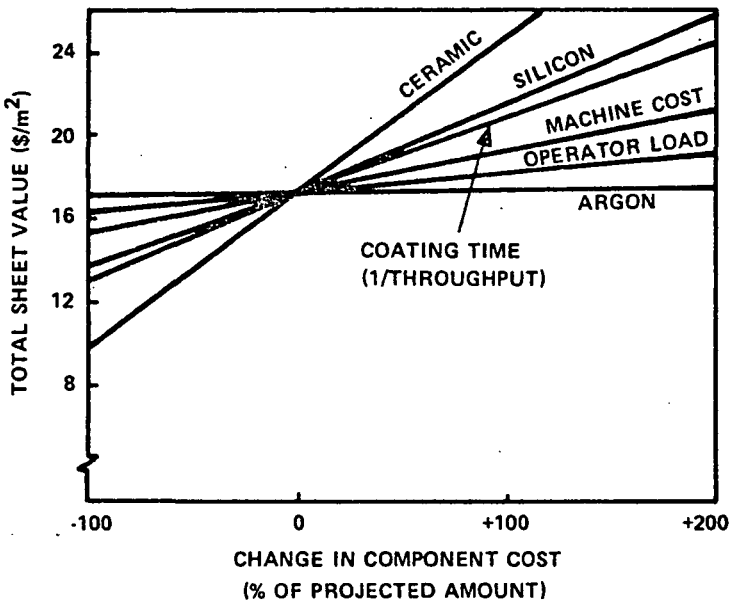

Figure 35. Sensitivity profiles for total sheet value according to projected technology. Abscissa represents relative (%) change in component cost (e.g., +100 and -50 denote doubling and halving, respectively).

Another major category of economic analysis deals with progress-to-date technology instead of projected low-cost technology. A number of parameters have been changed to reflect our perception of progress-to-date, particularly with respect to silicon coating throughput and operator load. Throughput is based on a pulling speed of 0.0625 cm/sec, operator load is 0.5, and machines are placed two to a stack for a prorated floor space of 72 ft^2 per machine. Compared with projected technology, direct silicon coating costs are thereby magnified by the following factors:

- Coating machines x4
- Materials (except Si) x4
- Operators x24
- Floor space x12

Table 8 gives direct costs for progress-to-date technology, with the assumptions according to Table 7 except as modified above.

Table 8. Cost data for progress-to-date technology.

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	34,358	649	61,804	687,800[a] 15,706,500[b]	14,131
Silicon coating	33,623,788	47,628	20,443,848	5,513,400[c] 8,881,464[d]	252,987
Inspect	501,500	2,396	862,491	---	7,345
Total	34,159,646	50,673	21,368,144	21,907,700[e] 30,789,164[f]	274,463

(a) through (f): See Table 7.

Based on the values of Table 8, the IPEG2 formula yields:

$44.57/m^2$ added value
$48.83/m^2$, including silicon

For price per peak watt, we assume an encapsulated cell efficiency of 8.4% and a subsequent net processing yield of 94.5%:

$56.1¢/W_p$ added value
$61.5¢/W_p$, including silicon.

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

- A design strategy to avoid buckling and breaking of substrates have been formulated, implemented, and verified.
- Thermal modeling has proven to be useful for improving the design of SCIM-II.
- A slow-cooldown after the phosphorus diffusions significantly improves cell performance.
- Cell performance of present SOC cells is limited by average diffusion length.

RECOMMENDATIONS

- The SCIM-II carbon parts should be purified to improve the performance of SOC cells from the SCIM coaters.
- Further experiments are needed to determine the conditions for stable, reproducible coatings by SCIM-coating.
- Additional experiments are also needed to determine the conditions for SCIM-coating using high-speeds growth modes. Fast growth exploits the inherent stability of supported growth and makes the economies of SOC production quite attractive for low-cost solar cells.

PROJECTION OF FUTURE ACTIVITIES

- Continue to use dip-coated cells for use in evaluating processing variations aimed at efficiency improvement.
- Continue to modify SCIM-II to attain uniform transverse temperatures.
- Explore the reasons for dendrite formation in SCIM-II and try methods of inhibiting dendrite formation.
- Install purified carbon parts in SCIM-II.
- Investigate effects of atmospheric during growth by using the experimental dip-coater.
- Investigate the relationship between diffusion length and structure by using etching of cross sections.
- Investigate the apparent inconsistency between different methods of determining effective diffusion length.

NEW TECHNOLOGY

A technique for supporting heater insulation with the heater itself has been shown to be effective in reducing heat loss. The process involves the use of graphite felt cemented directly to the heater. The process has been implemented with impure carbon parts in SCIM-II, but appears to be compatible with high-purity parts.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figs. 36, 37, and 38, respectively.

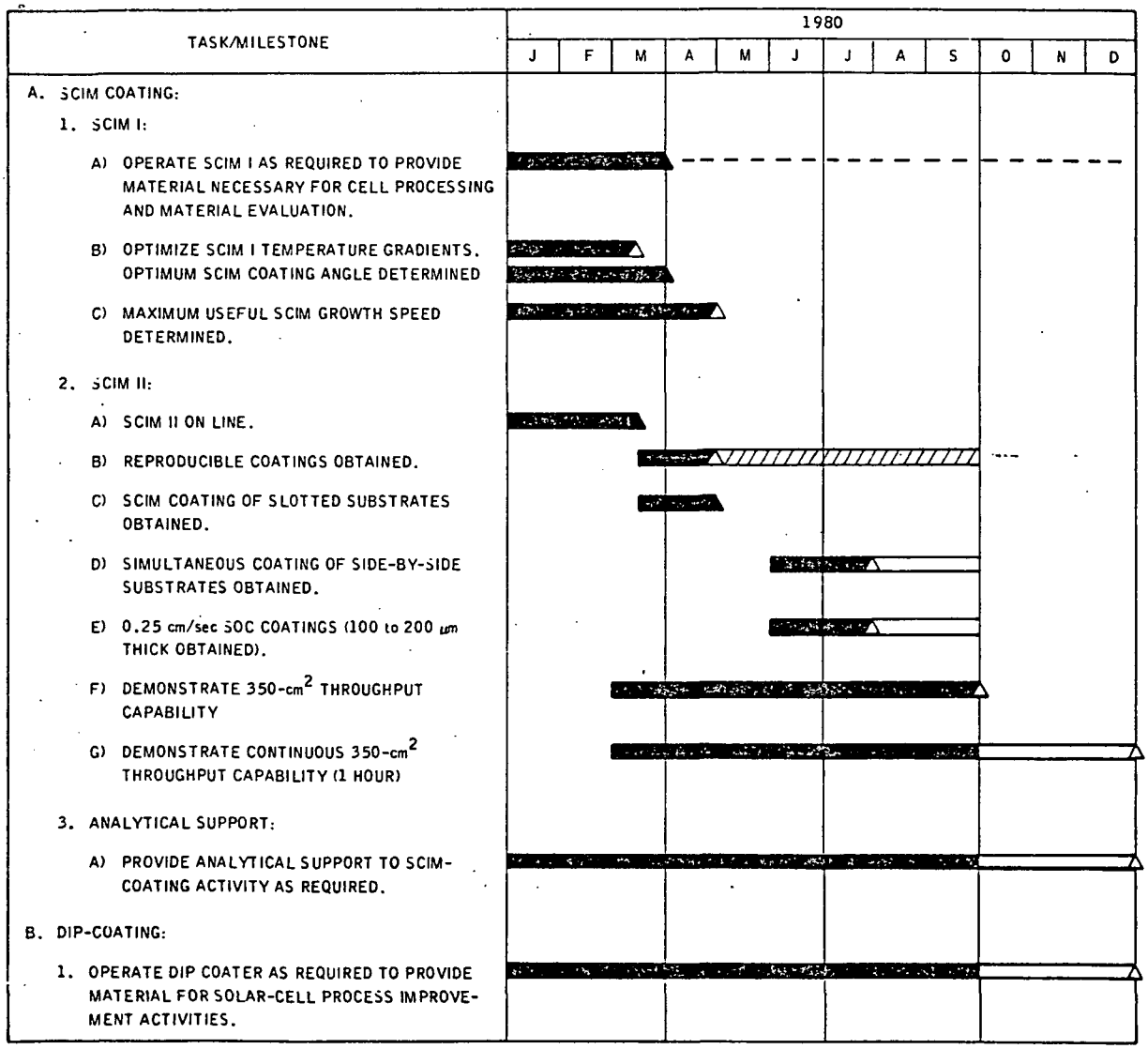

Figure 36. Updated program plan.

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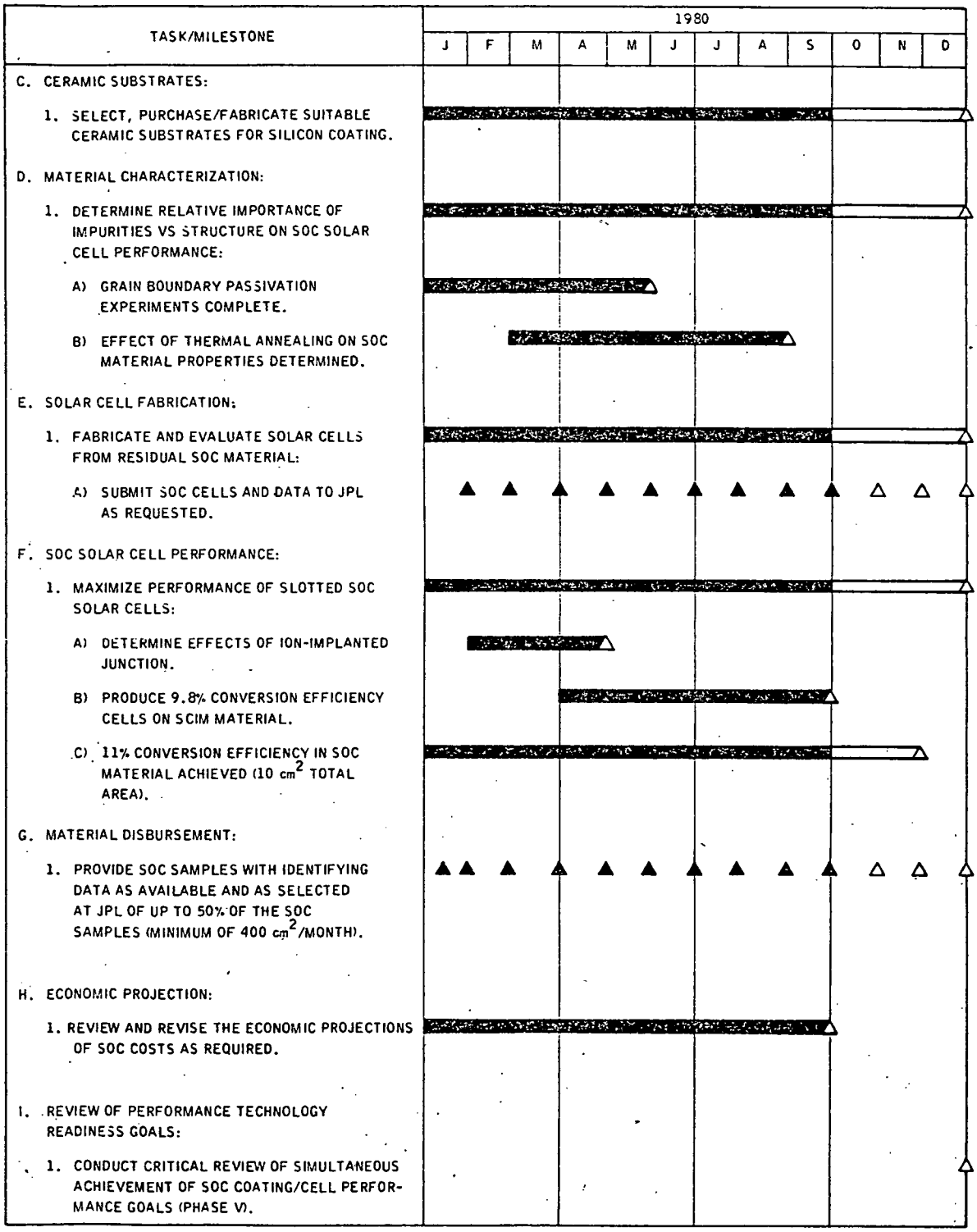

Figure 36. Updated program plan (concluded).

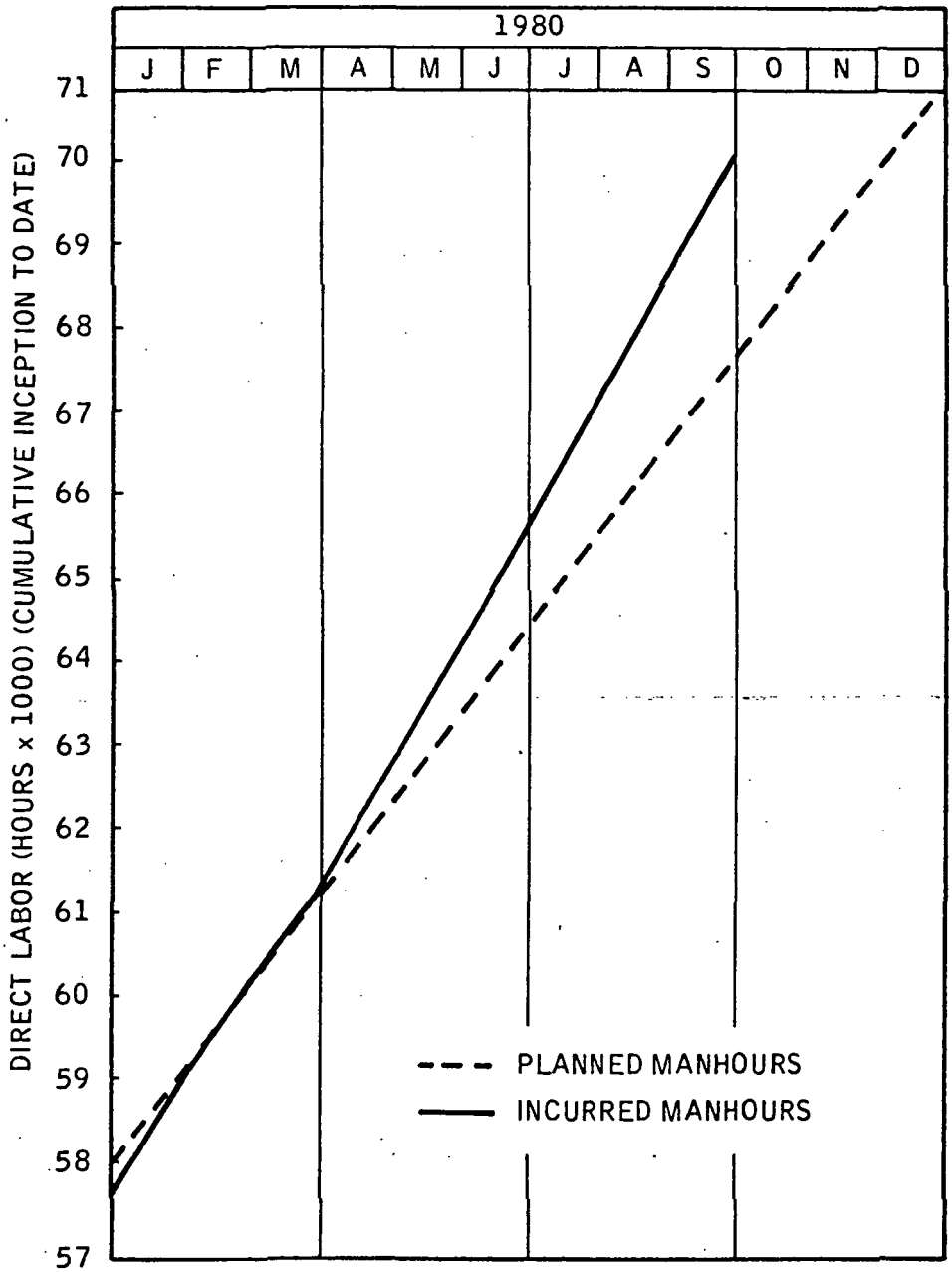

Figure 37. Updated program labor summary.

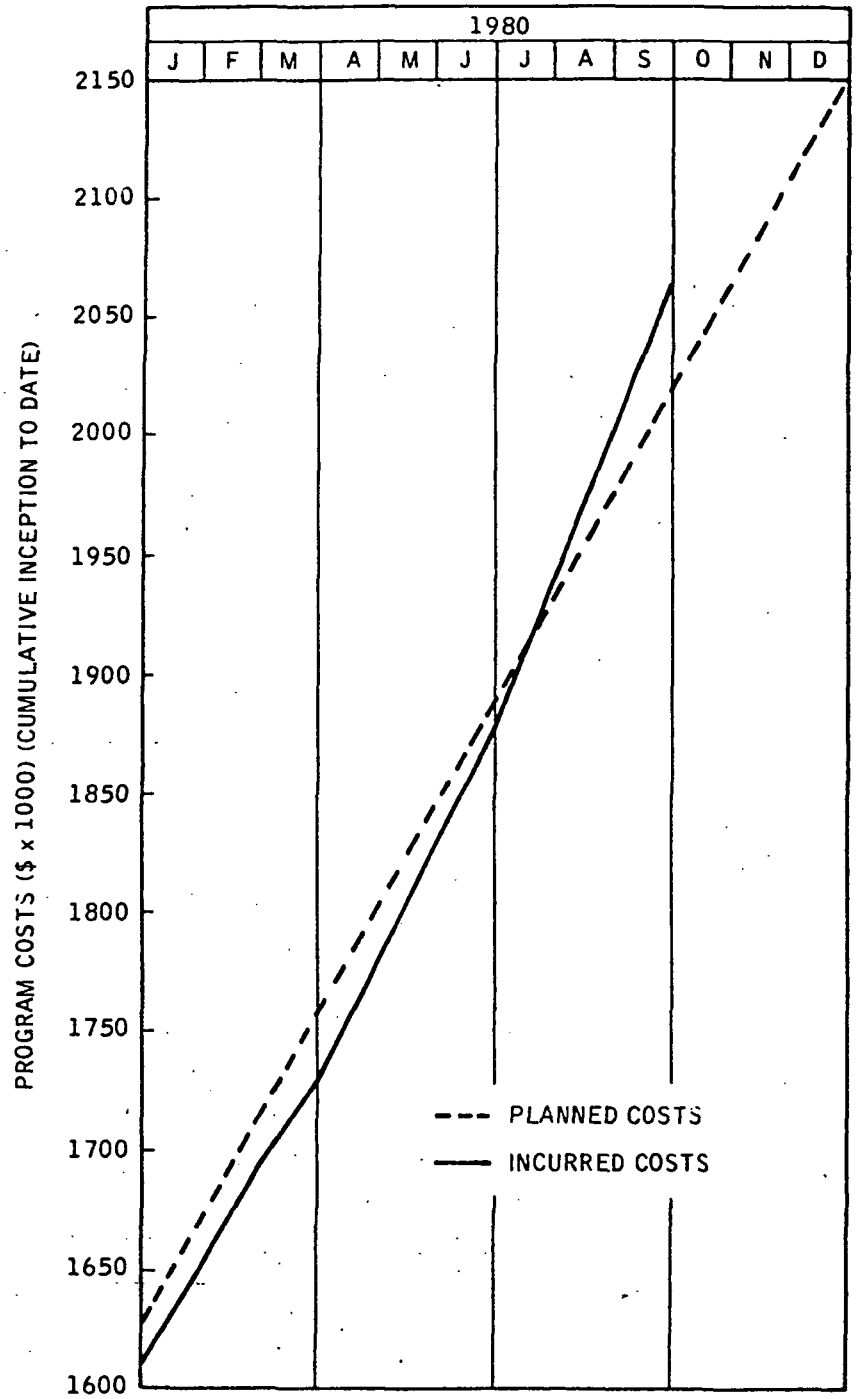

Figure 38. Updated program cost summary.