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An Experimental Investigation of Silicon Wafer Surface Roughness and its Effect on the Full-Strength of Plated Metals

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AN EXPERIMENTAL INVESTIGATION OF SILICON WAFER SURFACE ROUGHNESS AND ITS EFFECT ON THE PULL-STRENGTH OF PLATED METALS

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ABSTRACT

Plated silicon wafers with surface roughness ranging from 0.4 to 130 microinches were subjected to tensile pull-strength tests. Electroless Ni/electroless Cu/electroplated Cu and electroless Ni/electroplated Cu were the two types of plate contacts tested. It was found that smoother surfaces had higher pull-strengths than rougher, chemically-etched surfaces. The presence of the electroless Cu layer was found to be important to adhesion. The mode of fracture of the contact as it left the silicon was studied, and it was found that in almost all cases separation was due to fracture of the bulk silicon phase. The correlation between surface roughness and mode of contact failure is presented and interpreted.

INTRODUCTION

Field tests on solar cell arrays and performance analyses of space solar cells have indicated that most cell failures can be attributed to contact degradation due in part to thermal cycling (1). Furthermore, it has been shown (2,3,4) that adhesion between an adherend (substrate) and an adherate (film) can significantly affect the durability and longevity of the adherend-adherate system in real-time use; i.e., the quality of plated-contact adhesion to solar cells is an indication of how well the device will stand up to thermal cycling. The measurement of this adhesion is important to determine the effect of changes in process variables, i.e., substrate preparation, and thereby to optimize the conditions which yield the required adhesion strength (3). It is the purpose of this study to determine how variations in the roughness of silicon wafer surface affects the measured tensile pull-strength of metals plated to this surface.

BACKGROUND

Although the plating of solar cell contacts has been receiving much attention and study lately (5,6,7), the process is certainly not new. Studies from 1963 and earlier (8,9) describe the use of an electroless nickel bath to produce a contact grid pattern on solar cells. This process, however, was soon replaced by a technique offering longer cell lifetime (10) and higher cell efficiency, i.e., vapor deposition of metals such as chromium, titanium, palladium and silver.

It is the vapor deposition step in solar cell processing, however, that is contributing a major portion of the high capital cost of photovoltaic energy systems. The high costs of vapor deposition are due to (1) the high selling price of the precious metals involved, (2) the large percentage of the vaporized metals that go to waste by not impinging upon the cell, and (3) the high process costs involved with a low-throughput, high-vacuum system.

Plated contacts offer advantages over vapor deposited contacts in all of the above three cost considerations (6). Primarily, the metals commonly used (nickel, copper, lead-tin solder) are relatively low in cost. Secondly, these metals plate only on the solar cell, thus eliminating waste. Finally, the methods of electroless and electrolytic plating allow rapid thru-put of wafers, thus processing costs become a less significant factor.

Much work has been conducted lately to develop a high-quality plated-contact process. The driving force behind such studies is the need for low cost per unit of photovoltaic power. Motorola (7), OCLI (1), and Solarex (5) have demonstrated cells, with good I-V characteristics, made with various plate and plate-solder sequences.

The Motorola process is the most complex of the three demonstrated processes. This process consists of the sensitizing of silicon surface with an immersion palladium bath; sintering in nitrogen at 300° C; electrolessly plating a layer of palladium of 1000 Å; sintering again; electrolessly depositing a nickel layer of 5000 Å; then finally dipping in a lead-tin solder melt to provide a layer responsible for the electrical conduction of energy generated by the solar cell.

The OCLI sequence also begins with palladium sensitizing, but after sintering, a nickel deposition follows with an electroless copper plate of 500 Å and then an electrolytic copper layer 4 to 6 μm to provide the conduction path. The thin electroless copper layer is said to increase contact adhesion and to improve the quality of the electrolytic copper plate.

Compared to the other two processes, the Solarex contacting sequence is very simple, requiring only two steps: (1) the electroless plating of nickel directly to the silicon surface (palladium sensitizing was found to be unnecessary) and (2) the dipping into a lead-tin solder to provide a conduction layer. Cell performance and contact adhesion was found to be negligibly affected by sintering.

All three processes have undergone development studies which included measurement of the contacts'

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adhesive properties by a tensile pull-strength test. Tests of this nature must be made to determine if standard minimum pull-strength is obtainable. A strength of 450 g/0.02 cm^2 must be reached in order for an array of cells to be accepted for use in space-flight missions.

Comparing the reported (5,6,7,9) results of adhesion tests brings forth some incongruities concerning the effect of the silicon cell surface roughness on the pull-strength of the plated contacts. Motorola obtained both above (950 g/0.02 cm^2) and below (approx. 315 g/0.02 cm^2) standard results for chemically-polished and textured surfaces, respectively. Measurements by OCLI were below the standard for both a chemically-polished (approx. 140 g/0.02 cm^2) and textured (approx. 250 g/0.02 cm^2) surface. Results from the Solarex studies could not be analyzed as no reference was made to the area of contact being loaded during the tests. The fourth study, by Bell Labs, on nickel-plated contact adhesion showed a maximum pull-strength of 4500 and 1500 g/0.02 cm^2 for a textured and chemically-polished surface, respectively. A summary of the pull-strength studies indicates that: (1) one study found better adhesion on smooth surfaces, (2) another study found poor adhesion on both smooth and rough surfaces with adhesion to rough surfaces being slightly stronger, and (3) a third study showed excellent adhesion for both types of surfaces, again with a rough surface having the greater pull-strength. It was these reported inconsistencies which formed the justification to pursue this study.

EXPERIMENTAL

To analyze the effect of surface roughness on the pull-strength of plated contacts, the following procedure was employed: (1) silicon wafer surfaces with varying degrees of roughness were prepared, (2) metal was deposited onto these surfaces, and (3) the tensile pull-strength was determined.

Preparation of Surface Textures

Some electrical and physical properties of the silicon wafers used throughout the study are given in Table I; no P-N junctions were diffused in order to reduce variations among the wafers tested. These wafers came as-received with a mechanically-polished surface on one side and a chemically-etched surface on the other. In addition to these, two more textures were made on some of the Monsanto wafers by further etching in either a "Sodium" bath or a "Pyro" bath The composition and etching conditions for these two baths are listed in Table II. The Pyro bath composition was taken from Kern (11), but the etching time was increased from 67 minutes to 120 minutes in order to obtain a rougher surface. The Sodium bath composition was the result of the author's own experimentation with semiconductor etching chemicals.

Accurate assessment of the effect of silicon surface roughness on contact pull-strength required quantitative descriptions of the surfaces rather than qualitative statements such as "polished", "rough", or "very rough". This was accomplished by measuring the average roughness, Ra, of each wafer with a diamond profilometer. The average roughness is a measure of the average deviation in microinches from a graphical centerline of a surface profile (11). As a diamond stylus is drawn across the surface of a wafer, the peaks and valleys of the profile are converted into electrical signals, amplified, and recorded on chart paper. At the same time, the absolute value of the area under the recorded profile is divided by the distance traveled by the chart pen; this quotient is also recorded on the chart paper and represents the Ra value for that particular surface.

Profilometer measurements on the surfaces as-received deviated very little from wafer to wafer, while the Pyro- and Sodium-etched surfaces had wide ranges of Ra values. Generally, though, those surfaces made from the Sodium etch could be classified in one of two groups: (1) 40 to 50 microinches or (2) 75 to 90 microinches. The Pyro-etched surfaces were all within the range of 100 to 130 microinches. The results from the profilometer tests are given in Table III.

Deposition of Plated Layers

The first step necessary before any type of contact metals were deposited was to clean the wafers to ensure repeatable, high-quality plating (7). The cleaning process employed was one commonly used in the semiconductor industry to remove dirt, stains, and organic solvents from the surfaces of silicon wafers; the cleaning procedure is outlined in Table IV.

The four types of surfaces available from the Monsanto wafers (see Table III) were the first set to be plated. The wafers were plated in sets of four, one wafer from each of the four texture categories being selected; this provided equal plate thicknesses on each type of surface, thus minimizing the effect of layer thickness on the pull-strength measurements (5,9). Both sides of each wafer were plated to provide ample area on which a number of pull-strength tests could be performed.

The plating sequence employed for the first set of wafers was developed from selected procesing steps, solutions, and plate thicknesses given in the studies by Motorola, OCLI, and Solarex (1,5,7). The major elements of the plating sequence are (1) deposition of electroless nickel (5000 Å), (2) electroless deposition of copper (500 Å), and (3) electrolytic deposition of copper (3 μm). Electroless plating was carried out on hot plates with magnetic stirrers. A detailed listing of this plating sequence is given in Table V, and compositions of the plating solutions used are presented in Table VI.

Ten runs were made using this plating process, but only 28 of the original 40 wafers resulted with sufficient plate quality to allow pull-strength tests to be performed: nine wafers of Ra = 0.4; six of Ra = 13; four of Ra = 40-50; four of Ra = 75-90; and five of Ra = 100-130. The reason for the twelve wafers being unsuitable for testing was due to unexplainable inconsistencies in the deposition of electroless copper. In any given run, any one or more of the four wafers would have an adverse reaction in this solution, resulting in severe spalling of the electroless nickel layer away from the silicon surface; the other wafers would plate with good quality. The spalled wafers were

not conducive to electroplating, due to exposure of the silicon surface, and were removed from the study.

The second set of silicon wafers plated were those as-received from Semiconductor Processing. The plating sequence employed was similar to that outlined in Table V except that the electroless copper deposit was deleted to eliminate the spalling effects of the nickel layer. One wafer of each texture (Ra = 0.4, 40) was assigned to a run, nine such runs providing eighteen wafers all possessing good plate quality, i.e., no spalling and total coverage of the wafer surface.

Tensile Pull-Strength Testing

Forty-six wafers from the two plating sequences were available for tensile pull-strength testing. In a tensile test, a load (force) is applied perpendicularly to the metal-silicon interface until separation occurs. The area of this separation is divided into the load applied to obtain the pull-strength of the test.

Each of the nineteen runs was individually prepared for testing by the following procedure: (1) An aluminum stud, coated with a heat-curing epoxy at one end and threaded at the other, was clamped perpendicularly to the electrolytic copper layer of each wafer, (with Sodium and Pyro surfaces, the stud was attached to the side of the wafer that was originally textured, as-received). It was through this stud that the tensile load was applied. (2) Each run of wafers was placed into an oven having a nitrogen atmosphere at 125° C for 90 minutes to cure the epoxy. Penetration of the epoxy into the plated layers while curing would make for inconsistent test results, but the plate deposits were dense enough and the diffusion rate of the epoxy was slow enough to make this effect negligible. (3) After curing, the oven door was opened, allowing the wafers to gradually cool to room temperature. This reduced the formation of thermal stresses in the silicon, plated layers, and/or epoxy that would reduce the tensile load required for separation during pull-testing. Oxide formation was minimized by allowing the N_2 to flow while the wafers cooled. (4) The clamps on the studs were removed and a steel rectangle with a 0.5 cm hole in its center was placed over the stud of the wafer to be tested. This plate was used to minimize elastic deformation of the wafer during tensile loading. Elastic deformation causes a decrease in the load necessary for separation to occur. (5) A cylindrical piece of copper with a hook at one end was threaded onto the stud. (6) The entire assembly was clamped to a Chatillon pull-strength tester.

The pull-strength test was performed as follows. The load was gradually increased until either separation occurred or the loading limit of the Chatillon was reached. In the former case, the load at separation was recorded along with the separated area and the mode of failure. The mode of failure was always one of the following: (1) separation at the nickel-silicon interface, (2) fracture within the bulk silicon phase, or (3) failure of the epoxy bond. The pull-strength was calculated by dividing the load required for separation by the area of the failure and normalizing the quotient to the standard units of g/0.02 cm^2. In the latter case, in which the loading limit was reached, the pull-strength was recorded as being at least 5230 g/0.02 cm^2, this number being derivd from the load limit of 35 lbs. and the area of the stud-copper interface, 0.0607 cm^2.

RESULTS AND DISCUSSION

Cumulative data from 201 pull-strength tests on 46 wafers are presented in Tables VII and VIII for the Ni-Cu-Cu and the Ni-Cu plating sequences, respectively. It is clear from these two tables that the measured pull-strength of plated metals decreases with increasing silicon surface roughness. This trend agrees with the findings of Motorola (7), but differs with those of OCLI (6) and Bell Labs (9). Further, the trend seems to oppose one of the principles of the mechanical theory of adhesion (13) which states that adhesion of a film to a substrate increases with greater substrate surface roughness. This conflict can be resolved, however, when attention is given to the major mode of separation occurring throughout the pull-strength tests, i.e., fracture of the silicon phase (170 of the 201 tests performed were of this mode). In mechanical theory, the term "adhesion" refers to the measurement of the force required for separation to occur at the adherend-adherate interface, i.e., the "practical" adhesion of the system (3). Instead of measuring the "practical" adhesion in this study, cohesive strength (3) of the silicon substrate was measured. These test results demonstrate that for any given silicon wafer surface roughness, the adhesion of the plated contact is greater than the cohesive forces of the bulk silicon phase, thus indicating very good contact adhesion (7).

Increasing silicon wafer surface roughness effects a weakening of the cohesive strength of the wafer. A possible cause for this weakening may be the formation of microcracks or "etch pits" (14) at crystal defects in the silicon surface while the wafers were undergoing the chemical etch. The etch pits become the loci of stress concentrations during tensile loading, resulting in propagation of cracks until fracture of the silicon occurs. From Tables VII and VIII the observation can be made that pull-strength for a mechanically-polished surface is more than twice that for the as-received etch surface. This additional load required for silicon fracture may be due to the fact that no etch pits are present in the polished surface and therefore additional force is needed to initiate a crack in the crystal structure. However, once initiated, this crack propagates in the same manner as do the etch pits.

As noted in Table VII, the pull-strengths for a range of surface roughnesses do not change significantly after the initial drop of 500 g/0.02 cm^2 from the 13 to the 40 to 50 microinch roughness. This could be explained if the concentrations of etch pits formed by the Sodium and Pyro baths are the same. To substantiate these assumptions concerning etch pit effects on pull-strength, a study using standardized etches (14) to produce specific etch pit concentrations will be required.

Although an inverse relation was observed between pull-strength and surface roughness, the mean

value of pull-strength for all wafers plated with the Ni-Cu-Cu sequence exceeded the required 450 g/0.02 cm^2. Only the polished side of the Ni-Cu plated wafers was above the minimum standard, however. In regards to the latter sequence, the apparent effect of deleting the electroless copper layer was to further weaken the cohesive strength of the silicon. Specifically, at Ra = 0.4 microinches, the mean pull-strengths for the Ni-Cu-Cu and Ni-Cu wafers were 2290 and 850 g/0.02 cm^2, respectively. At Ra = 40 microinches, the testing results were 610 and 270 g/0.02 cm^2, respectively. All Ni-Cu wafer failures were due to silicon fracture, which may indicate a reduction of elastic deformation at the point of tensile loading when the electroless Cu layer is present. However, it is difficult to imagine that such large differences in pull-strengths could be the result of such a thin copper deposit.

Calculations on the scatter of data in Tables VII and VIII indicate standard deviations equal to 40 to 60 percent of the mean pull-strength, a range not out of the ordinary for pull-strength tests (6,7,9) on plated contacts.

Numerical results from pull-strength tests are subject to method; i.e., the same wafers tested in this study could have yielded higher or lower pull-strength magnitudes by performing the tensile test with a solder-welded grip instead of an epoxy grip (4). Therefore, numerical comparison of these test results to other studies cannot be directly made unless testing protocols are exactly the same. The lack of a standardized contact pull-strength test, therefore, is a primary obstacle in the field of adhesion measurement (3,4).

CONCLUSIONS

The effect of increasing silicon surface roughness on pull-strength of plated-metal deposits is to decrease the tensile load required for failure. This trend is due to the weakening of the bulk silicon phase when the surface roughness is increased. Formation of etch pits on the silicon wafer surface by chemical etching could be the cause for the observed weakening.

A plating sequence, involving deposition of electroless nickel and copper followed by electrodeposition of copper, provided mean pull-strength measurements exceeding the 450 g/0.02 cm^2 minimum standard when the average roughness of the silicon surface ranged from 0.4 to 130 microinches. However, the quality of the electroless copper layer was very difficult to control. A plating sequence which eliminated the electroless copper layer yielded good plate quality, but, for chemically-etched surfaces, resulted in pull-strengths below the minimum standard.

Comparison of the results of this study to other studies can go only so far as to note the general trends observed. A direct comparison of the numerical magnitudes of test results of this study with others is not posssible until standardized methods of measuring contact pull-strengths are established.

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TABLE I. - SOME PHYSICAL AND ELECTRICAL PROPERTIES OF SILICON WAFER USED IN THIS STUDY

Crystal orientation	Waver thickness, mm	Wafer diameter, mm	Resistivity, ohm-cm	Type
Monsanto wafers				
100	0.472-0.549	102	6-12	P
Semiconductor processing wafers				
100	0.279-0.330	50.8	1.8-2.6	P

TABLE II. - ETCHES USED TO PRODUCE TEXTURES ON SILICON WAFERS

Etch composition	Etch conditions
"Sodium" etch	
150 vol. $Na_2Cr_2O_7$ (3.3 %) 200 vol. HNO_3 (48 %) 100 vol. HF (49 %)	Room temperature 60 sec
"Pyro" etch	
300 ml ethylenediamine 200 ml deionized water 60.C g pyrocatechol	85° C 120 min

TABLE III. - SILICON WAFER SURFACE ROUGHNESS AVERAGE MEASUREMENTS

Surface description	Roughness average, Ra, μin.
Monsanto wafers	
Polished (as-received)	0.4
Etched (as-received)	13
"Sodium"-etched	40-90
"Pyro"-etched	100-130
Semiconductor processing wafers	
Polished (as-received)	0.4
Etched (as-received)	40

TABLE IV. - SILICON WAFER CLEANING SEQUENCE

Sequence step	Procedure
1	Boiling trichloroethylene, 10 min
2	Deionized water (DIW) rinse, 3 min
3	Boiling acetone, 10 min
4	DIW rinse, 3 min
5	Boiling methanol, 10 min
6	DIW rinse, 3 min
7	Boiling sulfuric acid (conc), 20 min
8	DIW rinse, 5 min
9	Boiling methanol, 2 min

TABLE V. - NI-CU-CU PLATING SEQUENCE

Sequence step	Description
1	Place wafers in 6% HF, 30 sec (remove silicon oxides)
2	Immediately transfer to electroless nickel bath; plate 5 min at 80 C; stir vigorously and maintain pH of bath above 8.5 by adding ammonium hydroxide
3	DIW rinse, 5 min
4	Dip in 6% HF, 5 sec
5	DIW rinse, 10 sec
6	Place in electroless copper bath; plate 5 min at room temperature; stir gently
7	DIW rinse, 3 min
8	Dip in 1% HCL, 2 sec
9	DIW rinse, 10 sec
10	Place in electrolytic copper bath; plate 15 min at 9.0 mA/cm^2 surface, room temperature
11	DIW rinse, 3 min
12	Blow dry with anhydrous nitrogen gas

TABLE VI. - COMPOSITION OF PLATING BATHS

Bath	Composition
Electroless nickel	Electronic grade electroless nickel solution, Allied Chemical Corporation
Electroless copper	100 vol. DIW; 10 vol. each of Cu-240A and Cu-240B, Thiokol/Dynachem Corporation
Electrolytic copper	3000 ml DIW; 30 ml H_2SO_4, electronic grade; 600 g copper sulfate

TABLE VII. - CUMULATIVE DATA FROM PULL-STRENGTH TESTS ON PLATED NI-CU-CU DEPOSITS

Roughness average, Ra, μin.	Pull-strength results g/0.02 cm^2				
	Mean	Standard deviation	High	Low	Number of tests performed
0.4	2290	1230	5230	410	40
13	1100	650	3140	130	27
40-50	610	320	2430	210	18
75-90	520	250	1080	150	18
100-130	550	140	1030	170	22

TABLE VIII. - CUMULATIVE DATA FROM PULL-STRENGTH TESTS ON PLATED NI-CU DEPOSITS

Roughness average, Ra, μin.	Pull-strength results g/0.02 cm^2				
	Mean	Standard deviation	High	Low	Number of tests performed
0.4	850	360	3570	160	37
40	270	110	780	110	39