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(NASA-TM-81267) A SOLID-STATE DIGITAL
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A SOLID-STATE DIGITAL TEMPERATURE RECORDER FOR SPACE USE

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INTRODUCTION

A solid-state, digital, temperature recorder has been developed and flown on a joint US/USSR earth-orbital biology mission, Cosmos 1129, September, 1979. It is also to be used with experiments to be flown aboard the Space Shuttle. The recorder is completely self-contained and includes a temperature sensor, all necessary electronics for signal conditioning, processing, storing, control and timing, and a battery power supply. No electrical interfacing with the particular spacecraft on which the unit is used is required. The recorder is small, light, and sturdy, and has no moving parts (figs. 1 and 2). It uses only biocompatible materials and has passed vibration and shock space-flight qualification tests. The unit is capable of storing 2048, -10 to +50°C, 8-bit temperature measurements taken at intervals selectable by factors of 2 from 1.875 up to 240 minutes, and data can be retained for at least 4 months. The basic recorder can be modified to accommodate a variety of applications by adding memory to allow more data to be recorded, by changing the front end to permit measurements other than temperature to be made, and by using different batteries to realize various operating periods.

Stored flight data is read out from the recorder by means of a ground read-out unit. Data is transferred from the flight unit to semipermanent, ultraviolet erasable, read-only memories in the ground unit via a cable. The ground unit contains numerous convenience features and safeguards to prevent accidental loss of data, and has analog, digital and visual LED outputs.

SYSTEM DESCRIPTION

The complete system consists of a flight recorder, a ground readout unit, and any suitable analog or digital recorder. In operation, the flight unit is activated by means of a special plug and placed in the location where it is desired to record temperature. The recorder will then store up to 2048 temperature readings taken at a precise, regular, predetermined intervals, after which it automatically switches to an ultralow power data-retention mode. At some convenient time, after the termination of the mission and recovery, the flight recorder may be connected to the ground unit for data readout. The ground readout unit has protective circuitry to prevent loss of flight data when data transfer is attempted. Subsequently, data is transferred to ultraviolet (UV) erasable, read-only memories by automatic, multicycle programming. There are controls for automatically scanning the data to allow for detection and display of maximum and minimum readings, an interface for outputting data

to a computer, and an analog-to-digital converter to provide signals for an X-Y recorder. Several other convenience features include fast or slow scan selection and direct readout in degrees centigrade through built-in ROM look-up tables. When data has been securely recorded, the data UV ROMs may be erased to allow their re-use on subsequent missions. All units are interchangeable, so that any flight recorder can be used with any ground readout unit.

Recorder

Figure 3 is a block diagram of the flight recorder. The essential elements of the system are:

- A crystal-controlled oscillator with divide-down counters used to provide the basic system timing cycles and memory addressing.
- A temperature transducer and signal conditioner with gain and offset control.
- An analog-to-digital converter.
- A 2048-byte memory array in which the temperature data is stored.
- Control logic.
- Sockets to allow calibration and start-up of the system, and to allow for data transfer to the ground readout unit.
- A battery power supply with regulators.

All timing for the circuit is derived from a precision 18.641 KHz crystal oscillator, whose output is divided down by two serially connected 14-bit ripple counters. If all 28 stages of the counter were used the temperature data-sampling rate would be once every 4 hr. In the instrument described here 25 stages were employed, giving a sampling rate of one reading every 30 min. Other periods, which are multiples of either 2 or 1/2 times 30 min, can be readily accommodated by appropriate selection of the number of counter stages.

The selected divided-down output — in this case, one pulse every 30 min — is used in two ways. In the first, it drives a 12-bit ripple counter, 11 of whose outputs are used to address the 2048-byte data-storage memory array. In the second, it drives the system control circuitry, whose function is to provide additional timing sequences within the basic 30-min period.

The transducer, which, in the initial flight models, is physically located within the flight unit, is a linear, current-output, integrated circuit, temperature sensor, the Analog Devices AD590. Its output is signal-conditioned by scaling and offsetting so as to appropriately interface with the 8-bit analog-to-digital converter. The scale factor and offset adjustments, which involve selection of two resistors, are the means by which

calibration and interchangeability from unit to unit are accomplished. The analog-to-digital converter is a dual-slope, integrating type, whose accuracy is independent of the values of both the integrating capacitor and the clock frequency.

The analog-to-digital converter 8-bit data word outputs are stored in a 2048-byte CMOS memory consisting of four 1024 × 4-bit Harris HM-6514-2 read/write memories.

The power supply consists of four 3-V lithium batteries connected as a ±6-V supply and two regulators, which are used as follows:

- +2.5-V regulator provides a voltage reference used with a precision resistor to provide the system offset control.
- -1.22-V regulator provides a voltage reference used with a precision resistor to provide the analog-to-digital converter reference current.

The temperature sensor is connected between the unregulated -6-V supply and an operational amplifier virtual ground, so that it is effectively powered with 6 V. A regulated supply is not required since the sensor is an integrated circuit with inherent regulation as long as its supply is above 4 V.

The recorder has sockets for two connectors (fig. 4). One connector is used for interfacing to the readout unit and the other is for startup and calibration. Startup or calibration is accomplished by inserting the appropriate one of two plugs into the startup/calibrate socket. The startup plug acts as a power on switch and causes the recorder to begin taking its readings. The calibrate socket applies continuous (as opposed to the normal pulsed) power to the sensor, the signal conditioning circuits, and the analog-to-digital converter, while disabling the crystal-oscillator. In the calibrate mode, continuous analog outputs are available from the signal conditioner and digital signals from the analog-to-digital converter to allow a calibration to be performed.

The system control circuitry consists of two monostable multivibrators for timing, logic gates to appropriately route control signals, and solid-state switches for power-supply and other switching functions.

The system timing may be understood by referring to figure 5. Figure 5(a) shows the timing of data acquisition and retention modes, and the system current drain. The data acquisition mode itself has two modes, so that there is a total of three modes of operation as follows:

- Temperature-reading mode which lasts approximately 50 msec.
- A standby mode which occurs between temperature readings and which lasts about 30 min for the particular flight unit described here.
- A data-retention mode which occurs after 2048 readings have been taken and during which the readings are retained for more than 4 months.

In the temperature-reading mode all circuits are powered for 50 msec and the total circuit current drain is 2 mA. Figure 5(b) shows details of the timing involved in this mode. The counted-down output of one pulse per 30 min triggers two monostable multivibrators, one with a 50-msec period and the other 25 msec. The 50-msec multivibrator output is used to switch power to all circuits. The 25-msec output enables the analog-to-digital converter, which has a 2-msec conversion time and which automatically starts a new conversion every 2 msec as long as the 25-msec enable pulse is high. The first few conversions will be inaccurate as the system is powered up from the leading edge of the 50-msec pulse, but, after a few milliseconds, the system settles and the readings become stable and accurate. All analog-to-digital converted readings for a given read pulse are written into the location in memory reserved for that reading, but only the last conversion is stored since each digital temperature reading is written over the previous one. Once an analog-to-digital conversion is started, it continues, even though the 25-msec enable pulse terminates during the conversion. The 50-msec power-up pulse is long enough to ensure that power is available to the analog-to-digital converter during time "t" in figure 5(b), and to account for the timing variations due to component tolerances and the fact that the 2-, 25-, and 50-msec periods in figure 5(b) are all nominal only.

In the standby mode in figure 5(a), only the crystal oscillator, the timing counters, the address counter, the memory array, and the solid-state power switches with their associated comparator are powered. All other circuitry is off, resulting in a battery current drain of 50 μ A.

After the memory has been filled with 2048, 8-bit temperature readings the system switches to the data-retention mode. In this condition circuits are powered as for the standby mode, except that the crystal oscillator is turned off also, thereby reducing the current to the retention level of 20 μ A. Certain counters and logic circuits are left powered to ensure defined logic levels, since they control and enable the memory where the data is stored.

Readout Unit

Figure 6 is a block diagram of the ground readout unit, the purpose of which is to transfer, record, display, and output the data recorded by the flight unit. The essential elements of the ground readout unit are:

- Input/output interface and logic circuitry which, via a 16-pin connector, controls the transfer of data from the flight recorder to the ground readout unit (fig. 7).
- A 2K, 8-bit, UV-erasable, programmable, read-only memory (UV-EPROM) in which the transferred data is stored.
- UV-EPROMs programmed with look-up tables to convert and scale binary temperature and sample-number data to BCD for driving visual displays.
- Digital-to-analog converters to provide analog temperature and sample-number data for driving an X-Y recorder.

- Buffered binary temperature and sample-number data for interfacing to a computer.

- Front panel controls for the following functions:

- Transfer of data from flight recorder to ground readout unit.
- Searching for maximum and minimum temperature values.
- Fast, medium, and slow-rate data recall.
- UP/DOWN sequential searching through temperature readings in forward or reverse order.
- Outputting data to an X-Y recorder.

Eight of the 16 interface lines on the input/output connector carry bidirectional data. Eight-bit temperature data words go from the flight recorder to the ground-readout unit, while a reserved 8-bit word of all 1's (FF_H) is written into the flight-recorder memory from the ground readout unit to mark the location in memory which follows the last temperature reading. The remaining 8 of the 16 interface lines carry signals and power from the ground readout unit to control the transfer of temperature data from the flight recorder. In addition to power and ground, there are enable and write signals for the CMOS read/write memory, control signals for the analog-to-digital converter, an address counter reset signal, and a clock signal. The interface also contains level-shifting circuitry to allow for a drop in the flight-recorder battery supply to as low as 3.0 V. Three-state logic elements are employed at the input/output interface to allow for bidirectional flow of data.

There are two compare circuits. Compare circuit number 1 is used to detect the presence of the reserved 8-bit data word (FF_H), which marks the end of the sequence of temperature readings. Compare circuit number 2 is used in the detection of maximum and minimum temperature readings. This circuit operates in such a way that if there is more than one reading having the maximum or minimum values, all may be displayed along with their addresses.

Data are stored in the ground readout unit in a 2048-byte memory comprised of two 1024-byte, UV-erasable, 2708 programmable read-only memories, addressed by an 11-bit counter. Each bit in these UV-EPROMs is programmed 256 times with a 400- μ sec programming pulse to ensure accurate data transfer and semipermanent (10-year) retention.

There are two temporary registers to allow for outputting of temperature data words and their corresponding addresses. Register number 1 holds 8-bit temperature words, while register number 2 holds the corresponding 11-bit sample numbers which are regenerated by the ground-readout unit internal counter.

The 8-bit temperature data in register number 1 is in binary form so it requires conversion to binary-coded decimal (BCD) for driving the light-emitting diode (LED) readout, which displays temperature in degrees Centigrade. This conversion is accomplished through look-up tables stored in a pair of 1702 UV-EPROMs. Similarly, look-up tables stored in four 2708 UV-EPROMs are employed to convert the binary quantities stored in 11-bit register number 2 to BCD for display of the sample number corresponding to the temperature simultaneously being displayed.

Both binary temperature and sample number words are converted to analog form via digital-to-analog converters to allow a temperature/time plot to be made on any conventional X-Y recorder, storage oscilloscope or strip-chart recorder (fig. 8). Three-state buffer number 2 strips the 8 most significant bits from the 11-bit sample-number counter output and uses them as dummy temperature data to facilitate setting up the X and Y scales on the X-Y recorder. The raw, binary temperature and sample number data are also outputted via digital buffers to permit interfacing with an external computer.

Provision is made for the inclusion, at a later date, of a third look-up table capable of storing 256 8-bit words in a 1702 UV-EPROM. This may be employed when future flight recorders are built having input sensors other than the temperature transducers used in the current model and will enable corrections to be made should any new sensors be nonlinear. Since the current temperature sensor is linear, the socket for the linearizing UV-EPROM in this model is simply jumpered across.

The front-panel controls allow the user to perform all necessary operating functions and there are several convenience features as well. After a connection is made between the flight recorder and the ground readout unit, depression of the TRANSFER button starts the multiple-step programming sequence and results in transfer of data from the CMOS read/write memories in the flight recorder to the UV-EPROMs in the ground readout unit. This takes about 5 min.

When data has been transferred, it can be recalled at any of three rates by depressing the FAST, MEDIUM, or SLOW buttons. Data recall consists of recording analog or digital outputs or observing the LED displays of temperature in degrees Centigrade. An UP/DOWN control is provided as a search aid to permit recall of data in either the original recording sequence or in reverse.

The SEARCH controls scan all temperature data for maximum and minimum readings, and, should either of these recur, have the capability of sequentially displaying the sample numbers corresponding to all maximum and minimum temperatures.

The OUTPUT MODE switch on the rear panel implements the internal analog output calibration feature in which the 8 most significant bits of the 11-bit address counter are used as dummy temperature readings. The DATA END MARKER may be disabled by the override switch on the rear panel.

CIRCUIT DESCRIPTION

Recorder

System clock- Integrated circuits CD4060BK and CD4020BK provide the basic system timing cycles and memory addressing (fig. 9). CD4060BK is a combination 14-bit Ripple-Carry Counter and oscillator whose output is serially connected to a CD4020BK Ripple-Carry Counter. Together they divide the oscillator frequency with up to 28 stages of binary reduction. If all 28 stages of the counters are used, the final output period would be 4 hr.

The oscillator section of the CD4020BK is used in a Pierce configuration which consists of a single inverter with the crystal connected between inverter output and input, with two phase shift capacitors. This type of oscillator has excellent stability, even at low currents. The crystal is a miniature, parallel-resonant Statek CX-IV operating at 18.641 KHz with a factory calibration of $\pm 0.003\%$. The operating frequency, which is relatively low, was chosen to minimize current drain and still allow the use of a small-sized crystal. The oscillator current is reduced further by limiting its supply current by means of a resistor in series with V_{DD} of the CD4060BK. This resistor also reduces the amplitude of the output voltage to about 90% of V_{DD} , a lower logic level which is nevertheless adequate to drive the CD4020BK reliably over a temperature range from -30 to $+60^{\circ}\text{C}$. Nominal oscillator current is 25 μA .

Output pads are provided on the printed circuit board so that any binary stage from 22 through 28 can be selected. This provision allows a choice of timing rates from 3-3/4, 7-1/2, 15, 30, 60, 120, and 240 min. At the 30-min rate, the accumulative timing error is less than ± 5 min over a 6-week period during which 2048 temperature readings are recorded. The selected timing pulse determines the temperature sampling rate and initiates additional timing sequences which control the circuits used during the brief data-recording period. These circuits activate the sensor circuitry and the analog-to-digital converter, advance the address counter, and generate a read cycle for storing the digital data in a memory array.

Temperature transducer and signal conditioner- The temperature transducer is a two-terminal, AD 590 integrated circuit which produces a current proportional to absolute temperature. For supply voltages above +4 V, the current output is 1 $\mu\text{A}/^{\circ}\text{K}$. Linearity is within $\pm 0.3^{\circ}\text{C}$ over a temperature range of -55°C to $+150^{\circ}\text{C}$ at a constant excitation of +5 V. Power supply rejection is 0.2 $\mu\text{A}/\text{V}$ for excitation voltages greater than +5 V. Supply variation in this circuit causes a maximum current change of 0.1 μA , or 0.1°C equivalent error.

Although in this application the transducer is located within the flight recorder, remote sensing is also practical since the device not only is sealed in a TO-52 package, but is insensitive to voltage drops over long lines since it has a high-impedance current output. The sensor chip is electrically isolated from the case so that grounding the package is optional.

The transducer is calibrated at the factory to produce 298.2 μA at 298.2°K (25°C). This is done by trimming the scale factor for each device to

within $\pm 0.5^{\circ}\text{C}$ at $+25^{\circ}\text{C}$. In addition to this calibration error, other variances from the actual temperature are the result of slope error and curvature, mostly at the temperature extremes of -55°C and $+150^{\circ}\text{C}$.

A signal conditioner is used which both minimizes these errors and eliminates the current bias produced by the temperature differential from absolute zero to the higher measurement range. This is accomplished by a circuit which provides a two-temperature trim for current offset and slope.

The AD 590 transducer is connected between the unregulated -6 V supply and the virtual ground at the inverting input of operational amplifier CA 3078AT. A positive current from the voltage regulator AD 580U is summed with the negative current of the temperature sensor via resistor R_1 . Current offset and transducer calibration error can be adjusted by trimming R_1 , so that the output of the amplifier is 0 V with the sensor exposed to the lowest temperature, in this case -10°C . The amplifier gain is controlled by R_2 . It is adjusted for a nominal output of $+3\text{ V}$ at the highest temperature of $+50^{\circ}\text{C}$. Thus, nonlinearity is the major contributor to error over temperature and is limited to the curvature spread between -10°C and $+50^{\circ}\text{C}$. Resistors R_1 and R_2 are fixed metal-film resistors with temperature coefficients of $10\text{ ppm}/^{\circ}\text{C}$. Fixed resistors are used since the recorder must operate under high g impact and vibration. Typical resistance values are $R_1 = 9.8\text{K ohms}$ and $R_2 = 47\text{K ohms}$ for a gain of about 4. The $+2.5\text{ V}$ regulator has a temperature coefficient of $10\text{ ppm}/^{\circ}\text{C}$ and a line regulation of 1 mV maximum.

The micropower operational amplifier has an equivalent output error of $\pm 0.2^{\circ}\text{C}$ due to voltage and current drift over the range of -10°C to $+50^{\circ}\text{C}$.

The transducer and signal conditioning circuitry operate from a $\pm 6\text{ V}$ supply and consume a nominal $\pm 1\text{ mA}$ of current.

Analog-to-digital converter- The ADC-ET8-BM is an 8-bit, low-power, integrating-type of analog-to-digital converter housed in a 24-pin dual in-line package. Circuits include an integrating amplifier, comparator, current switch, internal clock, counters, latching output buffers and control logic, all of which are fabricated using monolithic CMOS techniques. External components which must be provided are an integrating capacitor, two input-current control resistors, a negative voltage regulator, a supply-current bias resistor, a bypass resistor, and three bypass capacitors. The two external input resistors, along with the analog data and reference voltages, determine the current inputs to the single-ended ADC. The 300K ohm resistor allows a full-scale input current of $+10\text{ }\mu\text{A}$ when the analog output of CA3078AT is at $+3\text{ V}$. The 60.4K ohm resistor and the -1.22 V regulator, LM113H, provide a fixed reference current of $-20\text{ }\mu\text{A}$. Conversion accuracy is directly dependent on the stability of these components, so the resistors are metal film with a temperature coefficient of $\pm 10\text{ ppm}/^{\circ}\text{C}$ and the voltage regulator is stable within $\pm 0.06\%$ over a range of -10 to $+50^{\circ}\text{C}$. The 68 pf , ceramic integrating capacitor is shared during conversion by both the input and reference currents, so that conversion accuracy is independent of its stability.

Conversion is done by incrementally balancing current pulses derived from the reference source against oppositely signed continuous current applied by the analog data. The current pulses are generated by a comparator which monitors the output of the integrating amplifier. When the output deviates from zero, the comparator changes state, thereby closing a switch which introduces reference current to the summing input of the integrating amplifier. After autocorrection to zero, the comparator and switch return to the original state. The number of current pulses required to maintain the summing input near zero is counted and the binary result is latched into the output. The counter also resets the input circuitry and provides an end-of-conversion signal. All binary ones in the 8-bit word represent the high temperature reading and an analog output of +3 V. Low temperature is represented by binary zeros and an analog 0 V. Conversion accuracy is independent of the internal clock frequency.

Once a conversion is initiated, the cycle cannot be interrupted until the data is latched in the output. If the start convert control is held high, the converter will continuously refresh the data reading at a nominal 2 msec rate. The last reading will always be completed and latched at the output as long as the ADC is powered, regardless of the logic state at the start convert input. The outputs are three-state controllable and therefore may be switched to a high impedance or "off" state. This allows output connections to be bus organized for interfacing with attendant circuitry.

Although the ADC requires a ± 6 V supply, all digital inputs and outputs are 0 to +6 V, the negative supply being used primarily in the analog section of the converter. Supply current is set with the 680K bias resistor for a nominal ± 800 μ A at +25°C. Power supply sensitivity is typically $\pm 0.15\%$ as used in this system over a temperature range -10°C to +50°C and over the full operating life of the batteries.

Address counter and memory array— The address generator is a CD4040BF 12-stage ripple-carry binary counter and 11 of the outputs are used to address the memory array through a total of 2048 temperature readings with binary stage 12 providing a memory full signal.

The data-storage memory is composed of a four HM-6514-9, 1024×4 , static CMOS RAM array, which has the capacity to store 2048, 8-bit words. Each HM-6514-9 has a 10-stage address input and a 4-bit data word input/output. The data lines are three-state and can be forced to a high impedance or "off" state for memory expansion. The devices are paired to accept an 8-bit data word with a storage capacity of 1024 words and when the first pair is filled, the memory is automatically expanded to the second set for a total storage of 2048 words.

The HM-6514-9 has chip-enable and write-control inputs, which allow either a read or write cycle to be selected.

Power supply requirements for each unit are typically 0.1 μ A standby and 0.01 μ A for data retention at +6 V. Operating supply current is approximately 3 μ A at a 2 msec writing cycle and data can be retained down to a supply level of +2 V.

Control logic- The control logic resets all digital devices to their initial startup levels, activates the signal conditioner and analog-to-digital converter (ADC) during temperature readings, routes signals during conversion, addressing, and storing of data, and provides interface functions used during transfer of data to the temperature readout unit (TRU).

When connector B is placed into the receptacle located on the printed-circuit board, battery power is applied to the circuitry and all digital controls are reset to their start levels. First to be reset is the address counter CD4040BF. A high level at pin 11 sets it to an all-zero state. Next, clock counters CD4060BK and CD4020BK are reset with a high level at pins 12 and 11 to their all-zero state. The CD4040BF reset level returns low as determined by the RC time constant at pin 11. When binary Q_{12} at pin 1 is zero, the clock reset inputs are allowed to return low as determined by the RC time constant at their inputs. This part of the system is now operational with the address at its starting point.

CD4098BK is a dual monostable multivibrator, which controls the power to the signal conditioner and ADC, and provides the advance signal for the address counter. When power is turned on, the resets at pins 3 and 13 are held low for a period controlled by the RC time constant at these pins, thereby preventing output pulses during startup.

The counted-down output pulse from the clock counter triggers the two monostables at the start of each temperature reading. Trailing-edge triggering, used at pins 5 and 11, is consistent with the clock, whose state advances on negative transitions.

Nonretriggerable output Q_2 has a period of 50 msec as determined by time constant T_2 . This positive pulse activates the ± 6 V supply used by the transducer, signal conditioner, and ADC. Because Q_2 is a 0 to $+6$ V pulse, a voltage translation must be made to control the ± 6 V supplies. The new logic level is provided by the micropower comparator L161AL and the two solid-state switches CD4066BK, these devices being continuously powered by the ± 6 V supply. At the onset of Q_2 , the comparator changes state, which in turn switches the two CD4066BK bilaterals to their "on" state. This applies the ± 6 V to the switched power lines. The transducer and signal conditioner are now measuring temperature and the ADC is ready for conversions. Settling time is less than 5 msec.

Output Q_1 has a period of 25 msec as determined by time constant T_1 , a positive pulse that is applied to the Start Convert input of the ADC. As long as it is high, the converter is in a free-running mode with conversions occurring at a 2-msec rate. After several conversions, Q_1 returns low to stop further digitizing; however, even though Q_1 is low, the last conversion cycle will be completed with its 8-bit digital word latched at the output. This data is valid since the circuitry is fully settled.

Negative pulse \bar{Q}_2 of 50 msec is applied to the input of OR gate CD4071BK, which routes the Busy output of the ADC, via the following OR gate CD4071BK, to the Chip Enable inputs of memory pair A and C. The Write Enable inputs are already low, so that the memories are in a dedicated, writing only mode.

Each Busy output provides the appropriate time and level requirements for a memory-write cycle at the end of each data conversion, and each conversion is written over the previous one during the 25 msec recording period and the last conversion is stored.

The trailing edge of the 50 msec pulse Q_2 is used to advance the address and, since at this time the previous address already has been filled with data, the system is ready for the next temperature recording, which occurs after an interval of 30 min. Time periods T_1 and T_2 are not critical as they do not affect either conversion or timing accuracy. To insure that the last conversion is completed and stored in the memory before the power is turned off T_2 is made longer than T_1 . It is also sufficiently longer than T_1 so that the last 2 msec conversion will be completed before the address is advanced for the next reading.

When memories A and C are filled, Q_{11} at pin 15 of CD4040BK goes high which removes the ADC controls from this memory pair. The inputs/outputs of memories A and C are now in the high impedance state and the Busy output of the ADC is now routed to memory pair B and D. When memories B and D are filled, Q_{12} at pin 1 of the address counter goes high, stops the clock oscillator, and holds the outputs of both clock counters at zero. When the oscillator is off, the recorder is in its lowest current mode of about 20 μ A. Thus, the recorder has three current levels. First, there is the continuous clocking and holding current of about 50 μ A. Then, there is the current of 2 mA during the 50 msec temperature readings which results in a total drain at this rate of less than 2 min over the full 2048 data capacity. And finally, there is the data retention current of 20 μ A.

Other logic controls are used during calibration and transfer of data to the ground readout unit. This recorder circuitry is interfaced to external support equipment by means of connector A.

Connector A is a 16-pin, in-line receptacle mounted on the recorder printed circuit board. It includes connections for the 8-bit data word, the ADC Enable input, the dual monostable reset, the address clock input, the address reset, the memory Chip Enable \bar{E} , the memory Write Enable \bar{W} , +6 V power, +6 V switch control, and ground. Where appropriate, series resistors are employed to give the TRU priority over any directly connected recorder circuitry.

The controls for the +6 V switch and the ADC Enable are needed so that ADC can be powered and placed in its high-impedance output and nonconverting mode prior to transferring the memory data. At the same time, the CD4098BK is held in its reset condition during data transfer. However, if a data conversion is in progress when transfer is attempted, the comparator L161AL and switch CD4066BK at pin 15 of the connector block external control of the ADC until this conversion has been stored in the memory. Interface timing is such that no other transfer operations are scheduled until the last conversion is allowed to be completed, a scheduled delay is about 100 msec.

The +6 V connection is used to sample the control-logic level of the recorder for proper interfacing between the two units prior to sending command signals for data transfer.

If at the time of transfer the memory is not filled, the TRU writes an all "ones" 8-bit word in the recorder memory to mark the end of data. If the memory is filled, binary Q_{12} at pin 1 of the CD4040BF is high, which prevents the TRU from writing over the last data word by means of the OR gate CD4071BK at pin 13 of the connector. After the write command has been given, the memories are placed in a read mode and the address counter is reset. The TRU clock now controls the address counter during the data-transfer process.

Connector B applies the battery power to the system and engages the input of the comparator L161AL to the output of CA3078AT. The comparator changes state slightly below the +3 V full scale output, which closes switch CD4066BK at the LSB pin 12 of the ADC, thus preventing an all binary ones from being recorded. This word is therefore exclusive to the data-transfer operation.

All logic circuitry is continuously powered whenever the recorder is in use.

Batteries- The recorder power requirements are ± 6 V at a continuous current of 50 μ A with 2048 pulse discharges of 2 mA for 50 msec. In addition to these currents, there is a holding current of 20 μ A which occurs after the memories are filled. Temperature readings occur every 30 min so that it takes about 6 weeks to fill the memories and since data may not be transferred immediately, another 3 weeks of data retention is highly desirable.

Battery capacity is limited by the package constraints of the recorder, so that the volume available for a ± 6 V supply limits the battery capacity to about 250 MAH if four 3 V cells are used.

An operating temperature range of at least -10°C to $+50^{\circ}\text{C}$ is required, so the cells selected were Sanyo Lithium-Manganese Dioxide, CR2430H, also known as LF 1/2 WH. These cells have an open-circuit voltage of 3.10 and their rated capacity is 160 MAH with an operating temperature of -20°C to $+50^{\circ}\text{C}$. Their size is 25.5 mm diam with a thickness of 3 mm and they weigh 4 g.

Cell output is poorest at low temperatures so that at -10°C and a continuous drain of 50 μ A, the voltage ranged from 3.00 at a startup to 2.86 at 160 MAH discharge. Pulse-voltage depths for 50 msec at a 3 mA discharge rate ranged from 2.84 at startup to a 2.48 at 160 MAH discharge. The longest settling time for the voltage to stabilize during pulse discharges was 5 msec. At $+50^{\circ}\text{C}$ the result for the 50 μ A load was 3.08 V at startup to 2.88 V at 160 MAH discharge. Pulse depths were 3.04 V at startup to 2.80 V at 160 MAH. The greatest possible voltage variation is between battery startup at $+50^{\circ}\text{C}$ and the 160 MAH discharge point at -10°C and, for the 50 μ A curves, being 0.22 V. The pulse depth variation for these conditions is 0.32 V.

For a dual, two-cell output of ± 6 V, the variations of pulse-depth voltages are about ± 0.64 V, a variation that affects the data accuracy as reported in the descriptions of the transducer, signal conditioner, and ADC.

The clock is affected mostly by the continuous 50 μ A drain and little by the 50 msec pulses. Its frequency was measured at 18.6412 KHz at +6 V and 18.6412 KHz at +4.8 V; thus, frequency variations due to voltage fluctuation are very minor.

A conservative current drain of 3 mA was used in the tests of pulse discharge rather than the typical 2 mA load of the system. As used in this system, the batteries will provide at least a 6-week recording period and an additional data-retention capability of 12 weeks.

The cells were tested for seal evaluation and outgassing. During this test, four cells were placed in a chamber at a pressure of 10^{-6} torr and each cell was short-circuited. A mass spectrometer did not detect any outgassing at the onset of the short circuit or after 15 min of continuous monitoring. Upon immediate removal of the cells from the chamber, no evidence of heat was detected. The cells use a crimp-seal type of construction, a nonaqueous, organic electrolyte and their shelf life should be several years.

Calibration considerations- The temperature sensor, AD590, has a self-heating effect which is dependent upon the thermal environment to which it is exposed. The increase in current output due to self-heating is predictable and proportional to absolute temperature, so that the signal conditioning circuitry can be trimmed with the sensor in the same thermal medium, such as air, in which it will be used; the scale factor trim will then compensate for this effect over the entire temperature range. Since in this application the sensor is located within the recorder package, the entire recorder, with the exception of the offset and gain control resistors, R_1 and R_2 , is placed in a temperature chamber which uses air as the thermal medium. With the sensor and recorder exposed to the low calibration temperature, a potentiometer external to the chamber is substituted for resistor R_1 and adjusted for an all-zero output from the ADC at connector A. Next the chamber is raised to the highest temperature and a second potentiometer, substituting for resistor R_2 , is adjusted for an all ones digital output. The resistance values of the potentiometers are measured with a digital ohmmeter, after which metal film resistors are selected at these values and mounted on the recorder circuit board. This technique provides a two-point calibration which takes into account total system drift with temperature, except for resistors R_1 and R_2 , and also compensates for the effect of self-heating. Error is limited mostly to the nonlinearity between the two calibration points, and the drift of resistors R_1 and R_2 at a rate of 10 ppm/ $^{\circ}$ C. If an application were to require the sensor to be mounted remotely from the recorder, then calibration should be done with the sensor alone in the temperature chamber and the recorder at room temperature, or the expected ambient temperature. This procedure would again optimize performance. The temperature chamber may require several hours to stabilize precisely at the selected calibration point; therefore, the recorder should not be in the high current drain converting mode, so as to conserve the battery during the stabilizing period. When an adjustment trim is ready to be made, the ADC and signal conditioner are first activated, after which the start convert input is held high, allowing the ADC to be in the free-running mode which provides an updated output every 2 msec.

Readout Unit

The temperature readout unit (TRU) has been designed with a random-logic approach. The circuit card schematics are given in appendix B along with the backplane wiring list. The circuit description which follows frequently references these drawings.

System timing- The TRU derives two basic timing sequences from the system clock for control of all functions. These sequences are shown in figure 10. Sequence A is used for programming the 2708 data storage PROMs, while Sequence B is used mainly for recalling data.

Circuit card number 6 contains the clock and decoding logic for these timing sequences. U1, the 4047, is the system clock which runs at approximately 32 KHz and which drives the binary counter (U2) whose outputs are decoded into the two timing sequences. Synchronization with the start of the sequence is provided by using the Q₅ output of the binary counter (U2) as a strobe to enable the timing latches (U9, U10) only at the beginning of the sequence. When a sequence is requested by bringing its particular sync line high, the reset command to the D flip-flop (U8B) is removed. When Q₅ falls, signaling the beginning of both sequences, U8B is clocked and the output gated with the appropriate sync request line. This commands the selected timing latch, U9 or U10, to pass the desired sequence.

When the sync line is lowered, the flip-flop is reset and the 4042 outputs latch in their present state. Further gating is required to provide timing signals which return to their nonasserted state when the sync line is lowered. These signals are distinguished by the suffix "R" as shown on the drawing for card 5.

Data transfer- Data transferred from the flight recorder is stored in a pair of 2708 UV-EPROMs located in the front-panel, zero-insertion-force sockets. Card one contains the DC-to-DC converter which provides the 27 V required for the program pulses, as well as the logic controlling the bidirectional, tristate data lines.

The $\overline{\text{CS/WE}}$ control (pin 20) on the PROMs are three-level inputs instructing the data lines to be inputs (12 V), outputs (0 V) or in the tristate mode (5 V). The most significant address bit (A₁₀ at EC:4) selects the addressed PROM while disabling the other. A high level at EC:5 will tristate both memories allowing the data bus to be driven by the eight most significant address bits through U3 and U7 on card 9. This is the mechanism of the internal data ramp whose function is described in the operation manual (appendix A). A high level at EC:7 will select the write mode ($\overline{\text{CS/WE}} = 12 \text{ V}$) on the PROM addressed by A₁₀. EC:6 is the active low program pulse control, applying 27 V to the selected PROMs' program pin when asserted.

Data transfer control- Control of the transfer process is handled by card 2. The 4528 dual one-shot (U1) provides debouncing of the COPY switch and, through its enable control (pin 3), disables the switch after an error, during the plot mode, or during a transfer sequence.

When D flip-flop 2B is set, the output at edge connector pin 5 goes low signaling the start of a possible copy sequence. This signal is sent to the control interface on card 8, disabling the flight recorder and placing "FF" on the data lines. The output of flip-flop 2B is gated with the 100 msec debounce pulse on card 5, generating a request for the general timing sequence which has been delayed by 100 msec. This ensures that the recording sequence is not interrupted causing erroneous data to be stored.

The first pulse of the general timing sequence, GT1R, clocks flip flop 2A only if the flight recorder battery voltage is above 2.5 V (EC:S) and the first location of the PROM memory is erased (EC:14). Good data is thereby protected from being written over if the operator forgets to change the PROMs while the data from several recorders is being recovered.

If either of these conditions are not met, the second general timing pulse, GT2R, will clock flip flop 3B causing the copy sequence to be aborted and the error light to come on.

Assuming the conditions are met and flip flop 2A is set, the SWITCH signal at EC:C will go low closing the interface switches on cards 8 and 9. When GT2R is asserted at EC:L, the flight-recorder memory enable control (EC:8) is asserted. Since the write control (EC:7) is already asserted this is taken as a write command by the temperature recorder memory, which stores the Hexidecimal word "FF" at the end of the valid data in the temperature recorder. Now GT3R resets flip flop 2B, disabling the general timing sequence and "FF" data word. Flip flop 3A is now set and requests the transfer timing sequence.

The recommended programming sequence for the 2708 has been observed by using a 256 pass program cycle with each of the 2048 eight bit words being programmed with a 400 msec pulse. EC:K goes high at the start of the program sequence which causes the RESET command to the flight recorder address counter to be asserted at EC:9. The first program pulse will reset flip flop 2A (through EC:D) causing the reset command to be negated at the TRU address counter (EC:5), the flight recorder address counter, and the program cycle counter (U4). The program sequence is repeated over and over until the program cycle counter has counted 256 cycles of the programming sequence and U3A is reset. At this point the SWITCH control is returned to high and the transfer sequence is over.

Controls and data interface- The 16 interface lines are divided into eight bits of data, six recorder control signals, and the power and ground leads.

The data interface (card 9) is fairly simple. U6 and U10 are solid-state switches which close on command from the transfer control logic on card 2. U1 and U2 are the inverting tristate buffers which allow the data and marker to be recorded by the temperature recorder. Note that these buffers are powered by the temperature recorder battery. U5 and U9 are buffers which provide the level translation when the data is transferred to the readout unit. U4 and U8 are tristate buffers as are U3 and U7, which allow the data

bus to be controlled by the flight recorder data, the internal data ramp, or the front panel PROMs.

The controls interface is located on card 8. When the interface plug is first inserted, the flight recorder and readout unit grounds are connected through EC:21. The analog section of the flight recorder is powered-up by returning the battery voltage (EC:Y) to the analog section control (EC:20). When a data transfer is selected EC:5 will drop low, causing the first bank of solid state switches (U3) to close. This disables the analog to digital converter in the flight recorder through EC:X and also presents the battery voltage to the comparator U4.

The output of the comparator will switch high if the flight-recorder battery voltage is above 2.5 V. As explained previously, the data transfer control requires this signal to be high for the sequence to continue.

Reed relay (K1) switches the battery voltage to the level-shifting buffers on card 8 (U1) and card 9 (U5 and U9). The resistor and diode provide assurance that the battery voltage will not fall due to the higher current demand during readout. The memory **WRITE** and **ENABLE** controls are operated through EC:V and EC:18. The address counter **CLOCK** and **RESET** lines come from EC:W and EC:19.

Data recall- The recall of data is controlled by the logic on card 5. The three user selectable recall speeds are gated with three different stages of the delay counter (U3). In the quiescent state with no recall speed selected EC:D, E and F will all be low. This will keep U3 reset and both D flip flops 6A and 6B are reset due to the power-up circuitry. The computer interface data valid flag (EC:21) is low and so is the general timing sequence request line (EC:U).

When recall is selected, say at a medium speed, EC:E will be pulled high causing the reset to be negated at the delay counter (U3, pin 11). The delay counter clock (EC:4) is being driven by the system timing counter output Q₅ on card 6. After eight stages of delay have been counted, the Q₈ output is gated with the medium-speed selection to set flip flop 6B. This instantly resets the delay counter and requests the general timing sequence (EC:U). CT1R clocks the address counter on card 7 to the next data point and GT3R clocks 6B to a reset state. This negates the reset on the delay counter and the process repeats until the recall mode is no longer selected or EC:J goes high indicating that the address counter is pointing to the last valid data point as determined by the decoding logic on card 10.

Plot mode- The PLOT MODE refers to situations in which a continuous scan through the data is required, for example, while driving an X-Y recorder or while interfacing with a computer. Card 3 contains the logic which allows recall commands to be passed directly to card 5 from the front panel recall switches or to be latched automatically by the PLOT logic.

The 4528 dual one-shots (U1A, U1B) provide debouncing of the PLOT switch as well as disabling the switch during data transfer or after an error

condition. J-K flip-flop 2B is set up so that its outputs complement upon every clock pulse. When Q is low on this flip flop the PLOT mode is selected. After a power-up reset or when the address counter points to the end of valid data space the PLOT mode is deselected by setting 2B through pin 9.

Normally, with the PLOT mode not selected, flip flops 2A, 3A and 3B are held RESET, which means a recall command at EC: V, 19 or W is necessary to clock the corresponding flip flop and assert the recall command at EC: D, E or F. This condition will remain until the entire remaining data has been scanned or until the PLOT mode has been deselected by clocking 2B again.

Data search- The data search feature operates as follows: The 8-bit data register on card 10 (U8, U10) and 11-bit address register on card 7 (U6, U7, U8) are loaded with address 0 and the corresponding data. If MAX is pressed this stored data is compared (U9, U11 on card 10) with the next data point and replaces the previously stored value only if it is greater than or equal to the old value. The entire memory is scanned, resulting, after one pass, with the maximum data value and the last address at which it occurred stored in the registers. Now the second pass begins, but this time, when a value equal to this maximum value is encountered, the pass stops and this location is displayed. When MAX is pressed again, the TRU displays the next location with data equal to that value. Operation of the minimum value search is similar.

The decoding and controlling logic for the data-search function is contained on card 4. The actual comparison is performed by the two 4063 4-bit magnitude comparators U9 and U11 on card 10. The three possible comparator outputs ($A > B$, $A = B$, and $A < B$) appear on card 4 at EC: 11, 12, and 13. These three comparator outputs are gated with the outputs of U1B which indicate the particular search mode of interest. The output of U10A will be high whenever the data point being currently addressed is greater than or equal to (MAX mode), or less than or equal to (MIN mode) the previously stored value. U10A will also go high whenever the data recall mode has been selected. This signal is gated with GT3 and will cause the register LATCH command to go high. In this way the registers are updated in both the search and recall modes.

As was explained earlier, the first pass through the data is preceded by loading the registers with sample 0. This is done by gating the output of U8C which will be high at the beginning of a new search mode, with GT2R. U9A performs this function which causes the registers to be loaded. U8C has already reset the address counter through EC:R.

The control logic for the search mode starts with the two dual one shots (U2, U3), which provide debouncing of the MAX and MIN switch. The one-shots also inhibit these switches during a transfer or plot sequence or after an error. Flip-flop 1B is set by selecting the MAX function and reset by the MIN function. Its outputs will always reflect which search mode was last selected. Flip flop 4B is clocked to $Q = 0$ by selecting either the MAX or MIN function and set to $Q = 1$ by selecting any other function. Thus, its output is low whenever the search mode was the last mode selected. Flip flop 4A is also clocked by selecting either the MAX or MIN function. Its input is the output of flip flop 4B which is 1 only if the search mode is being selected

for the first time. So when the Q output of U4A goes high it means that the search mode has just been selected for the first time. U4A Q output is ORed with the outputs of flip flops 5B and 1A, one of which will be clocked each time the search mode selected changes from MIN to MAX or from MAX to MIN. The ORed outputs of U4A, U5B, and U1A give one signal which when high means that a new search mode is being started. The ORed output sets flip flop 7A which stays set for the first, uninterrupted pass through the memory, but is reset for the second pass. The Q output of U7A is one of the three signal sources which are ORed (U8B) to give the request for the general timing sequence at EC:N. Since U7A is set for one entire pass of the data, the general timing sequence will be enabled for at least that long.

At the end of the first pass through the data U7A is reset. The Q output of U5A is also low, which leaves the signal at the output of U9B as the only input to U8B. As explained previously, the output of U8B is used to request the general timing sequence. When a data point equal to the extreme value found on the first search is found, the output of U9B will go low. This causes EC:N to go low, deselecting the general timing sequence. The registers contain the extreme value and its first location. Now as the same extreme mode is selected U5A will be clocked, Q will go high and the general timing sequence will be requested. The first timing pulse will return Q low and the search for the next extreme value location will be under way.

LED outputs- The LED displays used in the TRU are HP 7300 type which contain BCD decoding and driving circuitry. Card 11 contains two 2708 PROM look-up tables which are programmed with the conversion from raw binary data to degrees celsius in leading zero blanked, signed BCD form for the displays.

The binary word "FF" is converted to "DDDD" which is decoded by the HP 7300's as four dashes. This is to emphasize that this value is a system code and not valid data.

Card 13 holds the look-up table which converts the 11-bit binary address to a four-digit, leading-zero blanked BCD address.

Analog and binary outputs- The TRU provides analog outputs of address and data information (time and temperature) for driving any analog recording device. Also, the raw binary information is available with a data valid flag (card 5) for interfacing with a computer.

Card 14 provides these two output modes for the address information. The D/A converter used gives a 0 to -10 V full-scale output which is inverted to provide the 0 to 10 V analog output. The binary outputs are buffered with 4050 CMOS buffers.

Card 12 contains the same output features for the temperature data. There is also a 2708 PROM look-up table which may be used to linearize the output from a nonlinear transducer. If this is not necessary the socket should be jumped from A7 to O7, A6 to O6, . . . , A0 to O0.

CALIBRATION

Six recorders were calibrated at high and low temperatures over a period of several hours. The units were calibrated in two separate batches. One batch consisted of recorders 1, 2, and 3; the other consisted of recorders 4, 5, and 6, as shown in table 1.

In table 1 "TR" refers to the temperature read from the recorder and "TC" refers to the temperature read from the calibration thermocouple.

TABLE 1.- CALIBRATION

(a) Low temperature calibration
(Units 1, 2, 3)

Time	TR 1	TC 1	TR 2	TC 2	TR 3	TC 3
10:15 a.m.	-5.3	-5.4	-4.1	-4.1	-5.1	-5.0
10:45 ↓	-5.8	-5.9	-4.6	-5.1	-5.3	-5.4
11:15 ↓	-5.5	-5.5	-4.6	-4.8	↓	-5.1
11:45 ↓	-5.5	-5.7	-4.6	-5.0	↓	-5.3
12:15 ↓	-5.3	-5.5	-4.4	-4.8	↓	-5.1

(b) High temperature calibration
(Units 1, 2, 3)

Time	TR 1	TC 1	TR 2	TC 2	TR 3	TC 3
12:15 p.m.	35.2	34.7	35.2	34.5	34.9	34.6
12:45 ↓	↓	↓	↓	34.5	↓	34.6
1:15 ↓	↓	↓	↓	34.5	↓	34.7
1:45 ↓	↓	↓	↓	34.6	↓	34.7
2:15 ↓	↓	↓	↓	34.4	↓	34.6

(c) Low temperature calibration
(Units 4, 5, 6)

Time	TR 4	TC 4	TR 5	TC 5	TR 6	TC 6
1:45 p.m.	-4.8	-5.0	-5.8	-6.0	-6.7	-6.4
2:15 ↓	↓	-5.1	-5.8	-6.0	-6.9	-6.5
2:45 ↓	↓	-4.8	-5.5	-5.7	-6.7	-6.2
3:15 ↓	↓	-5.0	-5.5	-5.7	-6.7	-6.4

(d) High temperature calibration
(Units 4, 5, 6)

Time	TR 4	TC 4	TR 5	TC 5	TR 6	TC 6
6:15 p.m.	34.5	34.2	35.4	34.8	36.8	36.4
6:45 p.m.	34.5	34.3	35.6	34.8	36.8	36.4
7:15 p.m.	34.5	34.2	35.4	34.9	36.6	36.4

APPENDIX A

OPERATION MANUAL: TEMPERATURE READOUT UNIT

General Description

The temperature readout unit (TRU) is the ground based portion of the space-qualified solid-state temperature recorder system. The purpose of the TRU is to transfer data from the battery-powered temperature recorder into nonvolatile memory and to subsequently display the data in conventional units. Additionally, the TRU is capable of driving an X-Y recorder providing temperature vs. time plots, or of presenting the straight binary information to a digital computer for further analysis.

Data Storage

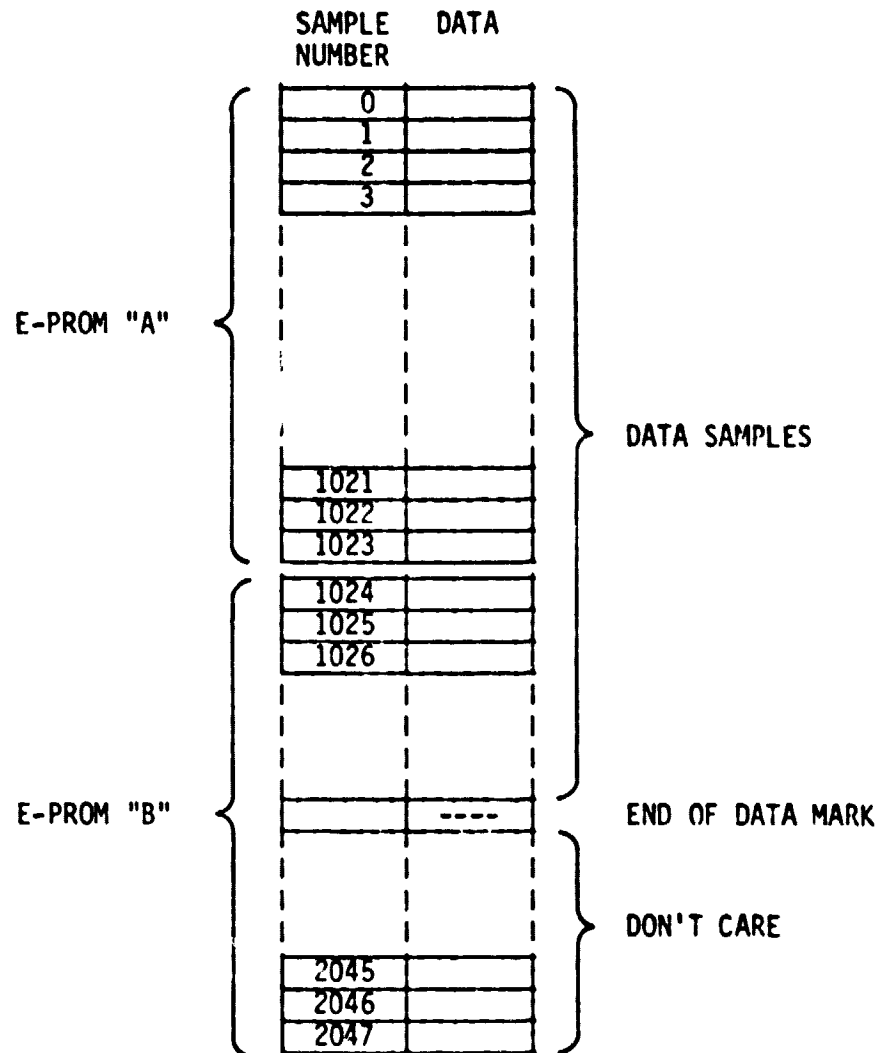
Temperature data which has been transferred from the temperature recorder to the TRU is stored in a pair of readily available 2708 erasable-programmable read only memories (E-PROMs).¹ These are located in the front panel zero insertion force sockets labeled "A" and "B."

Sketch (a) represents the organization of the E-PROM memory space after data has been transferred. Notice that E-PROM "A" contains samples zero through 1023 and E-PROM "B" contains samples 1024 through 2047. This distinction is transparent to the user; however, it can be of some advantage later in verifying that the E-PROMs are erased prior to data transfer.

Data end marker— Notice also in sketch (a) that the last data sample is followed by a "data end marker" consisting of four dashes. During the transfer process, the TRU automatically inserts the data end marker after the last data sample if the memory space is not entirely filled. This is needed to distinguish data from the random digits induced in the temperature recorder memory when it was first powered up. The TRU always looks ahead for the data end marker (or the end of memory space) and will not display anything past the last valid data point.

It is possible to override the data end marker with the data end marker override switch on the rear panel. This causes the TRU to treat everything as data and will stop only at the end of memory space. Normally the override feature is used only while verifying that the E-PROMs are erased, but it can also be used to look past the last apparent data point if the operator feels the data end marker is in error.

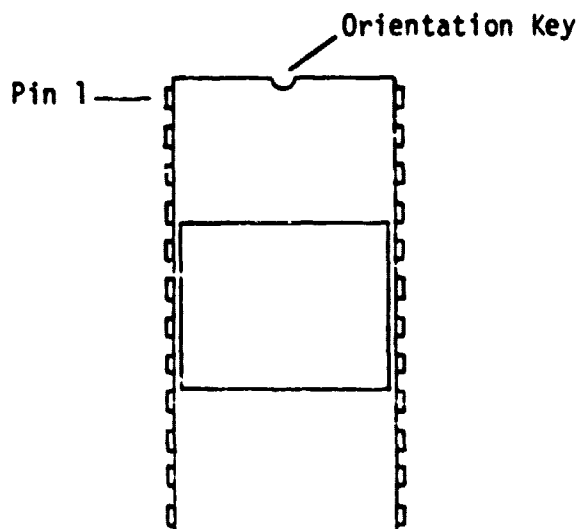
¹National Stock Number 5961-00-000-3056. Also available from Intel, National Semiconductor, Mostek and others.



Sketch (a).- Organization of data storage memory space.

Changing E-PROMs- The front panel zero-insertion force sockets make it very easy to exchange one set of E-PROMs with another. This may be done while the TRU is powered up; however, there are two general precautions which should be observed. First, the TRU should be reset to sample zero. Second, E-PROM "A" should be handled only while E-PROM "B" is locked in its socket. In other words, when removing the E-PROMs the correct sequence is "A" then "B," and while inserting E-PROMs the sequence should be "B" then "A."

Sketch (b) shows the relationship between Pin 1 and the orientation key on the E-PROM package. It is very important that the E-PROMs be aligned with Pin 1 in the top left corner (notched end up) as labeled on the TRU.

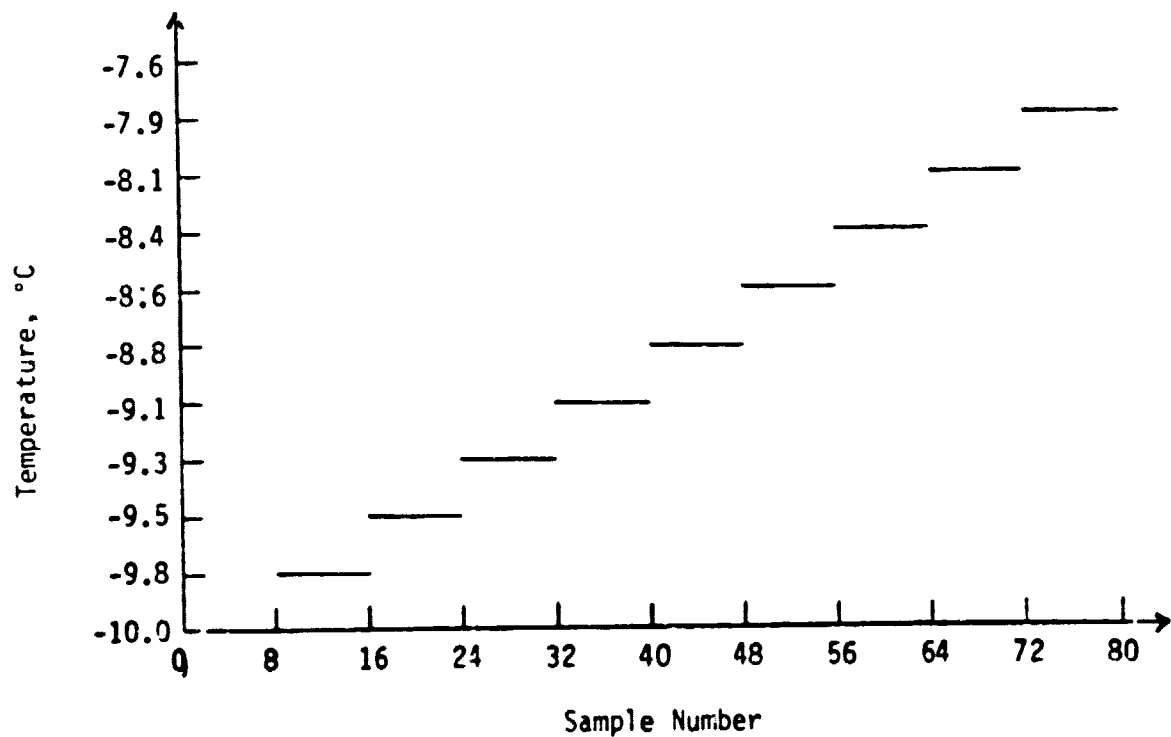
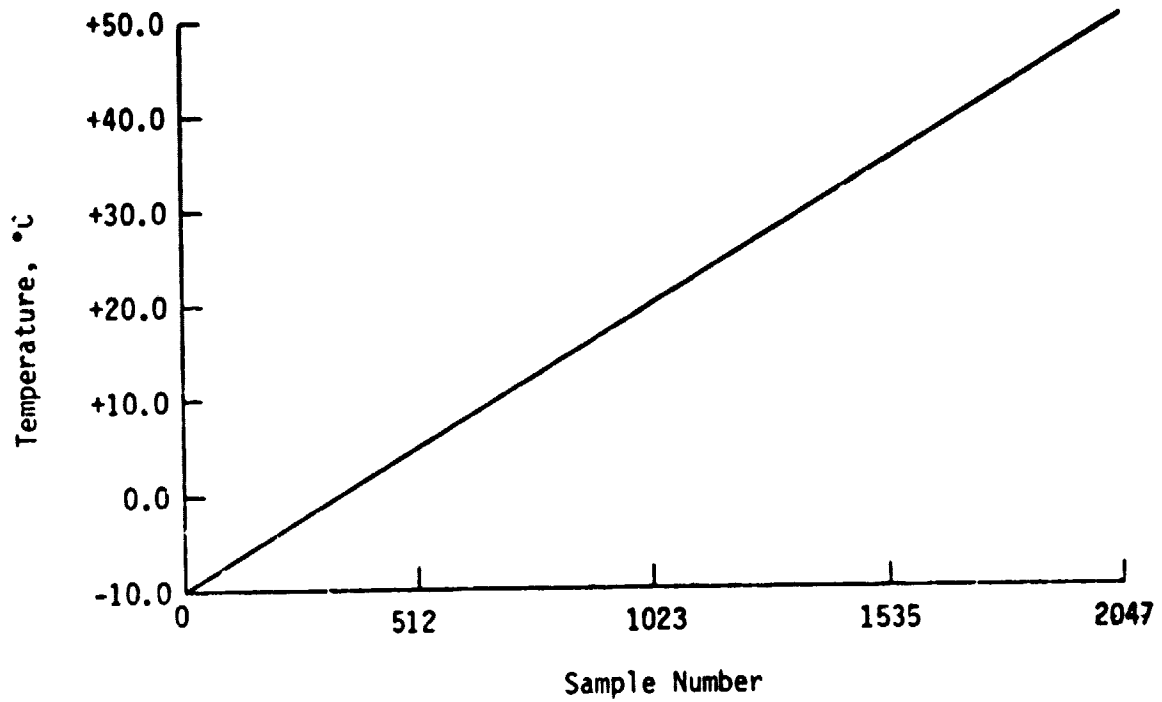


Sketch (b).- Location of E-PROM Pin 1 (top view).

Internal data ramp- Up until now the source of data has been the E-PROMs "A" and "B." However, there is an additional data bank, internal to the TRU, that can be selected via the rear panel OUTPUT MODE switch. This data bank contains a preprogrammed temperature ramp, starting with -10.0° at sample zero and increasing "linearly" with time as shown in sketch (c) (top). The ramp is actually composed of 256 steps, each containing eight samples, as shown in sketch (c) (bottom). The usefulness of this feature will become evident in the section which describes using an X-Y recorder to make temperature vs time graphs.

Data Recall

Stored temperature data may be viewed through the front panel numeric LED displays. These displays, one showing sample number and the other showing the recorded temperature in degrees Celsius, act as a "window" through which any data sample may be viewed. The controls for moving the window up and down through the data, as well as locating the highest and lowest recorded



Sketch (c).

temperatures, are located immediately below the displays. Their functions are as follows:

RESET returns the viewing window to sample zero.

SLOW, MED, and FAST cause the viewing window to move sequentially through the stored data. These are illuminated pushbutton switches which are active while being pressed. The fast recall speed is useful in moving the display window to an area of interest quickly, the medium speed is ideal for graphing, and the slow speed should be used for looking at individual data samples.

DOWN reverses the order in which the data is presented. This switch is illuminated while active.

PLOT can be pressed prior to selecting a recall speed to "lock in" the speed information instead of manually holding the speed button. This is especially useful while making temperature vs time plots or using the computer interface. The down button is still active, but must be selected prior to selecting a speed. Once the speed button has been pressed it will remain illuminated and active along with the plot button until the last valid data point has been displayed. At this point the process is over and both lights extinguish. In order to stop the process prematurely, the plot button may be pressed again.

MAX and MIN search through the data for the maximum and minimum temperature values, respectively. When a search mode is selected for the first time, the TRU resets and makes one complete pass through the data searching for the particular extreme value. This value is stored and the TRU resets and begins a second pass through the data, this time comparing each temperature value to the stored extreme value. When a match is detected the process stops and the sample number and temperature value are displayed. The entire process, from selecting the particular search mode until the first extreme value is displayed takes less than 1 sec. To display the next consecutive sample with that extreme value, simply press the same search button a second time. This may be done repetitively until the location of the first extreme value is displayed again. This indicates every location with that value has been displayed and the information will subsequently be repeated.

The MAX button may be used to locate the data end marker immediately since its binary value is greater than any data. The marker must be overridden before the TRU will treat it as data.

Data Transfer

Prior to data transfer it is wise to verify that the E-PROMs to be used are totally erased. This is accomplished by switching the data and marker switch from normal to override, pressing RESET, then MIN. If the display reads four dashes at sample zero, both E-PROMs are erased. If the display indicates something other than four dashes at sample zero, the E-PROM which contains the displayed location is not completely erased and should be replaced

with one that is. Remember that sample numbers zero through 1023 reside in E-PROM "A" and samples 1024 through 2047 reside in E-PROM "B."

After the E-PROMs are checked, their quartz windows should be covered to prevent light from entering during or after programming.

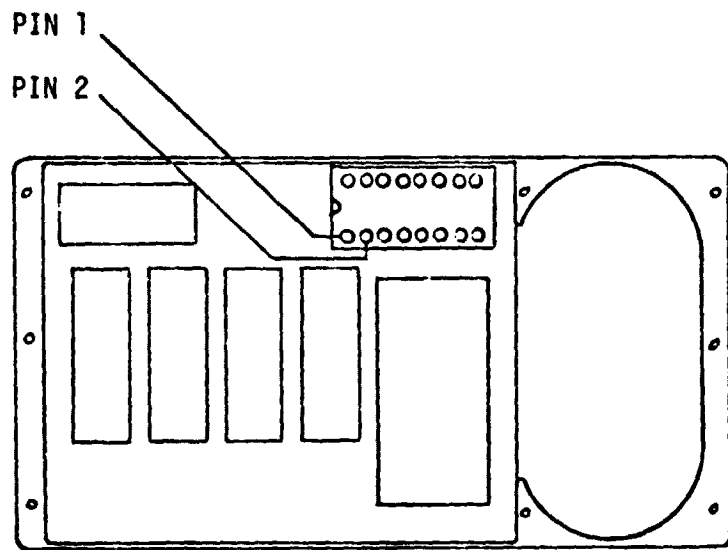
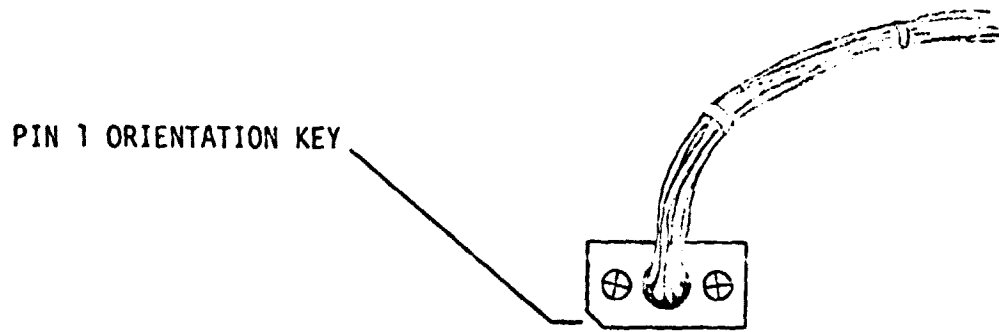
Next, the recorder interface connector should be attached to the TRU rear panel and both rear panel switches should be verified to be in their normal (LED off) positions. The final preparation of the TRU for data transfer is to press the RESET button.

The next step in the transfer procedure is the most critical. The recorder interface connector is to be inserted in the temperature recorder 16-pin IC socket. This must be done very carefully to avoid the possibility of electrically or physically damaging the components in the temperature recorder. Refer to sketch (d) which shows how to determine the proper orientation of the interface connector plug with respect to the temperature recorder. Start inserting the interface connector with the plug tilted towards pins 1 and 2 and then gradually straighten the connector as both rows of pins come into alignment. This procedure is advised for two reasons. First, by initially connecting only one pin at a time the operator's attention need only be focused on one area, thus limiting the chance of shorting a pin across two contacts. The second reason is that pin 2 is the ground pin and should be connected along with pin 1 before any of the other pins. This sequence of connecting pin 1 first, pin 2 second, and then the other 14 pins as they come, insures that the system will have a common ground before any other current return paths are set up.

To initiate the transfer process, press the COPY button. The COPY button should remain lighted and the numeric displays should be changing rapidly indicating the multicycle programming is taking place. This will last approximately 5 min after which the COPY light will go out and the interface plug may be removed from the temperature recorder. If the ERROR light comes on instead of the COPY light, then the interface connector should be removed and the E-PROMs reverified. The interface connector's junction with the TRU should also be checked. After this is done, the interface plug should again be inserted and the COPY button pressed. If the ERROR light still comes on, the temperature-recorder positive-battery voltage has dropped to below the minimum level required for operation of the circuit.

Data Outputs

Data may be output from the TRU in three different modes. The first mode is the already familiar front panel numeric display of sample number and corresponding temperature in degrees Celsius. The second is the rear panel analog output capable of driving an X-Y recorder providing temperature vs time graphs. The third output mode is a rear panel buffered binary output with a data valid flag for interfacing with a computer. All three output modes operate and are valid simultaneously.



Sketch (d).- Orientation of interface connector plug.

Temperature plots- A plot of recorded temperature over a period of time is perhaps the most convenient and meaningful form of output available. Any X-Y recorder with gain and offset controls can be used to generate a plot of the entire sampling sequence and temperature range. Additionally, any portion of the data may be plotted on an expanded scale to show more detail.

In order to adjust the X-Y recorder controls, the maximum and minimum values in the desired displayed range of each axis must be readily accessible. This is accomplished by the internal data ramp in which every possible data value and sample number is represented in an orderly, increasing fashion. In order to look at only one axis at a time for adjustment purposes, simply disconnect the cable feeding the other axis.

The adjustment of the offset and gain controls is an iterative process. First, step through the internal data ramp until the lower bound of that axis is displayed, then adjust the *offset* control to place the recording pen at the desired location. Next, step through the internal data ramp until the upper bound of that axis is displayed, this time adjusting the *gain* control to move the pen. Repeat this process until both axes are adjusted to satisfaction.

To make a plot, switch back to the true data mode and locate the first sample to be plotted. Check that the input cables to both axes are connected, lower the pen, and press PLOT then MED. The data will be plotted from the selected starting location to the last valid data point, where the TRU stops automatically. If only a portion of the data is desired, the plot may be terminated prior to the end of data by pressing the PLOT button a second time. After the plot is made be sure to raise the recorder pen immediately to avoid accidentally marking the paper.

Computer interface- The computer interface is designed to rapidly present each data point to a digital computer via the BINARY OUTPUT connector on the rear panel. As this output is powered at all times the TRU should be reset before the interface cable is attached. To initiate the process, press PLOT, then FAST. Each sample and its corresponding sample number will be presented, starting with sample zero and ending with the last sample before the end of data mark. The pin designations for this connector are shown in table A1.

Specifications

The accuracy of the solid-state temperature recorder system is $\pm 1^{\circ}\text{C}$. The major limitations on the accuracy arise from two sources. First is the inherent inaccuracy caused by recording an analog parameter as an 8-bit digital code. Second is the inaccuracy introduced by the analog front end of the temperature recorder.

The binary output of the TRU is a direct reproduction of data as recorded by the temperature recorder. There is no additional error due to the TRU in this case. The visual display has a resolution of 0.1°C and therefore can

cause an additional rounding error in the displayed data of $\pm 0.05^{\circ}\text{C}$. The analog outputs themselves add an inaccuracy of $\pm 0.12^{\circ}\text{C}$.

The TRU requires a line voltage of 105 to 120 VAC at 60 to 440 Hz.

Table A1.- BINARY OUTPUT connector.

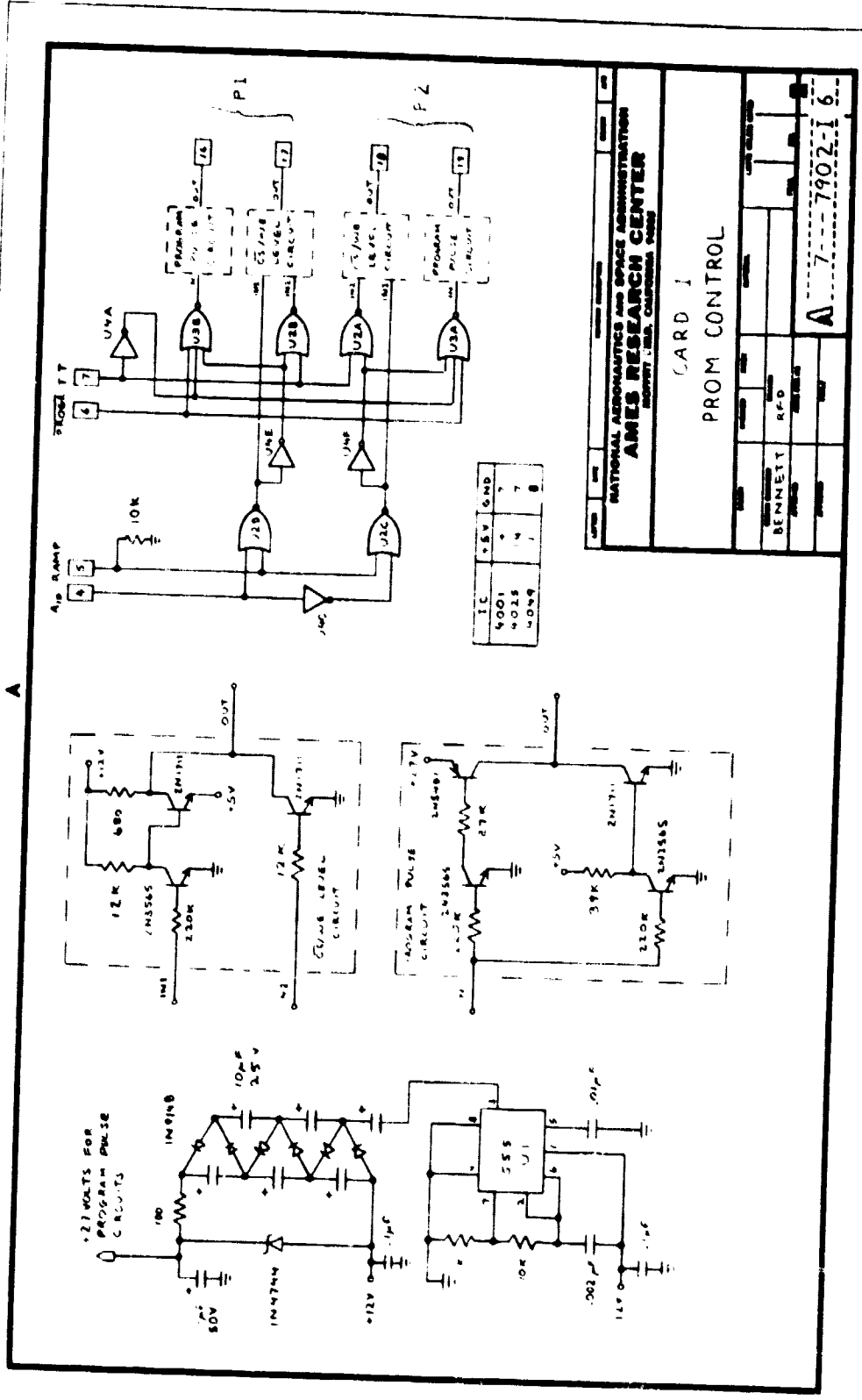
Pin number	Symbol	Function
1	A ₀	(LSB)
2	A ₁	
3	A ₂	
4	A ₃	
5	A ₄	
6	A ₅	address
7	A ₆	
8	A ₇	
9	A ₈	
10	A ₉	
11	A ₁₀	(MSB)
12	D ₀	(LSB)
13	D ₁	
14	D ₂	
15	D ₃	data
16	D ₄	
17	D ₅	
18	D ₆	
19	D ₇	(MSB)
20	DVF	data valid flag
21	NC	
22		no connection
23		
24		
25	GND	ground

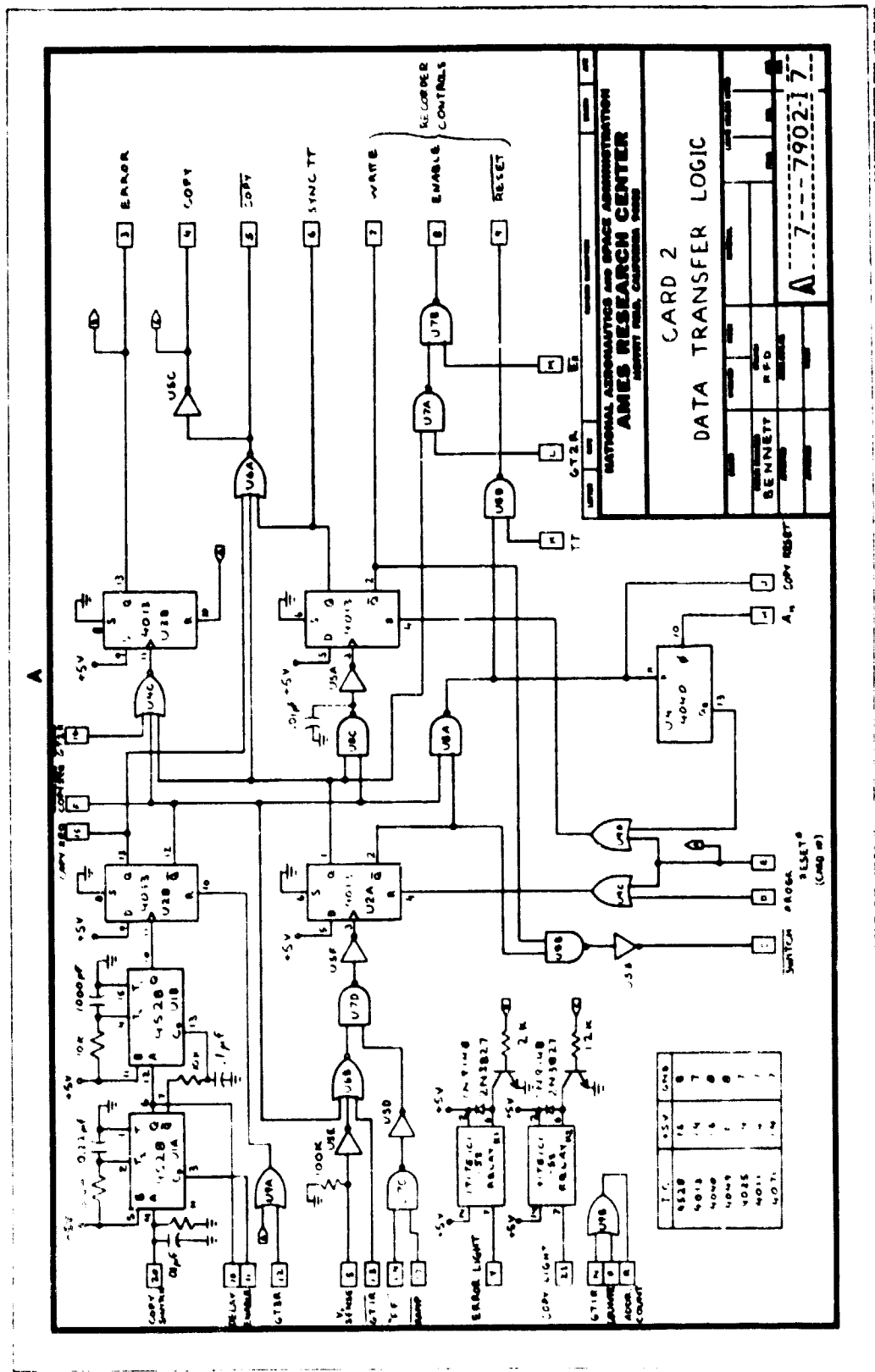
APPENDIX B

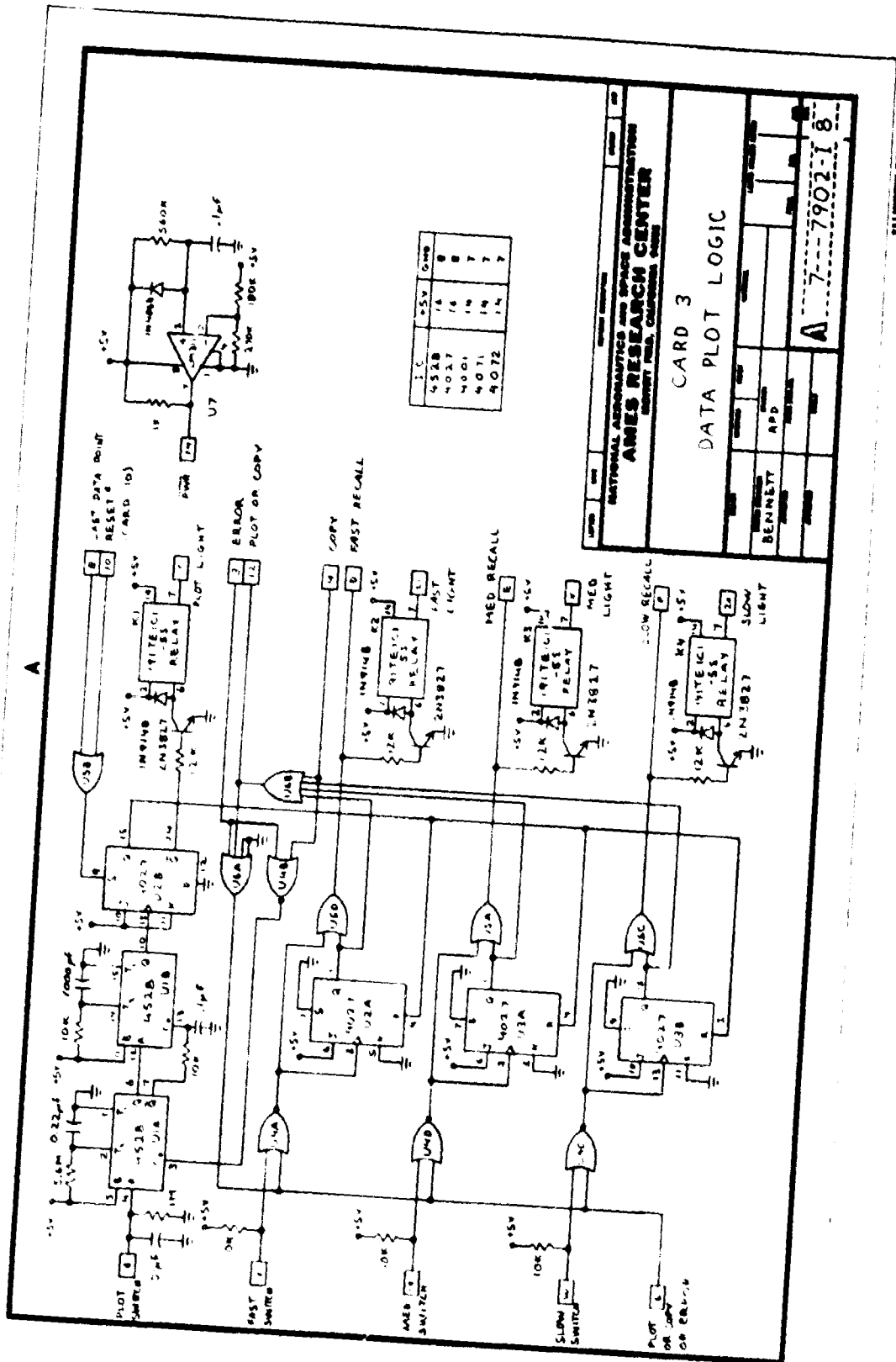
CIRCUIT DIAGRAM TEMPERATURE READOUT UNIT

Card

1	PROM control
2	Data transfer logic
3	Data plot logic
4	Data search logic
5	Data recall logic
6	System timing
7	Address counter and latch
8	Controls interface
9	Data interface
10	Data comparator and latch
11, 13	Look up tables
12, 14	Analog and binary outputs

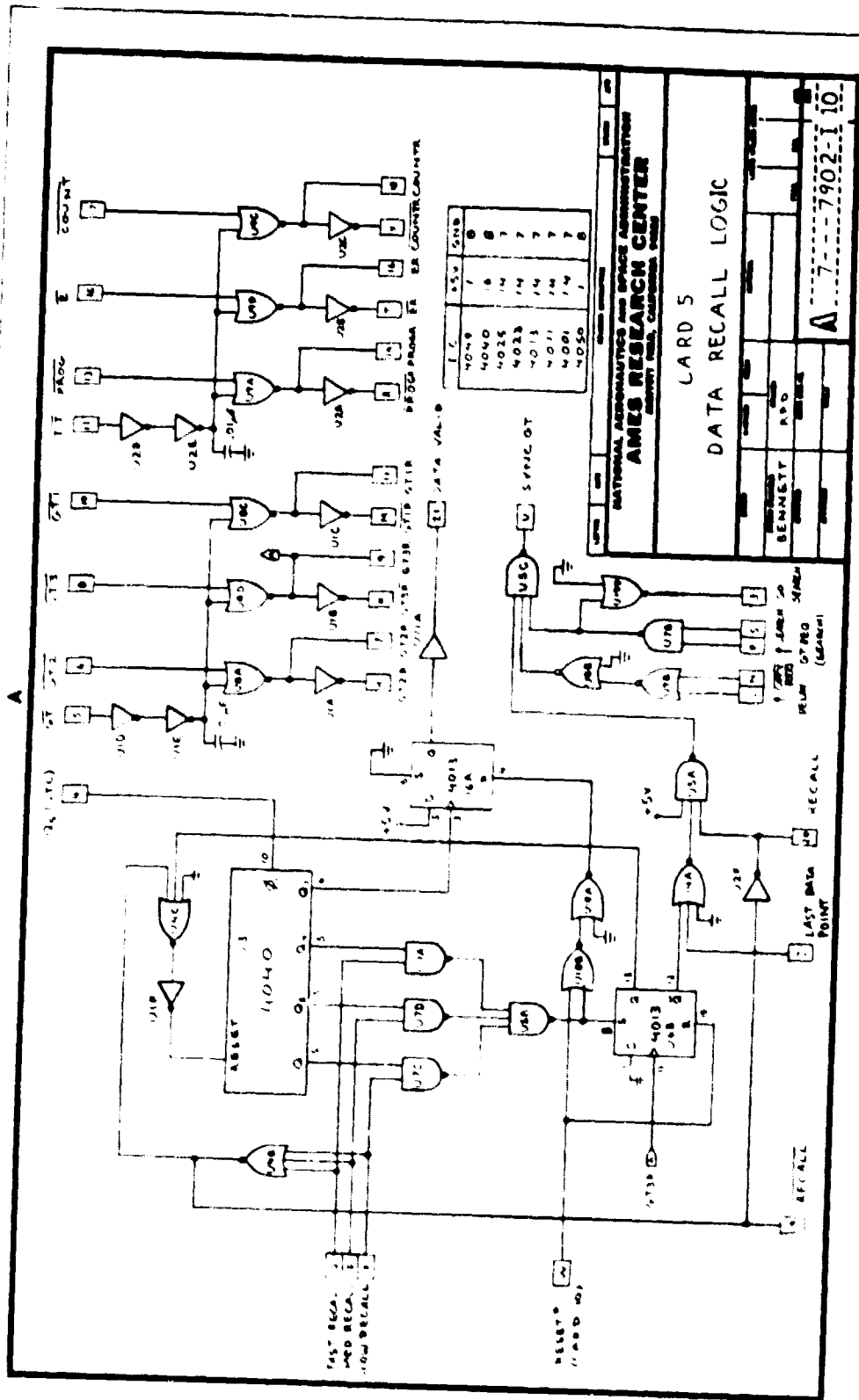


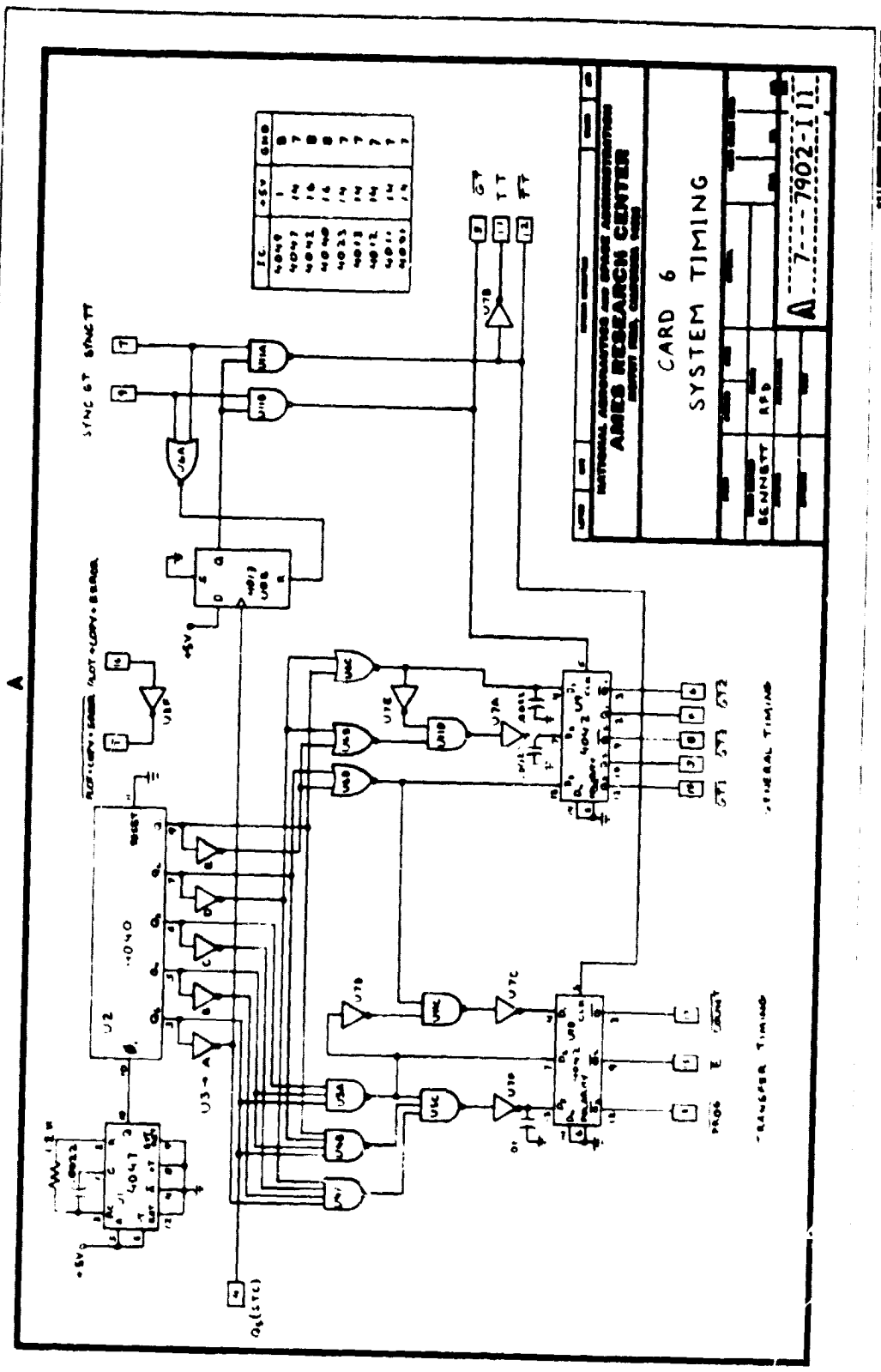




IC	5V	Other
4528	7A	B
4027	7A	B
4001	7A	B
4071	7A	B
4072	7A	B

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MOSBY ROAD, CALIFORNIA	
CARD 3	
DATA PLOT LOGIC	
BENNETT	APD
A 7-7902-18	





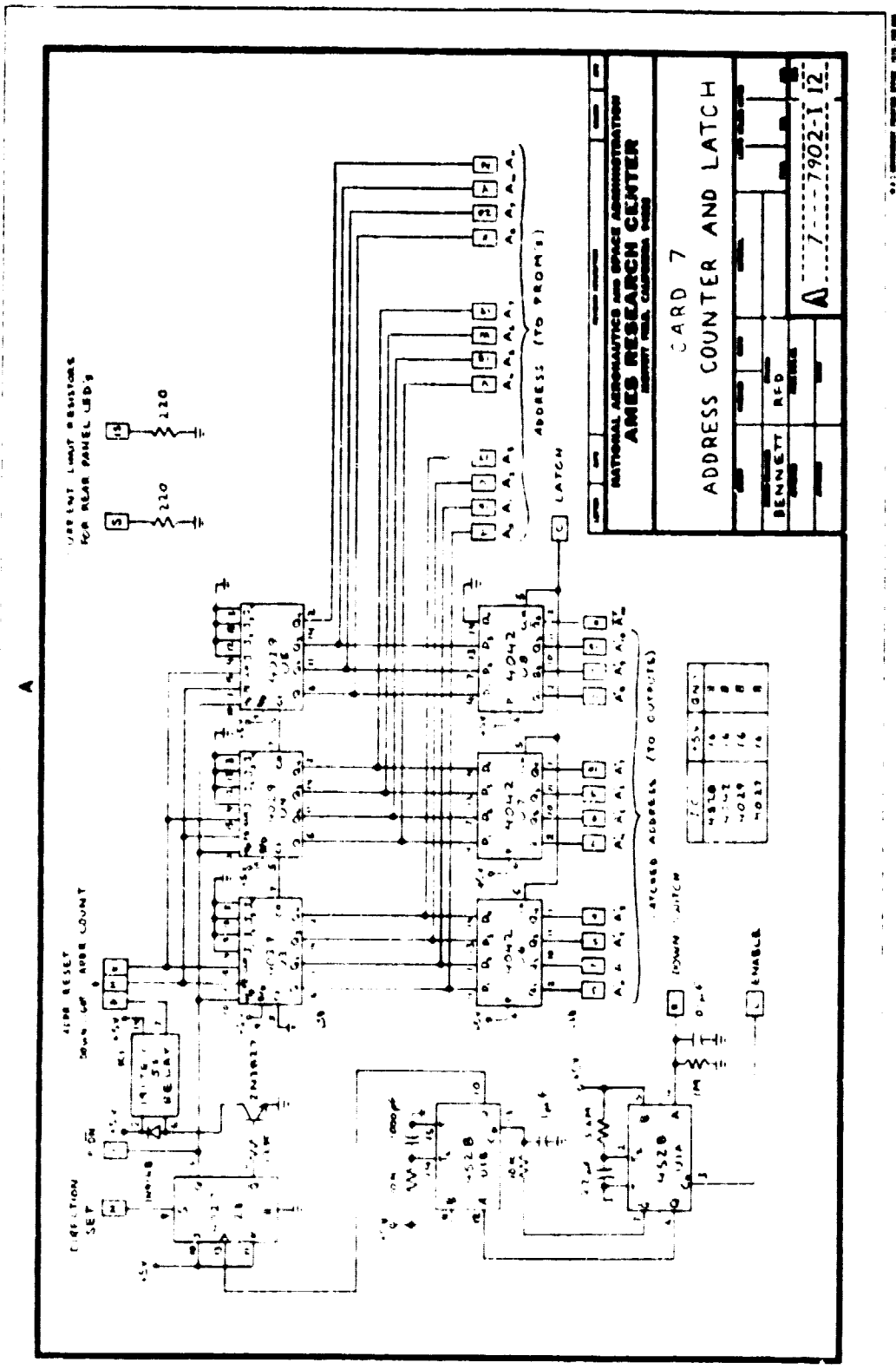
IC	Q54	Q55
4049	1	8
4047	14	7
4042	16	8
4048	16	8
4033	14	7
4013	14	7
4011	14	7
4001	14	7

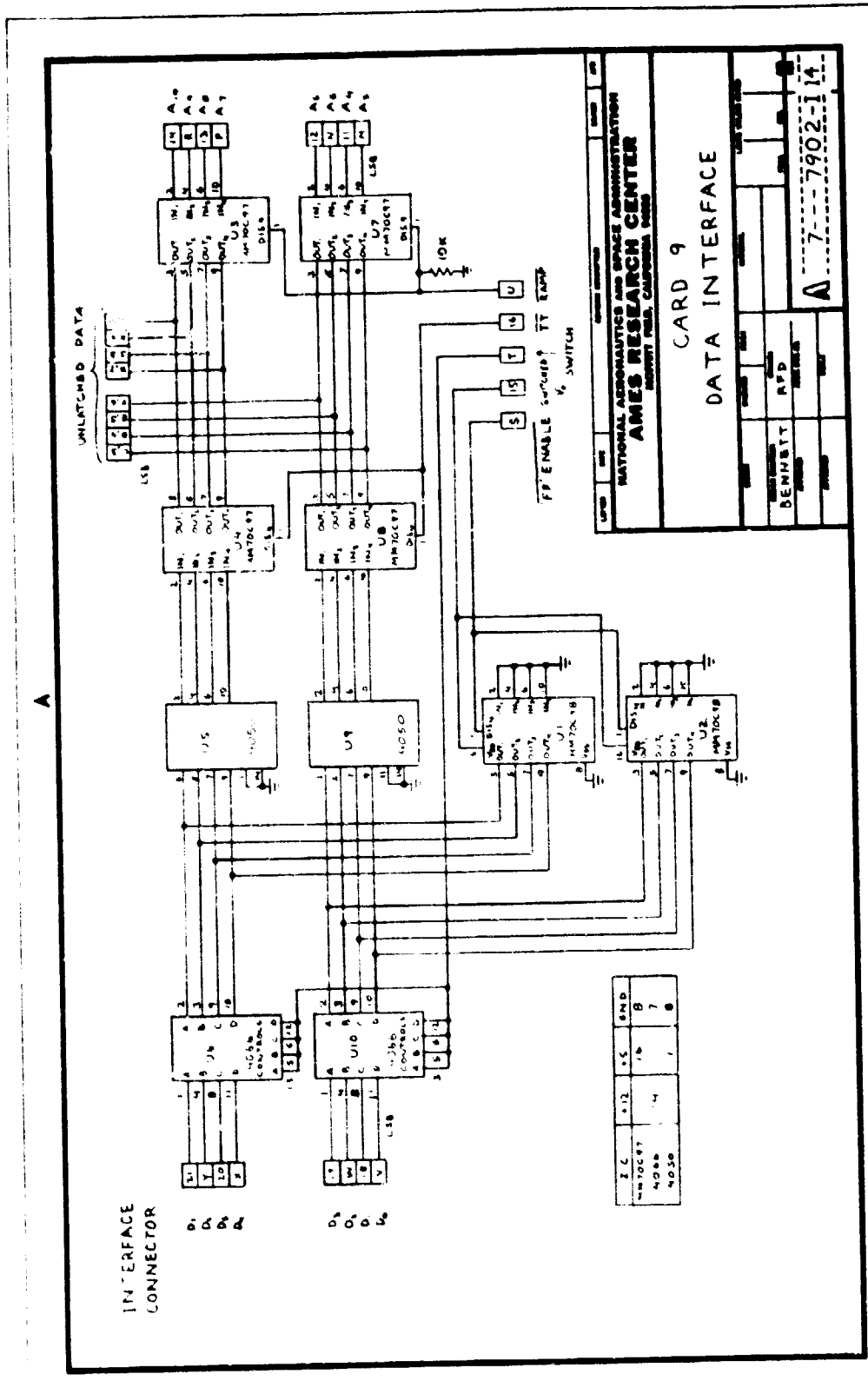
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AMES RESEARCH CENTER
 AMES-79-111

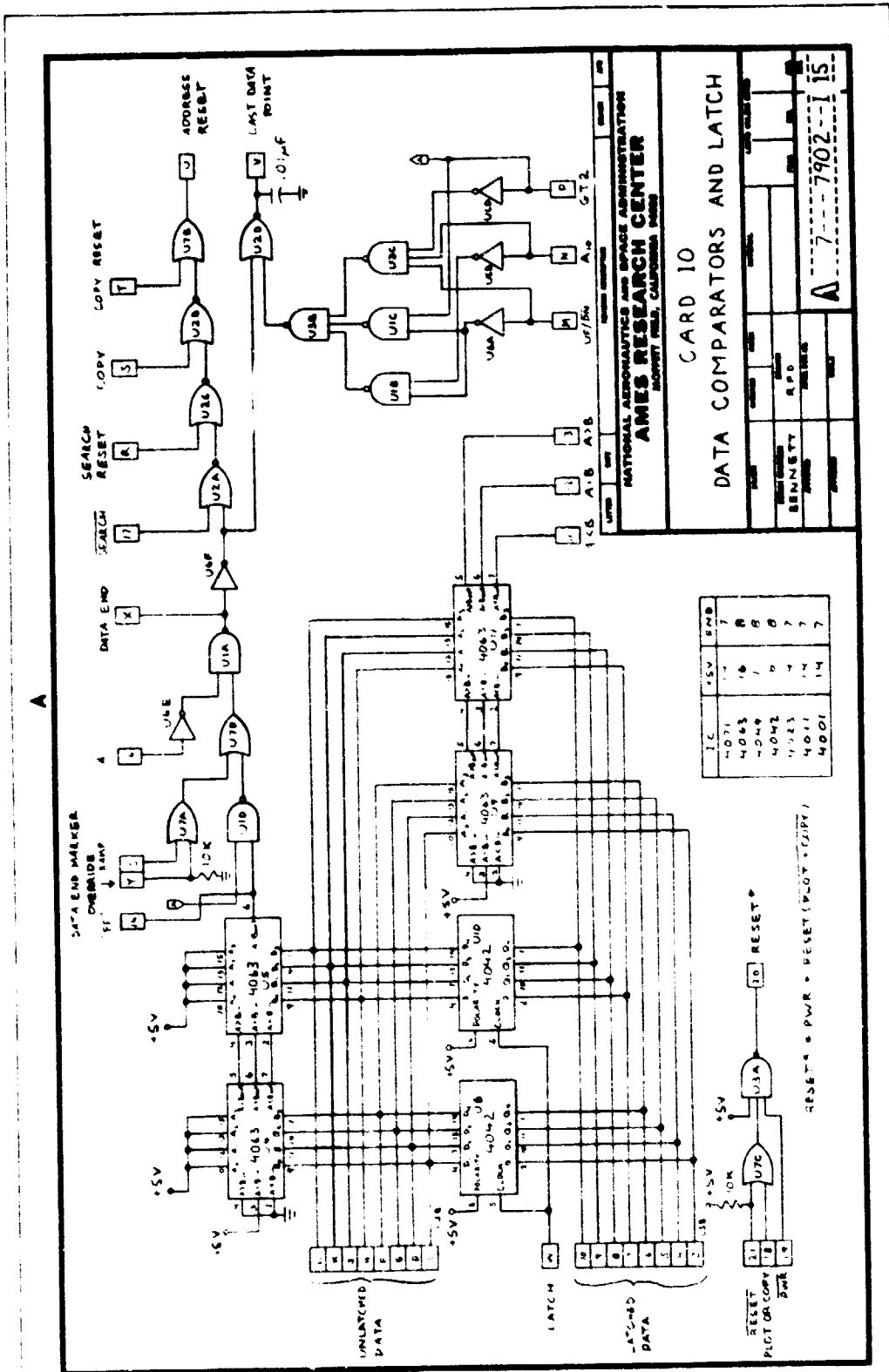
CARD 6
SYSTEM TIMING

DESIGNED BY	DATE
CHECKED BY	DATE
APPROVED BY	DATE
REVISIONS	
1	
2	
3	
4	
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100	

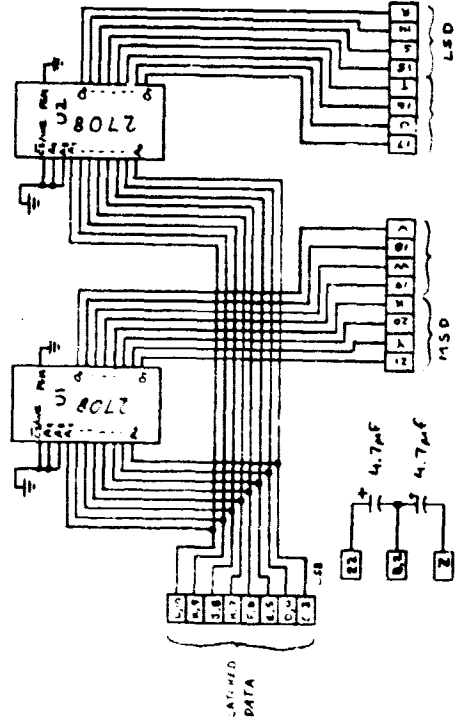
A 7-7902-111







CARD 11



8CD DATA OUT

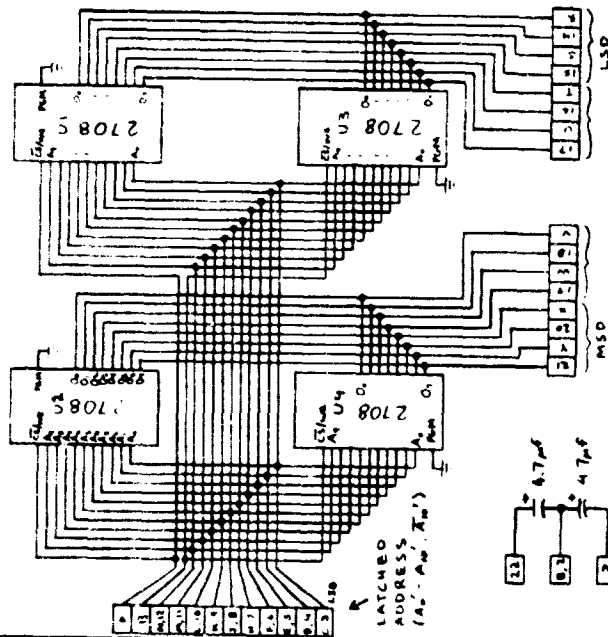
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CARDS 11 AND 13
LOOK-UP TABLES

BENNETT RPD

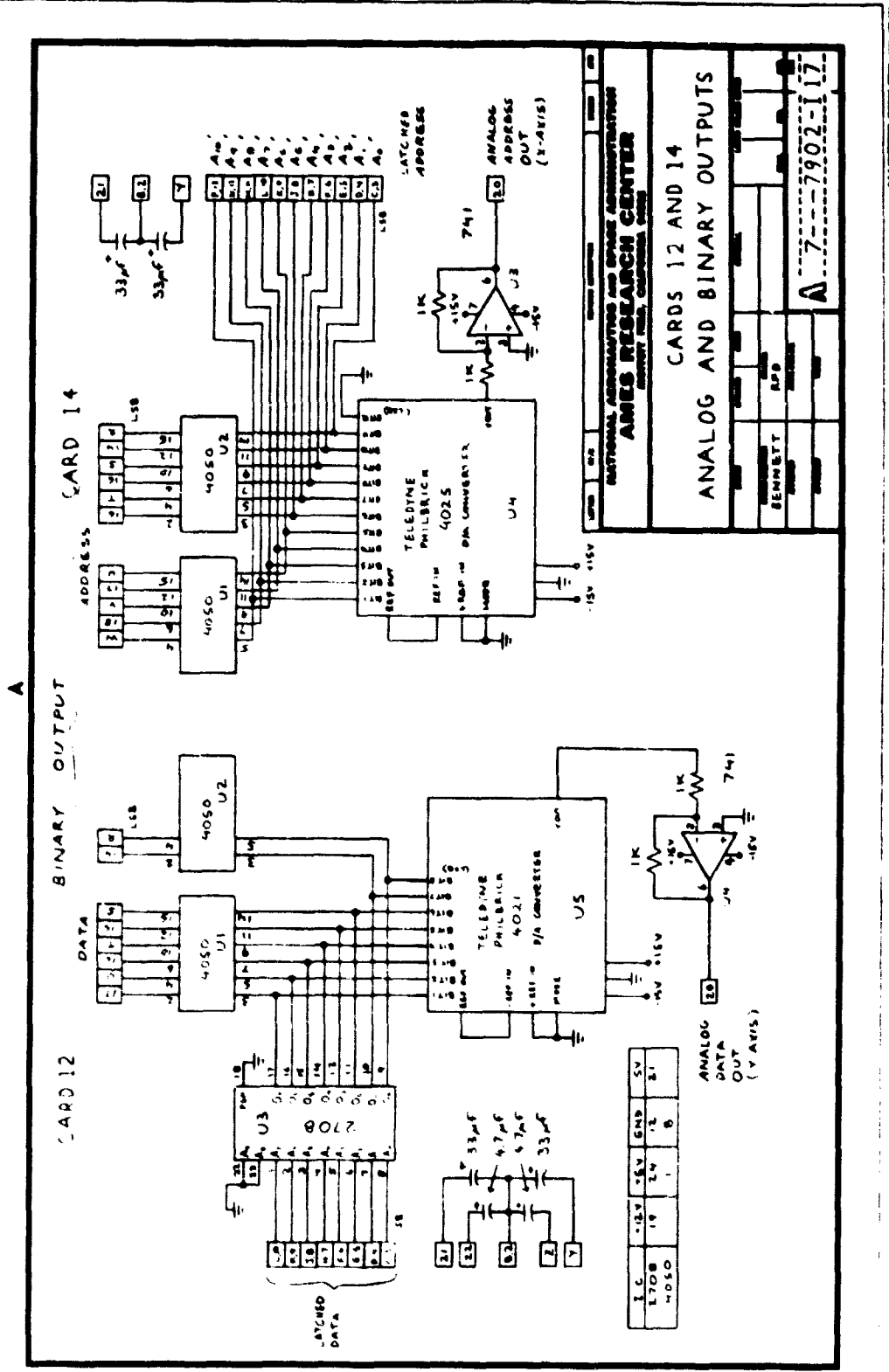
A 7-7902-1 16

CARD 13



8CD ADDRESS OUT

1 C	+12V	+5V	GND	-5V
2708	19	24	13	31



APPENDIX C

WIRING LIST TEMPERATURE READOUT UNIT

Card 1

From	To	To	To	To	Comments
1:A,1	+5V				
1:B,2	GND				
1:20	-12V				
1:22	+12V				
1:4	7:Y	10:N	9:14		
1:5	10:15	S12:3	I3:A		OUTPUT MODE SWITCH, LED
1:6	5:R				
1:7	6:11	2:K			
1:16	P1:18				
1:17	P1:20				
1:18	P2:20				
1:19	P2:18				

From	To	To	To	To	Comments
2:A,1	+5V				
2:B,2	GND				
2:3	3:3				
2:4	3:4	8:4	4:4	10:S	
2:5	8:5				
2:6	6:7	8:6			
2:7	8:7				
2:8	8:8				
2:9	8:9				
2:10	5:L				
2:11	6:T	4:T	7:L		
2:12	5:9	4:M			
2:13	5:M				
2:14	10:14				
2:15	8:11				
2:16	5:H				
2:17	9:U	S12:1			OUTPUT MODE SWITCH
2:C	8:12				
2:D	5:14				
2:E	10:20	3:10	4:20	5:W	
2:F	5:N				
2:H	7:N	10:16			
2:J	10:T				
2:K	6:11	1:7			
2:L	5:7	4:8			
2:M	5:T				
2:N	5:11	4:L			
2:P	5:18				
2:R	7:K				
2:S	8:15				
2:20	S2:C				TRANSFER SWITCH
2:21	S2:A+				TRANSFER LIGHT
2:Y	I1:A+				ERROR LIGHT

From	To	To	To	To	Comments
3:A,1	+5V				
3:B,2	GND				
2:3	2:3				
3:4	2:4	8:4	4:4	10:S	
3:D	5:D				
3:E	5:E				
3:F	5:F				
3:8	10:V	5:J			
3:10	10:20	4:20	2:E	5:W	
3:12	10:18				
3:14	10:19				
3:16	6:16				
3:18	S5:C				PLOT SWITCH
3:19	S9:C				MEDIUM SWITCH
3:20	S8:A+				SLOW LIGHT
3:21	S10:A+				FAST LIGHT
3:V	S10:C				FAST SWITCH
3:W	S8:C				SLOW SWITCH
3:X	S9:A+				MEDIUM LIGHT
3:Y	S5:A+				PLOT LIGHT

From	To	To	To	To	Comments
4:A,1	+5V				
4:B,2	GND				
4:3	5:S				
4:4	2:4	3:4	8:4	10:S	
4:5	5:20				
4:8	2:L	5:7			
4:9	6:J				
4:10	5:19				
4:11	10:11				
4:12	10:12				
4:13	10:13				
4:17	10:17				
4:20	2:E	3:10	10:20	5:W	
4:21	S3:C				MAXIMUM SWITCH
4:C	7:C	10:W			
4:D	10:X				
4:L	2:N	5:11			
4:M	2:12	5:9			
4:N	5:P				
4:P	7:M				
4:R	10:R				
4:T	2:11	6:T	7:L		
4:Y	S7:C				MINIMUM SWITCH
4:K	5:3				
4:7	5:K				

From	To	To	To	To	Comments
5:A,1	+5V				
5:B,2	GND				
5:4	6:4				
5:5	6:5				
5:6	6:6				
5:8	6:8				
5:10	6:10				
5:12	6:12	9:16			
5:13	6:13				
5:15	6:15				
5:17	6:17				
5:D	3:D				
5:E	3:E				
5:F	3:F				
5:H	2:16				
5:7	2:L	4:8			
5:K	4:7				
5:9	2:12	4:M			
5:M	2:13				
5:11	2:N	4:L			
5:R	1:6				
5:14	2:D				
5:T	2:M				
5:16	---				
5:V	8:10				
5:18	2:P				
5:J	3:8	10:V			
5:L	2:10				
5:N	2:F				
5:P	4:N				
5:S	4:3				
5:U	6:9				
5:19	4:10				
5:20	4:5				
5:21	C1:20				
5:3	4:K				
5:W	2:E	3:10	4:20	10:20	

From	To	To	To	To	Comments
6:A,1	+5V				
6:B,2	GND				
6:5	5:5				
6:7	2:6	8:6			
6:9	5:U				
6:11	1:7	2:K			
6:12	9:16	5:12			
6:6	5:6				
6:8	5:8				
6:10	5:10				
6:13	5:13				
6:15	5:15				
6:17	5:17				
6:16	3:16				
6:T	2:11	4:T	7:L		
6:4	5:4				
6:F	10:P				
6:J	4:9				

From	To	To	To	To	Comments
7:A,1	+5V				
7:B,2	GND				
7:3	14:C,3	13:C,3			
7:4	14:D,4	13:D,4			
7:5	14:E,5	13:E,5			
7:6	14:F,6	13:F,6			
7:7	14:H,7	13:H,7			
7:8	14:J,8	13:J,8			
7:9	14:K,9	13:K,9			
7:10	14:L,10	13:L,10			
7:11	14:M,11	13:M,11			
7:12	14:N,12	13:N,12			
7:13	14:P,13	13:13			
7:D	13:P				
7:C	10:W	4:C			
7:H	10:U				
7:K	7:R				
7:L	6:T	2:11	4:T		
7:M	4:P				
7:S	13:C				
7:15	12:C				
7:P	S4:A+				DOWN LIGHT
7:R	S4:C				DOWN SWITCH
7:J	10:M				
7:T	P1:8	P2:8			
7:16	P1:7	P2:7			
7:U	P1:6	P2:6			
7:17	P1:5	P2:5	9:M		
7:V	P1:4	P2:4	9:11		
7:18	P1:3	P2:3	9:N		
7:W	P1:2	P2:2	9:12		
7:19	P1:1	P2:1	9:P		
7:X	P1:23	P2:23	9:13		
7:20	P1:22	P2:22	9:R		
7:Y	1:4	10:N	9:14		
7:N	2:H	10:16			

From	To	To	To	To	Comments
8:A,1	+5V				
8:B,2	GND				
8:22	+12V				
8:7	2:7				
8:8	2:8				
8:9	2:9				
8:10	5:V				
8:11	2:15				
8:12	2:C				
8:15	2:S				
8:4	2:4	3:4	4:4	10:S	
8:S	9:S				
8:R	9:15				
8:T	9:T				
8:V	C2:13				
8:18	C2:16				
8:W	C2:11				
8:19	C2:3				
8:X	C2:15				
8:20	C2:14				
8:Y	C2:1				
8:21	C2:2				
8:5	2:5				
8:6	2:6	6:7			

From	To	To	To	To	Comments
9:A,1	+5V				
9:B,2	GND				
9:C,3	10:C	P1:9	P2:9		
9:D,4	10:D	P1:10	P2:10		
9:E,5	10:E	P1:11	P2:11		
9:F,6	10:F	P1:13	P2:13		
9:H,7	10:H	P1:14	P2:14		
9:J,8	10:J	P1:15	P2:15		
9:K,9	10:K	P1:16	P2:16		
9:L,10	10:L	P1:17	P2:17		
9:M	7:17	P1:5	P2:5		
9:11	7:V	P1:4	P2:4		
9:N	7:18	P1:3	P2:3		
9:12	7:W	P1:2	P2:2		
9:P	7:19	P1:1	P2:1		
9:13	7:X	P1:23	P2:23		
9:R	7:20	P1:22	P2:22		
9:14	7:Y	1:4	10:N		
9:S	8:S				
9:15	8:R				
9:T	8:T				
9:16	6:12	5:12			
9:U	2:17	S12:1			OUTPUT MODE SWITCH
9:V	C2:9				
9:18	C2:8				
9:W	C2:7				
9:19	C2:6				
9:X	C2:10				
9:20	C2:5				
9:Y	C2:12				
9:21	C2:4				

From	To	To	To	To	Comments
10:A,1	+5V				
10:B,2	GND				
10:3	11:C,3	12:C,3			
10:4	11:D,4	12:D,4			
10:5	11:E,5	12:E,5			
10:6	11:F,6	12:F,6			
10:7	11:H,7	12:H,7			
10:8	11:J,8	12:J,8			
10:9	11:K,9	12:K,9			
10:10	11:L,10	12:L,10			
10:C	9:C,3	P1:9	P2:9		
10:D	9:D,4	P1:10	P2:10		
10:E	9:E,5	P1:11	P2:11		
10:F	9:F,6	P1:13	P2:13		
10:H	9:H,7	P1:14	P2:14		
10:J	9:J,8	P1:15	P2:15		
10:K	9:K,9	P1:16	P2:16		
10:L	9:L,10	P1:17	P2:17		
10:11	4:11				
10:12	4:12				
10:13	4:13				
10:M	7:J				
10:N	1:4	7:Y	9:14		
10:P	6:F				
10:14	2:14				
10:15	1:5	S12:3	13:A		OUTPUT MODE SWITCH, LED
10:16	7:N	2:H			
10:17	4:17				
10:R	4:R				
10:S	2:4	3:4	4:4	8:4	
10:T	2:J				
10:U	7:H				
10:V	5:J	3:8			
10:18	3:12				
10:19	3:14				
10:20	4:20	3:10	2:E	5:W	
10:21	S6:C				
10:W	7:C	4:C			
10:Y	S11:3	12:A			DATA END MARKER SWITCH, LED
10:X	4:D				

From	To	To	To	To	Comments
11:A,1	+5V				
11:B,2	GND				
11:22	+12V				
11:Z	-5V				
11:C,3	12:C,3	10:3			
11:D,4	12:D,4	10:4			
11:E,5	12:E,5	10:5			
11:F,6	12:F,6	10:6			
11:H,7	12:H,7	10:7			
11:J,8	12:J,8	10:8			
11:K,9	12:K,9	10:9			
11:L,10	12:L,10	10:10			
11:R	LD0:8				
11:14	LD0:1				
11:S	LD0:2				
11:15	LD0:3				
11:T	LD1:8				
11:16	LD1:1				
11:U	LD1:2				
11:17	LD1:3				
11:V	LD2:8				
11:18	LD2:1				
11:W	LD2:2				
11:19	LD2:3				
11:X	LD3:8				
11:20	LD3:1				
11:Y	LD3:2				
11:21	LD3:3				

From	To	To	To	To	Comments
12:A,1	+5V				
12:B,2	GND				
12:Y	-15V				
12:21	+15V				
12:22	+12V				
12:Z	-5V				
12:C,3	11:C,3	10:3			
12:D,4	11:D,4	10:4			
12:E,5	11:E,5	10:5			
12:F,6	11:F,6	10:6			
12:H,7	11:H,7	10:7			
12:J,8	11:J,8	10:8			
12:K,9	11:K,9	10:9			
12:L,10	11:L,10	10:10			
12:R	C1:12				BINARY OUTPUTS - DATA (LSB)
12:14	C1:13				
12:S	C1:14				
12:15	C1:15				
12:T	C1:16				
12:16	C1:17				
12:U	C1:18				
12:17	C1:19				
12:20	B:2				Y-AXIS ANALOG OUTPUT

From	To	To	To	To	Comments
13:A,1	+5V				
13:B,2	GND				
13:22	+12V				
13:Z	-5V				
13:C,3	14:C,3	7:3			
13:D,4	14:D,4	7:4			
13:E,5	14:E,5	7:5			
13:F,6	14:F,6	7:6			
13:H,7	14:H,7	7:7			
13:J,8	14:J,8	7:8			
13:K,9	14:K,9	7:9			
13:L,10	14:L,10	7:10			
13:M,11	14:M,11	7:11			
13:N,12	14:N,12	7:12			
13:13	14:P,13	7:13			
13:P	7:D				
13:R	LA0:8				
13:14	LA0:1				
13:S	LA0:2				
13:15	LA0:3				
13:T	LA1:8				
13:16	LA1:1				
13:U	LA1:2				
13:17	LA1:3				
13:V	LA2:8				
13:18	LA2:1				
13:W	LA2:2				
13:19	LA2:3				
13:X	LA3:8				
13:20	LA3:1				
13:Y	LA3:2				
13:21	LA3:3				

From	To	To	To	To	Comments
14:A,1	+5V				
14:B,2	GND				
14:Y	-15V				
14:21	+15V				
14:C,3	13:C,3	7:3			
14:D,4	13:D,4	7:4			
14:E,5	13:E,5	7:5			
14:F,6	13:F,6	7:6			
14:H,7	13:H,7	7:7			
14:J,8	13:J,8	7:8			
14:K,9	13:K,9	7:9			
14:L,10	13:L,10	7:10			
14:M,11	13:M,11	7:11			
14:N,12	13:N,12	7:12			
14:P,13	13:13	7:13			
14:R	C1:1				BINARY OUTPUTS - ADDRESS (LSB)
14:14	C1:2				
14:S	C1:3				
14:15	C1:4				
14:T	C1:5				
14:16	C1:6				
14:U	C1:7				
14:17	C1:8				
14:V	C1:9				
14:18	C1:10				
14:W	C1:11				
14:20	B:1				X-AXIS ANALOG OUTPUT

Front panel switches

From	To	To	To	To	Comments
S2:NO	+5V				TRANSFER SWITCH
S2:C	2:20				
S2:A+	2:21				
S2:A	GND				
S3:NO	+5V				MAXIMUM SWITCH
S3:C	4:21				
S3:A+	---				
S3:A	---				
S4:NO	+5V				DOWN SWITCH
S4:C	7:R				
S4:A+	7:P				
S4:A	GND				
S5:NO	+5V				PLOT SWITCH
S5:C	3:18				
S5:A+	3:Y				
S5:A	GND				
S6:NO	GND				RESET SWITCH
S6:C	10:21				
S6:A+	---				
S6:A	---				
S7:NO	+5V				MINIMUM SWITCH
S7:C	4:Y				
S7:A+	---				
S7:A	---				
S8:NO	GND				SLOW SWITCH
S8:C	3:W				
S8:A+	3:20				
S8:A	GND				
S9:NO	GND				MEDIUM SWITCH
S9:C	3:19				
S9:A+	3:X				
S9:A	GND				
S10:NO	GND				FAST SWITCH
S10:C	3:V				
S10:A+	3:21				
S10:A	GND				
11:A+	2:Y				ERROR LIGHT
11:A	GND				

Front panel LED displays

From	To	To	To	To	Comments
LA:7	+5V	} All			ADDRESS LED DISPLAY
LA:6	GND				
LA:5	GND				
LA0:8	13:R				
LA0:1	13:14				
LA0:2	13:S				
LA0:3	13:15				
LA0:4	+5V				
LA1:8	13:T				
LA1:1	13:16				
LA1:2	13:U				
LA1:3	13:17				
LA1:4	+5V				
LA2:8	13:V				
LA2:1	13:18				
LA2:2	13:W				
LA2:3	13:19				
LA2:4	+5V				
LA3:8	13:X				
LA3:1	13:20				
LA3:2	13:Y				
LA3:3	13:21				
LA3:4	+5V				
LD:7	+5V	} All			DATA LED DISPLAY
LD:6	GND				
LD:5	GND				
LD0:8	11:R				
LD0:1	11:14				
LD0:2	11:S				
LD0:3	11:15				
LD0:4	+5V				
LD1:8	11:T				
LD1:1	11:16				
LD1:2	11:U				
LD1:3	11:17				
LD1:4	GND				
LD2:8	11:V				
LD2:1	11:18				
LD2:2	11:W				
LD2:3	11:19				
LD2:4	+5V				
LD3:8	11:X				
LD3:1	11:20				
LD3:2	11:Y				
LD3:3	11:21				
LD3:4	+5V				

PROM socket A

From	To	To	To	To	Comments
P1:1	P2:1	7:19	9:P		
P1:2	P2:2	7:W	9:12		
P1:3	P2:3	7:18	9:N		
P1:4	P2:4	7:V	9:11		
P1:5	P2:5	7:17	9:M		
P1:6	P2:6	7:U			
P1:7	P2:7	7:16			
P1:8	P2:8	7:T			
P1:9	P2:9	10:C	9:C,3		
P1:10	P2:10	10:D	9:D,4		
P1:11	P2:11	10:E	9:E,5		
P1:12	GND				
P1:13	P2:13	10:F	9:F,6		
P1:14	P2:14	10:H	9:H,7		
P1:15	P2:15	10:J	9:J,8		
P1:16	P2:16	10:K	9:K,9		
P1:17	P2:17	10:L	9:L,10		
P1:18	1:16				
P1:19	+12V				
P1:20	1:17				
P1:21	-5V				
P1:22	P2:22	7:20	9:R		
P1:23	P2:23	7:X	9:13		
P1:24	+5V				

PROM socket B

From	To	To	To	To	Comments
P2:1	P1:1	7:19	9:P		
P2:2	P1:2	7:W	9:12		
P2:3	P1:3	7:18	9:N		
P2:4	P1:4	7:V	9:11		
P2:5	P1:5	7:17	9:M		
P2:6	P1:6	7:U			
P2:7	P1:7	7:16			
P2:8	P1:8	7:T			
P2:9	P1:9	10:C	9:C,3		
P2:10	P1:10	10:D	9:D,4		
P2:11	P1:11	10:E	9:E,5		
P2:12	GND				
P2:13	P1:13	10:F	9:F,6		
P2:14	P1:14	10:H	9:H,7		
P2:15	P1:15	10:J	9:J,8		
P2:16	P1:16	10:K	9:K,9		
P2:17	P1:17	10:L	9:L,10		
P2:18	1:19				
P2:19	+12V				
P2:20	1:18				
P2:21	-5V				
P2:22	P1:22	7:20	9:R		
P2:23	P1:23	7:X	9:13		
P2:24	+5V				

Rear panel

From	To	To	To	To	Comments
C2:1	8:Y				RECORDER +5V
C2:2	8:21				RECORDER GND
C2:3	8:19				RECORDER CLOCK
C2:4	9:21				RECORDER D ₇ (MSB)
C2:5	9:20				RECORDER D ₅
C2:6	9:19				RECORDER D ₃
C2:7	9:W				RECORDER D ₂
C2:8	9:18				RECORDER D ₁
C2:9	9:V				RECORDER D ₀ (LSB)
C2:10	9:X				RECORDER D ₄
C2:11	8:W				RECORDER RESET
C2:12	9:Y				RECORDER D ₆
C2:13	8:V				RECORDER W
C2:14	8:20				RECORDER ANALOG ON
C2:15	8:X				RECORDER ADC ENABLE
C2:16	8:18				RECORDER E
I2:A	S11:3	10:Y			DATA END MARKER LED (ANODE)
I2:C	7:15				(CATHODE)
I3:A	S12:3	10:15	1:5		OUTPUT MODE LED (ANODE)
I3:C	7:S				(CATHODE)
S11:2	+5V				DATA END MARKER SWITCH
S11:3	10:Y	I2:A			
S12:1	9:U	2:17			OUTPUT MODE SWITCH
S12:2	+5V				
S12:3	1:5	10:15	I3:A		
B:1	14:20				X-AXIS ANALOG OUTPUT
B:2	12:20				Y-AXIS ANALOG OUTPUT
C1:1	14:R				BINARY OUTPUTS - ADDRESS (LSB)
C1:2	14:14				
C1:3	14:S				
C1:4	14:15				
C1:5	14:T				
C1:6	14:16				
C1:7	14:U				
C1:8	14:17				
C1:9	14:V				
C1:10	14:18				
C1:11	14:W				
C1:12	12:R				BINARY OUTPUTS - DATA (LSB)
C1:13	12:14				
C1:14	12:S				
C1:15	12:15				
C1:16	12:T				
C1:17	12:16				
C1:18	12:U				
C1:19	12:17				
C1:20	5:21				DATA VALID FLAG
C1:25	GND				

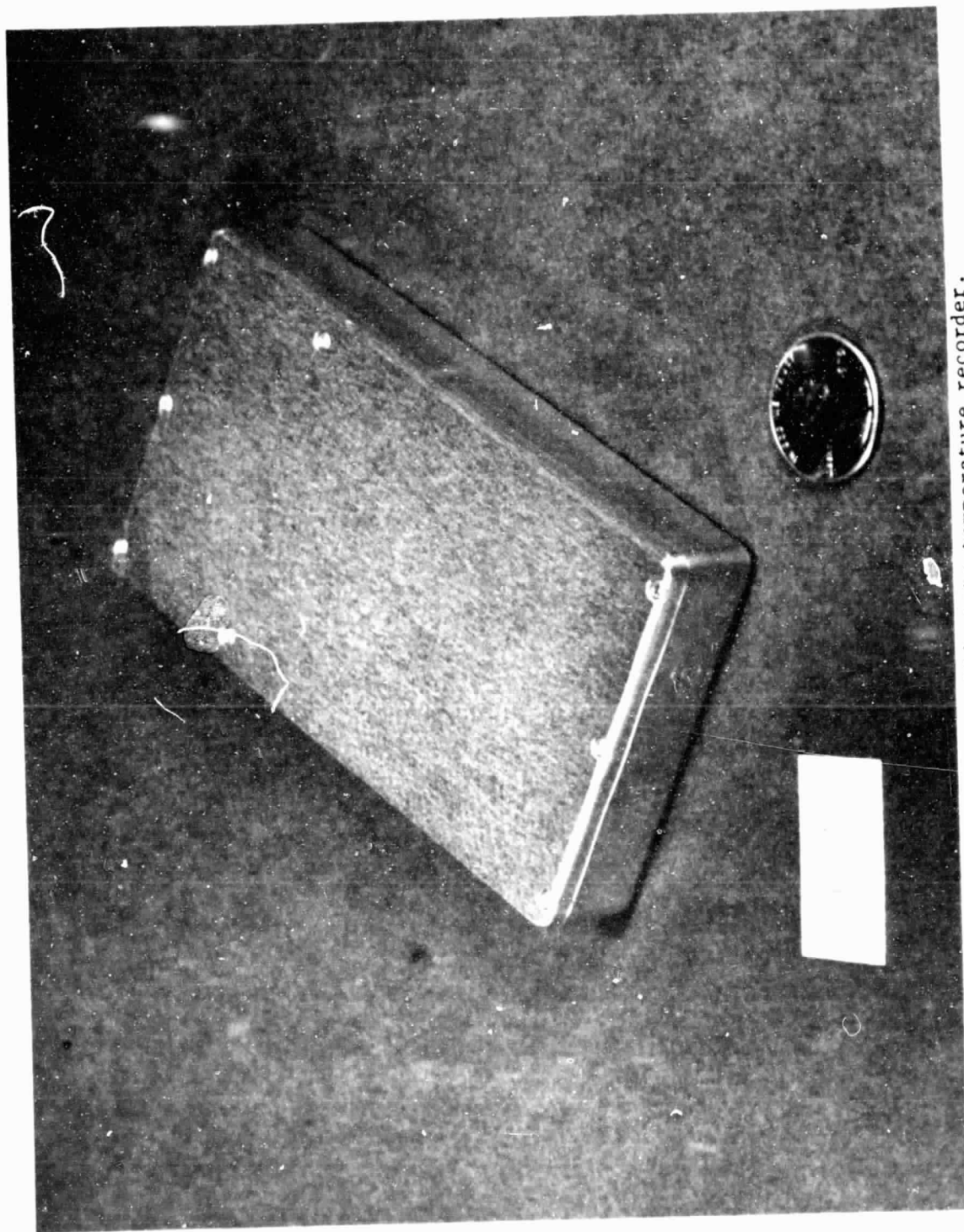


Figure 1.- Solid-state temperature recorder.

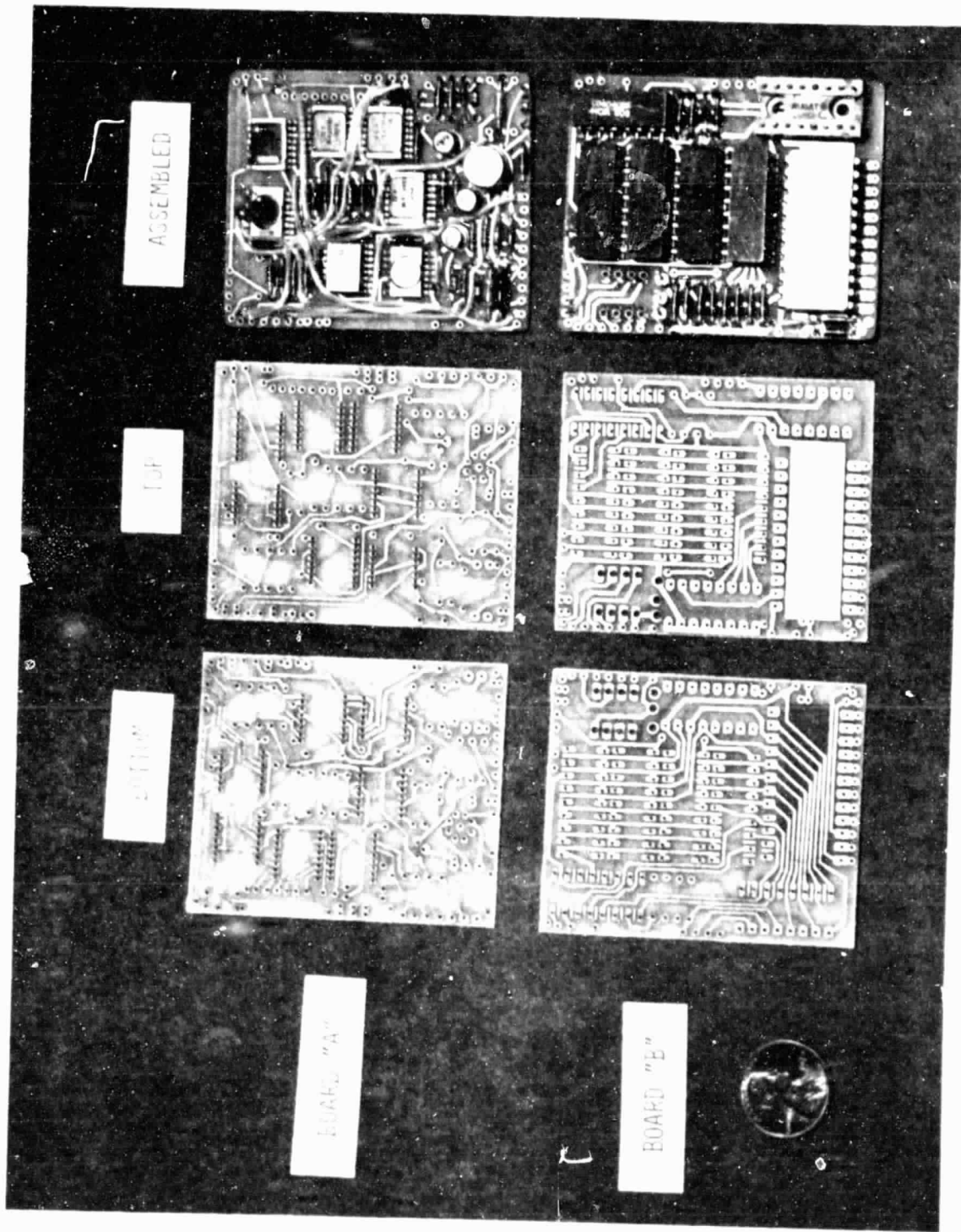


Figure 2.- Recorder construction.

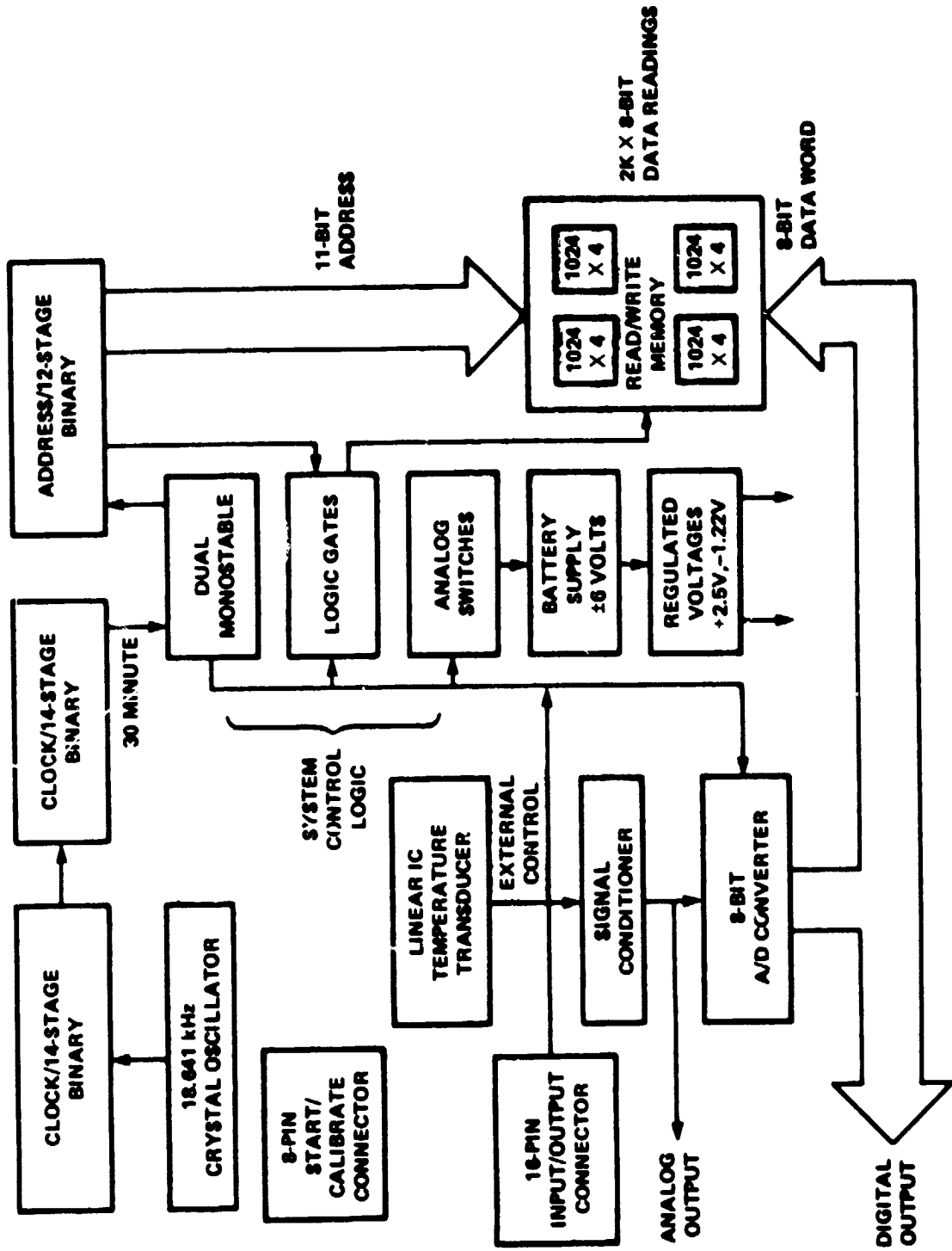


Figure 3.- Flight recorder block diagram.

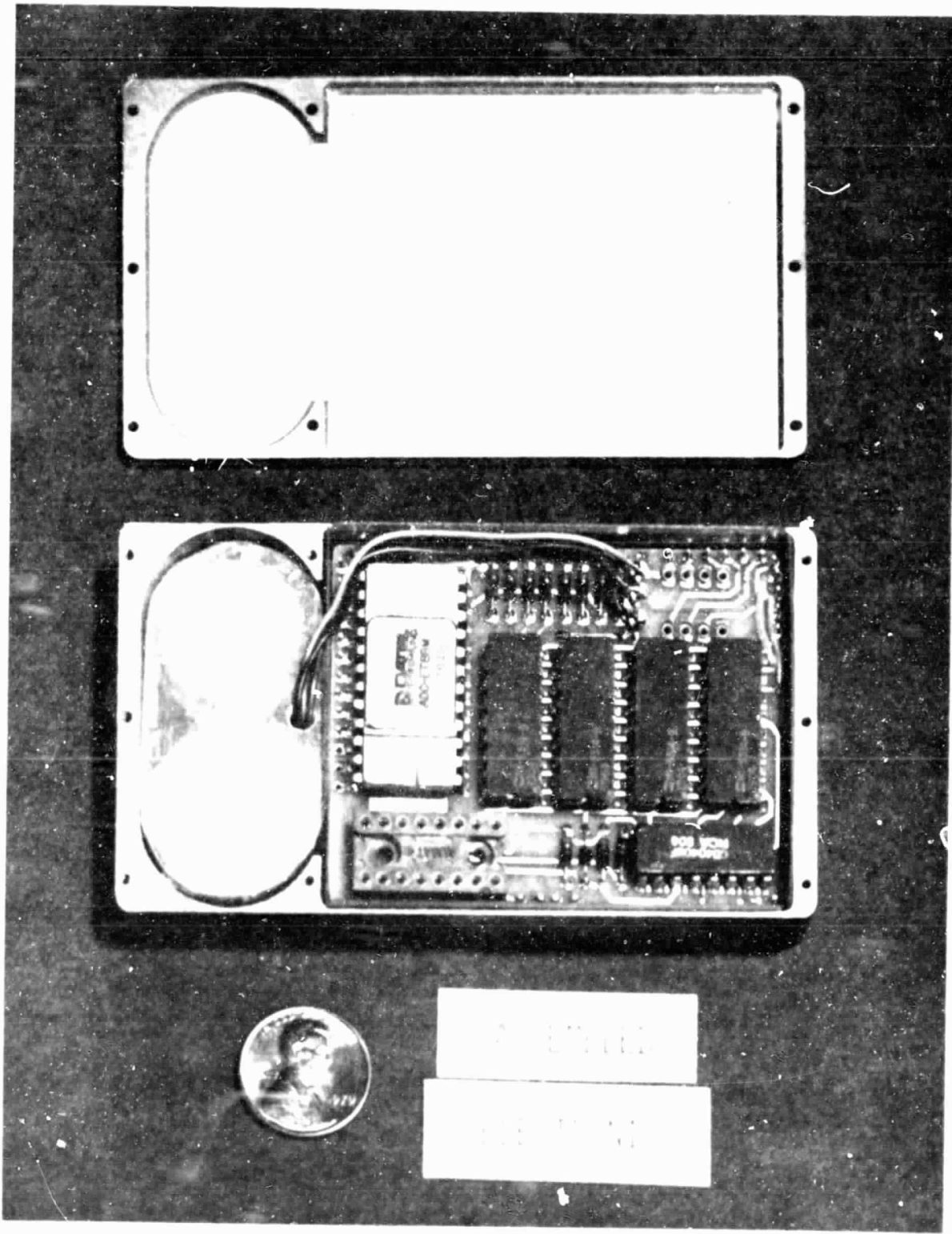
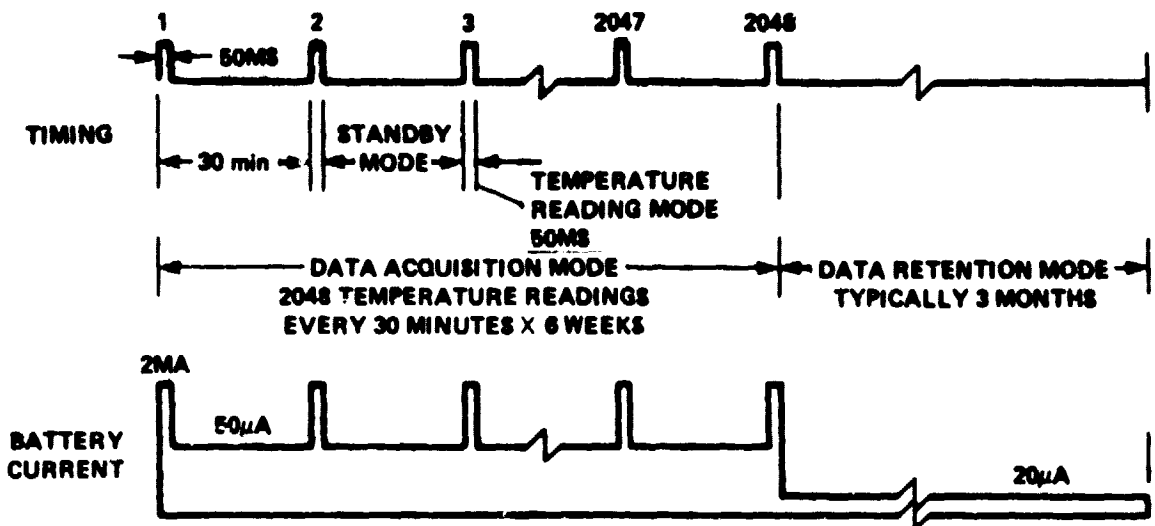
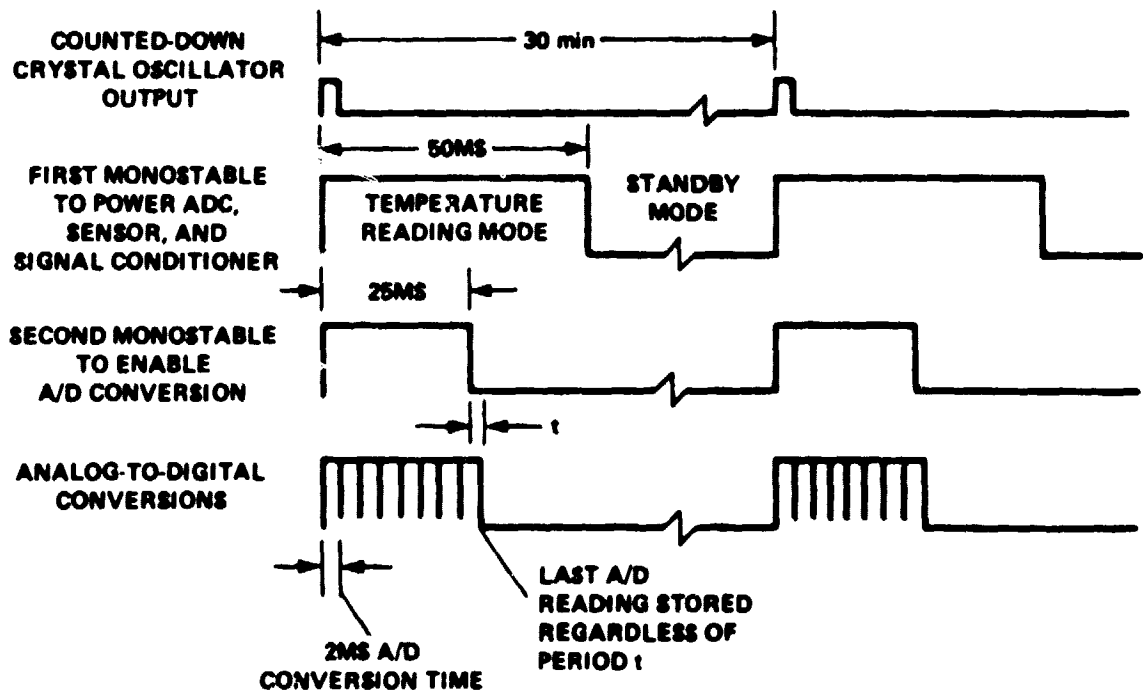


Figure 4.- Recorder with cover removed.



(a) Data acquisition and retention modes timing, and battery current drain.



(b) Temperature reading timing.

Figure 5.- Flight recorder timing diagrams.

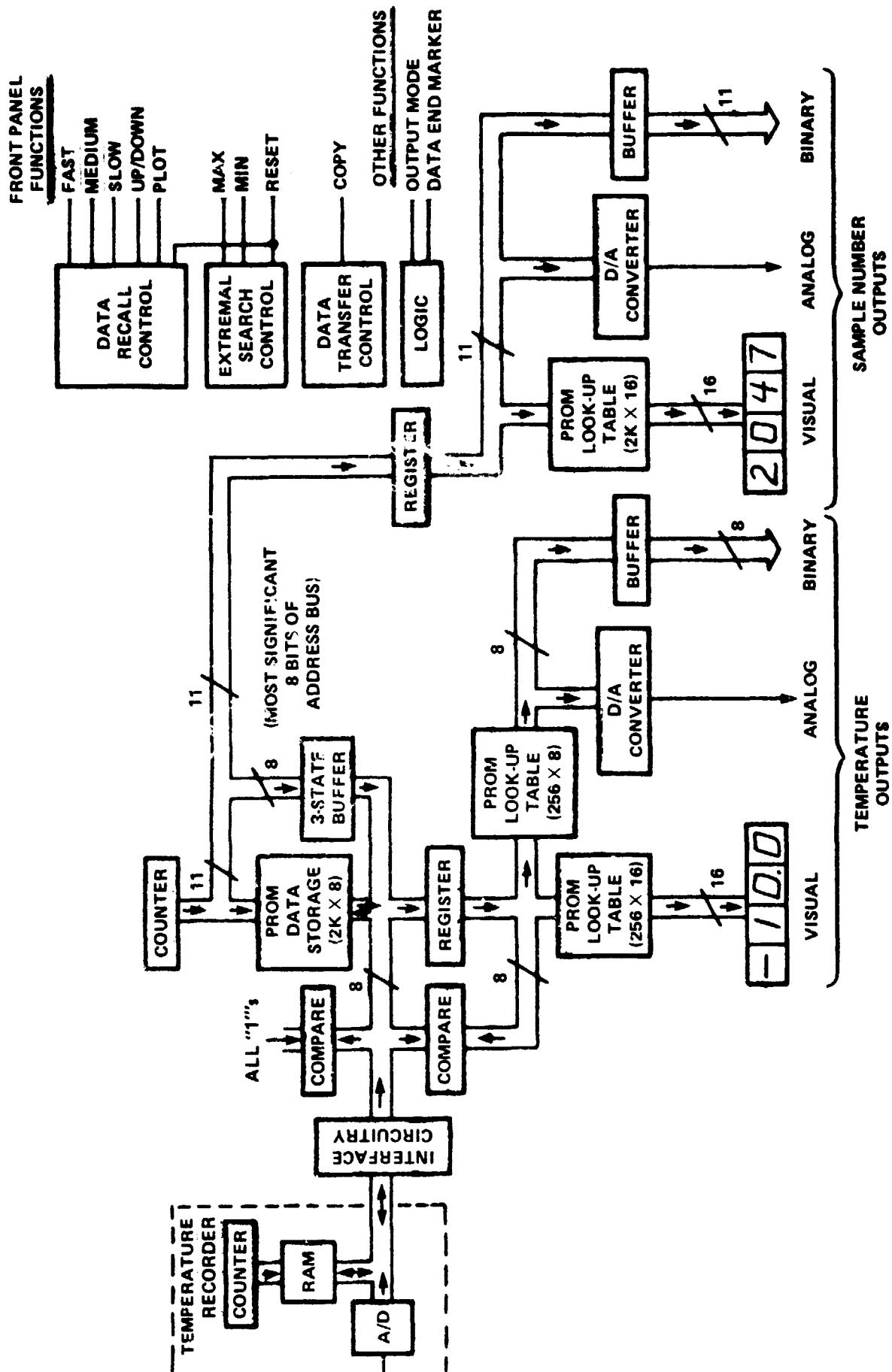


Figure 6.- Ground readout unit block diagram.

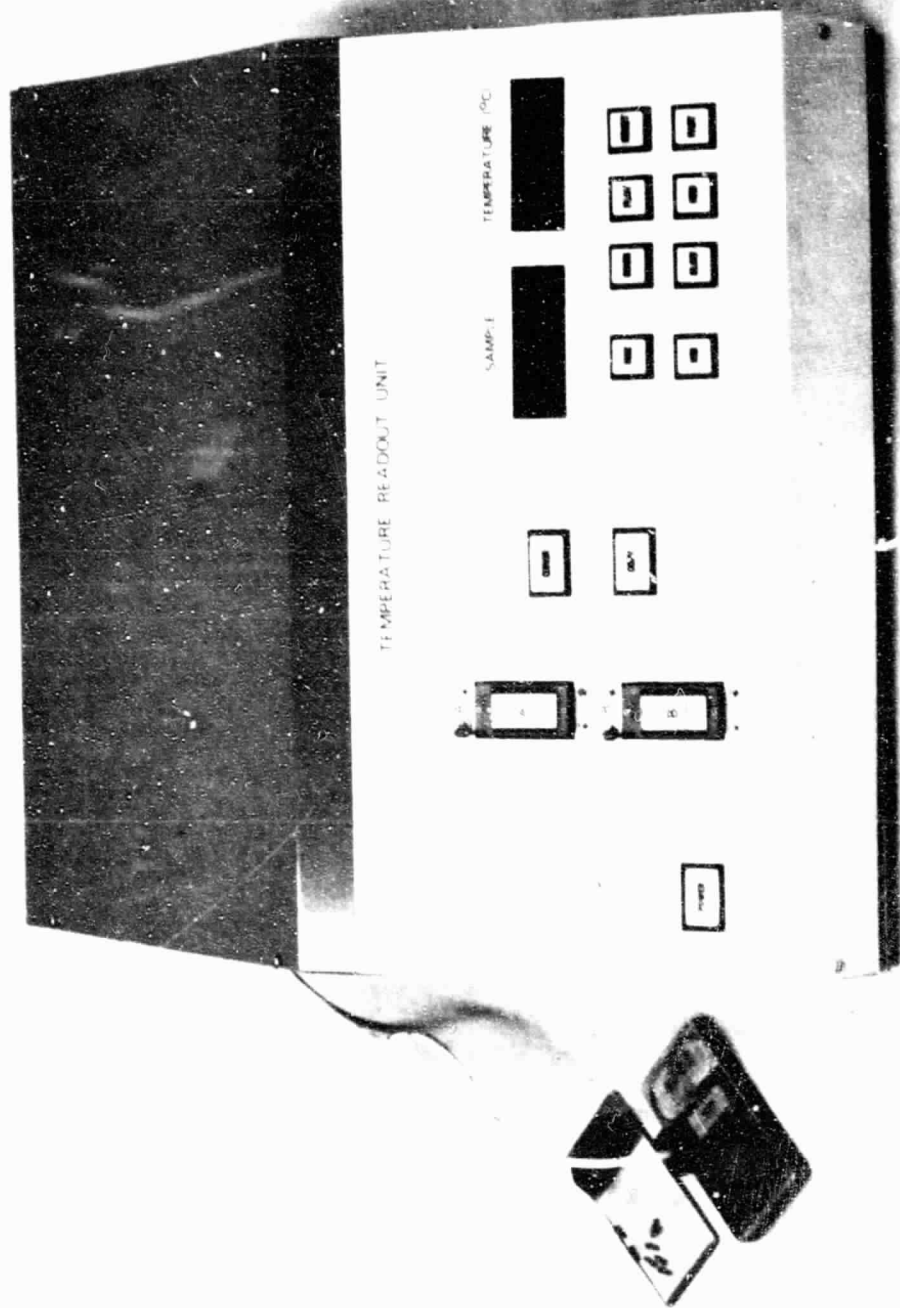


Figure 7.- Temperature readout unit connected to recorder.

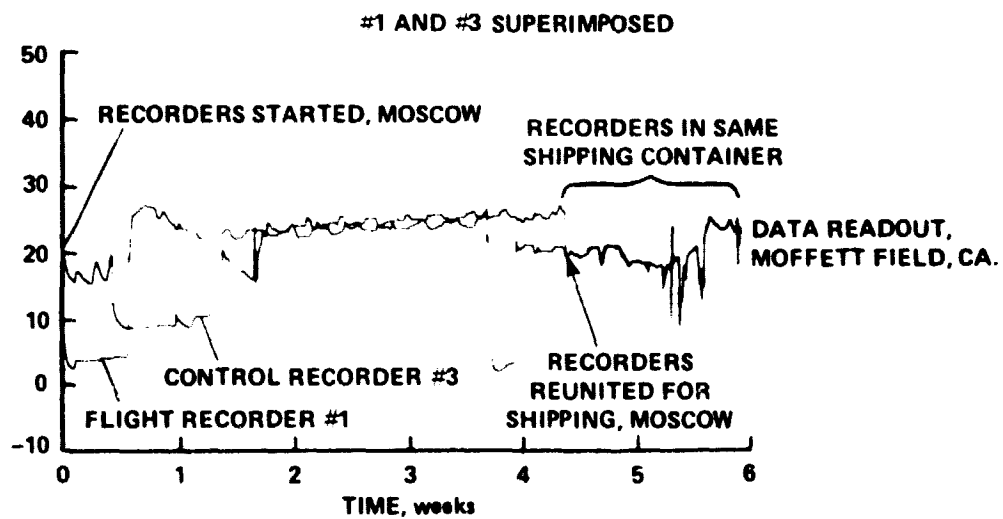
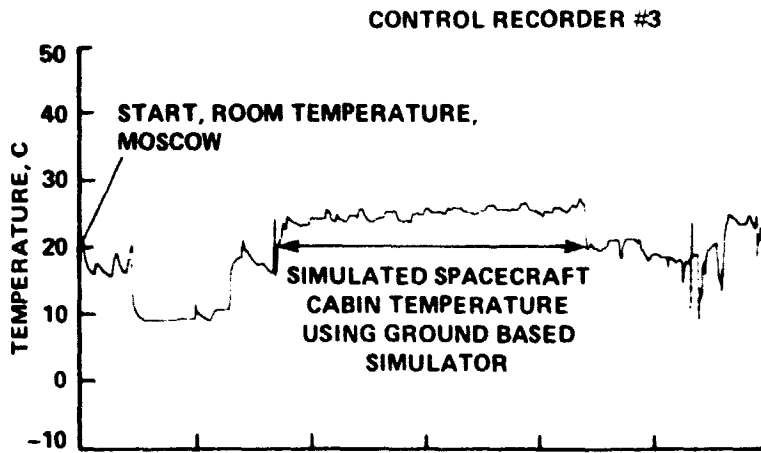
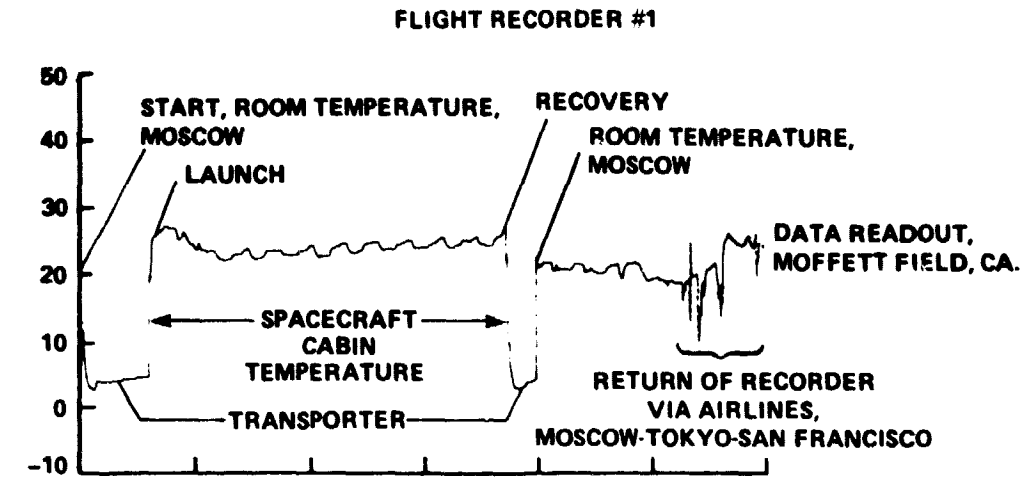


Figure 8.- Typical temperature/time plots from two of six recorders in Cosmos Mission. (K. A. Souza and M. R. Heinrich, Final Results of U.S. Experiments Flown on the Soviet Biological Satellite Cosmos 1129, 1981.

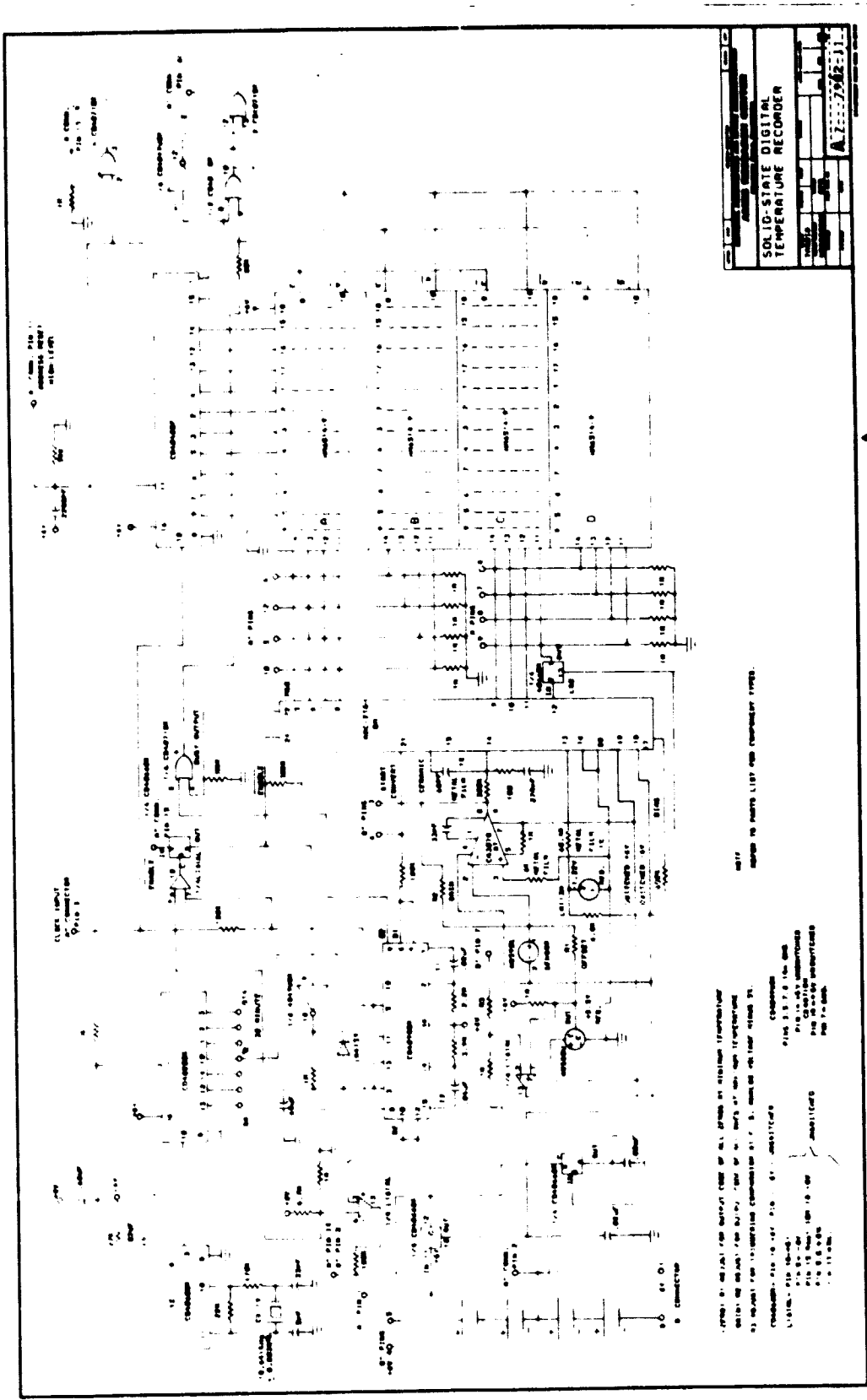


Figure 9.- Circuit diagram of recorder.

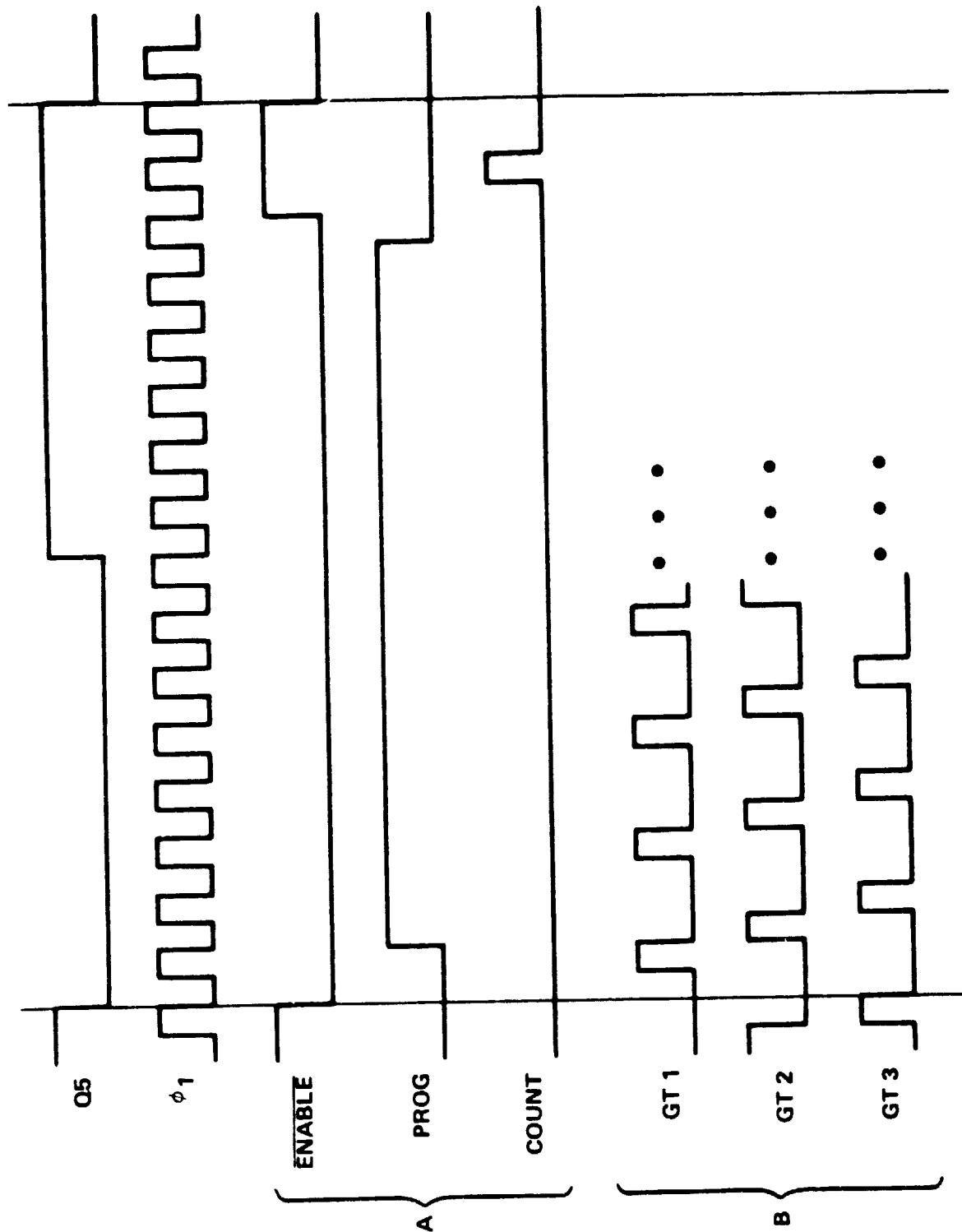


Figure 10.- Readout unit system timing.