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FINAL REPORT ON

PROTOTYPE MICROPROCESSOR CONTROLLER

Prepared For:

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Contract No.NAS5-25356

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WASHINGTON ANALYTICAL SERVICES CENTER, INC.
WOLF RESEARCH AND DEVELOPMENT GROUP

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SECTION 1.0
INTRODUCTION

The requirement for a microcomputer controller for STDN antennas was developed to solve problems with the present antenna control system and to add features that improve performance and simplify system maintenance and repair.

The application of microcomputer technology to this system reduces its physical size by the implementation in firmware of functions presently performed by hardwired logic. The reduction in the number of components increases system reliability. A simular benefit is derived when a graphic video display is substituted for several control and indicator panels. A substantial reduction in the number of cables, connectors and mechanical switches is achieved.

In contrast with the equipment they replace, the microcomputer and video display are programmable. The implementation of new features or the modification of existing functions is no longer a major effort and fewer, if any, hardware components would be required. The present system is used only when tracking. Between satellite passes the system remains idle. On the other hand, the microcomputer-based system can be programmed to perform calibration and diagnostics, to update the satellite orbital vector, and to communicate with other network systems.

This new design is equally applicable to antennas and lasers. Differences in system operation can easily be accommodated in the software so that a greater degree of hardware standardization may be achieved.

In Figure 1.1 the present antenna control system is shown. Its principal components are the dual-axis servo-

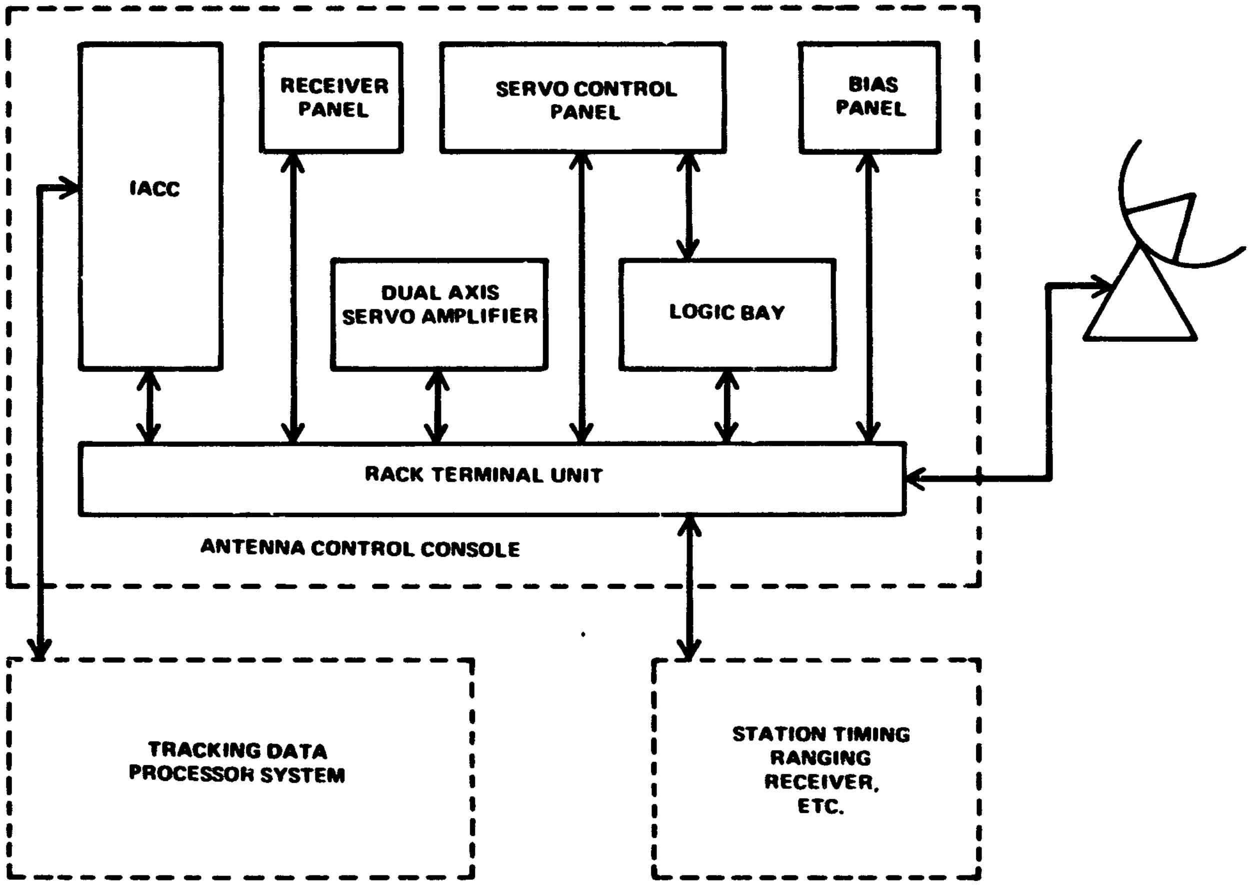

FIGURE 1.1. ANTENNA CONTROL SYSTEM

amplifier, logic bay, servo control panel, bias panel, receiver panel and the IACC (Interface to the Antenna Control Console). The rack terminal unit distributes signals to the various antenna subsystems. The proposed Antenna Control Console is shown in Figure 1.2. The logic bay, the dual axis servo-amplifier and the IACC are replaced by the microcomputer chassis, while the graphic video display system is substituted for the various control and indicator panels.

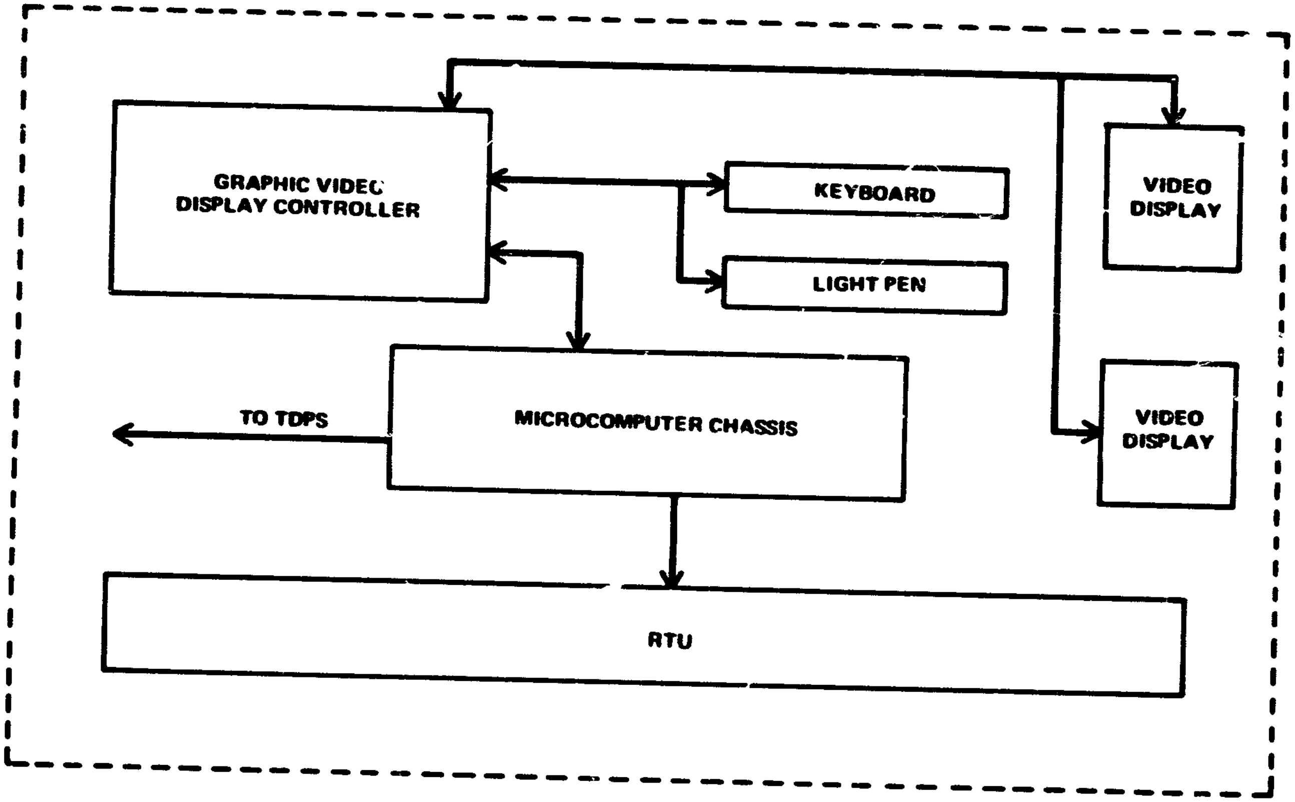

FIGURE 1.2. MICROCOMPUTER–BASED CONTROL SYSTEM

SECTION 2.0
SYSTEM DESIGN AND DEVELOPMENT

Given the basic approach outlined in the introduction, the next task consisted of the selection of components for its implementation.

The criteria for the selection of microcomputers are basically the same as for all computers. Word size, instruction set, speed, addressing range, accessories and available software are some of the considerations that affect the selection of any computer. Although cost of the hardware is almost always a major consideration, the cost of microcomputer hardware is relatively small compared to system development costs, so that performance should be the principal criterion.

Several 8-bit and 16-bit microprocessors are available. Of the 16-bit devices one, the INTEL 8086, is a new design while the others are micro-versions of minicomputers. Being upwardly compatible with previous INTEL 8-bit micros, the 8086 can use most of the support hardware already available. The INTEL development system, particularly when equipped with an in-circuit emulator (a device that allows running programs written for one computer on a different computer), is a powerful and versatile system for the development and testing of software and hardware. In other respects, the 8086 meets all the performance criteria. Insofar as the instruction set, addressing range, and speed are concerned, the 8086 is superior to some mini-computers.

Many types of graphic video displays are available. It was decided to select a color display since color conveys greater information and provides better image contrast. Graphic displays come in several screen sizes and image resolutions. Since the displays would replace panels that controlled and displayed many functions, a large monitor screen would be preferred. A medium resolution 19" monitor was selected that displayed 512 and 512 pixels (image dot). This resolution is adequate for the type of information to be displayed.

This information consists of alpha-numeric and graphic data. The system should be able to display rapidly changing data in real-time. The Chromatics CG1999 met this requirement. A typical format for tracking with the USB 9 meter antenna is shown in Figure 2.1. The alphanumeric data in the upper third of the display is updated at a rate of 3/s. The remaining alphanumeric fields and graphic data are updated as necessary. The background graphic data, i.e. the squares, rectangles and labels are initialized once at the start. Data is displayed by sending a sequence of commands to the display controller. In order to meet the real-time requirement, the display is furnished with a Direct Memory Access (DMA) channel. The 8086 is similarly equipped. However, the communication protocols for the two channels are not compatible. A custom interface was designed to arbitrate the data transfer between them. The combined system is capable of transferring 400 K bytes per second.

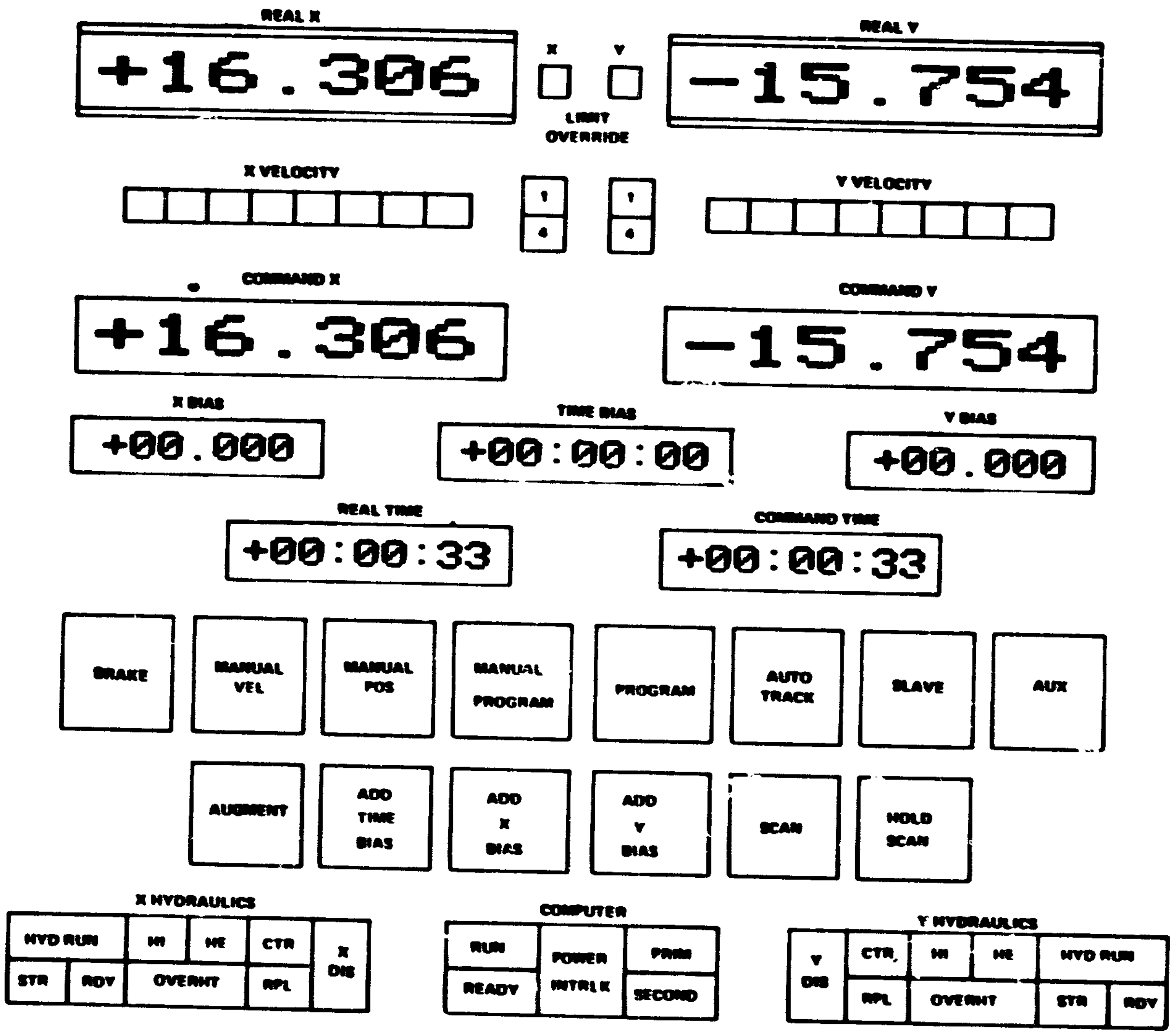

FIGURE 2.1. TYPICAL DISPLAY FORMAT

SECTION 3.0
HARDWARD IMPLEMENTATION

The entire system consists of a Digital Controller subsystem, a video display and the antenna simulator. The modularity of computer boards increases the reliability and ease of maintenance of each part of the system. A block diagram of the entire development system is shown in Figure 3.1.

Most of the programming was done for the Digital Controller which is the heart of the system. Erasable Programmable Read Only Memory (EPROM) was used during development so that changes were easily made by erasing and then reprogramming them. If changes ever need to be made while the system is in the field, only the PROMs would be affected.

Each iSBC 86/12A board contains 32K Random Access Memory (RAM), expandable to 64K and enough ROM socket space to hold 32K bytes. The 8086 microprocessor being used is extremely fast and is capable of accessing up to one megabyte directly. This system has ample capacity for any upgrade which may be needed.

3.1 DIGITAL CONTROLLER

The system consists of a main Central Processing Unit (CPU) board, an auxiliary CPU board containing additional memory, a Direct Memory Access (DMA) controller board and a wirewrap board on which a DMA interface circuit was implemented. The configuration of the boards in the chassis is shown in Figure 3.2.

During development of the software, an in-circuit emulator, ICE-86, was used because of its full symbolic debugging

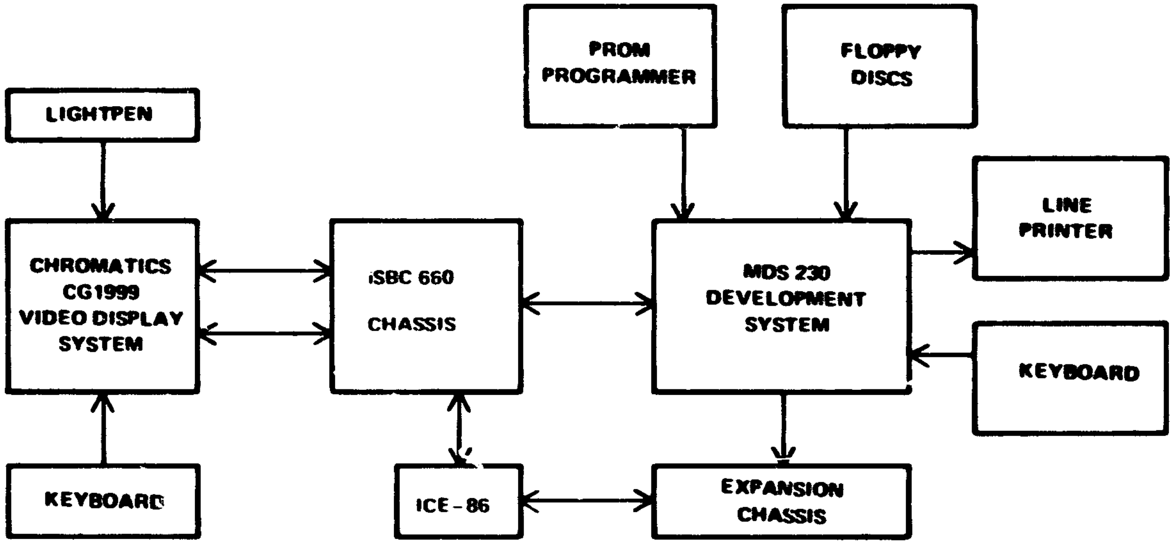

FIGURE 3.1 DEVELOPMENT SYSTEM

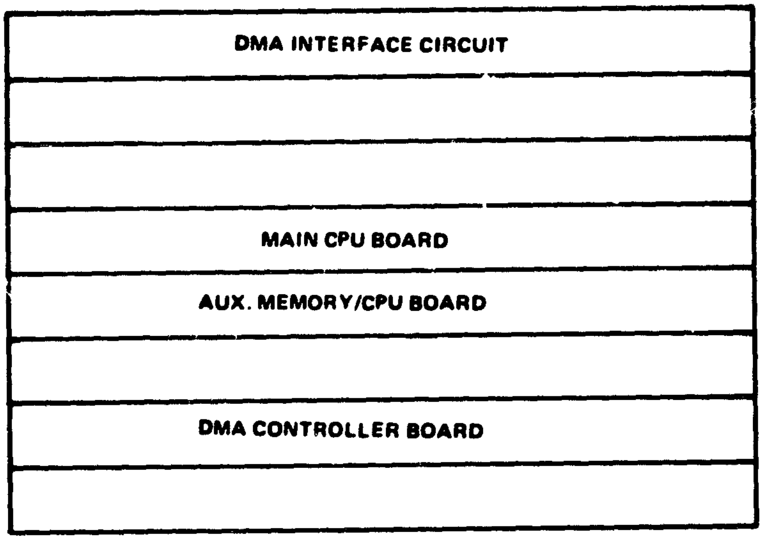

FIGURE 3.2. DIGITAL CONTROLLER BOARD LAYOUT

capability. In the final system, however, the in-circuit emulator was removed and the software was programmed into PROMs. With the in-circuit emulator removed, the development system is used as an antenna simulator.

The system bus is the INTEL MULTIBUS. The two CPU boards and the DMA controller board all communicate over this bus. A diagram of the interfacing to the MULTIBUS is shown in Figure 3.3.

3.2 DISPLAY AND OPERATOR INTERFACE

The CHROMATICS video display system contains the main output display for antenna status. It also acts as the operator's interactive device to the antenna. The system consists of a color CRT, a keyboard, a lightpen, a DMA controller board and software to generate graphic functions and to handle the Serial Input/Output (SIO).

The SIO input, keyboard and lightpen functions all have an appropriate interrupt. The SIO and keyboard functions have a single data byte associated with them whereas the lightpen has 4 data bytes.

The SIO line is interfaced to the main CPU board in the Digital Controller system. It runs at 9600 baud using no parity bits and 1 stop bit. It is used primarily for the transfer of command strings from the digital controller to the CHROMATICS video display system. Only short strings of specific commands are sent across this line because of its slow speed. Block data transfers are carried out by the DMA, which is described in the next section. The SIO is also used to transfer operator initiated commands to the digital controller.

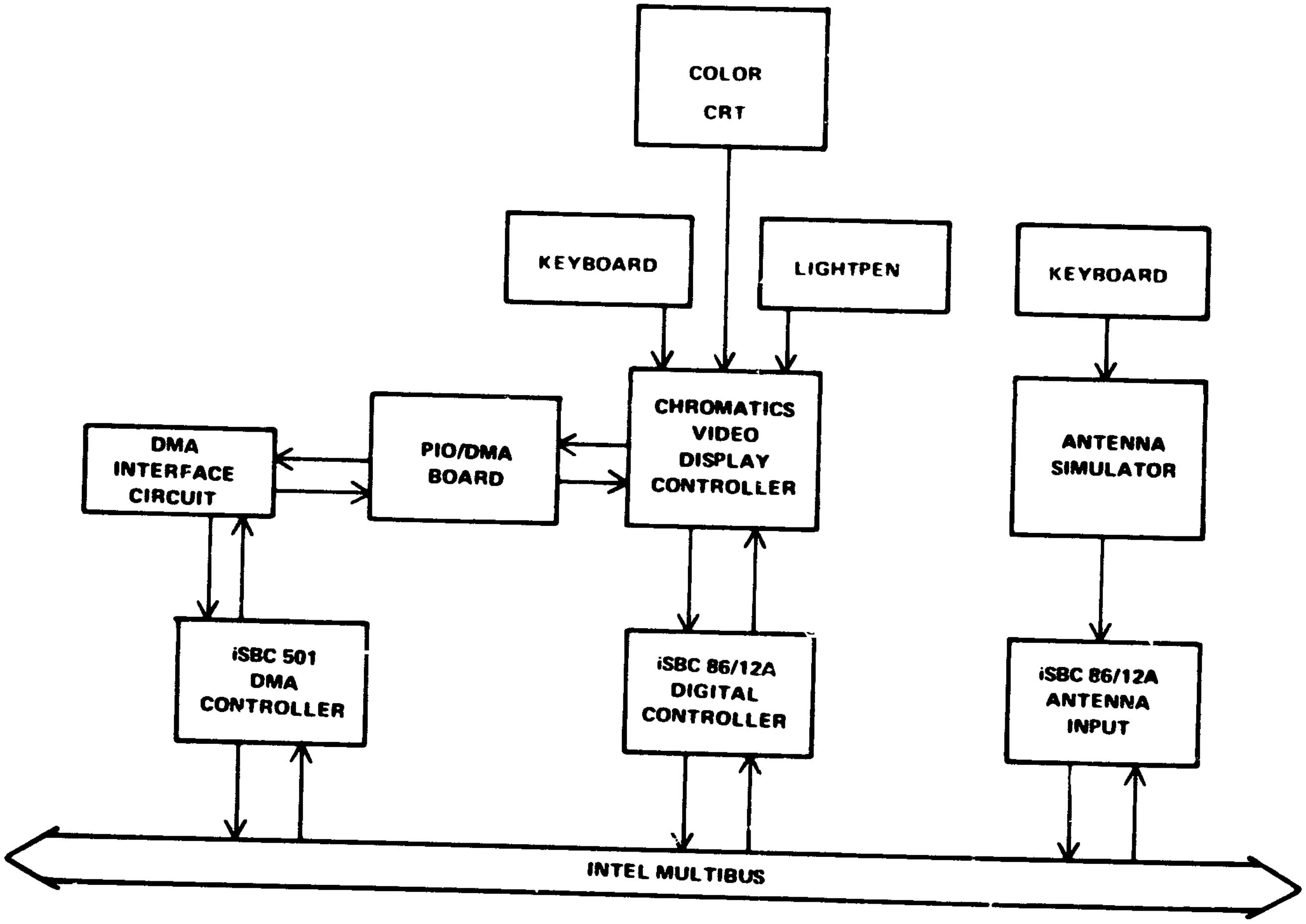

FIGURE 3.3. SYSTEM INTERCONNECTION DIAGRAM

The keyboard is interfaced directly to the CPU operating system of the CHROMATICS. It is used only by the operator when he wishes to enter a character into a selected bias to be processed by the digital controller. The keyboard is only enabled when a bias has been selected (which is indicated by a cursor prompt on the appropriate position on the screen), and there are no previous keyboard data waiting to be processed.

The lightpen is interfaced through a control board in the CHROMATICS to the operating system of the display. It is used by the operator when he wishes to select a mode or choose another function of the antenna control system. The procedure is to point the pen at the desired location on the CRT screen and touch the tip of the pen with the forefinger. This will flood the screen with blue from the top, down to the lightpen position and generate an interrupt to the CPU operating system. The screen coordinates are then transfered over the SIO line to the digital controller where they are processed. The lightpen is enabled only if there is no previous lightpen data waiting to be processed.

3.3 DIRECT MEMORY ACCESS

For the purpose of high speed data block transfer, direct memory access, DMA, is used. Since the Intel and Chromatics DMA boards' protocols are incompatible, an interface circuit is required. The circuit is responsible for synchronizing the DMA signals upon initiation of a transfer and the subsequent timing of handshaking signals for the remainder of the transfer. The circuit is shown in Figure 3.4.

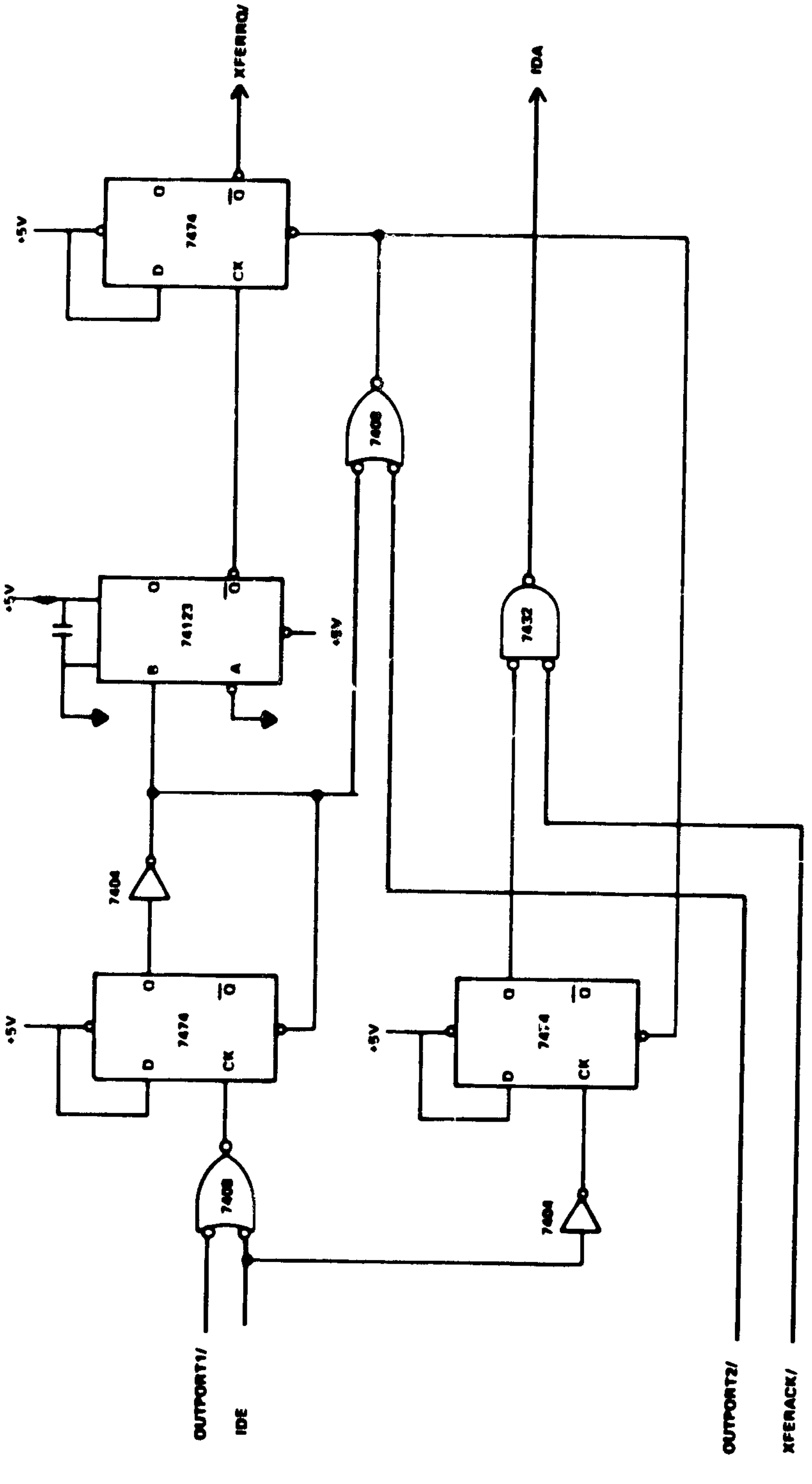

FIGURE 3.4. DMA CIRCUIT

3.3.1 Theory of Operation

DMA operation can be considered independent of the rest of the system because during the transfer of data, it only interacts with the system in order to steal a bus cycle to read a byte from memory. Until it is ready to read another byte, it interacts only with the peripheral device through the interface circuit. After the DMA transfer is complete, the main CPU is interrupted, signaling the operation is complete.

The DMA sequence of events are as follows:

- If the DMA controller is ready to initiate a transfer, then XFER RQ/ is pre-reset through OUTPORT2/.
- The length register is filled with the number of bytes to be transfered.
- The control register is filled with a control word specifying 8-bit transfer from system memory to the peripheral device (the CHROMATICS DMA board).
- The address register is filled with the first memory location to be accessed.
- XFER RQ/ is asserted through OUTORT1/ which initiates the DMA transfer.
- As XFER RQ/ is asserted, the DMA board gains control of the bus and generates a memory read command. After the data byte is placed on the bus, the control logic issues a transfer acknowledge signal (XFER ACK/)

- The CHROMATICS DMA asserts $\overline{\text{IDE}}$ a short time thereafter when the data byte is accepted. $\overline{\text{IDA}}$ is then reset.

- $\overline{\text{IDE}}$ remains true for a minimum of 1 microsecond for the data byte to be read. As $\overline{\text{IDE}}$ is reset, XFER RQ/ is also reset. The data transfer is complete.

- The length register is decremented and if not zero, the DMA control logic asserts XFER RQ/ again and another transfer cycle is begun.

- When the length register becomes zero, an interrupt is generated to signal that the block transfer has been completed.

The timing diagram for DMA operation is shown in Figure 3.5.

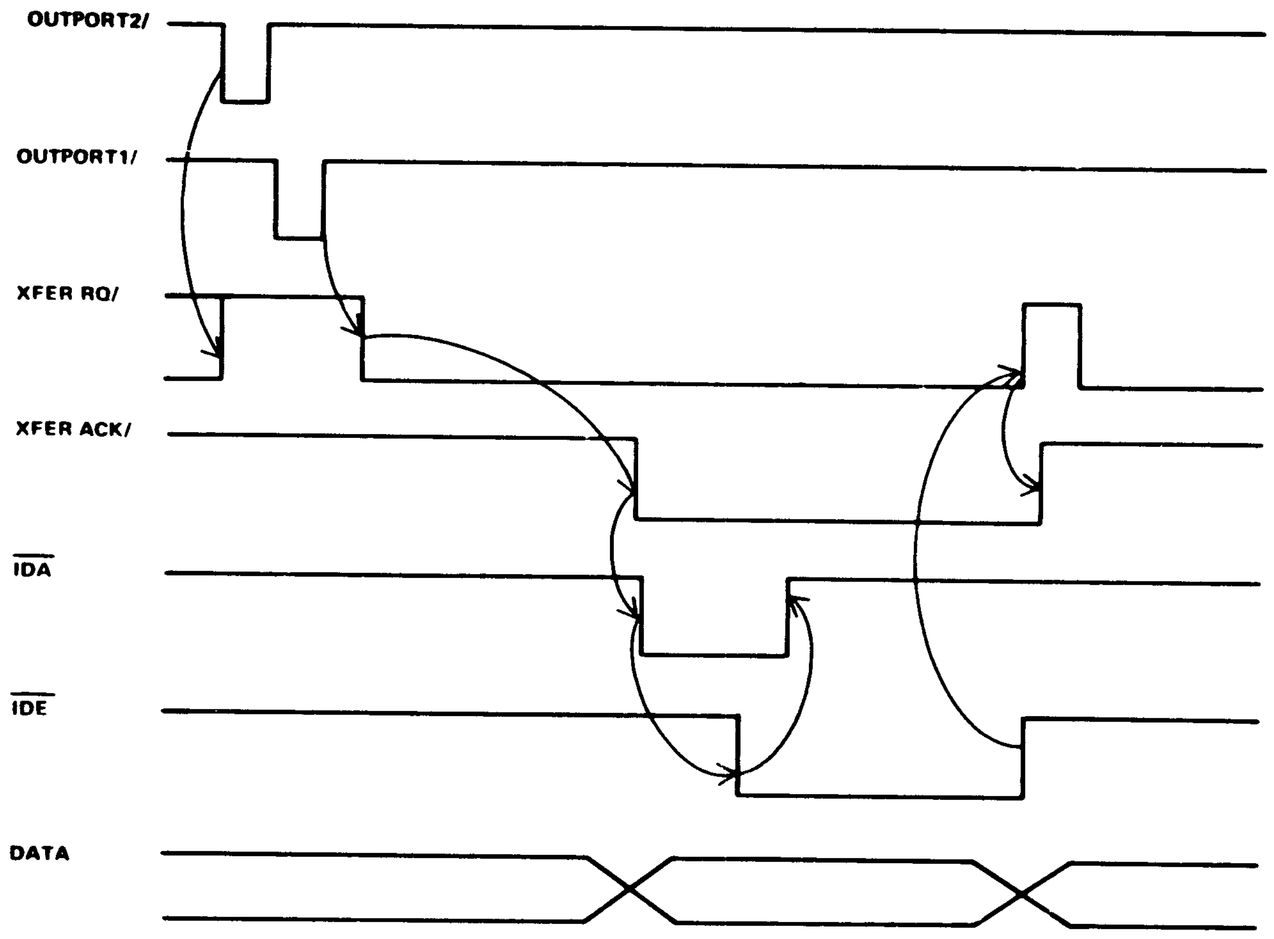

FIGURE 3.5. DMA TIMING

SECTION 4.0
SOFTWARE

The majority of the software was written for the INTEL 8086 microprocessor in the Digital Controller. INTEL's assembly language, ASM86, was used because of its efficiency in the programming of real-time processing routines.

The main program resides in PROM on the main CPU board and is just over 5000 bytes in length. The program on the auxiliary CPU board is very small because it just transfers status data from the antenna simulator to the main program.

The remainder of the software is written in Z-80 assembly language for the CHROMATICS video display system. This is a relatively small program, since the CHROMATICS system is provided with extensive software. The program accepts command strings from the Digital Controller and passes them to the CHROMATICS graphics operating system to be processes, and transfers operator commands to the Digital Controller.

4.1 CONTROL SYSTEM PROGRAMS

The control system programs comprise the bulk of the software. These programs include real-time processing of interrupts, hydraulics control, mode control and operator command processing.

4.1.1 Interrupt Processing

There are a total of 4 interrupts used in normal processing on the main board. These are separated into 2 types, synchronous and asynchronous.

Synchronous interrupts occur at predefined intervals. The real-time clock interrupt occurs 3 time per second. It sets the DMA process flag on every occurrence, and signals to the main program that it is to initiate a DMA transfer to refresh the display positions and velocities. The other function of this interrupt is to update the real-time clock once per second.

The other synchronous interrupt is the hydraulic startup timer which, when started, produces 15 interrupts spaced 1/3 second apart which creates a 5 second delay. If both the control and replenish pressures are not high after this period, then the hydraulics are shut down.

There are also asynchronous interrupts which occur only to signal an event. These are the DMA completion interrupt which signals the completion of a DMA transfer and the SIO interrupt which signals that a data byte has been received.

The function of the SIO interrupt routine is simply to read the data sent, store it in a circular buffer and increment the buffer pointer.

The DMA completion interrupt clears the DMA busy flag and resets the DMA processor.

The interrupts range from highest priority, those which contain little processing, to lowest priority, those which require more processing as follows:

IR4 - DMA completion interrupt
    - From Multibus signal INT4/generated by
      the DMA controller

IR5 - Hydraulics Startup time
- From 8253 PIT Timer 1 Out (TMR1 INTR)
- In Rate Generator Mode

IR6 - Real-time clock Interrupt
- From 8253 PIT Timer 0 Out (TMRO INTR)
- in Rate Generator Mode

IR7 - SIO Data Available
- From 8251A USART Receiver Buffer Full (51RX INTR)

4.1.2 Hydraulics

There are four function of the hydraulics software:

1. Display update
2. Status update
3. Hydraulics start-up (X or Y)
4. Interaction with braking system

There are separate control words, status words and motion flag for each axis along with a flag containing information about hydraulic running condition for both axes.

The format of the control words is the same as that of the status words for both axes. If a bit is set in a control word, this means that the status of that parameter is to be toggled whereas a bit set in a status word denotes a specific condition. If more than one bit is set in a control word, each bit is processed before an exit to the main program is made.

TABLE 4.1

HYDRAULIC CONTROL/STATUS WORD

BIT	FUNCTION
0	AXIS DISABLE
1	POWER INTERLOCK
2	HYDRAULICS STARTED
3	K2 - RELAY ON
4	REMOTE START
5	TDPS START
6	OPERATOR START-UP
7	REPLENISH PRESSURE LOW
8	CONTROL PRESSURE LOW
9	OVERHEAT
10	HEAT EXCHANGE TERMPERATURE
11	HI TEMPERATURE
12	HYDRAULICS RUNNING
13	HYDRAULICS STARTED
14	HYDRAULICS READY

The hydraulics program is entered through either the X-axis or Y-axis and the only interaction between the two would take place when a hydraulic system is started or shut down which would send the entire system into brakemode, disabling the axes.

The control word is tested to find out which parameter of the hydraulics needs to be updated. After all changes have been made the display is updated. A check is made to set flags indicating brakes are to be released, enabling the antenna to be moved by the mode control program. If the hydraulics are started then the status is updated upon re-entrance of the routine after a 5-second delay is executed.

4.1.3 Mode Control

Upon entering the mode control program, first the status of system is updated, then the status of the display is changed. There are a total of 4 words need to accomplish this task:

REQUESTMODE: Requests the status of a mode be changed.

CONTROLMODE: Indicates whether a particular mode is selected or not.

VALIDMODE: Indicates whether a mode is valid to be selected.

INVALIDMODE: Indicates a mode is neither selected nor valid.

TABLE 4.2
MODE CONTROL WORD

BIT	FUNCTION
0	TDPS RUN
1	PRIMARY/SECONDARY
2	HOLD SCAN
3	SCAN
4	ADD Y BIAS
5	ADD X BIAS
6	ADD TIME BIAS
7	AUGMENT
8	AUXILIARY
9	SLAVE
10	AUTOTRACK
11	PROGRAM
12	MANUAL PROGRAM
13	MANUAL POSITION
14	MANUAL VELOCITY
15	BRAKEMODE

All four words have the same format as far as bit positioning. A bit set in REQUESTMODE indicates a request to change modes whereas a bit set in the other words represents status. Even though it is obvious that if a mode is selected then it is also valid, it is only represented as being selected in order to avoid ambiguity in coloring the appropriate square in the display part of the program.

There are 4 distinct classes of modes that are selectable, which are:

MAJORMODE: Can be selected but not toggled, can only be turned off by selecting another major mode.

BRAKEMODE: Is a major mode but it is automatically selected if an adverse condition arises in the hydraulics or if a hydraulic system is started. Also may occur when a major mode is selected while both axes are disabled.

SUBMODE: Submodes are valid only after an appropriate major mode is selected. Submodes can be toggled.

PRIMARY/SECONDARY: Toggle switch which determines which major modes are valid.

All modes are lighted green if selected, blue if they are valid and black if invalid.

Upon entering the mode control program, if multiple bits are set in REQUESTMODE the one with the highest priority is processed and all others disregarded. The priorities are as follows:

TDPSRDY is always tested first because it is indicator of the status of the TPDS computer. If it is set then TDPS RUN is made valid, if not, then TDPS RUN indicator is automatically extinguished.

Priorities are assigned starting at the highest order bit of REQUESTMODE, which is brakemode. Major modes are of higher priority than submodes. The primary/secondary switch has the lowest priority.

If the brakemode bit was not set in REQUESTMODE, then the next lower bit is tested and so on until the correct bit is found. It is processed, the display is updated and exit is made to the main program.

4.1.4 Lightpen Processing

The X and Y-coordinates obtained directly from the CHROMATICS System are multiplied by a factor of 2^5 and 2^6 respectively. They represent the coordinates of a point on the CHROMATICS CRT with the origin at the lower left hand corner.

Upon entering the lightpen processing routine, the raw coordinates are shifted right the appropriate number of bits in order for the coordinates to be useful in a 512 x 512 point representation of the display CRT. Successive testing of coordinates, beginning at the top of the CRT image, is done and if the set of coordinates lie within a certain predefined boundary then appropriate action is taken, such as selecting a mode. If the selected point does not lie within a valid boundary then the routine is simply exited.

4.1.5 Keyboard Processing

The keyboard is only used to enter data into X-axis, Time or Y-axis bias values from the CHROMATICS keyboard.

The keyboard will only be enabled if no previous data remains to be processed and if a bias position has been selected, as designated by a cursor prompt on the specific character to be changed in the bias field. If the character is valid then the internal value of the bias and the displayed value will be changed accordingly, and the prompt is advanced to the next character. If the next displayed character is a colon or period, it is passed over and the next character is prompted. At the end of the displayed value, the prompt is removed.

The operator might wish to advance the prompt manually, in which case the left and right arrows are used to move the cursor. In order to remove the prompt, the operator would press "home".

If the system is in an add bias mode, the updated bias is added automatically to the displayed position or time.

4.2 CHROMATICS DISPLAY SOFTWARE

The CHROMATICS System functions mainly as a display and control panel. It contains software to generate many graphic symbols. The system uses a relatively slow Z-80 CPU to handle I/O and graphics so that it s not capable of handling complicated tasks in real-time.

All control data that is to be output from the system is put in a circular buffer. Each cycle of the program outputs a single byte. The buffer is scanned continuously for lightpen and keyboard data to be transferred to the Digital Controller.

Input data is processed immediately because there are only a few tasks involved other than commands to update the display. There are:

1. Enabling keyboard interrupt

2. Enabling lightpen interrupt

3. Initiating DMA transfer

Enabling interrupts are simple one-byte commands. Initiating the DMA controller for a transfer consists of one byte to begin the DMA initiation, 2 bytes for a start address and 2 bytes for length of data block to be transfered. After all of these parameters have been read, a flag is set and control is returned to the main program.. After completion of the transfer, normal program execution resumes.

4.3 COMMUNICATION ROUTINES

The Digital Controller and the CHROMATICS Video Display communicate over a serial I/O (SIO) line and via DMA.

The SIO is operated at 9600 band, approximately 960 characters per second. The DMA transfers data at a rate close to 400 K bytes/second. These two types of I/O also differ in their requirement for CPU overhead. For the SIO, the CPU must process every character sent or received. However, once the DMA is set up, it requires no further attention from the CPU until the block transfer is complete.

For these reasons, the SIO is used for the transfer of short strings of data, such as lightpen position ASCII keyboard data and the DMA for the transfer of large blocks of data such as graphics data, which can amount to several thousand bytes.

4.3.1 SIO - Input

Serial input to the main processor board consists only of operator initiated commands from the CHROMATIC Display Control system. There are two types of commands, a lightpen selection or a keyboard entry for the bias panel.

The lightpen selection data string consists of six consecutive bytes, the first being a special start byte indicating that the data are screen coordinates on the CHROMATICS CRT. The data itself consists of four bytes.

1. The lower byte of the X - coordinate

2. The higher byte of the X - coordinate

3. The lower byte of the Y - coordinate

4. The higher byte of the Y - coordinate

There is also a sixth and final byte sent from the CHROMATICS which is a special stop byte ending the screen coordinate transfer.

Keyboard data is also sent over this same line. The keyboard data string consists of only two bytes. The one byte is simply the ASCII code for the key and the other is a special stop byte to end the data string.

The SIO interrupt handler palces each byte of data in a circular buffer to be processed later after all pending interrupts are serviced.

4.3.2 SIO - Output

Serial output consists of commands from the master CPU to the CHROMATICS Display program pertaining to the control of interrupt enabling (lightpen & keyboard), DMA transfer initiation and the updating of the output display.

During the normal processing of serial input data and real-time updating of time displays, a large amount of data is assembled for output to the display. The data is assembled in strings and the address of the first byte of data is placed in a circular output buffer. The string is terminated by a null byte.

Since the output of data is a relatively slow operation, because polling of the USART is needed to avoid overrun errors, only one string is output during any processing cycle.

4.3.3 DMA

The DMA was described in detail in Section 3.3.

SECTION 5.0
CONCLUSIONS

The principal advantage of this implementation over the present system is the utilization of a general purpose microcomputer as opposed to hardwired logic. This approach allows the use of all system resources for different applications at different times. This is achieved by activating a specific program, from several stored in the system, to perform the required function. Additional functions or modifications are accomodated simply and economically by adding programs or modifying existing ones.

In terms of hardware, a system based on a microcomputer is more compact, simpler to design, and often more economical. The microcomputer board contains the CPU, sufficient memory to store the programs and some I/O capability. With additional boards to interface with the controlled equipment and the proper software, the system is basically complete.

The inherent advantages of general purpose microcomputers and the availability of high-level languages and better peripherals greatly simplify system design and development.