DEVELOPMENT & FABRICATION OF A FAST RECOVERY, HIGH VOLTAGE POWER DIODE

POWER TRANSISTOR COMPANY
800 WEST CARSON STREET
TORRANCE, CA 90502

PREPARED FOR
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
NASA LEWIS RESEARCH CENTER
CONTRACT NAS3-22539

NASA CR-165411

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16 Abstract

A high voltage, high current, fast recovery silicon diode has been designed and fabricated utilizing a positive bevel PIN mesa structure with glass passivation. The diodes are encapsulated in a standard DO-5 package and have the following characteristics: peak inverse voltage, 1200 volts - forward voltages at 50 amperes, 1.5 volts - reverse recovery time of 200 nanoseconds.

This project describes the use of positive bevels for PIN mesa structures to achieve high voltages. The technique of glass passivation for mesa structures is described. The utilization of high-energy radiation to control the lifetime of carriers in silicon is reported as a means to achieve fast recovery times.

Characterization data is reported and is in agreement with design concepts developed for power diodes.

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1. SUMMARY

The objective of this program is to develop a fast recovery 1200 volt, 50 ampere, silicon diode as specified by NASA Contract Number NAS3-22539, dated September 18, 1980.

In order to meet the specifications of this contract a PIN diffused structure was proposed. A positive bevel mesa structure was used to reduce surface fields in order to utilize a lower starting silicon resistivity in order to achieve the specified forward voltage with a minimum silicon area.

A positive bevel was etched into the p-n junction, which was later glass passivated.

Metallization used for contacting the cathode and anode areas was a TRI-METAL composition, which permitted solder reflow assembly.

The device was encapsulated in a DO-5 diode package. Solder-reflow techniques were used to assemble the device. The characterization data presented is in agreement with the design concepts presented in this report.

All devices delivered to NASA under this contract met or exceeded the required specifications. A full characterization of the diode is included in this final report.

2. INTRODUCTION

The NASA requirement in avionic systems for electrical power beyond the ten kilowatt level requires the use of a fast switching, high voltage, high current transistor.

The use of a fast switch, high voltage, high current power transistor necessitates a fast switching, high voltage diode with equivalent power capability of the transistor.

The recovery time of the diode would have to be shorter than that of the transistor by a factor of two in order to protect the transistor.

Diodes with these characteristics are used in snubber networks, as freewheeling diodes in inverter circuits and as rectifiers in high frequency power conversion equipment.

The combination of fast switch speed and high voltage required by the NASA specification is in the realm of the-state-of-the-art of power semiconductor device fabrication.

The NASA requirement for such a high voltage, fast switching diode is also a requirement for the industrial electronics market.

Specific applications are in electric vehicle motor drives AC and DC motor controllers. The 1000 volt capability of the diode will have an application in industrial motor controllers where the bus line

voltages are 480 volts. At the present time, two fast switch low voltage parts must be used in series to achieve the 1000 volt requirement and speed requirement at the expense of switching efficiency.

Diodes fabricated under this contract have been utilized in AC motor controller inverter circuits operating from 480 volt lines.

3. DEVICE DESIGN

3.1 Structure

The device is fabricated from 35 Ωcm thermal neutron, transmutation N-type doped, float zone silicon. Float zone silicon exhibits high minority carrier lifetime and low oxygen and carbon content. Neutron transmutation doping involves the nuclear conversion of silicon atoms into phosphorus dopant atoms by exposing (intrinsic) silicon to a flux of thermal neutrons in a nuclear reactor core. The nuclear reaction is $Si^{30}_{14} + n \rightarrow P^{31}_{15} + e^-$. The silicon isotope Si^{30}_{14} absorbs a thermal neutron and becomes Si^{31}_{14}, Si^{31}_{14} is unstable and emits an electron to become P^{31}_{15}. This technique allows the fabrication of N-doped float zone silicon of extreme homogenity, i.e., small radial variations and reduced striations (resistivity microvariations); a result impossible by any of the other growing and doping methods. Low resistivity variations across the wafer minimizes the wafer thickness required as a function of the resistivity and the intrinsic layer minority carrier lifetime.

Terminating the p-n junction with a glass passivated positive bevel moat allows the use of material with a relatively low resistivity level. The use of this material improves the trade-offs between blocking voltage, forward voltage drop and switch time.

The basic impurity concentration profile consists of a deep diffused P^+ anode 125 to 140 microns deep, an intrinsic material layer and a shallow (15 microns), low resistivity N^+ cathode cap. The diffused anode and low resistivity cathode aid in reducing the diode's double injection forward bias voltage drop. The thick intrinsic layer is required to sustain high voltage reverse biases.

A hexagonal geometry is employed in order to reduce the forward voltage drop by reducing the current density. This geometry maximizes the use of the circular area of the DO-5 package while allowing the wafer to be diced easily and by conventional means. See Figure 1.

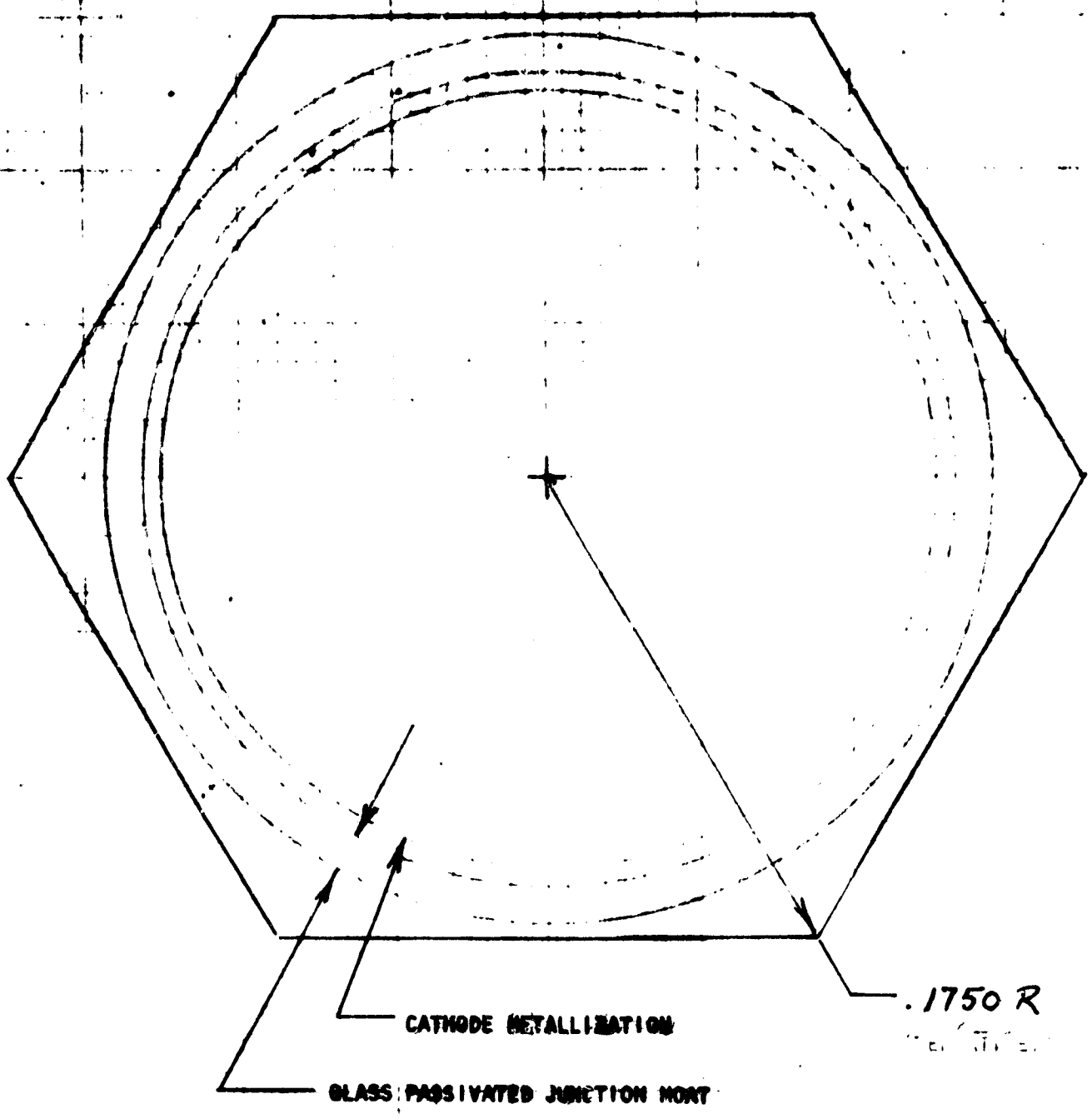

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FIGURE 1

3.2 Voltage Design

The requirement that the device endure a peak non-repetitive reverse voltage of 1.25 times the blocking voltage of 1000 volts or 1250 volts without undergoing bulk breakdown will be met by using 35 ohm-cm starting (intrinsic) material. Figure 2, taken from Reference 1, indicates 35 ohm-cm silicon, with a donor concentration of 1.5×10^{14} atoms/cc, will allow a reverse voltage of between 1600 and 1700 volts when the junction is 140 microns deep, which is the case with this device.

For a diffused (graded) junction, the required depletion region thickness is given by the following formula:

$$(1) \qquad d = (12\, K\varepsilon_o V_{BD}/qa)^{1/3}$$

where a = the grade constant of a diffused junction

$$= \frac{N_D}{X_J} \ln\left(\frac{P_o}{N_D}\right) = 12.88/\mu^4$$

X_J = the junction depth = 140 microns

P_o = the diffused surface concentration = 2.5×10^{19} atoms/cc

d = total depletion layer thickness

ε_o = permittivity of free space = $55.4 \frac{\text{electron charges}}{\text{volt-micron}}$

K = dielectric constant of silicon = 12

q = electron charge = 1.6×10^{19} coulombs

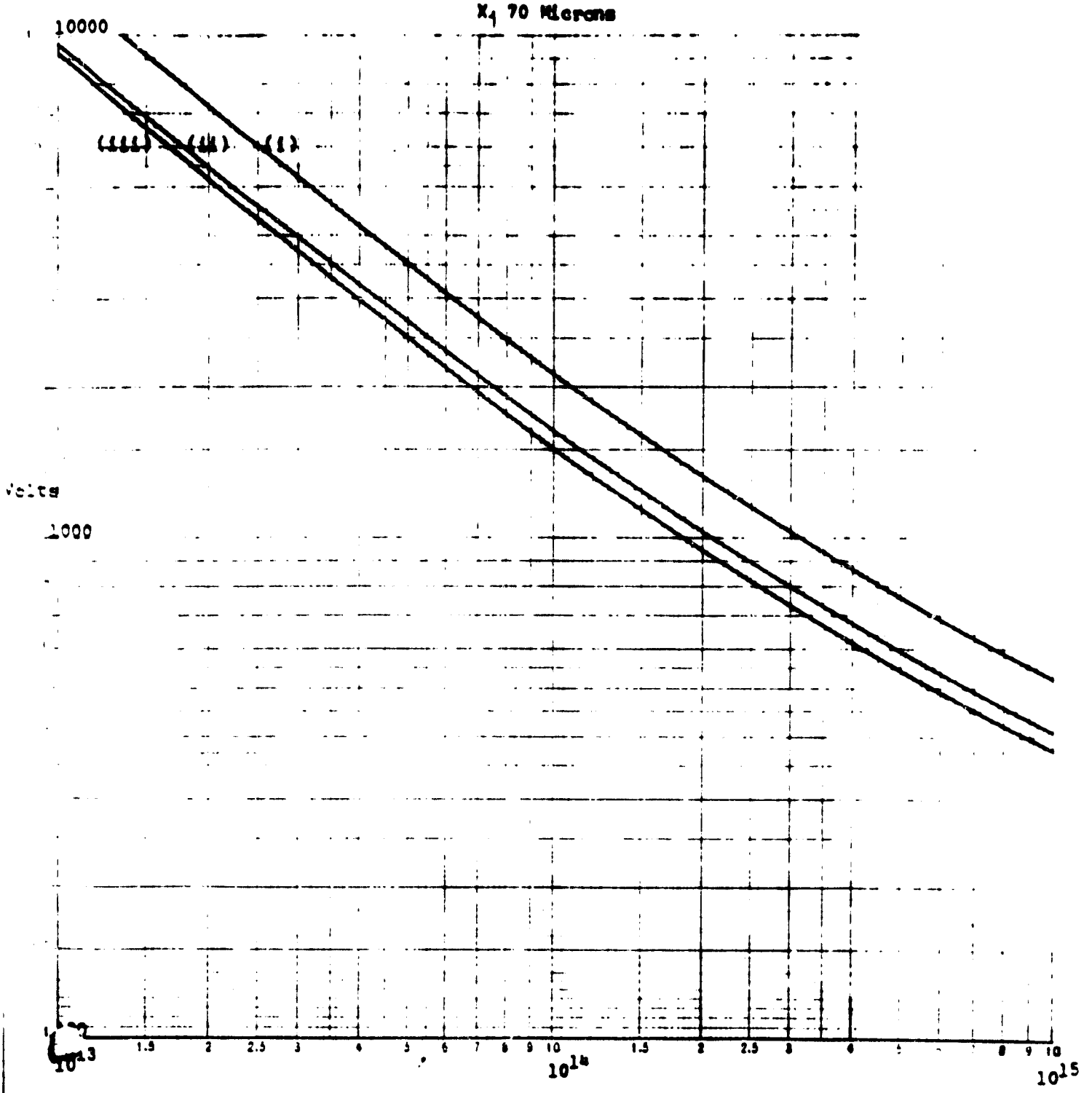
N_D = density of donor atoms in 35 ohm-cm N-type silicon

= 1.5×10^{14} atoms/cc

and V_{BD} = the breakdown voltage = 1250 volts

(i) Meserlian
(ii) Moll & Van Overstraeten
(iii) Lee etal

FIGURE 2
Avalanche Breakdown
Surface Concentration 10^{19}
X_j 70 Microns



The calculation of the depletion layer yields a thickness of 92 microns. The region depleted of carriers lies partly in the P^+ layer and partly in the intrinsic layer.

Our initial estimate of 106 microns was found from the expression for the required width of a step (non-graded) junction:

$$d = (2K\varepsilon_o V_{BD} / qN_D)^{1/2} \qquad (2)$$

This provided a good estimate, later revised as data (Table 1) indicated that this width was too large.

Table 1

V_{BD} Versus Intrinsic Thickness

Lot No.	Intrinsic Thickness (microns)	V_{BD} (volts)
001	43 - 56	1000
002	56 - 58	1100
006	74 - 86	1140
007	74 - 86	1090
008	76 - 81	1175
009	81 - 89	1290

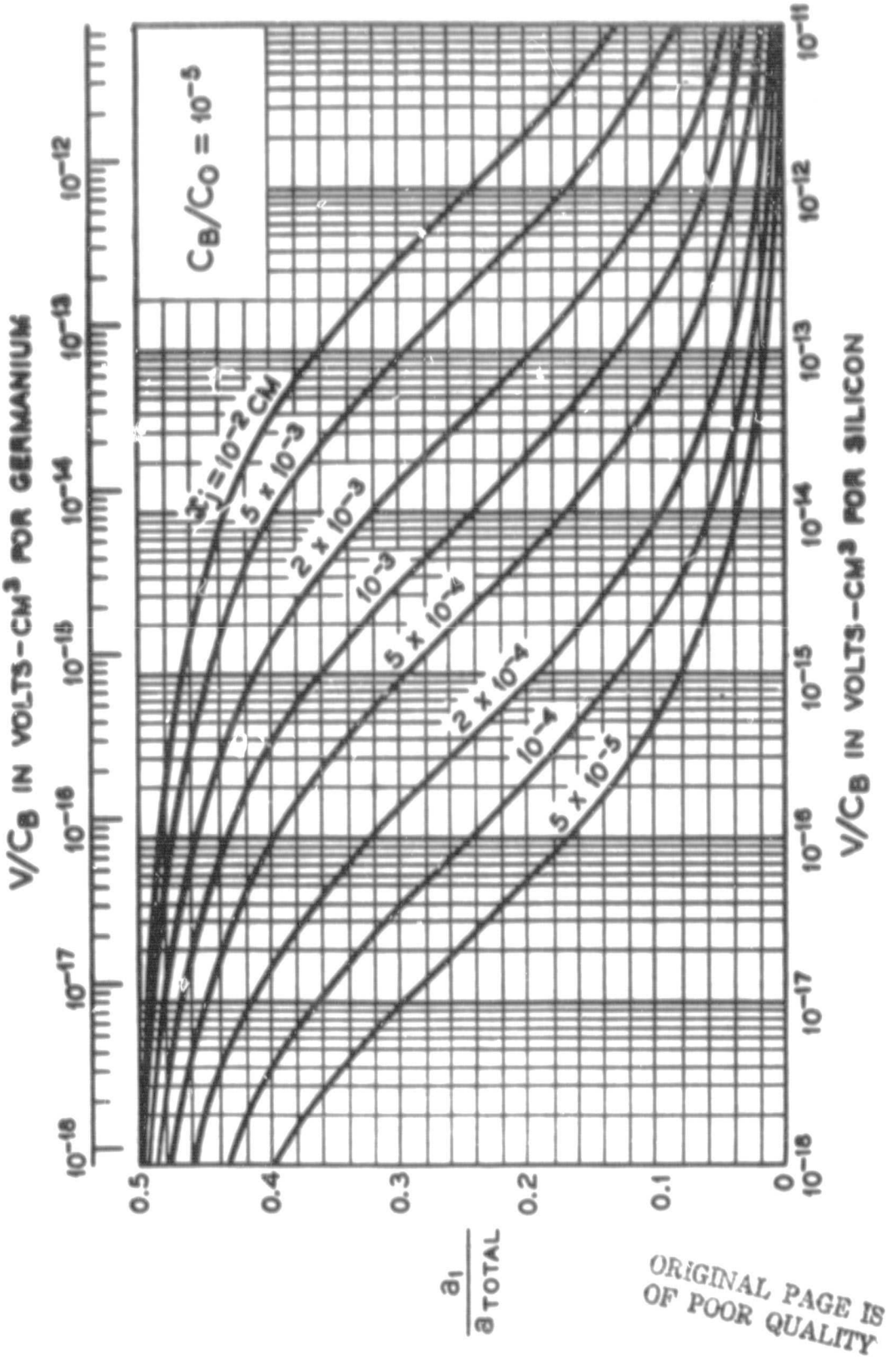


Fig. 29 — Chart for use in range 3×10^{-4} to 3×10^{-4}, gaussian distribution.

Figure 3 Breakdown voltage curves

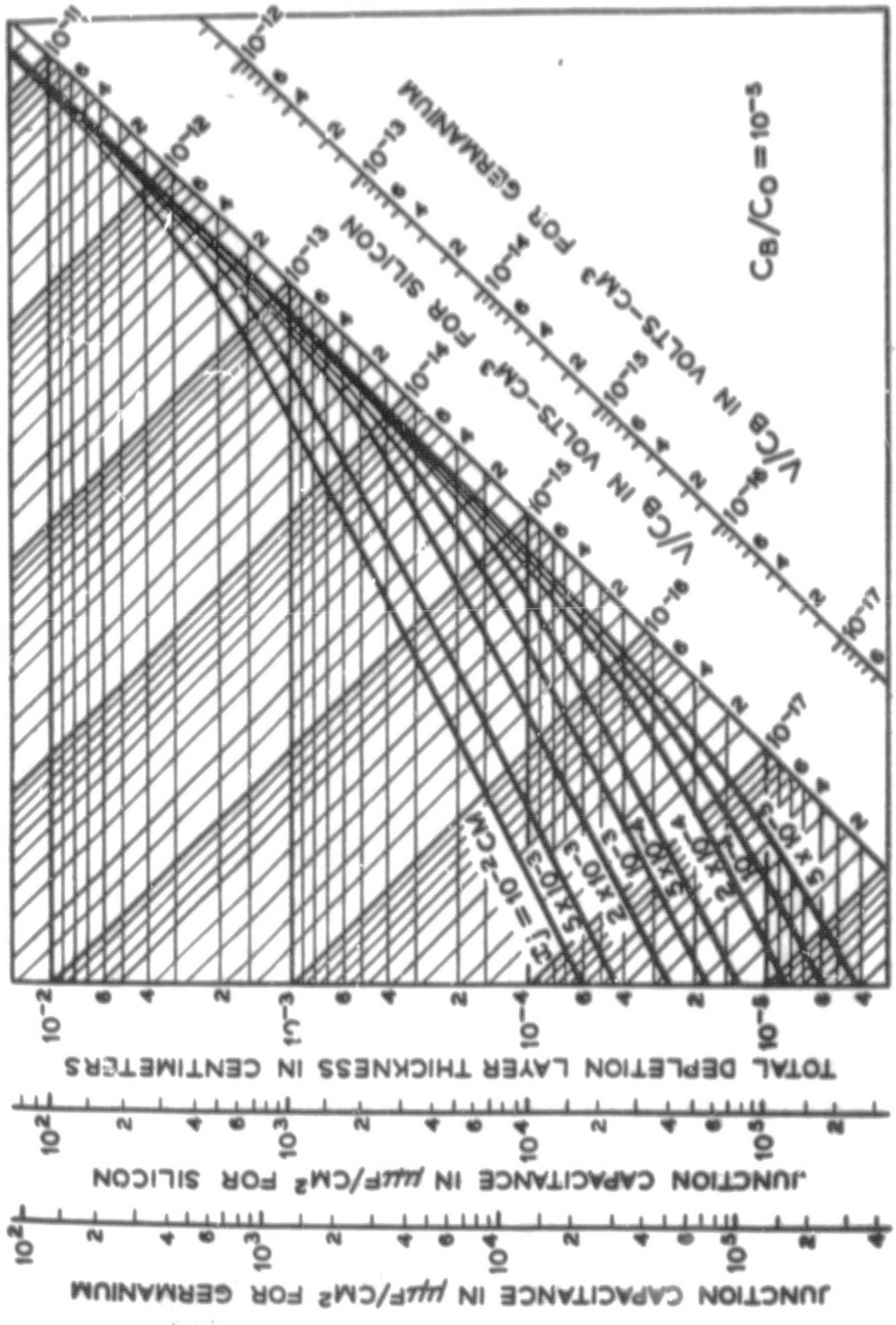


Fig. 21 — Chart for use in range 3×10^{-4} to 3×10^{-3}, gaussian distribution.

Figure 4 Depletion layer thickness curves

Figures 3 and 4, from reference 2, indicate that for a junction depth of 140 microns and surface concentration of 2.5×10^{19} atoms/cc, 15% of the depletion region lies in the P^+ layer and the intrinsic layer should be at least 85% of 92 microns or 78 microns thick to block 1250 volts.

Table 1 shows the average breakdown voltage and intrinsic layer thickness for several diffusion lots produced for this contract

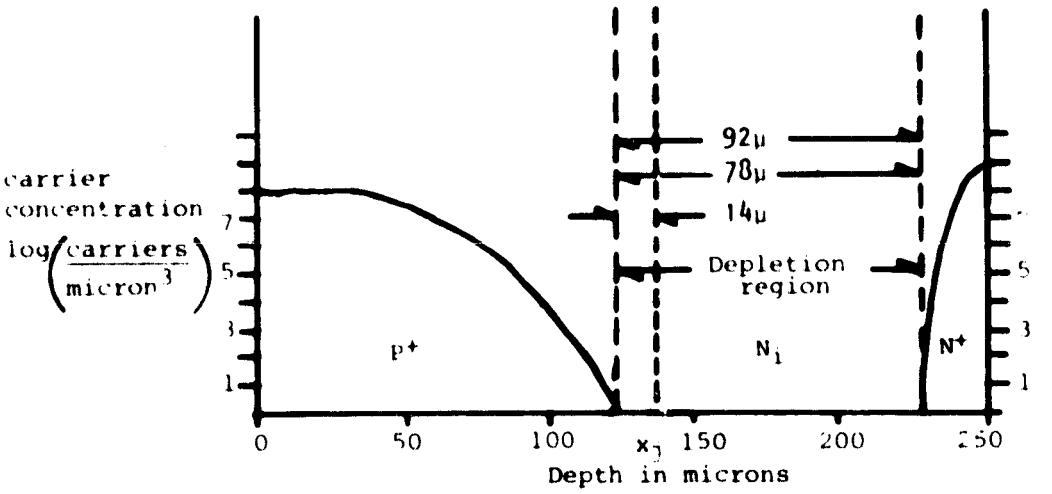
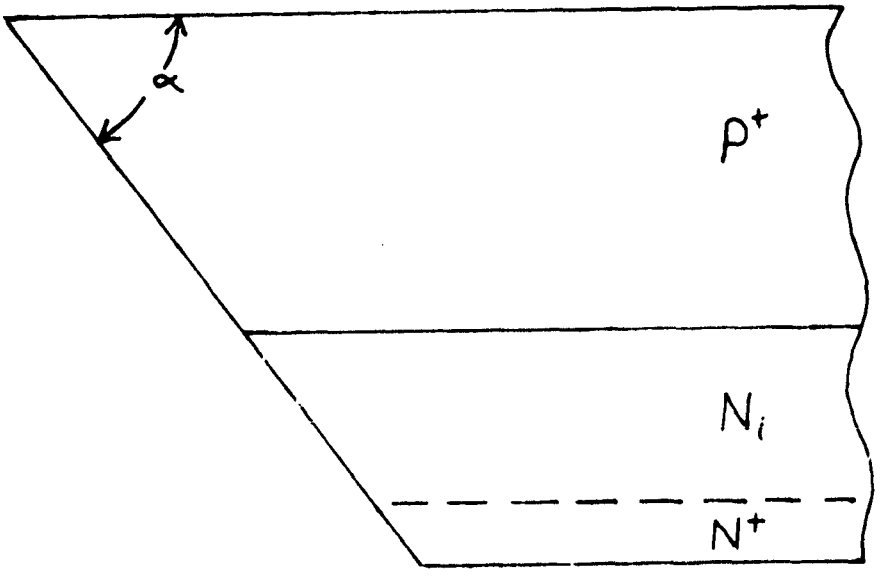


Figure 5 Depletion layer diagram

Equation (1) assumes device failure will occur due to avalanche breakdown within the bulk of the device. However, the use of a standard straight wall mesa would limit the voltage breakdown to 800 to 900 volts as the device will fail at the edge of the junction due to the higher field there. Therefore, the positive beveled mesa structure in Figure 6 is mandatory for our high voltage requirement. A planar device in Figure 7, produced by P diffusion in an N-



α = bevel angle

P^+-N_i-N^+ Junction with a Positive Bevel

Figure 6

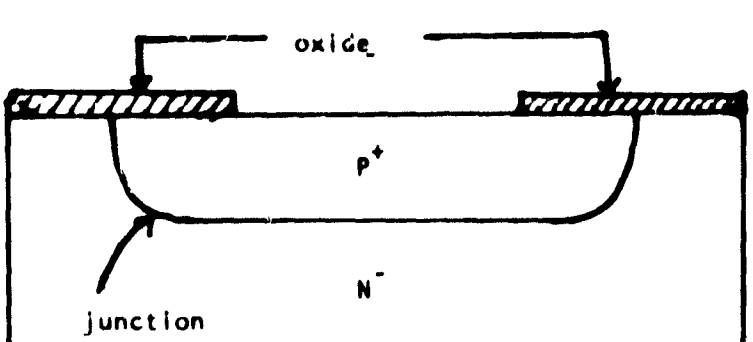


Figure 7 Planar structure junction

starting material has such concentration of the electric field (during reverse bias) at the corners that typically 30% of the blocking voltage is lost at 1000 volts. The structure in Figure 6 has a positive bevel on the edge as measured from N- to P^+. This is produced by groove etching from the intrinsic side. This positive bevel assures that the avalanche breakdown voltage will be the maximum allowed by the starting resistivity and diffusion profile, i.e., it will occur inside the device and not on the edge. This is shown by the following brief analysis. See Reference 3.

Avalanche breakdown occurs in a diffused junction when the applied voltage raises the internal electric field in the device to the critical field (E_c), the maximum value that can be sustained in silicon (approximately 30 volts/micron) before releasing electrons from the next lowest valence level. The field arises due to carrier migration in the N and P regions towards the + and - electrodes respectively, which leaves a charged region behind to block conduction across the junction. The charged region

will follow the doping profiles away from the junction until E_c is reached.

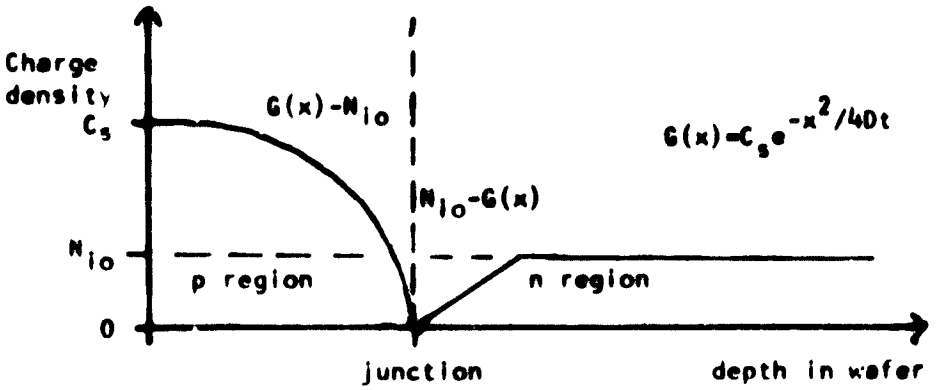


Figure 8 Charge density profile

The total charge on either side of the junction is the same, however, since the highest charge density occurs on the P side due to the steepness of the diffusion profile (Figure 8) this region will predominate at E_{max}. The local field is determined by integrating the charge density divided by the distance squared. See Figure 9.

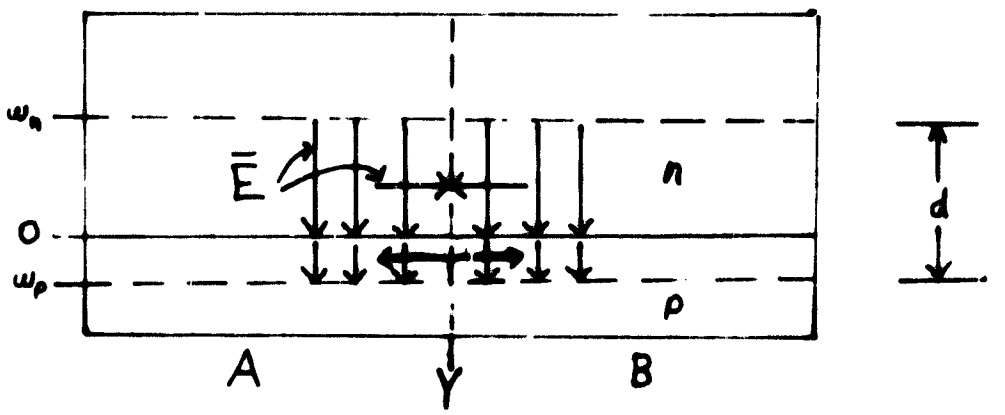


Figure 9 Electric field diagram I

Considering a point Y far from the edge, by lateral symmetry the normal field (E_n) is composed of equal contributions from both regions A and B. If the point Y is moved to the edge, or region B removed, the normal field should be half of the applied field (E_o), $E_n = E_o/2$. See Figure 10.

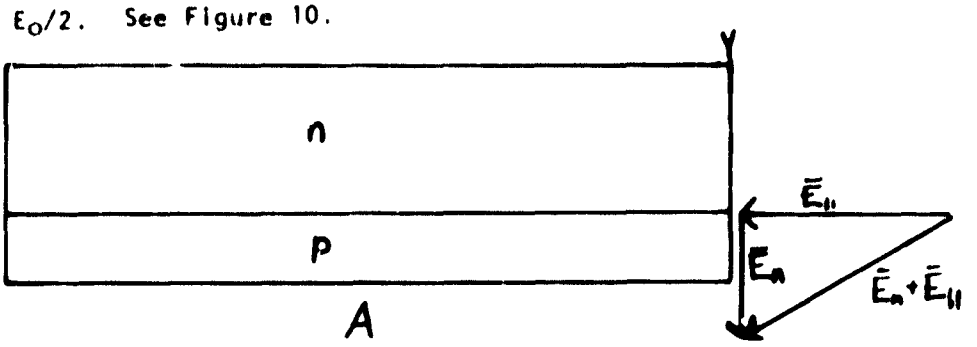


Figure 10 Electric field diagram II

Since region B is gone, there exists a laterally unbalanced parallel field ($E_{\parallel}$) at the point Y also. (We are considering only the P region since the field gradient is much higher there.) Make two assumptions for simplicity; 1) the width of the field in the P region is small compared to the depletion layer width, and 2) the charge density in the P region is uniform in both the parallel and normal directions. Then by symmetry, $E_{\parallel} = E_o$ and $E_{\parallel} = 2E_n$. The vector sum is in a direction 60° to the normal and of magnitude $1.1 \times E_o$. Actually, since the charged P region is not uniform, the highest field sum will exceed this value and the angle will be somewhat greater. To assure a minimum field on the edge, the bevel, or edge angle of the moat, should be 60° to the junction, i.e.,

perpendicular to the field since edge passivation material (glass) will prevent current flowing through the air.

3.3 Reverse Recovery Time

The relations between the specified rate of decay of the current, dI_f/dt, the reverse recovery time, t_{rr}, and the carrier lifetime, τ, are given by solving

(3) $$Q_R = \tfrac{1}{2}(\tau^2 dI_f/dt)$$

where $Q_R = \int_0^{t_{rr}} i(t)dt$ is the recovery charge and the JEDEC test requires that $dI_f/dt = 25 \times 10^6$ amps/second while t_{rr} is specified to be 200×10^{-9} seconds. See Figure 11.

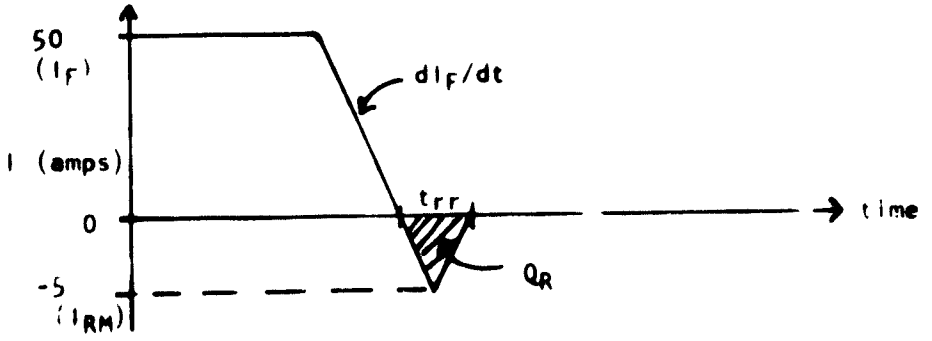


Figure 11 Reverse recovery time

(4) $$Q_R = \int_0^{t_{RR}} (dI_F/dt)\, t\, dt = \left(\frac{t_{rr}}{2}\right)^2 (dI_F/dt$$
$$= 5 \times 10^{-7} \text{ coulombs}$$

by (3) $$\tau = (2Q_R/dI_F/dt)^{\frac{1}{2}} = 2 \times 10^{-7} \text{ seconds}$$

is the required carrier lifetime.

It has been shown that high-energy radiation of silicon de.ices displaces silicon atoms from their normal lattice positions forming vacancies and interstitial defects. These defects act as recombination centers for electrons and holes with an energy within the forbidden range (gap) of silicon, which effect the lifetime of carriers in silicon.

The effect of electron radiation on the recombination of carriers is given by the following formula:

(5) $$R = R_O + K_T \emptyset$$

where R = the post-irradiation recombination rate, sec^{-1}

R_O = the pre-irradiation recombination rate, sec^{-1}

K_T = the carrier lifetime damage factor, cm^2/sec

and $\emptyset$ = the radiation dose, electrons/cm^2

Since the recombination rate is the inverse of the carrier lifetime, (5) may be stated as

(6) $$1/\tau = 1/\tau_O + K_t \emptyset$$

where τ = post-irradiation lifetime

and τ_O = initial lifetime

As the radiation dose, $\emptyset$, is increased, the initial lifetime, τ_O, becomes less important.

The following are the advantages of the high-energy radiation technique in controlling the lifetime of silicon diodes: 1) irradiation may be performed on dice alone, 2) there is approximately 80% less reverse leakage at 150°C than for a gold diffused diode with the same t_{rr} and 3) radiation provides a spatially homogeneous distribution of lifetimes throughout the diode. Radiation has proven to be the most controllable process for lifetime reduction.

Two sets of sixteen dice, each from lot NASA-007 were sent out for beta radiation. One set received 12 megarads and the other 16 megarads to provide data points from which to interpolate the correct radiation dose. (Tables 2 and 3) The results indicate that a radiation dose of 14 megarads may be routinely used. This dose produces devices with a high V_F and low t_{rr}. Adjusting the time and temperature of the reflow furnace used during the assembly in the DO-5 package allows the correct V_F to be achieved while retaining a satisfactory t_{rr}.

Device Number	V_F @ 50A (Volts)	V_R @ 500uA (Volts)	t_{rr} (Nanoseconds)
168	1.35	1300	250
169	1.33	1270	200
170	1.32	1120	250
171	1.24	1000	250
172	1.27	1260	225

Table 2 Forward voltage drop, blocking voltage and reverse recovery time of lot NASA-007 devices radiated with 12 megarads β radiation. (After packaging)

Device Number	V_F @ 50A (Volts)	V_R @ 500uA (Volts)	t_{rr} (Nanoseconds)
174	1.42	1260	175
175	1.38	1000	175
176	1.60	750	175
177	1.31	1240	175
178	1.25	1100	200

Table 3 Forward voltage drop, blocking voltage and reverse recovery time of lot NASA-007 devices radiated with 16 megarads β radiation. (After packaging)

3.4 Forward Voltage Drop

The voltage drop across the diode in the forward mode consists of five components: N^+-N junction, V_o, P^+-N_i junction, V_1, and the three regions (N^+, N_i, P^+) V_N, V_i, V_p. See Figure 12.

$$V_F = V_o + V_1 + V_N + V_i + V_p \tag{7}$$

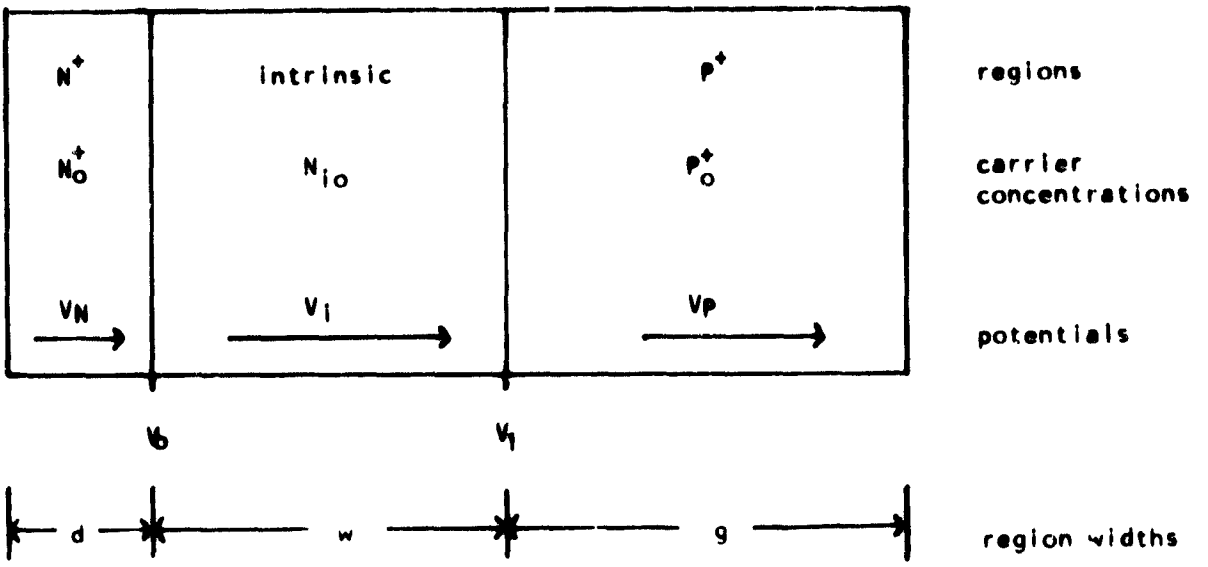


Figure 12 Forward voltage drop

The following analysis is similar to the one found in Reference (4). The symbols are defined as follows:

d = the width of the N^+ region = 25 microns

g = the width of the P^+ region = 137 microns

w = the width of the intrinsic region = 90 microns

q = the electron charge = 1.6×10^{-19} coulombs

D = the diffusion coefficient for holes and electrons at high carrier concentration, assumed equal = $6.5/cm^2 sec$

J = the forward current density = 125 amps/cm^2 @ 50 amps

N_{io} = the intrinsic carrier density = 1.5×10^{14} atoms/cc

N_o^+ = the thermal equilibrium carrier concentration of the N^+ region = 6.5×10^{19} atoms/cc

P_o^+ = the thermal equilibrium carrier concentration of the P^+ region = 1.44×10^{19} atoms/cc

$\theta = q/kT = 38.6$ volts $^{-1}$

τ = the carrier lifetime = 2×10^{-7} seconds

μ = the mobility of electrons and holes, assumed equal = $250/cm^2$sec volt

At the N^+ -N; region, the voltage drop is given by

(8) $$V_o = \frac{1}{2\theta} \ln (JdN_o^+/2N_{io}^+qD)$$

where (9) J_p = the hole current = $qDN_o^+\psi_o^2/d = J/2$

and (10) $$\psi_o^2 = \frac{N_{io}^2 e^{2\theta V_o}}{N_o^{+2}}$$ is the concentration imbalance coefficient for this region.

At the N_i -P^+ junction, the voltage is given by

(11) $$V_1 = \frac{1}{2\theta} \ln (JgP_o^+/2qDN_{io}^2)$$

where (12) J_n = the electron current = $qDP_o^+\psi_1^2/g = J/2$

and (13) $$\psi_1^2 = \frac{N_{io}^4 e^{2\theta V_1}}{P_o^{+2}N_o^{+2}}$$ is the concentration imbalance coefficient for the junction.

V_o and V_1 from (1) and (4) may be summed to give the total drop across the 2 regions, V_j:

(14) $$V_j = V_o + V_1 = \frac{1}{\theta} \ln (J (gdP_o^+N_o^+)^{\frac{1}{2}}/2qDN_{io}^2)$$

In our case the voltage across both junctions, $V_j = 0.542$ volts. The current through the N^+ region is

(15) $$J = 2q\mu N(x)E(x)$$

Integrating the electric field, E(x) yields V_N

$$(16)\quad V_N = \int_0^d E(x)dx = \int_0^d \frac{J\,dx}{2q\mu N_o^+} = 3.2 \times 10^{-5} \text{ volts.}$$

Similarly, the voltage drop through the p^+ region is

$$(17)\quad V_p = \int_0^g \frac{Jg}{2q\mu P_o^+} = 7.01 \times 10^{-3} \text{ volts.}$$

The voltage drop through the intrinsic region is again the integral of the electric field, which is a function of the carrier concentration, which varies through the region.

$$(18)\quad V_I = \frac{J}{2q\mu}\int_0^w \frac{dx}{N(x)}$$

There are 2 functions giving the concentration for each of the two sides of the intrinsic region. See Figure 13.

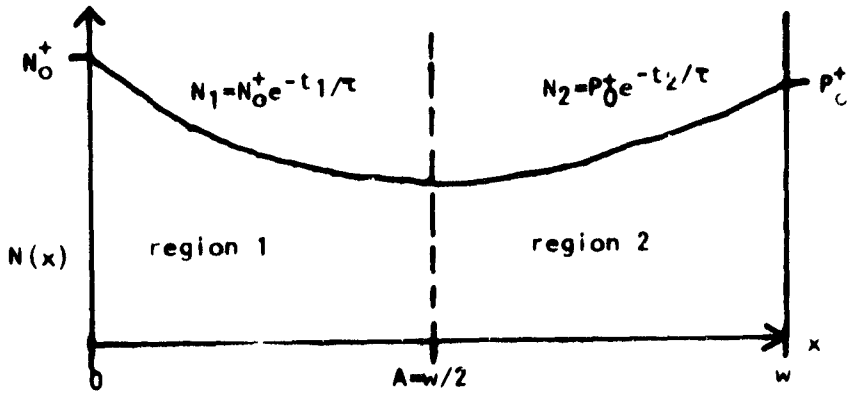


Figure 13 Intrinsic region

At point A, the concentrations given by the two functions are equal and so point A is the transition between the 2 functions.

In region 1,

(19) $N_1(t) = N_o^+ e^{-t_1/\tau}$ is the concentration of carriers on the N^+ side of the intrinsic region as a function of the carrier's time in the region, t_1, and the carrier lifetime, τ.

In region 2,

(20) $N_2(x) = P_o^+ e^{-t_2/\tau}$ is the concentration of carriers on the P^+ side of the intrinsic region as a function of the carrier's time in the region, t_2, and the carrier lifetime, τ.

which represent exponential decay of carriers from both sides.

The concentrations of holes and electrons are assumed equal in the intrinsic region. The time in the region, t, is given by the distance traveled, x, divided by the average velocity of the carriers, $\bar{v}$, $t_1 = x_1/\bar{v}$. The average velocity is the current divided by the concentration and carrier charge, $\bar{v} = J/gN_1(x)$. Therefore, in region 1, $t_1 = qx_1N_1(x)/J$ and by the same reasoning in region 2, $t_2 = qx_2N_2(x)/J$. x, is the distance from the N^+ boundary and so is just x, x_2 is the distance from the P^+ boundary given by (w-x). We have $t_1 = qxN_1(x)/J$ and $t_2 = q(w-x)N2(x)/J$.

These give

$$(21) \qquad N_1(x) = N_O^+ \exp(-qxN_1(x)/J\tau) \qquad \text{for } x < A$$

and $$(22) \qquad N_2(x) = P_0^+ \exp(-q(w-x)N_2(x)/J\tau) \qquad \text{for } x > A$$

These may be approximated by

$$(23) \qquad N_1(x) = N_O^+/(1+qN_O^+x/J\tau)$$

and $$(24) \qquad N_2(x) = P_o^+/(1-qP_o^+(x-w)/J\tau)$$

which, when placed in (18) and integrated, yield

$$(25) \quad V_j = \frac{J}{2q\mu}\int_o^w \frac{dx}{N(x)} = \frac{J}{2q\mu}\left(\int_o^A \frac{dx}{N_1(x)} + \int_A^w \frac{dx}{N_2(x)}\right)$$

$$= \frac{J}{2q\mu}\left(\frac{w}{2P_O^+} + \frac{w}{2N_O^+} + \frac{qw^2}{4J\tau}\left(1 + \frac{N_O^+}{P_O^+}\right)\right)$$

since $A = \frac{w}{2}$ to within a percent

therefore $V_j = 0.836$ volts and

$$V_F = 0.518 + 0.00006 + .00152 + 0.836 = 1.355 \text{ volts}$$

at $I_F = 50$ amps

This voltage is less than that measured across the assembled device at 50 amps which is typically 1.5 volts. The discrepancy may be accounted for by several factors. The ohmic contacts between the chip and the stud, the top contact and chip and the top contact and cap crimp may add 200-300 mv, while the lifetime reducing radiation tends to increase intrinsic resistivity 20-50% due to lattice damage. This increase is in addition to that caused by shortening the carrier lifetime, τ.

3.5 Trade-offs

The major electrical characteristics (forward voltage droo, blocking voltage and reverse recovery time) of this device are inter-dependent. Both the forward voltage drop and the blocking voltage are functions of the intrinsic layer thickness. The peak reverse voltage required determines this thickness and so its contribution to the forward voltage. A lower blocking voltage will give a device a lower forward voltage as seen from Table 1.

A critical trade-off exists between the forward voltage drop and the reverse recovery time. They are inversely coupled; as reverse recovery time decreases, forward voltage increases. The radiation that reduces lifetime disrupts the crystal lattice and so raises the forward voltage. Time spent at temperatures above the annealing temperature of silicon reverses this damage, thereby raising t_{rr} and lowering V_F. This trade-off was advantageous as devices initially too fast and with a V_F too large were reannealed to bring both parameters to acceptable levels.

A third trade-off exists between blocking voltage and t_{rr} since t_{rr} is a function of Q_R, the charge stored in the device after the forward current ceases. The thick intrinsic layer of high voltage devices holds much of this charge and therefore a lower voltage device with a thinner intrinsic layer will be faster than a higher voltage device, all else being the same.

4. WAFER PROCESSING

4.1 Diffusion and Lap & Polish

The $P^+/N^-/N^+$ device profile is formed on 35-40 ohm cm n-type neutron doped silicon material.

Using spin-on liquid boron source, P^+ layers are diffused simultaneously on both sides of the wafer. To achieve the required 5.4 mil junction depth, drive-in diffusion is performed at 1250°C for 264 hours.

The P^+ layer is removed from one side of the wafer by mechanical lapping, followed by chemical polishing to provide adequate surface finish for subsequent moat and cathode geometry formations. The intrinsic material thickness target is 4.5 mils, resulting in 9.9 mils thick wafers after lap and polish.

The N^+ cathode layer is diffused using $POCl_3$ source during one hour deposition at 1130°C, followed by drive-in diffusion targeted for 1 mil N^+ depth on 3.5 mil thick intrinsic N^- region. See Figure 14.

4.2 Positive Bevel Moat

By standard photoresist and masking techniques the moat geometry (Dgw. No. 100003-11, mask No. 2) is defined on the cathode side of the wafer. Silicon dioxide is removed from that area and approximately 5 mil deep moat is etched to form the positive

bevel junction. Figures 6 and 14.

4.3 Glass Passivation

High temperature glass, suspended in a binder, is deposited in the freshly etched and cleaned moat. In a two step furnace processing the binder is burned off and the glass is fired at 730°C and fused to the walls of the moat. To assure complete and continous glass passivation of the high voltage junction, the glass deposition and firing process is performed twice.

4.4 Metallization

A metallization process that is compatible with glass passivated junctions and provides solderable contacts to cathode and anode has been developed. These contacts have series voltage drops comparable to the standard aluminum and gold contact systems.

The new metallization is a tri-metal system, consisting of aluminum, titanium and nickel. The metals are evaporated in a high vacuum equipment. Aluminum is deposited first. A thin layer of titanium is flashed on the aluminum to act as a binder between the aluminum and nickel. A layer of nickel provides the solderable contact. The cathode contact areas are defined by standard photoresist and masking (Dwg. No. 100003-11, mask No. 3) techniques and selective etching. On the anode side of the wafer a continous metallization of the same system is deposited.

The contacts are sintered in a nonoxidizing ambient to establish low resistance ohmic contacts between the aluminum and silicon surfaces.

4.5 Wafer Test and Dicing

To complete the wafer processing, 100% wafer probing is performed to test for minimum acceptable blocking voltage.

The wafers are diamond saw cut into the hexagonal geometry dice, sorted for electrical and mechanical acceptance and delivered for assembly.

PROCESS SEQUENCE OUTLINE

1. STARTING MATERIAL WAFER NEUTRON DOPED N-TYPE SILICON

2. BORON DEPOSITION AND DRIVE IN DIFFUSION

3. SINGLE SIDE LAP & POLISH OXIDATION (ONE SIDE)

4. PHOSPHORUS DEPOSITION AND DRIVE-IN DIFFUSION

5. PHOTORESIST MASK, OXIDE AND MOAT FORMATION ETCH

6. HARD GLASS PASSIVATION IN THE MOAT

7. CONTACT PHOTORESIST AND OXIDE ETCH

8. ANODE AND CATHODE FOUR LAYER METALLIZATION

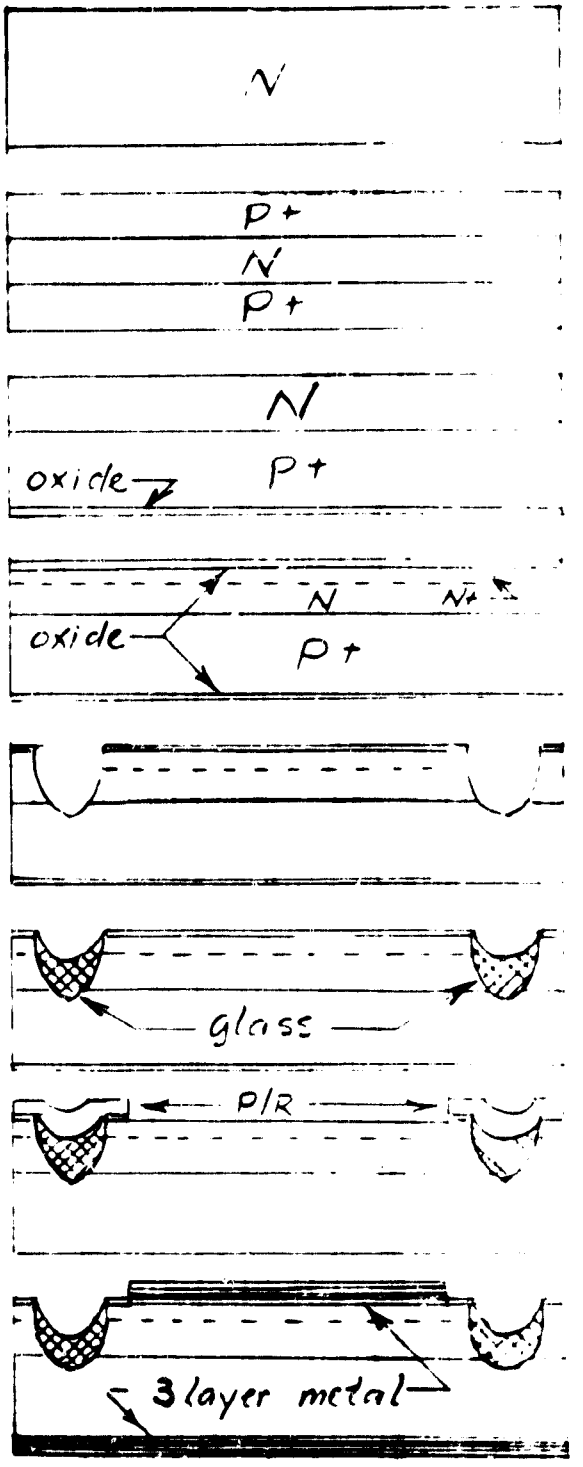


FIGURE 14

5. ENCAPSULATION

5.1 Package

The device is encapsulated in JEDEC standard DO-5 assembly, utilizing soft solder reflow process and hemetically sealed by resistance welded cap. The diode is assembled in the reverse polarity, i.e., DO-5 stud is the anode and the cap terminal is the cathode.

The specifications of the assembly componets are detailed in the following drawings:

DO-5 stud - Impex, 1404

DO-5 cap - 50-0016

Moly tab, cathode - 50-0003-4

Moly tab, anode - 50-0003-3

Internal lead - 50-0011

Solder preform, cathode - 50-0004-7

Solder preform, anode - 50-0004-6

5.2 Assembly

In one-pass solder reflow process the die is mounted on the nickel plated stud platform and the internal lead attached. For improved coefficient of expansion matching between the silicon material and copper electrodes, molybdenum back-up plates are

utilized. Indalloy preforms from Indium Corporation of America form the metallurgical bond between the nickel plated assembly componets. Figure 15.

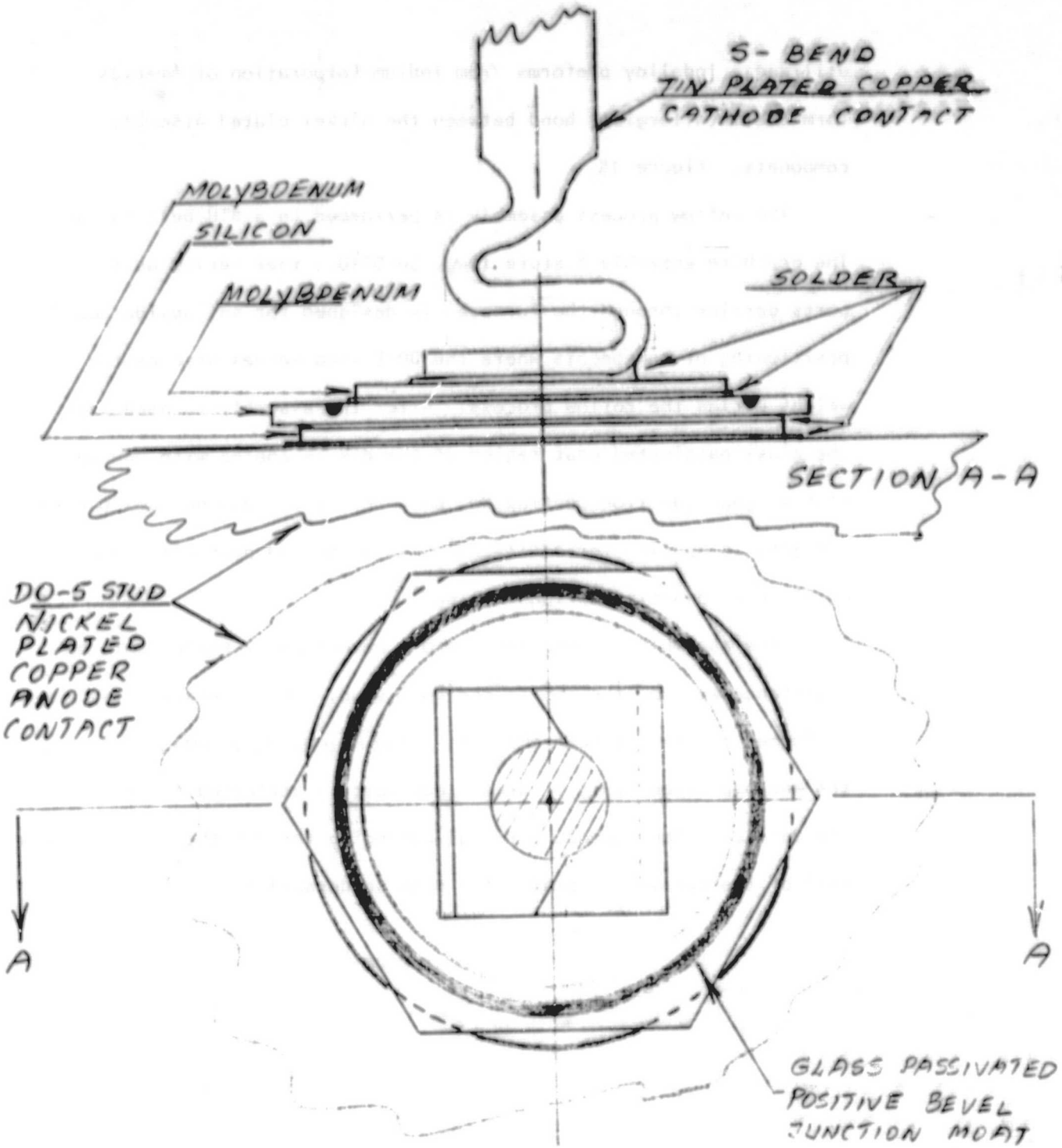
The reflow process assembly is performed in a BTU belt furnace. The graphite assembly fixture (Dwg. 50-0010), that serves as the parts carrier through the furnace, is designed for an "upside-down" positioning of components where the DO-5 stud serves also as the weight during the reflow process. After the assembly furnace pass, the glass passivated moat region of the die is coated with Dow Corning high voltage junction coating No. 643. Prior to capping, Dow Corning RTV 3140 is applied for additional insulation and protection against possible weld arcing during capping.

The assembly is completed into a hermetically sealed unit by resistance welding the cap to the DO-5 stud. This operation is performed in dry nitrogen ambient, achieving inert conditions inside the encapsulation cavity. Gross leak test is performed for 100% of the devices. The cathode terminal extending through the glass to metal seal of the cap is tin plated for good solderability.

SOLDER REFLOW ASSEMBLY

REVERSE POLARITY

DIODE



APPROXIMATE SCALE 10:1

FIG. 15

5.3 Polarity Trade-off

The initial proposal specified a normal polarity assembly, i.e., cathode mounted on the DO-5 stud and the cap terminal serving as the anode contact. (Figures 16 & 17) A large number of the assembled 1000-1400 volt units exhibited corona effect between the positive bevel moat region and the moly cathode back-up plate. The use of Dow Corning high voltage semiconductor junction coating No. 643 had only limited success because of the narrow access spacing between the surfaces to be isolated.

This problem could not be reliably eliminated without a major change in the DO-5 stud design; therefore, it was agreed that the contract be completed on time with the diode assembled in the reverse polarity, as shown in Figure 15 and described in the assembly process.

The DO-5 stud base that is proposed for the normal polarity assembly to be investigated, is available from the Nipert Company as P/N 068-8903-05. The pedestal of the cold formed copper stud with the brazed molybdenum back-up plate provides 0.060 inch clearance between the main body of the stud and the surface area of the silicon die extending over the pedestal. This clearance provides sufficient space for applying high voltage dielectric coating to the exposed surfaces of the silicon die and the cathode stud, thereby eliminating arcing. Figure 18.

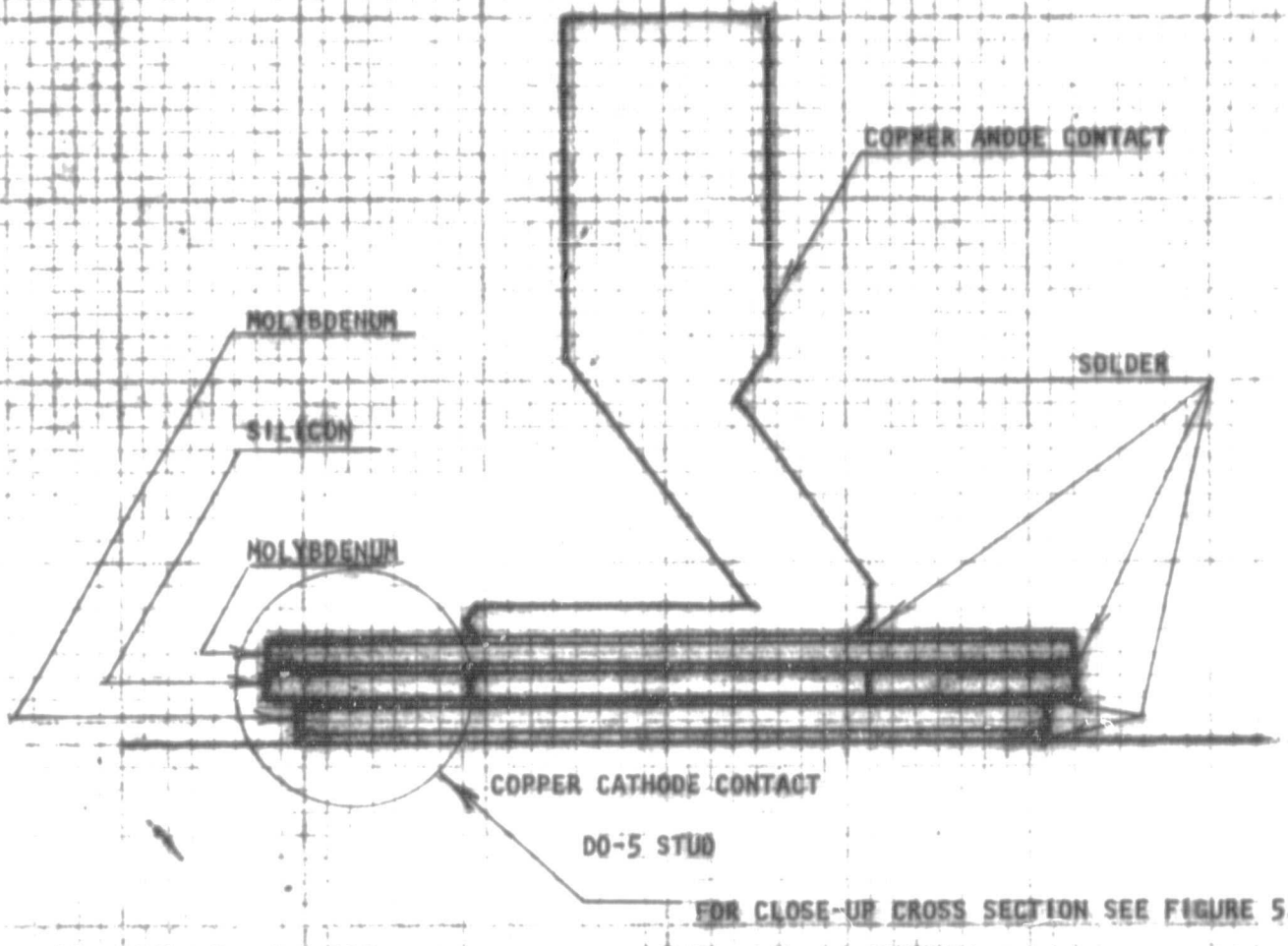
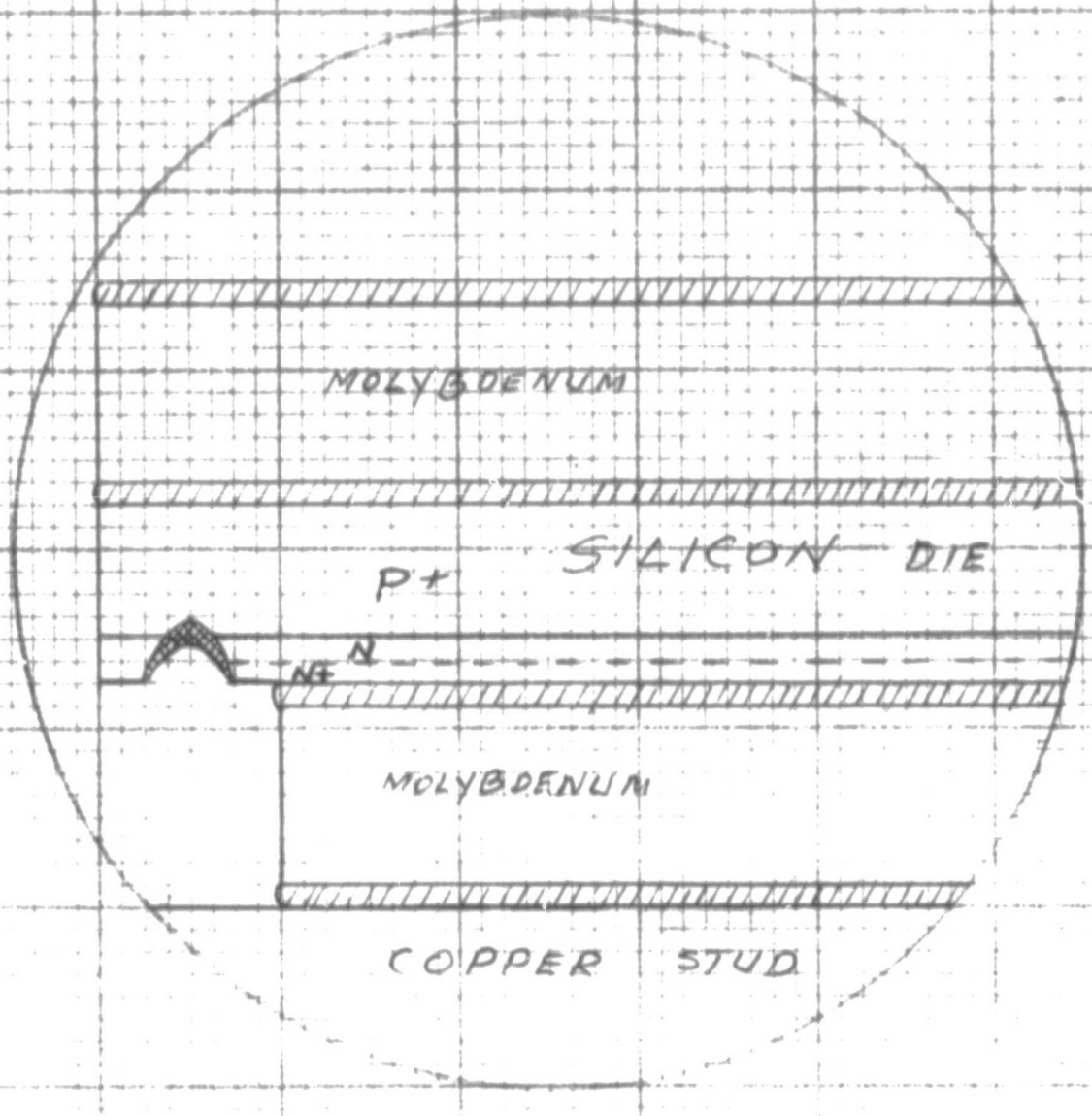


FIGURE 46

CLOSE-UP CROSS SECTION FROM FIGURE 16



HARD GLASS

SOLDER

FIGURE 37

NORMAL POLARITY ASSEMBLY
(MODIFIED VERSION)

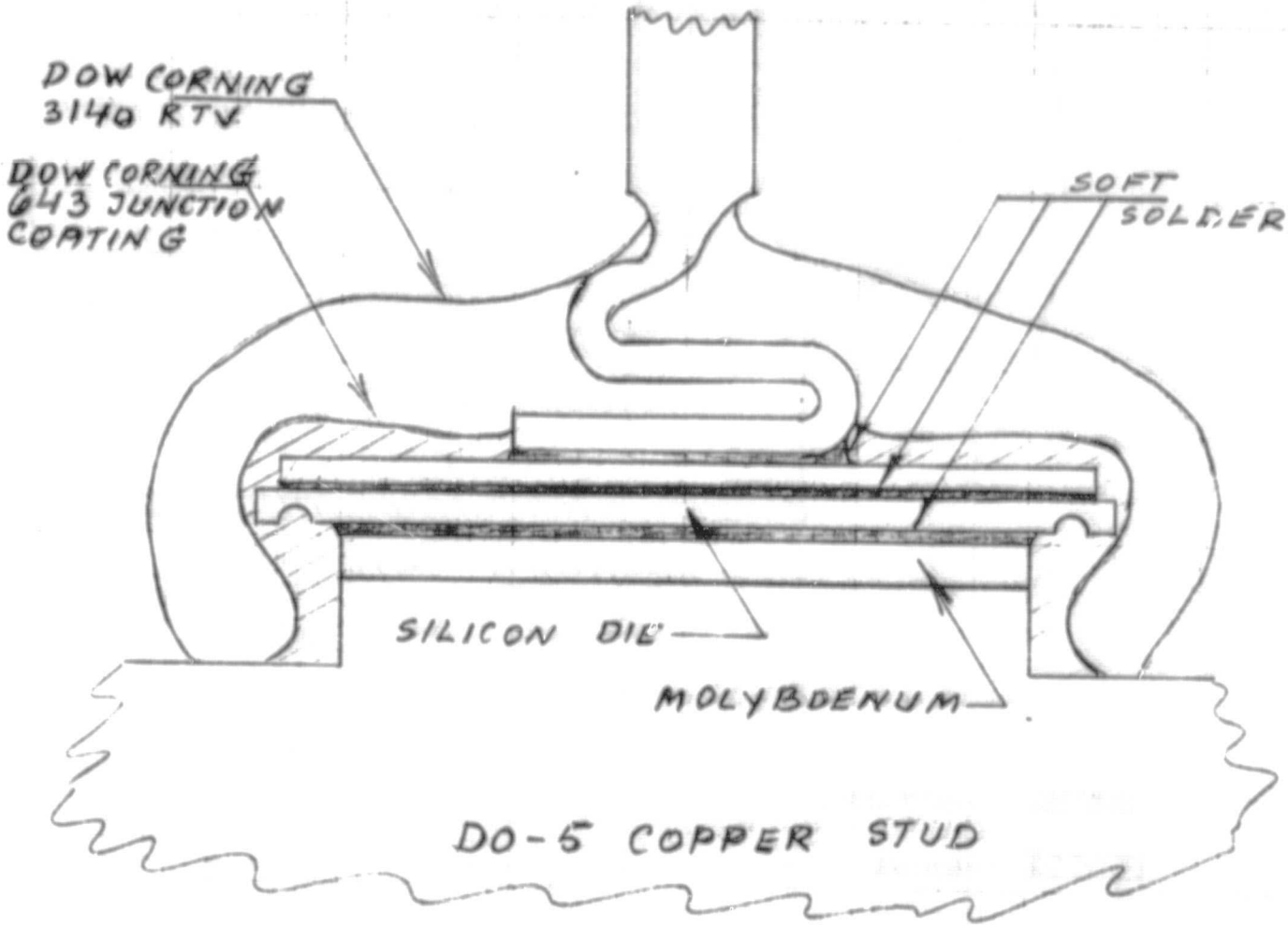


FIGURE 18.

5.4 High Voltage Cap

New DO-5 cap designed to comply with Underwiter's Laboratories specifications for high voltage devices has been designed (Dwg. No. 50-0017) and fabrication funded by Power Transistor Company. The standard DO-5 glass-to-metal seal is replaced by ceramic-to-metal assembly. This design provides insulation between the anode and the cathode of 0.625 inch minimum surface length in any direction.

5.5 Thermal Ratings

Junction temperature is determined by the total power dissapation in the device P_T, the ambient or case temperature T_C, and the thermal resistance θ_{JC} from junction to case.

$$T_J = T_C + \theta_{JC} P_T \tag{26}$$

The basic equation for the conduction of thermal energy is

$$Q = \frac{KA}{L} \Delta T = \frac{KA}{L} (T_1 - T_2) \tag{27}$$

where Q = heat flow/unit of time

K = thermal conductivity constant, W/cm, ^oC

A = area of thermal path, cm^2

L = length of thermal path, cm

T_1 = temperature of heat source, ^oC

T_2 = temperature of heat sink, ^oC

rewritten (27)

$$Q = \frac{T_1 - T_2}{L/KA} = \frac{T_1 - T_2}{\theta} \tag{28}$$

and

$$\theta = \frac{L}{KA} \tag{29}$$

The thermal spreading is taken into consideration by applying the following equation for circular geometry:

$$\theta_{circle} = \frac{L}{K \cdot (r^2 + rL)} \tag{30}$$

where r = radius of the circle

The equivalent diagram in Figure 19 shows the thermal conductive path considered and the calculated theoretical values of each thermal resistance element.

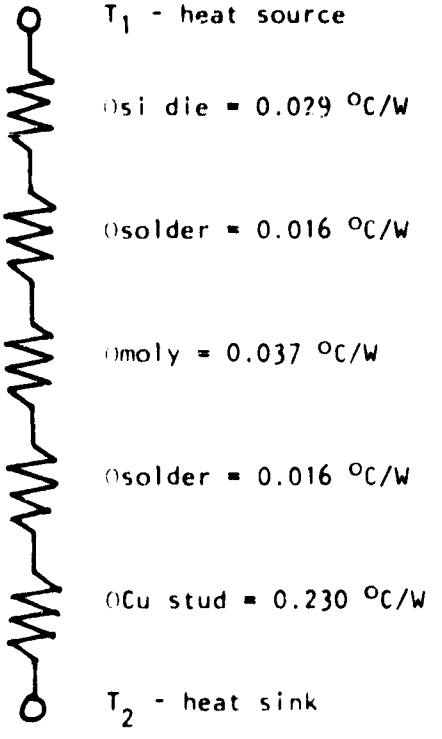


Figure 19 Thermal resistance, equivalent diagram

The resulting junction to case thermal resistance, O_{JC} is 0.33 °C/W

6. TEST

6.1 Test Plan

1. Expose all diodes to 1000A non-repetitive peak surge current
2. Screen on Mastech 216 automatic tester for
   a) I_R = 100 μA MAX. @ 1000v
   b) V_F = 1.51v MAX. @ 50A
3. Serialize and trademark
4. Read and record reverse recovery time at T_C = 100°C
5. Read and record forward voltage at I_F = 50A
6. Read and record DC blocking voltage at T_C = 25°C and T_C = 150°C
7. Read and record maximum reverse current at rated V_{RRM} and T_C = 25°C and T_C = 150°C
8. Select deliverable diodes that meet the "specifications"
9. Select samples and generate characteristic curves for
   a) capacitance versus reverse voltage
   b) forward voltage versus forward current
   c) reverse current versus reverse voltage as a function of temperature

The required specification read and record data of the deliverable diodes is tabulated in Table 4. The test equipment and procedures of the tests are discussed in the following paragraphs.

6.2 Non-Repetitive Peak Surge Current, I_{FSM}

As a potentially destructive test I_{FSM} has been performed to screen all devices prior to serializing and performing any other tests. All devices were exposed to 1100A half-cycle surge to insure compliance with the 1000A requirement.

The major components of the peak surge test equipment are: high current variac, SCR and SCR pulse firing circuit, transformer with a high current secondary, current sensing resistor, and oscilloscope, connected as shown in Figure 20.

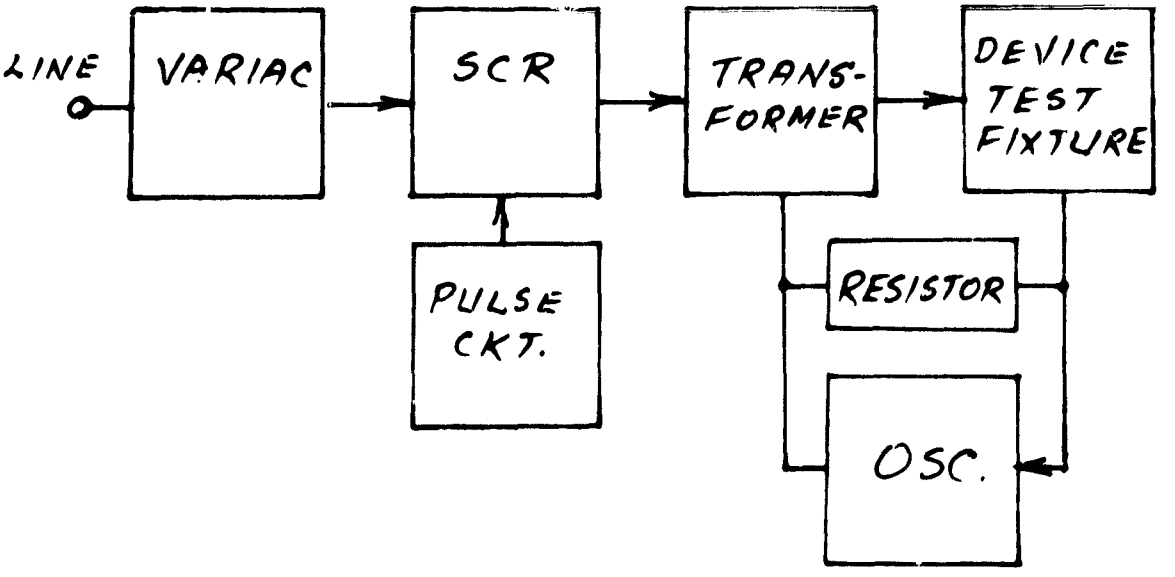


Figure 20

Test Circuit Block Diagram

The device under test is clamp-held in a safety test fixture, Figure 21, while a high current pulse, triggered by the SCR firing circuit, is applied. The amplitude of the current pulse is determined by observing the voltage pulse across the non-inductive one milliohm resistor in series with the diode, as displayed on the oscilloscope. Figure 22. The variac is adjusted for the required pulse amplitude.

Following the high current surge test, a survivor screening test was performed using Mastech 216 automatic tester. At room temperature the diodes were tested for

$$I_R = 100\ \mu A\ MAX\ @\ 1000\ volts$$

and $$V_F = 1.51v\ MAX\ @\ 50A$$

Units that passed the series of tests were serialized for the subsequent read and record tests.

6.3 Reverse Recovery Time, t_{rr}

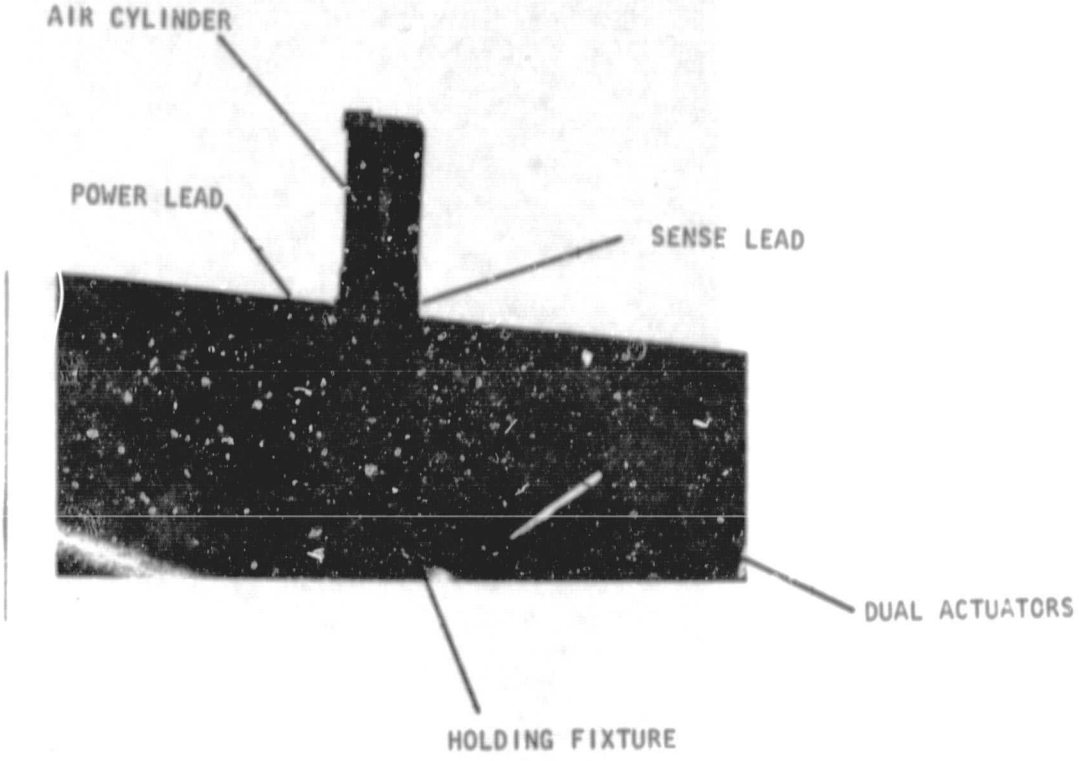
The reverse recovery test was performed in a JEDEC type test circuit.

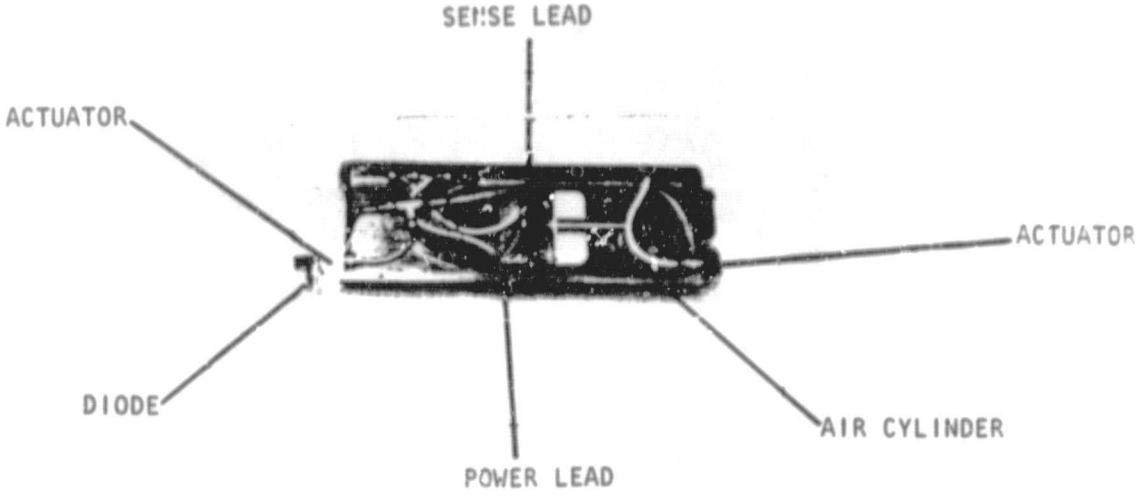
The current through the diode is reduced at a rate of 25A/sec. When the sign of the current through the diode changes, zero reference line is established. The measurement of the reverse recovery time is made from that point (t_o) to its maximum negative value (t_1) and to the approximate point where the reverse current has returned to 10% of its maximum value, I_{RM}(REC.). See Figure 23.

The diodes were stabilized at 100°C in an oven. Using the reverse recovery test circuit, set at I_{FM} = 50A and dI/dt = 25A/μsec.

DIODE TESTING FIXTURE

Figure 21





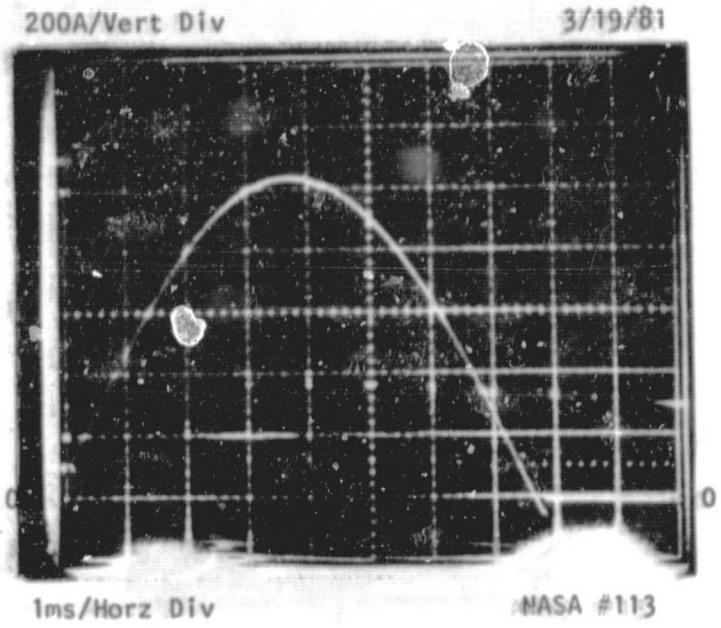


Figure 22 Peak surge current pulse

the t_{rr} was read on Tektronix 465 oscilloscope and recorded for each unit.

The t_{rr} test utilizes Tektronix CT5 high current transformer with P6021 current probe. During the performance and the evaluation of the test it was determined that the response limitations of the probe resulted in some loss of accuracy in the oscilloscope reading. Due to some saturation at 50A and even lower current levels the zero reference line is shifted slightly from the initial setting, causing an error in the reading. The upper limit of the probe frequency response rating ($20MH_Z$), reduces the accuracy of the time measurement during the very fast recovery from t_1 to t_2, Figure 23. At 20 MH_Z the period is 50ns, and the accuracy of reading the time during that segment of recovery is limited to about 100ns. Figure 24.

To eliminate the inaccuracy of this test, new test equipment is being designed to read the current in terms of a voltage directly across a non-inductive resistor in series with the diode under test.

To indicate the true performance of the device, two data points have been logged:

t_1 - the time from the sign change of the recovery current at t_o to its maximum negative value,

t_2 - the time from t_o to the approximate point where the reverse recovery current has returned to 10% of its maximum value. See Figures 23 and 24.

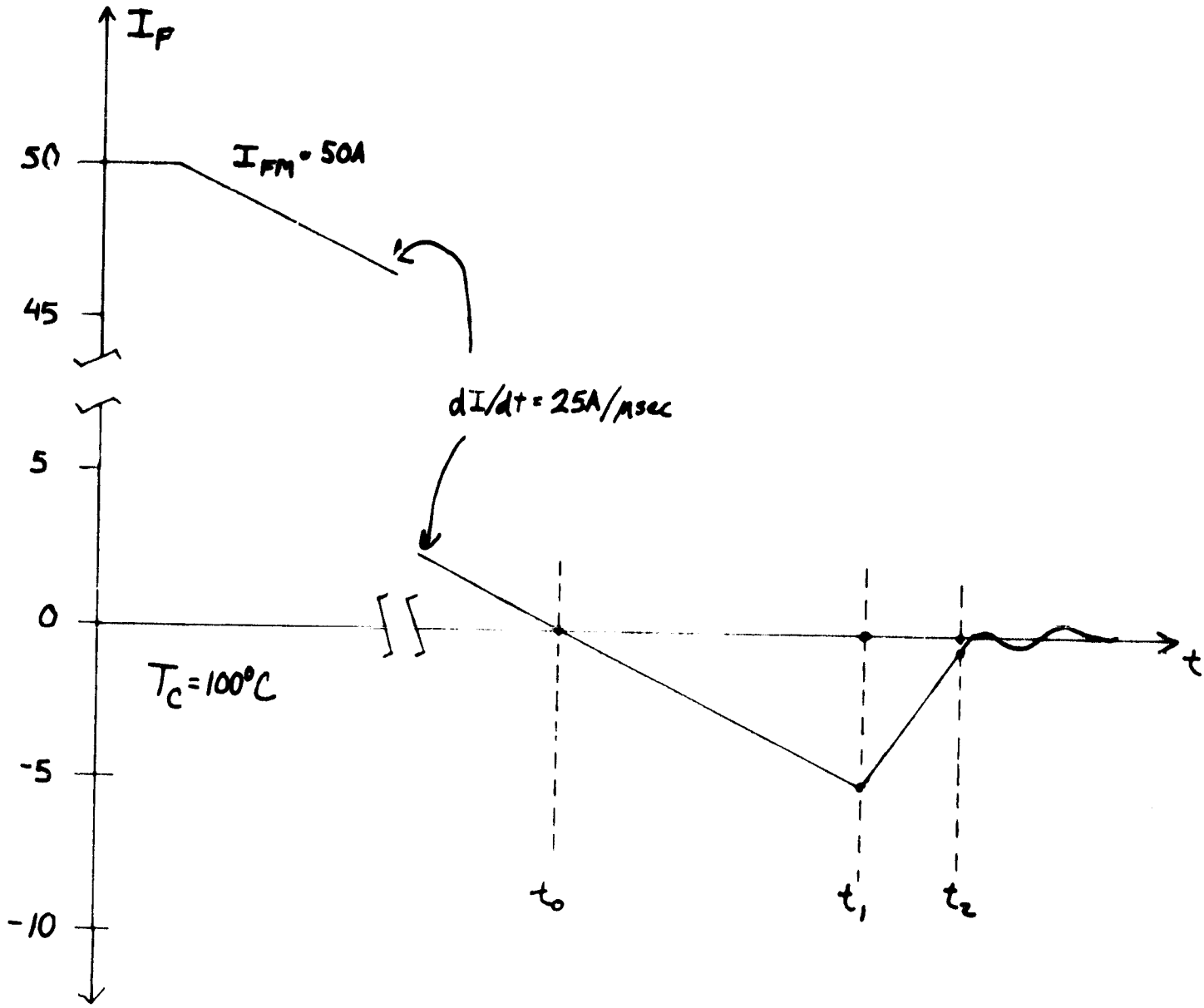
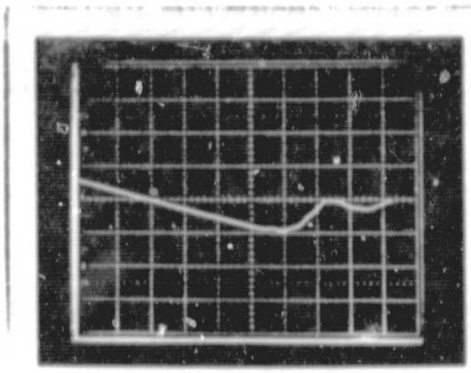
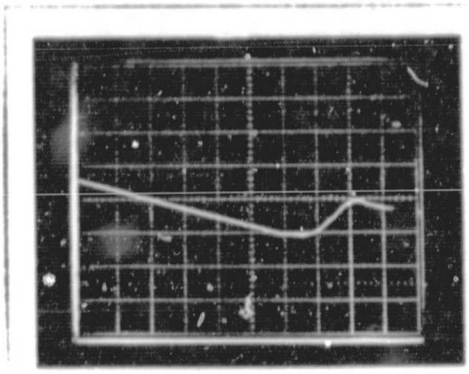


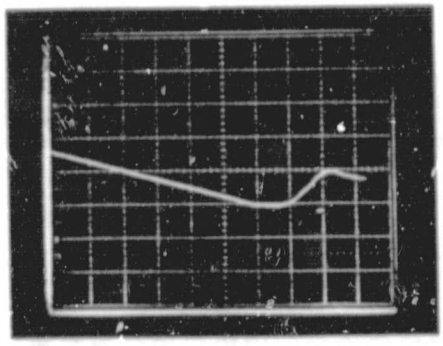
Figure 23 - Reverse recovery waveform



Device #031



Device #038



Device #060

Vertical Scale: 4A/div

Horizontal Scale: 50 nsec/div

Figure 24 Typical T_{rr} waveforms

Device No.	V_F @ 50A Volts	V_R @ 500μA T_C = 25°C Volts	V_R @ 5mA T_C @ 150°C Volts	I_R @ 1000V T_C = 25°C μA	I_R @ 150°C μA 800V	1000V	T_{rr} from 50A di/dt = 25A/μsec @ 100°C, t_1/t_2 nsec
002	1.49	1225	1350	2	350	450	325/500
010	1.40	1330	1280	3	300	350	400/500
012	1.39	1350	1260	2	250	300	400/500
013	1.32	1200	1280	2	150	200	400/500
014	1.50	1290	1300	3.5	450	500	300/425
019	1.46	1340	1380	1.5	1000	1200	325/450
020	1.44	1345	1180	6	1350	1600	350/450
024	1.30	1370	1280	1.5	750	800	500/600
026	1.44	1160	1285	2	700	900	325/425
027	1.41	1390	1180	5	1200	1350	400/500
029	1.48	1350	1300	2.5	750	900	300/400
033	1.46	1340	1260	2	1000	1250	300/400
036	1.48	1360	1410	4	900	1000	350/450
038	1.50	1330	1400	10	1000	1200	275/350
039	1.50	1225	1280	9	1100	1300	275/350
040	1.53	1320	1200	8	1300	1400	275/350
044	1.49	1160	1180	12	1000	1300	350/450
045	1.42	1315	1350	5	500	600	350/450
047	1.37	1195	1160	1.5	500	650	275/350
048	1.41	1300	1200	2	600	750	250/325
049	1.46	1215	1240	12	1100	1300	275/350
050	1.52	1190	1300	3	1000	1200	275/350
051	1.31	1160	1240	10	750	1000	350/400
052	1.48	1360	1350	2.5	900	1100	275/350
053	1.52	1340	1300	10	850	1000	250/350
054	1.51	1325	1340	7	700	900	250/325
056	1.44	1140	1265	2	700	900	250/300
058	1.42	1130	1200	8	1800	2500	250/300
059	1.38	1200	1260	6.5	2200	2500	275/350
060	1.42	1250	1280	6	1100	1400	275/350
061	1.45	1320	1350	2	700	850	280/340
062	1.54	1290	1260	5.5	2000	2300	325/400
066	1.37	1275	1330	4	700	900	280/340
067	1.45	1280	1380	3.5	1400	1700	325/400
068	1.42	1320	1340	2	850	1100	280/330

Table 4

Device No.	V_F @ 50A Volts	V_R @ 500μA T_C = 25°C Volts	V_R @ 5mA T_C @ 150°C Volts	I_R @ 1000V T_C = 25°C μA	I_R @ 150°C μA 800V	1000V	T_{rr} from 50A di/dt = 25A/μsec @ 100°C, t_1/t_2 nsec
069	1.39	1310	1200	6	2200	2500	300/400
070	1.50	1295	1320	7	1500	2000	300/400
071	1.48	1290	1350	1.5	550	650	250/300
072	1.49	1340	1300	4	1400	1700	275/325
074	1.43	1315	1275	11	1500	1800	260/325
075	1.49	1210	1360	5	1000	1250	275/325
077	1.45	1340	1300	3	800	1000	275/325
078	1.48	1295	1320	8	1600	2000	275/325
079	1.53	1250	1370	5	900	1100	275/350
080	1.43	1330	1280	4	850	1100	250/310
081	1.48	1370	1400	4	600	800	300/450
083	1.50	1340	1400	7	900	1100	300/400
086	1.49	1440	1310	45	1600	1900	275/350
087	1.46	1440	1420	12	1350	1600	325/450
088	1.47	1200	1330	1.5	300	400	300/400
089	1.43	1330	1320	10	1450	1800	300/400
092	1.46	1230	1340	2.5	500	600	275/400
094	1.50	1330	1300	6.5	1400	1750	250/350
096	1.36	1265	1360	20	500	600	350/500

Table 4 (cont'd)

6.4 Forward Voltage, V_{FM}

The Mastech 216, using the digital readout option, was employed to read and record the forward voltage drop at I_F = 50A. A typical V_{FM} characteristic trace is shown in Figure 25, as displayed on the Tektronix 576 curve tracer.

6.5 DC Blocking Voltage, V_R

The blocking voltage at 25°C , 500 μA and at 150°C, 5 mA was read on Tektronix 576 curve tracer.

6.6 Reverse Current, I_R

Utilizing Tektronix 576 curve tracer in the Leakage Mode, the reverse leakage current was recorded for V_R = 100 volts at T_C = 25°C and for V_R = 800 volts and 1000 volts at T_L = 150°C.

All high temperature characteristics were read and recorded with the devices heated in an oven and stablized at the required elevated temperature.

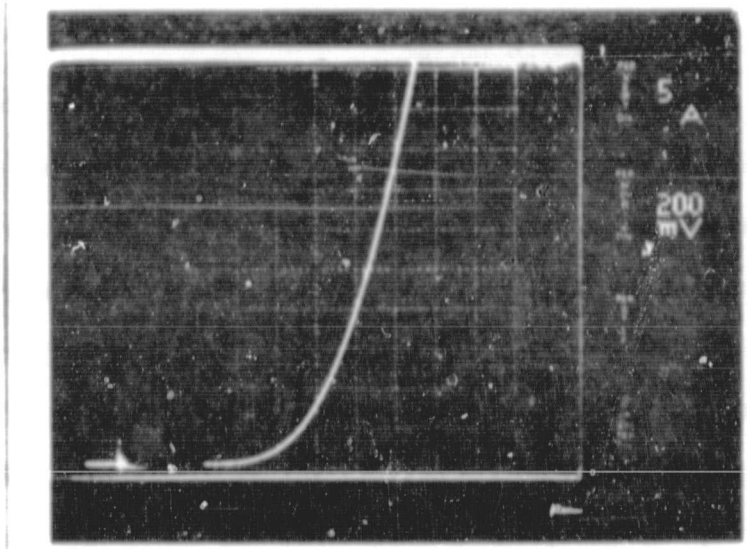


Figure 25

Forward Voltage, V_{FM}

7. ELECTRICAL PERFORMANCE

7.1 Characteristic Curves

Five devices, numbers 031, 038, 039, 046 and 060 were chosen as typical of the lot and three characteristic curves were generated for each device; forward voltage drop versus forward current (Figures 26-30), reverse leakage current versus reverse voltage at six temperatures (Figures 31-35), average leakage current versus temperature of the five units (Figure 36), and capacitance versus reverse voltage (Figures 37-41).

V_F versus I_F was plotted from 100 mA to 100A using the Mastech. V_F for I_F of 100, 200, 300 and 500 amps was found by adjusting the surge current tester to deliver a peak current of the correct value and then displaying the voltage across the device on an oscilloscope. The voltage at 100A was higher when measured with the surge tester than when measured by the Mastech. This implies that the higher current level voltages are offset. The affect was determined to be caused by ohmic drops through the sense wires of the surge test fixture. Therefore, the high current data points have been normalized based on the offset at 100A. Curves have been drawn through both the normalized and the measured points. The actual curves lies between these curves.

The leakage current versus reverse voltage curves were generated by heating the diodes in an oven, stabilizing and then measuring the leakage at 200, 400, 600, 800 and 1000 volts on a 576 curve tracer. The curves that result are straight lines on a semi-log graph whose slopes are independent of temperature. By plotting the average leakage current of the devices at 800 volts against temperature on a semi-log graph, a straight line results which indicates the leakage increases exponentially with temperature (Figure 11).

Capacitance was plotted against reverse voltage by using a Boonton model 72BD capacitance meter and a Hyland high voltage power supply. The resulting curve is a straight line on logarithmic graph paper. The capacitance plot was terminated at 600 volts due to the maximum limitations of the test equipment.

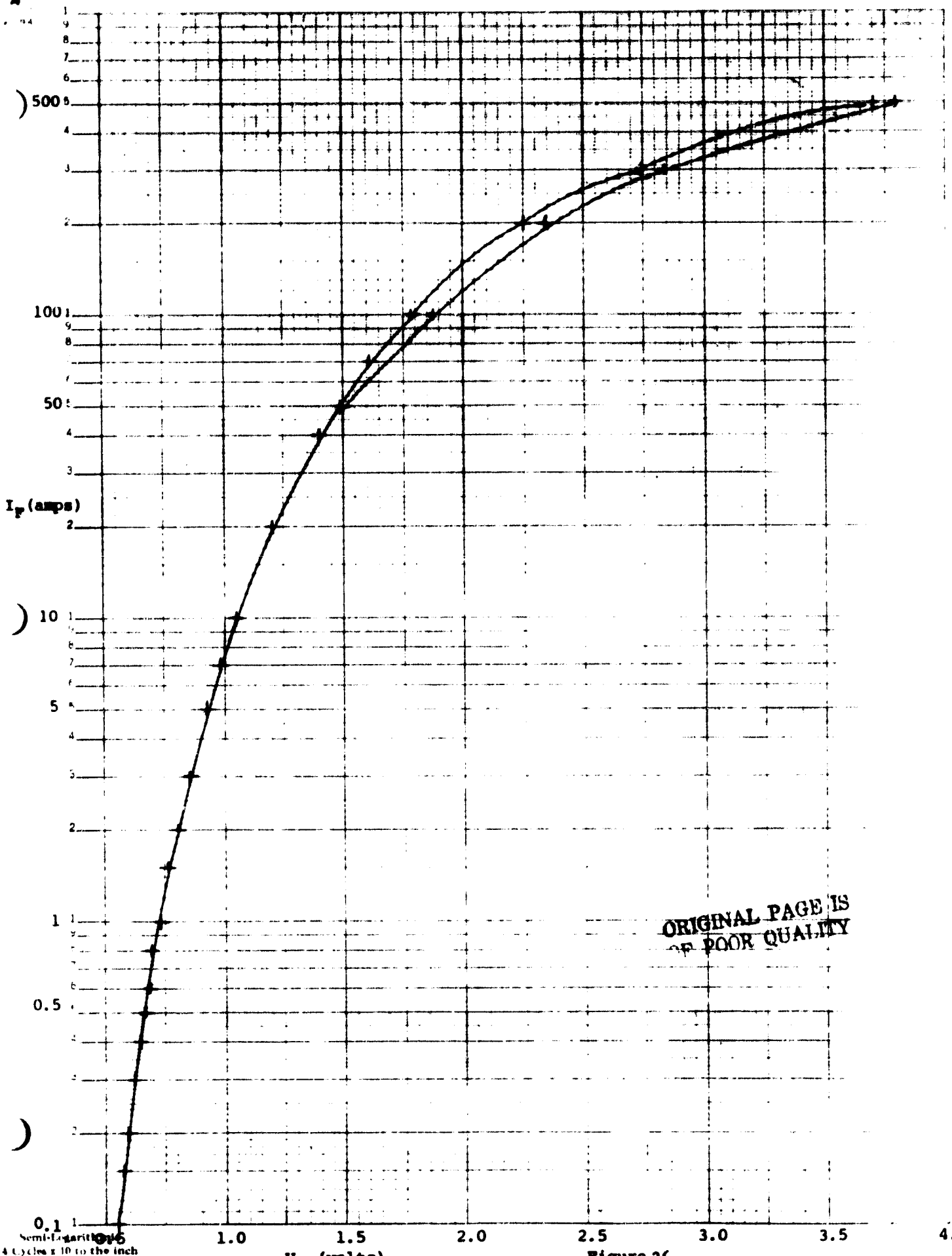


Figure 26

Device #038 Forward characteristic curve

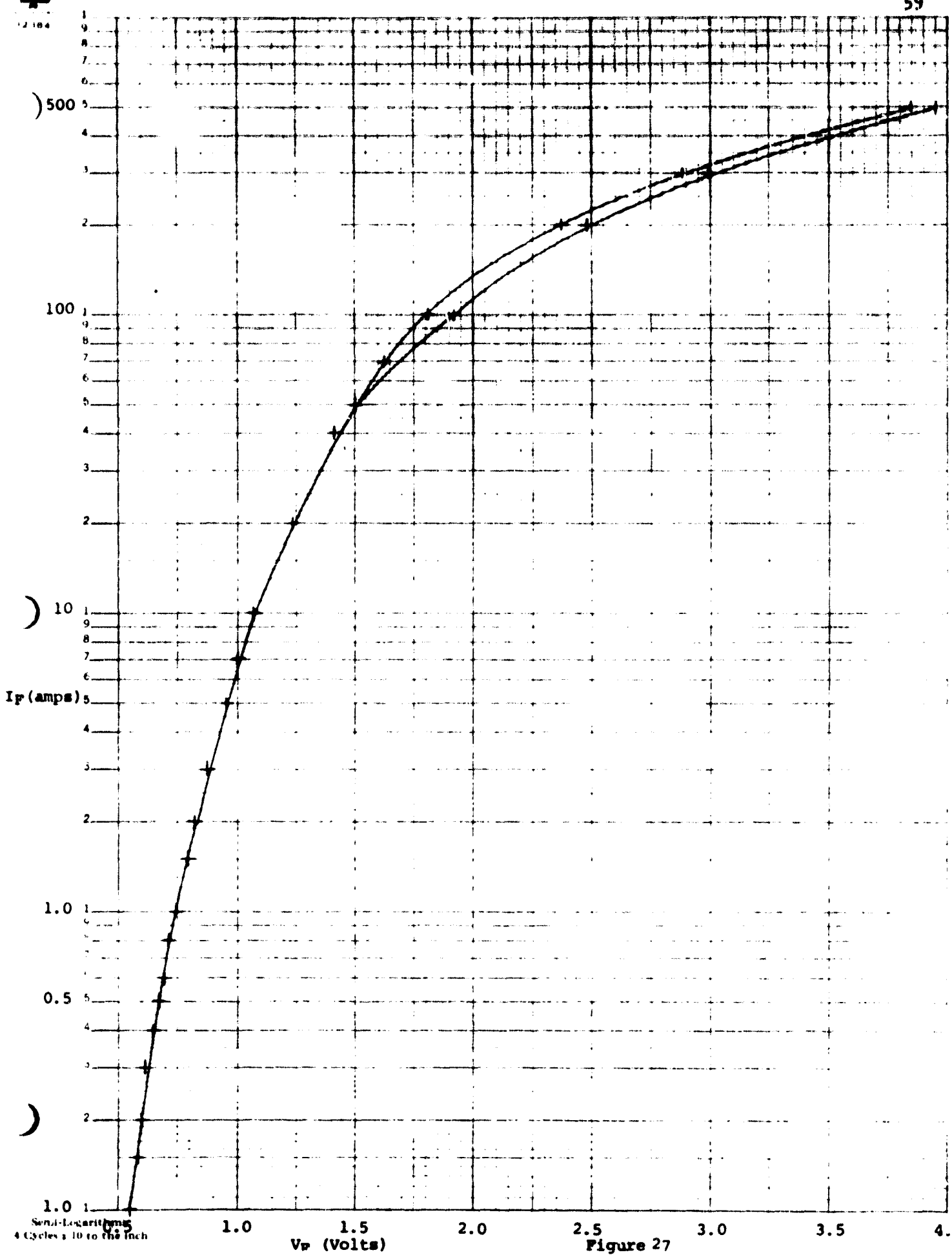


Figure 27

Device #039 Forward characteristic curve

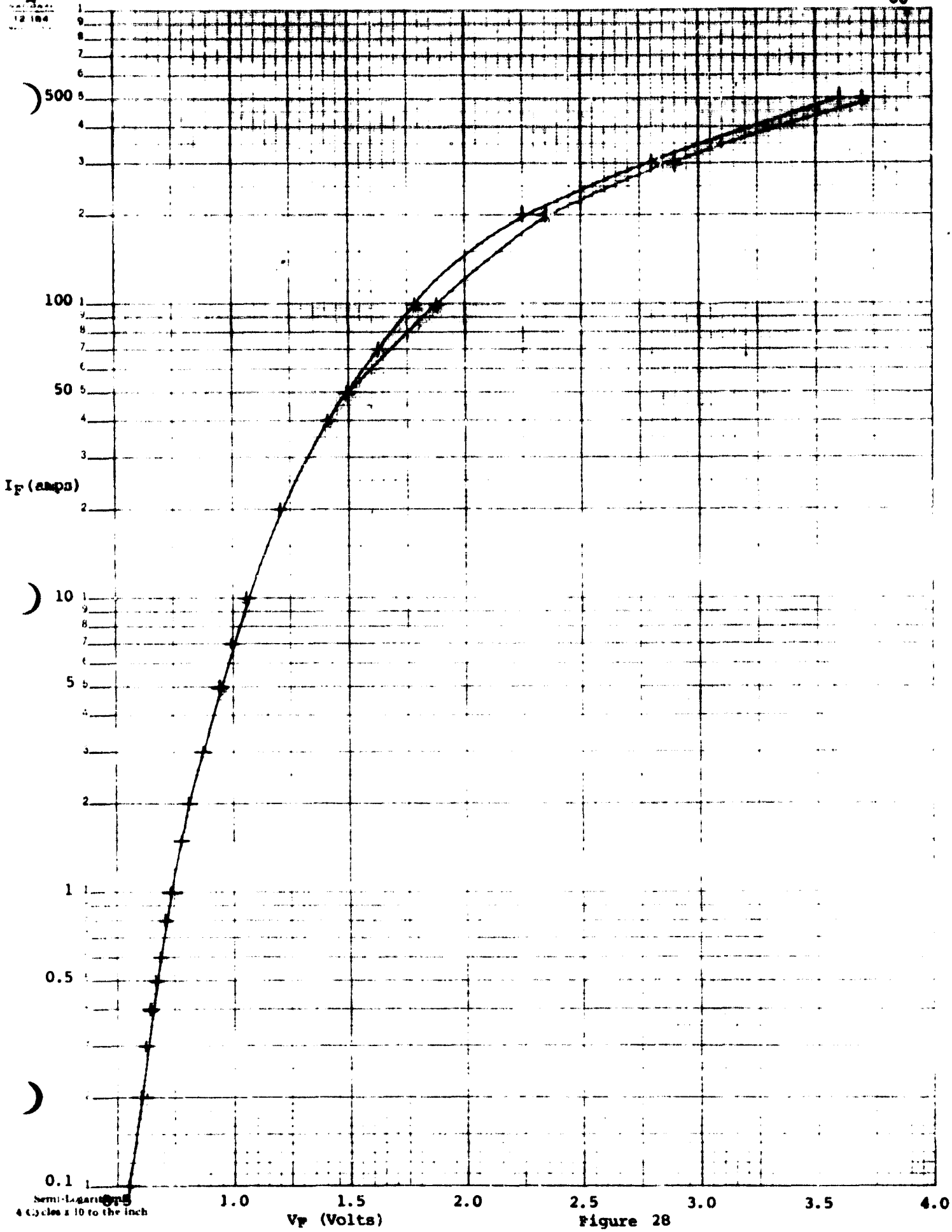
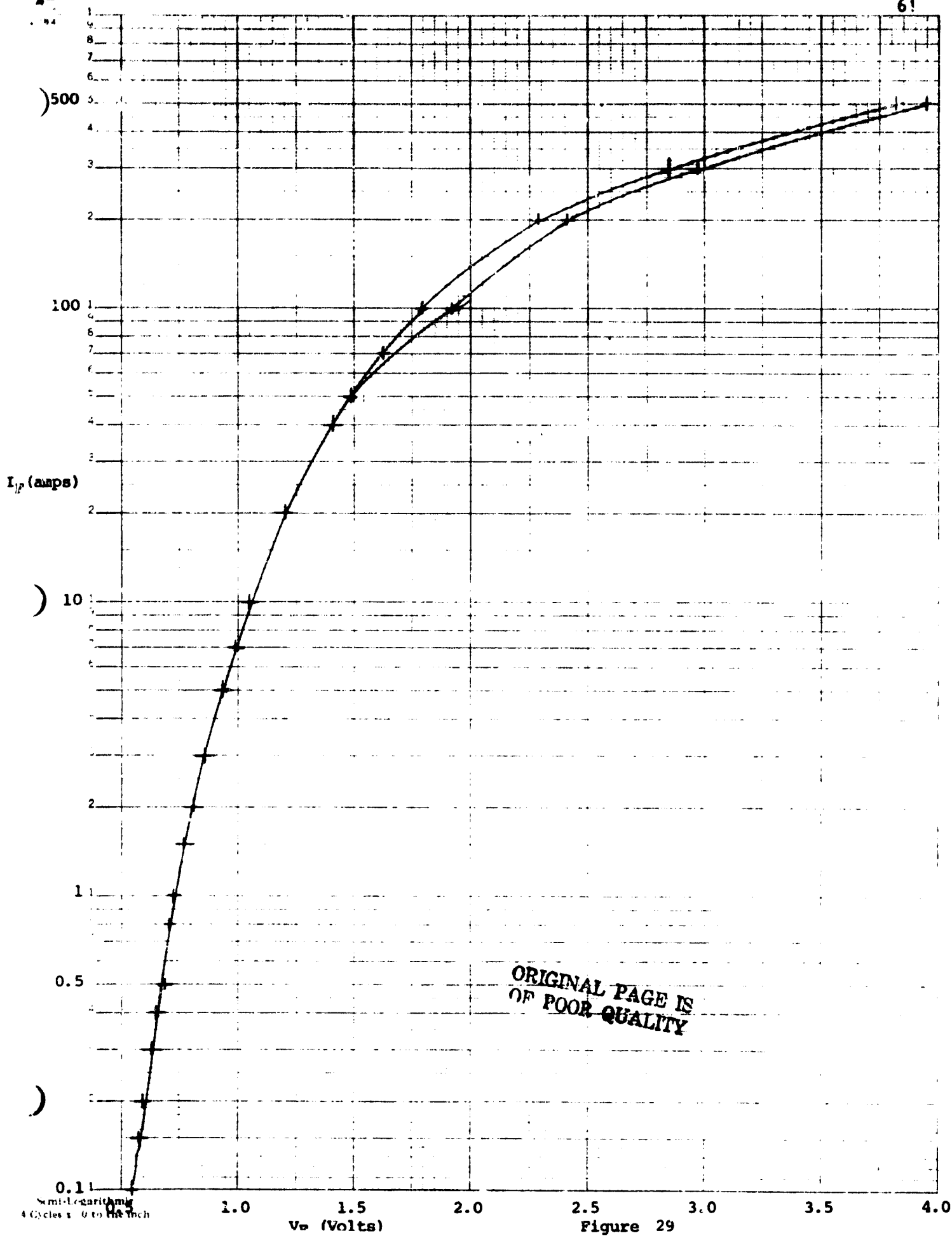


Figure 28

Device # 046 Forward characteristic curve



Semi-Logarithmic
4 Cycles x 10 to the Inch

Figure 29

Device #060 Forward characteristic curve

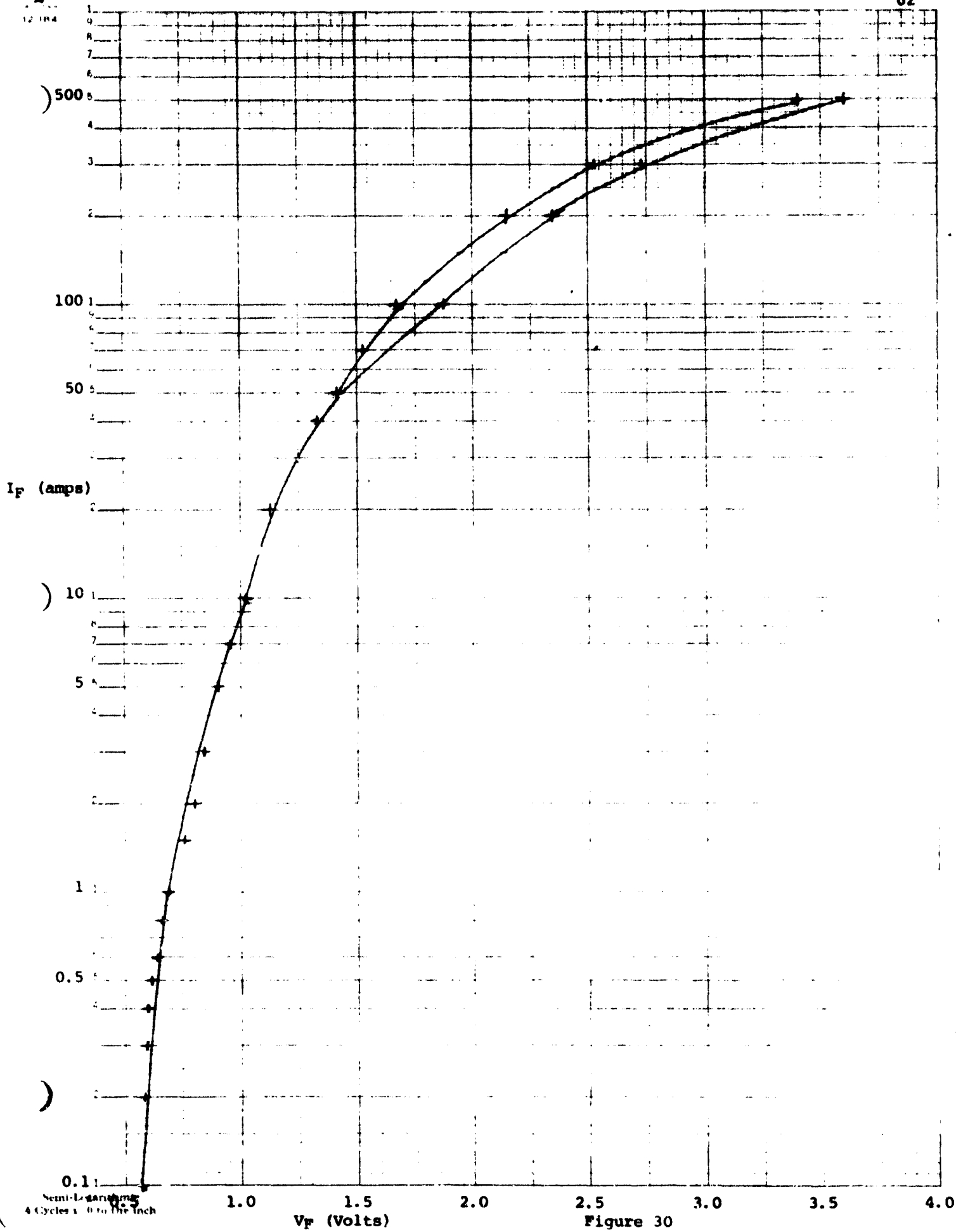


Figure 30

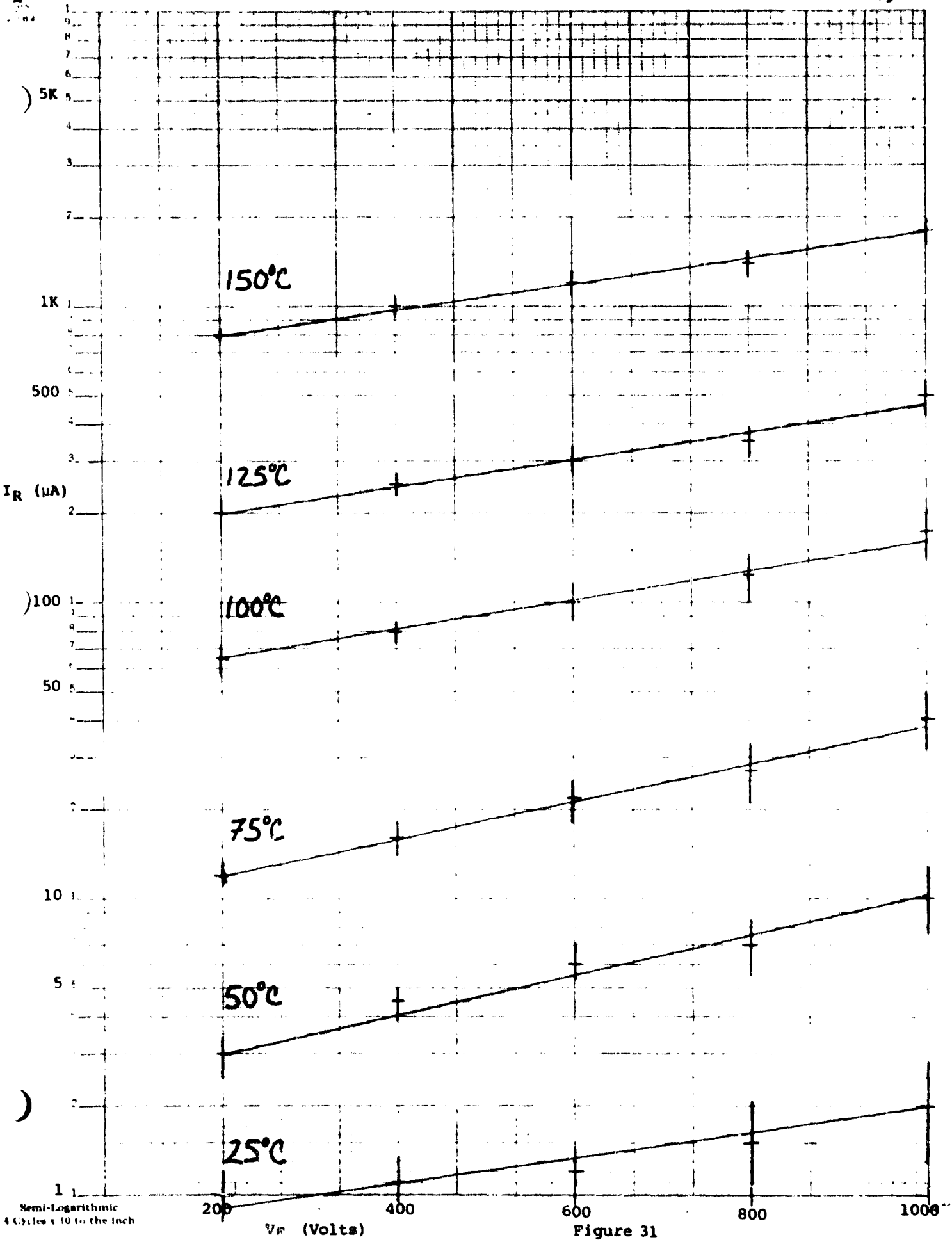

5K
1K
500
100
50
10
5
1
150°C
125°C
100°C
75°C
50°C
25°C
I_R (μA)
200
400
600
800
1000
V_R (Volts)
Semi-Logarithmic
4 Cycles x 10 to the Inch

Figure 31

Device # 038 Reverse leakage

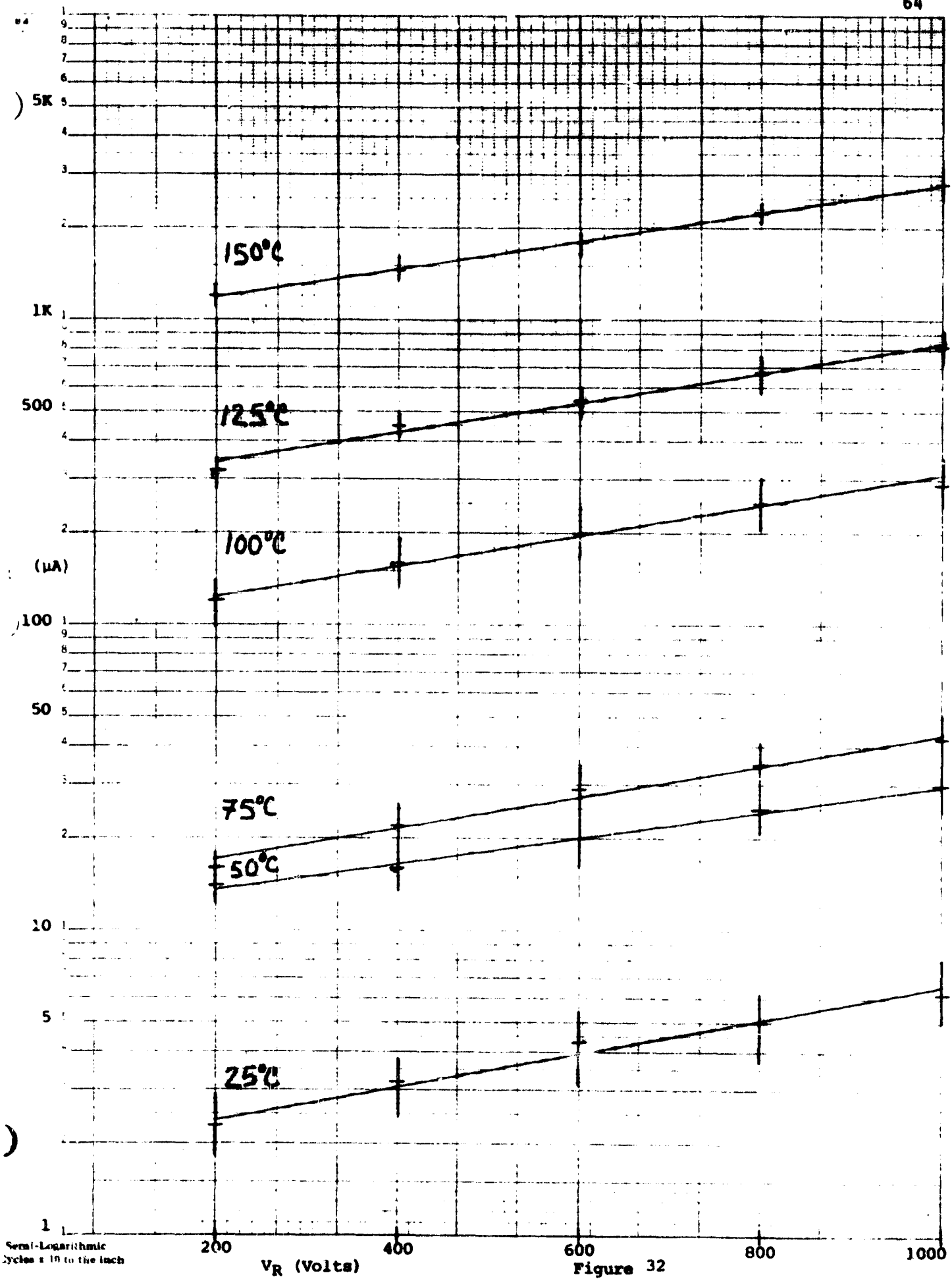


Figure 32

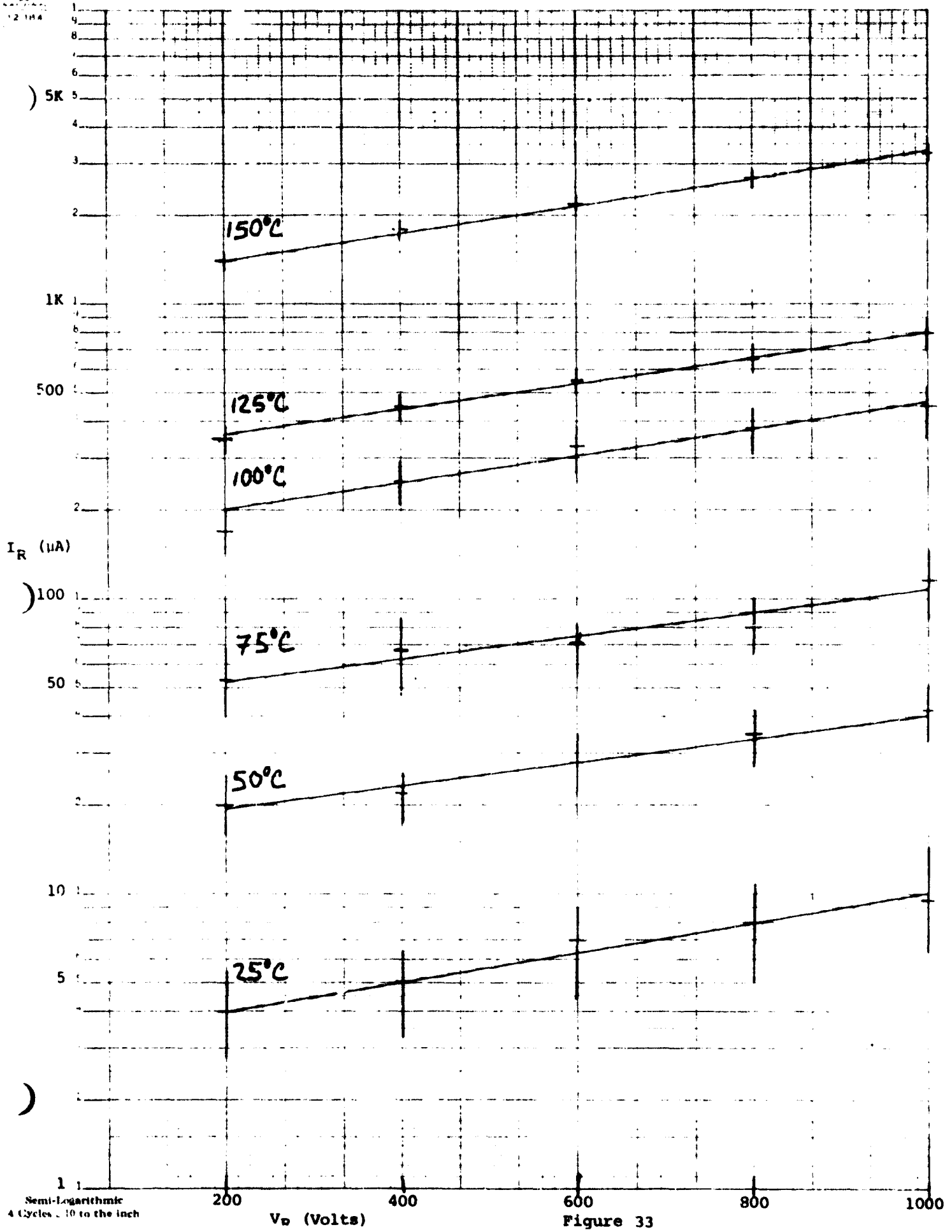

5K
1K
500
100
50
10
5
1
150°C
125°C
100°C
75°C
50°C
25°C
I_R (μA)
200
400
600
800
1000
V_D (Volts)
Semi-Logarithmic
4 Cycles - 10 to the inch

Figure 33

Device #046 Reverse leakage

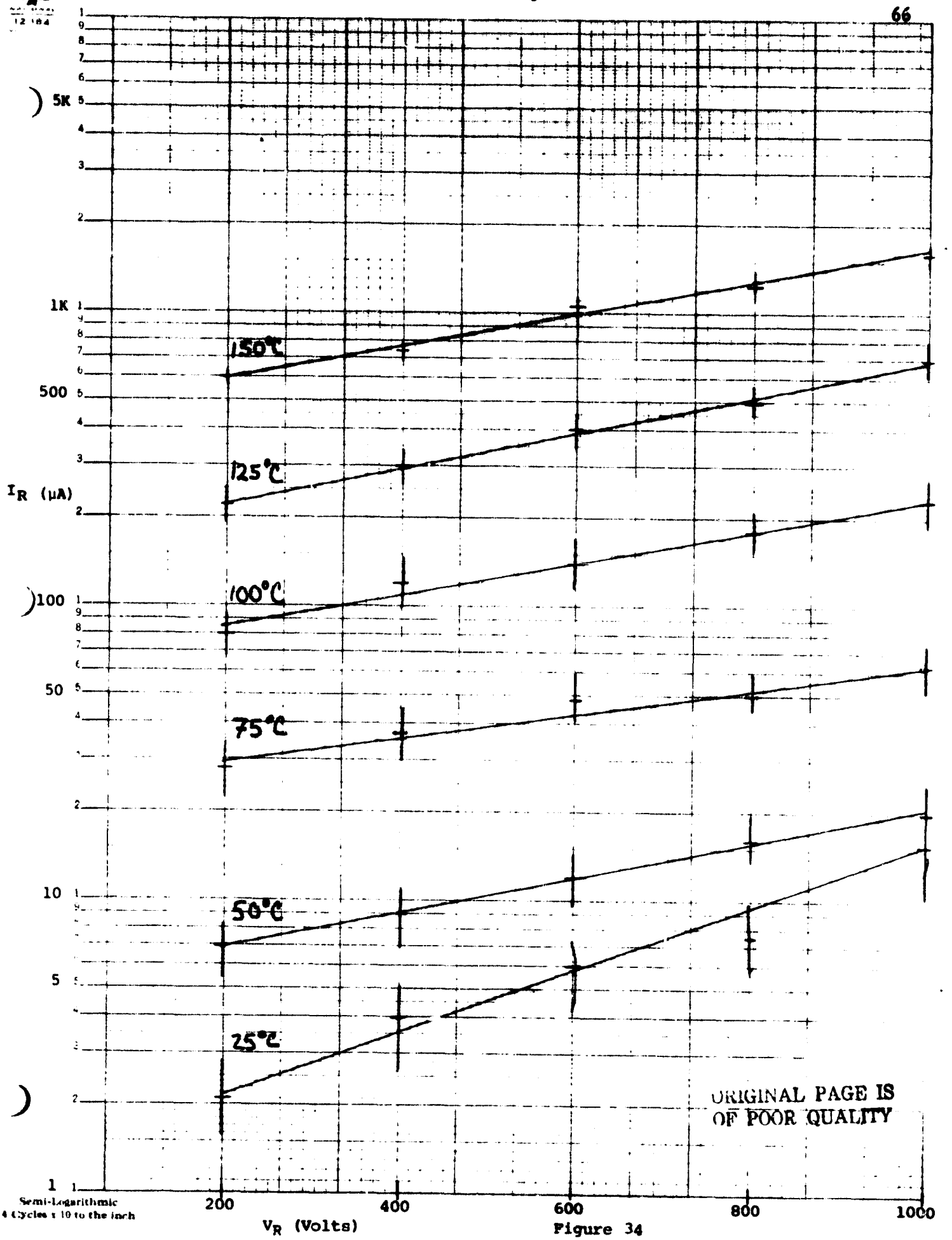


Figure 34

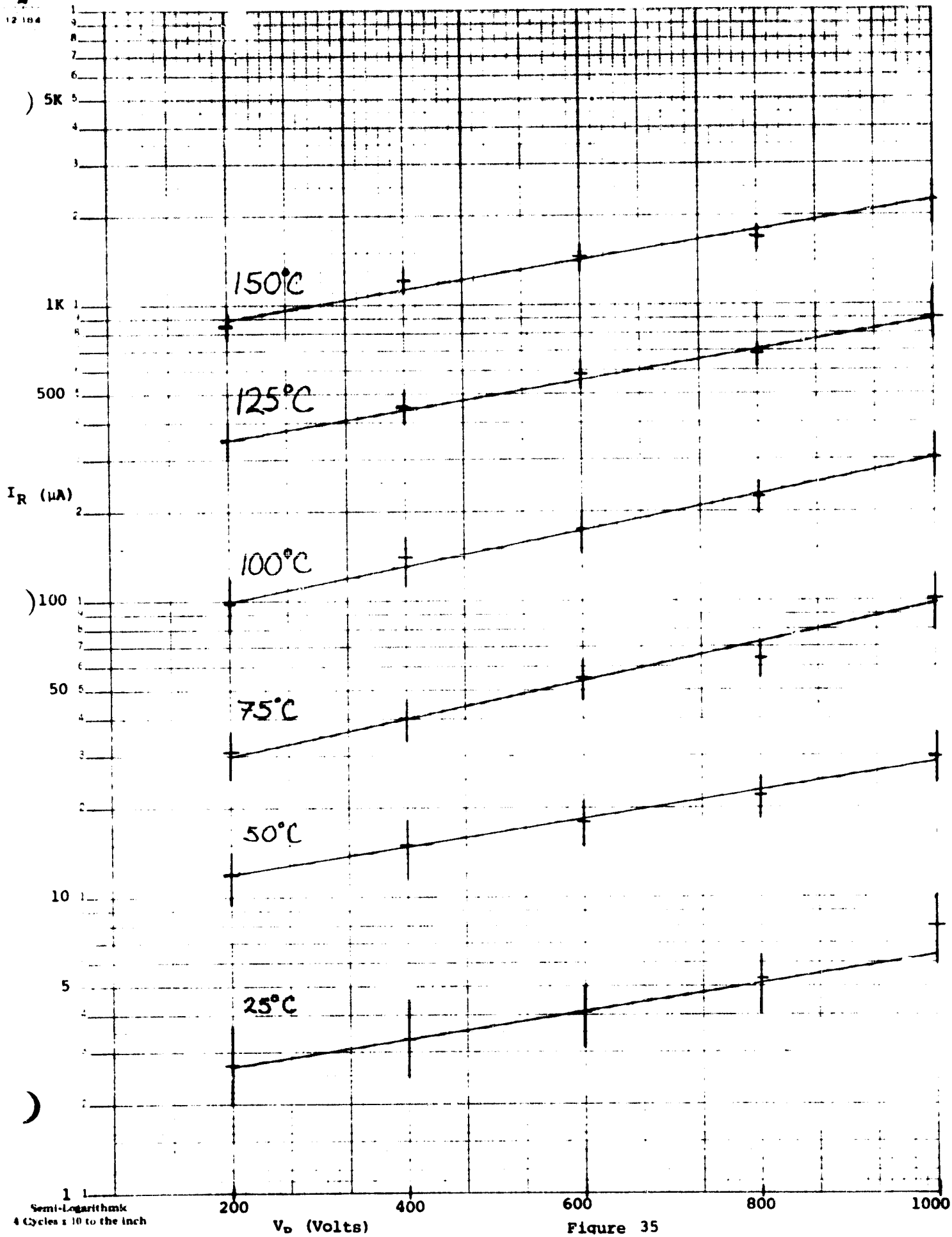

5K
1K
500
100
50
10
5
1
I_R (μA)
150°C
125°C
100°C
75°C
50°C
25°C
200
400
600
800
1000
V_D (Volts)
Semi-Logarithmic
4 Cycles x 10 to the inch

Figure 35

Leakage versus temperature

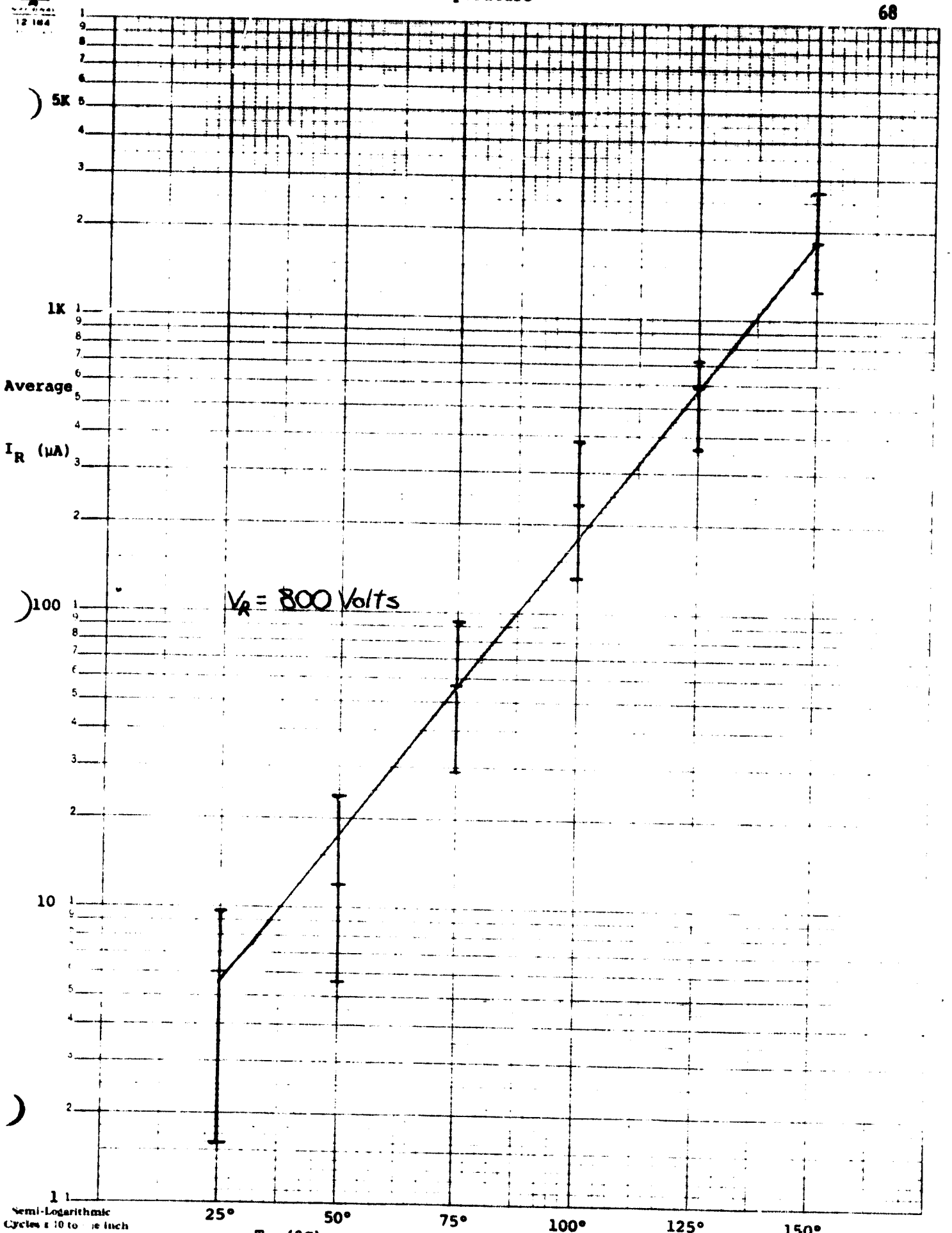


Figure 36

Device #031 Capacitiance versus reverse voltage

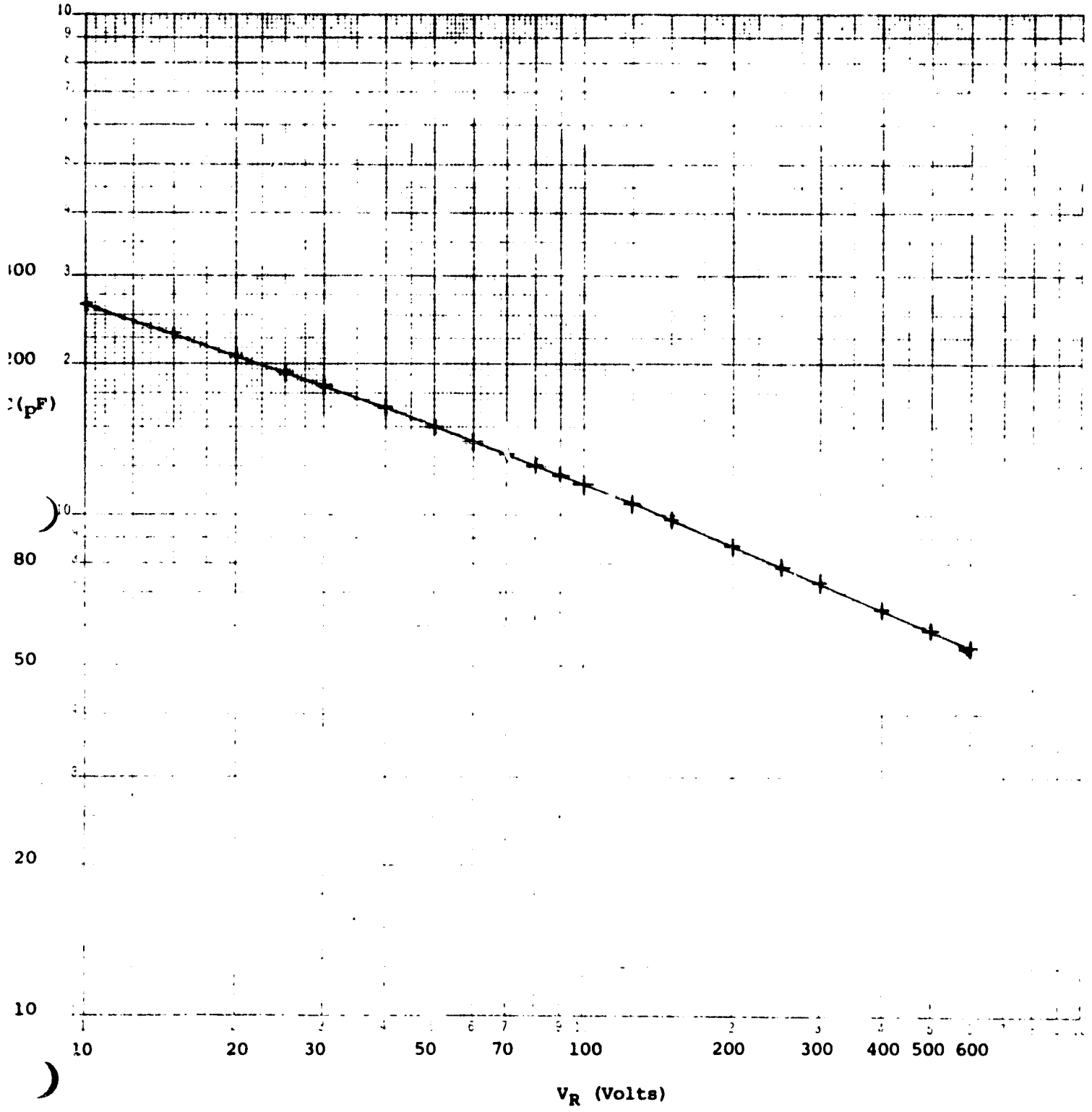


Figure 37

Logarithmic, 2 x 2 Cycles

Device #038 Capacitance versus reverse voltage

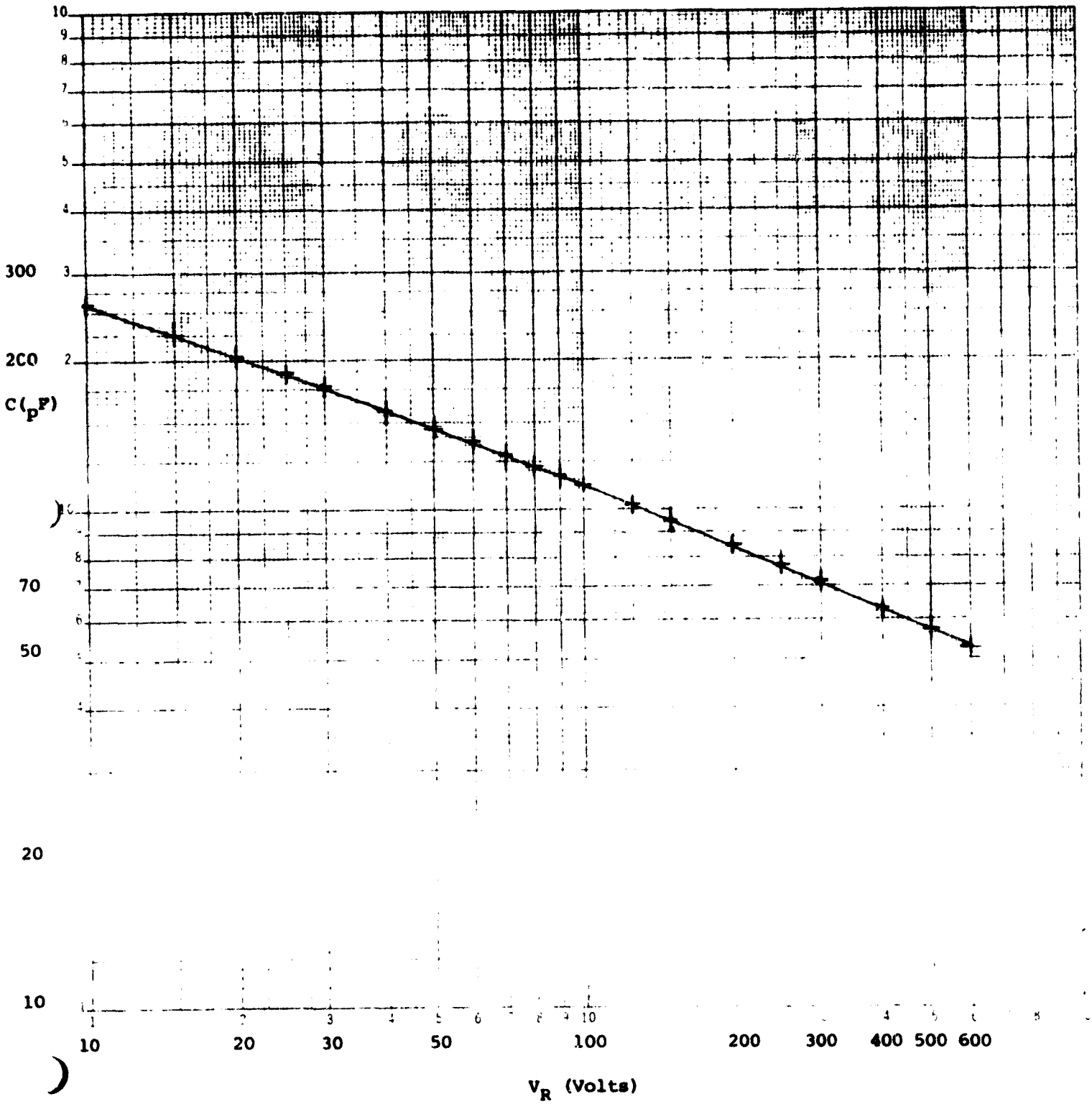


Figure 38

Logarithmic, 2 x 2 Cycles

Device #039 Capacitance versus reverse voltage

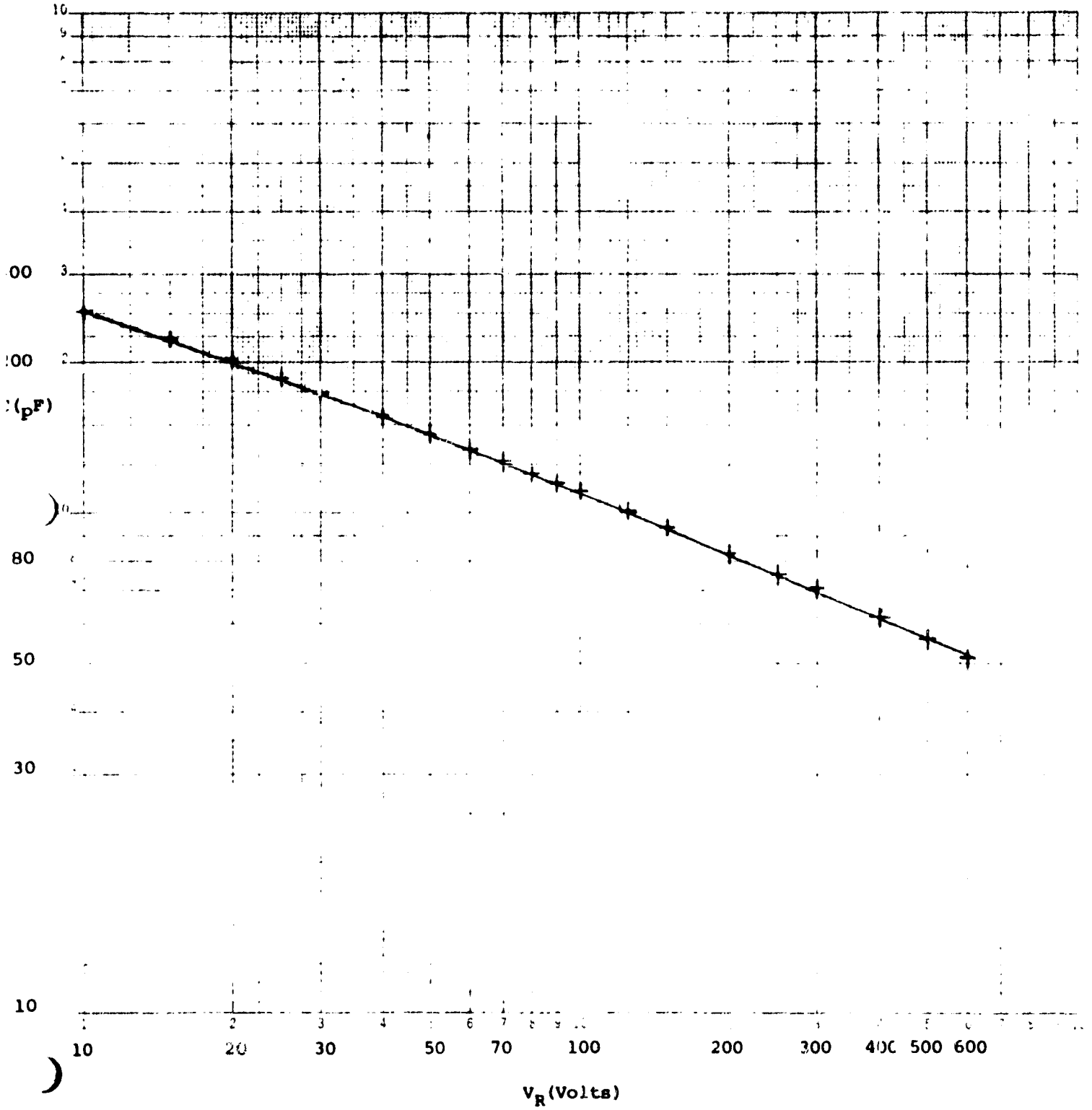


Figure 39

Logarithmic, 2 x 2 Cycles

Device #046 Capacitance versus reverse voltage

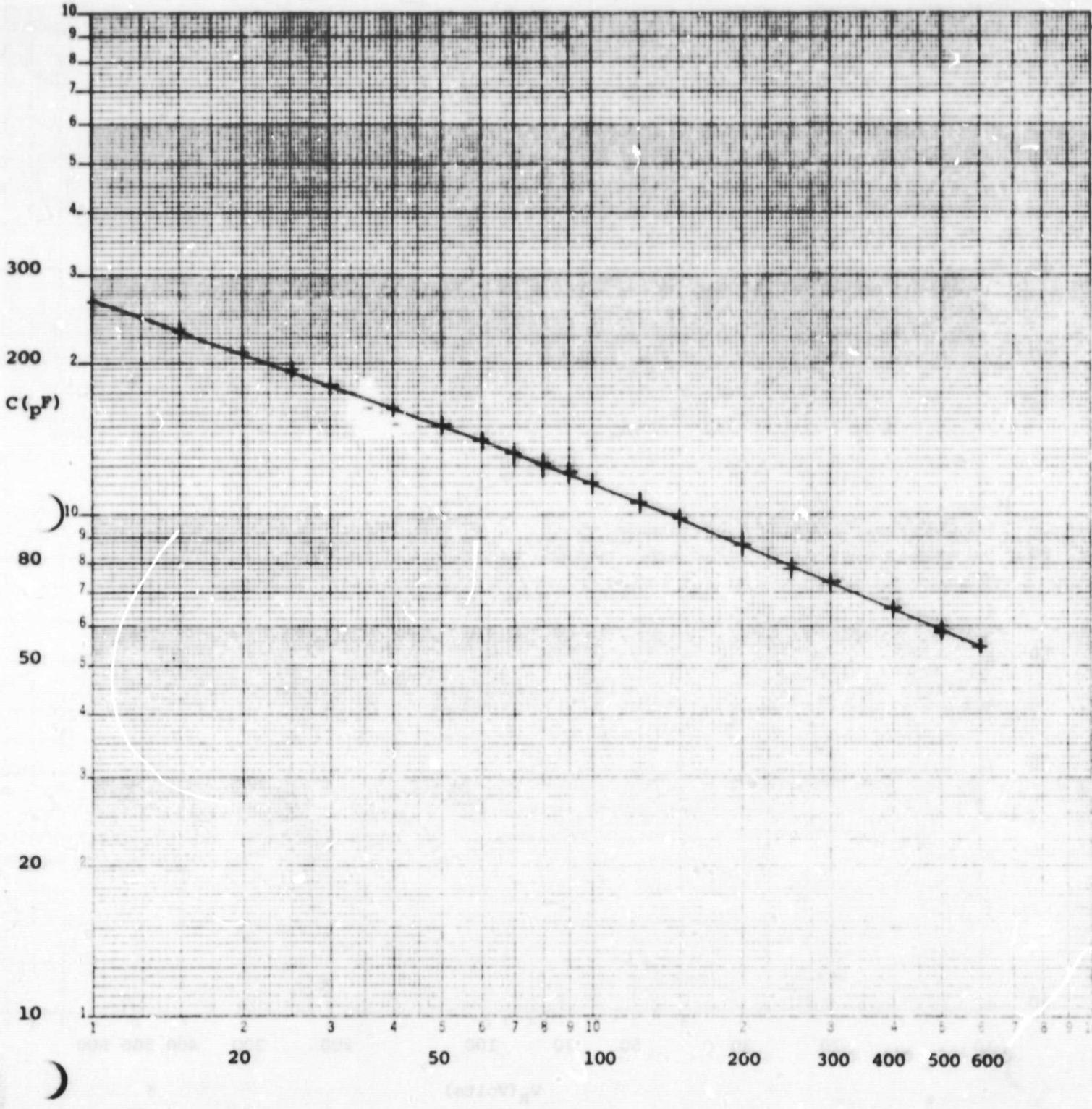


Figure 40

Logarithmic, 2 x 2 Cycles

Device #060 Capacitance versus reverse voltage

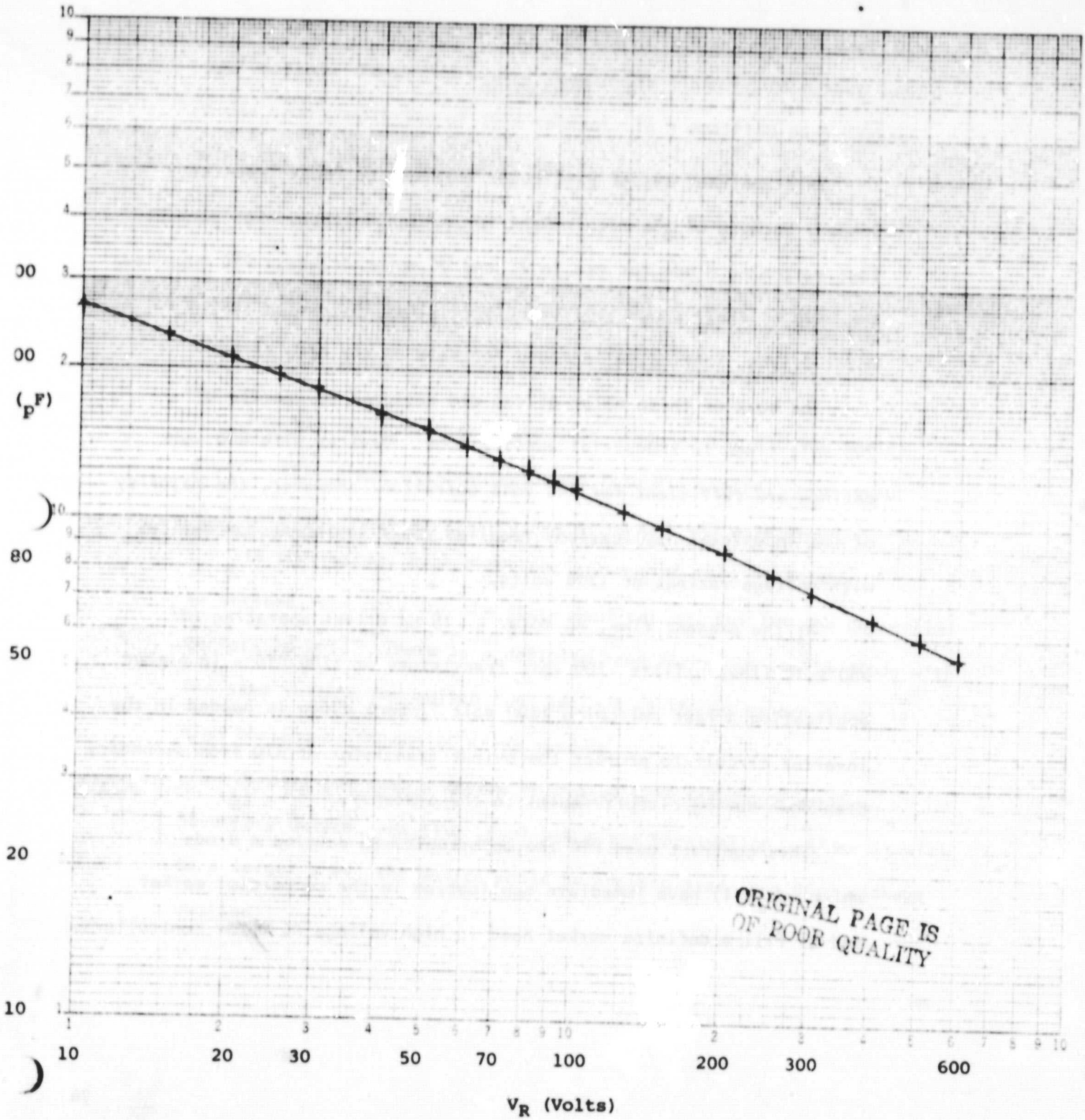


Figure 41

Logarithmic, 2 x 2 Cycles

8. CONCLUSION

This contract was of particular interest to Power Transistor Company because of the requirement for a high voltage, high current, fast switching diode for use in AC and DC motor drives. PTC supplies the bulk of their power semiconductor devices for energy saving AC motor drives, fabricated in-house for sale on the open market.

The bulk of these motor drives are designed to operate off 240 volt lines in industrial applications. Devices with 600 volt ratings are sufficient for 240 volt operation. However, the majority of the industrial applications requires power semiconductor devices with voltage ratings of 1200 volts.

At the present time, AC motor 5 - 15 hp drives operating off 480 volt lines utilize 1200 volt transistors or 1200 GTO's in either application a fast switching 1200 volt flyback diode is needed in the inverter circuit to protect the output transistor or GTO from secondary breakdown during circuit faults in the system.

This contract gave PTC the opportunity to develop a diode which would 1) have immediate application in the commercial market and 2) fill a definite market need in high voltage AC motor controllers.

Currently, there are no diodes commercially available to meet this application. Power Transistor Company is planning to market such a diode upon completion of this contact, in a modified DO-5 package with the following specifications:

Peak inverse voltage	-	1200 volts minimum
Forward voltage @ 50 amperes	-	1.5 volts maximum
Reverse recovery time	-	400 nanoseconds maximum
Surge rating	-	600 amperes minimum

PTC has designated the 1200 volt diode as the PTC 900 series diode. This diode has been designed into PTI Controls prototype 15 horsepower AC drive systems operating off 480 volt lines.

In the future, higher current ratings of this diode should be pursued, not only for the space application, but for the commercial markets as well. There is a definite need for a 150 ampere diode with the same voltage and switch time ratings as the 50 ampere diode in high horsepower AC and DC drive systems.

We envision such a device to be the same structure as the 50 ampere device, positive bevel and glass passivation. Since it will be a larger area, the device would be encapsulated in a DO-9 package outline.

9. ACKNOWLEDGEMENTS

Editor: Vilnis Balodis

Contributors:

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James J. Duffin

Charles Gaugh

Helen M. Karatnicki

Guin Troutman

10. REFERENCES

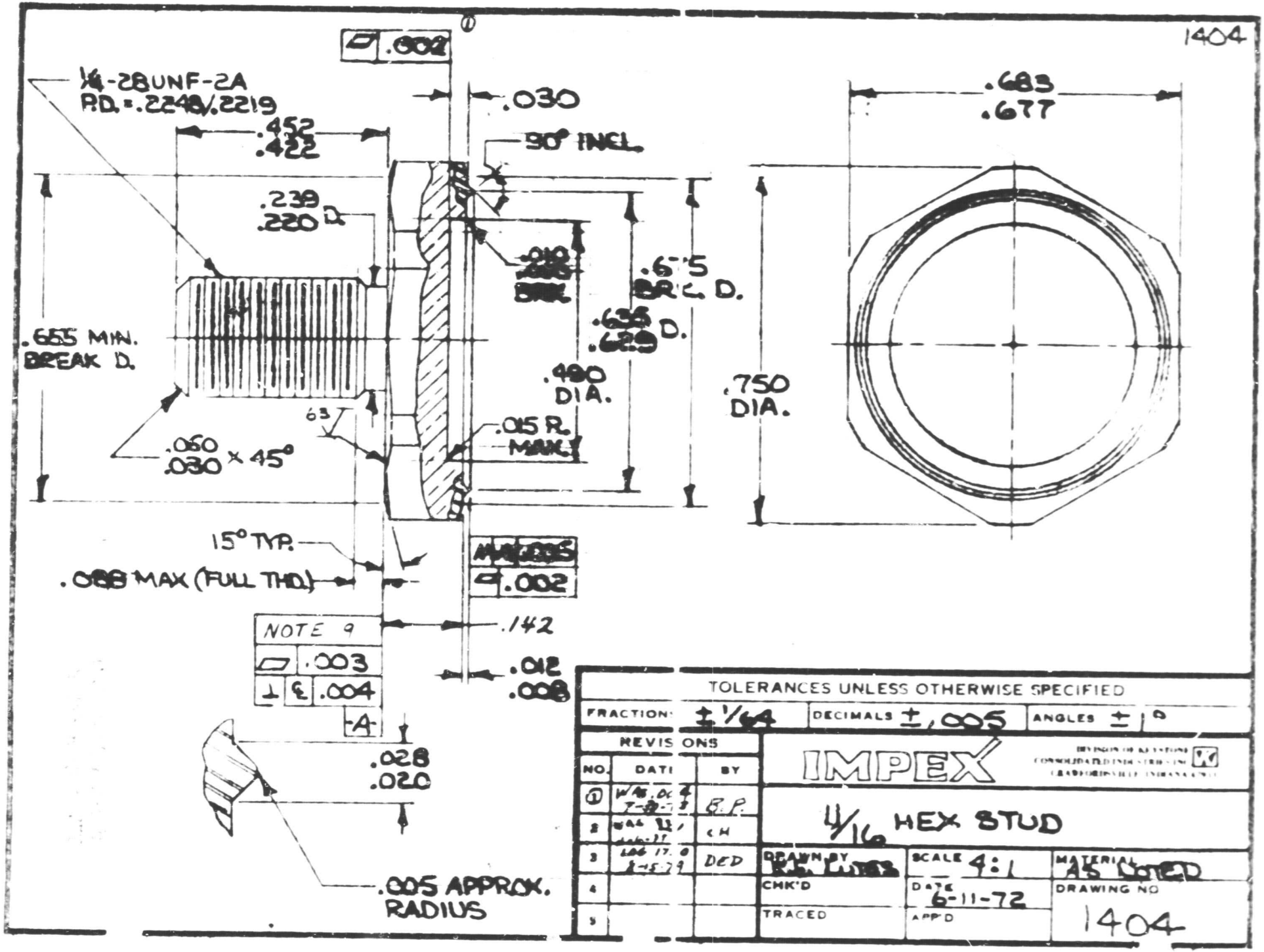
1. A. H. Berman, "Avalanche Breakdown in Diffused P-N Junctions In Silicon", Private Communication (1980)
2. H. Lawrence and R. M. Warner, "Diffused Junction Depletion Layer Calculations", Bell Systems Tech. J. pg 47 (1959)
3. R. L. Davies and F. E. Gentry, "Control of Electric Field at the Surface of P-N Junctions", IEEE Transactions on Electron Devices, ED-11, No. 7, pg 313-323 (1964)
4. M. Otsuka, "The Forward Characteristics of Thyristors", Proceedings of the IEEE, Vol. 55, No. 1 pp. 1400-1408 (1967)

11.1 SPECIFICATIONS FOR FAST RECOVERY, HIGH VOLTAGE POWER DIODE CASE TEMPERATURE = 25°C UNLESS OTHERWISE SPECIFIED

Type 1 - Fast Recovery Power Diode, 50A Avg. Current Rating

SYMBOL	CHARACTERISTICS WITH TEST CONDITIONS	VALUE	UNITS
V_{RRM}	Peak Repetitive Reverse Voltage, T_J = 150°C	800 to 1000	Volts
V_R	DC Blocking Voltage, T_J = 150°C	800 to 1000	Volts
V_{RSM}	Peak Non-repetitive Reverse Voltage, T_J = 150°C	$\geq$ 1.25 V_{RRM}	Volts
I_{RRM}	Max. Reverse Current at Rated V_{RRM} I_F = 50A Forward Current T_J = 25°C T_J = 150°C	 0.05 5.0	 Milliamps Milliamps
I_F	Average Forward Current at T_C = 100°C	50	Amps
I_{FSM}	Non-Repetitive Peak Surge Current (1/2 cycle surge current at 60Hz under load)	1000	Amps
V_{FM}	Forward Voltage at Rated I_F = 50A	1.5	Volts
T_J	Operating Junction Temperature Range	-65 to 200	°C
T_{STG}	Storage Temperature Range	-65 to 200	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.5	°C/W
t_{rr}	Reverse Recovery Time, T_C = 100°C I_F = 1.0A to V_R = 30 V_{dc} I_{FM} = 50A, dI/dt = 25A/µsec (JEDEC circuit)	 50 200	 nsec nsec
$I_{RM(REC)}$	Peak Reverse Recovery Cirrent I_{FM} = 50A, dI/dt = 25A/µsec (JEDEC circuit)	5	Amps

1404



TOLERANCES UNLESS OTHERWISE SPECIFIED

FRACTIONS ±1/64 | DECIMALS ±.005 | ANGLES ±1°

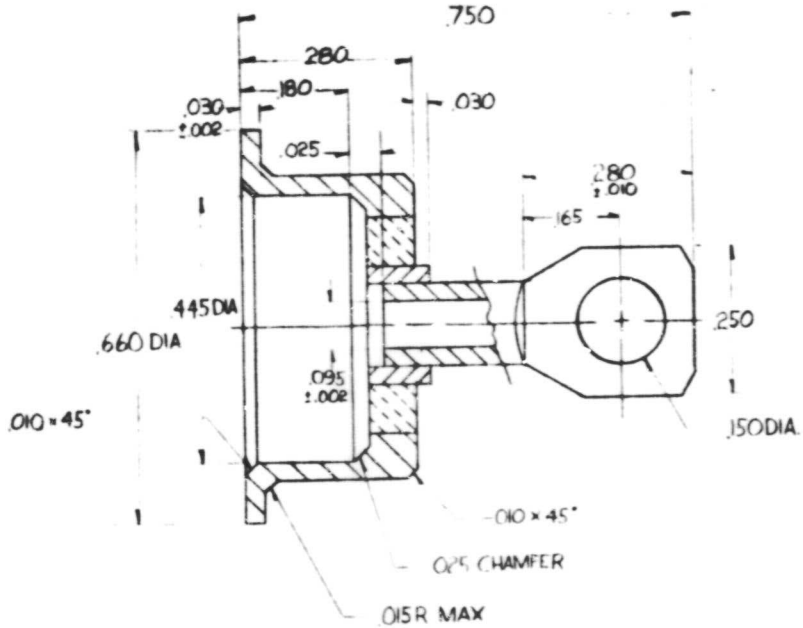
REVISIONS			
NO.	DATE	BY	
1	[illegible]	B.P.	
2	[illegible]	C.H.	
3	[illegible]	DED	
4			
5			

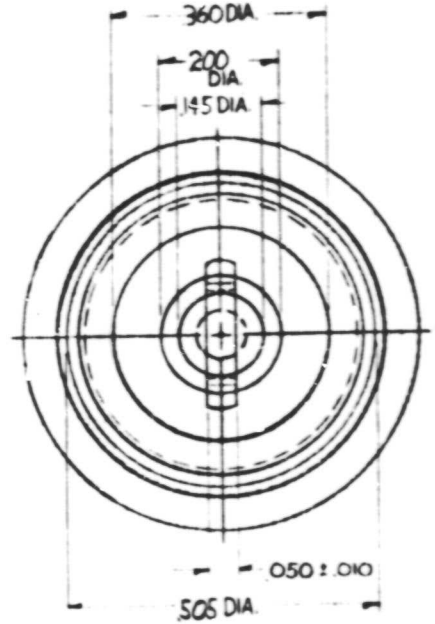
IMPEX

4/16 HEX STUD

DRAWN BY [illegible]	SCALE 4:1	MATERIAL AS NOTED
CHK'D	DATE 6-11-72	DRAWING NO 1404
TRACED	APP'D	

REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPD'D
NC				





ITEM NO	QTY REQ'D	PART NO	DESCRIPTION	UNIT WEIGHT	MFG
			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED
TOLERANCES
FRACTIONS ± .03
.XX ± .03
.XXX ± .010
ANGLES ± 1°

DRAWN BY RJS 2/28/81
CHECKED
APPROVED

PTI PRECISION TRANSFORMER
ARANSAS, CALIF.

TITLE
DO-5 CAP HOUSING

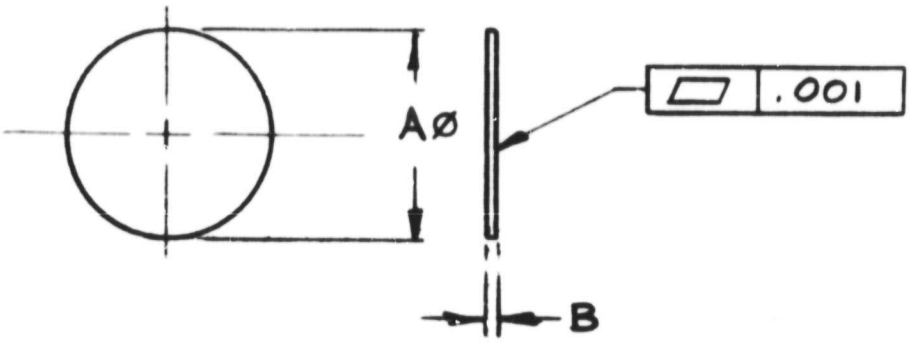
SCALE 5X
SHEET OF

SIZE B
CODE NO. 50-0016
REV NC

NEXT ASSY
USED ON

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPR'D



UNLESS OTHERWISE SPECIFIED	POWER TRANSISTOR CO. TORRANCE, CALIF., 90502			
TOLERANCES .XX ± ____ .XXX ± .002 ANGLES ± ____	SCALE: NONE DATE: 25 APR 80	APPROVED BY	CHECKED BY	DRAWN BY SHEET 1 OF 2
	TITLE MOLY TAB, ROUND			
		REV N/C	DRAWING NUMBER 50-0003	

DIETZGEN MASTER FORM 108MF

DWG NO.	DIM. A	DIM. B	MATERIAL	FINISH	
-1	.160	.010/.012	1	2	
-2	.300	.010/.012	1	2	
-3	.310	.010/.012	1	2	
-4	.250	.010/.012	1	2	

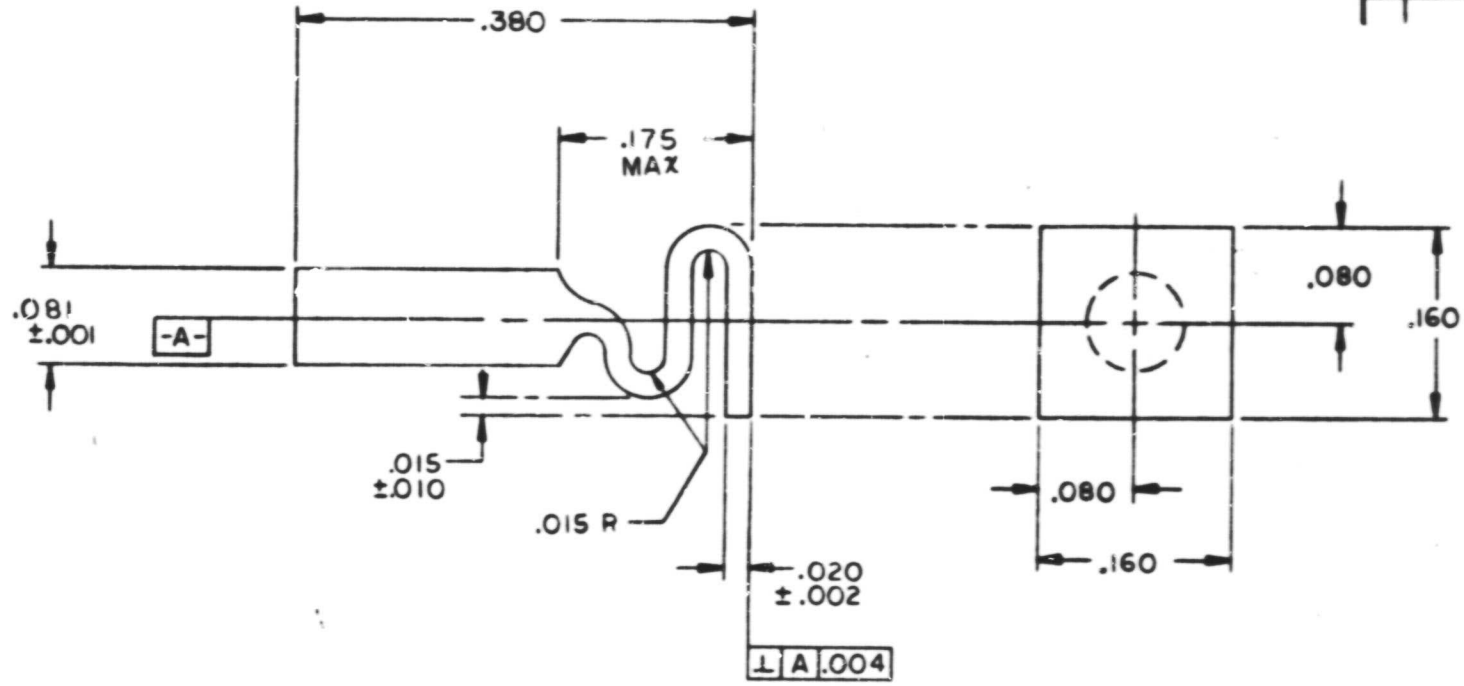
3. REMOVE BURRS.

2. FINISH: NICKEL PLATE

1. MATERIAL: MOLYBDENUM

NOTES: UNLESS OTHERWISE SPECIFIED

SCALE NONE	DWG NO.	REV
SHEET 2 OF 2	50-0003	N/C



3. FINISH: PART IS TO BE FREE OF OXIDATION, SCALE, FOREIGN MATERIAL, EXCEPT LUBRICANTS EASILY REMOVED BY NORMAL TRICHLORCLEANING OPERATION.
2. PART MUST NOT BECOME BRITTLE AFTER ANNEALING TO A DEAD SOFT CONDITION IN A HYDROGEN ATMOSPHERE.
1. MATL: OFHC COPPER WIRE, .081±.001 DIA, AS DRAWN OR ANNEALED.

NOTES: UNLESS OTHERWISE SPECIFIED

PTI PRECISION TRANSFORMER
ANAHEIM, CALIF.

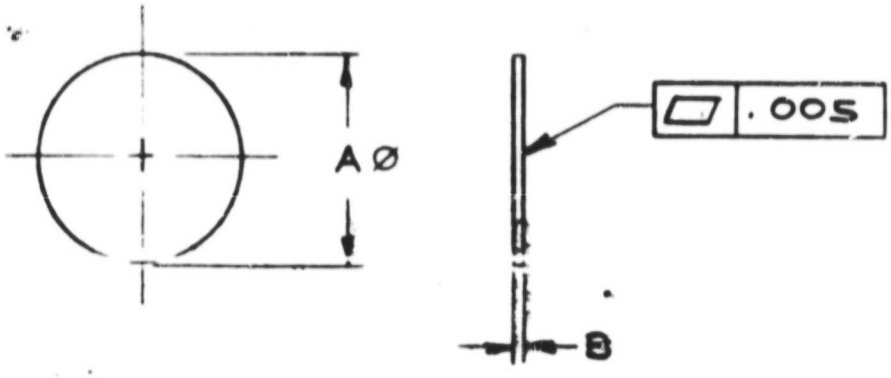
LEAD, INTERNAL, "S" BEND

DRAWN RS 9-18-80
CHECKED RC 9-18-80
APPROVED

SCALE 10X
SHEET 1 OF 1

SIZE B
DWG NO. 50-0011

REVISIONS				
SYM	DESCRIPTION	BY	DATE	APPR'D
A	ADD DWG NO -5	V.B.	10/10/80	



UNLESS OTHERWISE SPECIFIED	POWER TRANSISTOR CO. TORRANCE, CALIF., 90502			
TOLERANCES .XX ± .__ .XXX ± .002 ANGLES ± ____	SCALE: NONE DATE: 25 APR 80	APPROVED BY	CHECKED BY	DRAWN BY SHEET 1 OF 2
	TITLE PREFORM, SOLDER, ROUND			
		REV A	DRAWING NUMBER 50-0004	

DWG NO.	DIM. A	DIM. B	MATERIAL
-1	.150	.002/.003	1
-2	.300	.002/.003	1
-3	.160	.002/.003	2
-4	.310	.002/.003	2
-5	.160	.002/.003	1
-6	.250	.002/.003	3
-7	.160	.002/.003	3

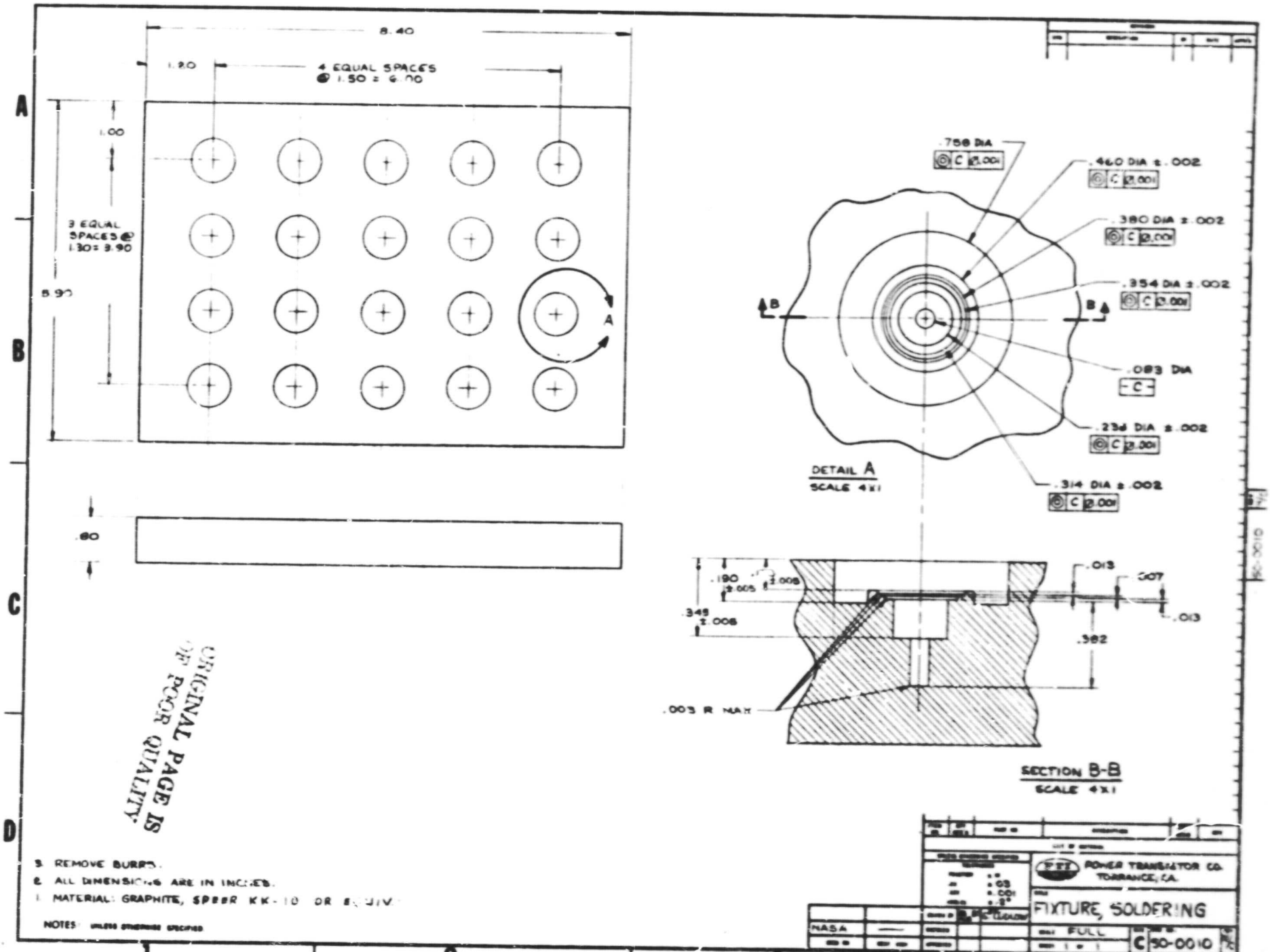
3 MATERIAL: SOLDER 50/50 Pb/In

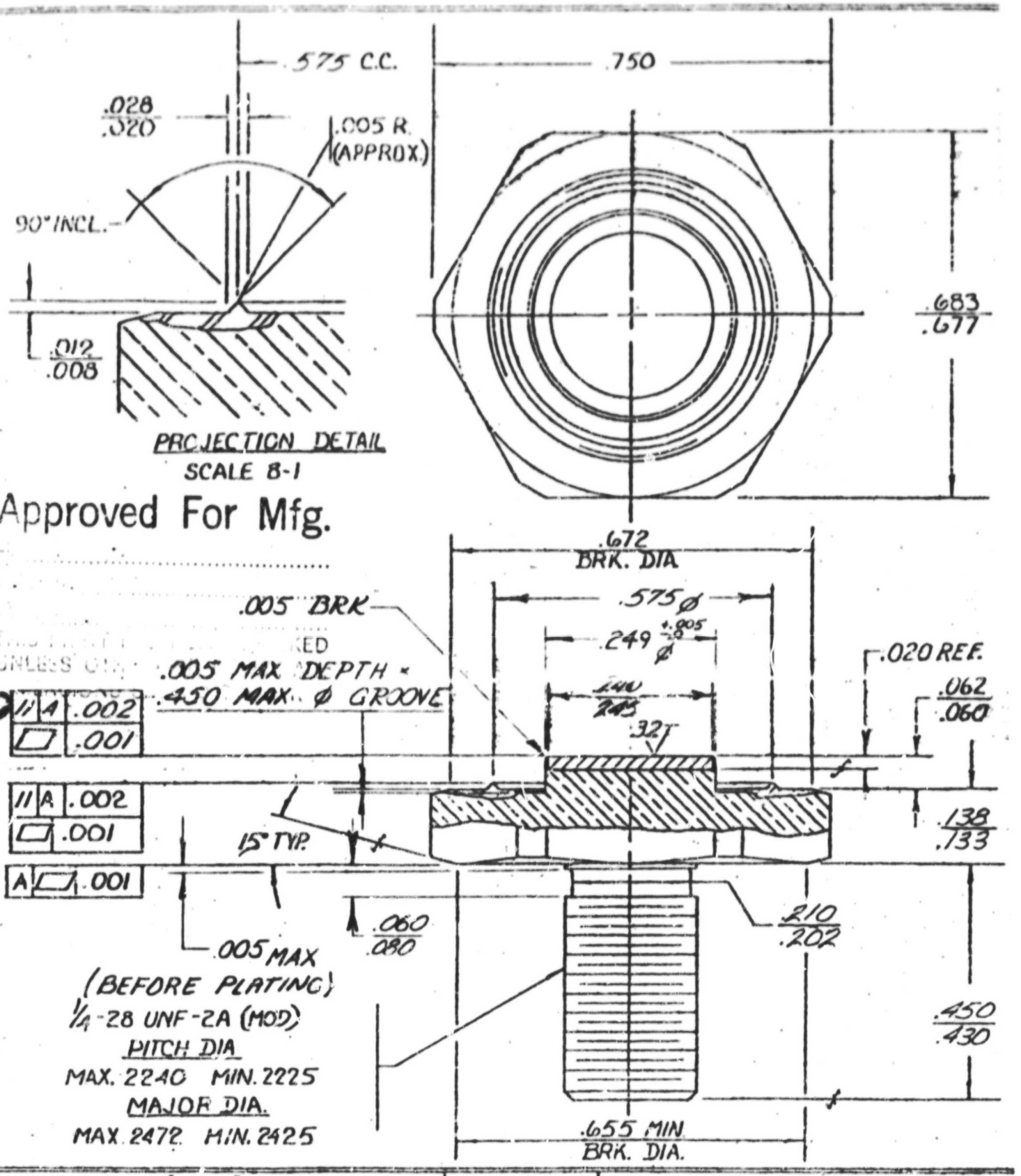
2 MATERIAL: SOLDER 92.5/2.5/5.0, Pb/Ag/In

1 MATERIAL: SOLDER 5/95, Sn/Pb.

NOTES: UNLESS OTHERWISE SPECIFIED:

SCALE NONE	DWG NO.	REV
SHEET 2 OF 2	50-0004	A


8.40
1.20
4 EQUAL SPACES @ 1.50 = 6.00
1.00
3 EQUAL SPACES @ 1.30 = 3.90
5.90
A
.80
.758 DIA
C
.460 DIA ± .002
.380 DIA ± .002
.354 DIA ± .002
.093 DIA
.234 DIA ± .002
.314 DIA ± .002
B
DETAIL A
SCALE 4X1
.190
.345 ± .006
.013
.007
.013
.382
.003 R MAX
SECTION B-B
SCALE 4X1
ORIGINAL PAGE IS OF POOR QUALITY
3. REMOVE BURRS.
2. ALL DIMENSIONS ARE IN INCHES.
1. MATERIAL: GRAPHITE, SPEER KK-10 OR EQUIV.
NOTES: UNLESS OTHERWISE SPECIFIED
POWER TRANSISTOR CO.
TORRANCE, CA.
FIXTURE, SOLDERING
NASA
FULL
C
50-0010



PROJECTION DETAIL
SCALE 8-1

Approved For Mfg.

UNLESS OTHERWISE SPECIFIED

THE Nippert COMPANY

853 PITTSBURGH DR. DELAWARE, O.

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± 1/16
DECIMALS ± .005
ANGLES ± 2°
√ MACH'D SURF.

ORIGINAL PAGE IS OF POOR QUALITY

APPROVED BY SS DATE 4-27-78
DRAWN BY KAT DATE 7-29-78

"N-6" — REGISTERED TRADEMARK
APPLICABLE U.S. AND FOREIGN PATENTS LISTED ON SHIPPING CARTONS. OTHER PATENTS PENDING.

MATERIAL NOTED
PART NAME STUD BASE
SHEET

ISSUED FEB 18 1980
SCALE 4:1
PART NO. 068-8703
REV 05

END
DATE
NOV. 19, 1981