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COMPARISONS OF SOME LARGE SCIENTIFIC COMPUTERS 1964 – 1986

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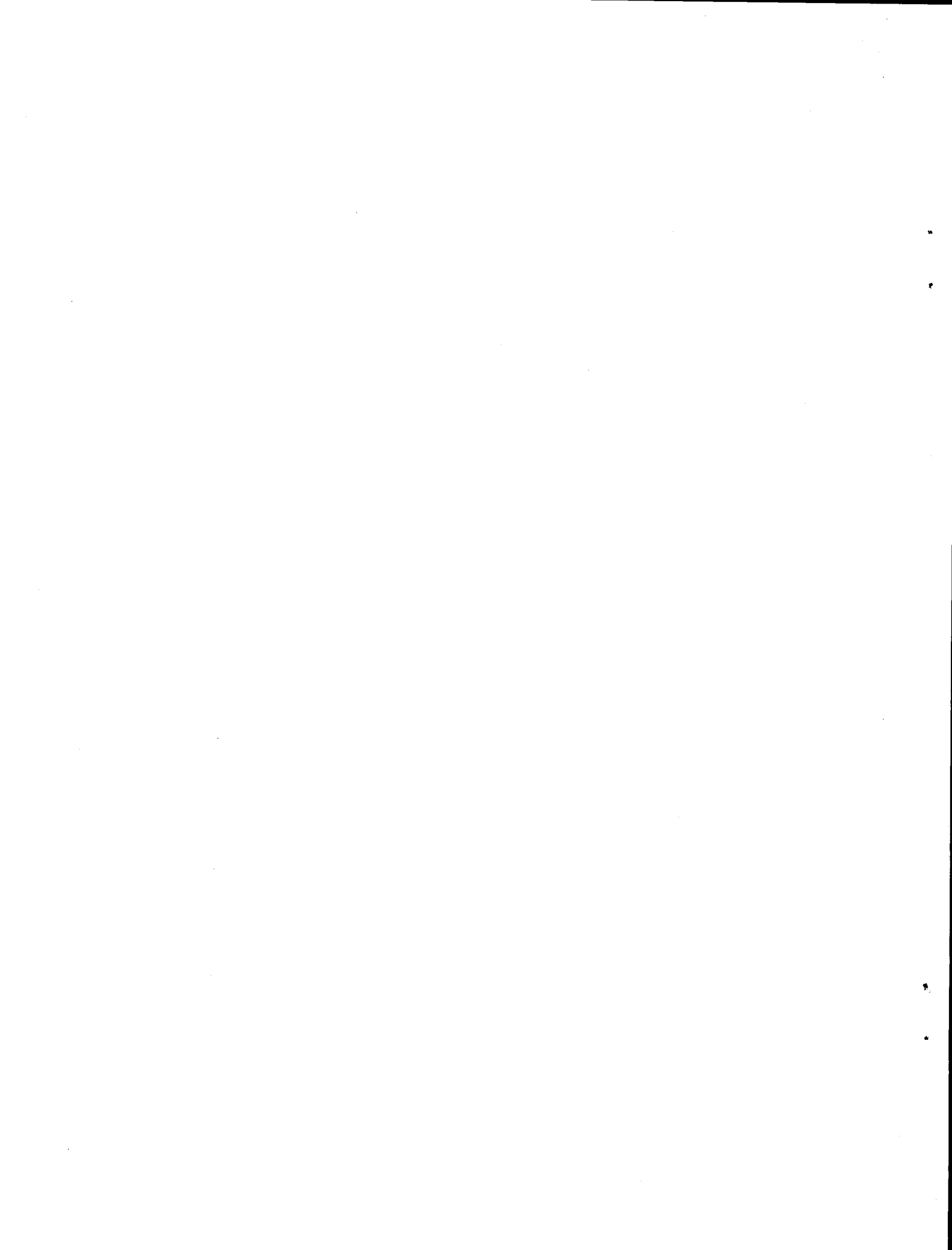
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COMPUTERS 1964 - 1986

by

Karen R. Credeur

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HAMPTON, VIRGINIA

SUMMARY

In 1975, the National Aeronautics and Space Administration (NASA) began studies to assess the technical and economic feasibility of developing a computer having a sustained computational speed of one billion floating point operations per second and a working memory of at least 240 million words. Such a powerful computer would allow computational aerodynamics to play a major role in aeronautical design and advanced fluid dynamics research. Based on favorable results from these studies, NASA proceeded with developmental plans. The computer was named the Numerical Aerodynamic Simulator (NAS).

To help insure that the estimated cost, schedule, and technical scope were realistic, a brief study was made of past large scientific computers. Large discrepancies between inception and operation in scope, cost, or schedule were studied so that they could be minimized with NASA's proposed new computer. The main computers studied were the ILLIAC IV, STAR 100, Parallel Element Processor Ensemble (PEPE), and Shuttle Mission Simulator (SMS) computer. Comparison data on memory and speed were also obtained on the IBM 650, 704, 7090, 7094, 360-50, 360-67, 360-91, and 370-195; the CDC 6400, 6600, 7600, CYBER 203, and CYBER 205; CRAY 1; and the Advanced Scientific Computer (ASC). A few lessons learned conclude the report.

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GLOSSARY

| | |
|--------|----------------------------------------------------------|
| ABM | anti-ballistic missile |
| AEC | Atomic Energy Commission |
| ARPA | Advanced Research Projects Agency |
| ASC | Advanced Scientific Computer, built by Texas Instruments |
| BMDATC | Ballistic Missile Defense Advanced Technology Center |
| CAU | command arithmetic units |
| CDC | Control Data Corporation |
| CFD | computational fluid dynamics |
| CPAF | cost plus award fee (contract) |
| CPFF | cost plus fixed fee (contract) |
| CPU | central processing unit |
| CU | correlation unit (input unit on PEPE) |
| DARPA | Department of Defense ARPA |
| DOD | Department of Defense |
| FLOPS | floating point operations per second |
| FMP | flow model processor for NAS |
| FP | fixed price (contract) |
| GFE | government furnished equipment |
| JSC | NASA's Johnson Space Center in Houston, Texas |
| K | thousand (of dollars) |
| M | million (of dollars) |
| MFLOPS | one million FLOPS |
| NAS | NASA's proposed Numerical Aerodynamic Simulator |
| NASA | National Aeronautics and Space Administration |
| NTE | not to exceed (contract cost) |
| R&D | research and development |
| PE | processing elements |
| PEPE | Parallel Element Processor Ensemble |
| RFP | request for proposal |
| SDC | System Development Corporation |
| SMS | Shuttle Mission Simulator |
| SPS | support processing system for NAS |

This paper is adapted from invited lectures given in Washington, D.C., at an IEEE/DOD Electronics and Aerospace Systems Conference in 1980 and a George Washington University Colloquium in 1981.

INTRODUCTION

In 1977, after two years of in-house studies, the National Aeronautics and Space Administration (NASA) funded two studies to assess the feasibility of developing a computer to improve aerodynamic design processes and research in the physics of fluid dynamics phenomena. The goal was to improve preliminary aeronautical design, increase efficiency of wind-tunnel testing, and reduce design time, cost, and risk. Such a computer was eventually determined to require a speed of one billion floating point operations per second and a memory of at least 240 million words. The two studies showed that such a computer was economically and technically feasible and NASA proceeded with developmental plans. The computer was named the Numerical Aerodynamic Simulator (NAS).

To help insure that the estimated cost, scope, and schedule were realistic, a brief study was made of past large scientific computers. Large discrepancies between inception and operation in technical scope, cost, or schedule were studied so that they could be minimized with NAS. The main computers studied were ILLIAC IV, STAR 100, the Parallel Element Processor Ensemble (PEPE), and the Shuttle Mission Simulator (SMS) computer. Comparison data on memory and speed were also obtained on the IBM 650, 704, 7090, 7094, 360-50, 360-67, 360-91, and 370-195; the CDC 6400, 6600, 7600, CYBER 203, and CYBER 205; CRAY 1; and the Advanced Scientific Computer (ASC). A few lessons learned conclude the report.

The Numerical Aerodynamic Simulator (NAS) will be an important part of an effort to reverse a declining leadership role by the United States in both aeronautics and large scientific computers. Aircraft fuel efficiency, balance of international trade, and military posture will be affected.

COMPUTATIONAL AERODYNAMICS

The proposed Numerical Aerodynamic Simulator (NAS) would be used primarily for aeronautical research and development in computational aerodynamics, although it would also be available to support other disciplines of interest to NASA. Computational aerodynamics is the simulation of aerodynamic flow fields through the numerical solution of fluid dynamic equations by using high-speed computers. This field has been essential in the solution of many aerodynamic design problems associated with commercial, general, and military aircraft. The main disciplines comprising computational aerodynamics are aerodynamics, fluid physics, mathematics, and computer science. NAS would be primarily used for basic research, preliminary design, configuration refinement and optimization, and design verification. Research would be conducted mainly in the physics of fluid dynamics phenomena, particularly concerning boundary-layer transition, turbulence, flow separation and attachment, and aerodynamic noise.

The goal in preliminary design would be to better define initial designs before committing to costly and time-consuming wind-tunnel tests. Because actual flight tests are extremely expensive, as much design and verification work as possible has been conducted in wind tunnels in the past. However, with rapidly rising electrical costs and increasingly complex configurations, greater emphasis must be placed on optimizing wind-tunnel usage. This optimization can occur through greater use of computational aerodynamics, particularly appropriate since computational costs have so greatly decreased over the past several decades. For a given mission, feasible design concepts would be explored by the computer to select a fewer number of most promising candidates. These candidates would then be further studied in wind-tunnel experiments. From these experiments, and any subsequent refinements, the best design would be chosen for implementation. The use of computational aerodynamics also improves the likelihood that ranges initially chosen for design parameters are optimum.

As discussed in Reference 1, configuration refinement and optimization are important uses of computational aerodynamics. Applications, however, have generally been limited to simple physics and isolated three-dimensional components, such as wings, nacelles, and fuselages, in limited flight regimes or to more complex physics but restricted to two-dimensional flows. Figure 1 shows the development of computational aerodynamics from the 1960's to the 1990's. Successive levels of approximations to the Navier-Stokes equations, computed aerodynamic results, and computer class for practical three-dimensional engineering computations are given. Application to more complex three-dimensional cases concerning complete aircraft design optimization or performance prediction under both cruise and maneuver conditions requires substantially more computational power than is available in 1981. The computational power required for this capability is given in Figure 2 and would be satisfied by NAS. The speed required is one billion floating point operations per second for an average sustained rate and for a 64-bit word size. The memory required is 200 million words of block addressable memory plus 40 million words of random access memory.

Figure 3 relates these memory and speed requirements for NAS with those for current large computers and with various levels of aeronautical design capability. Figure 4 (adapted from References 1 - 3) gives the relative computational cost for computer simulation of a given flow for these and earlier computers and gives the number of wind-tunnel test hours for various aircraft since the Wright Flyer. As shown, for the past 50 years the number of wind-tunnel test hours for an aircraft has increased by three orders of magnitude, from approximately 50 hours to over 50,000 hours. Excluding the latest electrical-power price rises, costs for these wind-tunnel tests have correspondingly increased from a few thousand dollars to nearly \$100,000,000. At the same time, however, computational costs have decreased by four orders of magnitude; the computational cost using NAS in the mid-1980's would be about four orders of magnitude less than that for the IBM 650 in the early 1950's for the same problem.

The Numerical Aerodynamic Simulator (NAS) is important in any continued world leadership role by the United States in civil and military aviation. Use of NAS will improve U.S. aircraft fuel efficiency, military posture, and balance of international trade. The latter is particularly important in that aeronautics and large computers are two of the few areas in which this country still has a favorable balance of trade. Yet, even that balance is changing. As detailed in Reference 4, a workshop of 60 experts sponsored by the National Research Council of the National Academy of Sciences recently expressed concern that the United States is in danger of losing its dominant world position in the aircraft industry because of eroded momentum in aeronautical technology. If the United States does not maintain and improve its aeronautical technological capabilities, then steadily gaining foreign competition might surpass this Country in aeronautical leadership during the decade of the 1980's. As noted in the Council's report on NASA's role in aeronautics, the United States recently lost 20 percent of the commercial transport market to European competitors.

A similar reversal is occurring in large computers. For example, in April, 1981, Japan's federal budget included funds for their National Aerospace Laboratory to build a computer that is comparable to NAS. As described in Reference 5, this computer was just one of three new programs in Japan's efforts to overtake the United States in world leadership of the computer industry. Japan's Ministry of International Trade and Industry (MITI) has budgeted as much as \$150M for this computer.

NUMERICAL AERODYNAMIC SIMULATOR

As detailed in Figure 5, the Numerical Aerodynamic Simulator (NAS) Processing System contains a Flow Model Processor (FMP) and a Support Processing System (SPS). The FMP will consist of a high-speed computing engine capable of a sustained rate of one billion floating point operations per second (FLOPS), 40 million words of random access main memory, and 200 million words of block addressable secondary memory. The Support Processing System (SPS) will consist of general-purpose processing systems; data input/output, storage, and manipulation; user interface; and operational management required to support the FMP.

The SPS will provide two billion words of on-line file storage and 100 billion words of off-line storage. The computer will be housed in a 60,000 net sq.-ft. (5,600 sq.-m.) building at NASA, Ames Research Center, Moffett Field, California. Other laboratories in the government, industry, and university communities will have access to NAS. A conceptual sketch of NAS and approximate cost percentages are given in Figure 6.

Between 1975 and 1979, several in-house and contracted studies concerning NAS were conducted. These studies found that, based on new architectural concepts and early 1980's electronic components, NAS was technically and economically feasible. Between 1980 and 1981, the processing system design will be defined, to be followed by detailed design, fabrication, test and integration. The computer is expected to be operational by October 1986. Additional information on NAS can be found in References 1 - 3 and 6.

Important endorsements for NAS have come from numerous advisory groups, including the Aeronautics and Space Engineering Board (ASEB), the Aeronautics Panel of the Aeronautics and Astronautics Coordinating Board (AACB), and the NASA Advisory Council. Further, representatives of the aircraft industry, Department of Defense (DOD), universities, and other NASA centers have participated in defining NASA requirements.

COMPUTER COMPARISONS

Introduction

To help assess the realism of the estimated cost, schedule, scope, and problems for NASA's proposed new computer complex NAS, a brief study was made of several large scientific computers built over the past fifteen years. The purpose of the remaining paper is to summarize that study. How accurately did initial estimates agree with the final cost, schedule, and product? What might be learned from these past projects with respect to problems, constraints, uniqueness, motivators, usage, procurement plans, and technology advances that might be helpful in meeting NAS targets? Cost concerns included comparison of final cost with respect to initial estimates; percentage of funds spent on studies, planning, design, software, hardware, and facility; and constraints. Interest in acquisition plans included in-house versus contracted efforts, types of contracts, and use of "systems houses."

Computers for the study were selected based on their range of identification with these concerns and on the availability of data. The computers chosen are listed in Figure 7. Besides NAS, the computers selected were the ILLIAC IV at NASA, Ames Research Center, in Moffett Field, California; Parallel Element Processor Ensemble (PEPE) at the Army Advanced Ballistic Missile Defense Agency (ABMDA) site in Huntsville, Alabama; the Shuttle Mission Simulator (SMS) computer at NASA, Johnson Space Center, in Houston, Texas; and STAR 100 at the Lawrence Livermore Labs (LLL) in Livermore, California. The time periods given range from start of initial studies to completion of initial objectives (some level of computer operation).

Note that much of the data given must be considered as best estimates. Many of the key sources for at least some of the computer development or construction information were not available. Therefore, some information is based on memory or unofficial records. Costs often were not budget line items in the agencies congressional submittals; for example, for PEPE and STAR 100. Therefore, all costs have not necessarily always been totaled for each

computer; some elements might be missing and some costs are unknown. For example, some STAR 100 costs were absorbed by Control Data Corporation. The amount has never been made public. In addition, one or more of the designs, specifications, contractors, and funding agencies might have changed over time; for example, contractors for PEPE changed from Bell Labs to Burroughs to Honeywell back to Burroughs and funding agencies for ILLIAC IV went from the Advanced Research Project Agency (ARPA) to ARPA plus other government agencies. Cost analyses also depended in part in which phase the source was involved. If the source primarily worked only hardware, his estimates of software might not have been as reliable. Finally, costs were not always separated for design, hardware, and software; for example, the SMS computer, PEPE, and ILLIAC IV. Therefore, cost comparisons among computers were more difficult.

There were also other differences that made comparisons among computers difficult. Tasks that were contracted out for some computers were done in-house for others. For example, software was developed in-house for STAR 100, by a systems house for PEPE, and by the same contractor that integrated the computer into the SMS Complex for the Space Shuttle Mission Simulator. Further, contract procedures varied from direct to indirect. For example, ILLIAC IV was subcontracted for through a university, PEPE was procured through a systems-house intermediary, and NAS will be contracted for directly. Acquisition plans differed. ILLIAC IV was procured by a cost-plus-fixed-fee (CPFF) contract that was shifted to cost sharing after several cost overruns and schedule delays. STAR 100 was procured under a fixed-price (FP) contract; PEPE, under a CPFF contract with a not-to-exceed clause restricting total cost. For the SMS computer, a FP contract was used for basic hardware, whereas a cost-plus-award-fee (CPAF) contract was used for software, frame job, and integration. The NAS is expected to be procured under some type of cost award or cost sharing contract.

The computers had different main components. For example, PEPE had limited memory, the SMS was a real-time computer, and NAS will have a huge

memory and extremely fast speed. Further, different constraints governed construction. For example, ILLIAC IV was constrained by schedule. Therefore, when problems occurred, cost overran. On the other hand, PEPE was constrained by cost. When problems occurred, scope was adjusted; the number of processing elements (PE) was reduced from 36 to 11. However, in this particular reduction, quality and main objectives did not suffer.

As illustrated in Figure 8, the U.S. Government played an important role in advancing computer capability from the mid-1940's with ENIAC to the late 1960's with ILLIAC IV when ILLIAC IV was initially being designed for use in anti-ICBM control. This historical government role terminated about that time. One reason might have been large cost overruns incurred by ILLIAC IV. The initial cost estimate for ILLIAC-IV hardware and design was about \$8M (\$8,000,000). An intermediate estimate was \$22M - \$24M. The actual, final cost, including a small amount for software specifications, was approximately \$50M. This large overrun was due primarily to ILLIAC-IV development being driven by computer-research, rather than application (or non-computer research), interests. After the justification for ILLIAC IV changed from anti-ICBM control systems, ILLIAC IV primarily became a research and development tool for the purpose of understanding parallel processors. The new main objectives were for the ILLIAC IV to demonstrate successfully the value of parallel array processing, to enable the development of appropriate software, and to evaluate the usefulness of parallel processing for various user applications. As such, the technical requirements and immediate objectives were continuously evolving and cost and schedule suffered.

However, unlike ILLIAC IV, most computers are application driven. They are specifically developed to advance the state of the art in areas of research other than the computer itself. Therefore, it is unfortunate that many government agencies have used the ILLIAC-IV cost overrun as a major reason not to develop more computers. Instead, these agencies lease or purchase only "off-the-shelf" equipment, even though their needs are application, rather than computer-research, driven.

ILLIAC IV

In 1966, the Department of Defense, Advanced Research Projects Agency (DARPA), subcontracted to Burroughs through the University of Illinois to begin final design and construction of the ILLIAC IV. The ILLIAC IV was designed to be a high-speed, state-of-the-art processor based on the concepts of parallel architecture, an array memory, and very high transfer rates between the memory and computational units. The main objective was to demonstrate the usefulness, efficiency, cost effectiveness, and versatility of parallel array processing. Thus, ILLIAC IV was an R&D tool to study parallel processors. Under an interagency agreement on sharing of further cost and usage (about 80 percent ARPA and 20 percent NASA), ILLIAC IV was delivered in 1972 to NASA's Ames Research Center, a leader in computational fluid dynamics (CFD). In 1973, ILLIAC IV was put into limited operation and by July, 1976, the essential initial objectives were achieved. In addition to computational fluid dynamics (CFD), ILLIAC IV is useful for problems in atmospheric modeling, weather prediction, fluid dynamics, and radar signal processing.

ILLIAC IV has 64 processing elements (PE's), each capable of executing the same instruction at the same time. Each PE has 2,048 64-bit words of local memory. The working storage, therefore, is essentially comprised of an array of 64 columns, one for each processing element, and 2,048 rows for a total capacity of over 130,000 64-bit words. A vector consists of up to 64 elements with each element in the memory of a different PE. When operating on vectors, the computer is capable of over 40 million floating-point operations per second.

The main memory had a design capacity of about 16 million 64-bit words or 32 million 32-bit words, of which 8 - 12 million 64-bit words have been operational. The disk transfer rate is 500 million bits per second. ILLIAC IV is dedicated to the execution of user code. The operating system support and utility functions are performed by a set of processors, large central memory, and interface devices which together are called the Central System.

ILLIAC IV performs the usual scalar operations by utilizing only one processing element. It does not have separate scalar hardware. References 7 and 8 provide additional information on ILLIAC IV.

Designed and built by Burroughs Corporation, ILLIAC IV was initially planned to be four times larger than its current size and have a speed of up to 1/2 billion operations per second. However, cost escalations and schedule delays arising from developmental problems in memory and logic circuits resulted in the smaller version. A cost-plus-fixed-fee (CPFF) contract was initially awarded to Burroughs. After several cost overruns and schedule delays, however, the contract was changed to cost sharing. In 1971 NASA joined DARPA in funding ILLIAC IV. The total cost for hardware/software design, development, test, and integration was approximately \$50M (\$50,000,000). This cost was roughly divided into 1 percent for performance specifications, 15 percent for systems software and user interface software, and the remaining 84 percent for hardware. NASA also spent about \$1.5M for a facility to house ILLIAC IV. ILLIAC IV was separately listed as a line item in the congressional budget submittal by ARPA, but not by NASA.

STAR 100

One year after ILLIAC IV was put into limited operation at NASA's Ames Research Center, the first Control Data Corporation (CDC) STAR 100 was delivered in 1974 to Lawrence Livermore Laboratories (LLL) in Livermore, California. The STAR 100 has a memory of about one million 64-bit words or twice as many 32-bit words. When operating in the 32-bit mode, STAR 100 can achieve over 100 MFLOPS. If a problem is about 95 percent vectorized, the STAR 100 is about three to four times faster than a CDC 7600.

The Central Processing Unit (CPU) of the STAR 100 consists of two pipelines. Vectors whose length is a multiple of eight are the most efficient. Unlike ILLIAC IV, the elements of vectors must occupy contiguous locations. On the other hand, there are no sharp discontinuities in result rates for

STAR 100 as there are for ILLIAC IV. For example, operations on vectors of length 65 for ILLIAC IV would take almost twice as long as for vectors of length 64, since there are only 64 processing elements. Unlike ILLIAC IV, STAR 100 has separate scalar hardware. However, the scalar performance of STAR 100 is relatively poor; it is only about one-fifth that of a CDC 7600 and, hence, about equal to that of a CDC 6600. Further information on STAR 100 can be found in References 8 and 9.

The STAR 100 was both computer-research (for pipeline processors) and application driven. It was built for the Atomic Energy Commission (AEC) primarily for weapon studies which involved coupled partial differential equations. The AEC awarded a fixed-price contract for \$24M to CDC. In addition, unknown costs were absorbed by CDC. STAR 100 was not a congressional budget line item for the AEC. About 70 percent of the AEC's \$24M cost went to design and construction of hardware. The remaining 30 percent went to systems and user interface software. The STAR 100 was housed in an existing building; hence, there was no major facility cost.

Shuttle Mission Simulator Computer

As illustrated in Figure 9, the Shuttle Mission Simulator (SMS) digital computer complex services two Space Shuttle crew stations simultaneously for both on-orbit and transition flight training. This computer complex consists of a number of interconnected computers. Of these, the main computer is a Sperry UNIVAC 1100/46. This host computer contains a majority of the mathematical models for simulation of motion, sound, aerodynamics, visuals, and instruments. The computer makes a real-time solution of most of these mathematical models. Changes in the software of the operating system were required for these real-time solutions. In addition to simulation support, the UNIVAC 1100/46 provides terminal and batch operations for analysis and simulation modification.

The UNIVAC 1100/46 is a central processing unit consisting of six command arithmetic units (CAU's), the equivalent of the instruction processing portion of a CPU. It has three input/output access units (IOAU's) which control all transfers of data between the peripheral devices and memory. The UNIVAC 1100/

46 has a 36-bit word length and can execute approximately two million operations per second of an average simulation mix. It has two levels of solid-state memories. Each memory has close to 525,000 36-bit words. References 10 through 13 contain additional information on the Shuttle Mission Simulator Computer Complex.

NASA's Johnson Space Center (JSC) issued a request for proposal (RFP) to major computer companies to provide a computer system with hardware and software features to accommodate the SMS simulation. Under a fixed-price (FP) contract, JSC selected Sperry-Univac's proposal to take an off-the-shelf UNIVAC 1100/46 and modify it for a special real-time clock, other special timing, and about 20 percent of the operating system. The UNIVAC 1100/46 was then delivered on site. The Link Division of Singer was then given the UNIVAC 1100/46 as government furnished equipment (GFE) and a cost-plus-award-fee (CPAF) contract to develop all applications and systems software except the standard compilers and do the frame job. As part of this contract, Singer-Link also integrated the resulting computer with data-gathering mini computers, simulation interface devices, flight computer systems, digital image generation computers, and various other interface, input/output, and peripheral equipments.

This main-computer portion of the SMS Computer Complex cost \$7.9M in the mid-1970's. Of this amount, about 15 percent went to design, 77 percent to hardware, and 8 percent to systems and user interface software. Since design and non-application software were included in the fabrication contract, these percentages had to be estimated. In addition, \$3.2M was spent for applications software and \$450K was spent for two sizing studies. One contract was to study the computer for memory and speed while estimating the size of the basic simulator. The other contract was simultaneously to study the basic simulator while estimating the memory and speed required in the computer. The two studies differed only by about 10 percent in estimating computational requirements. Both the \$3.2M applications software and \$7.9M main-computer expenses were out of a \$60M total cost for the Shuttle Mission Simulator. This computer complex was a line item in the congressional budget submitted from NASA. No facility was needed in addition to the SMS Complex.

PEPE

The ILLIAC technology updated for the use of high-speed emitter-coupled logic circuits was used to develop a special-purpose computer PEPE (Parallel Element Processor Ensemble). Burroughs designed and built this computer for the Army Ballistic Missile Defense Advanced Technology Center (BMDATC) for research on ballistic missile defense systems. PEPE combines associative and highly parallel techniques for ballistic-missile-defense data processing. PEPE's architecture is comprised mainly of disconnectable, simple processing elements (PE's) which are repeatedly replicated.

Although PEPE was built with only 11 PE's, it can support up to 288. (The number 288 is a physical, and not a theoretical, limitation.) There is no direct communication between processing elements; all communication occurs through the control console. Therefore, failure in any one element affects neither the remaining hardware nor the software. The PEPE system configuration, with a CDC 7600/7700 as a front-end, host computer, is illustrated in Figure 10. Figure 11 gives additional information on the control console and processing elements. As shown, the control console has three control units, one each for input (Correlation Control Unit - CCU), calculation (Arithmetic Control Unit - ACU), and output (Associative Output Control Unit - AOCU). Each control unit has separate program and data memories. Each processing element consists of a memory and three units, the correlation unit (CU), arithmetic unit (AU), and associative output unit (AOU), corresponding to respective units in the control console.

Radar information is broadcast by the CCU to all CU's in the PE's simultaneously. In each PE, the CU compares the characteristics of each radar return with the characteristics of tracked objects held in memory to determine which input units should accept the radar data. Input is made to those CU's where correlation occurs between the stored and broadcast data. In the event of no association with an existing object, an empty PE is activated by the CU. Output information sent to the radar is handled by the AOU's under the control of the AOCU after the files are updated by the AU's and transferred to memory for access by the AOU's. Program memories in each of the control units allows the PEPE ensemble to operate concurrently with the host computer.

Each processing element (PE) has 2,048 32-bit words of memory for storage of operands and intermediate results. In the double-precision mode, each word is 64-bits long. Speed for the arithmetic unit is one million operations per second or 11 million operations per second for the 11 PE's. Execution rate for input and output units is five million operations per second for each PE. Additional information on PEPE can be found in References 9 and 14 through 17.

Excluding initial studies, application software, and building, PEPE cost \$14.5M between 1969 and 1976. About 28 percent of this amount went to planning and design; 12 percent to systems and user interface software, and the remaining 60 percent to hardware. Systems Development Corporation (SDC) was awarded a cost-plus-fixed-fee (CPFF) contract with a not-to-exceed (NTF) clause restricting total cost. Acting as a systems house, SDC then subcontracted to Burroughs for the hardware. However, SDC acted as prime contractor on software. In addition to the \$14.5M, approximately \$3M was spent on initial studies. PEPE used an existing building. Therefore, no facility funding was required. PEPE was not a line item in the agency's congressional budget submittal.

Summary

Figure 12 gives summary comparisons of five computers ILLIAC IV, STAR 100, PEPE, SMS computer, and NAS. Pie charts show the approximate cost percentages spent on design, systems software, hardware, and reserve. Estimated costs for each project, excluding initial studies, application software, and building, are given. Time periods from initial studies to completion of initial objectives are shown. Contract type, funding agency, and main usage are also shown.

The important driver (computer-research versus application or non-computer-research) is noted at the top of Figure 12. After an anti-ICBM control system was eliminated as a driver for ILLIAC IV, the main driver became computer research for parallel processors. Since the mid-1970's, NASA has primarily used ILLIAC IV for research in computational fluid dynamics. The STAR 100 was built for weapon studies, primarily concerned with coupled partial differential equations, and, in part, as an R&D tool for pipeline processors. As discussed, ILLIAC IV greatly exceeded estimated cost. The STAR 100 also exceeded estimated cost. However, both application-driven computers, PEPE and the SMS computer, were

built within estimated cost and schedule. The NAS will be application driven. Its primary use will be in aeronautical research and development. Some time will also be made available for other disciplines, such as weather and climate modeling, computational chemistry, and computational astrophysics.

LESSONS LEARNED

Several facts emerged from this brief study. The first was that mission success in acquiring a new super computer within initial technical scope, cost, and schedule was dependent not only on whether existing, proven technology was used, but also on whether the computer was driven by computer research or non-computer, application research. As Figure 12 illustrated with ILLIAC IV versus STAR 100 versus the SMS computer, PEPE, and NAS, the more a computer was motivated by computer research (e.g., ILLIAC IV to study parallel processors), the more likely cost overruns, schedule slippages, and technical changes were to occur.

No one mode of acquisition appeared favored. Each mode had advantages and disadvantages. Under a fixed-price contract, the project cost is not exceeded and the fabricator is allowed the most freedom. A disadvantage is that the result might not be of the highest quality. (But is the highest quality always needed?) To fabricate the computer within allocated funds, a company might shortcut some steps. Optimal usage of this procurement mode is made by not allowing change orders that require cost increases or schedule delays; specification stability is essential. The advantage to the fabricator is freedom from continuous monitoring by the procurer; the disadvantage is the financial constraint. Under one of the cost-plus-fee type contracts, the procurer will get the desired computer results but at a greater risk in cost overruns and schedule changes. To be successful, such a contractual arrangement must be monitored closely, such as weekly. Such close monitoring requires that the procurer must have and then commit the necessary in-house manpower from his organization. The advantage to the fabricator is the ability to fabricate a quality product without having to absorb any costs. The disadvantage is limited freedom and secrecy. Successful use of a systems-house intermediary depends on the particular systems house, procurer, and subcontractors to the systems house. Results have ranged from excellent to poor. The main drawback to the procurer is less direct control of the fabricator.

Another result from the study is that high-order languages, such as FORTRAN instead of machine language, should be required. High-order languages are easier for the procurer to understand and they reduce the cost otherwise required for big compilers. There is a greater assurance of high-order languages working. These languages also minimize programming changes and modifications and they are easier for eventual users.

If possible, the computer should be built on site. The procurer would have greater control of results and the problems and extra time involved in disassembly, shipping, and reassembly would be eliminated. Although fabricators will almost always argue that a computer cannot be built on site, it often can. Where the procurer is a government agency, it will achieve best results by cooperating with Government Services Agency (GSA) rules and regulations from project beginning.

Where possible, computer specifications should be written in-house. Where specifications must be contracted out, particular care should be exercised if an academic is used as a prime technical consultant to insure that the consultant has appropriate experience and will not unduly emphasize his current area of research. A computer company should not write the specifications. (At least one has tried and then failed in the Courts.) Finally, inclusion of complex specifications or equipment for which there is a low probability of future need should be minimized. Too often a possible future need of small likelihood drives a large percentage of the total computer developmental cost and schedule.

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FIGURE 1 - DEVELOPMENT OF COMPUTATIONAL AERODYNAMICS

| STAGE | APPROXIMATION | COMPUTED RESULTS | COMPUTER CLASS FOR PRACTICAL 3D ENGINEERING COMPUTATIONS |
|-----------------------------------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|
| INVISCID LINEARIZED (1960's) | VISCOUS AND NONLINEAR INVISCID TERMS NEGLECTED | <ul style="list-style-type: none"> • PRESSURE DISTRIBUTION • VORTEX DRAG • SUPERSONIC WAVE DRAG | IBM 360 CDC 6600 |
| INVISCID NONLINEAR (1977) | VISCOUS TERMS NEGLECTED | ABOVE PLUS: <ul style="list-style-type: none"> • TRANSONIC FLOW • HYPERSONIC FLOW | CDC 7600 STAR CRAY ILLIAC IV |
| REYNOLDS TIME-AVERAGED NAVIER-STOKES (EARLY 1980's) | NO TERMS NEGLECTED: TURBULENT MOMENTUM AND HEAT TRANSPORT TERMS MODELED | ABOVE PLUS: <ul style="list-style-type: none"> • SEPARATED FLOW • TOTAL DRAG • PERFORMANCE • BUFFETING, BUZZ | AT LEAST 40 TIMES CURRENT SUPERCOMPUTERS (NAS) |
| FULL TIME - DEPENDENT NAVIER-STOKES (CIRCA 1990) | SUB-GRID SCALE TURBULENCE MODELED | ABOVE PLUS: <ul style="list-style-type: none"> • AERODYNAMIC NOISE • TRANSITION • SURFACE PRESSURE FLUCTUATIONS | AT LEAST 100 TIMES (NAS) |

COMPUTATIONAL POWER REQUIRED FOR NUMERICAL AERODYNAMIC SIMULATOR (NAS)

SPEED: 1 BILLION FLOATING POINT OPERATIONS PER SECOND FOR AVERAGE
SUSTAINED RATE 64-BIT WORD

MEMORY: 200 MILLION WORDS BLOCK ADDRESSABLE MEMORY +
40 MILLION WORDS RANDOM ACCESS MEMORY (RAM)

FIGURE 2

FIGURE 3 - COMPUTER SPEED AND MEMORY REQUIREMENTS COMPARED WITH COMPUTER CAPABILITIES

SPEED REQUIREMENT BASED ON 15-MIN RUN WITH 1985 ALGORITHMS
 REYNOLDS AVERAGED NAVIER STOKES EQUATIONS

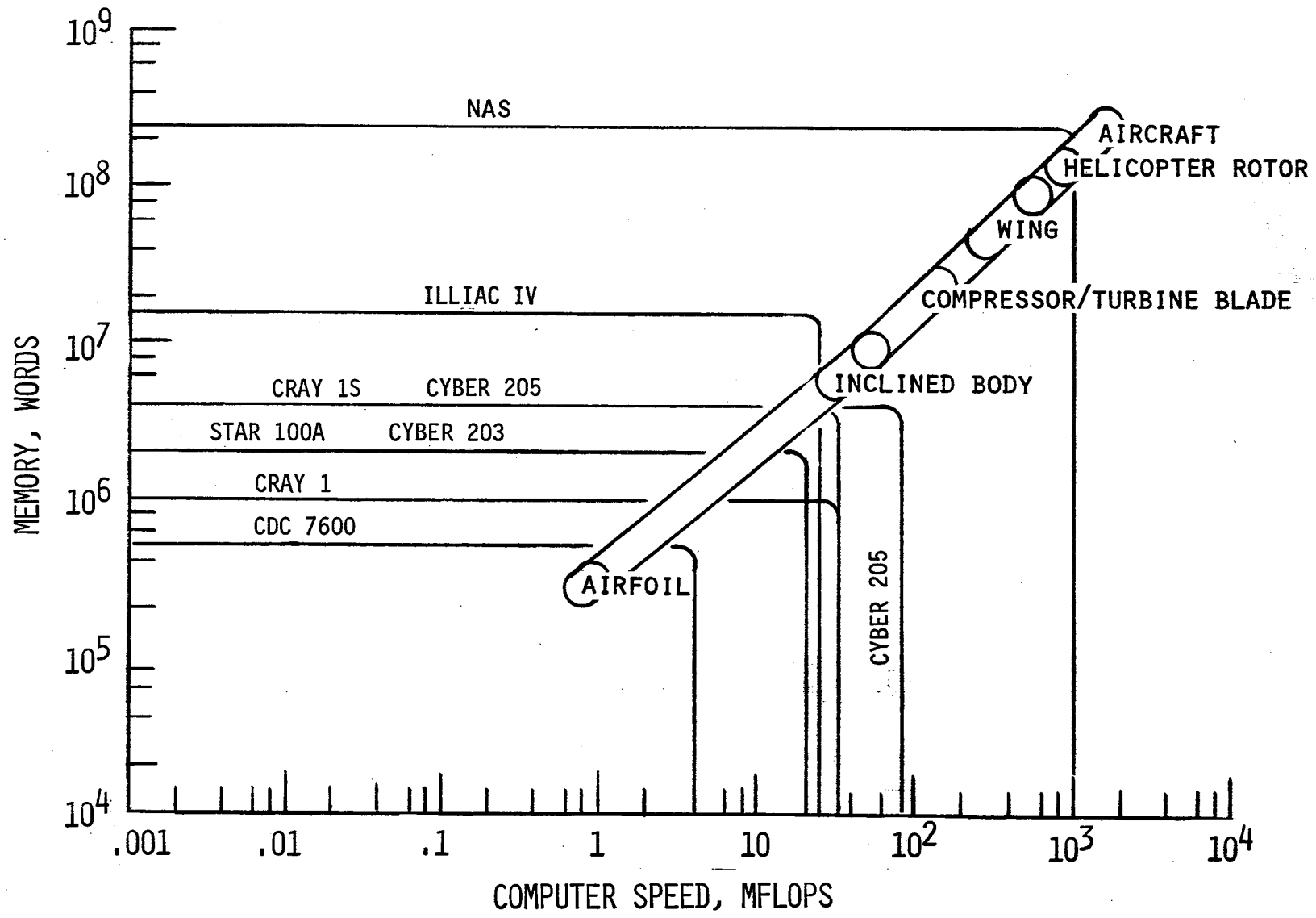
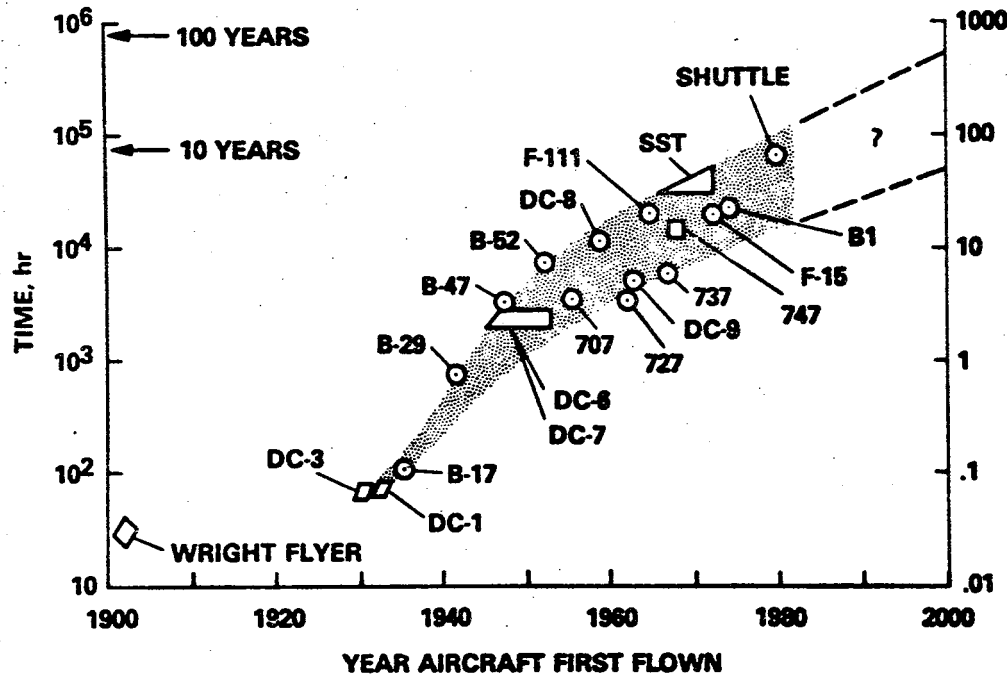


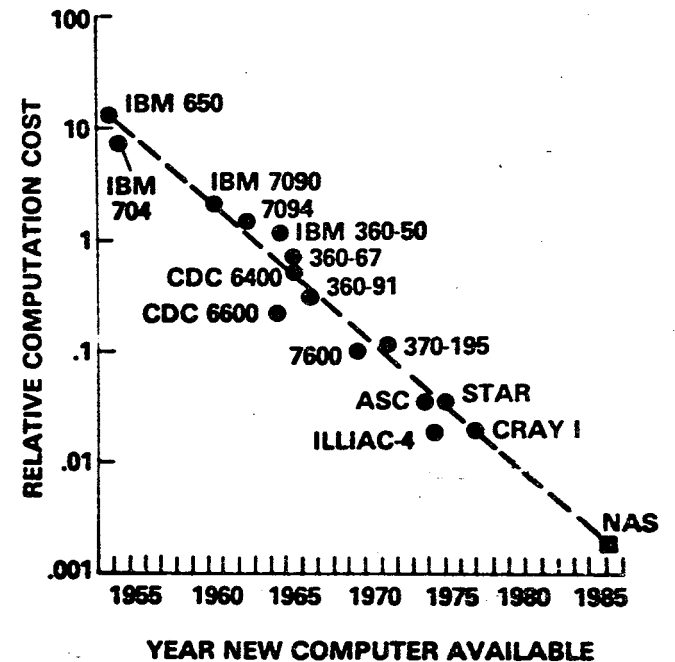
FIGURE 4

TRENDS FOR WIND-TUNNEL USAGE AND COST OF COMPUTER SIMULATION

WIND-TUNNEL TEST HOURS FOR VARIOUS AIRCRAFT



COST FOR COMPUTER SIMULATION OF GIVEN FLOW



NUMERICAL AERODYNAMIC SIMULATOR PROCESSING SYSTEM

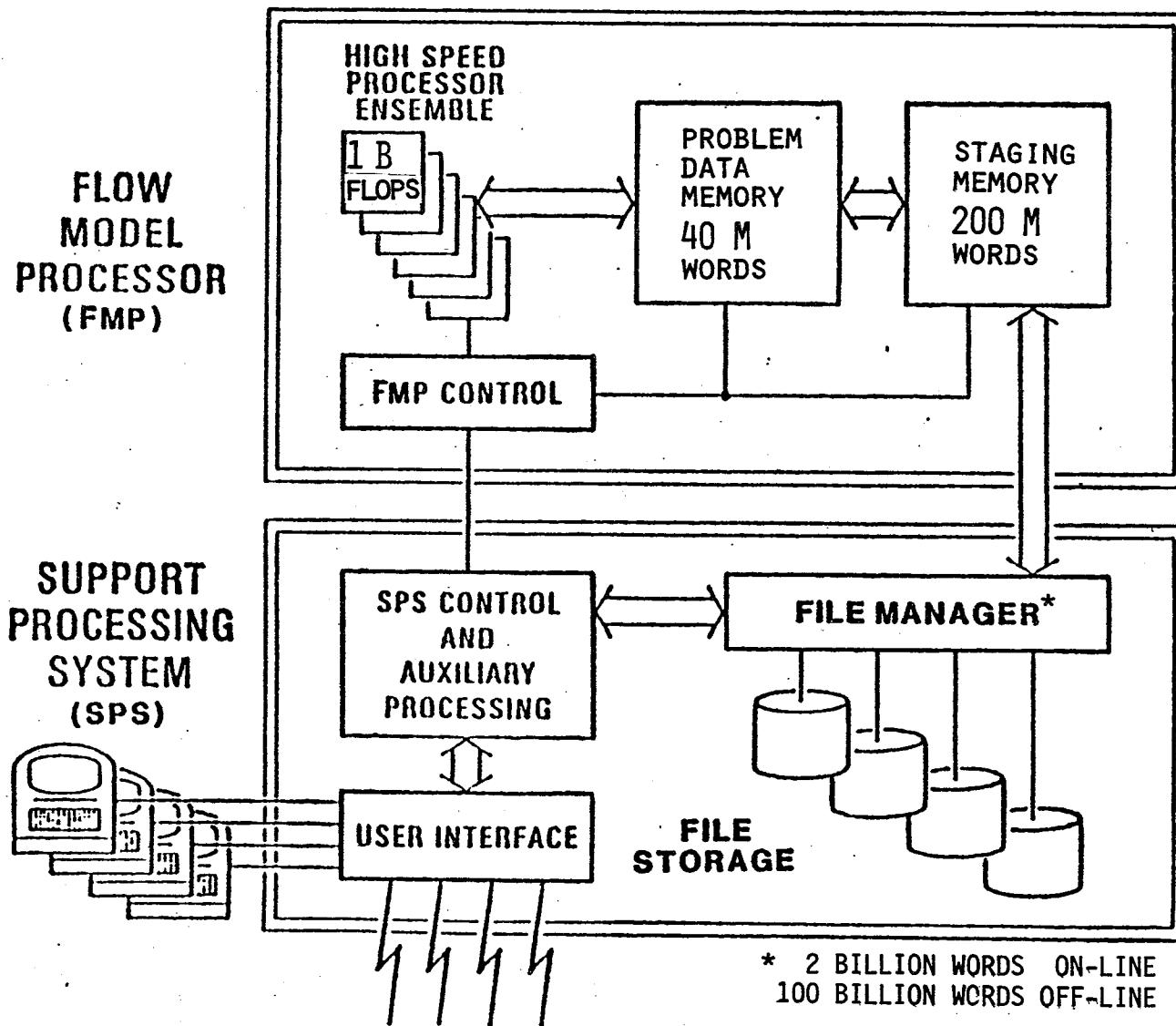
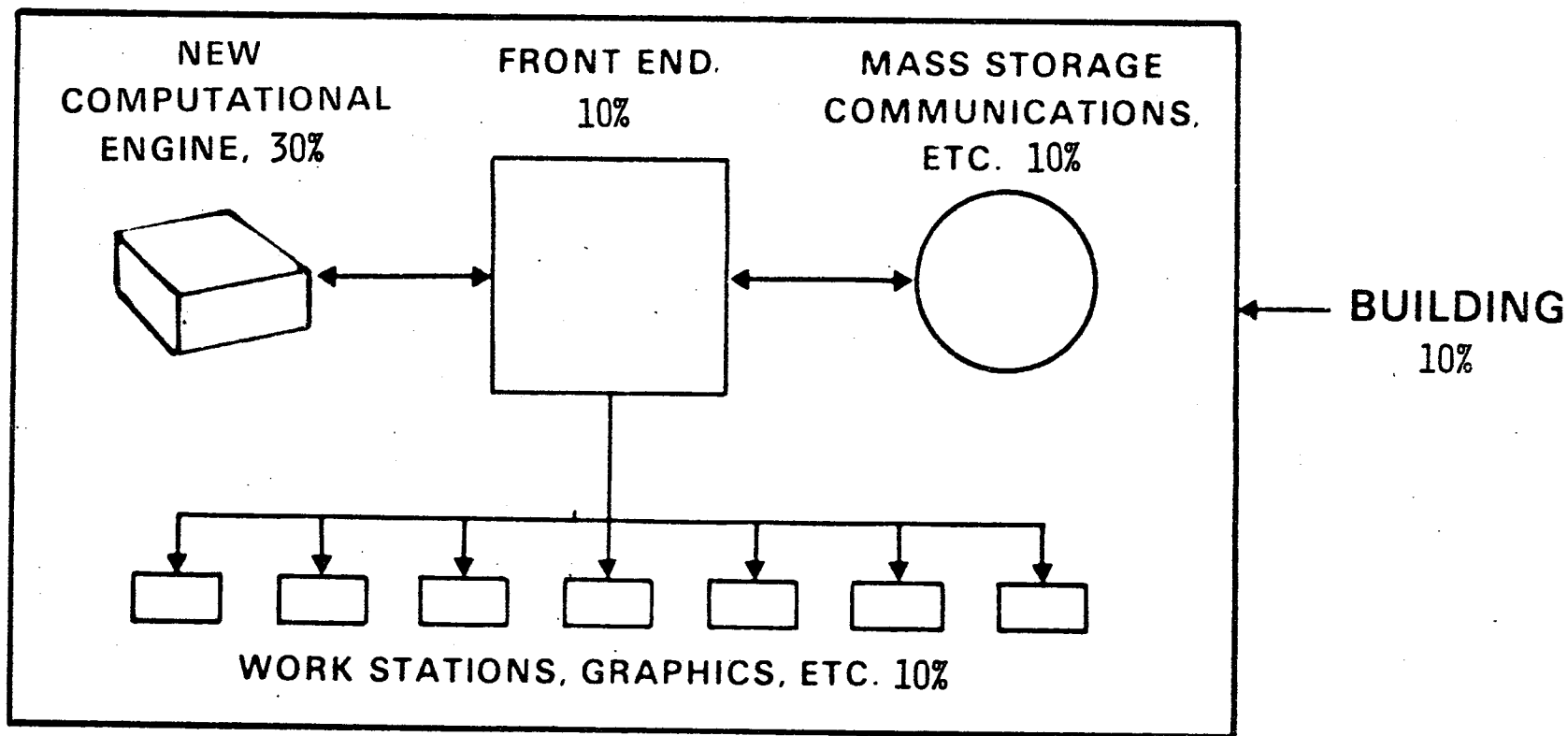


FIGURE 5

FIGURE 6 - CONCEPTUAL SKETCH OF NAS WITH APPROXIMATE COST PERCENTAGES



REMAINING 30% WILL BE DISTRIBUTED AMONG ABOVE ITEMS AND INTEGRATION SUPPORT

OPERATIONAL DATE OCT. 1986

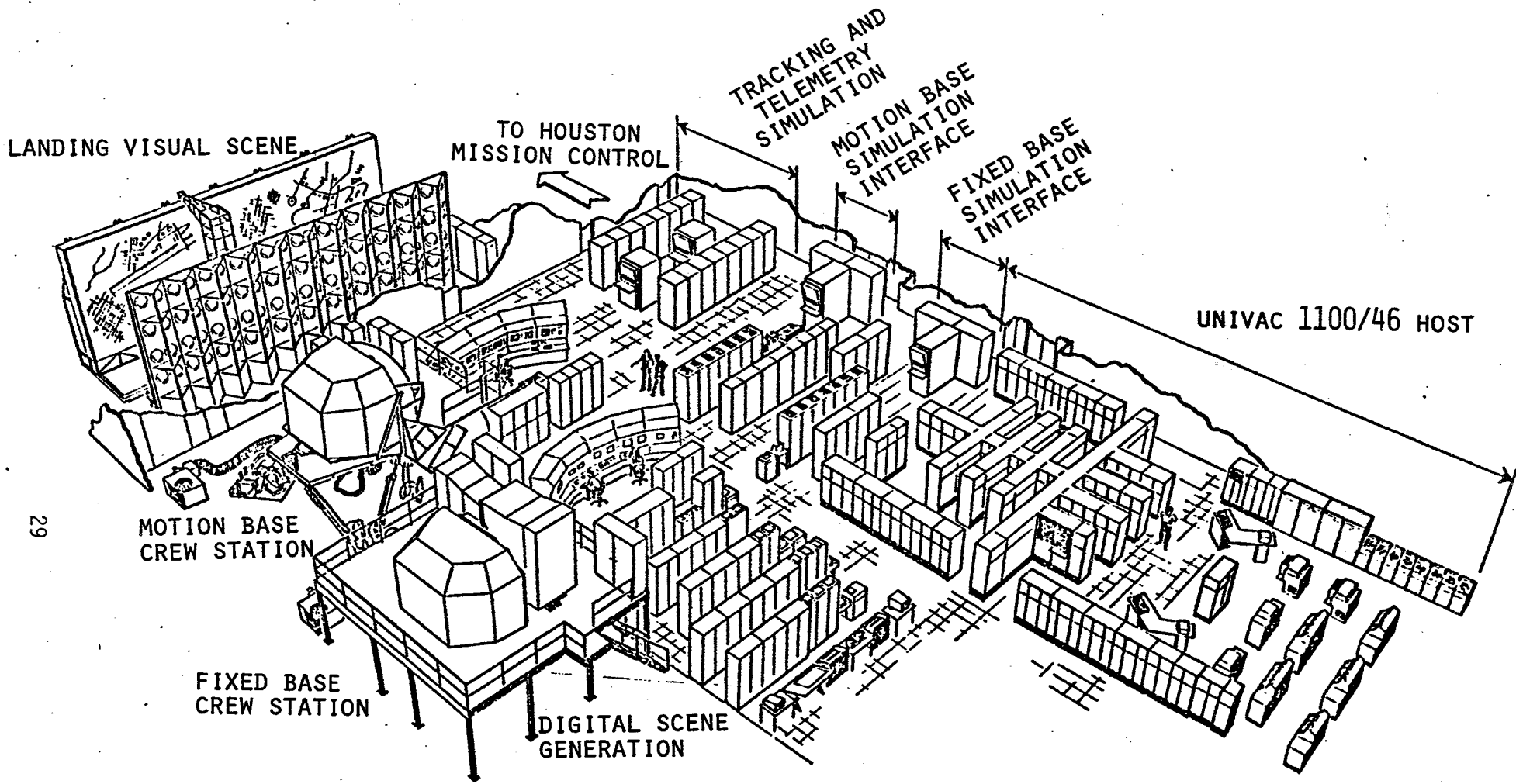
FIGURE 7 - COMPUTERS STUDIED*

| COMPUTER | DATES | LOCATION | |
|-----------------------------------------------|-------------|--------------------------------------------------------------|--------------------------------------------|
| STAR 100 | 1964 - 1974 | LAWRENCE LIVERMORE LABS | LIVERMORE, CALIF. |
| ILLIAC IV | 1965 - 1976 | UNIVERSITY OF ILLINOIS/ NASA, AMES RESEARCH CENTER | URBANA, ILLINOIS/ MOFFETT FIELD, CALIF. |
| PARALLEL ELEMENT PROCESSOR ENSEMBLE (PEPE) | 1969 - 1976 | ARMY ADVANCED BALLISTIC MISSILE DEFENSE AGENCY (ABMDA) | HUNTSVILLE, ALA. |
| SHUTTLE MISSION SIMULATOR (SMS) COMPUTER | 1972 - 1976 | NASA, JOHNSON SPACE CENTER | HOUSTON, TEXAS |
| NUMERICAL AERODYNAMIC SIMULATOR (NAS) | 1975 - 1986 | NASA, AMES RESEARCH CENTER | MOFFETT FIELD, CALIF. |

*based on data availability and range of responses

| <u>TIME</u> | <u>DRIVING NEED</u> | <u>SPONSOR</u> | <u>COMPUTER DEVELOPED</u> | <u>KEY TECHNOLOGY</u> | <u>COMMERICAL FOLLOW-ONS</u> |
|-----------------------|----------------------------------------------------------------|----------------|---------------------------|-------------------------------------------------------|------------------------------|
| MID 1940's (WW II) | MULTITUDE OF BALLISTIC TABLES | BRL | ENIAC | VACUUM TUBE ELECTRONIC COMPUTING | IBM 701 UNIVAC 1 |
| EARLY-MID 1950's | DEW AIR DEFENSE FOR TRACKING BOMBER FLEET | US AF | AN FSQ-7 | MAGNETIC CORE MEMORY | IBM 709 |
| EARLY 1960's | SUPERIOR DESIGN CAPABILITY FOR SMALL NUCLEAR DEVICES | AEC | CDC 6600 | INTEGRATED CIRCUITS | CDC 7600, IBM 370 |
| LATE 1960's | ANTI-ICBM CONTROL SYSTEM (NEED ELIMINATED POLITICALLY) | DARPA | ILLIAC IV | SEMICONDUCTOR MEMORY AND PARALLEL PROCESSING | CDC STAR, CRAY 1 |
| EARLY 1970's | COMPUTER RESCH PARALLEL PROC (LATER: COMPTL FLUID DYNAMICS) | DARPA/NASA | ↓ | | |
| MID 1980's | SUPERIOR DESIGN CAPABILITY FOR AIRCRAFT | NASA | NAS | CONCURRENT PROCESSING ARCHITECTURE | |

FIGURE 8 - HISTORICAL ROLE OF GOVERNMENT AS PRIME DRIVER IN ADVANCING COMPUTER CAPABILITY



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SKETCH OF SHUTTLE MISSION SIMULATOR

FIGURE 9

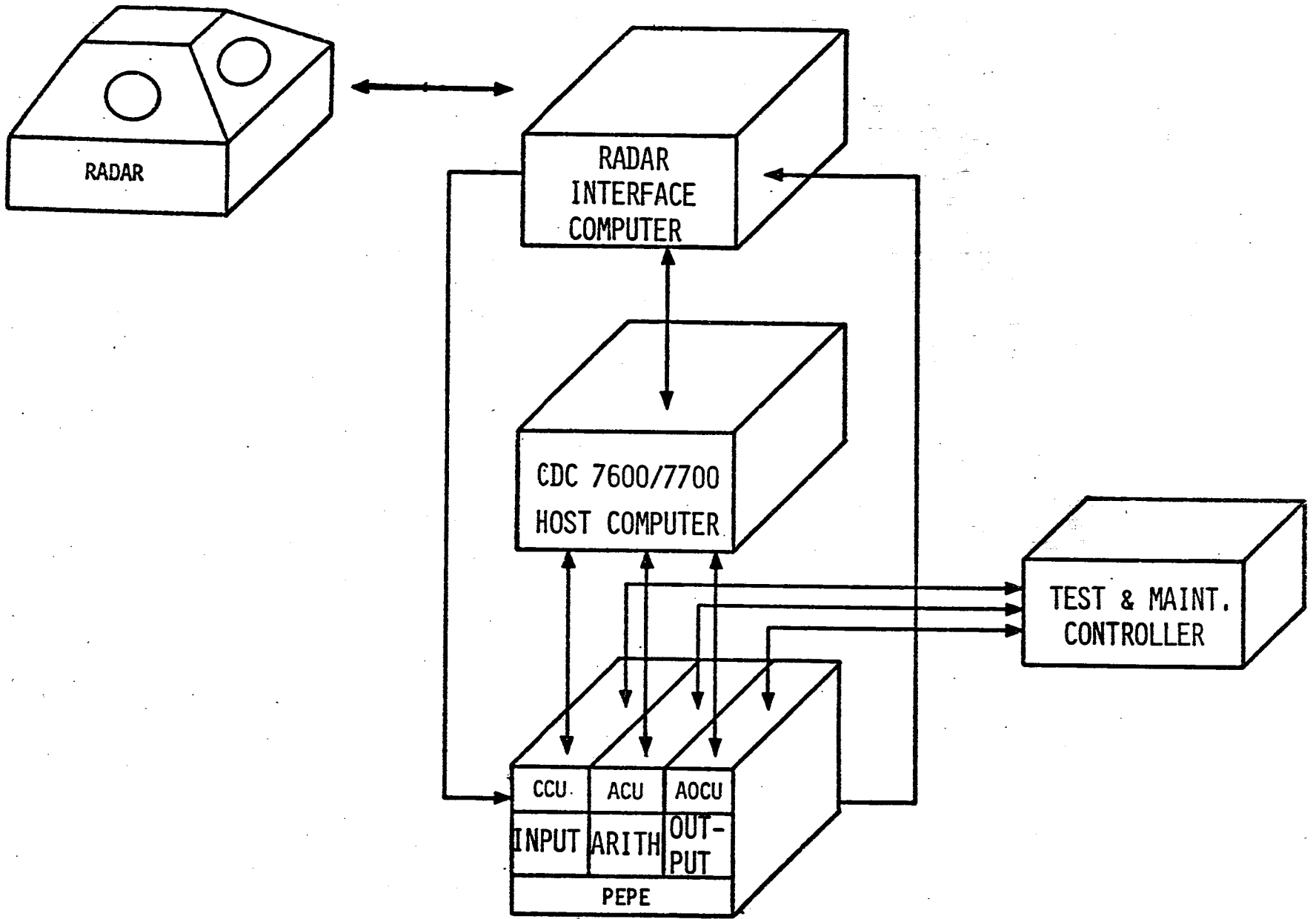


FIGURE 10 - PEPE SYSTEM CONFIGURATION

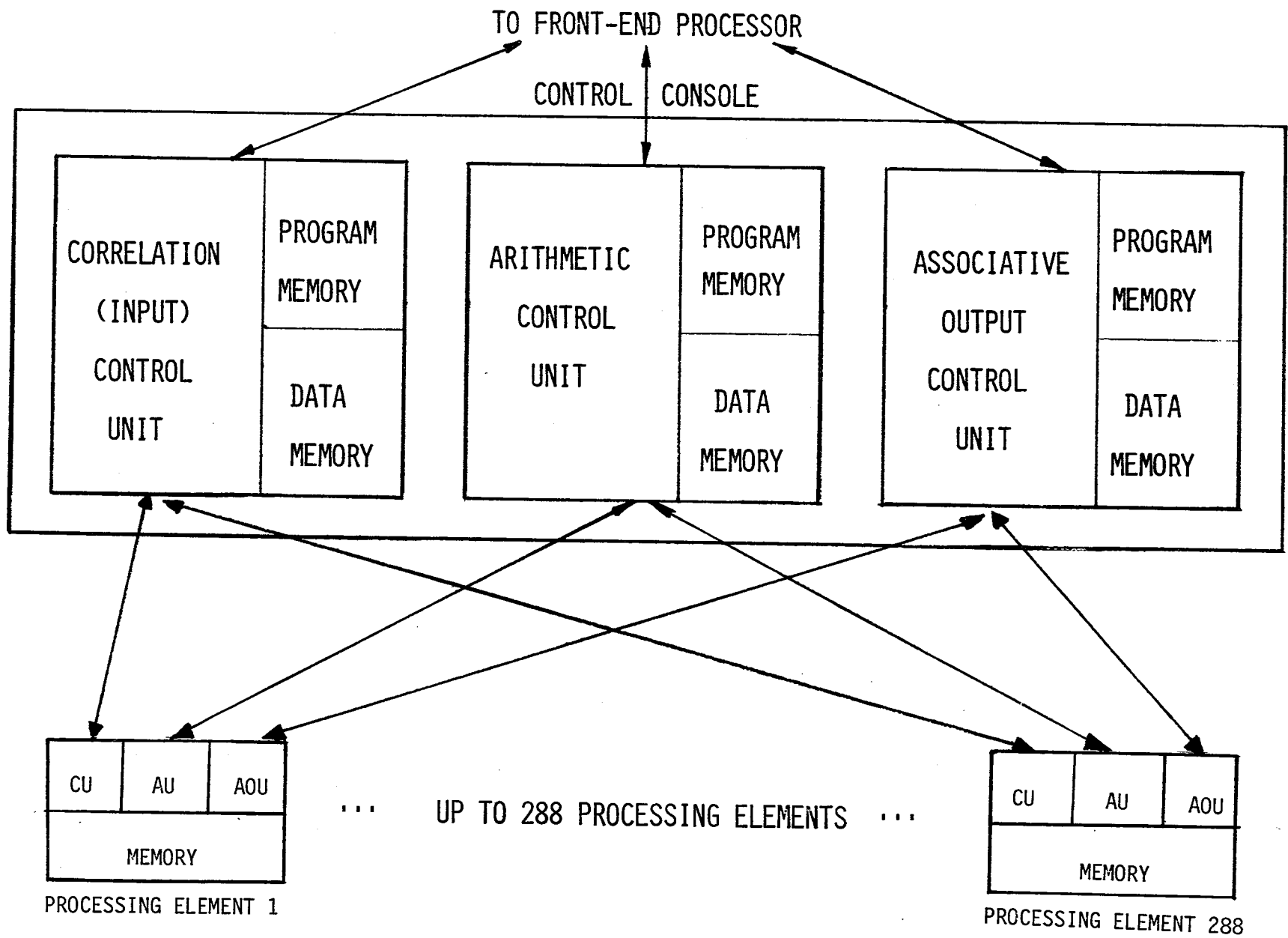
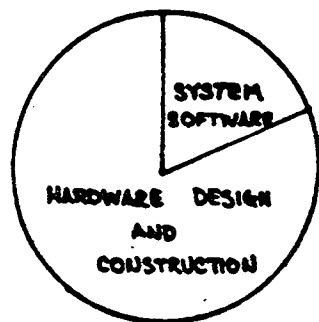


FIGURE 11 - PEPE CONTROL CONSOLE AND PROCESSING ELEMENTS

FIGURE 12 - SUMMARY COMPUTER COMPARISONS



ILLIAC IV



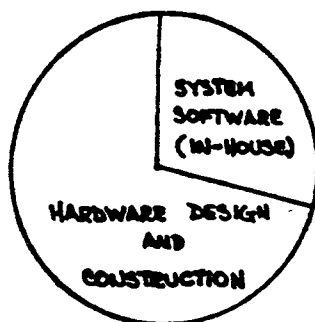
APPROX \$50M*

1965-1976

CPFF → CS
MIX R&D
BUDGET LINE

R&D (PARALLEL
PROCESSORS)
CFD

STAR 100



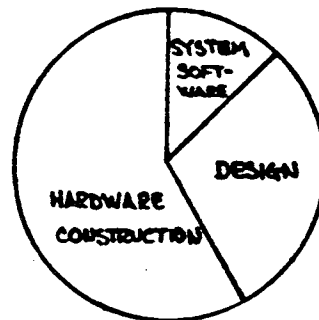
\$24M**

1964-1974

FP
AEC R&D

WEAPON STUDIES
(COUPLED PDE'S)
R&D (PIPELINE PROCESSORS)

PEPE



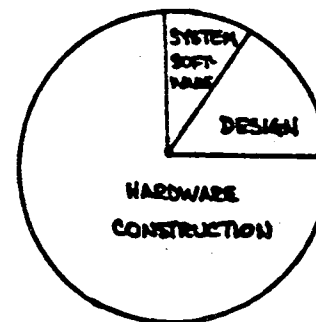
\$14.5M*

1969-1976

CPFF, NTE CLAUSE
ARMY R&D

ABM WEAPONS
SYSTEM

SMS COMPUTER



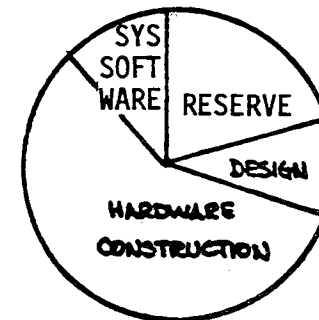
\$7.9M*

1972-1976

FP/CPAF
NASA R&D
BUDGET LINE

SHUTTLE MISSION
SIMULATOR

NAS**



1976-1986

COST AWARD
NASA R&D
BUDGET LINE

COMPUTATIONAL
FLUID DYNAMICS
(CFD)

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* EXCLUDING INITIAL STUDIES, APPLICATION SOFTWARE, AND BUILDING

** PROJECTED

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|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------------------------------|--|---------------------------------------------------------------------------------------|------------------|
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| 15. Supplementary Notes Computer Comparisons 1955 - 1986 with emphasis on NASA's proposed Numerical Aerodynamic Simulator (NAS), ILLIAC IV, STAR 100, PEPE, and SMS computers. | | | | | |
| 16. Abstract <p>In 1975, the National Aeronautics and Space Administration (NASA) began studies to assess the technical and economic feasibility of developing a computer having a sustained computational speed of one billion floating point operations per second and a working memory of at least 240 million words. Such a powerful computer would allow computational aerodynamics to play a major role in aeronautical design and advanced fluid dynamics research. Based on favorable results from these studies, NASA proceeded with developmental plans. The computer was named the Numerical Aerodynamic Simulator (NAS).</p> <p>To help insure that the estimated cost, schedule, and technical scope were realistic, a brief study was made of past large scientific computers. Large discrepancies between inception and operation in scope, cost, or schedule were studied so that they could be minimized with NASA's proposed new computer. The main computers studied were the ILLIAC IV, STAR 100, Parallel Element Processor Ensemble (PEPE), and Shuttle Mission Simulator (SMS) computer. Comparison data on memory and speed were also obtained on the IBM 650, 704, 7090, 7094, 360-50, 360-67, 360-91, and 370-195; the CDC 6400, 6600, 7600, CYBER 203, and CYBER 205; CRAY 1; and the Advanced Scientific Computer (ASC). A few lessons learned conclude the report.</p> | | | | | |
| 17. Key Words (Suggested by Author(s)) Computer History, Numerical Aerodynamic Simulator (NAS), ILLIAC IV, STAR 100, PEPE, and Shuttle Mission Simulator (SMS) Computer | | | | 18. Distribution Statement Unclassified - Unlimited Subject Category 62 | |
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