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SILICON-ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet Task of the Low-Cost Solar Array Project

FINAL REPORT

Prepared by

B. L. Grung, J. D. Heaps, F. M. Schmit, S. B. Schuldt and J. D. Zook

Period Covered: 10/21/75 - 12/31/80

Published: 3 March 1981

Honeywell Corporate Material Sciences Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

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PREFACE

This Final Report discusses the investigative results of a silicon-on-ceramic process for producing silicon sheet material. It was performed under the JPL Large-Area Silicon Sheet Task of the Low-Cost Solar Array Project.

The objective of the program was to investigate the technical and economic feasibility of producing solar-cell sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. The effort was divided into several areas of investigation in order to most efficiently meet the goals of the program. These areas include: 1) dip-coating; 2) continuous coating; 3) material characterization; 4) cell fabrication; and 5) theoretical analysis. The work in the continuous-coating technology development area was funded directly by Honeywell Inc. from 1 January 1979 to 30 September 1979. Additional support to certain phases of the continuous-coating effort was contributed by the Solar Energy Research Institute (SERI) under the title of "Supported Growth of Polycrystalline Silicon Sheet on Low-Cost Ceramic, Carbon, or Reusable Substrates," SERI contract No. XS-9-8119-1. Results from each of these separately funded efforts are included in this report for completeness.

The work was performed during the period 21 October 1975 to 31 December 1980 at the Honeywell Corporate Technology Center in Bloomington, Minnesota, under JPL contract No. 954356.

During the course of the program, the Project Managers were P.W. Chapman and J.D. Zook, and the Principal Investigators were J.D. Zook, J.D. Heaps, and B.L. Grung. Others who participated in this program are listed in another section of this report.

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SUMMARY

The objective of this Research and Development program was to investigate the technical feasibility of producing solar-cell-quality sheet silicon to meet the Department of Energy (DOE) 1986 overall price goal of $0.70/watt. With the silicon-on-ceramic (SOC) approach, a low-cost ceramic substrate is coated with large-grain polycrystalline silicon by unidirectional soldification of molten silicon. This R&D effort was divided into several areas of investigation in order to most efficiently meet the goals of the program. These areas include: 1) dip-coating; 2) continuous coating-designated SCIM-coating, an acronym for Silicon Coating by an Inverted Meniscus; 3) material characterization; 4) cell fabrication and evaluation; and 5) theoretical analysis.

Both coating approaches were successful in producing thin layers of large-grain, solar-cell-quality silicon. The dip-coating approach was initially investigated and considerable effort was given to this technique. The SCIM technique was adopted later because of its scale-up potentiality and its capability to more conveniently produce large areas of SOC.

Large (10 cm x 100 cm) ceramic substrates were developed by Coors Porcelain Co. for the purpose of this investigation. The substrates contained slot openings for making electrical contact to the bottom surface of the silicon coating. Mullite was the ceramic selected. It was compositionally modified to be thermally compatible with silicon.

By virtue of unidirectional solidification, the thin (50 to 250μm) silicon layers contain columnar grains as large as 5mm in width and several centimeters long. The single grains are heavily twinned with their boundaries, as well as the normal boundaries, generally normal to the surface of the layer. Thus, the layers are, in general, only one crystal thick. The silicon-to-ceramic bond is mechanical in nature and has proven to be reliably secure in practice.

It was determined that substrate slot openings which are oriented perpendicular to the growth direction perturb the silicon structure to a lesser extent than those which are parallel to the direction of growth. In either case, coverage with silicon is satisfactory. The thickness of the layer is inversely related to the melt temperature and is also proportional to the inverse of the coating speed squared, when the heat of fusion is removed

from the growing layer by radiation alone. It was experimentally demonstrated, however, that the growth rate can be substantially enhanced by the addition of convective cooling, and coating rates commensurate with project's economic goals can be achieved in this manner.

The mullite substrates are slightly soluble in molten silicon, causing the melt to become progressively contaminated using the dip-coating process. This is minimized with the SCIM technique by reducing the contact time and area the substrate has with the melt.

The surfaces of SOC coatings are smooth and shiny and need no further preparation other than a standard clean-up procedure prior to forming the p-n junction.

SOC solar cells can be reproducibly produced with an average conversion efficiency of 9.6% (AM1, AR). The slot openings in the ceramic substrates, however, must cover approximately 50% of the total substrate area to achieve this level of cell performance. The need for this large slot opening ratio is to minimize internal series resistance in the cell, a fact that resulted from a supporting analysis of parasitic resistance. The highest conversion efficiency for a dip-coated SOC cell was 10.54% (AM1, AR) and the highest efficiency for a SCIM-coated SOC cell was 7.6% (AM1, AR). The higher efficiencies are produced with a PH_3 diffusion at 850^{o}C, followed by a slow cooldown at about 5^{o}C/min.

Theoretical modeling of SOC solar cells shows that present cell performance is limited by diffusion length, and that 13% SOC cells are possible with a diffusion Length of 50μm.

The average diffusion length, L, in SOC material is 15 to 25μm. The diffusion length within good grains is three times the average diffusion length. Closely spaced grain boundaries, high dislocation densities, and subsurface grain boundaries have been identified as structural causes of the reduction in L.

Cost estimates of the SOC process are \$13/m^2 added value, or \$17.25/m^2 including silicon at \$14/kg. Based on 11% module efficiency, this corresponds to a sheet price of \$0.125/W_p added value, and \$0.166/W_p, including silicon. The analysis shows that the cost of ceramic is the largest cost driver in the SOC process.

INTRODUCTION

This R&D program began 21 October 1975. Its purpose was to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods developed were directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 11% or greater. At this period in time, sheet silicon, for the most part, was produced by growing cylindrical single-crystal ingots and slicing them into round wafers. This slicing effort not only requires labor and time, but is accomplished by a costly diamond-edged saw which in turn produces a kerf loss of expensive silicon. The sliced wafers are then mechanically polished and subsequently chemically etched to remove surface damage. For the purpose of safe handling, these wafers are made thicker than is necessary to produce solar cells of a reasonable conversion efficiency. Once this type of solar cell is fabricated, much less than half of the starting silicon material plays a role in the photovoltaic conversion of solar energy. The numerous processes required are labor-intensive and the round geometry of the final cell does not contribute to an area-efficient solar module.

The silicon-on-ceramic approach, on the other hand, eliminates many of the above costly features. With the SOC process, a graphite coating is applied to one surface of an inexpensive ceramic substrate, causing molten silicon to wet, upon contact, only that suface of the substrate to produce a uniform, thin layer of large-grain polycrystalline silicon. With this process, nearly all of the silicon consumed is used in energy conversion.

The surfaces of these thin layers are smooth and shiny and need no further preparation other than a cleanup before being processed into solar cells. Such layers are coated onto large areas of rectangular substrates, thereby maximizing the active-area/total area ratio of a final solar module.

During the course of this program, two silicon coating techniques were investigated:

- Dip-coating
- Continuous SCIM-coating (SCIM is an acronym for Silicon Coating by Inverted Meniscus)

Figure 1 illustrates the principle of dip-coating. A carbon or graphite coating is applied to one face of a ceramic substrate. The substrate is then dipped into and pulled from a crucible of molten silicon. As the substrate is withdrawn from the melt, unidirectional solidification occurs on the carbon-coated face of the substrate, forming a thin layer having large columnar silicon grains.

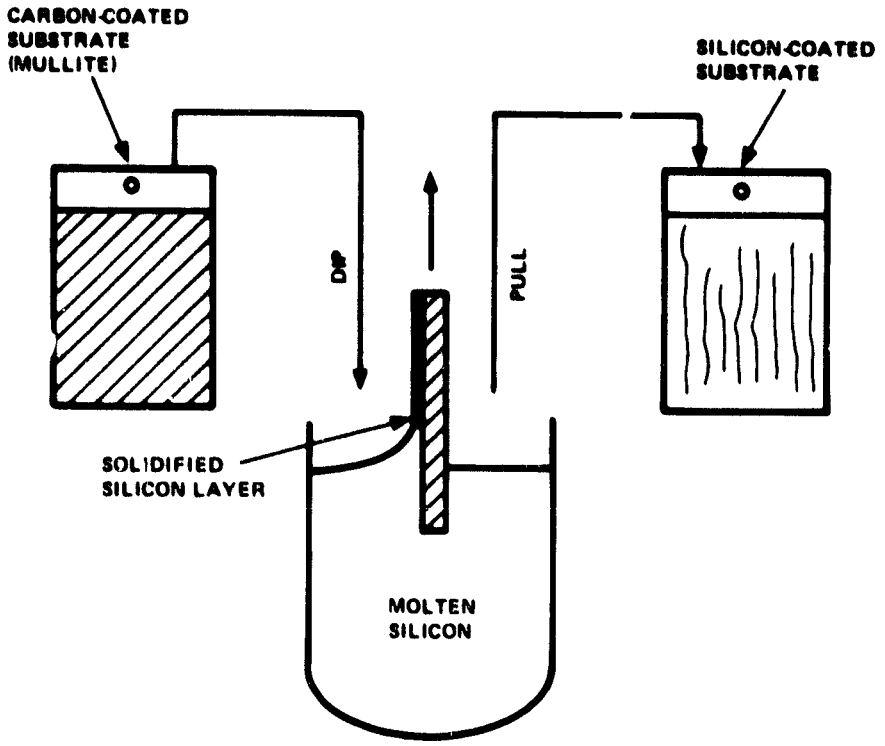


Figure 1. Silicon dip-coating principle.

The continuous SCIM technique is illustrated in Fig. 2. Molten silicon is contained in a fused-silica crucible having an attached trough as shown. A plunger is lowered into the crucible, displacing molten silicon along the trough to form a raised meniscus. As the ceramic substrate passes over this trough, the meniscus contacts the carbon-coated side of the substrate, forming a thin silicon layer which is virtually identical to that of the dip-coating technique. Since only the carbon-coated side of the ceramic comes into contact with the melt, there is, in principle, no direct contact between the ceramic and the melt. Thus, contamination of the melt is greatly reduced as compared with that obtained from the dip-coating technique.

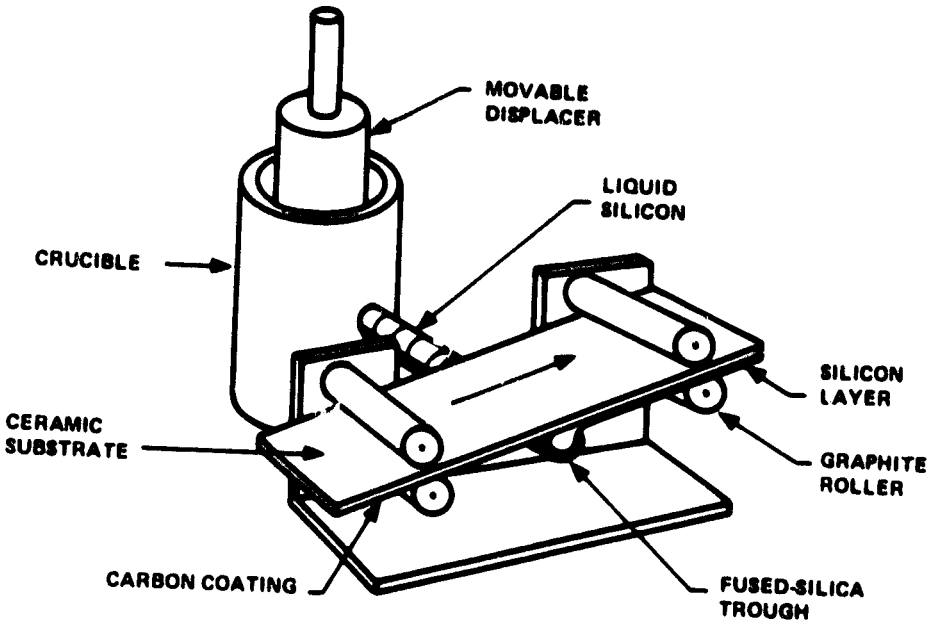


Figure 2. Schematic diagram of the Silicon-Coating-by-an-Inverted-Meniscus (SCIM) technique.

In support of this program, Coors Porcelain Co. of Golden, Colorado, developed cost-effective large-area (10cm x 100cm) mullite substrates whose composition was modified to be thermally compatible with that of silicon. These substrates contained slot openings for the purpose of making electrical contact to the bottom side of the silicon layer.

During this investigation, two dip-coating facilities and two SCIM-coating facilities were constructed. The second SCIM-coating facility is capable of simultaneously coating, side by side, two 12.5cm wide by 100cm long slotted substrates in a continuous manner.

The investigation demonstrated that antireflection (AR)-coated solar cells having an average conversion efficiency of 9.6% could be routinely produced from SOC material. The highest efficiency achieved was 10.54% (AM1, AR).

The economic analyses conducted throughout the investigation clearly show that if a coating throughput of 350 cm^2/min can be achieved, the process can produce silicon sheet within DOE's 1986 goal (with 11% efficient modules).

This report discusses the results of this 5+ years of work along with the approaches used in determining the results.

TECHNICAL DISCUSSION

SHEET SILICON COATING FACILITIES

Introduction

The silicon dip-coating technique, discussed in the introductory section of this report, initially provided the basis for this R&D program.

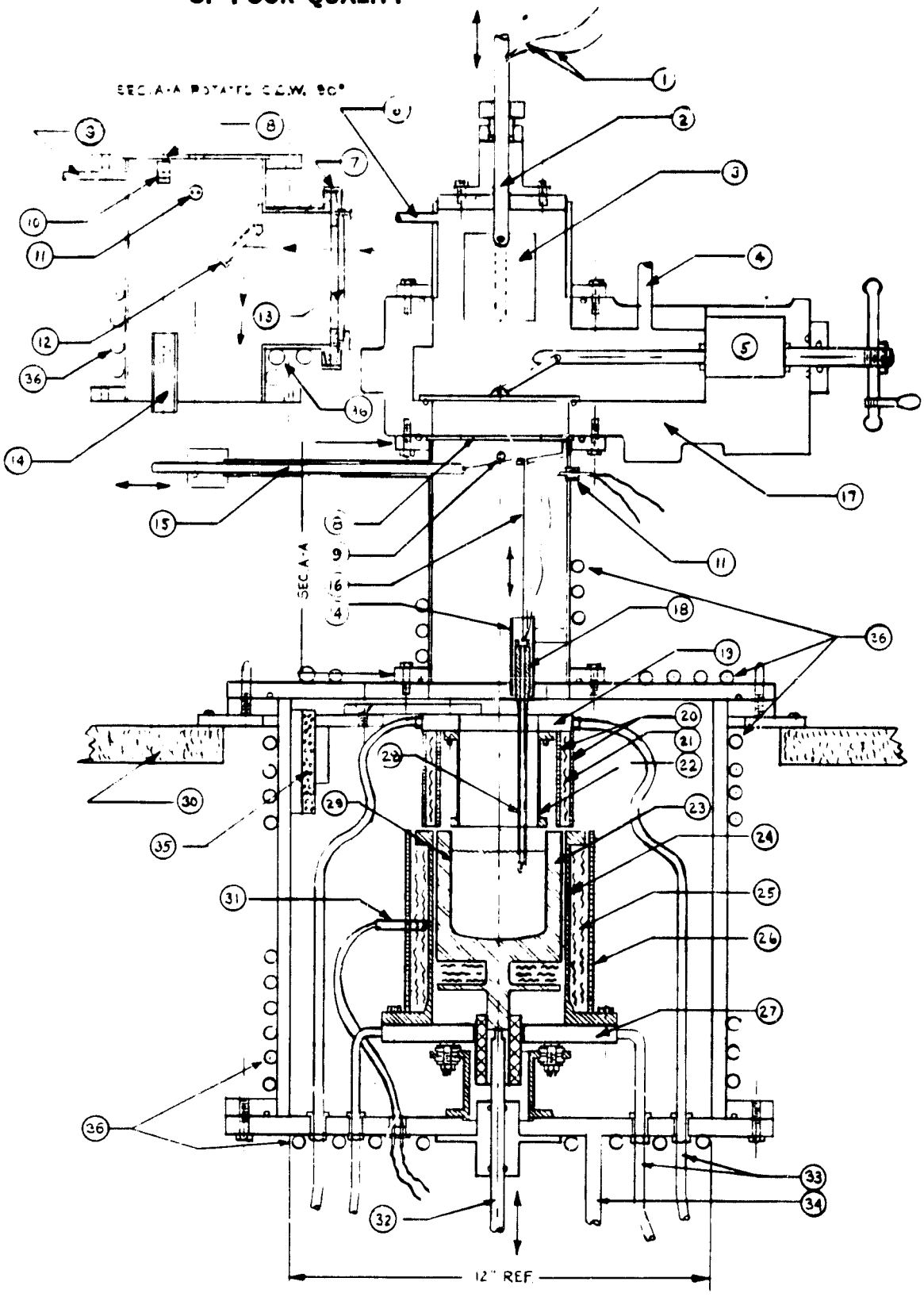
To satisfy the earlier needs of the program, two dip-coating facilities were designed, constructed, and successfully used in pursuit of the work. As the program progressed, other sheet silicon coating techniques were considered and the SCIM technique (also previously discussed) was adopted and successfully developed. In pursuit of this work, two SCIM-coating facilities were also designed and constructed.

This portion of the report addresses the purpose and function along with a detailed description of these four coating facilities.

Dip-Coater No. 1

To perform systematically an investigation of growth parameters which affect grain size, dislocation density, and layer purity, a versatile and reliable dip-coating facility was assembled. To the greatest extent possible, the facility was designed and constructed in such a way that its characteristics did not further complicate the problems to be solved. Since modifications were expected from time to time, sufficient design flexibility permitted such modifications to be performed with minimum time and expense. Once the necessary modifications were made, however, which permitted this coater to routinely produce good reproducible sheet silicon coatings, its design was for the most part frozen and it was then used for providing sheet silicon for the solar cell development effort.

A sectional drawing of the facility is shown in Fig. 3 and a photograph of the assembled facility is shown in Fig. 4.



(a) Sectional view.

Figure 3. Dip-coater No. 1.

(1) Substrate Thermocouple Lead Wires
(2) Dip-Pull Quartz Tube
(3) Ceramic Substrate
(4) Gas Lock Chamber Pumping Port
(5) Gate Valve Gear Box
(6) Gas Lock Chamber Gas Outlet
(7) Vacuum Connector Clamp
(8) Stainless Steel or Moly Heat Shield
(9) Melt-Dipping Chamber Gas Outlet
(10) Melt Thermocouple Wire Guide
(11) Melt Thermocouple Feed-Thru
(12) 45-degree Chromium Plated Mirror
(13) Quartz Window
(14) Melt Thermocouple Weight Guide
(15) Melt Thermocouple Positioning Rod
(16) Nichrome Wire
(17) Vacuum Gate Valve
(18) Melt Thermocouple Weight
(19) Water-Cooled "After Heater" Base Plate
(20) Graphite Heat Shields ("After Heater")
(21) Carbon Felt Insulation ("After Heater")
(22) Graphite "After Heater"
(23) Crucible Holder (Graphite)
(24) Graphite Silicon Melt Heater
(25) Carbon Felt Insulation (Silicon Melt Heater)
(26) Graphite Heat Shield (Silicon Melt Heater)
(27) Water-Cooled Silicon Melt Heater Base Plate
(28) Quartz-Covered Melt Thermocouple
(29) Quartz Crucible
(30) Dip-Coating Facility Main Frame
(31) Silicon Melt Heater Control Thermocouple
(32) Crucible Positioning Rod
(33) Water-Cooled Heater Electrical Leads
(34) Melt-Dipping Chamber Pumping Port
(35) Ceramic Insulation
(36) Water-Cooled Surfaces

(b) Nomenclature.

Figure 3. Dip-coater No. 1 (concluded).

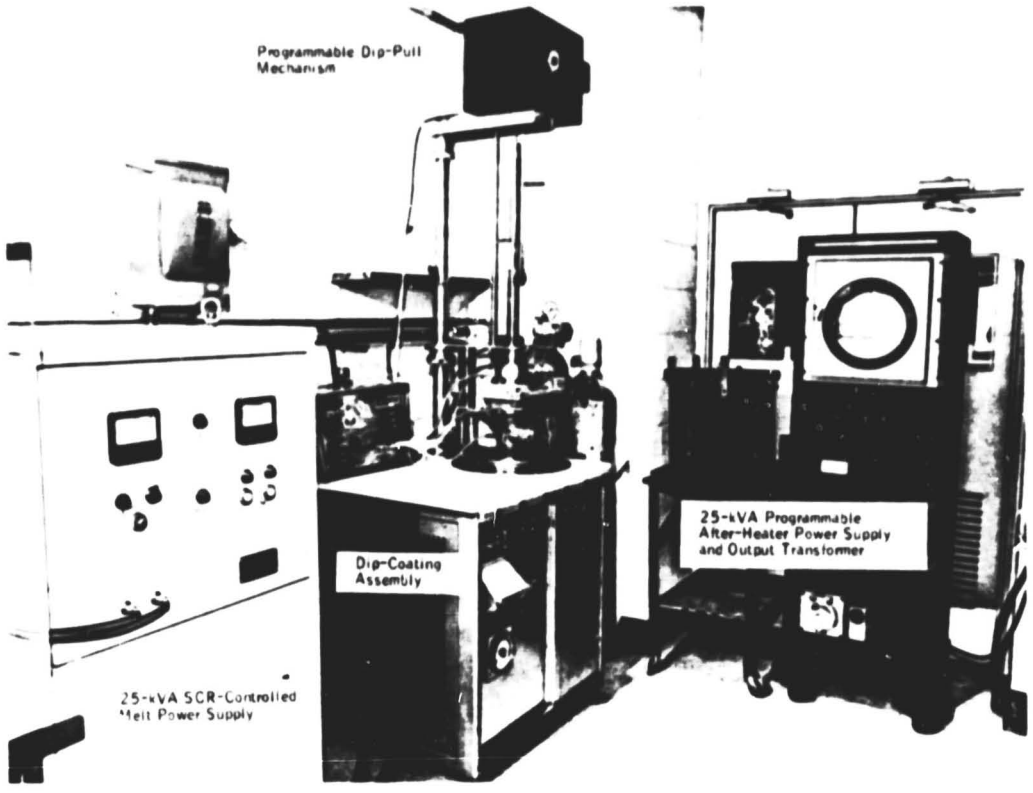


Figure 4. Dip-coater No. 1 and associated equipment.

The coater included the following features:

- A melt crucible (item No. 29) capable of dip-coating 6.5cm x 5.0cm substrates. This capability permitted us to produce sheet silicon coatings in excess of the $20cm^2$ JPL requirement.
- A purified graphite silicon melt heating element (item No. 24) powered by a temperature-controlled 25kW power supply. The heater assembly is mounted on a water-cooled copper base (item No. 27) and has only purified graphite cylinders item No. 26 and carbon felt (item No. 25) for insulation. This reduces melt chamber chemical contamination to a minimum.

- A Honeywell three-mode, precision temperature controller.

- A water-cooled, stainless-steel melt chamber (item No. 36) and viewing port assembly. This water cooling is needed to offset the lack of heater-element insulation. This feature also contributes to a low level of chemical contamination. The cleanable viewing port is used for observing the substrate as it is entering and leaving the melt.

- A gas-lock chamber (item No. 4) which permits the operator to load uncoated substrates and remove coated ones without shutting down the melt power. This feature is made possible by a large vacuum gate valve (item No. 5) which is located between the dip-coating chamber and the gas-lock chamber. The gas-lock chamber is readily purged with argon prior to opening the gate valve.

- A programmable, variable-speed dipping and pulling mechanism.

- A two-pen Honeywell electronic-type chart recorder for recording substrate position and temperature, both with reference to the melt. To efficiently characterize the optimum growth parameters it was mandatory that the growth conditions be accurately recorded for each sample substrate that was dip-coated. By doing so, as the physical properties of each coated sample were analyzed with respect to their particular growth conditions, positive direction could be given to the investigation. To provide this capability, the dipping and pulling mechanism was designed to provide an electrical readout which, when combined with the recorder's chart speed, provided dip-pull rate information.

- An afterheater (item No. 22), if needed, located immediately above the silicon melt. This heater, however, was never used for layers grown at normal (3 to 6 cm/min) pull rates, but was used later in the program for fast (> 12 cm/min) growth studies.

- A capability for orienting the substrate at an angle while performing the dip-pull operation. There were no well-defined theories which suggested that angle dipping may enhance grain size, but intuitively we expected that dipping an angle-oriented substrate would modify the liquid-solid interface, perhaps in a beneficial way. Future experiments, however, demonstrated that this was not the case.

- Two adjustable gas flowmeters, one for regulating and monitoring the gas flow through the melt chamber and another for purging the gas-lock assembly.
- A two-way gas valve for transferring from the argon gas cylinder to another cylinder should another type gas be desirable during a particular run.
- A water failure shutdown switch.
- A control panel for operating the facility.

Dip Coater No. 2

As the program progressed and dip-coater No. 1 was producing excellent large-grain sheet silicon coatings, we became reluctant to further modify No. 1 for experimental purposes. Dip-coater No. 2 was then designed and constructed to perform future experimental functions. The major task for this coater was to define the optimum conditions necessary to grow reasonably thick (i.e., 100μm) films at high rates (i.e., 9 to 18 cm/min). The design of this experimental dip-coater closely resembled that of dip-coater No. 1 with a few major exceptions. Dip-coater No. 2 was larger to allow more access around the liquid-solid interface and to allow special afterheaters to be used. The initial attempts to improve the growth rate while maintaining a film of reasonable thickness would involve the use of cold fingers to increase the temperature gradient at the liquid-solid interface. Dip-coater No. 2 had more access ports to accommodate the extra heating and/or cooling equipment necessary to grow at higher rates. The main experimental approach used to increase growth rates is to remove the latent heat of solidification by forced convective and radiative cooling through the use of cooling shoes placed near the liquid-solid interface. As will be discussed below, when this is done, an afterheater must also be used to prevent fracture of the coated substrate during cooling.

A photograph of dip-coater No. 2 is shown in Fig. 5. There are four access ports in the central portion of the chamber. Two are aligned at 30° to the geometrical center of the parting plane between the upper and lower chambers. There are four access ports in the top of the chamber that also point to the center of the parting plane and are inclined at an angle of 60°. During a run, the melt surface is typically level with the parting plane.

The heater assembly is shown in Fig. 6. A silicon charge is shown inside a fused-silica crucible in a graphite crucible holder. The crucible holder in turn is situated inside a graphite resistance heater which is surrounded by a heat shield consisting of two concentric graphite cylinders spaced with graphite wool. The heat shield, heater, and crucible holder can be independently positioned. The glass tube on the right of the heater is used to blow argon gas over the melt surface during some runs to minimize SiO formation on the silicon coating when cooling shoes are not use The heater is a picket-fence design considered to be more rugged than the thin-wall heater used in the other coater.

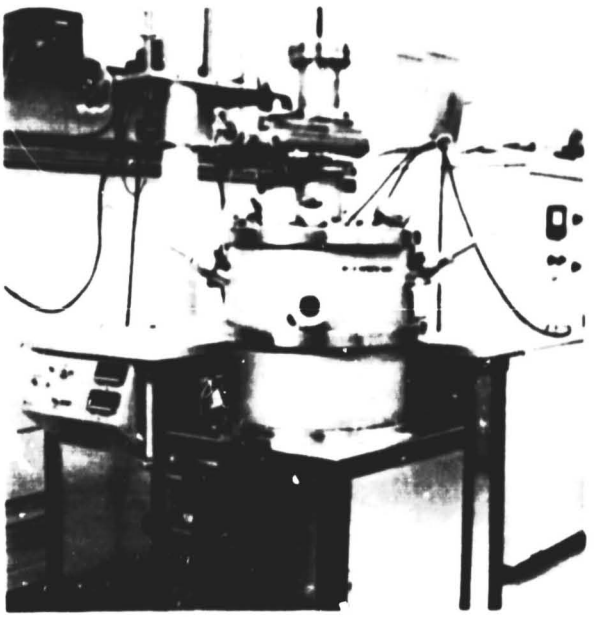


Figure 5.
Experimental dip-coater.

Figure 6.
Heater assembly in experimental dip-coater.

The position of front and back cooling shoes with respect to the substrate and heater assembly is shown in Fig. 7. The cooling shoes are machined from nickel and contain passages for both water cooling and gas flow. The cooling and gas flow in a cooling shoe is shown in Fig. 8. The gas exits through holes drilled in the end of the shoe. This was not an acceptable situation because the nonuniform cooling on the silicon results in coatings with ve-

tical striations. Examples will be shown later. On the other hand, nonuniform gas coverage clearly shows the effects of gas cooling on the growth pattern during dip-coating. Future modifications of the cooling shoes provided more even gas coverage over the surface of the substrate.

When forced convective cooling is provided at the liquid-solid interface during dip-coating, the thermal shock is almost always sufficient to fracture the substrate particularly at higher pull rates. To minimize thermal stresses in the coated substrate, an afterheater must be used. Early attempts with "passive" afterheaters (i.e., those heated only by conduction or radiation from the melt zone) were not satisfactory and an independently powered graphite resistance afterheater was eventually installed.

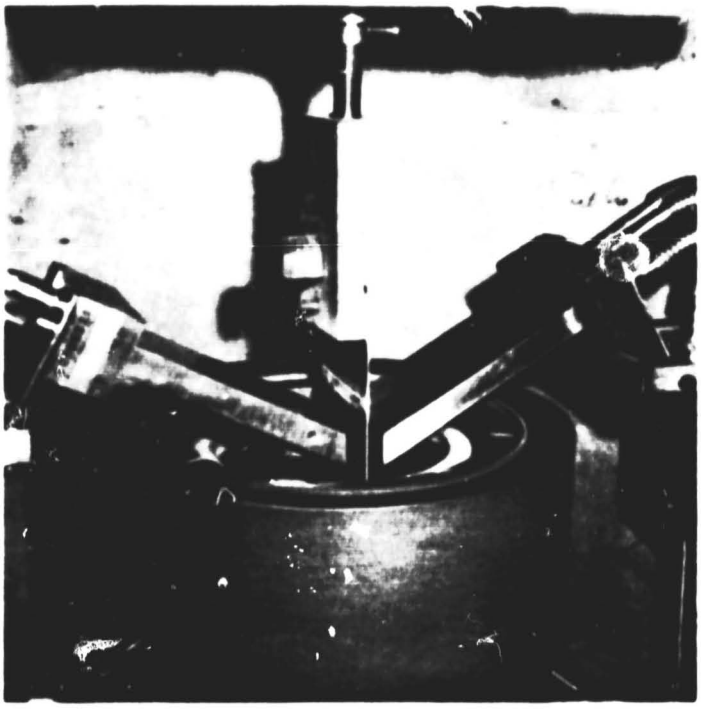


Figure 7.
Photograph showing front and back cooling shoes in place in experimental dip-coater.

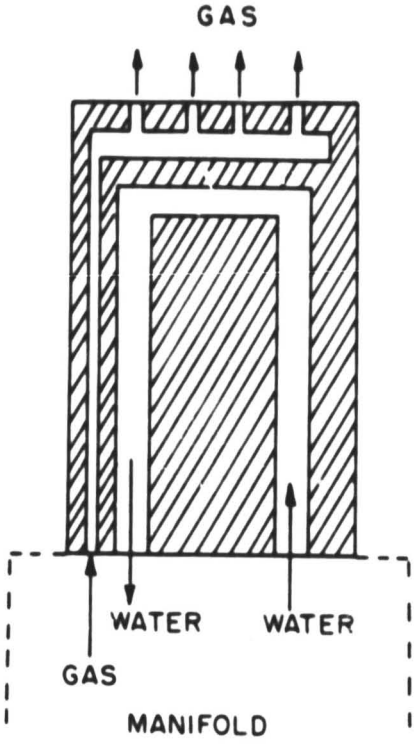


Figure 8.
Schematic showing water and gas flow in cooling shoes.

The heater is a thin-wall, cylindrical, split-resistance element similar to those used early in the program as crucible heaters. The heater is powered by unregulated a-c current through two transformers in series. The relation-

ship of the crucible, cooling, and afterheater is shown in Fig. 9. The cooling shoes are inclined at an angle of 20° to the melt surface. The arrows on the sketch indicate the direction of gas flow in each shoe. Note that in the shoe facing the uncoated side of the substrate, the holes are drilled parallel to the axis of the shoe, while the holes in the other shoe are drilled perpendicular to the substrate surface. This arrangement allows the back side of the substrate to be cooled slightly below the liquid-solid interface, while the front side is cooled above the interface. Typically, the gas flow rate on the back side of the substrate is four times that through the front shoe.

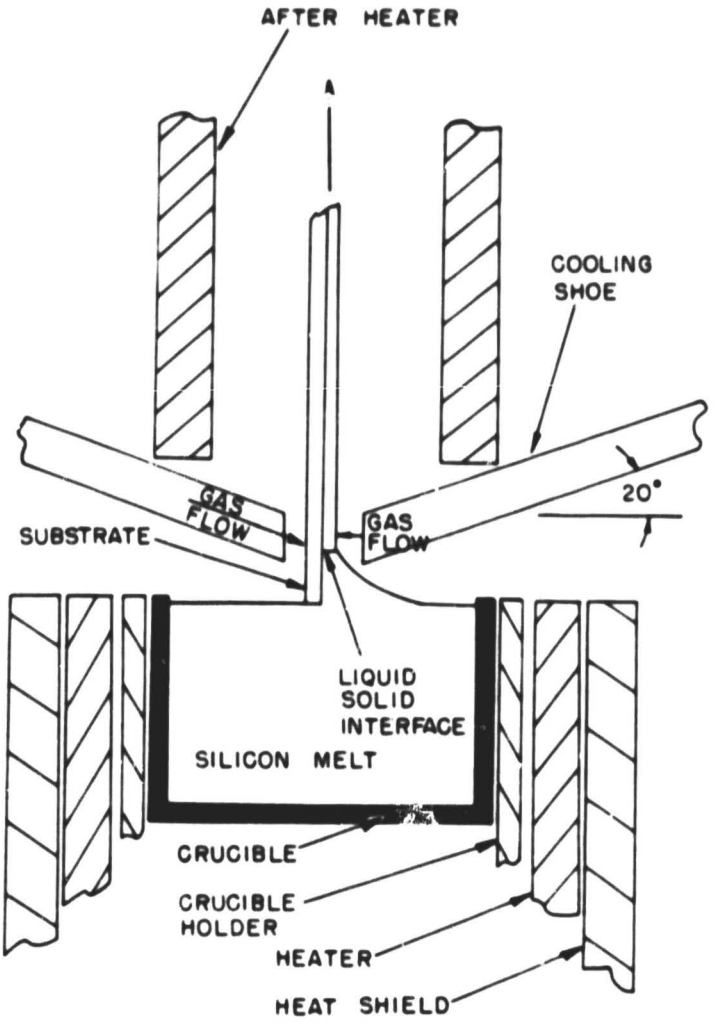


Figure 9. Schematic showing relationship of afterheater, cooling shoes, and crucible assembly in experimental dip-coater.

SCIM-Coater No. 1 (SCIM-I)

It was recognized early in the program that even though the dip-coating technique was successfully producing thin, smooth sheet silicon coatings of solar-cell quality, the method, nevertheless, was not easily adaptable to a continuous coating technique. In addition to this, experimentation had shown that the silicon melt was being progressively contaminated with each successive substrate that was silicon-coated. In an effort to overcome these disadvantages, the SCIM technique (described in the Introduction of this report) was adopted as a promising continuous-coating method. The principal advantages of the SCIM technique are:

- Its coating principle vastly reduces the area of, and the time that the substrate is in contact with, the silicon melt. This feature lessens the possibility of the melt being progressively contaminated by the substrate.

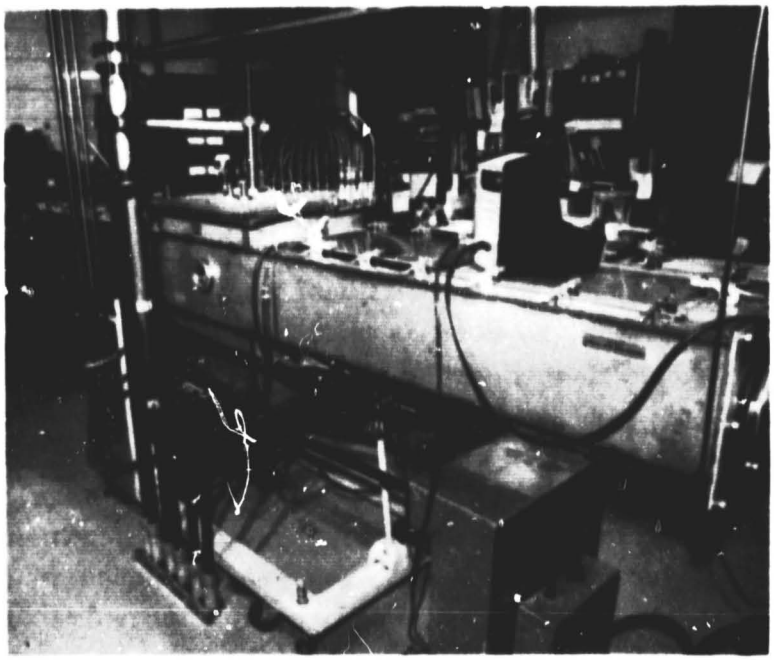
- This technique permits the use of much larger substrates, which should allow the individual crystalline grains to develop larger in size.

- The scale-up coating throughput of this method is potentially superior because it eliminates the dipping and soaking time required with the dip-coating technique.

- The thermal stability of the solidification zone of a continuous coater should also be superior to a dip-coater, since the melt temperature would not be constantly upset by the immersion of unheated substrates.

Figure 10 shows photographs of the SCIM-I facility. The coater is divided into five sections: (1) a compartment for substrate loading; (2) a preheater section for bringing the substrate up to temperature; (3) a silicon coating compartment; (4) a postheater section for cooling the substrate; and (5) a compartment for substrate removal. During a coating run, these compartments are flushed with an inert gas, most generally argon. The coater is powered by four temperature-controlled power supplies, two of which power the upper and lower preheaters. The third supply powers the main melt furnace and the fourth supply the coating trough furnace.

(a) SCIM coater No. 1 during operational run.



(b) SCIM coater No. 1 showing bus bars from remotely located power supplies.

Figure 10. Photographs of SCIM-I.

Three of these four heaters are shown in Fig. 11. The preheater assembly consisted of a long graphite tunnel through which the substrates pass. A longitudinal temperature gradient was created along the tunnel by heating one end of the tunnel with the upper and lower preheater elements. This tunnel assembly was subsequently surrounded by a dual-walled insulated housing, also shown in Fig. 11. A cross-sectional view of the preheater assembly is illustrated in Fig. 12. The postheater is similar to the preheater except that it is slightly longer and passively heated by the coating trough and preheater. Figures 11 and 13 show the longitudinal thermal profiles which existed with this heating configuration. Initially, SCIM-I's transport mechanism consisted of stainless-steel chain conveyors which carried the substrates to, through, and from the growth chamber. The chain conveyors were driven by a "Digilok"-controlled, variable-speed drive system which was adjustable for growth velocities of tenths of cm/min to many cm/min. Given a relatively flat substrate, the fore and after chain conveyors were spaced to allow the substrate's center of gravity to carry it from one conveyor to the other. Special silicone rubber end gates permitted substrates to pass through the coater with a minimum of gas leakage. While the facility was primarily designed to horizontally coat substrates, provision was made for tilting the entire facility through about $\pm 30^{\circ}$. This proved to be a valuable feature, since it was never possible to successfully coat substrates in the horizontal position.

The isotherms shown in Figs. 14 and 15 illustrate that the transverse temperature uniformity near the coating trough was very bad. Likewise, with this furnace configuration, the longitudinal temperature profile shown in Fig. 11 did not indicate a sharp enough temperature drop in the solidification zone of the coater. To correct both of these thermal inadequacies, a new type of trough-heater assembly was installed in the coater.

This heater was fabricated in such a way that the graphite trough holder itself was an active resistive element of the assembly (see Fig. 16). The rectangular legs of this heating assembly served the final substrate heating requirement. The power density of each leg was graduated in such a way that the substrate temperature never exceeded the melting point of silicon. Contrary to the original approach (see Fig. 11), the heating zone now terminated abruptly at the downstream edge of the trough.

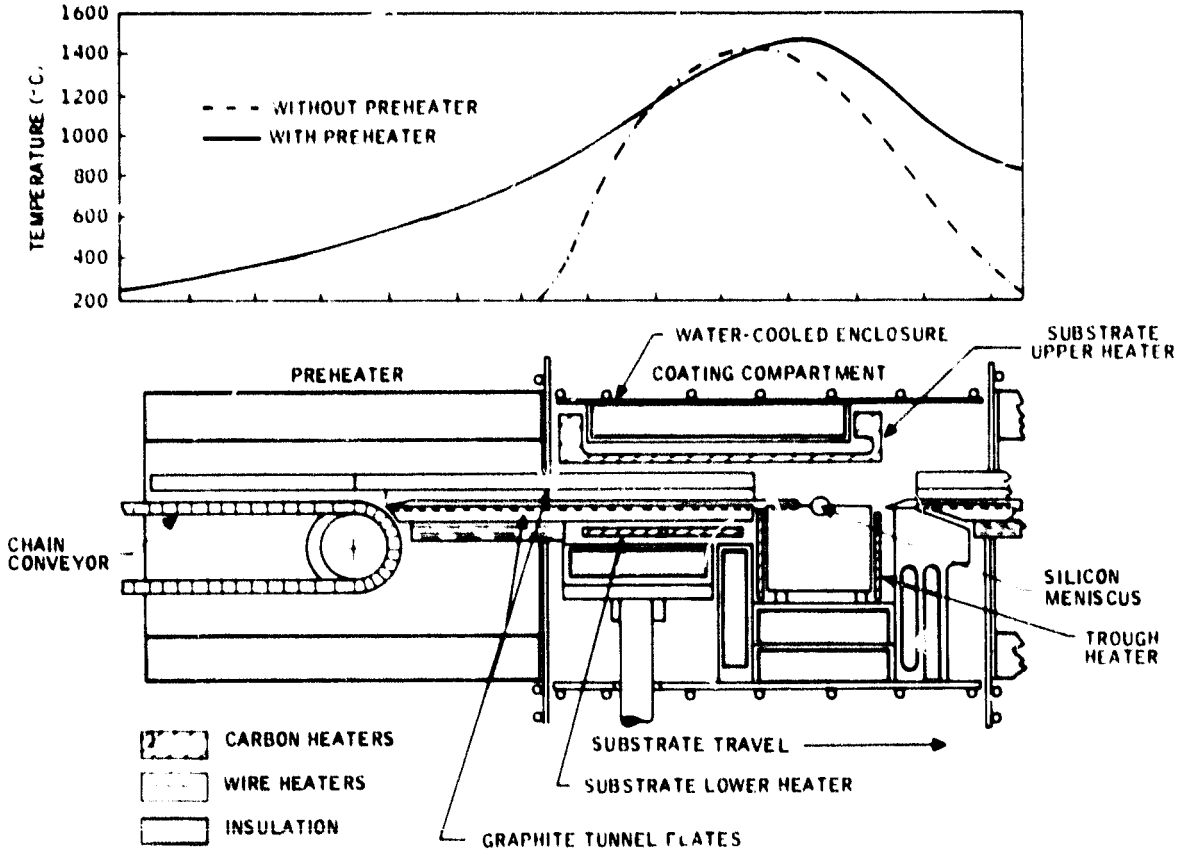


Figure 11. SCIM-I preheater longitudinal thermal profiles.

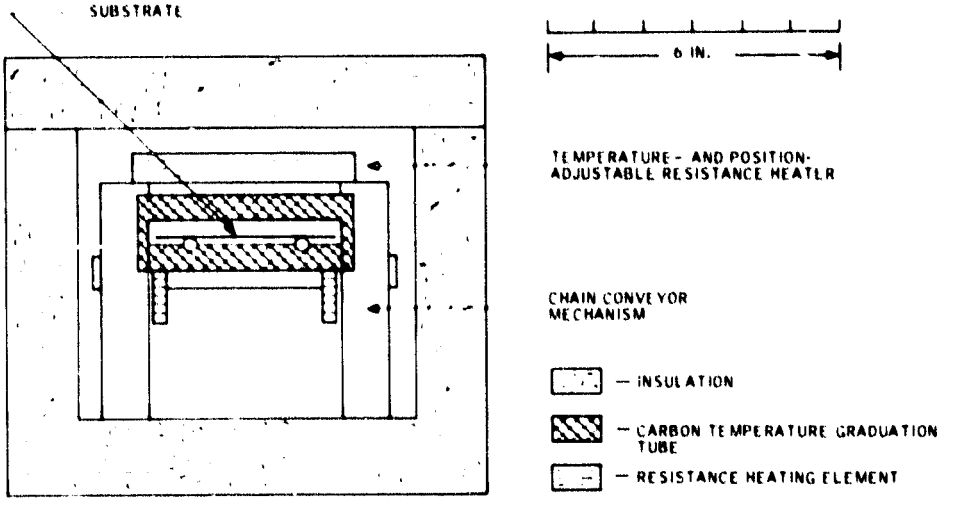


Figure 12. Cross-sectional view looking into SCIM-I preheater compartment as viewed from the coating chamber.

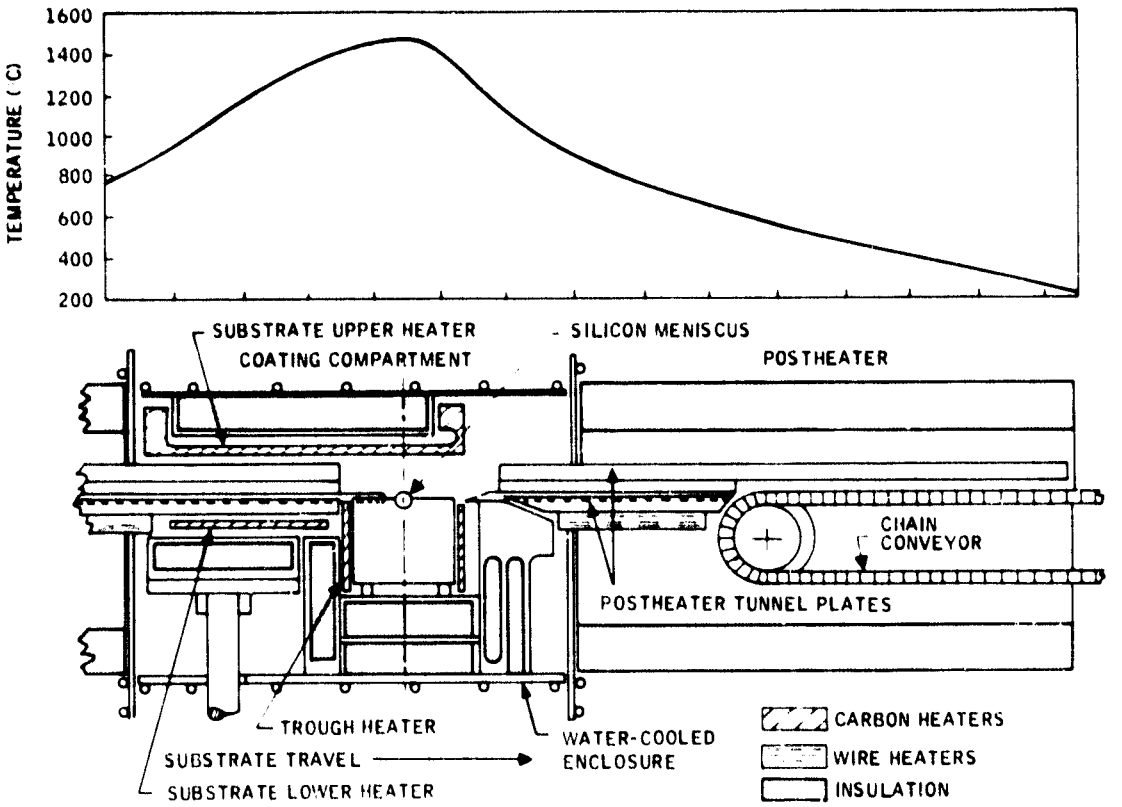
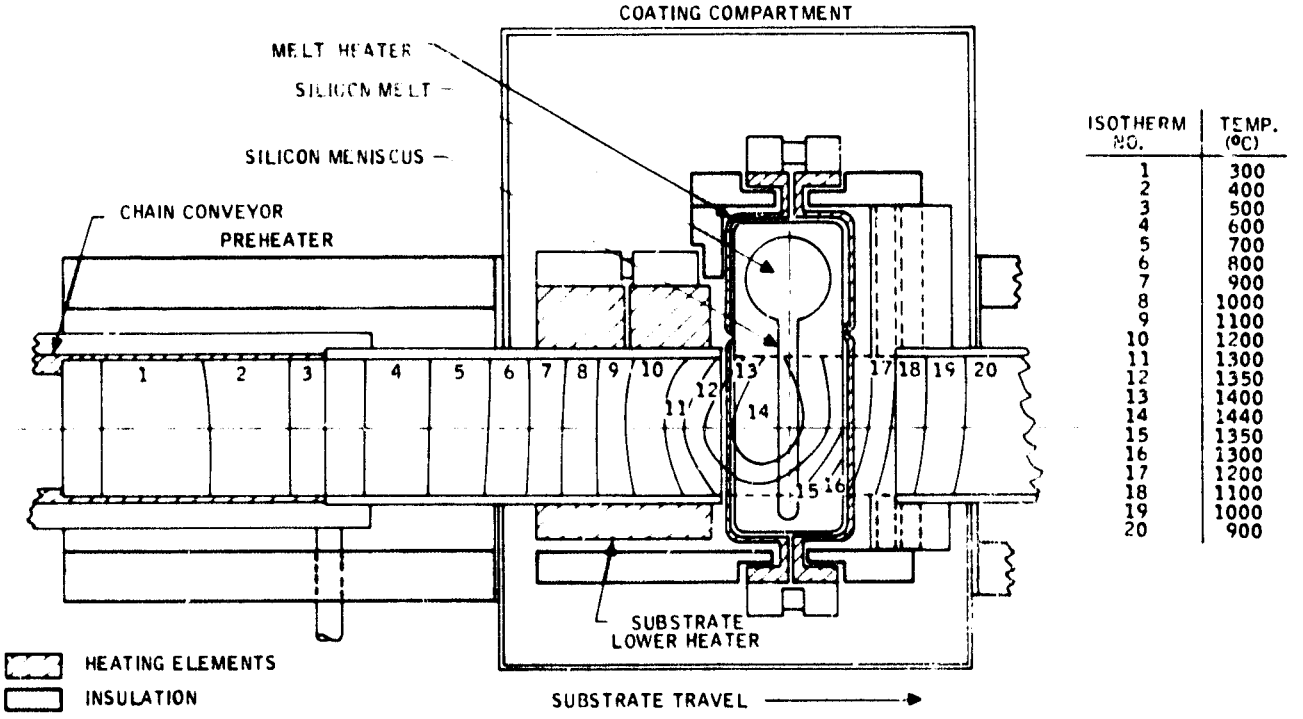


Figure 13. SCIM-I postheater longitudinal thermal profile.



ISOTHERM NO.	TEMP. (°C)
1	300
2	400
3	500
4	600
5	700
6	800
7	900
8	1000
9	1100
10	1200
11	1300
12	1350
13	1400
14	1440
15	1350
16	1300
17	1200
18	1100
19	1000
20	900

Figure 14. SCIM-I preheater isotherms.

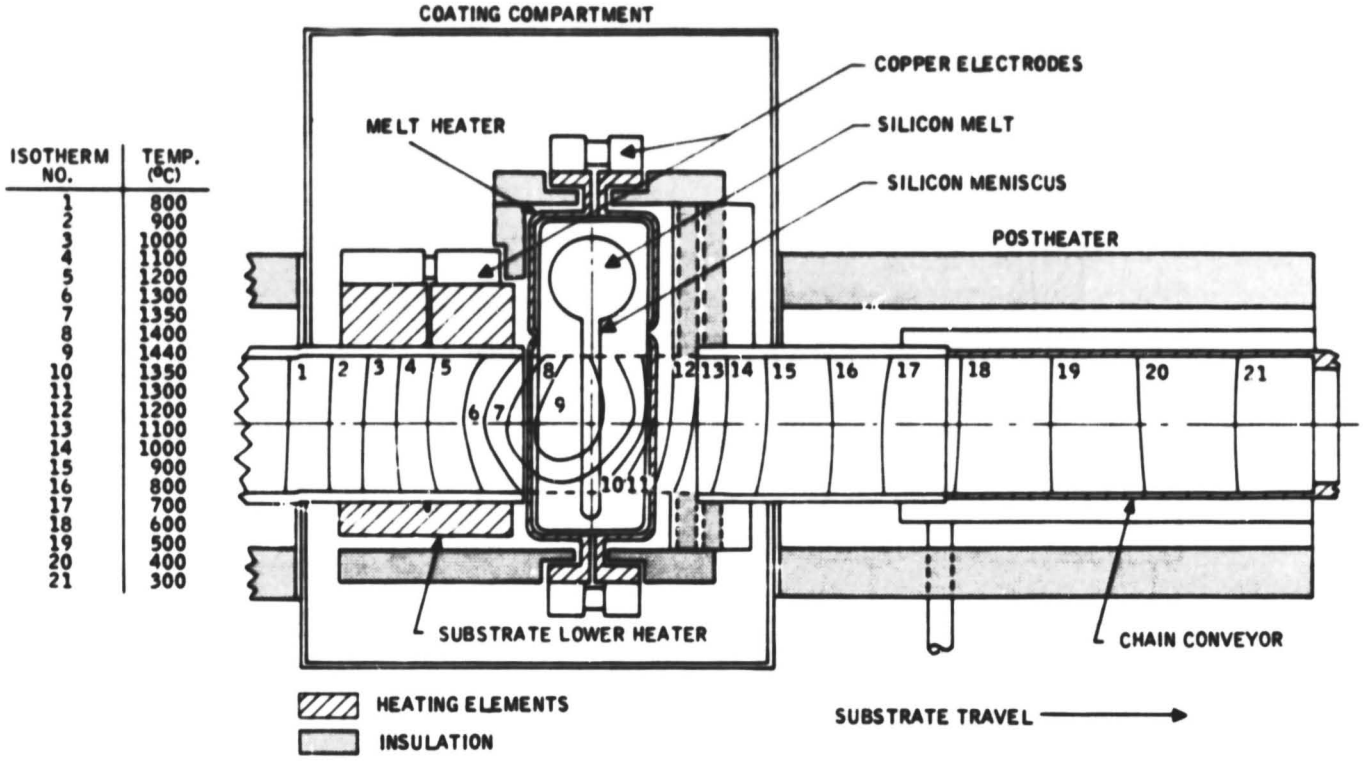


Figure 15. SCIM-I postheater isotherms.

Figure 16.
New trough/substrate heater
(also showing quartz crucible/
trough piece).

As shown in Fig. 17, the upper substrate heater was shortened, thereby shifting the peak temperature in an upstream direction.

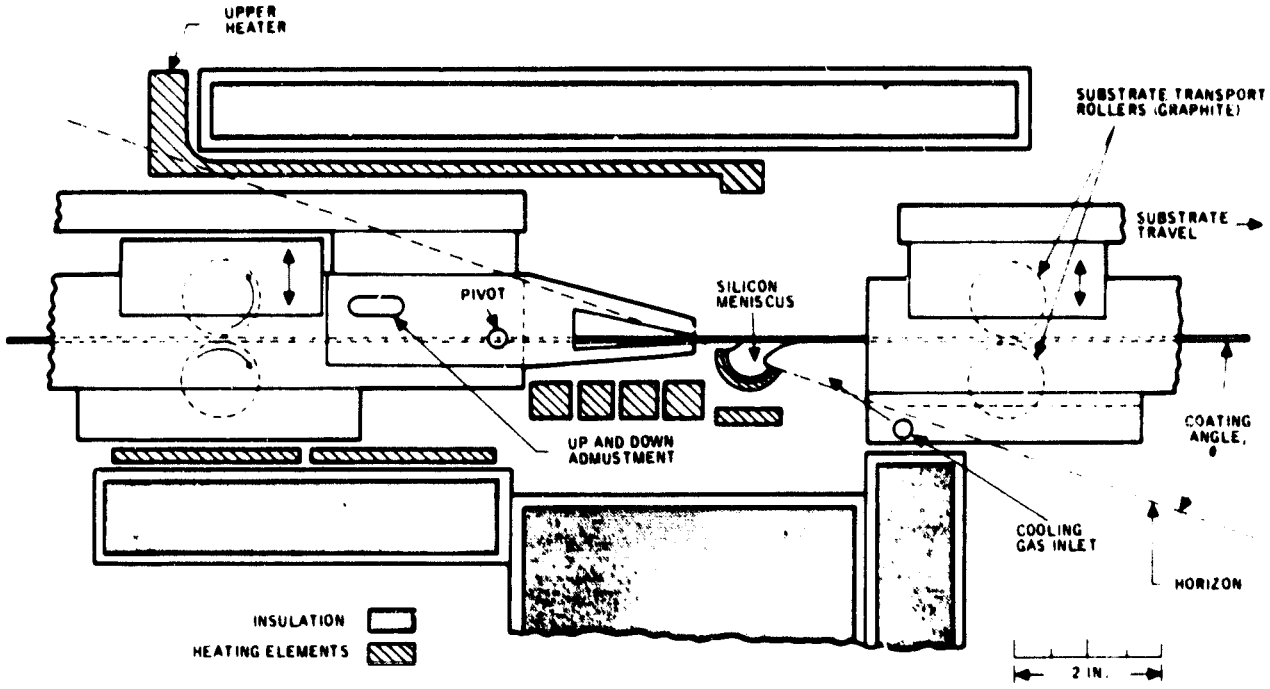


Figure 17. SCIM-I coating chamber configuration showing combination trough/substrate heater.

Following the above modifications, the liquid-solid interface, if desired, could now be shifted until solidification occurred at the edge of the trough. This is the dip-coating equivalent of having the surface of the melt freeze around the substrate as it is being withdrawn from the melt. The temperature of this shorter heater was now a critical coating parameter. If too hot, solidification, as usual, occurred too far downstream. If not hot enough, the substrate would freeze to the melt. In spite of this fact, the solidification position could now be controlled.

The original chain-conveyor transport mechanism proved to be inadequate. Therefore, while the above furnace modifications were being implemented, a multiple-roller-type mechanism was installed in the coater. The lower roller was driven, whereas the upper roller served as an idler to maintain the alignment of the substrate. The rollers were made of graphite, since two sets of them operated at temperatues as high as 1200^{o}C. The addition of these transport rollers required a modification to be made in the pre-

heater and postheater assemblies, also shown in Fig. 17. It was with this coating configuration that the first successful continuous coating was performed.

SCIM-Coater No. 2 (SCIM-II)

In the last year of this contract, a second continuous-coating system (designated SCIM-II) was designed, constructed, and made operational. Its primary function was to demonstrate the capability of producing silicon sheet at a throughput rate of 350 cm^2/min.

To achieve this goal, the coater was designed as shown in Fig. 18 to simultaneously coat (side-by-side) two 12.5cm-wide x 100cm-long mullite substrates The coating experience acquired using SCIM-I was a valuable asset in the design of SCIM-II. The design of this new coater is shown schematically in Fig. 19.

Figure 18. SCIM-II exterior showing two side-by-side substrates entering the coater.

There are several key features which are different from the SCIM-I system. They are:

1) All assemblies within the coater are attached to a common water-cooled chassis (see Fig. 20). This assures us that proper alignment of key

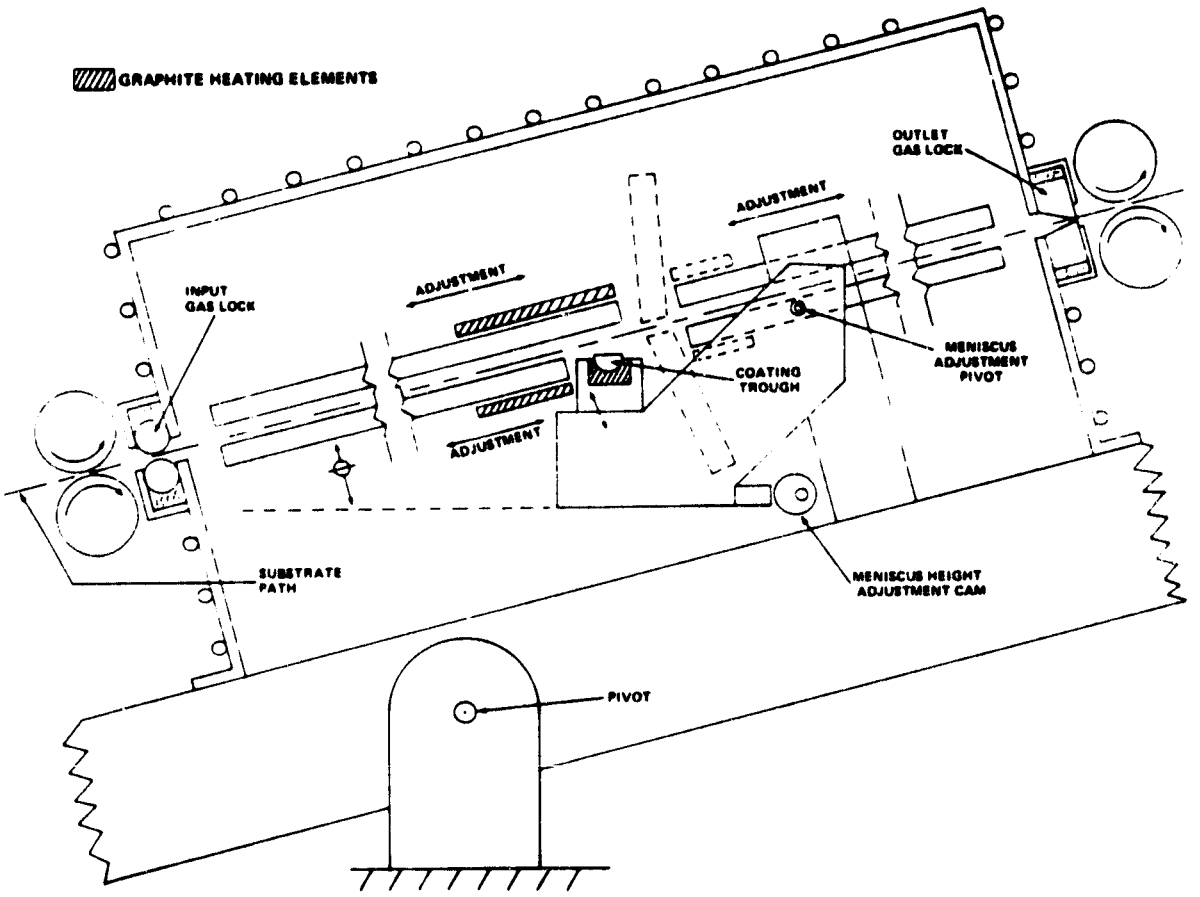


Figure 19. Schematic cross section of SCIM-II.

parts will be maintained irrespective of operating temperature.

2) All metallic parts within the coater are water-cooled to improve the purity of the silicon layer, and the majority of the remaining parts are fabricated from graphite which can be purified prior to assembly.

3) The melt crucible and trough are contained in a graphite cradle assembly which permits convenient adjustment of trough-to-substrate distance during operation.

4) Side heaters powered by a separate power supply were installed tc improve the transverse temperature uniformity in the substrate preheater. These side heaters, however, have proven so far not to be a necessary feature.

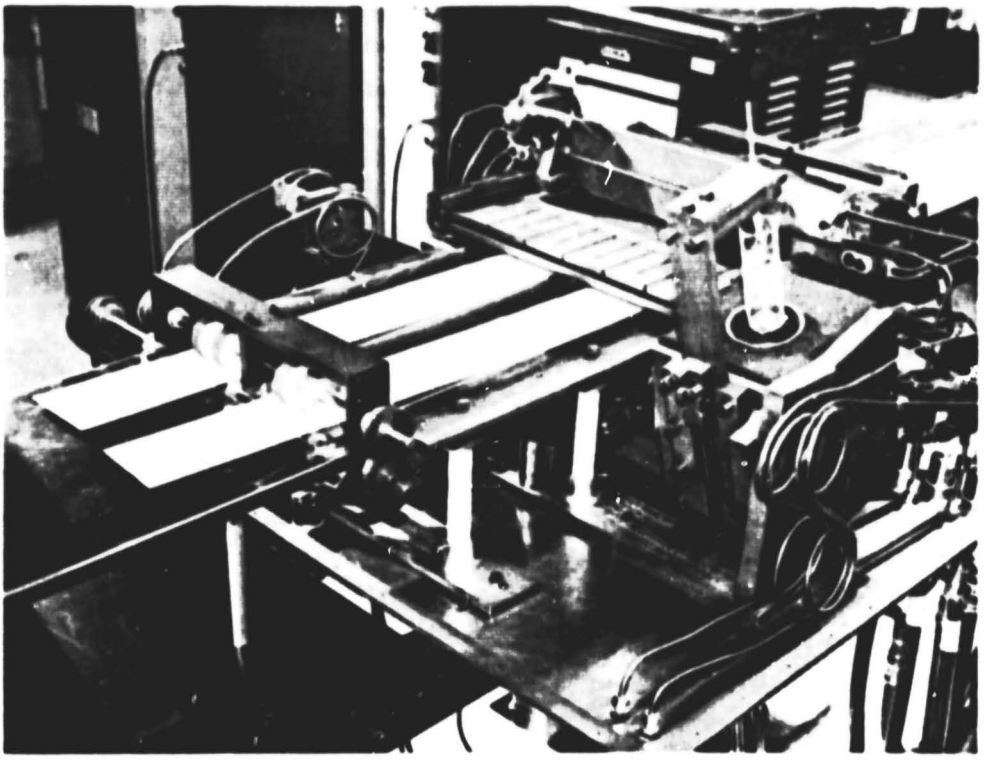


Figure 20. SCIM-II interior showing water-cooled base and substrates emerging from preheater.

5) The substrate transport mechanism consists of aluminum rollers which are fitted with several silicone rubber "O"-rings. The upper, as well as the lower roller, is driven by a loosely coupled spur gear. The entrance and exit rollers are positioned external to the cover containing the inert atmosphere needed for growth. In operation, they have proven to be very effective in performing the transport function. With this method of substrate transport, however, the substrate used must be at least as long as the distance (97cm) between the rollers. This can be a problem if a substrate breaks during coating. In this respect, the multiple-roller method used in SCIM-I is superior. However, the numerous rollers in SCIM-I, some of which operate at temperatures as high as 1200^{o}C, proved to be only marginally dependable.

6) The water-cooled cover on SCIM-II serves only the function of containing the inert gas. As such, when this cover is removed, the inner walls are easy to clean. Likewise, when removed, the entire inner-workings of the coater are easily accessible for maintenance.

The preheater and postheater design used in SCIM-II was fashioned after that of SCIM-I. This design was used because these functions in SCIM-I performed well. The purpose of the preheater is to bring the substrate from room temperature to the melting point of silicon in a manner which neither fractures nor warps the substrate. This is done by using a narrow graphite tunnel through which the substrate passes. One end of the tunnel is heated by a graphite resistance heater, and thermal conduction along the tunnel creates the needed temperature gradient. The postheater is similarly constructed. It, however, is a passive element deriving its heat from the preheater and the coating trough. This coating configuration produces a temperature profile with a rapid fall in temperature immediately downstream from the coating trough, thus creating the required thermal environment for solidification. To ensure that the coated substrate will emerge from the machine at a temperature of less than 232^{o}C (the maximum operating temperature of the silicone rubber "O"-rings), a water-cooled heat sink is attached to the downstream end of the postheater. The thermal modeling contributing to this design is discussed later in this report. In order to achieve a uniform transverse temperature, the preheater and postheater are substantially wider than the width of the side-by-side substrates being coated.

The trough heater and the fused-silica trough-crucible assembly are also fashioned after the design used in SCIM-I. The quartz trough nestles in an electrically active trough heater. The cross section of this heater is reduced at the electrode end in order that additional power can be generated to offset losses by conduction to the water-cooled copper electrodes and by radiation through the viewing port. The trough heater is also made purposely long for temperature uniformity reasons.

As with SCIM-I, SCIM-II can also be tilted to coating angles up to 20^{o} to provide the necessary meniscus stability. To date, 10cm-wide substrates have been coated at angles of 10^{o} and 20^{o} these results are included elsewhere in this report.

The most obvious problem during the initial operation of SCIM-II was the

buckling and/or breakage of the coated substrates. Experiments were performed without silicon in the system to clarify the situation. Initial experiments quickly showed that at high speed (15 cm/min) there was only minor buckling, but at lower speeds, the buckling became more severe, and below 6 cm/min the substrates broke. The results were qualitatively the same regardless of the silicon coating and regardless of whether one side of the substrate was carbon-coated.

The original design of the entrance and exit tunnels was based on a design speed of 15 cm/min. The most interesting result is that at this high speed there has been little warping and no cracking of any substrates. This is true of the original design as well as all subsequent modifications.

The problem is that without forced convective cooling or use of an asymmetric growth mode, there is no chance of getting the desired silicon thickness at high speed. The thickness is needed to demonstrate slot coverage and cell performance. Thus, we wanted to do initial coatings in the range of 4 to 6 cm/min. At these lower speeds, the substrates have warped, buckled, or cracked. The proposed explanation is that the longitudinal temperature profile must be the cause of the problem. At high speeds, the longitudinal profile is smoother than at low speeds because the heat capacity of the substrate causes a temperature lag. Thus, the purpose of the changes in tunnel design has been to linearize the temperature profile. Fortunately, this has reduced the problem at low speeds, and has not created any problem at high speeds.

The explanation in terms of thermal stresses caused by longitudinal temperature gradients is the same as that proposed by Surek for edge-defined, film-fed ribbon growth or EFG.[1] The origin of thermal stress and the strategy to avoid it are discussed in SOC Quarterly Report No. 15, published 31 July 1980.

As discussed by Surek,[1] the equation for the stress is

$$\sigma_{xx} = \frac{\alpha E b^2}{\sigma} \left(1 - \frac{3y^2}{b^2} \right) \frac{d^2T}{dx^2} \qquad (1)$$

in the case where the second derivative of the temperature is significant. Here, α is the expansion coefficient, E is young's modulus, and b is one-half the substrate width. The solution is positive at the center (y = 0) and

[1] A. D. Morrison, et al., "Large-Area Silicon Sheet by EFG," Mobile Tyco Energy Corporation Annual Progress Report, September 15, 1976.

negative at the edges ($y = \pm b$), indicating tension and compression, respectively, when d^2T/dx^2 is positive. At the ends of the substrate, the solution is not valid, since $\sigma_{xx} = 0$. Thus, in the vicinity of the end, there are σ_{yy} and σ_{xy} stresses which can also be derived analytically.[1]

It is obvious that the temperature profile cannot be entirely linear in any substrate which is heated and then cooled and that both types of nonlinearities must be encountered, as shown in Fig. 21. Thus, thermal stress must always exist. However, there is a strategy which, at least in principle, can reduce the residual thermal stress to zero.[1] This strategy is detailed in Fig. 21. The idea is to have the concave portions of the profile in regions with high yield stress. Thus, thermal stresses do exist, but they result only in elastic deformation so that when the sample is again in a $d^2T/dx^2 = 0$ region, the residual thermal stress is zero.

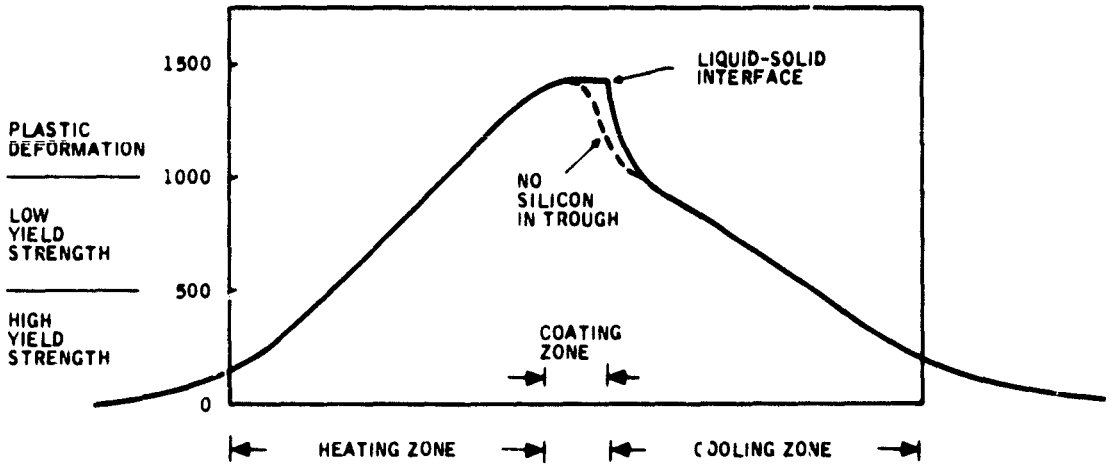


Figure 21. Strategy to eliminate effects of thermal stress. In the high-temperature regions, the ceramic can deform without buckling or cracking, and stress in the silicon is annealed as it is generated. At low temperatures, only elastic deformation occurs. The intermediate temperature ranges are critical, and the temperature profile must be linear.

At sufficiently high temperatures, the yield strength of both the ceramic and the silicon is low so that the sample can undergo plastic deformation with no buckling or cracking. Stress relaxation studies in silicon[1] show that at 1000°C the stress relaxation time is a few seconds Thus, in the vicinity of the trough and especially at the liquid-solid interface, the

presence of large nonlinearities in the temperature gradient will not have harmful effects.

In summary, the strategy is to consider the problems in terms of three temperature zones. The following strategy applies to both the heating and cooling zones:

a) The high-temperature zone ($T \geq 1000^{o}C$) can tolerate large nonlinearities in the temperature profile.

b) The intermediate-temperature zone ($1000^{o}C \geq T \geq 700^{o}C$) must have a very linear profile.

c) The low-temperature zone ($500^{o}C \geq T$) can tolerate large nonlinearities such that the thermal stress does not exceed the elastic limit of silicon on ceramic.

According to the design strategy based on stress analysis (Fig. 21), a linear longitudinal temperature profile is sought for the temperature range of low yield strength, from 500 to $1000^{o}C$. The linear profile is necessary in both heating and cooling in order to eliminate or at least greatly reduce residual stresses in the coated ceramic panels. A second requirement is to provide rapid initial cooling of the coated substrate, as prescribed by heat balance at the silicon liquid-solid interface. The second requirement will not be in conflict with the first one if rapid cooling is restricted to the plastic deformation region, as indicated in Fig. 21.

It is expected that the thermal design of a production coater can be optimized for a given fixed feed rate. In the experimental growth system, thermal design is complicated by the need to accommodate more than one feed rate; an ideal temperature profile is difficult to maintain over a wide range of feed rates. At low speed, the substrate is likely to heat up over-rapidly on first entering the heating chamber. At higher speeds, this is moderated by the thermal inertial time lag. On the other hand, high-speed panels tend to emerge from the cooling chamber insufficiently cooled. The first problem can be eliminated by heat-sinking at the entrance to the heating chamber, whereas the second problem is relieved by heat-sinking at the exit from the cooling chamber. A more flexible means of accommo-

dating different speeds is to vary the amount of insulation placed in the respective chambers.

A great deal of insight into these and other aspects of the thermal design problem has been provided by a mathematical analysis of the heating and cooling chambers. A brief thermal description of the mathematical models follows.

The substrate panels are transported at ambient temperature to the heating chamber, which is shown in schematic cross section in the left half of Fig. 22. This is made up of pairs of active heaters, carbon guides (also functioning as the passive heaters), and insulating layers. The 1mm-thick ceramic substrates move left to right between the guides, acquiring heat by radiation from the guides, so that they reach 1693K when they arrive at the right end of the tunnel. At this temperature, the melting point of silicon, they are ready for silicon coating in the chamber immediately to the right. It will be noted that the moving substrates extract a total of $\rho Cwt\Delta T$ joules of heat per centimeter of length, where ρ and C are the density and specific heat, w and t are panel width and thickness, and ΔT is the temperature rise. If the panel feed rate is v cm/sec, the active heaters then must supply energy at a rate greater than $\rho Cwt\Delta T$ watts. The "greater than" may be made to approach "equal to" if wasted heat is minimized; that is, the quantity and placement of insulation are such as to prevent significant losses to the water-cooled case.

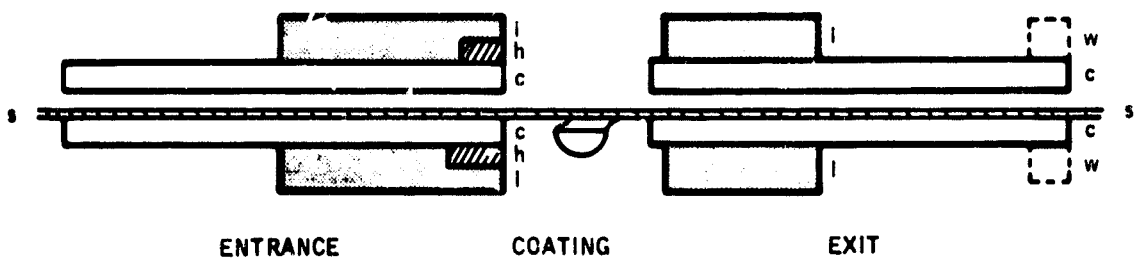


Figure 22. Schematic cross section of SCIM-II showing simplified arrangement of various thermal elements used in modeling. h = resistive heater; c = carbon (guide); i = insulation; w = heat sink (when present); s = substrate.

After the silicon coating step, the substrates traverse a cooling chamber (right half of Fig. 22) of similar geometry to the entrance tunnel. The important difference is the omission of the active heaters. However, the water-cooled case and variable insulation are essential. Inasmuch as cooling is passive with the case being the heat sink, the carbon guides are a hindrance to cooling though needed for mechanical support. The guides act like heat shields, interrupting the radiative transfer from silicon-coated panels to the case. The important heat escape path is vertical from substrate to guide to case, with a lesser contribution by way of longitudinal conduction through the guides.

The need for design flexibility is reflected in the variable structure of the mathematical models; provisions are included also for experimental calibration:

- The amount of insulation used in the heating and cooling chambers can be varied. Adjusting insulation may be the quickest and easiest way to set up different substrate speeds.

- The far ends of the cooling chamber guides have tended to reach excessively high temperatures in both theory and practice. The theoretical model includes an optional heat sink at these ends.

- "Standby" versions of the models have been provided. These represent heating and cooling chamber with heaters active but no substrate present. The main purpose for these versions is to calibrate the models against temperature measurements, which are normally taken with the chambers empty.

Only longitudinal temperature profiles are analyzed here, since these are believed to be associated with warping and breakage. Transverse temperature variations also occur and are discussed elsewhere. The main problem caused by transverse variations is coating nonuniformity, and this is being successfully attacked by heater redesign.

The physical relationship upon which the thermal models are based will next be summarized. All temperature profiles are assumed to be one-dimensional; thus, variations in the transverse direction are ignored. Several thermal elements interact with one another (Fig. 22) so that as many as five coupled heat equations must be solved. Basically, the electrical input produces heat in the resistive heaters (h), and this heat spreads along both heating

chamber guides (c) by thermal conduction. In the steady state, the heated guides release part of this energy by radiation to the entering substrate(s) and the rest is lost by radiation and conduction to the ambient. The model includes a convective heat transfer coefficient, but this has been set equal to zero in the calculations reported here. A significant portion of the heat loss takes place from insulated surfaces due to the limited thicknesses of carbon felt. The substrate(s) acquires heat from the guides so that its temperature increases from approximately ambient at the left to the coating temperature ($1420^{o}C$).

In the cooling chamber, the process is essentially reversed. The substrate is progressively cooled by radiation to the cooling chamber guides and by conduction in the downstream direction. Because of the heat-shield effect, the cooling rate is lower than it would be in the case of direct radiation to the 300K ambient. The cooling problem is further aggravated at the far (right) end because thermal conduction within the guides tends to elevate the temperature at that end. This effect can be greatly relieved by heat-sinking (w).

End effects are found to be significant and are included both at the external end facing the cool environment, and the internal ends facing the coating chamber. Not only the actual end surfaces are affected but also parts of the internal surfaces close to the ends The moving substrate is not completely cooled when it emerges from the cooling chamber. It is important that enough cooling has taken place at this point to avoid a further precipitous temperature drop outside of the chamber. In the numerical calculations, a practical approximation is required for the boundary condition at infinity. We use $T = T_{o}$ (room temperature) at a point some distance (a few cm) beyond the tunnel end. Over this distance, the radiation environment is assumed to be at temperature T_{o}. It is easily verified that the approximate boundary condition does not affect the numerical solutions for the temperature within the chamber. Figure 23 shows calibration of the model against measurements taken by using a thermocouple instead of the substrate.

The finite-difference grid for the heating chamber represents 1cm increments in longitudinal position, or 41 points for a 40cm tunnel. Since there are five coupled layers (two heater-insulation layers, two guides, and one substrate), there are $5 \times 41 = 205$ nodal equations which are solved by a

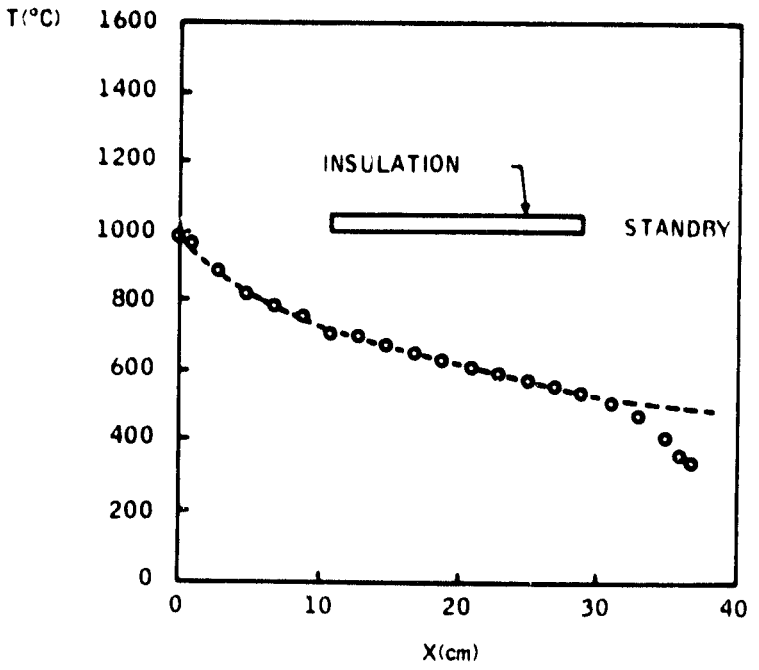
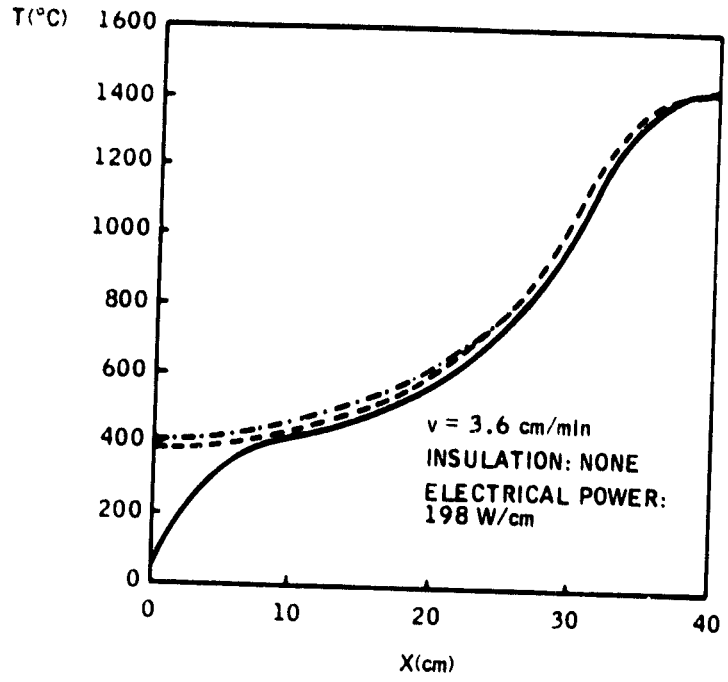


Figure 23. Calculated versus experimental exit tunnel temperature with no substrate in chamber.

direct-inversion method for sparse matrices. The matrix has a bandwidth of 11 and is asymmetric due to the moving substrate. Since the radiation law is nonlinear and thermal conductivities are temperature-dependent, the equations are resolved iteratively with updated coefficients for the nodal equations. Convergence occurs in about 20 iterations. For the cooling chamber, a finer grid (0.33cm) is used, but heater-insulation layers are not required.

Heating Chamber (Entrance Tunnel) Results - Calculated temperature profiles are shown in Fig. 24 for two substrate speeds. The solid curve gives the substrate temperature and the dashed curve gives the mean guide temperature. (The two guides may differ up to 20°C from each other at any x position.) The third curve consisting of dashes and dots, represents mean guide temperature under standby conditions-the same electrical input but no substrate.



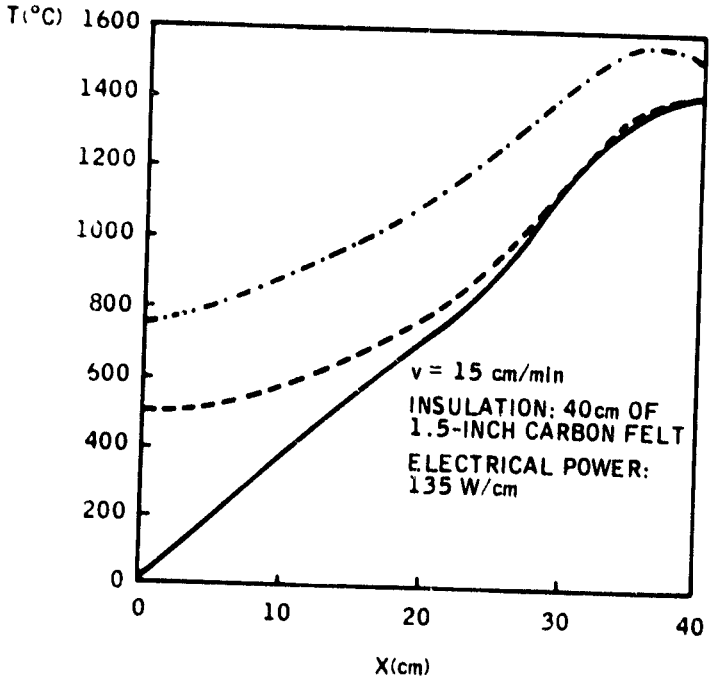


Figure 24. Calculated entrance tunnel profiles corresponding to slow and fast operation. Guides are 0.5 inch thick and the channel height is 0.5 inch. The solid profile corresponds to the substrate; the dashed to the guides under operating conditions; and the dashed and dotted to guides in standby conditions with same electrical input.

The high-speed substrate profile is nearly linear, indicating optimum design for high speed. Electrical input is 135 W/cm of width, of which 92 W/cm heats the substrate, the rest being absorbed by the ambient environment. The standby profile is considerably elevated because the entire 135 watts is wasted to the environment, thus requiring a higher average radiation temperature.

The low-speed profile demonstrates some of the difficulties encountered in trying to optimize the basic chamber design for a range of substrate speeds. With all the insulation in place, the initial temperature rise in the substrate is extremely rapid. This is moderated by removing all of the insulation, giving the indicated profile, which is still somewhat too steep and has excessive curvature. The curvature is initially convex but becomes concave in the middle due to the large radiation losses from the guides. It becomes convex once again at the end, where the active heaters are located. The electrical input, 198 W/cm, is almost totally wasted, with only 12 W/cm required to heat the substrate. As discussed in SOC Quarterly Report No. 13, published 15 February 1980, the theoretical profile for the low-speed case is best improved by increasing the thermal resistance of the guides - for example, reducing their thickness. A compromise solution is being investigated experimentally; carbon has been removed in transverse grooves at the ends of the guides.

Cooling Chamber (Exit Tunnel) Results - The substrate temperature distribution in the cooling chamber should satisfy two requirements: (1) a large initial gradient to carry the latent heat of fusion out of the grown silicon layer; (2) a nearly constant gradient from 1000°C to 500°C. As previously explained, these requirements are difficult to satisfy simultaneously under all conditions. The location of the insulation is critical; since the cooling curve has the greatest curvature at high temperatures, the insulation should be placed fairly close to the beginning of the chamber. On the other hand, the first requirement demands a fast initial cooling, and this dictates leaving a finite uninsulated gap at the very beginning. A 1cm gap was found to be sufficient to retain the full initial cooling rate. The next approximately 18cm of both guides are insulated for present experimental work, and the same insulation interval (1 to 19cm) was used in the numerical calculations plotted in Fig. 25. The effects of this insulation are readily observed by comparison with Fig. 26, which represents the uninsulated case.

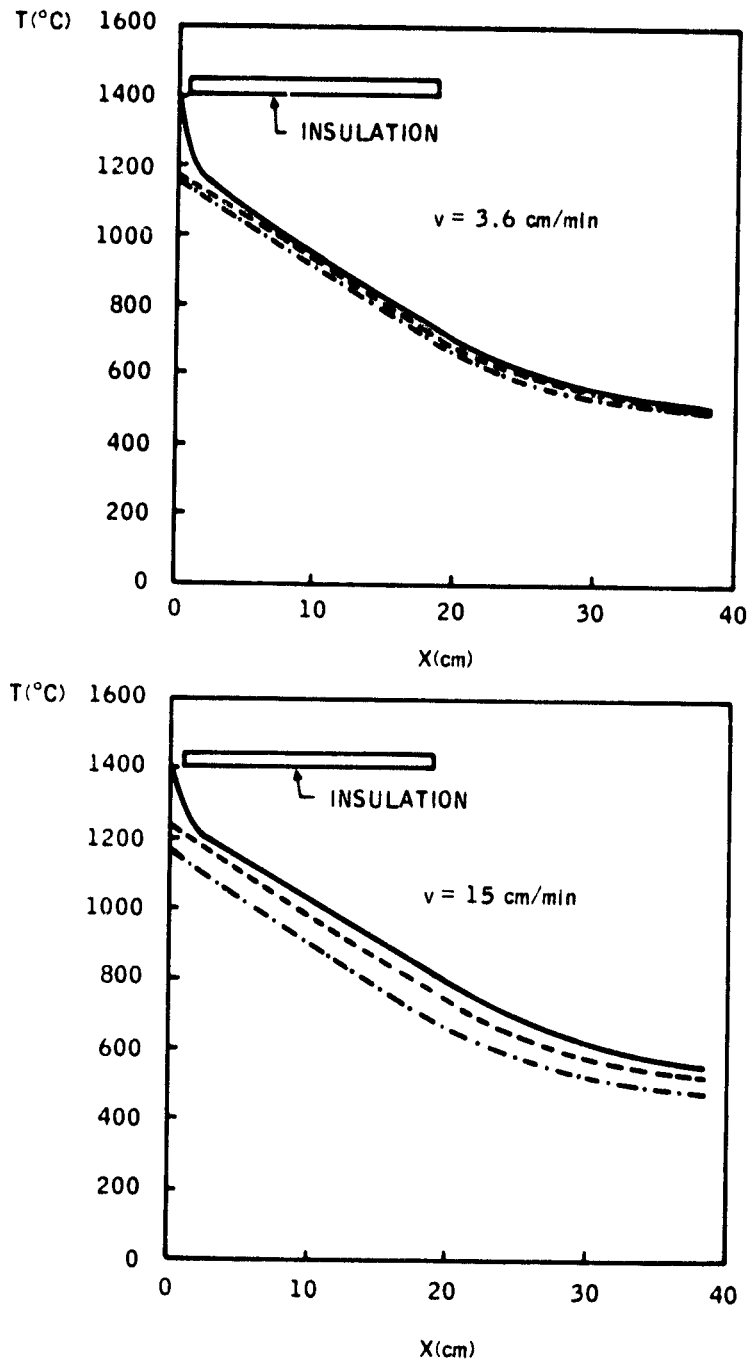


Figure 25. Calculated exit tunnel profiles at different speeds with insulation located as indicated (carbon guides are not heat-sunk). The solid profile corresponds to guides under operating conditions, and the dashed and dashed-and-dotted profiles to guides in standby conditions with different electrical inputs.

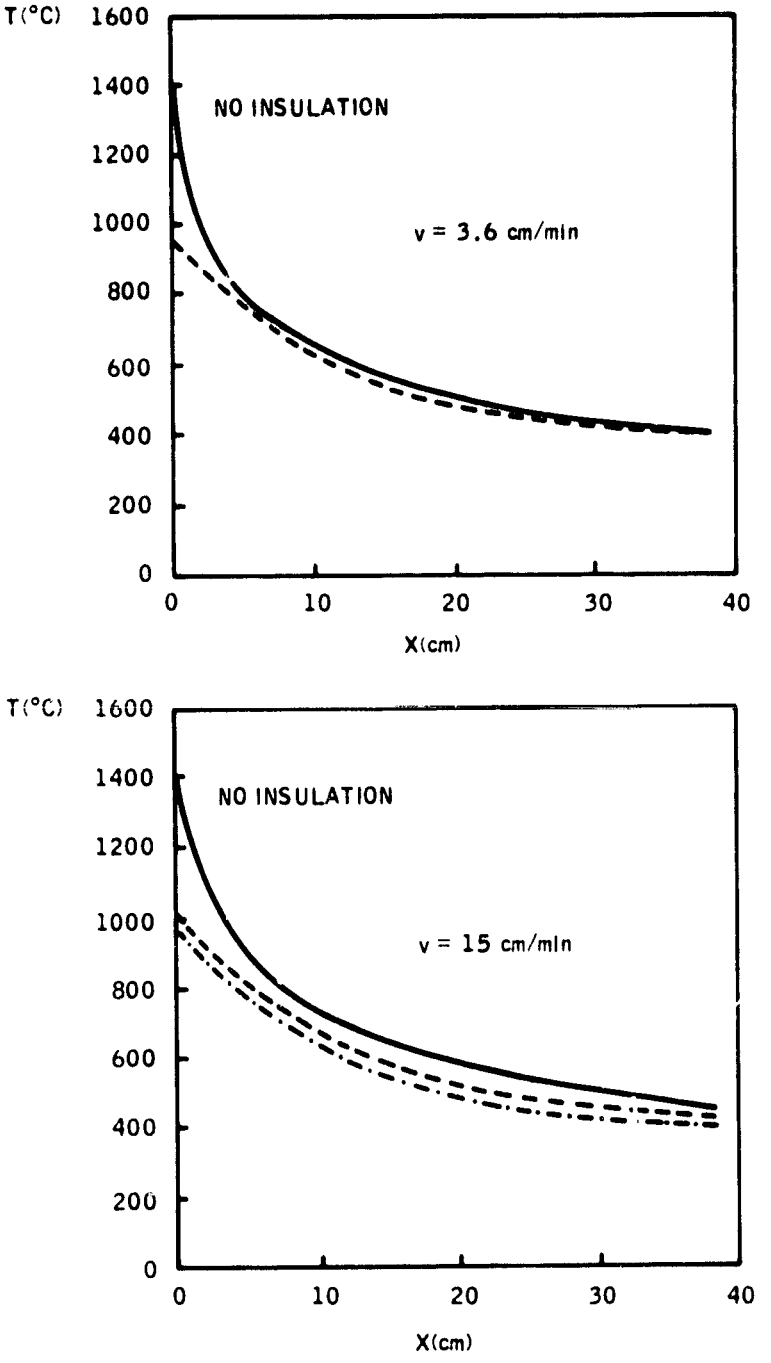


Figure 26. Calculated exit tunnel profiles at different speeds without insulation. Carbon guides are not heat-sunk. The solid profile corresponds to substrate; the dashed profile corresponds to guides under operating conditions; and the dashed-and-dotted profile corresponds to guides in standby conditions.

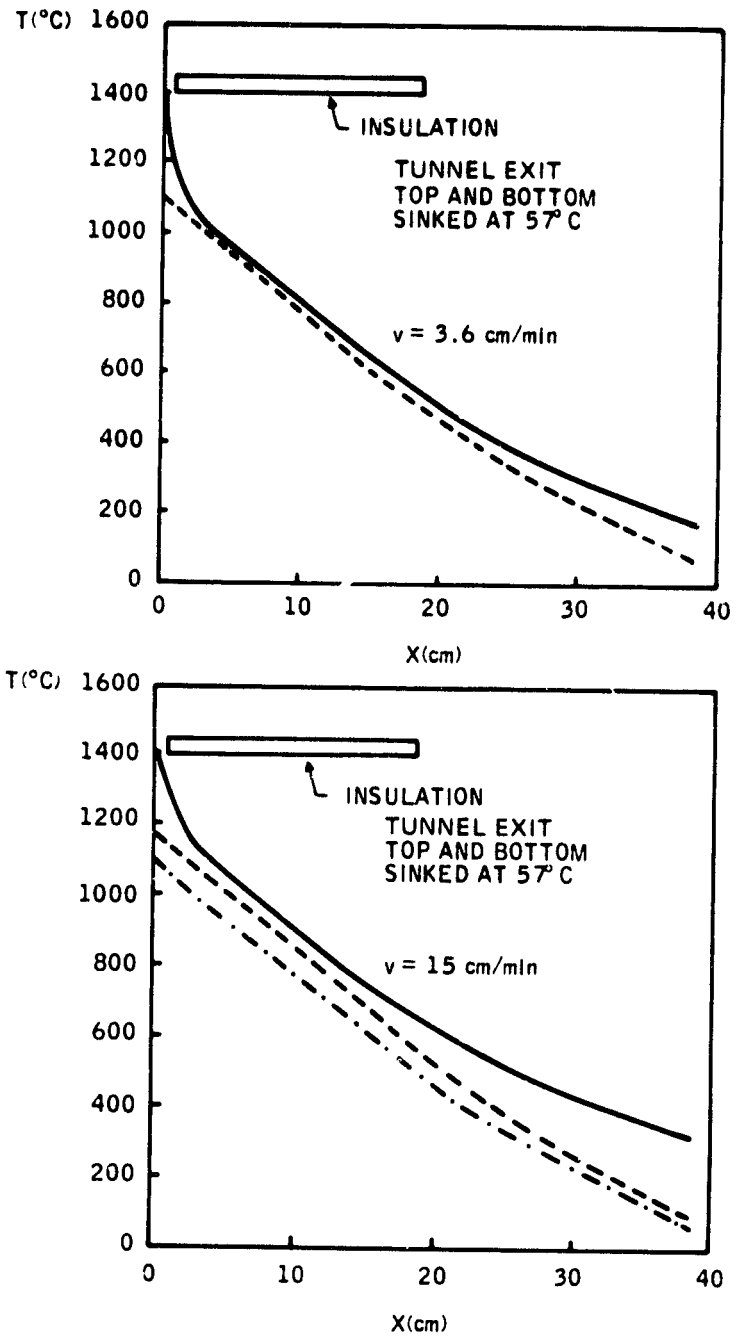


Figure 27. Calculated exit tunnel profiles with heat sink at exit end. The solid profile corresponds to substrate; the dashed profile corresponds to guides under operating conditions; and the dashed-and-dotted profile corresponds to guides in standby conditions.

As discussed above, the high exit temperatures are intolerable. A water-cooled heat sink was therefore added at each guide end, and, according to calculations (Fig. 27), a substantial lowering of the exit temperature was expected. As discussed below, this was indeed the result.

To eliminate this substrate warpage and breakage in practice, a large number of modifications were made in the system:

- Entrance tunnel heaters were simplified and moved forward.
- The side heaters were found to be unnecessary with the new entrance tunnel heaters.
- The method of measuring temperature profiles was improved by relocating the thermocouples.
- Insulation was added or removed as required to obtain the desired profile.
- The trough heater was designed to compensate for unavoidable conduction and radiation heat loss nonuniformities.
- The exit tunnel was connected to a water-cooled heat sink as indicated by modeling and by measurements.
- Closed-loop control for the temperature in the trough was implemented.
- The angle of the quartz trough was changed so that it tilts backwards in operation.

These modifications gave much improved operation.

Temperature Profile Measurement - Careful measurement shows that when the thermocouple is inserted from the entrance port, the reading is different from when the same thermocouple is at the same position when inserted from the exit port of the coater. The discrepancy is opposite to that expected on the basis of conduction of heat along the thermocouple. For example, the temperature above the trough is 30 degrees hotter when measured from the exit port, where heat is conducted away from the probe. The only reasonable explanation for the discrepancy is that the thermocouple is responding to the direct radiative environment and that the presence of the ceramic probe blocks the radiation. Thus, in the above example, the probe

pointed toward the hot entrance tunnel reads hotter than when it is pointed at the cold exit tunnel. A different method of reading the temperature profiles was adopted. A series of thermocouples was installed by drilling holes into the half-inch plates and cementing a thermocouple into each hole. The results of the measurements which followed are discussed below.

The temperature of the exit-tunnel plates as indicated by the type-K thermocouples shows a sharp discontinuity at the edge of the insulation. This result also follows from the thermal modeling (see Fig. 27). Figure 28 plots this profile and sketches the insulation position. The function of these carbon plates is to take the sample from a high temperature, where the

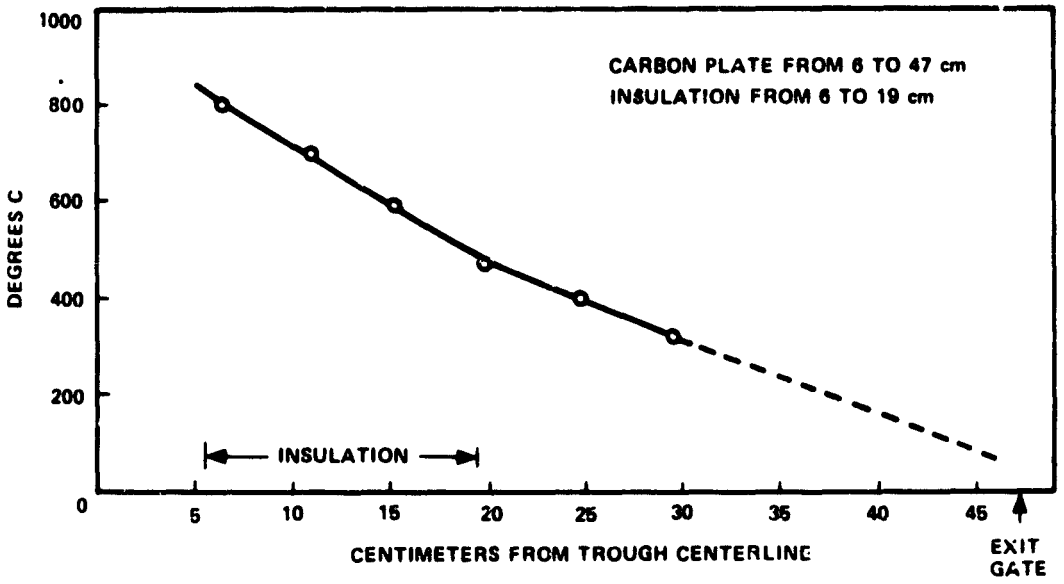


Figure 28. Temperature profile of partially insulated exit tunnel. The horizontal scale is measured in cm from the center of the trough. The data were taken with thermocouples imbedded in the carbon plates to avoid radiative coupling problems.

ceramic is soft, smoothly down to a low temperature where the sample is strong enough to withstand the strains (Fig. 21). There is a change in slope at the end of the insulation. In this case, breakage of substrates occurred presumably due to the sizeable second derivative in the profile. Figure 29 shows the case where there was no insulation at all, and the profile is quite linear. Obviously, no insualtion is not very energy efficient.

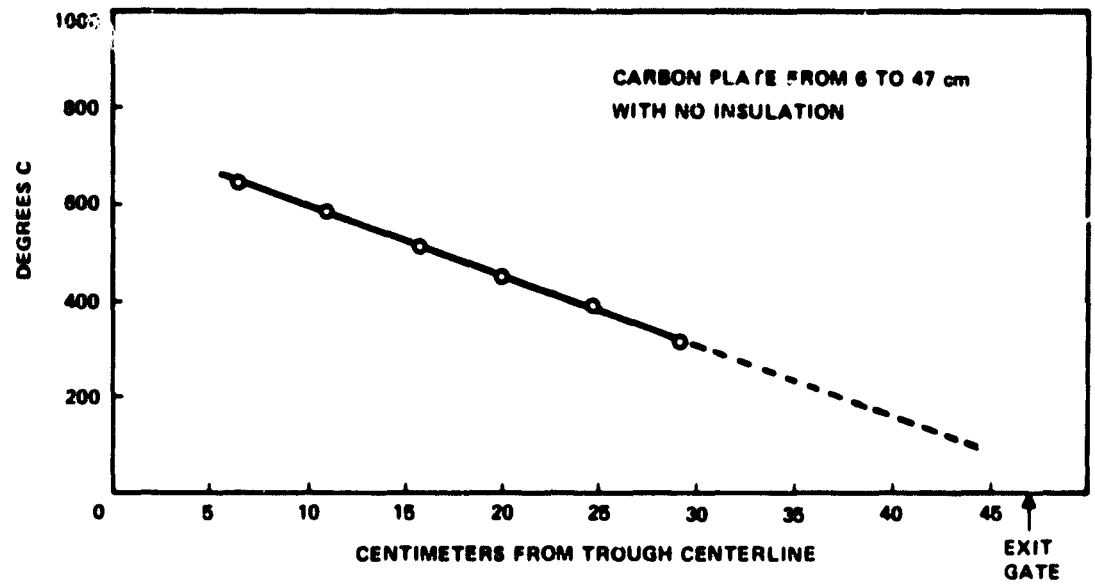


Figure 29. Measured profile of uninsulated exit tunnel.

It also prevents bringing the leading edge of the exit tunnel up to the 1000°C temperature range required by the mullite. We then covered the exit tunnel with a uniform layer of graphite felt from the leading edge of the carbon all the way back to overlap the water-cooled copper plates. Figure 30 shows the profile of the present exit tunnel and shows the position of

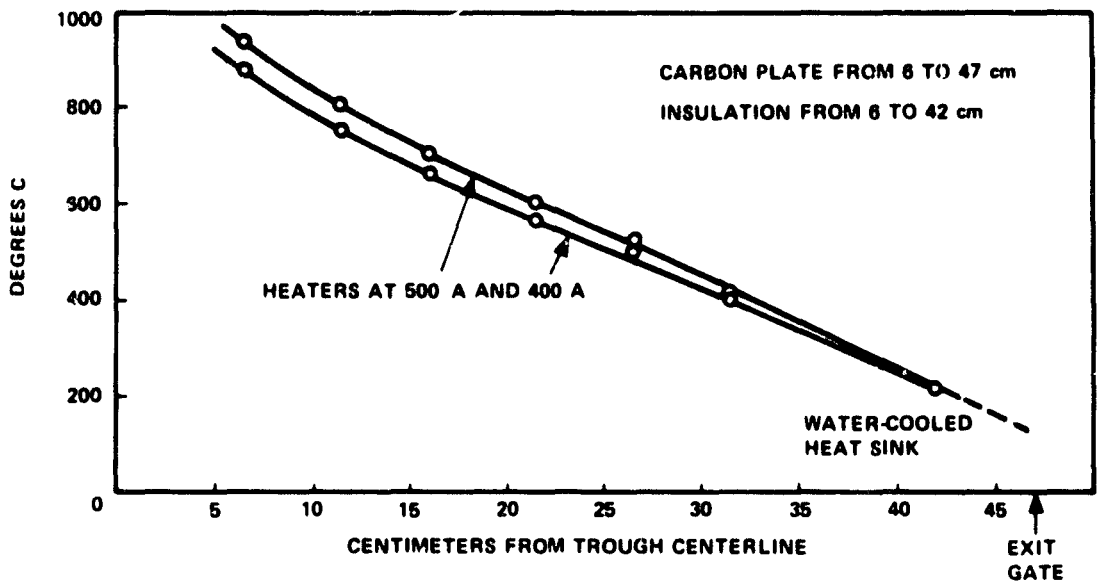


Figure 30. Measured profile of exit tunnel with insulation along full length.

the insulation and water-cooling. A similar set of thermocouples was mounted in the entrance tunnel to provide a profile of the entire SCIM-II coater. Figure 31 is a plot of the profile of the entrance and exit tunnels at two different input power levels. Considerable crosstalk between the trough heater temperature and the entrance tunnel heaters is indicated by the fact that the trough heater alone cannot reach 1400°C. Also note the 900°C temperature at the leading edge of the exit tunnel corresponding to 400 A. Under these conditions, thermal stresses were excessive. We have concluded that at 900°C the exit tunnel is too low to begin cooldown on the substrate, whereas at 1000°C or more the 10cm by 100cm samples do not buckle at low or high speeds.

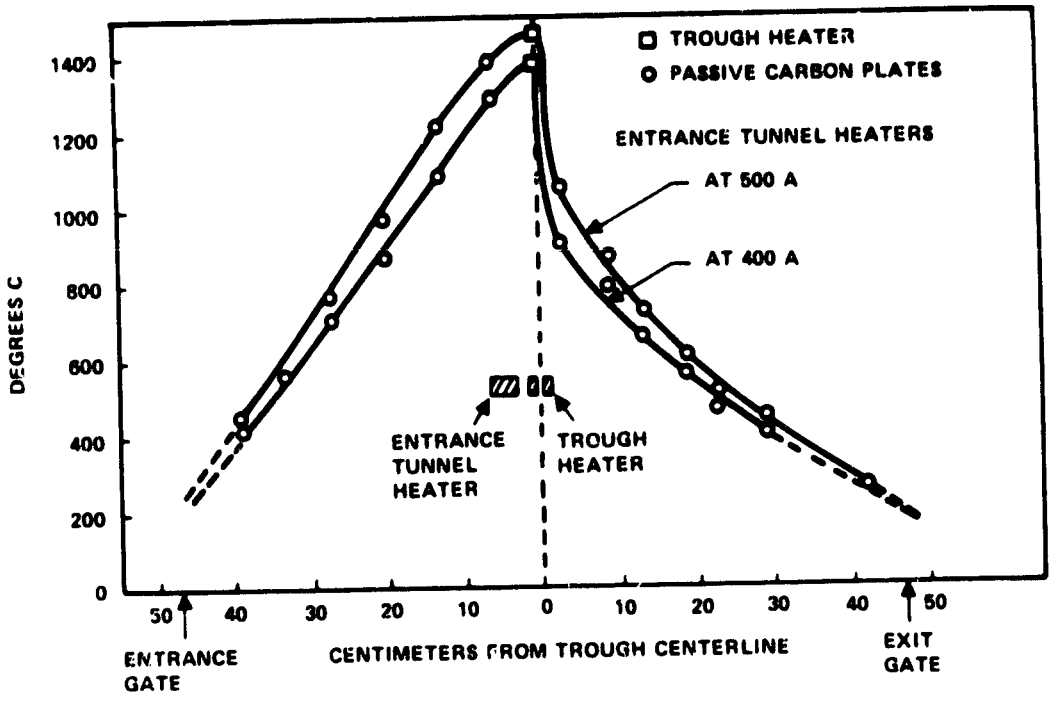


Figure 31. Measured profile at two heater powers.

The data in Figs. 28 through 31 all have been taken without samples or silicon in the trough. Figure 32 is the operating profile of SCIM-II, including all of the following cases:

- Substrates going through from 3 to 10 cm/min
- No substrates at all

- Silicon in the trough
- No silicon in the trough
- Coating SOC at 5 cm/min

The height of the bars shows the total variation in temperature under these conditions. This variation was only ±20°C at the most critical point (at the leading edge of the exit tunnel). With these conditions, the system can coat silicon on 10cm x 100cm ceramic substrates without buckling or cracking due to thermal stress.

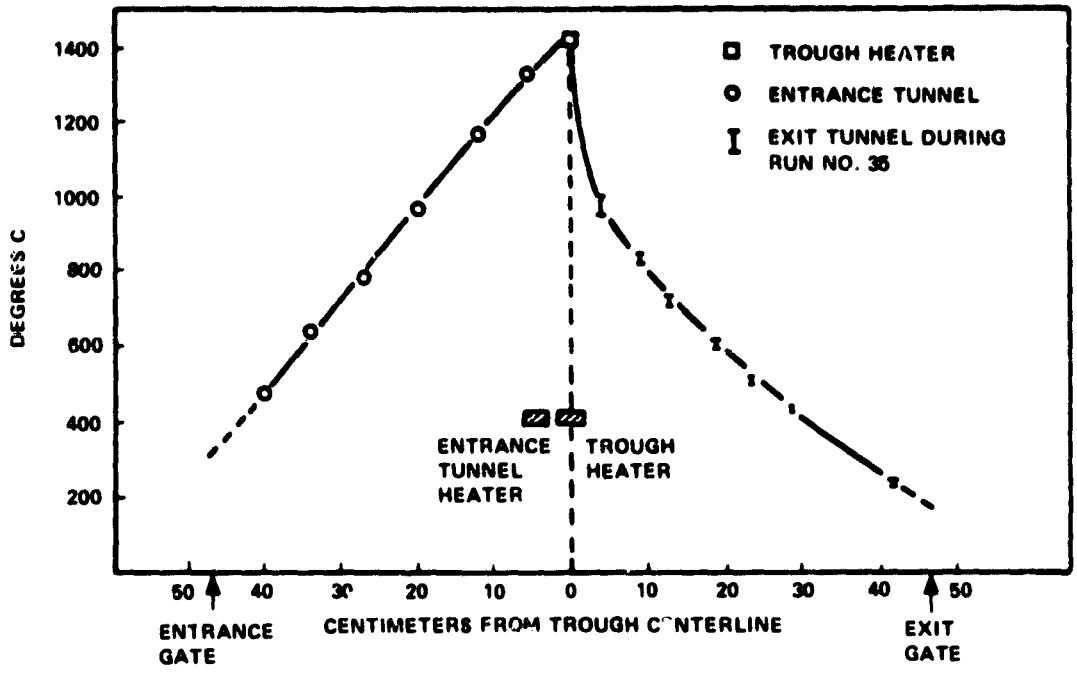


Figure 32. Measured profile during a coating run.

Heater Insulation - Resistive carbon heaters are designed and built to surround the crucible or trough as much as possible. For the entrance tunnel, the heaters are adjacent to the carbon plate to be heated. In these cases, only one side of the heater sees the material to be heated, whereas the other side (outside, backside) radiates into some free-standing insulated structure which should act as a radiation shield. As the element to be heated approaches operating temperature, e.g., 1400°C in our system, it no longer requires a great deal of power from the heater, whereas the box

between the heater and the insulation that is holding the insulation continues to drain power from the system.

Three of our four heaters have been modified to minimize this loss and focus the radiation in the direction intended, by simply attaching the insulation directly to the electrically active heater element. The structure to hold the insulation is now the heater itself and no longer need be the elaborate structure previously used. The hottest part of the heater is now in contact with the insulation with reduced radiation, convection, or conduction losses on that side. The bare portion of the heater still radiates directly into the intended heat sink.

The insulation on the top entrance tunnel heater is simply a straight flat blanket cemented on top of the heater. The bottom heater is identical except for the insulation being underneath. The trough heater is somewhat more elaborate in that three sides of the heater are insulated at the end where the current connections are made, two sides are insulated where the heater reaches into the crucible container and nearly touches the crucible heater. There is a small stretch of three-side insulation between the crucible box and the coating area as well. All along the trough heater the insulation is divided, since there is a voltage drop between the two sides. The 2mm gap in the heater is sufficient to maintain separation of both heater and insulation. Figure 33 gives a cross-sectional view of heaters, plates, and insulation.

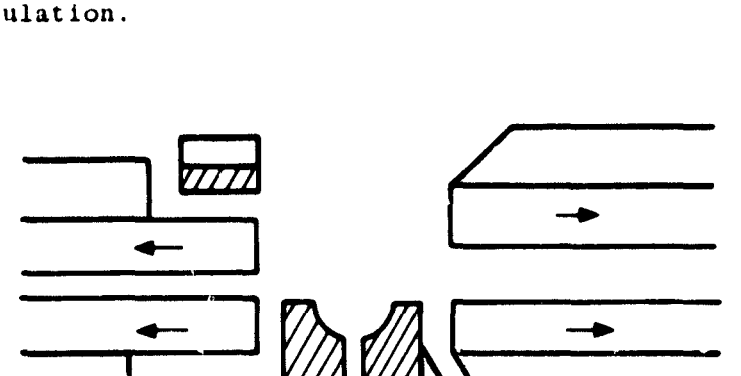


Figure 33. Schematic cross section of coating zone, including heaters, insulation, and passive plates.

Coating results using this thermal configuration are reported in the Sheet Silicon Growth section of this report.

CERAMIC SUBSTRATE DEVELOPMENT EFFORT

Introduction

Early in 1975, when silicon dip-coating was first conceived, carbon appeared to be a logical choice as a substrate material. Small substrates were machined from graphite and dip-coated with silicon. Thin, smooth silicon coatings were produced having columnar grains similar in structure to the most recent SOC layers. Samples of Grafoil (a graphite foil) were also dip-coated at that time with surprisingly good results. A promising characteristic of carbon or graphite was the fact that it is electrically conductive and could conceivably form the back contact to the silicon layer. A preliminary investigation, however, into the economics of carbon substrates proved to be unfavorable and our attention turned to ceramic as a potentially low-cost substrate material. Sections of mullite tubing were then cut up into small substrates and successfully dip-coated with silicon. In the early phase of this program, Honeywell's Ceramic Center was asked to assist us in selecting a suitable ceramic.

Later in the program, we learned of Coors Porcelain Company's expertise in large-area substrates and they were consulted and subsequently very much impacted the SOC effort. The results of these efforts are discussed below.

Ceramic Material Selection

The Honeywell Ceramics Center played an important role in helping us in the selection of a suitable ceramic material. This selection had to be made on the basis of thermal expansion coefficient, thermal shock resistance, chemical purity and, most importantly, cost.

The Ceramics Center, in addition to purchasing or developing substrate materials, spent time examining several processing approaches, which could be scaled-up to produce square-meter-size substrates. These approaches included rolling, casting, doctor-blading, and hot-pressing. Rolling of a high-plasticity, mullite material was examined and substrates as large as 500cm^2 were formed and fired. Rolling and doctor-blading of a calcium-

aluminate bound alumina material were shown to be feasible. Casting and doctor-blading of silica substrates were demonstrated. Hot-pressing of fiberglass products into large, 500cm^2 sheets was also accomplished.

Standard 5cm x 7cm test samples for this program were prepared or received from vendors as indicated in Table 1. Each of these materials is discussed in the paragraphs that follow.

Table 1. Substrate materials investigated.

Material	Trade Name	Source	Fabrication Process	Firing Temperature
Mullite	MV-20	McDanel Corp.	Rolling	1640°C 20% glass
Mullite	MV-30	McDanel Corp.	Casting	-- 15% glass
Mullite	Fiberfrax	Carborundum	Hot pressing	1400°C
Mullite		American Lava	Pressed	
Cordierite	Alsimag 701	American Lava	(purchased)	--
Cordierite	A-3171	Du-Co	(samples)	--
Alumina	Alsimag 614	American Lava	(purchased)	-- 96% Al_2O_3
Alumina	Alsimag 798	American Lava	(purchased)	-- 85% Al_2O_3
Polygranular SiO_2	GP-31	Glasrock Products, Inc.	Casting	1160°C 1400°C 1640°C
Calcium Aluminate	CA-25	Alcoa	Pressing and rolling	60°C 1160°C 1640°C
Zirconia	Alsimag 475	American Lava		
Sapphire	To be acquired			

Mullite - Mullite is an aluminum silicate compound ($3Al_2O_3 \cdot 2SiO_2$) which is available in many forms. The crystalline material has a melting point of about 1850°C, but up to 30% glassy phase is commonly found in this material, which lowers the softening temperature. The thermal expansion and conductivity of mullite is about 5 x 10^{-6}/°C and 3.5 Btu/hr-ft°F, respectively, and its theoretical density is 3.26 gm/cc. Four types of mullite were initially obtained for this program:

- Honeywell rolled MV-20
- McDanel cast MV-30

- Honeywell hot-pressed Fiberfrax
- American Lava pressed material

McDanel mullite composition MV-20 was procured in a plastic extrudable form. Test substrates (5 x 7 x 0.2cm thick) were produced by rolling the material over a smooth, oiled surface and controlled drying and firing to 1640°C. After rolling, the sheet material was cut to oversized 5cm x 7cm coupons. The coupons were dried between flat plaster of paris blocks for 20 hours at 60°C. They were then bisque-fired on mullite sagger plates to 600°C and finally high-temperature-fired (on mullite) to 1640°C. Several larger 7cm x 12cm substrates and 20cm x 22cm substrates were successfully prepared of this material by the rolling methods.

A second McDanel mullite composition, MV-30, was procured in fired tubular form. Eight test coupons were cut from this material. The MV-20 and MV-30 materials typically contain 20 and 15% glassy phase after firing, respectively.

Additional test samples of experimentally pressed mullite substrates were received from American Lava Division of 3M Inc. Rigid sheets of mullite fibers were also formed by pressing double or triple layers of Fiberfrax (1.2mm-thick Carborundum sheet) under a load at 1400°C. Flat, very porous, rigid sheets 1mm to 1.5mm thick with a density of 0.5 gm/cc were formed by this process.

Alumina - Alumina substrates are the most common type of flat ceramic material used for electronic curcuitry. Pure Al_2O_3 has a melting point of about 2000°C and a thermal expansion and conductivity 6.7 x 10^{-6}/°C and 10 Btu/hr-ft-°F, respectively. The theoretical density of this material is 3.98 gm/cc.

Two types of alumina substrates were obtained from American Lava for this program, namely pressed 96% and 85% alumina. These are designated as Alsimag 614 and 798, respectively. A third type of alumina was fabricated at Honeywell by rolling, pressing, and doctor-blading a calcium-aluminate bound alumina material. Table 2 gives four compositions that were formulated from Alcoa CA-25 calcium aluminate cement and tabular alumina filter. The consistency of the mixture was varied by addition of water based on the method of forming.

Table 2. Honeywell Ceramic Center formulation data.

Formulation No.	Materials	Proportions (% by wt)	Water (% by wt)	Forming Methods	Drying (60 C)	Bisque Firing (900 C)	H. T. Firing (1160 C)	H. T. Firing (1400 C)	H. T. Firing (1640 C)
1	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	55 30	20	Casting	X				
2	Glasrock GP-31	100	20	Casting	X X	X X	X	X	
3	Glasrock GP-31 Glasrock GP-71	80 20	19	Casting	X X	X	X		X
4	Alcoa CA-25 Tab. Al_2O_3-325	15 85	10	Pressing	X	X	X		
5	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	15 70 15	12	Pressing	X	X	X		
6	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	15 55 30	10 15 ± 2	Pressing Rolling	X X X X	X X X X	X X		X X
7	Carborundum Fibertrax			H. T. Sinter				X	

Smooth compress surfaces with no sticking were obtained at 5000-psi pressure. No apparent warpage occurred during firing. Rolled substrates had some surface roughness, and slight warpage occurred during high-temperature firing. These materials were still somewhat porous but still had a density over 3 gm/cc.

Zircon - Zircon is a zirconia silicate ($ZrO_2 \cdot SiO_2$) compound with a melting point of 1530°C and theoretical density of 4.68 gm/cc. The thermal expansion and conductivity of this material is 6.0 x 10^{-6}/°C and 3.8 Btu/hr-ft-°F, respectively.

Cordierite - Cordierite is a magnesium aluminum silicate ($2M_5O \cdot 2Al_2O_3 \cdot 5SiO_2$) with a melting point of 1200°C; however, slightly different modifications may be as high as 1400°C. This material has a thermal expansion of 1.5 x 10^{-6}/°C.

Sample Cordierite substrates were obtained from the following two suppliers:

- Minnesota Mining and Manufacturing Co. (3M - Alsimag 701)
- Du-Co Ceramics Co. (A-3171)

A specimen of each material was fired at 1500°C with the results shown in Fig. 34. Both materials show leaching out of a lower melting-point constituent. The 3M material retained its shape, but the Du-Co material melted completely. The Du-Co material was therefore not evaluated for the silicon dip-coating application.

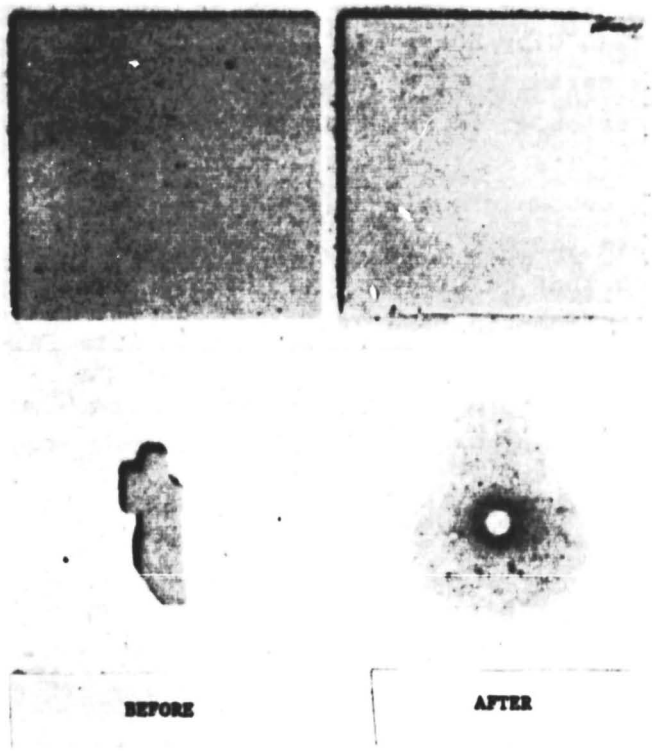


Figure 34. Cordierite substrate samples.

Silica - Silica in powdered form was procured from Glasrock Products. This Glasrock grade "I" material (99% SiO_2) was of two particle sizes designated GP31 (Fisher sieve 2.0) and GP71 (Fisher sieve 4.5). Two formulations were made (see Table 2). In each case, a slip was prepared by high-shear mixing of the solid ingredients and water. The material was then cast on a flat porous substrate. The castings were dried at 60°C, and subsequently high-temperature-fired at either of two higher temperatures (see Table 1).

A slight warpage of the cast sheets occurred after high-temperature firing. This was attributed to a nonuniform particle size distribution through the sheet thickness. The fired substrates appeared to have adequate structural strength for subsequent processing.

With the exception of the cordierite substrate, all of the ceramics previously discussed were dip-coated with varying degrees of success. All of the materials with the exception of American Lava's pressed mullite withstood the thermal shock of being immersed into molten silicon with only a relatively short preheat cycle prior to their immersions. Of those listed, the McDanel MV-20 mullite plastic composition, which was rolled, dried, and fired at 1640°C by Honeywell's Ceramics Center, stood out as a strong favorite. This ceramic, as a substrate material, appeared to satisfy the important criterion of being defined a suitable material for the dip-coating process. Its cost-effective qualification also appeared to satisfy the long-range economic goals of JPL's Low-Cost Silicon Solar Array Project, and its thermal expansion coefficient (5×10^{-6} °C) was reasonably compatible with that of silicon. No obvious stress or strain was evident, in either the silicon coating or the substrate.

At this point in the program, the rolled, dried, and fired McDanel MV-20 mullite substrates were adopted for further SOC studies.

Mullite Substrate Development

Later mullite substrates of similar composition to MV-20 were obtained from Coors Porcelain Co. They were designated as a S1SI composition and were produced by a cold-pressing and sintering process.

The success of the coating experiments run with MV-20 mullite prompted an effort to see if the properties of the substrate could be optimized by compositional modifications. Based on discussions with M. Leipold of JPL and engineers at Coors Porcelain Co., substrates with experimental compositions based on variations of the 55 wt. % Al_2O_3 composition were identified and were produced by Coors.* The experimental compositions are listed in Table 3 and briefly discussed below.

The data for the McDanel ceramic were obtained from a company brochure. The Coors analysis was based on analyses of the starting materials. The only notable difference between the two is the higher titanium in the S1SI. The high-mullite and high-silicon modifications were produced to determine

*For additional information, refer to reports titled "Development of Mullite Substrates and Containers" and "Silicon Sheet Growth Development for the Large-Area Silicon Sheet Task of the Low-Cost Silicon Solar Array Project" by D. G. Wirth and J. D. Sibold, Coors Porcelain Company Golden, Colorado. Work Performed Under Contract No. NAS-7-100-954878

whether the mullite or the glass phase dominates the thermal behavior of the substrate during the coating operation. The boric acid modification was intended to be a body in which the glass phase is doped with B_2O_3 to produce a low-expansion glass and possibly act as a source of boron in the silicon coating. The open porosity modification is a body intentionally produced with higher porosity. The higher porosity will enhance the thermal shock resistance and will allow deeper penetration of the silicon coating into the substrate. The high-purity modification is a body produced from starting materials selected for their low-impurity content. As noted in Table 3, the iron, sodium, and titanium are noticeably low in this material. The electrically fused mullite is produced from a mixture of electrically fused mullite and silica powders. The impurity levels in this material are understandably low. The reducing-fire modification is a standard SISI mullite body that has been fired in a reducing atmosphere. The intent was to produce a material with high porosity that contained residual carbon in the form of unoxidized binder materials.

A better idea of the phase relationships existing in fireclay refractories can be obtained from alumina-silica equilibrium phase diagram of Aksay and Pask[2] shown in Fig. 35. Mullite is a compound that exists over a measurable range of compositions, and, according to Aksay and Pask, melts incongruently. Disagreements on the melting behavior of mullite still exist in the literature. Referring to Fig. 35, the equilibrium structure at room temperature of a composition containing about 55 wt. % Al_2O_3 consists of mullite crystallites in a eutectic matrix consisting of a finely divided mixture of SiO_2 and mullite. In reality, the liquid present at the firing temperature (approx. 1600°C) does not crystallize at the eutectic temperature and instead forms a continuous glass matrix around the mullite crystallites. It should be further mentioned that the clay starting materials do not contain any mullite but decompose during firing into a high-silica liquid into which the mullite crystallizes as firing proceeds.

Structure and Properties of Ceramic Substrates - The structures and properties of the substrates were measured at Honeywell and at Coors Porcelain Co. Microstructure, density, and modulus of rupture (MOR) determinations were made at Honeywell's Corporate Materials Science Center (CMSC), and density, firing, shrinkage, thermal expansion, and x-ray percent of mullite were determined at Coors. The Honeywell Ceramics Center provided firing

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[2] A. Pask, Science 183, 69 (1974).

Table 3. Composition of mullite-based ceramic substrates (in wt.%).

Code	Material	Al_2O_3	SiO_2	Fe_2O_3	CaO	MgO	K_2O	Na_2O	TiO_2	B_2O_2	MnO	CaO	V_2O_5	Comments
Commercial Compositions														
I	McDanel MV-20	55.4	42.0	0.8	0.1	0.04	0.7	0.5	0.5					Nominal McDanel
		52.6	43.7	0.45	0.09	0.14	0.74	0.74	0.82					Coors analysis
		-	-	1.27	0.15	0.33	-	0.38	1.30		0.07	0.01	0.07	Emission spectroanalysis
A	Coors SISI	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors analysis
II	McDanel MV-30	60.0	38.0	0.5	0.1	0.2	0.5	0.08	0.5					Nominal McDanel
		58.3	38.9	0.82	0.19	0.19	0.48	0.10	0.83					Coors analysis
		-	-	0.79	0.04	0.33	-	0.13	0.90		0.012	0.01	0.03	Emission spectroanalysis
Experimental Compositions from Coors Porcelain Co.														
B	High-mullite	67.2	31.4	0.45	0.02	0.01	0.16	0.18	0.54					Coors analysis
C	High-silica	52.2	44.7	0.56	0.13	0.22	0.83	0.22	1.01					Coors analysis
D	Boric acid	56.7	38.3	0.61	0.13	0.24	0.90	0.24	1.10	1.50				Coors analysis
E	Open-porosity	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors analysis
F	High-purity	59.5	39.1	0.44	0.21	0.13	0.34	0 05	0.30					Coors analysis
G	Electrically-fused	77.5	21.9	0.12	0.00	0.00	0.00	0.35	0.05					Coors analysis
H	Reducing-fire	57.6	38.9	0.62	0.13	0.25	0.92	0.25	1.12					Coors analysis

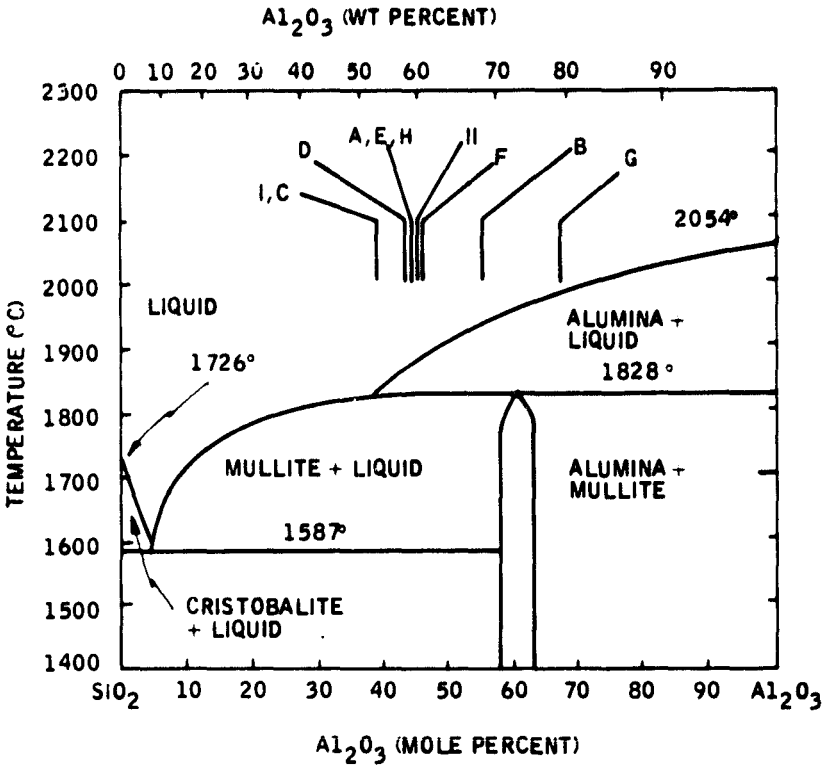


Figure 35. Alumina-silica phase diagram. Also shown are the compositions of the various substrate materials currently being examined (the code letters are explained in Table 3).

shrinkage data on the MV-20 and MV-30 substrates. The properties measured to date are summarized in Table 4. The thermal expansion of these materials is in accordance with the good thermal shock resistance of fireclay refractories. As shown in Fig. 36, the thermal expansion of the mullites is slightly greater than silicon. Thus, after cooling to room temperature, the silicon coating should be under a compressive status. Preliminary x-ray measurements (discussed later) of residual stress in the silicon have indicated this to be the case.

The strengths of the MV-20 and boric acid modifications were the lowest of the group. The strongest samples were those containing greater amounts of mullite (i.e., SISI and the high-mullite modification and the material fired in a reducing atmosphere). Both the strength and thermal expansion

Table 4. Properties of mullite-based ceramic substrates.

Code	Material	Density (gm/cc)	% Porosity	Thickness Shrinkage %	Length Shrinkage (%)	X-Ray % Mullite	Equilibrium % Mullite	Thermal Expansion RT to 1000°C (%)	MOR (kpsi)
Commercial Compositions									
I	McDanel MV-20	2.50	-	14.0	10.2	-	74	0.495	15.3 ± 1.5
A	Coors S1S1	2.70	0.32	12.1	16.7	76.5	81	0.520	23.7 ± 1.4
II	McDanel MV-30	-	-	-	-	-	82	0.470	-
Experimental Compositions from Coors Porcelain Co.									
B	High-mullite	2.86	0.22	12.1	12.7	70.2	95	0.485	25.9 ± 1.2
C	High-silica	-	-	-	-	56.1	74	0.480	-
D	Boric acid	2.60	0.19	11.7	13.7	66.8	80	0.535	15.6 ± 0.7
E	Open-porosity	2.55	7.27	11.6	13.8	66.4	81	0.525	18.8 ± 1.8
F	High-purity	7.70	0.53	14.9	19.5	66.8	84	0.510	20.1 ± 1.0
G	Electrically-fused	2.6 to 2.8	-	10.4	11.3	84.2	87	0.530	18.6 ± 1.4
H	Reducing-fire	2.7 to 2.9	-	12.5	18.1	66.4	81	0.515	23.8 ± 1.6

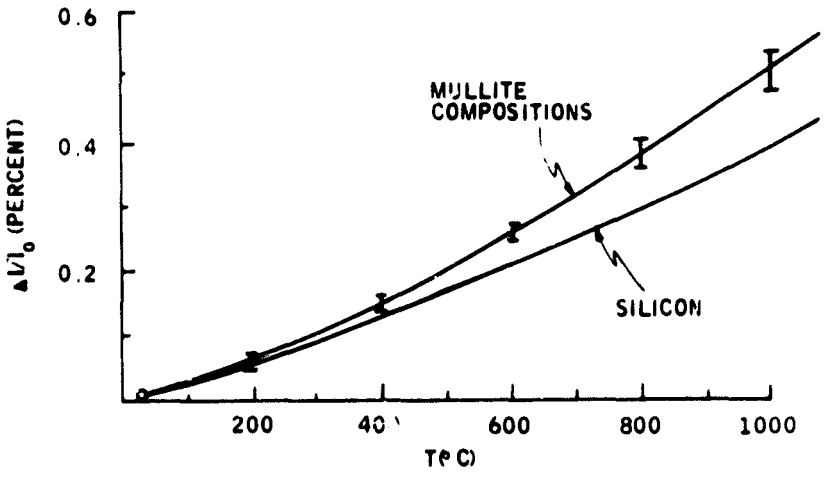


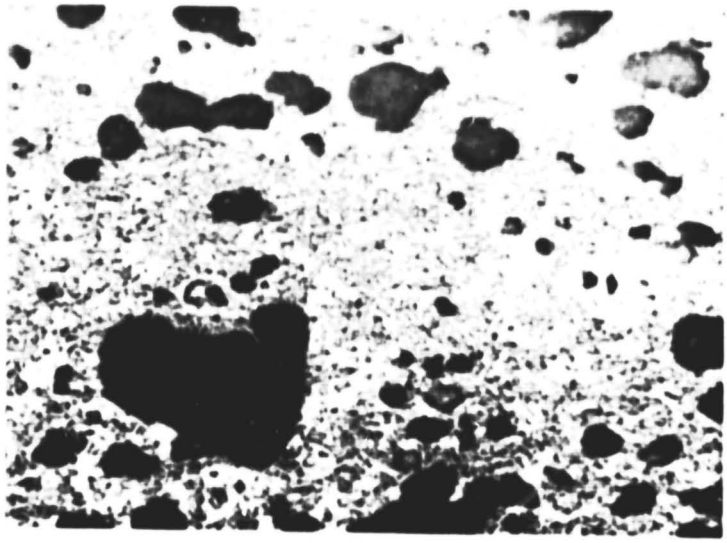
Figure 36. Thermal expansion of mullite compared with silicon.

affect the thermal shock resistance. Materials with low expansion and high strength, such as the high-mullite modifications, are expected to have good thermal shock resistance.

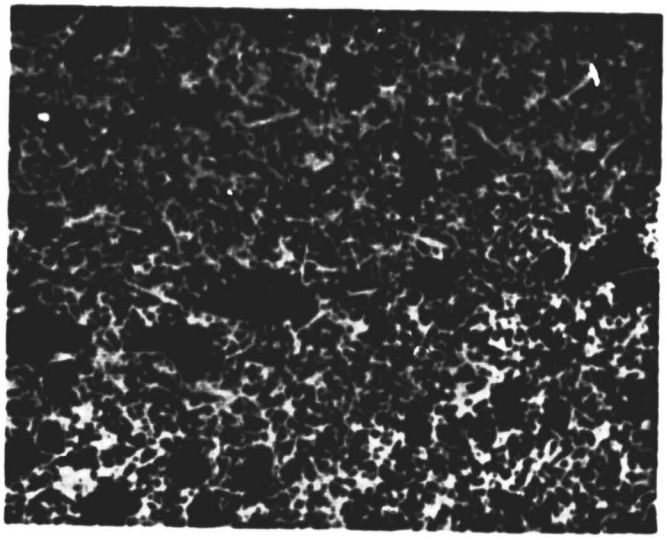
The average thermal expansion for mullite from room temperature to 1000°C is 0.526%.[3] This value is at the upper limit of those listed in Table 4 and, as discussed later, indicates that the thermal properties of the glass phase rather than the mullite are dominating the properties of the substrates.

The microstructures of McDanel MV-20 and Coors S1SI mullite refractories are shown in Fig. 37. The light regions are mullite crystallites and the dark phase is the glass matrix. The S1SI structure has more mullite and less porosity. This is consistent with the data in Table 4; the S1SI has a higher density and contains more Al_2O_3, which corresponds to a higher mullite content. The microstructures of most of the experimental compositions were similar to those shown in Fig. 38. The major differences were in the amounts of the phases (i.e., glass, mullite, and porosity). The microstructure of the electrically fused mullite body is shown in Fig. 38. The light areas are presumably mullite and the dark regions are silica.

[3]T. G. Godfrey, Jr., MS Thesis, Clemson College, Clemson, S.C.



(a) McDanel MV-20, specimen MR-114.



(b) Coors SiSi, Specimen MC-1.

Figure 37. Optical micrographs of mullite refractory specimens.

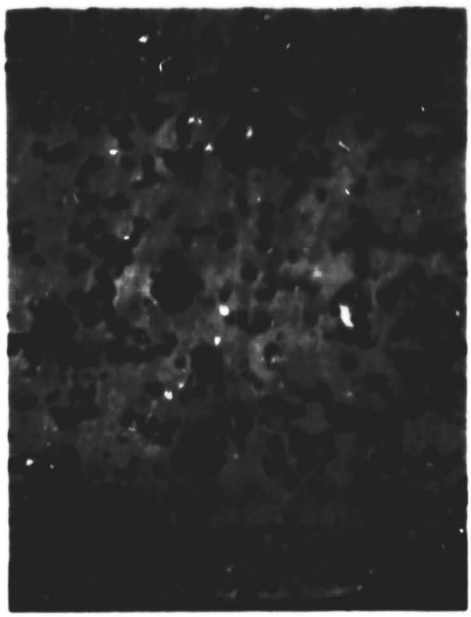
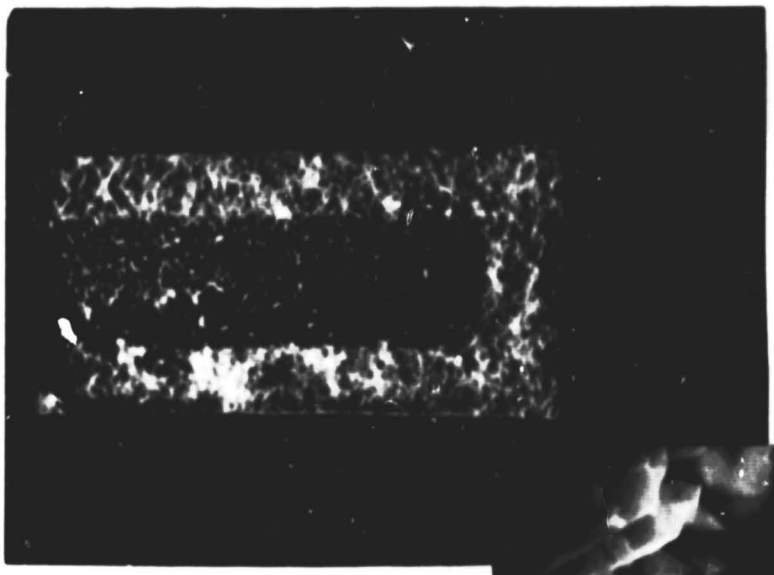


Figure 38. Optical micrograph of an electrically fused mullite substrate (500x).

Characterization of Acid-Leached Mullite Refractory - Most of the impurities in a mullite refractory are in the glass phase. In an effort to eliminate some of the impurities prior to coating, a number of pieces of McDanel MV-20 were leached in hydrofluoric acid to dissolve the glass phase. A scanning electron micrograph of a fractured cross section of an MV-20 substrate is shown in Fig. 39(a). This substrate was immersed in hydrofluoric acid until about half the total cross section had been acid-leached. A higher magnification photo of the interface region of the leached layer is shown in Fig. 39(b), while a still higher magnification photo is shown in Fig. 39(c). The acicular morphology of the mullite crystallites that precipated during firing is readily apparent. The structure appears to contain only the continuous-glass phase and the mullite needles. The results of EDAX analyses of regions in the center and at the edge of the leached sample showed that, as expected, the aluminum/silicon ratio increased and the potassium and titanium were lower in the leached region. The iron content was hardly altered by leaching.

Although the leaching operation lowered the surface impurity content, it also weakened the substrate. Leached substrates that were carbon-coated and dipped in silicon repeatedly fractured during dipping.



(a) Sample at 20x.

(b) Region at base of leached zone (2100x).

(c) Region near linear base of leached zone (5300x).

Figure 39. Scanning electron micrographs of a fractured surface of an MV-20 sample that had been immersed in HF to leach the glass phase to a depth of approximately one-third the specimen thickness.

The residual stress in the silicon layer can be estimated from an expression used for stresses in glaze coatings applied to ceramics.[4] For a thin silicon coating on an infinite substrate, the stress at temperature, T, is

$$\sigma_{Si} = E\left(T_o - T\right)\left(\alpha_{Si} - \alpha_{ceramic}\right)\left(1 - 3j + 6j^2\right) \qquad (2)$$

where E is Young's modulus and is assumed to be equal in the substrate and the coating, T_o is the temperature at which the substrate and coating are at a stress-free state, $(\alpha_{Si} - \alpha_{ceramic})$ is the difference in linear thermal expansion coefficients of the coating and substrate, and j is the ratio of coating to substrate thickness.

For the coatings applied in this work, the last term in the equation is negligible. Silicon is assumed to deform above 600°C (i.e., T_o = 600°C) and E is approximately 15 x 10^6 psi. The room temperature stresses in the coatings estimated from the above range from about 4500 to 7500 psi, depending on the substrate material. A compressive stress in the coating is, of course, beneficial, since it raises the fracture stress of the coating.

Some x-ray measurements have been made which have detected the residual stress in the silicon layer. In these measurements the Bond technique[5] of precision lattice parameter measurement was used to detect any stress-induced change in lattice spacing. Since the technique can be used only on stressed single crystals or samples with large grain sizes, only large-grained samples were examined. The x-ray measurements showed the (110) lattice spacing in the silicon layer to be less than the <110> spacing in a stress-free single crystal by 65 ppm. This confirms the sign of the residual stress. The <110> direction in the grain examined lay 20 degrees off the normal to the specimen surface. As a result, the strain (and stress) distribution parallel to the specimen surface could not be calculated because the orientation of the crystal axes of the silicon grain with respect to the specimen surface are not known. A very rough estimate of the residual stress in the coating corresponding to a strain of 65 ppm can be made as follows. If we assume that the strain normal to the surface is 65 ppm, then

$$\sigma = E\varepsilon = \frac{15 \times 10^6 \times 65 \times 10^{-6}}{0.3} = 3250 \text{ psi} \qquad (3)$$

where Poisson's ratio, ν, is assumed to be 0.3. This stress is on the order of that arrived at earlier on the basis of the thermal expansion mismatch.

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[4] W. D. Kingery, H. K. Bower and D. R. Wilman, Introduction to Ceramics, 2nd Ed., Wiley, New York (1976) 1, p. 609.

[5] W. L. Bond, Acta Cryst. 13, 814 (1960).

Figure 40 shows the thermal expansion of the experimental substrate compositions from Coors plotted as a function of mullite content as determined by x-ray analysis. Also plotted on the figure are the expansions of pure mullite and vitreous silica. Each data point is identified by the code letters defined in Table 4. The results can be discussed in terms of the glass content and impurity content in each material. The addition of impurities to vitreous silica increases the thermal expansion. The total impurity content as determined from Table 3 increases steadily through the series of samples with similar glass contents as follows: B, F, H, E, D.

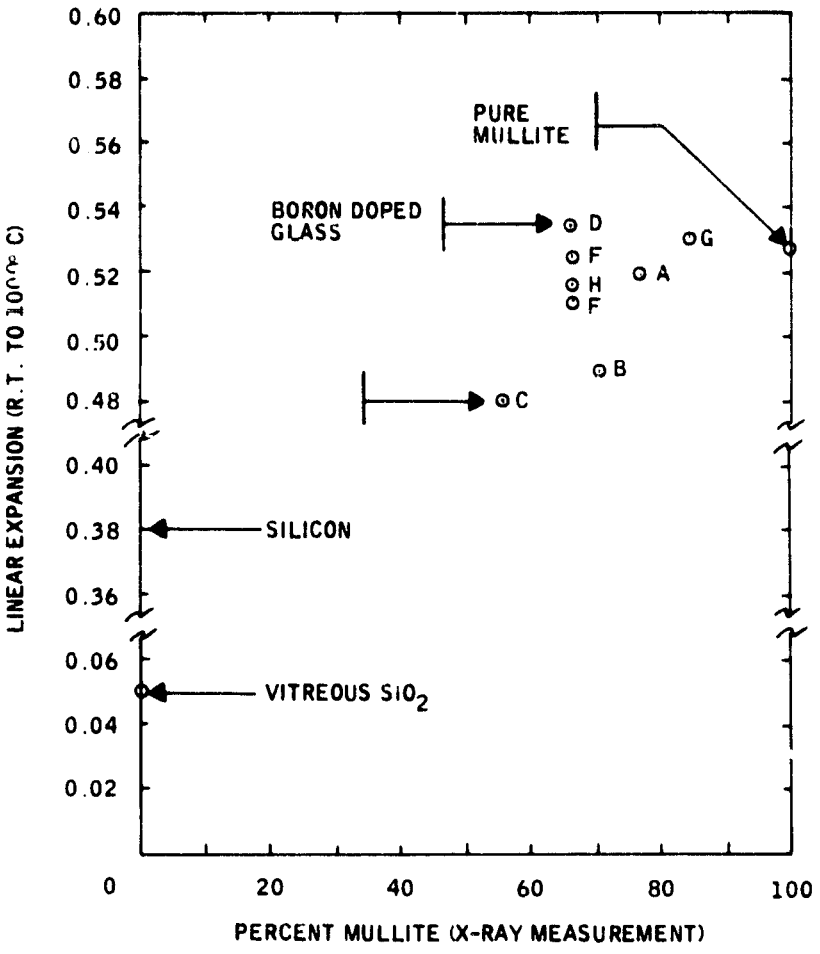


Figure 40. Thermal expansion from 25°C to 1000°C of experimental substrate materials.

The boric acid modification material (sample D) has the highest purity content of all and the largest expansion. Sample A has the same impurity content as samples E and H but contains more mullite. Sample C has a higher impurity content than B but contains more glass. The conclusion here is that the thermal expansion of a mullite-bas refractory is determined not only by the relative amounts of glass and m e in the material but also by the impurity content which primarily resides in the glass and alters its expansion. Impurities such as transition metals may be deleterious to the ultimate performance of the photovoltaic coating. Thus, if substrates are to be designed to be more thermally compatible with silicon, the most likely approach will be to alter the glass content rather than the glass chemistry.

The boric acid additions were to produce a low-expansion glass to lower the thermal expansion coefficient to a value closer to that of silicon. This was not found to be the case. This problem was resolved with other composition modifications discussed later. The porous body was produced to improve the thermal shock resistance and to allow more penetration of silicon into the ceramic. The results were marginal. The material fired in a reducing atmosphere contained a high porosity and a carbonaceous residue from unoxidized binder. Both were to enhance silicon penetration into the ceramic. Again the results were marginal.

Modifications B through F and H survived the dip-coating operation but too few were dipped to make a valid comparison of the effects of the compositional modifications. In fact, only one solar cell was fabricated on one of these substrates. The efficiency was only 3.41%. The G-Mod material was the only substrate not to survive the dip-coating operation. This is attributed to the higher total mullite content in the body. The thermal expansions of these materials are discussed in more detail later.

Semiquantitative analyses of the impurity contents of a number of these materials have been run and are given in Table 5.

Notable differences include the lower impurity content in the F-Mod material and the higher titanium and copper and lower iron in S1SI compared with MV-20. As noted above, there have not been enough solar cells made on the B through H modifications to evaluate the impurity effects. The mechanical properties and thermal shock resistance of S1SI and of the Coors substrate materials A through H which were extensively characterized are discussed in the paragraphs that follow.

Table 5. Semiquantitative emission spectrochemical analysis of mullite substrates (in wt. %).

Sample	Ti	Cu	Mg	Fe	Ca	V	Ni	Cr	Mn
MV20	0.78	<0.01	0.20	0.89	0.11	0.031	---	---	0.041
S1SI	1.1	0.071	0.29	0.68	0.070	0.051	<0.03	0.030	<0.03
Open-porosity modification	1.45	0.038	0.29	0.57	0.062	0.036	<0.03	0.026	<0.03
Reducing-fire modification	1.0	0.27	0.27	0.52	0.062	0.042	<0.03	0.28	<0.03
High-purity modification	0.27	0.047	0.14	0.45	0.080	<0.03	<0.03	N.D.	<0.03

The fracture strength and thermal shock resistance of these materials are listed in Table 6. The fracture strengths were measured in four-point bending at room temperature on bars with a nominal cross section of 0.1 x 0.1 inch over a span of 1 inch. The fracture strengths of the Coors C-Mod and McDanel MV-20 material were about the same. As previously determined, the Al_2O_3/SiO_2 ratios and presumably, the glass contents, are also similar. With the exception of the open-porosity and electrically-fused mullite substrates, the fracture strengths of the rest of the Coors materials were about 20 kpsi.

The critical quench temperature refers to a thermal shock resistance measurement attributed to Hasselman.[6] In the technique the room temperature fracture strength (usually in bending) of samples quenched from elevated temperatures is measured as a function of the quench temperature. When the quenching stresses are sufficient to propagate localized surface flaws in the ceramic, the room temperature strength decreases abruptly. The quench temperature causing the decrease in strength is an indication of how much thermal shock the material can withstand. Higher critical quench temperatures imply greater thermal shock resistance. The data listed in Table 6 were obtained on bars with a nominal cross section of 0.08 x 0.08 inch tested in four-point bending over a span of 0.75 inch. Tests were run

[6] D. P. H. Hasselman, J. Am. Ceramic Soc. 52, 600 (1969).

Table 6. Room-temperature fracture strength and critical quench temperature for mullite refractory substrates.

Code	Material	Strength (Kpsi)	Critical Quench Temperature (°C)
7-50	MV20	15.0 ± 2.7	340
7-300	MV20	13.8 ± 2.3	340
A	SISI	21.7 ± 1.4	*
B	High-mullite	21.0 ± 1.6	300
C	High-glass	13.8 ± 0.8	360
D	Glass-property modification	21.1 ± 1.4	325
E	Open-porosity	16.6 ± 1.8	325
F	High-purity	19.4 ± 0.9	325
G	Electrically-fused	16.2 ± 6.5	315
H	Reducing-fire	22.3 ± 1.5	315

*Not measured to date.

on SISI samples but the bars were larger in cross section. Since there is a size effect in thermal shock testing, these data need to be repeated on smaller specimens. The critical quenching temperature increases for smaller cross sections. Representative data showing the fracture strength as a function of quench temperature for MV-20 mullite are shown in Fig. 41. With the exception of the MV-20 and C-Mod material, the critical quenching temperature is around 325°C. It is slightly less for materials with higher mullite contents (B and G-Mod) and for the material fired in a reducing atmosphere. It is slightly higher for materials containing more glass, presumably as a result of their slightly lower thermal expansion. The thermal expansion data will be reported later in this section.

Fracture toughness measurements have been made on MV-20 and on the Coors material A through H, excluding the C-Mod material. Briefly, the fracture toughness is an indication of the resistance of a material to fast, catastrophic crack propagation and is usually denoted by the critical stress intensity factor, K_{IC}. K_{IC} is a measure of the stress at a crack tip during fast fracture in terms of the crack tip and loading geometry, the crack size, and the remote applied stress according to $K_{IC} = Y \sigma_F a$, where Y is a geometrical constant, σ_F is the fracture stress, and a is the crack length.

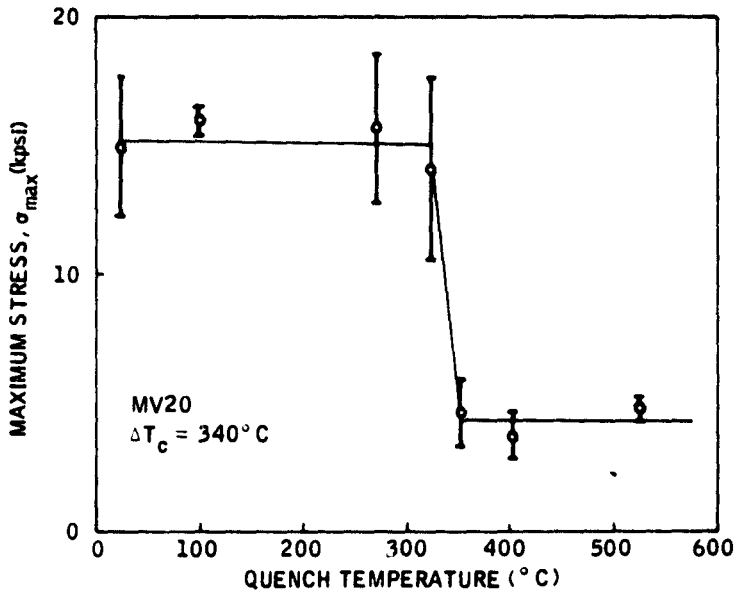


Figure 41. Room-temperature fracture strength of MV-20 mullite.

K_{IC} is a material property and is determined by measuring the load required to fracture precracked specimens with known loading and crack geometries.

In this work, the constant-moment modification of the double-cantilever beam technique, devised by Freiman et al.,[7] is being used to measure K_{IC}. An advantage of this technique is that the stress intensity factor is independent of crack length. Thus, the fracture toughness measurement can be made by simply loading a precracked specimen to failure. Crack length measurements are not necessary. A schematic of the specimen and loading geometry is shown in Fig. 42. A side groove is cut into the specimen, as shown in Fig. 42, to guide the crack.

K_{IC} is calculated from

$$K_{IC} = \frac{P_c L}{(It)^{1/2}} \qquad (4)$$

[7] S. W. Freiman, D. R. Mulville and P. W. Mast, J. Mater. Sci. 8, 1527 (1973).

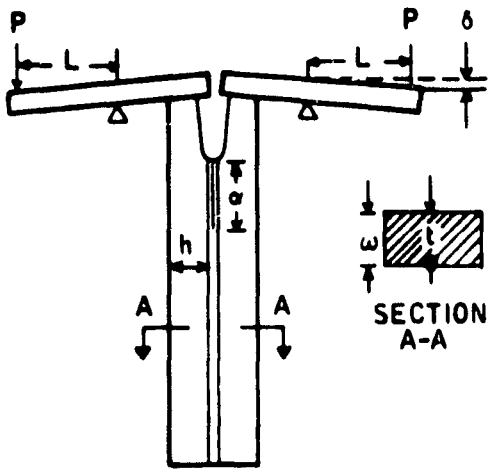


Figure 42. Schematic showing specimen and loading arrangement used in the constant-moment test. δ is the deflection of the point of load application during the test.

where I is the moment of inertia of one-half of the specimen, L is the moment arm, and t is the thickness at the base of the crack-guiding notch shown in the cross-section diagram in Fig. 42. Neglecting the effect of the reduced cross section at the crack, $I = wh^3/12$. Note that the general form of both these expressions is $K_{IC} = AP_c$, where A is a geometrical term and P_c is the applied load at fracture. In this test, K_I is independent of the crack length, a, and the measurements are correspondingly simplified, as noted above.

Fracture toughness data taken to date are summarized in Table 7.

Table 7. Fracture toughness measurements on mullite substrate materials.

Code	Material	K_{IC} ($MNm^{-3/2}$)
MV20	MV20	1.98 ± 0.23
A	SISI	2.39 ± 0.34
B	High-mullite	2.22 ± 0.06
D	Class property modification	2.37 ± 0.29
E	Open-porosity	2.16 ± 0.25
F	High-purity	2.23 ± 0.25
G	Electrically-fused	2.10 ± 0.31
H	Reducing-fire	2.30 ± 0.34

The fracture toughness of the mullite refractories listed in Table 7 are about the same. The lowest of the Coors materials is the electrically-fused mullite fired with fused silica. To put the numbers in Table 7 in perspective, values of the fracture toughness of ceramics range from 0.75 $MNm^{-3/2}$ for soda lime glass to greater than 6 $MNm^{-3/2}$ for hot-pressed silicon nitride. Fine-grained aluminum oxide has a fracture toughness of about 5 $MNm^{-3/2}$. The fracture toughness of metals is typically an order of magnitude higher.

An estimate of the flaw size initiating fracture in these materials may be obtained from $K_{IC} = \sigma_F Y A^{1/2}$, where σ_F is the fracture strength and Y is a constant depending on the flaw and loading geometry. For penny-shaped surface flaws, Y = 1.26.[8]

Flaw sizes calculated from K_{IC} and σ_F measurements on SISI and MV-20 materials are 160 and 230μm, respectively. These are relatively large flaws and may indicate most failures in these ceramics originate from pores or pore clusters.

Before the thermal expansion data are presented, some recent work on new mullite compositions should be pointed out. One of the goals of the work on the first series of Coors substrates (i.e., B through H-Mod) was to see if the thermal expansion of mullite-based refractories could be altered by compositional control. This was the reason that boric acid was added to SISI to form the D-Mod substrates. The resulting borosilicate glass was expected to lower the thermal-expansion coefficient of the material. As previously noted, this was not the case and the expansion of the D-Mod substrates was actually slightly higher than that of SISI. We realized that substrates with thermal expansions closer to that of silicon would probably have to be developed when slotted substrates were used because the stress concentrations in the substrates due to the slots might initiate fractures in the substrates and coatings. This we later found to be true.

Since fused silica has a lower thermal expansion than silicon and mullite has a higher thermal expansion, in principal, the thermal expansion of the two-phase refractory should be a function of the relative amounts of each phase. These are controlled by the Al_2O_3/SiO_2 ratio according to the phase diagrams shown in Fig. 35. With this in mind, J. Sibold and D. Wirth at Coors started formulating another experimental series of mullite composi-

[8] G. R. Irwin and P. C. Paris, pp. 1-46 in Fracture, Vol. III, H. Liebowitz ed., Academic Press, New York (1971)

tions by adding excess silica to the SiSI composition. This had already been done in the first series of compositions (i.e., the B and C-Mod materials), but in the "high-silica" modification, only enough silica was added to SiSI to bring the Al_2O_3/SiO_2 ratio down to that of MV-20. In the next series, even more SiO_2 was added. The compositions of the second series of Coors experimental substrates are given in Table 8.

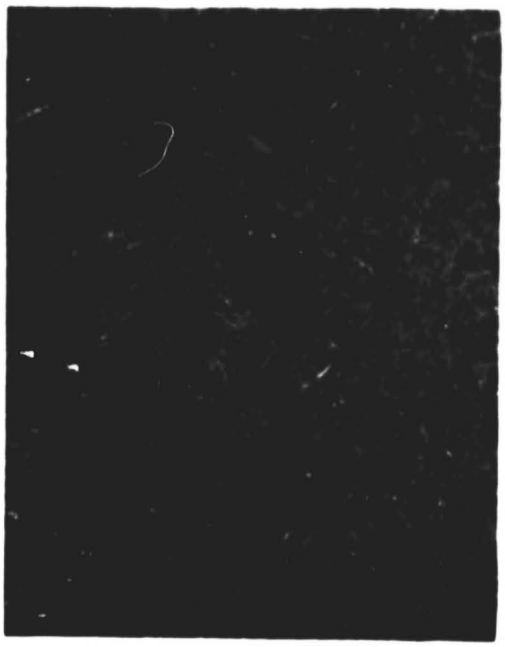
Table 8. Composition of the second series of Coors experimental substrates.

Code	Material	Composition wt. % Al_2O_3	Al_2O_3/SiO_2 Ratio
A	SiSI	57.6	1.48
C	"High-silica mod" SiSI + 10 wt. % excess SiO_2	52.2	1.17
I	SiSI + 18 wt. % excess SiO_2	48.8	1.01
J	SiSI + 25 wt. % excess SiO_2	45.8	0.89
K	SiSI + 38 wt. % excess SiO_2	41.4	0.74

We see in what follows that the material with the highest silica content (i.e., K-Mod) has properties that make it much more applicable as a substrate for SOC than any others tested to date.

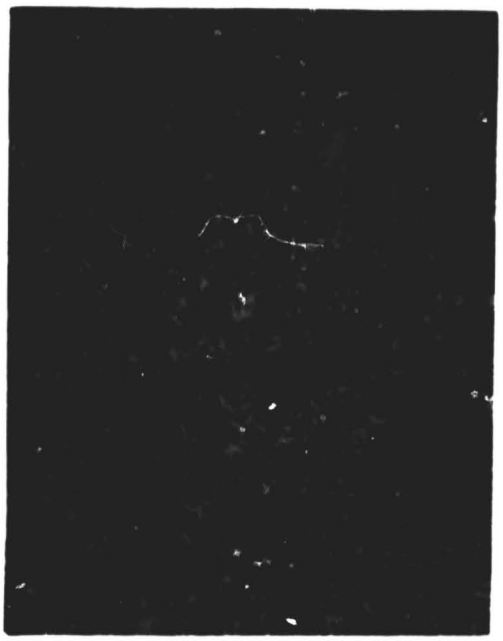
The microstructures of the A, I, and K-Mod materials are shown in Fig. 43. The darker phase is the continuous glass phase. The amount of glass phase is seen to increase as the Al_2O_3/SiO_2 ratio decreases. The pore size also appears to increase with increasing silica additions. Measurements have not been made of the densities at this time. The mechanical properties and thermal shock resistance of these materials have also not been determined. Thermal expansion data have been provided by Coors and are discussed below.

The thermal expansions of the substrate materials produced by adding excess silica to the SiSI composition are shown in Fig. 44. The data are plotted as the linear thermal expansion from room temperature to 700°C as a function of the Al_2O_3/SiO_2 ratio. The residual stresses between the silicon layer and the substrate are presumed to be negligible above 700°C. The



(a) S1SI.

(b) S1SI + 18 wt. % excess SiO_2.



(c) S1SI + 38 wt. % excess SiO_2.

Figure 43. Photomicrographs of various mullite bodies (magnification 150x).

data corresponding to SISI, I and K modifications are indicated as such on the figure. The thermal expansion of silicon is also included in the figure. Note that as the silica content increases, the thermal expansion decreases in the manner expected and that the thermal expansion of a mullite refractory with an Al_2O_3/SiO_2 of approximately 0.45 should be equal to that of silicon.

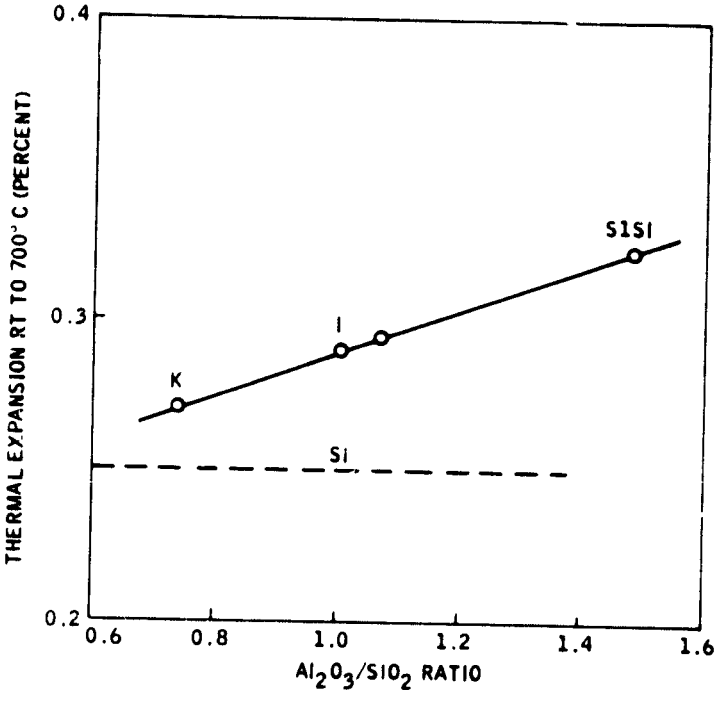


Figure 44. Thermal expansion of SISI mullite containing excess silica.

A silicon-coated substrate with this composition should not show any residual stresses between the coating and the substrate. The residual stresses in the silicon coating can be estimated by

$$\sigma = E\Delta T \left(\alpha_{Si} - \alpha_{ceramic}\right) \qquad (5)$$

where Young's modulus, E, is assumed to be equal in the substrate and the coating, ΔT is the temperature difference when the composite cools below its stress-free state, and α_{Si} and $\alpha_{ceramic}$ are the linear thermal-expansion coefficients of silicon and the substrate, respectively. If we assume E is

15×10^6 psi, α_{Si} (RT - 700°C) = $3.7 \times 10^{-6} °C^{-1}$, and a stress-free state at 700°C (i.e., $\Delta T \sim 675°C$), the residual stresses in the silicon layers on S1SI and the K-Mod substrates are:

Material	α (RT - 700°C) ($°C^{-1}$)	σ (psi)
S1SI	4.7×10^{-6}	10,000
K-Mod	4.0×10^{-6}	3,040

Note that with even a small thermal mismatch, significant thermal stresses can develop. These stresses can cause the slow growth of flaws. When subcritical flaws reach critical size under a constant applied stress, large-scale fracture may occur.

The K-Mod substrates proved to be very comfortable with the SOC process in every respect and innumerable satisfactory SOC layers, large and small, were achieved using them. Minor modifications to the K-Mod substrates were later made and designated as N and O mods. While no in-house characterization of these latest modifications was performed, they too proved to be completely satisfactory for SOC purposes.

Slotted and Large-Area Substrate Development - The ceramic substrates used in SOC solar cells will necessarily have to be produced by a continuous process in order to meet the economic goals of the program. To this end, J. Sibold and D. Wirth at Coors have been adapting their roll compaction process to the manufacture of mullite substrates for the SOC process. This effort was quite successful. Large, 10cm x 100cm S1SI substrates were produced from roll-compacted tape. These substrates were 1.0mm thick and are some of the largest single substrates produced by a tape process.

Roll-compacted tape has also been used to produce slotted substrates for back-contacted SOC solar cells. In this process, slotted substrates with dimensions shown in Fig. 45 and 46 were produced by punching the slot patterns in green, unfired tape with plastic die sets. The properties of silicon coatings put down on slotted substrates are discussed elsewhere in this report.

A final comment is made pertaining to the mechanical integrity of slotted

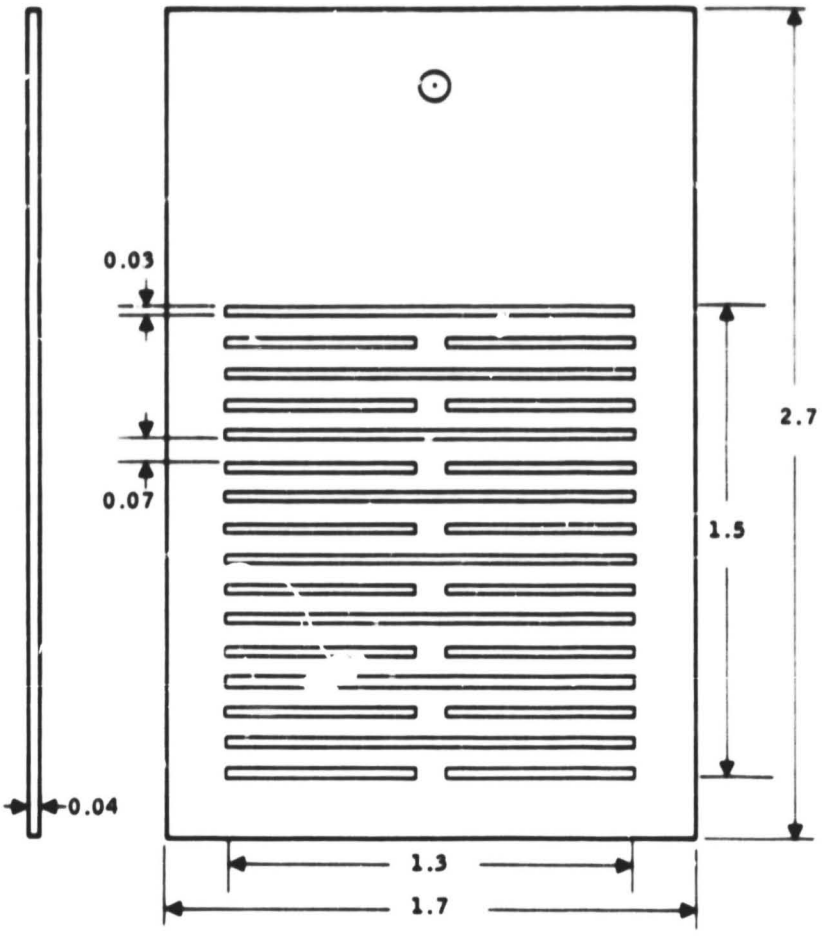


Figure 45. Dimensions of slotted substrates produced at Coors. Taken from September 15, 1978, Monthly Peport from Coors. All dimensions are in inches.

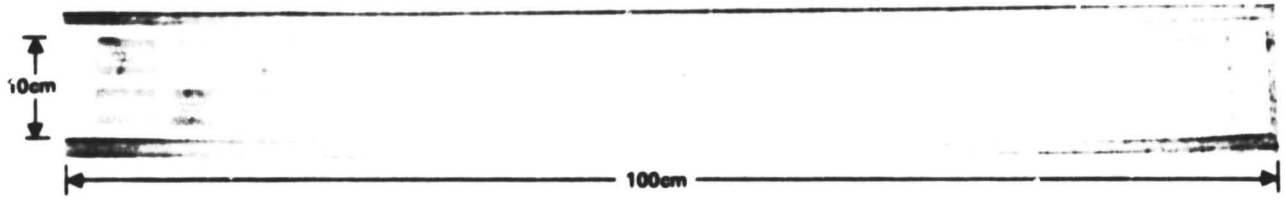


Figure 46. 10cm x 100cm slotted substrate produced at Coors.

substrates. It was noted that slotted substrates have more of a tendency to crack after coating with silicon and during subsequent processing than unslotted substrates. This was expected and results from the tendency for subcritical crack growth to occur in ceramics and from the stress concentrations associated with a slot. Since the thermal expansion of the substrate is greater than silicon, the substrate is in tension at room temperature. The stress concentration at the end of a slot can raise the local stress to values larger than those listed above. The fracture stress of a ceramic depends on the fractive toughness and the flaw size. If flaws in the substrate can slowly grow under a constant residual stress, they may grow to a size where they become critical and initiate fast fracture. This is the origin of delayed failure in glasses and other ceramic materials and has been observed by us in silicon-coated mullite. This problem has been minimized by using the K-Mod and C-Mod substrate materials, but is still occasionally observed.

SUBSTRATE CARBON COATING EFFORT

As discussed in the Introductory section of the report, the carbon or graphite coatings play a key role making SOC possible.

Initially, the substrate carbonization was performed by simply hand-scrubbing high-purity graphite onto the substrate. It was originally believed that this graphite coating, in addition to making the substrate wettable to molten silicon, could perhaps serve as a back contact to silicon coating which otherwise was electrically insulated by the ceramic substrate. It was also not known to what extent, if any, the type or nature of carbon coating would ultimately affect the crystalline structure of the subsequent silicon layer.

The scrub-on-coatings proved to do an excellent job in producing good adhering, smooth, large-grain layers, but they did not appear to be cost-effective in a scale-up process. For this reason, early in the program, the following alternate carbon coating methods were investigated:

- Applying carbon soot to one surface of the substrate, using an acetylene torch.
- Applying black Aqua-Dag to one surface of the substrate and subsequently firing it at 900^{o}C in an argon atmosphere.

- Applying a liquid coating of pure acrylic which had been dissolved in 1-2 Dichloroethane ($C_2H_4Cl_2$) to one surface of the substrate followed by a 900°C firing in an argon atmosphere.

- Pyrolyzing a layer of transparent 3M-brand Scotch tape in a 900°C furnace having a nitrogen atmosphere.

Of these methods, only the rubbed-carbon technique produced uniform coatings of silicon. Except for the Aqua-Dag which flaked off the substrate following the 900°C firing, the remaining methods produced only spotty wetting of the silicon.

Later in the program, five different liquid-carbon-coating compounds were purchased from Dylon Industries. These coatings had the viscosity of latex paint and were water-soluble. A total of 22 substrates were silicon coated that were first coated with the various Dylon compounds. It was found necessary to oven dry these coatings, as residual moisture caused them to blister or "boil" off when dipped in the molten silicon, as shown in Fig. 47. It was also noted that the granular nature of most of these coatings promoted nucleation which decreased the grain size, and that carbides formed throughout the silicon layer. However, in cases where the granular surface was smoothed by wiping off the excess graphite and the coating was oven-dried, the Dylon coatings gave large grain size similar to the hand-rubbed graphite coatings. Unfortunately, our chemical analysis of these coatings has revealed that they contain from 1 to 2% impurities and were unsuited for our application.

Another somewhat novel method of carbon coating was also investigated - plasma decomposition of propane gas in an RF sputtering apparatus. The carbon is deposited uniformly and its purity reflects that of the gas. The morphology and grain size of the silicon film formed on such substrates is comparable to those on hand-rubbed graphite coatings.

Several methods of incorporating the carbonization with the ceramic processing were also examined. These were rolling graphite or silicon carbide particles into one surface of the substrate and then firing in an inert atmosphere or just firing the ceramic in an inert atmosphere so that the residue from the organic binders would form a carbon film. None of these approaches proved satisfactory for silicon coating. The plain ceramic fired in an inert atmosphere shattered in the temperature gradient above the

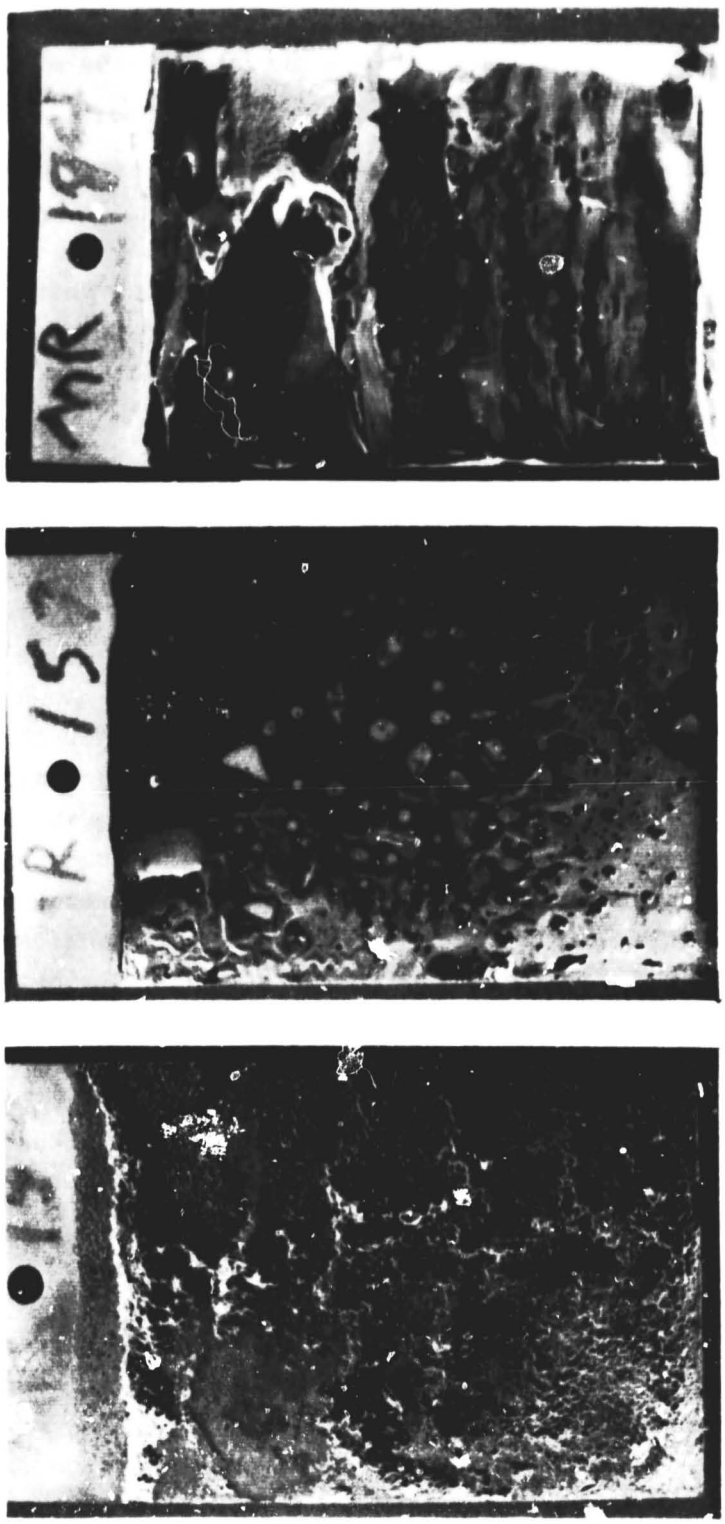


Figure 47. Blistered and spotty silicon film formation as the result of incomplete drying of Dylon carbon coatings (1.7x).

melt before it could be dipped. The substrate with silicon carbide developed large blisters and it appeared that the silicon did not wet the surface. The substrate with the graphite particles appeared to have been wet by the silicon, but either there was not sufficient carbon or the particles did not stay embedded to permit the growth of a silicon layer.

Some very promising experiments were conducted using colloidal carbon suspensions obtained from Acheson Colloids Co., Port Huron, Michigan. Four different mixtures were tested: Dag 154; Electrodag 154; Electrodag 155; and Electrodag 502. The 154 mixtures are graphite in isopropyl alcohol with a cellulosic binder. Electrodag 155 is a mixture of graphite in trichlorethylene with a cellulosic binder. Electrodag 502 is a graphite and carbon-black mixture in methyl ethyl ketone (2-butanone) with a fluroelastomer binder. Drying posed no problems and coating thickness was relatively easy to control.

Spectrographic analysis shows that the dags should be suitable for solar cell application. The results of the analysis are shown in Table 9.

Table 9. Spectrographic analysis results of colloidal carbon suspensions from Acheson Colloid Co. Values are in ppm.

Element	Dag 154*	Dag 154	E'dag 502	E'dag 154	E'dag 155
AR	88	ND < 10	110	20	33
Mo	100	ND < 33	34	ND < 33	ND < 33
Sn	52	ND < 10	ND < 10	ND < 10	ND < 10
Ca	180	43	68	39	56
V	33	ND < 33	ND < 33	ND < 33	ND < 33
Ti	24	8	53	7	8
Ni	15	2	2	2	2
Si	220	35	72	73	51
Pb	35	ND < 33	ND < 33	ND < 33	ND < 33
Mg	4	2	14	2	3
B	3	ND < 1	37	ND < 1	3
Mn	4	2	3	2	3
Na	200	ND < 100	270	ND < 100	ND < 100
Fe	1500	260	370	285	290

*Older stock.

The growth morphology of the silicon was not adversely affected by the dags. Metallographic examination of cross sections of SOC which were carbonized with Dag 154 showed excellent wetting of and bonding to the ceramic surface by the silicon, as shown in Fig. 48.

Figure 48. Silicon-ceramic interface carbonized with dag 154 (500x).

Vitreous carbon coatings were applied to several mullite substrates by the Tylan Corporation, Torrance, California. Their process is proprietary, but they report the thickness of the coating to be approximately 7μm. While our primary purpose for these coatings was to prevent substrate dissolution, upon dip-coating with silicon, a secondary interest was related to the possibility that these coatings may provide a conductive silicon-ceramic interface. With this purpose in mind for all of the carbon coatings, the electrical resistivity of several carbon coatings was measured.

There are several important aspects of the electrical resistivity of carbon layers. First, the electrical resistance can be used to evaluate the uniformity and reproducibility of the carbon-coating process. Secondly, the sheet resistance of the carbon may affect the resistivity measurement of the silicon. Thirdly, it would be desirable to use the carbon as a back contact

to the silicon to decrease parasitic series resistance of solar cells. Table 10 summarizes our measurements on sheet resistance of carbon layers.

It is clear from Table 10 that with the rubbed and the dag-borosilicate coatings, graphite is almost entirely removed by the melt. The dag only layer is partially removed, but has the appearance of being continuous and intact after removal of the SOC by etching or spalling.

Table 10. Typical carbon sheet resistivities.

Carbon Type	As Deposited (ohms/square)	After CP-4 Etching to Remove SOC Layer (ohms/square)
Graphite rubbed on rolled mullite (MV-20)[a]	10 to 25	250 to 600
Graphite rubbed on pressed mullite (American Lava)	100 to 150	1K to 60K
Vitreous carbon (Vitregraf) on MV-20	2.5 to 5.0	2.5 to 5.0
Dag (colloidal carbon in alcohol) on MV-20	20K to 40K (unfired)	120 to 600
	20 to 40 (fired)	70 to 450 (where SOC spalled off)
Dag and borosilicate glass (1:1)	-	5K to 1M

[a]The thickness of the layer based on weight gain is 7μm, which would give a sheet resistivity of about 2.5 ohms/square.

The vitreous carbon layers, on the other hand, even after 1 hour of contact with the melt, are almost wholly intact. Since the sheet resistivity of the vitreous carbon is only 2 to 5 ohms/square, it is much lower than the sheet resistivity of the p-type silicon layer (50 to 500 ohms/square) and could seriously affect the sheet resistivity measurement if there is low-

resistance contact between p-silicon and vitreous graphite. The nature of this contact was therefore investigated.

Samples were mounted in a metallurgical mount, and cut and polished to show the cross section. The microscope showed that there was an interface layer that was harder than either the carbon or the silicon - a strong suggestion of SiC formation.

The samples were then removed from the potting compound and the cross section was examined using scanning Auger microscopy at Physical Electronics, Inc. Some of the results are shown in Fig. 49. A complete Auger spectrum of the interfacial material showed only silicon and carbon, and no impurities (at the 0.1% level). It is interesting, however, that the shape of the carbon peak and the silicon-to-carbon stoichiometry varied from that of a polycrystalline silicon-carbide standard. It is not known whether these discrepancies are significant, but they suggest that the form of silicon carbide is different from the usual form.

At any rate, several comments on the silicon-carbide interface are in order. The SiC appeared thickest at the top of sample MR-78, which had been in the melt for an hour. Since it was much thicker than the carbon coating, the SiC must be formed from carbon particles which float to the top of the melt. There was no detectable SiC at the top of sample MR-106, which had been in the melt a minimum amount of time. Away from the surface, the SiC thickness appeared about the same in the two samples, varying from 2 to 10μm. Typically, the SiC was somewhat thinner than the vitreous carbon coating remaining.

The samples were etched in Sirtl etch after polishing, which revealed the presence of cracks. The region shown in Fig. 49 was selected because the SiC was of maximum thickness and because it showed some cracks in the silicon and at the silicon-SiC interface. These cracks may be responsible for the nonuniformity of the electrical contact, or it may be due to variations in SiC thickness.

A goal was to improve the conductance (increase the thickness) of the carbon layer used to wet the ceramic and to obtain ohmic contact between the carbon and the p-type silicon so that the carbon contributes significantly to decreasing the series resistance of the solar cells. Two addi-

Figure 49. Scanning Auger micrographs of the silicon-vitreous graphite interface at 2500x. Photo at left is a secondary electron image; the center photo is the carbon image; at right is the silicon image of a section of sample MR-106. Silicon is at the top, carbon is at the bottom, and the silicon carbide is in between.

tional goals were: (1) to investigate the use of doped carbons as diffusion sources for doping of the back surface of silicon to provide a BSF effect, and (2) to investigate the use of the glassy carbon (GC) as a protective barrier against unwanted impurity diffusions from the substrate into the silicon layer.

An important part of this effort was to have control of the carbon layer. For this reason, we attempted to develop a method of producing doped GC layers. We had previously demonstrated that "Vitregraph" GC coatings made by Tylan Corporation showed very little erosion by the molten silicon. This is important if the vitreous carbon is to be used as a protective barrier.

In Table 11, silicon-to-carbon contacting is indicated in the dipped GC-coated substrates by a lower ρ_s measurement of 8 to 40 ohms/square. In contrast, the hand-rubbed Ultra-Carbon control sample is 200 ohms/square. On some of the dipped samples, the silicon was etched off with CP4 etch and considerable erosion of the vitreous carbon layer was observed. There was evidence of the boron-doped carbon doping the melt. This is indicated by contrasting the ρ_s of the silicon layer on the doped-carbon samples and the ρ_s of the silicon on the hand-rubbed Ultra-Carbon sample dipped after the doped-carbon samples.

Table 11. Sheet resistivity of silicon coatings (first dip run).

Substrate	Silicon Layer ρ_s (Ω/□)
Hand-rubbed Ultra-Carbon control before	200
900° fired GC (4 samples)	8 to 40
900° fired boron-doped GC (dipped) near end of run	4.2, 4.4
Hand-rubbed Ultra-Carbon dipped after boron-doped samples	17

In a second dip run, eight GC-coated substrates with thinner carbon coatings (average ρ_s = 52 ohms/square were dipped. The silicon coated all of the substrates very well. Sheet resistivity measurements for the sequence are summarized in Table 12. All samples were dipped with the same pull-rate, resulting in similar silicon coating thicknesses.

Table 12. Sheet resistivity of silicon coatings (second dip run).

Substrate	Silicon Layer $\rho_{\square}$ ($\Omega/\square$)
Hand-rubbed Ultra-Carbon control before	120
Unheat-treated GC (3 samples)	avg. = 130
Boron-doped GC (5 samples)	avg 3.4
Hand-rubbed Ultra-Carbon control after GC samples	2.1

Comparison of the first two lines of Table 12 shows no evidence of electrical contact between the silicon and carbon. This is possibly due to the high erosion of the thinner carbon layer by silicon. The bottom two lines indicate boron doping of the melt by the GC for the same reasons as previously mentioned. Diodes were made from this dip run and results are listed in Table 13.

Table 13. Summary of SOC with glassy carbons.

Diode	No. of Diodes	Avg. Active Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor	Avg. Eff (%)	Max Eff (%)	Comments
120-1A-Q11	5	0.046	0.47	22.2	0.668	7.2	8.2	Hand-rubbed carbon control
120-3B-Q11A	6	0.070	0.50	21.6	0.679	7.25	8.4	GC
120-3B-Q11B	6	0.085	0.50	22.0	0.672	7.4	7.7	GC
120-3A-Q11	1	1.05	0.50	19.5	0.619	6.0	6.0	GC

The cell measurements show that the GC coatings can produce performance at least as good as that produced with hand-rubbed carbon.

It was expected that the erosion resistance and the impermeability of the GC layers would be increased by high-temperature firing. For this purpose, an induction furnace for high-temperature firing of vitreous carbon coatings was set up. Some problems arose with the first few samples which were fired. The first coating fired successfully, but succeeding coatings tended to flake off. This problem was later rectified by thinning the polymer and laying down a much thinner coat for the second and succeeding coatings.

In summary, GC layers have been demonstrated to act effectively as wetting agents and as diffusion sources for doping silicon layers. Firing at 900°C does not appear to give adequate erosion resistance and impermeability, although such films are adequate to produce good cell performance. High-temperature firing is needed to reduce the erosion effect of the molten silicon.

At this point in the work with glass-carbon coatings, the work was temporarily discontinued due to the loss of personnel who were performing the work.

With respect to the behavior of a carbon coating as a wetting agent, it appeared that any means of applying a smooth, uniform, dense coating of carbon of suitable thickness and purity will promote the coating of ceramic with silicon. Because of the ease of application of the dag mixtures, they were eventually adopted as a final method for applying the carbon coating.

SHEET SILICON GROWTH EFFORT

Introduction

Sheet silicon growth was obtained during the investigation by two very different coating techniques. These techniques were, as previously discussed, dip-coating and SCIM-coating methods. In this section of the report it will be shown, however, that each of these techniques produced a final product which was structurally very similar. In an effort to fully understand the growth mechanisms of these two growth processes, considerable analytical support was given to the experimental effort. Since day-to-day experimental progress can only be judged through analysis of results, considerable material characterization was also performed. This subsection of the report summarizes the various phases of analytical and experimental growth studies along with the numerous characterization studies required to pursue this investigation.

Thermal Analysis of Sheet Silicon Growth Processes

Introduction - The growth rate of sheet silicon appears to be limited by heat-extraction efficiency. Our economic analyses indicate that a throughput speed of about 14 cm/min is required to meet the price goals, and,

to date, our best solar cells have been grown at one-fourth this speed. We have dedicated a large amount of effort to increasing our understanding of the thermal mechanism of our growth process with the aim of attaining the necessary high throughput.

The present SOC growth appears to proceed from a liquid-solid interface which is roughly perpendicular to the pull direction (see Fig. 50). We have been using the word "symmetric" to refer to this type of growth.

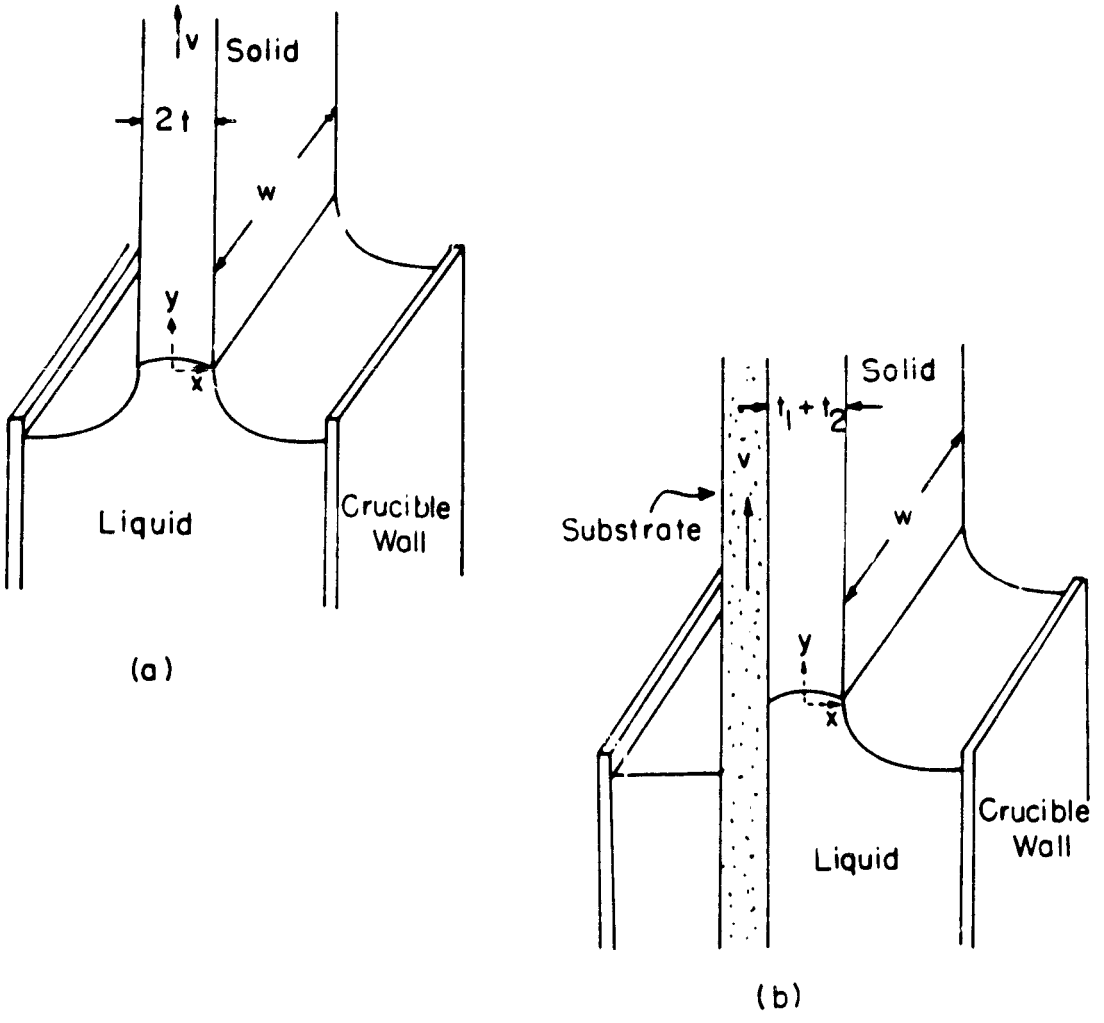


Figure 50. Vertical growth of sheet silicon. (a) Unsupported growth. (b) Supported growth. In the present discussion, the effect of a die to stabilize the unsupported growth is neglected.

Symmetric growth may be unsupported, as in the edge-defined, film-fed growth (EFG)[9-13] or the web-dendritic ribbon[14] processes, or supported on a substrate, as in the silicon-on-ceramic (SOC)[15,16] or ribbon-against-drop (RAD)[17] methods. In either case, the attainable growth rate is limited by heat extraction efficiency. The steady-state analysis of unsupported silicon growth is greatly simplified by the symmetry of the structure, leading to an uncomplicated solution to the heat equations.[16] Important by-products of the analysis are expressions for pull speed versus sheet thickness and for the shape of the crystallization or freezing front. This simplicity does not exist in the case of silicon grown on ceramic, and numerical methods must be chosen to solve the heat equations. The first part of this subsection is an analysis of supported symmetric growth, for the SOC case in particular. It is found from the symmetric growth studies that the economic throughput target of 12 to 18 cm/min will probably not be met in symmetric growth with only passive (radiative) cooling.

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[9] J. G. Swartz, T. Surek and B. Chalmers, "The EFG Process Applied to Growth of Silicon Ribbons," J. Electronic Material 4, pp. 255-279 (1975).

[10] A. E. Bell, "Thermal Analysis of Single-Crystal Silicon Ribbon Growth Processes," RCA Review 38, pp. 109-139 (1977).

[11] T. F. Ciszek, "Maximum Growth Rates for Melt-Grown-Ribbon-Shaped Crystals," J. Appl. Phys. 47, pp. 440-442 (1976).

[12] T. Surek and S. R. Coriell, "The Edge-Defined, Film-Fed Growth of Controlled-Shape Crystals," J. Crystal Growth 37, pp. 253-271 (1977).

[13] T. Surek, C. B. Hari Rao, J. C. Swartz and L. C. Garme, "Surface Morphology and End-Shape Stability in Silicon Ribbons Grown by the Edge-Defined, Film-Fed Process," J. Electrochem. Soc. 124, pp. 112-123 (1977).

[14] M. D. Harril, G. A. Rhodes, J. W. Faust and R. B. Hilborn, "Thermal Analysis of Solidification in Web-Dendrite Ribbon Growth," J. Crystal Growth 44, pp. 34-44 (1978).

[15] J. D. Zook, S. B. Schuldt, R. B. Maciolek and J. D. Heaps, "Growth Evaluation, and Modeling of Silicon-on-Ceramic Solar Cells," Proc. 13th IEEE Photovoltaic Spec. Conf., IEEE Press (1978), pp. 972-978.

[16] J. D. Zook and S. B. Schuldt, "Analysis of Conditions of High-Speed Growth of Silicon Sheet," J. Crystal Growth 50, pp. 51-61 (1980).

[17] E. Fabre S. Makrain-Ebeid and Y. Baudet, "Solar Cells on RAD Polycrystalline Silicon," 13th Photovoltaic Specialist's Conf., op. cit., pp. 1101-1105.

We have also begun a theoretical study of the so-called wedge-shaped or asymmetric growth as an alternative to the more conventional, symmetric growth. Asymmetric growth offers high throughput potential and possibly other advantages such as sweeping impurities out of the active solar-cell region. However, very little is known about this growth mode, particularly the thermal and mechanical design factors which must be incorporated in the growth apparatus to produce and maintain a stable wedge-shaped growth region. These factors are analyzed in the second part of this subsection. Only unsupported asymmetric growth has been considered here. The extension to substrate supported growth is left for a future investigation.

Part I: Supported Symmetric Growth - The thermal analysis of supported symmetric growth does not assume any particular orientation in the gravitational field but a vertical orientation is elected for purposes of illustration (Fig. 51). The important considerations are the rate of release of the latent heat of fusion and the thermal properties of the SOC beginning at the location of the liquid-solid interface and extending downstream. These consist of the heat loss mechanism, assumed to be primarily radiative, at the front silicon and back ceramic surfaces, and conductive as well as convective heat transport through the silicon and ceramic materials. Except for possible gaseous convection, which is not considered here, these properties are independent of orientation in the gravitational field. The analysis applies to both dip-coated and SCIM-coated material, except for the details of the mensicus shape which do not affect the main result of the analysis - the growth velocity versus silicon thickness tradeoff. The dip-coating geometry was selected to represent the upstream boundary conditions in our thermal model of the process. The essential features of dip-coated SOC are shown in Fig. 51. Ceramic substrates are pulled vertically from the silicon melt at constant speed, v. The freezing front appears at a height y_F above the melt. The value of y_F at zero pulling speed may be calculated from hydrostatic considerations.[18] Moreover, this appears to remain unchanged in actual steady-state growth for pulling speeds well into the millimeter-per-second range.[19] Above y_F, the temperatures in the structure begin to fall toward some effective radiation temperature, T_o, of the environment.

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[18] J. C. Brice, The Growth of Crystals from Liquids, North-Holland Press (1973), pp. 160-170.

[19] J. D. Zook, B. G. Koepke, B. L. Grung and M. H. Leipold, "Supported Growth of Sheet Silicon from the Melt," J. Crystal Growth 50, pp. 260-277 (1980).

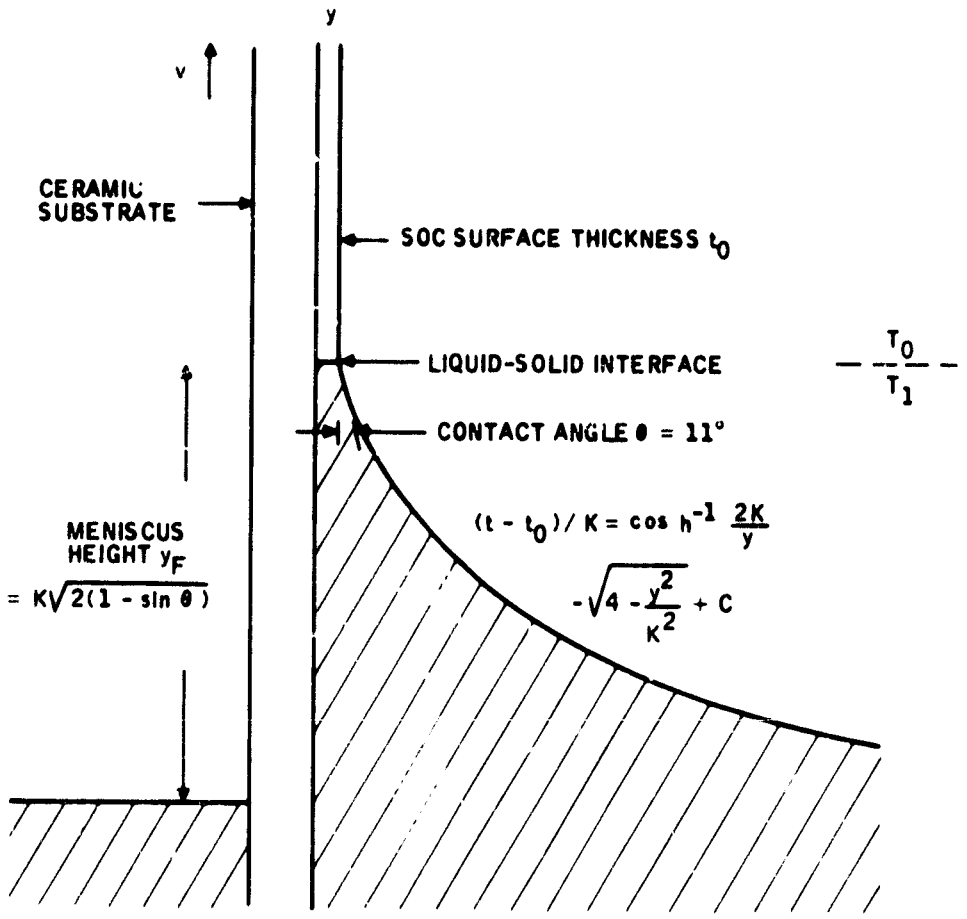

Figure 51. Cross-sectional view of SOC growth. The meniscus shape is based on hydrostatic equilibrium. Radiative background temperatures T_0 and T_1 are seen above and below the liquid-solid interface.

A possibly different radiation temperature, T_1, is seen by the portion of the structure below the freezing front. In the present study, only radiative heat removal was considered and the temperatures T_1 and T_0 were assumed uniform over $0 < y < y_F$ and $y_F < y < \infty$, respectively. The simple two-part background is used to give a crude approximation to the effect of a heat shield located at y_F. More general heat loss functions are easily incorporated and may be investigated later. As was true in the unsupported case, the rate of heat extraction by radiation must balance the rate of removal of sensible heat from the melt (by convection) plus the rate of release of latent heat at the freezing front. In the present case, most of the sensible

heat is carried in the ceramic owing to the greater thermal mass.

Heat Equations -- Two zones are identified because of the different thermal properties of molten and solid silicon. In the zone $y_F \leq y \leq \infty$, the steady-state heat equations in the ceramic portion follow from two-dimensional heat balance, including convective terms:[20]

$$\frac{\partial}{\partial x}\left(k_c \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_c \frac{\partial T}{\partial y}\right) - \rho_c C_c v \frac{\partial T}{\partial y} = 0 \quad 0 \leq x \leq t_c \tag{6}$$

$$k_c \frac{\partial}{\partial x} T(0,y) = \varepsilon_c \sigma \left\{\left[T(0,y)\right]^4 - T_o\right\}^4 \tag{7}$$

$$T(x,\infty) = T_o \tag{8}$$

The two-dimensional model is appropriate because the width of the structure (z-dimension) is assumed large compared with the thickness, $t_c + t_o$. Physical parameters are identified in Table 14. For the silicon portion, a one-dimensional temperature profile, $U_o(y)$, is used, equivalent to assuming the isotherms are horizontal. This assumption can be checked by estimating the inclination of the isotherms in the solid silicon portion. The steady-state equations in the solid silicon ($y \geq y_F$) are

$$t_o \left\{\frac{d}{dy}\left(k_o \frac{dU_o}{dy}\right) - \rho_o C_o v \frac{dU_o}{dy}\right\} = f_o(y) \tag{9}$$

$$f_o(y) = \varepsilon_o \sigma \left\{\left[U_o(y)\right]^4 - T_o^4\right\} - k_c \frac{\partial}{\partial x} T(t_c,y) \tag{10}$$

$$U_o(y) = T(t_c,y) \tag{11}$$

$$U_o(y_F) = T_F \tag{12}$$

The extraction term, $f_o(y)$, includes both radiation at the external surface and conduction across the internal surface into the ceramic.

In the zone $0 \leq y \leq y_F$, the equations for the ceramic portion are similar to Equations (6) and (7), except for the radiation temperature, T_1, in place of T_o (Fig. 50) and a new boundary condition at y = 0 instead of

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[20] H. S. Carslaw and J. C. Jaeger, Conduction of Heat in Solids, 2nd Ed., Oxford Univ. Press (1959).

C-2

Table 14. Nomenclature and numerical data.

Symbol	Description	Value/Units
C_c	Specific heat of ceramic	1.04 (J/g °K)
$C_o = C_1$	Specific heat of silicon	0.954 (J/g °K)
$J_o(y)$	Silicon heat flux density ($y > y_F$)	(W/cm^2)
$J_1(y)$	Silicon heat flux density ($y < y_F$)	(W/cm^2)
k_c	Heat conductivity of ceramic	0.041 (W/cm °K)
k_o	Heat conductivity of solid silicon	$343/U_o$ (W/cm °K)
k_1	Heat conductivity of liquid silicon	0.6 (W/cm °K)
L	Latent heat of fusion of silicon	1802 (J/g)
T(x, y)	Ceramic temperature	(°K)
T_o	Downstream ($y > y_F$) ambient temperature	(°K)
T_1	Upstream ($y < y_F$) ambient temperature	(°K)
T_M	Melt temperature	(°K)
T_F	Silicon freezing temperature	1685 (°K)
t_c	Ceramic thickness	(cm)
t_o	Solid-silicon layer thickness	(cm)
$t_1(y)$	Liquid-silicon layer thickness	(cm)
$U_o(y)$	Silicon temperature ($y \geq y_F$)	(°K)
$U_1(y)$	Silicon temperature ($y \leq y_F$)	(°K)
v	Pull speed	(cm/sec)
y_F	Total meniscus height above melt	0.5 or 0.69 (cm)
δ	Numerical grid spacing	0.02 (cm)
ρ_c	Ceramic density	2.25 (g/cm^3)
$\rho_o = \rho_1$	Silicon density	2.33 (g/cm^3)

$y = y_F$, as given by Eq. (15):

$$\frac{\partial}{\partial x}\left(k_c \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_c \frac{\partial T}{\partial y}\right) - \rho_c C_c v \frac{\partial T}{\partial y} = 0 \tag{13}$$

$$k_c \frac{\partial}{\partial x} T(0,y) = \varepsilon_c \sigma \left\{\left[T(0,y)\right]^4 - T_1^4\right\} \tag{14}$$

$$T(x,0) = T_M \tag{15}$$

In the liquid-silicon portion, the variable thickness t_1 must be taken into account. The following is derived based on the assumption of horizontal isotherms see next subsection for derivation of Eq. (16) :

$$\frac{d}{dy}\left(t_1 k_1 \frac{dU_1}{dy}\right) - \rho_o v t_o C_1 \frac{dU_1}{dy} = f_1(y) \tag{16}$$

$$f_1(y) = \left\{1 + \left(\frac{dt_1}{dy}\right)^2\right\}^{1/2} \varepsilon_1 \sigma \left\{\left[U_1(y)\right]^4 - T_1^4\right\} - k_c \frac{\partial}{\partial x} T(t_c, y) \tag{17}$$

$$U_1(y) = T(t_c, y) \tag{18}$$

$$U_1(y_F) = T_F \tag{19}$$

A final condition expresses the fact that the freezing front is the source of a heat flux density (vertical component) equal to $\rho_o vL$:

$$-k_1 \frac{d}{dy} U_1 (y_F) + \rho_o vL = -k_o \frac{d}{dy} U_o (y_F) \tag{20}$$

Derivation of Eq. (16) -- Refer to Fig. 52. We assume horizontal isotherms so that temperature can be denoted by $U_1(y)$. Vertical mass flow, independent of y, is equal to $\rho_o v t_o$. If $t_1(y)$ denotes local thickness, vertical heat flux, H(y), per unit width is

$$H(y) = \rho_o v t_o C_1 U_1 - t_1 k_1 dU_1/dy \tag{21}$$

Denoting by $f_1(y)$ the heat flux density lost by radiation at the curved surface and by conduction to the ceramic, we then have

$$dH/dy + f_1 = 0$$

or

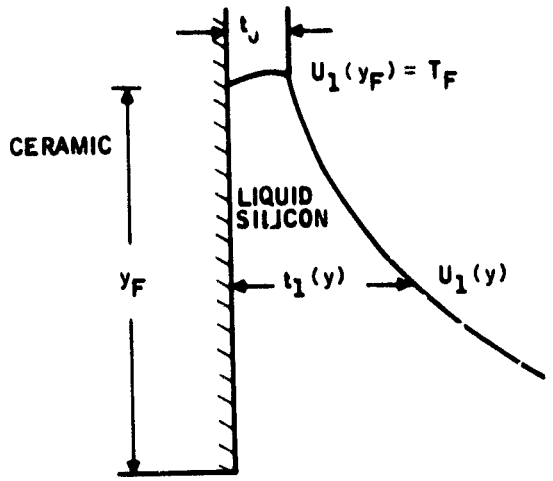

Figure 52. Diagram of meniscus region.

$$\frac{d}{dy}\left(t_1 k_1 \frac{dU_1}{dy}\right) - \rho_o v t_o C_1 \frac{dU_1}{dy} = f_1(y) \tag{22}$$

For $t_1(y)$, we use the result from Harrill, et al.:[14]

$$(t_1 - t_o)/K = \cosh^{-1}(2K/y) - \cosh^{-1}(2K/y_F) + \left[4 - (y_F/K)^2\right]^{1/2} - \left[4 - (y/K)^2\right]^{1/2} \tag{23}$$

where $K/y_F = [2(1 - \sin\theta)]^{-1/2} = 0.79$ if the contact angle, θ, is 11^o.

Finite-Difference Model -- A finite two-dimensional array of nodes was selected (Fig. 53) as the framework to approximate the solution of the above equations by finite differences. The ceramic thickness, t_c, is represented by seven nodes, which are equally spaced except for the edge pairs, where one-half the standard spacing is used. Hence, the standard spacing, δ, is equal to $t_c/5$. The standard spacing is also used vertically, except for the end pairs. An integer, m_F, labels the approximate location, y_F, of the freezing front, separating the liquid and solid silicon phases. If m = 0 denotes the bottom row of nodes, the correspondence between m and y is:

$$y = (m - 1/2)\,\delta,\ m = 1,2,\ \ldots \qquad (24)$$

and m_F is the largest integer contained in $1 + y_F/\delta$.

The right-hand column of nodes is sufficient to represent the entire silicon thickness due to our assumed horizontal isotherms. There are no discontinuities in the two-dimensional temperature profile; hence, the silicon temperatures are equal to the ceramic temperatures at the silicon-ceramic interface.

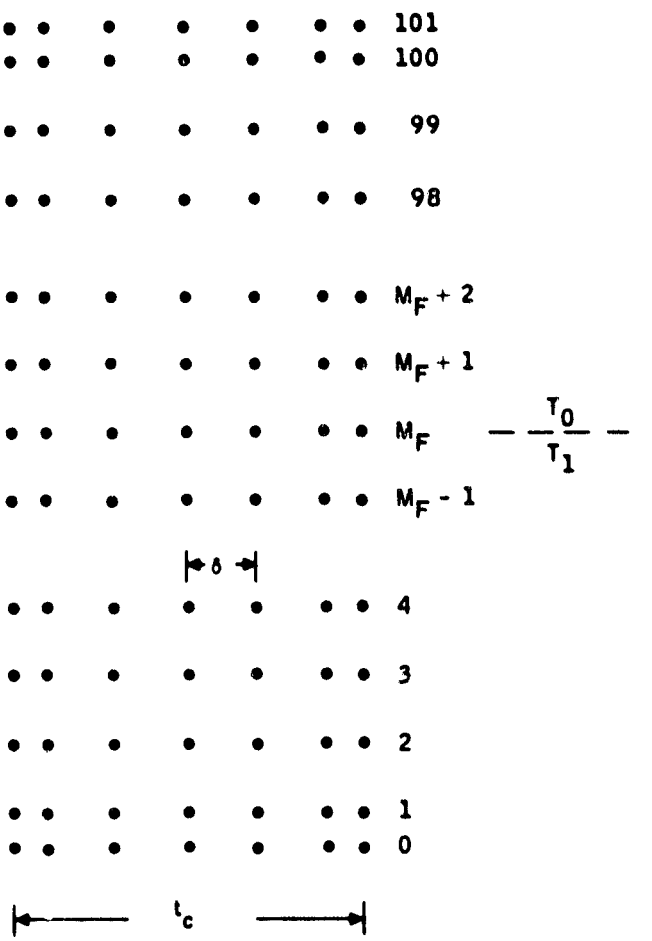

Figure 53. Finite-difference array for calculating SOC temperature profile. Right-hand column of nodes corresponds to silicon layer (one-dimensional approximation) and right-hand edge of substrate. The rest of the nodes represent locations within and at the left-hand edge of the substrate.

The details of the solution technique, a modified over-relaxation method (Gauss-Seidel),[21] are omitted here. The equations are nonlinear due to the Stefan-Boltzmann relations and the temperature-dependent k_o. For the latter, an approximate inverse temperature dependence, $k_o = 343/U_o$, is inferred from recommended data over the range 800K < U_o < 1685K. These nonlinearities are handled by means of coefficient updates at each Gauss-Seidel iteration.

The steady-state temperature profile depends on the thicknesses of ceramic and silicon, the pull speed, the melt temperature, and the background temperatures, T_o and T_1. Of course, T_F is fixed at 1685K. Not all of the foregoing can be independently specified, since the problem would be overdetermined and a solution would, in general, be non-existent. As a mathematical convenience, we have chosen the melt temperature to be a dependent variable, and this is therefore an output of the calculation along with the temperature profile. Also, we specify the temperature differences $T_M - T_o$ and $T_M - T_1$ rather than T_o and T_1 directly (e.g., $T_M - T_1 = 1385K$ will result in T_o being a little above room temperature because T_M will generally be a few degrees above 1685K.

Interpretation -- At the present time, the complete temperature profiles in ceramic and silicon are of only casual interest. Isotherms obtained by interpolation of output data of two computer runs are shown in Fig. 54. The sparse, sharply-bent isotherms below the freezing front, and the sudden increase in isotherm density above the point of latent heat release, are features found in all the runs.

On the other hand, the silicon part of the profile is crucial and gives the nucleus of information for our interpretation of thickness versus growth speed. As in the case of unsupported silicon sheet growth,[16] a major assumption here is that stable growth of SOC requires the liquid meniscus to be at or above the freezing temperature; that is, heat flow in the liquid must not be away from the freezing front. A condition for the limiting stable growth rate is that the temperature gradient on the liquid side of the interface approach zero. According to Brice,[18] maximum silicon thickness at a given velocity may be obtained by adjusting the melt temperature to a point just above the value where the interface becomes unstable and dendritic growth develops. In a computer calculation, this would correspond to zero temperature gradient in the liquid at $y = y_F$.

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[21] L. Fox, Numerical Solution of Ordinary and Partial Differential Equations, Pergammon Press (1962), p. 289.

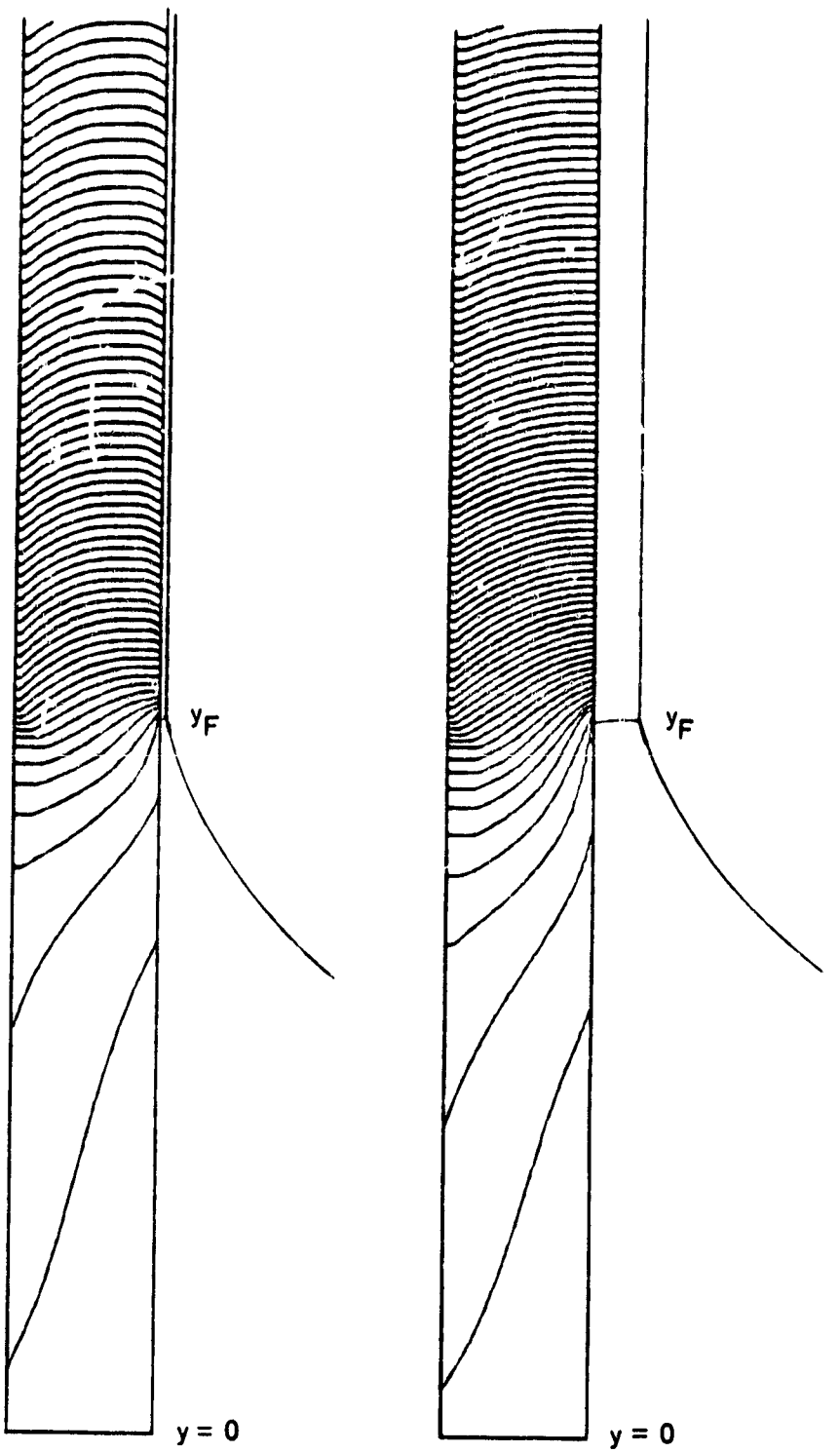


Figure 54. Isotherms for $T = T_M$. $T = T_M - 5n$, $n = 1, 2, \ldots$, by two-dimensional interpolation; $t_c = 0.1$cm, $y_F = 0.5$cm $T_M - T_o = 1385$K, $T_M - T_1 = 300$K. Left: $t_o = 0.003$cm, $v = 0.153$ cm/sec. Right: $t_o = 0.03$cm, $v = 0.0685$ cm/sec.

Fig. 55 shows calculated normalized heat flux, $Jt/\rho vLT_o$ as a function of y, for three melt temperatures at the same pull speed, where

$$J = J_1 = -k_1 \frac{dU}{dy} \text{ (liquid)} \tag{25}$$

$$J = J_o = -k_o \frac{dU}{dy} \text{ (solid)} \tag{26}$$

In Fig. 55, the middle case (II) gives maximum stable t_o because $J_1(y_F) = 0$. Case I, with a higher melt temperature and lower t_o, is within the stability limit, but Case III (lower melt temperature) is unstable.

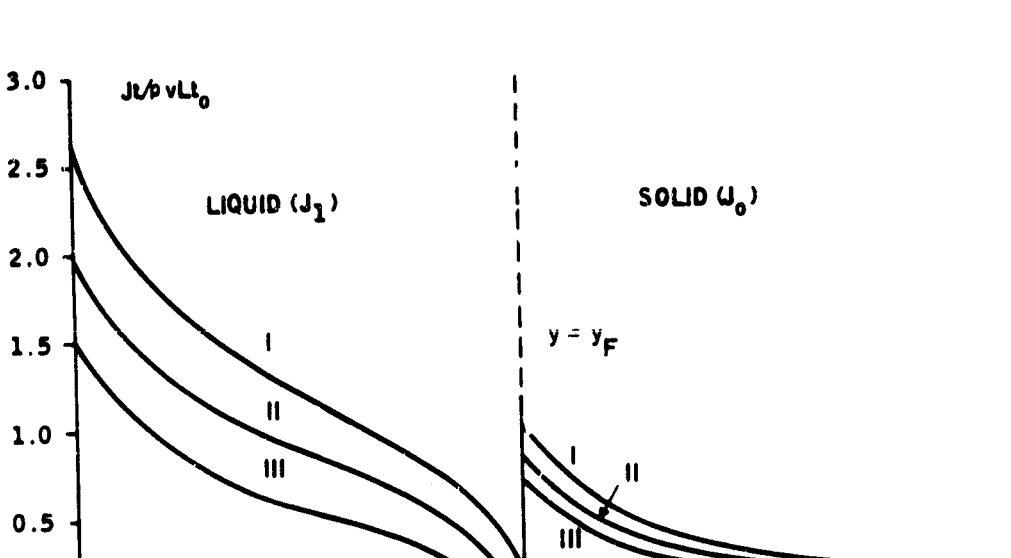


Figure 55. Normalized thermal flux in liquid and solid parts of the silicon layer at height y above melt surface. v = 0.098 cm/sec for all three cases. The degree of stability is determined by the melt temperature. Case I (stable): $T_M - T_F = 22.3^o$; $t_o = 0.0067$cm; $J_1\ (y_F) > 0$. Case II (stable): $T_M - T_F = 15.1^o$; $t_o = 0.0100$cm, $J_1\ (y_F) = 0$. Case III (unstable): $T_M - T_F = 6.5^o$; $t_o = 0.0143$cm; $J_1\ (y_F) < 0$.

Figure 56 gives further computed data assuming the same fixed v. $J_1(y_F)$ is seen to be a monotonic increasing function of T_M, and t_o is a monotonic decreasing function of T_M. According to this figure, silicon thicknesses up

to 0.01cm can be stably grown at v = 0.098 cm/sec on 0.1cm ceramic, assuming that heat is removed by radiation to an environment at room temperature.

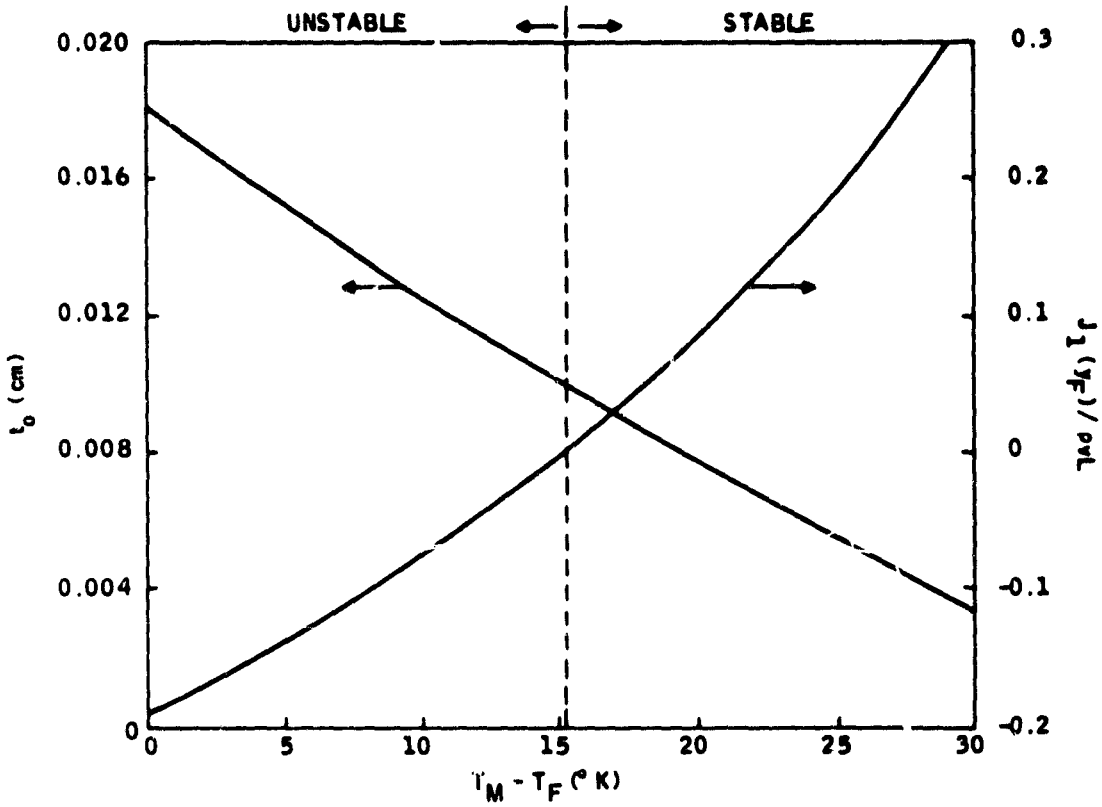


Figure 56. Normalized J_1 (y_F) and silicon thickness as functions of melt temperature. Pull speed fixed at 0.098 cm/sec; t_c = 0.1cm; $T_M - T_o$ = 1385K; $T_M - T_1$ = 50K; y_F = 0.5cm.

Figure 57 shows t_o and $J_1(y_F)/\rho_o vL$ as functions of pull speed when melt temperature is held constant. We note that t_o always decreases as v increases, but $J_1(y_F)/\rho_o vL$ reaches a minimum and then increases with v. In general, the model indicates that growth is more stable at both extremes of pull speed (fixed T_M) and tends to become less stable or unstable at intermediate pull speeds. If a lower T_M were used in these calculations, there would be a larger range of pull speeds corresponding to unstable growth, and stable growth would be possible at both higher and lower pull speeds outside of this range.

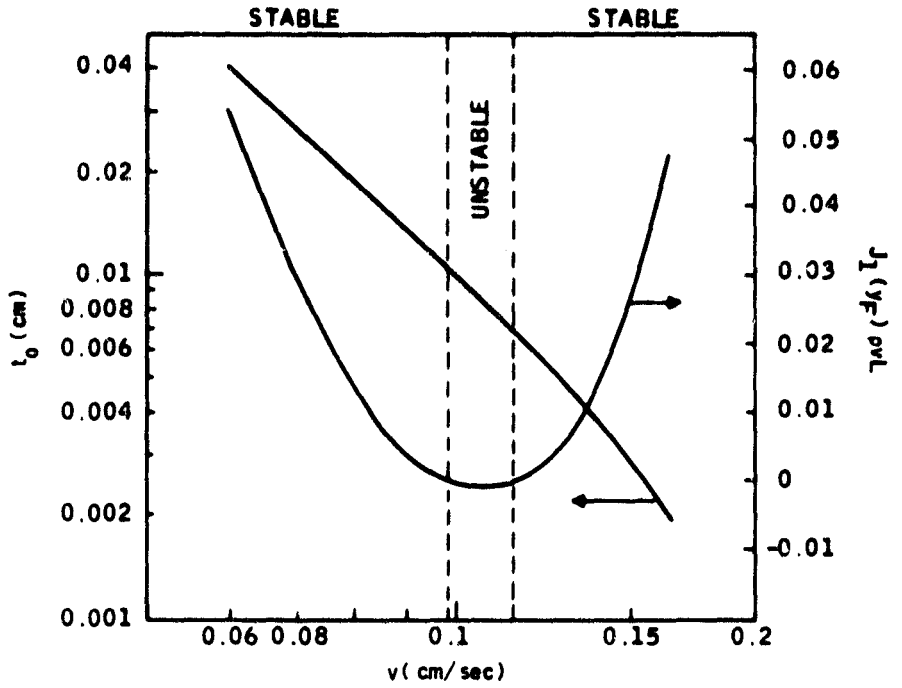


Figure 57. Normalized J_1 (y_F) and silicon thickness as functions of pull speed. $T_M - T_F$ fixed at 15.1°; t_c = 0.1cm; $T_M - T_o$ = 1385K; $T_M - T_1$ = 50K; y_F - 0.5cm.

Figure 58 gives conditions of limiting stable growth; in other words, v and T_M are simultaneously varied to keep $J_1(y_F) = 0$. Solid curves represent the effects of two substrate thicknesses. Dashed lines are limiting growth conditions for unsupported silicon from the one-dimensional analysis.[16] That analysis predicts a constant $v^2 t_o$ for each background temperature, giving straight lines with a slope of -2 on the logarithmic plot. On the other hand, the $v^2 t$ product for SOC is seen to fall rapidly at higher pull speeds, as thermal convection in the ceramic begins to dominate the heat disposal problem. The experimental data shown were obtained with the "fast dipper" on 0.1cm-thick ceramic with an undetermined background temperature.

The Role of T_1 and y_F -- The calculations discussed so far have been based on the values $y_F = 0.5$cm and $T_M - T_1 = 50°$. To test the generality of the results, the calculations for the Fig. 58 curves were repeated for two different combinations of y_F and T_1: (1) $y_F = 0.69$cm, $T_1 - T_M = 50°$; (2) $y_F = 0.5$cm, $T_1 - T_M = 300°$. It was found that these new combinations gave

the same limiting v vs. t_o relationships as before. This is a surprising result and it indicates that neither of these parameters has a significant effect on the important limiting relationship This also tends to enhance the credibility of our earlier analysis of the unsupported sheet silicon growth, in which J_1 was assumed equal to zero, and further details of the liquid meniscus, such as its shape and temperature distribution, were ignored.

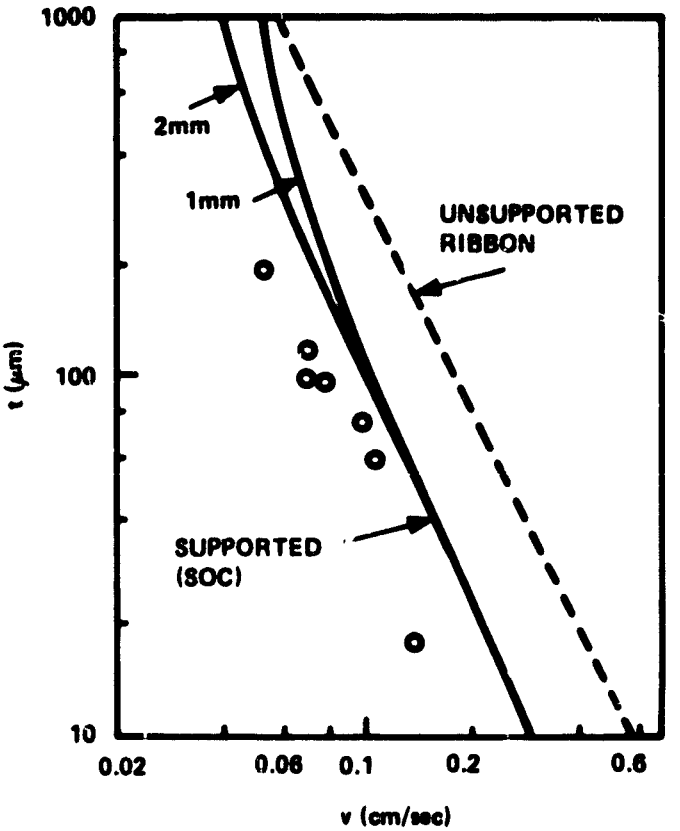


Figure 58. Silicon thickness versus pull speed for supported (1mm and 2mm substrates) and unsupported[16] growth. Maximum stable growth assumed [$J_1(y_F) = 0$]. $T_M - T_o$ = 1385K. Experimental data (circles) obtained on 1mm unslotted substrate.

Isotherms Shapes Within the Solid Silicon -- The isotherms were assumed flat in the silicon part of the structure. The error in this assumption may be estimated by analyzing heat flows up the silicon and laterally toward the radiation and ceramic surfaces. In the solid silicon portion, the greatest departure from flatness occurs near the freezing isotherm itself, so the discussion is restricted to that region. No attempt is made to examine the liquid portion. We proceed as follows.

Let $\vec{j}_1$ and $\vec{j}_2$ be flux density vectors at the corners as shown in Fig. 59. In a column of cross-section dxdz, the latent heat released per unit time is $\rho_o vLdxdz$. This is obviously the same quantity as $|\vec{j}_1|$ dsdz; hence,

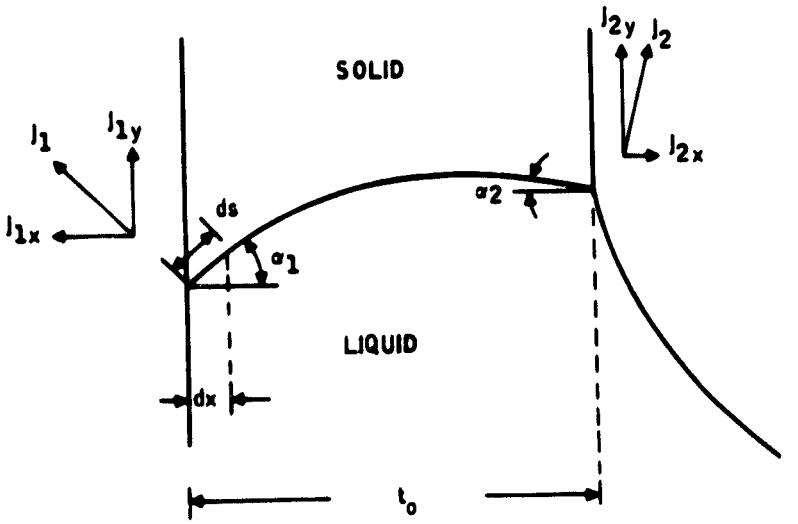


Figure 59. Analysis of freezing front shape by means of heat flux components.

$$|\vec{j}_1| = \rho_o vLdx/ds = \rho_o vL\cos\alpha_1 \tag{27}$$

Similarly,

$$|\vec{j}_2| = \rho_o vL\cos\alpha_2 \tag{28}$$

The lateral components are then

$$j_{1x} = \rho_o vL \sin\alpha_1 \cos\alpha_1 \tag{29}$$

$$j_{2x} = \rho_o vL \sin\alpha_2 \cos\alpha_2 \tag{30}$$

By continuity of lateral heat flow, j_{1x} is also the heat conducted into the ceramic:

$$j_{1x} = k_c |\partial T/\partial x| \tag{31}$$

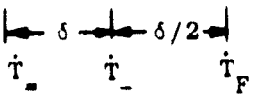
and J_{2x} is the radiated heat

$$J_{2x} = \epsilon_o \sigma \left(T_F^4 - T_o^4 \right) \tag{32}$$

$$\alpha_1 = 1/2 \sin^{-1} \left\{ 2k_c \left| \partial T/\partial x \right| / \rho_o v L \right\} \tag{33}$$

$$\alpha_2 = 1/2 \sin^{-1} \left\{ 2\epsilon_o \sigma \left(T_F^4 - T_o^4 \right) / \rho_o v L \right\} \tag{34}$$

The angle α_2 may be evaluated directly, but for α_1 it is necessary to calculate $\left|\partial T/\partial x\right|$. A three-point interpolation formula may be used incorporating the calculated temperatures at $y = y_F$ and the last three columns in the finite difference lattice, recalling the spacing as shown:



The interpolation formula yields

$$\frac{\partial T}{\partial X} = \frac{1}{\delta} \left(\frac{8}{3} T_F - 3\dot{T}_- + \frac{1}{3} \dot{T}_= \right) \tag{35}$$

at the right-hand edge.

Angles α_1 and α_2 are plotted against thickness, t_o, in Fig. 60 from data for the cold background case represented by the right-hand solid curve in Fig. 58. The maximum angles occur at the largest t_o, which is 0.1cm. We restrict our attention to this condition, which is the severest test of our flatness assumption.

In Fig. 61, that particular crystallization front is represented as a circular arc. From this geometry, the highest Δy spanned by the crysalization front is calculated to be 0.008cm. Since the finite difference increment, δ, is 0.02cm, we conclude that the worst-case Δy is only about half the numerical lattice spacing, and this justifies the flatness assumption.

It would be incorrect to conclude that most of the heat from the silicon is conducted into the substrate, although this is locally true near the interface, where $\alpha_1 > \alpha_2$. In fact, angle α_1 decreases and eventually becomes negative with increasing height above the interface. In the balance, more heat flows from the ceramic into the silicon than the other way around.

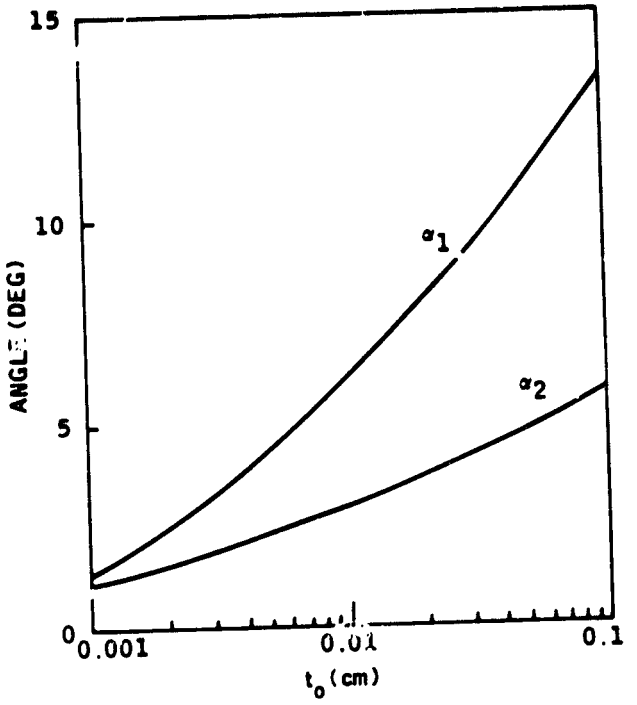


Figure 60. Inclinations of freezing isotherm versus silicon thickness. Growth conditions as in (a) of Fig. 58. α_1 = inclination at silicon interface; α_2 = inclination at as-grown surface.

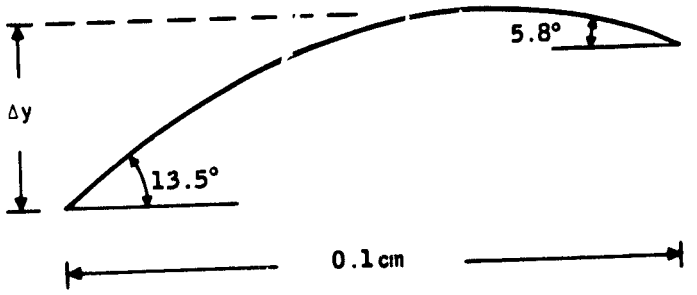


Figure 61. Approximate worst-case crystallization front geometry (exaggerated scale).

This is certainly to be expected in view of the large contribution made by the substrate to the total heat that must be radiated away.

Part II: Unsupported Wedge-Shaped (Asymmetric) Growth - The growth of unsupported sheet silicon or silicon ribbon from the melt can happen, in principle, in either of two modes, as illustrated in Fig. 62. In the conventional mode (a), the liquid-solid interface (LSI) is oriented approxi-

mately perpendicular to the pull direction, as was the case in the supported growth discussed in Part I. The latent heat of fusion released at the LSI is carried in the pull direction and must be disposed of by radiation and convection to the relatively cool environment of the solid ribbon. The word "symmetric" fits this mode because of the plane of symmetry through the half-thickness points. The other mode (b) lacks a plane of symmetry, as diagrammed here, and may be called "asymmetric." Because the LSI is inclined at a small angle, θ, to the pull direction, most of the latent heat of fusion is eliminated immediately by crossing transversely to the free solid surface. Only a small fraction of the latent heat remains to be disposed of downstream (upwards as represented in Fig. 62) from the solidification wedge. It is debatable whether asymmetric growth has ever been successfully demonstrated, but is is critically important technology to pursue theoretically and experimentally. It is inherently much faster than symmetric growth and may have other advantages such as entrapment of impurities.

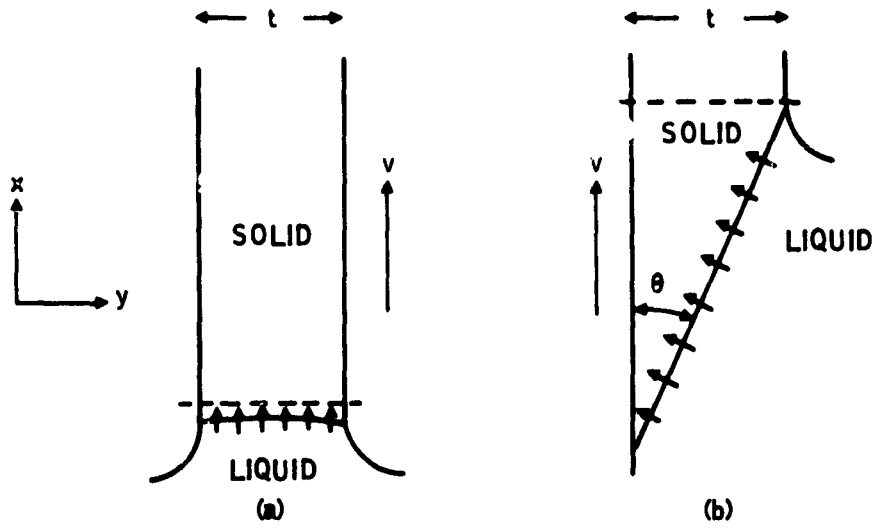


Figure 62. Silicon ribbon growth in (a) symmetric and (b) asymmetric modes. The letters v and t are pull speed and ribbon thickness, respectively.

A heat transfer model was developed for the wedge-shaped region[22] in asymmetric growth but it does not address the problem of how to cool the ribbon as it travels away from this region. This report indicates that downstream cooling is too rapid for pure wedge-shaped asymmetric growth if a 300K

22 J. Zoutendyk, "Theoretical Analysis of Heat Flow in Horizontal Ribbon Growth."

ambient is assumed for the entire solid ribbon. The cooling can be retarded to the proper rate by including postheaters in that apparatus. The present analysis applies directly to unsupported ribbon growth. Extension to supported asymmetric sheet growth, as in SOC, will be done at a later time.

In both symmetric and asymmetric growth it is useful to consider lines of demarcation between the solidification zones and the fully developed solid, downstream regions. These are indicated as dashed lines in Fig. 62. The heat flux approaching the line from below, consisting of convected heat, heat flux from the liquid, and any latent heat of fusion not already disposed of, must balance the heat flux away from the line into the downstream region. This simple conservation principle leads to a v vs. t tradeoff in the case of unsupported symmetric growth, as reviewed briefly below. In the asymmetric growth model, the conservation of heat flux does not imply any direct tradeoff limitation, but it does dictate the use of postheaters.

Review of Symmetric Growth Model -- The conservation principle for symmetric growth can be expressed as

$$t(\rho cvT_F + J_o + \rho Lv) = t(kq + \rho cvT_F) \qquad (36)$$

where ρ and c are the density and heat capacity of solid silicon at $T \sim T_F$, T_F is the melting temperature, J_o the x-component of heat flux density in the liquid, L is the latent heat of fusion, k is the heat conductivity of solid silicon (independent of temperature in this analysis), and $q = -dT/dx$, the downstream component of the temperature gradient at the dotted line in Fig. 62a. Values used for these parameters are given in Table 15. The first term in Eq. (36) represents convected heat flux, the second term is the heat flux from the liquid silicon, and the third term is heat flux due to latent heat of fusion. The tkq term is heat flux by conduction into the downstream solid region. Note that convected heat cancels in Eq. (36). If J_o is assumed equal to zero (maximum throughput), the equation becomes

$$\rho Lv/k = q\big|_{T=T_F} \qquad (37)$$

The value of q is derived independent of the solidification zone parameters by integrating the heat equation for the downstream silicon portion, subject to appropriate initial condition. Since symmetric growth is very nearly one-dimensional in character, the following heat equation is convenient to use:[16]

Table 15. Values for silicon parameters for Part II.

Parameter	Value
ρ	2.33 g/cm^3
c	0.954 J/g deg
k	0.216 W cm/deg
L	1802 J/g
T_F	1685K
J_o	0.0 W/cm^2

$$t\left|k\, q\, \frac{dq}{dT} + \rho cv\, q\right| = F(T,\ T_A) \qquad (38)$$

where F is the cooling function depending on the ribbon temperature, T, and effective ambient temperature, T_A. This equation is equivalent to the standard one-dimensional heat equation in which the coordinate x is the independent variable. The transformation was made by substituting -q for dT/dx. If heat disposal is by radiation from both surfaces to an effective 300K blackbody ambient, Eq. (38) becomes

$$t\left|kq\, \frac{dq}{dT} + \rho cv\, q\right| = 2\varepsilon\sigma\ (T^4 - 300^4) \qquad (39)$$

The initial condition is that the gradient, q, tends to zero as T approaches ambient; i.e., q(300) = 0. The solid silicon emissivity is taken to be ε = 0.46, and Eq. (39) is integrated numerically from T = T_A to T = T_F, since $q(T_F)$ is the value required in Eq. (37).

The q obtained from the integration depends upon t, and to a lesser extent upon v due to the convective term in Eq. (39). Figure 63 is a plot of q vs. t for various pull speeds, along with $\rho Lv/k$ (dashed lines). The intersections of the two sets, marked with heavy dots, reveal the v vs. t tradeoff and illustrate the flux conservation principle.

Ribbon Thickness in Asymmetric Growth -- A thermal model of asymmetric growth is independent of orientation, and the pull direction has been taken vertically (Fig. 64) for comparison with symmetric growth. We will use a horizontal orientation in the later analysis. Mechanical factors could dictate other orientations, such as the one shown in Fig. 64. In this configuration, point A, which presumably defines the downstream limit of the

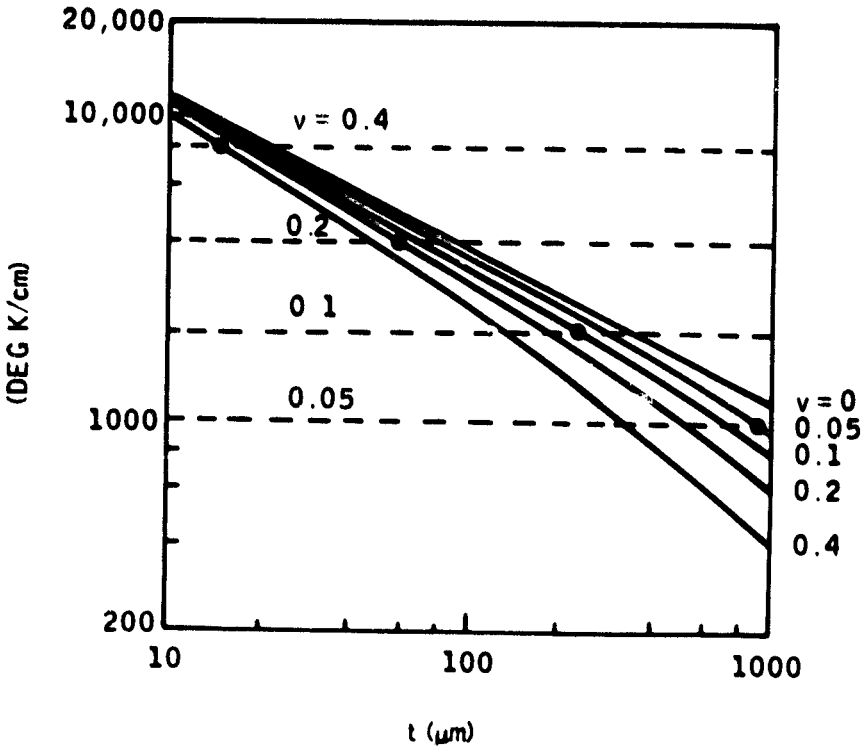


Figure 63. Heat fluxes from solidification region (dashed lines) and into downstream region (solid lines). Balance is at the intersection points (heavy dots), establishing the v versus t tradeoff for symmetric growth.

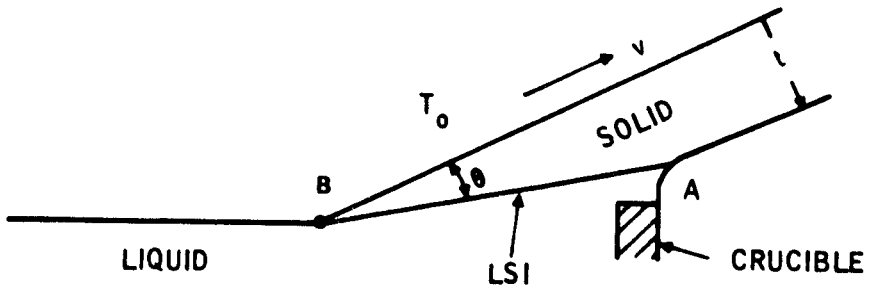


Figure 64. Nonvertical implementation of asymmetric growth.

LSI, is fixed by meniscus stability consideration.[23] The wedge angle, θ, is given by

$$\theta = \varepsilon\sigma \left(T_F^4 - T_o^4\right)/\rho vL \text{ radian} \tag{40}$$

if heat flux into the LSI from the melt is neglected.[22] If the top-side ambient T_o is 300K, this becomes

$$\theta = 0.005/v$$

and for pull speeds of the order of 0.1 cm/sec or higher, the wedge angle is less than 3^o. Although θ is established by thermal considerations involving the pull speed, the thickness, t, is not, since

$$t = \theta \cdot AB \tag{41}$$

and the length AB is an adjustable parameter based on the design of the apparatus. The position of B might be fixed, for example, by heating the melt surface to the left of B and allowing it to cool on the right. Equations (40) and (41) show that an indirect tradeoff exists between v and t; given a fixed wedge length AB, t is inversely proportional to v. For the subsequent calculations, this dimension is arbitrarily assumed to be 0.8cm.

Temperature Profile in the Solidification Region -- Subject to a number of assumptions which will be examined, the two-dimensional heat equation yields a nearly linear temperature distribution in the solid portion of the region $x = 0$ to $x = \ell$ (see Fig. 65):

$$T(x,y) = T_F - \Delta \cdot (x/\ell - y/t) \tag{42}$$

with

$$\Delta = \varepsilon\sigma\left(T_F^4 - T_o^4\right) \cdot t/k \tag{43}$$

and

$$t/\ell = \theta = \varepsilon\sigma \left(T_F^4 - T_o^4\right)/\rho vL \tag{44}$$

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[23] C. A. Rhodes, M. M. Sarrof and C. H. Liu, "Investigation of the Meniscus Stability in Horizontal Crystal Ribbon Growth," J. Crystal Growth 50, pp. 99-101 (1980).

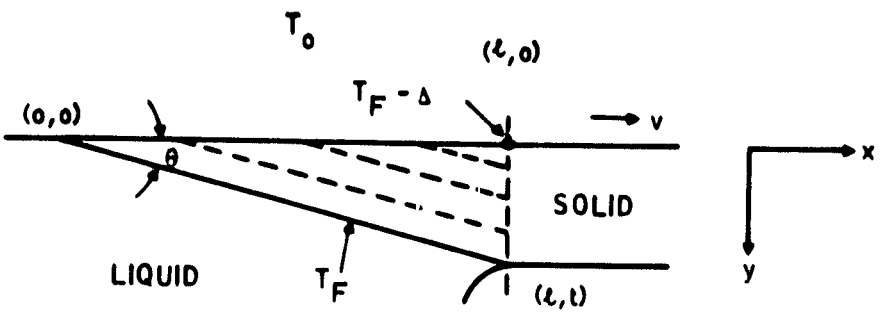


Figure 65. Linear temperature distribution in wedge-shaped solidification region.

The validity of the assumptions rests on their self-consistency, which we will attempt to establish:

1) We assume the LSI is indeed a straight line and an isotherm at temperature T_F.

2) Given (1), the linear temperature distribution obviously satisfies the steady-state heat equation:

$$k(\partial^2 T/\partial x^2 + \partial^2 T/\partial y^2) - \rho cv\ \partial T/\partial x = 0 \qquad (45)$$

provided that the ρcv term can be neglected, Zoutendyk[22] gives the following condition for neglecting the ρcv term:

$$vt << k/\rho c = 0.097 \qquad (46)$$

We will return to this condition.

3) A heat flux emerges from the LSI due to the latent heat of fusion. If there are no temperature gradients in the liquid, this flux is normal to the LSI and of constant density. That is,

$$J = \rho vL \sin\theta \qquad (47)$$

because the LSI is a straight line of length $t/\sin\theta$ and the total flux is ρvLT. From Eqs. (42) and (47) we see that

$$J_x = k\Delta/\ell = \rho vL\sin^2\theta \tag{48}$$

and

$$J_y = k\Delta/t = \rho vL \sin\theta \cos\theta \tag{49}$$

4) The radiated flux density from the surface y = 0 is approximately constant, provided that Δ is small, and equal to $\varepsilon\sigma\left(T_F^4 - T_o^4\right)$. Equating this to the vertical component J_y in Eq. (49) gives

$$\Delta = \varepsilon\sigma\left(T_F^4 - T_o^4\right)\cdot t/k \tag{50}$$

which establishes Eq.(43)and confirms that Δ is small ($\Delta = 4.9^o$ if t = 0.1cm).

5) Combining Eqs. (43) and (49) also gives

$$\sin\theta\cos\theta \simeq \theta \simeq \varepsilon\sigma\left(T_F^4 - T_o^4\right)\Big/\rho vL \tag{51}$$

which establishes Eq.(49).Finally, since $\theta \simeq t/\ell$, Eq. (51) may be rewritten as

$$vt \simeq \varepsilon\sigma\left(T_F^4 - T_o^4\right)\cdot \ell/\rho L \tag{52}$$

or vt ≃ 0.005 if $\ell \simeq$ 1cm. (It has been already noted that ℓ is somewhat arbitrary.) Since 0.005 << 0.097, the condition Eq. (46) for neglecting the ρcv term is satisfied.

Matching the Temperature Distribution to the Downstream Region -- As observed previously, the component of latent heat carried downstream is much smaller in asymmetric growth. In fact, since

$$J_x = \rho vL\sin^2\theta \simeq \left[\varepsilon\sigma\left(T_F^4 - T_o^4\right)\right]^2/\rho vL$$

from Eqs. (44) and (48), the conservation principle for the wedge model becomes

$$\left[\varepsilon\sigma\left(T_F^4 - T_o^4\right)\right]^2/\rho vLk = q\Big|_{T\sim T_F} \tag{53}$$

For a cooling environment of 300K along the whole silicon ribbon, q was found to be in the 10^2 to 10^4 deg/cm range (Fig. 63), whereas the left-hand side of Eq. (53) is much smaller (e.g., about 5 deg/cm for v = 0.1 cm/sec). It is obvious that the cold downstream environment is not compatible with the wedge model. We will see in more detail later (Fig. 70) what happens when we try to force the cold downstream environment on the wedge model.

It is not so obvious that the cold environment precludes any kind of asymmetric growth. It is conceivable that some kind of curved LSI is possible with a portion of it nearly parallel to the surface, for higher throughput, and another portion at a large inclination to the surface in order to match the high q.

The approach taken here is an attempt to stabilize the wedge pattern by extending the linear distribution for some distance into the downstream region. This will automatically satisfy continuity of not only $\partial T/\partial x$ but $\partial T/\partial y$ as well. It is assumed that afterheaters can be constructed to provide an arbitrary distribution, $T_A(x)$, of effective ambient temperature on the meniscus side of the ribbon. The other side will remain exposed to the cold ambient. A restriction on this approach is that $T_A(x)$ (i.e., the design of the afterheaters) must depend on v and t. A change in either of these parameters would force a redesign of the afterheaters. The required $T_A(x)$ is estimated using the one-dimensional heat equation, Eq. (38), and then "verified" by applying it to a computer program which (numerically) solves the two-dimensional heat equation for the entire silicon ribbon. The method is demonstrated for the particular case, ℓ = 0.8cm, v = 0.1 cm/sec, and t = 0.04cm.

To begin, let $F(T, T_A)$ in Eq. (38) be written

$$F\left[T,\ T_A(T)\right] = f(T,300) + f\left[T,T_A(T)\right] \tag{54}$$

where $f(T,U) = \varepsilon\sigma(T^4 - U^4)$ and hence $F(T,300) = 2f(T,300) = 2\varepsilon\sigma(T^4 - 300^4)$. The procedure will be to find a $T_A(T)$ to suit our purposes and then convert to $T_A(x)$ using

$$x = \ell + \int_{T_F}^{T} - dT/q(T) \tag{55}$$

where q is obtained from Eq. (38) with $T_A = T_A(x)$. Let $q_o(T)$ be the integral of Eq. (38), with $T_A = 300K$. This is plotted in Fig. 66 over the range $T \sim 1685K$ to $T = 1200K$. For the desired distribution, q(T), let the linear temperature range (constant $q = \Delta/\ell$) be extended to $x = 1.2\ell = 0.96cm$, and let T_1 and T_2 denote the half-thickness temperatures at $x = \ell$ and $x = 1.2\ell$, as in Fig. 67. The values of T_1 and T_2 are indicated in Fig. 66. Next, let q(T) increase as the temperature decreases from T_2 and join it smoothly to $q_o(T)$ at some T_3, as shown by the dashed curve in Fig. 66. "Smoothly" means that $q = q_o$ and $dq/dT = dq_o/dT$ at $T = T_3$.

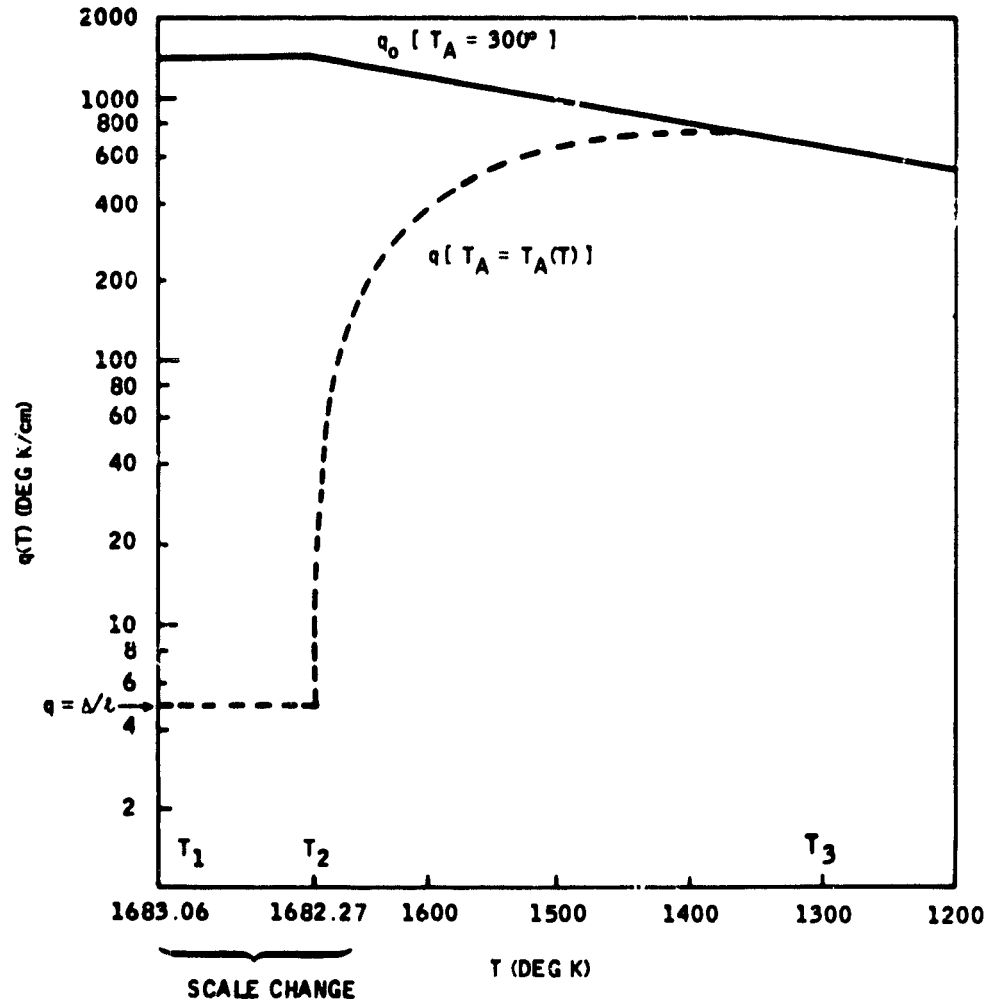


Figure 66. Original (q_o) and afterheater-modified (q) temperature gradients for the case v = 0.1 cm/sec, t = 0.04cm.

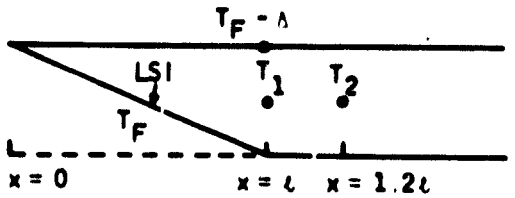


Figure 67. Linear temperature distribution.

Some observations may be inferred from the approach as outlined so far. It will be noted that q and q_o satisfy

$$t(k\ q\ dq/dT + \rho cv\ q) = F\left[T, T_A(T)\right] \tag{56}$$

and

$$t(k\ q_o\ dq_o/dT + \rho cv\ q_o) = F(T, 300) \tag{57}$$

Inspection of Fig. 66 reveals that $q \leq q_o$ and $qdq/dT \leq q_o dq_o/dT$. It follows that $F\left[T, T_A(T)\right] \leq F(T, 300)$, and, therefore, $T_A(T) \geq 300$. In other words, $T_A(T)$ is realiable with heaters. Second, since both q, q_o and their derivatives match at $T = T_3$, the value of $T_A(T)$ falls to 300K at $T = T_3$ and remains constant at lower ribbon temperatures. Finally, to the same approximations that were discussed earlier, continuity of both dT/dy and dT/dx is assured at $x = \ell$. That is, the linear temperature distribution is extended past $x = \ell$: (a) Since dT/dx is constant by design throughout the extension, dT/dy is also constant throughout the extension because $d^2T/dx^2 + d^2T/dy^2 = 0$ (neglecting the ρcv term). (b) Because the ambient seen by the ribbon surface opposite the meniscus is 300K, it follows that

$$dT/dy = (1/k)f(T_F, 300) \tag{58}$$

throughout the extension, as it is also in the wedge region. This is the primary rationale for placing the afterheaters on the meniscus side.

A simple function having the required properties is

$$q(T) = \Delta/\ell + a_1(T_2 - T) + a_2(T_2 - T)^2, \text{ where } T_2 \geq T \geq T_3 \tag{59}$$

with a_1 and a_2 selected so that $q(T_3) = q_o(T_3)$ and $q'(T_3) = q_o'(T_3)$. If $T_3 = 1300K$, these are $q(T_3) = 672.17$ and $q'(T_3) = 1027.46$, and the coefficients are found to be $a_1 = 5.0197$ and $a_2 = -0.0085649$. Now $T_A(T)$ is easily determined algebraically from Eq. (38) over the range $T_1 > T > T_2$ using $q = \Delta/\ell$ and $q' = 0$, and over the range $T_2 > T > T_3$ using q and q' from Eq. (59). Then $T_A(x)$ may be found by integrating as in Eq. (55) to obtain the relation between x and T.

Two-Dimensional Verification -- The two-dimensional steady-state heat equation, Eq. (45), was solved numerically on a 7 x 300 grid representing a rectangular region t = 0.04cm wide and about 2.4cm long. The first 0.8cm (100 grid points) corresponds to the wedge portion, the next 0.16cm (20 grid points) represents the linear extension region $T_1 > T > T_2$, and the remainder covers the rest of the afterheater distribution, including a very short final portion (approximately 0.04cm in length) where $T_A = 300K$. Boundary conditions were set up as indicated in Fig. 68. Temperatures were specified on segments 1, 2, and 5, whereas derivative conditions were used on segments 3 and 4 corresponding to the nonlinear radiation law. An approximately linear temperature distribution was set up in the wedge region by treating the liquid as an extension of the solid. The temperature on the edge segments 1 and 2 was set to increase linearly from T_F at the LSI corners to $T_F + \Delta$ at (o,t).

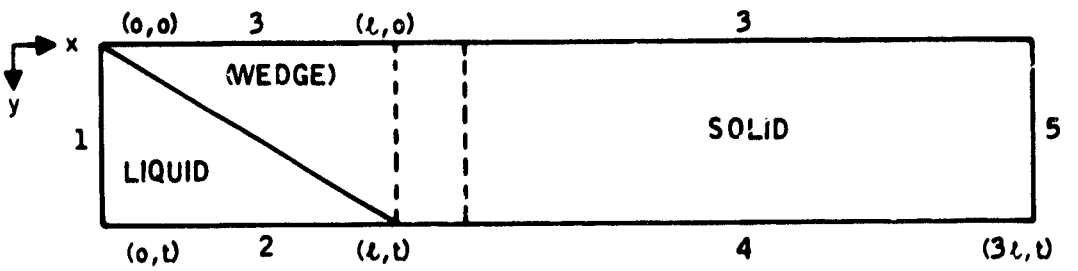


Figure 68. Boundary conditions for numerical integration of Eq. (57). Segment 1: $T = T_F + (y/t)\Delta$. Segment 2: $T = (T_F + \Delta) - (x/\ell)\Delta$. Segment 3: $|\partial T/\partial y| = (1/k)$ f (T, 300). Segment 4: $|\partial T/\partial y| = (1/k)$ f $[T, T_A(x)]$. Segment 5: T = 1275K.

The 2100-point system was solved by means of a successive over-relaxation method. The main features of the calculated temperature distribution are plotted in Fig. 69 along with the effective ambient, $T_A(x)$. The partials $\partial T/\partial x$ and $\partial T/\partial y$ are of particular interest and are seen to remain essentially constant through the solidification region, ending at the point marked with an arrow. In other words, the linear profile remains intact throughout this region. The required T_A is approximately constant at just over 2000K to a distance of 1cm from the LSI-meniscus juncture and then falls rapidly to 300K over the next 0.55cm.

For comparison, Eq. (45) was solved with $T_A(x)$ set equal to 300K, corresponding to the omission of afterheaters. The boundary conditions on segments 1, 2, and 3 were the same as given in the caption for Fig. 68 except for segment 4, $\partial T/\partial y = (1/k)f(T,300)$. The results are plotted in Fig. 70. Note that the rapid downstream cooling causes drastic variations in both $\partial T/\partial x$ and $\partial T/\partial y$ near the LSI-meniscus juncture. It is clear that the linear temperature distribution is completely destroyed.

Summary --

Part I: Supported Symmetric Growth -- For supported symmetric growth, a steady-state vertical growth model of dip-coated SOC yields a system of nonlinear, coupled differential equations for the temperature profiles in ceramic and silicon portions of the structure. Cooling of the structure is assumed to be by radiation to a specified environment, and the cooling rate must balance the rates of diffusion of latent heat of fusion and convected heat from the melt. Liquid meniscus height is fixed by hydrostatic considerations and does not vary over the normal range of growth speed. Because of the complicated geometry and essential nonlinearity of the system, numerical solution of the equations is the method of choice.

Due to the overall heat balance requirement, only certain combinations of ceramic thickness (T_C), silicon coating thickness (T_O), pull speed (v), and melt temperature (T_M) will yield steady-state temperature profiles. In actual growth, the coating thickness is not arbitrarily specified but is a dependent function of t_c, v, and $T_M(>T_F)$.

A theoretical stability criterion[18] places a further restriction on the allowable combinations of growth parameters. Growth is not stable if heat

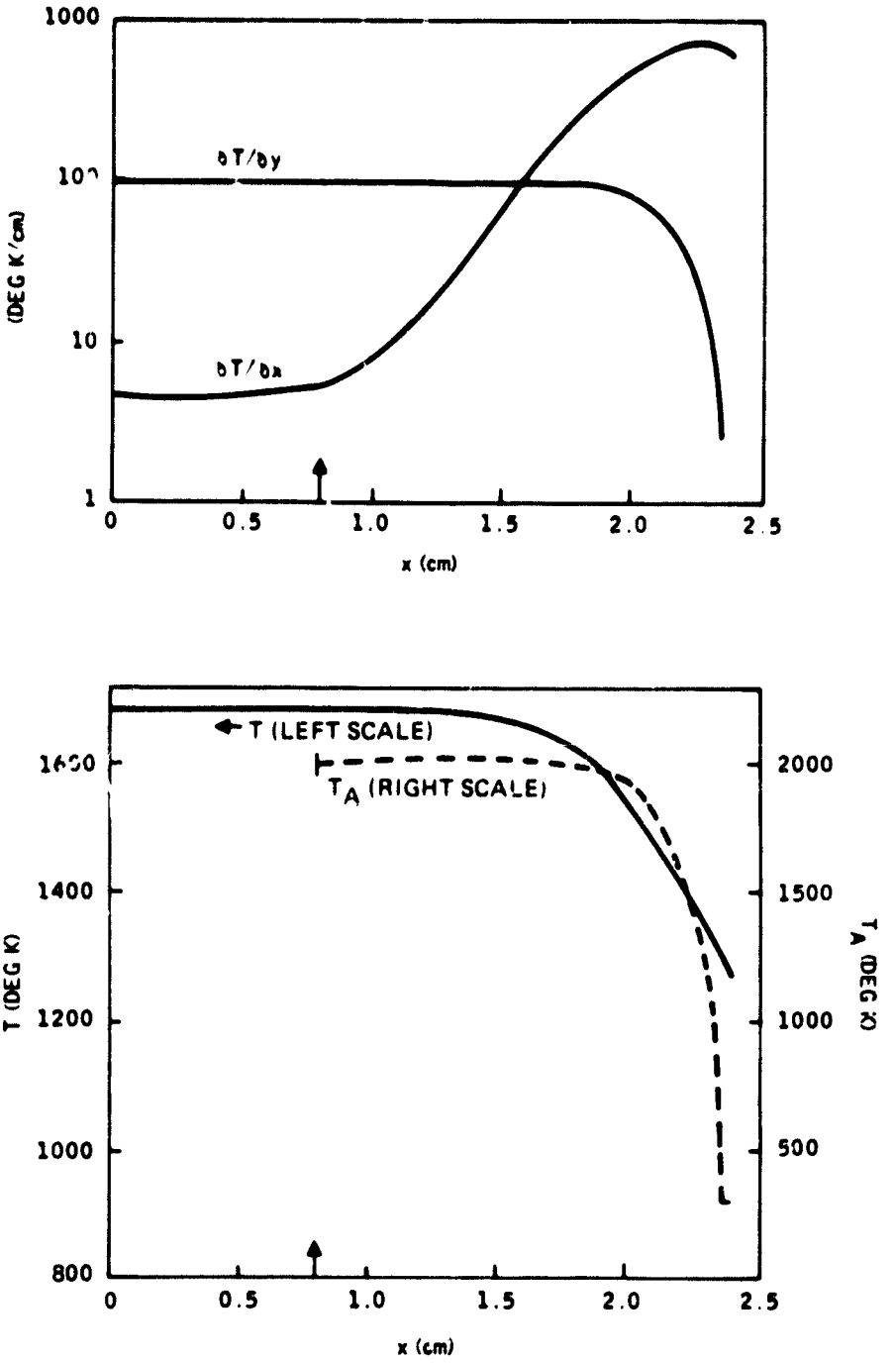


Figure 69. Two-dimensional temperature distribution in silicon ribbon drawn through the heated environment, $T_A(x)$ (dashed curve). T and the partials, $\partial T/\partial x$ and $\partial T/\partial y$, are averaged over the width of the ribbon. A well-established linear temperature distribution is indicated by the near constancy of $\partial T/\partial x$ and $\partial T/\partial y$ up to the end of the wedge (marked with an arrow).

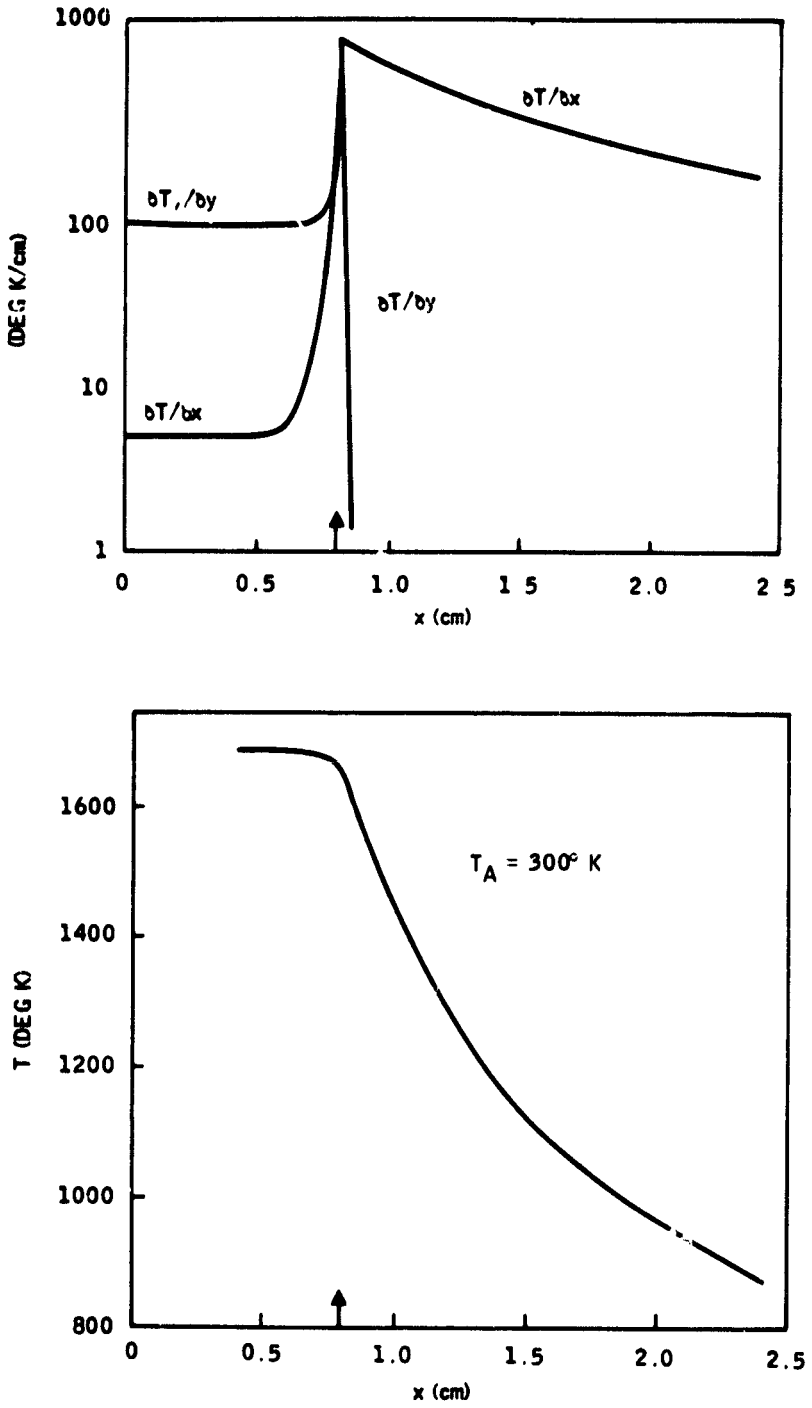


Figure 70. Two-dimensional temperature distribution in silicon ribbon with no heated environment. The linear temperature distribution is totally destroyed, indicating that a wedge-shaped solidification zone is not possible in a cold environment.

flows backwards from the crystallization fronts; in other words, stability requires that $dy/dy\ U_1 j(y_F) < 0$. For given pull speed, t_o increases monotonically as T_M is lowered toward T_F, but $d/dy\ U_1(y_F)$ decreases at the same time. Maximum coating thickness for stable growth occurs, therefore, when $d/dy\ U_1(y_F) = 0$. This limiting thickness and the corresponding melt temperature both depend on pull speed, ceramic thickness, and radiation environment.

Finally, the one-dimensional approximation in solid-silicon portion was critically examined by estimating the maximum departure, Δy, from flatness for the freezing isotherm. This turned out to be of the order of 0.01cm, which would appear to justify the approximation. Also, the freezing isotherm was found to be bowed upward, making a large inclination to the horizontal at the ceramic surface than at the as-grown surface. Although most of the latent heat is carried vertically, this would indicate that the net lateral heat transfer in the neighborhood of the freezing front is into the ceramic as opposed to out from the free surface. This is true only locally, however. In fact, over the structure as a whole, net heat transfer across the silicon-ceramic interface is from ceramic to silicon, and not the other way around.

Part II: Unsupported Wedge-Shaped (Asymmetric) Growth - In part II, we have attempted to establish some consistent thermal conditions for high-speed, asymmetric growth. It is theoretically possible to grow thicker layers of silicon at a given pull rate in asymmetric growth. One way to explain this is in terms of the rapid removal of the latent heat of fusion. This takes place on a radiating surface very close to its source in the liquid-solid interface. In symmetric growth, heat tends to be transported farther in the solid material before being released (less efficiently) at a lower radiation temperature. A thermal analysis of the asymmetric growth zone, together with the cooling portion downstream, has shown that a post-heater is a necessary part of the growth apparatus if a strictly wedge-shaped growth zone is to be maintained.

Dip-Coating Results

Introduction - When a 7cm x 5cm carbon-coated mullite substrate is dipped into and subsequently pulled from a silicon melt, silicon coatings or layers of large elongated grains result which are aligned in the direction

of withdrawal. When growth conditions are proper, the layers are smooth and shiny in appearance as shown in Fig. 71. To satisfy the needs of this R&D program, the number dipped in this manner was in the thousands during the course of the investigation.

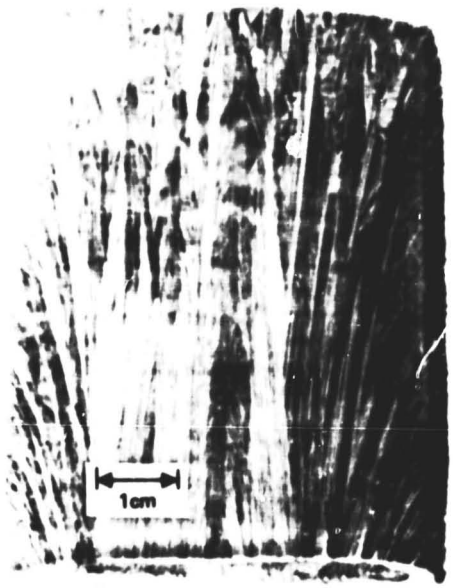


Figure 71. Etched surface of SOC sample. Note the directionality of the structure and grain size.

This subsection of the report describes the experimental options investigated, along with growth parameters of the technique and the physical and electrical properties of the resulting layers.

Angle Dip-Coating - In the interest of improving grain size and/or growth rate, a number of substrates were dip-coated, with the substrates held at an angle as opposed to being perpendicular to the melt. Examination of these silicon coatings showed that angle dipping did not drastically alter the rate or manner in which the coatings solidified. The coatings looked

quite comparable to those dipped vertically, with coating thickness decreasing with increasing pull rate.

Silicon-Ceramic Bonding - Initially, it was assumed that the silicon reacted with the carbon to form a thin silicon-carbide (SiC) film which subsequently wet the silicon. It was further presumed that this thin SiC film penetrated the pores of the ceramic to form a mechanical bond. Occasional layer separation from the ceramic substrate prompted a further study of this silicon-substrate bonding mechanism.

It was observed that if a very thorough and heavy carbon coating was applied to the substrate, thicker (125 to 250μm) silicon layers sometimes flake off if the total time the substrate remains in the melt is short. This conclusion is further supported by the fact that the flaking occurs more predominantly near the top of the substrate (that portion which remains in the melt the least time). Visual Microscopic examination of the bottom surface of separated layers, along with examination of that portion of the substrate from which it separated, strongly suggests that the formation of SiC, if any, plays an insignificant role in bonding the silicon layers to the substrate.

One could conclude from the visual inspection, however, that silicon bonds directly to the pores of the ceramic only in regions where there are voids in the carbon coating. These voids could occur partially by an incomplete carbon coating and partially by the thinner regions of the carbon coating entering the silicon solution upon dipping. From the beginning, it was observed that when the substrate was dipped approximately 1/8 inch into the melt and allowed to remain there for a prolonged time, this portion of the substrate had a poor silicon coating. This small portion of the silicon-coated substrate also had a distinct absence of carbon remaining. The possibility exists that at this high temperature there is sufficient oxygen present from the disintegrating quartz crucible to permit carbon monoxide to form, but it is also possible that the carbon is merely going into the silicon solution.

Further examination of coated substrates revealed that layers which have separated from the substrate all remained in the melt relatively short periods of time. On the other hand, if the carbon coating were too thin, the entire carbon film could be dissolved before the silicon could

intermittently wet and bond to the substrate, thus producing only spotty wetting. While the presence of a carbon coating is essential to producing a silicon coating on a ceramic substrate, it appears to act merely as a wetting agent.

Figure 72 shows the silicon-ceramic interface of substrate MR-8, unetched. The silicon-ceramic bond is apparently mechanical in nature, formed when the molten silicon penetrates the porous substrate. This intimate contact is achieved over less than 10% of the surface but is generally sufficient to provide excellent adherence of the film to the substrate. The black areas between the silicon and ceramic are believed to be holes where unreacted carbon was pulled out during polishing. Figure 73 shows photographs of the

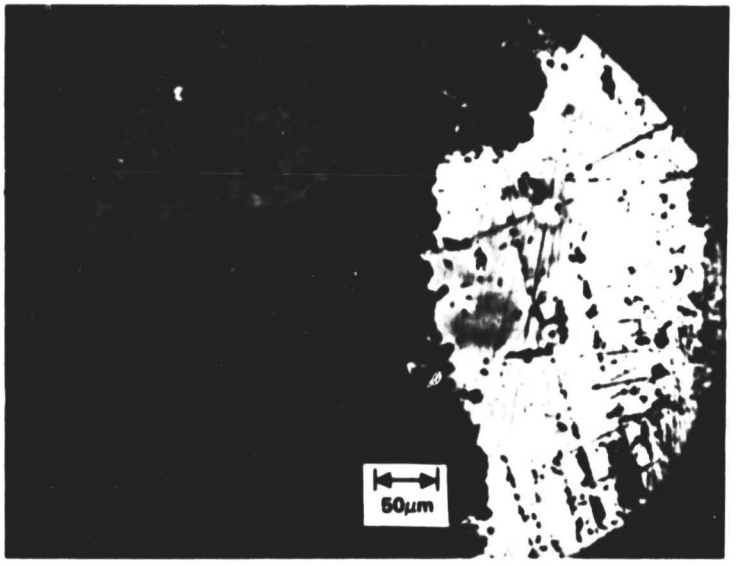
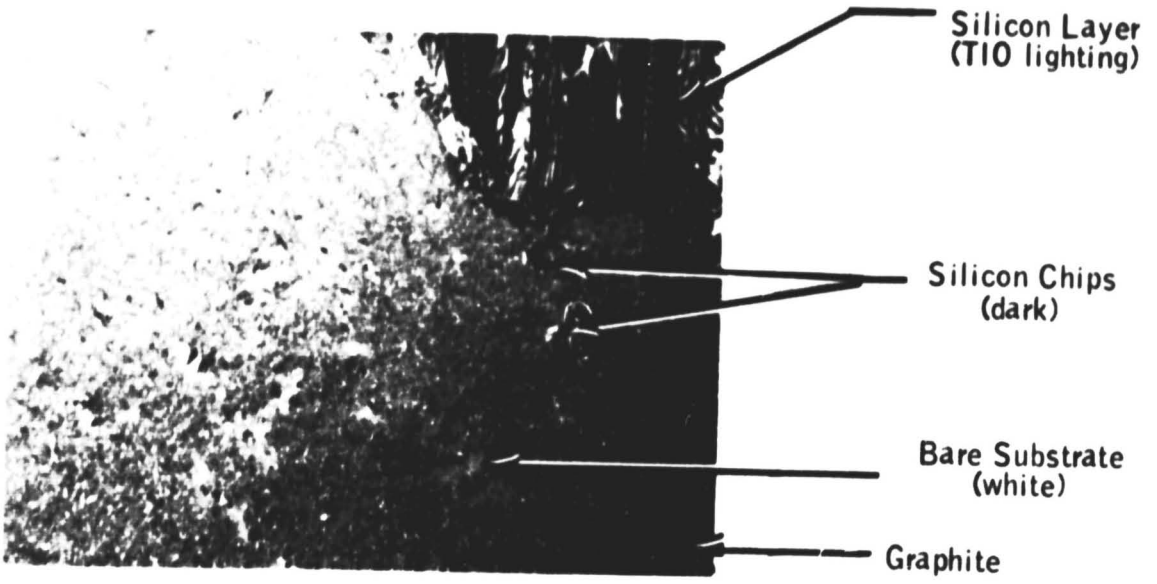
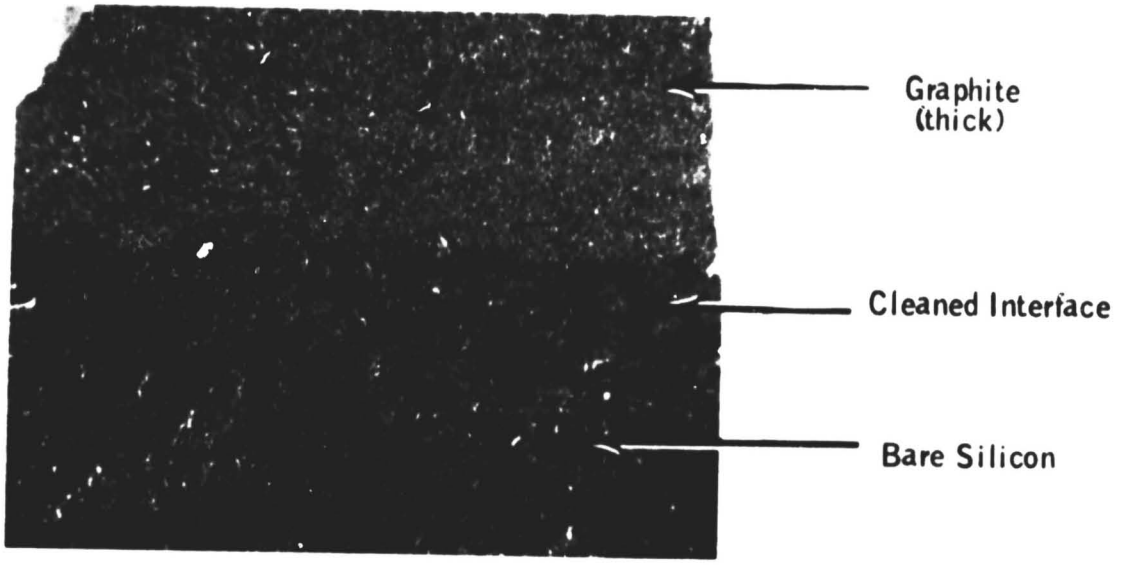


Figure 72. Silicon-ceramic interface (unetched) of substrate MR-8.

back side of a portion of a separated silicon layer and that portion of the substrate from which it separated. These photographs further illustrate that the silicon bonds directly to the substrate only in regions that are void of the carbon coating.



(a) Substrate (30x).



(b) Separated layer (30x).

Figure 73. Substrate MR-32 and separated layer.

Figure 74 shows photographs of silicon-alumina and silicon-pressed mullite interfaces, respectively, where the ceramics are not as porous as the rolled mullite and not penetrated by the molten silicon. It was noted that the silicon coating did not adhere as well to these denser ceramics as it did to the more porous mullite. However, it was also noted that if an exceptionally heavy carbon coating is supplied to the mullite, the silicon does not adhere well to it either.

Seeded Growth - In an effort to promote large-grain growth, four substrates were dipped with single-crystal silicon seeds attached. Thin wafers of single-crystal silicon were simply clamped to the substrate at the top edge of the carbon coating. The results can be seen in Fig. 75, which shows the interface between the single-crystal seed and the ensuing silicon film. Although the desired result, single-crystal film growth, did not occur, the procedure shows promise. The seed-film junction is continuous, indicating that with a suitably oriented seed, large grain growth may be induced.

Growth Parameters - It was observed early in the program that the layer thickness was dependent on such growth parameters as melt temperature and growth rate (pulling speed in the dip-coating technique). The layer thickness was inversely related to both melt temperature and growth rate. This observation, along with other unexplanable observations, gave rise to the previously discussed growth modeling study in support of our experimental effort. Velocity thickness data are summarized in Fig. 76. The straight lines denote constant values of v^2t product. We observe that at a given crucible position the maximum thickness at a given velocity tends to a constant v^2t relationship. When the crucible is low with respect to the heater, the v^2t product also is lower.

Early in the program we were not sure where solidification occurred along the SOC layer. Now, however, we believe that solidification occurs at the top of the meniscus. Direct evidence of this is a bright line right at the upper edge of the meniscus. The increased brightness is due to the higher emmissivity of the solid. The narrowness of the line is because of the steep temperature gradient in the solid. Our observations can be summarized as follows:

1) Solidification takes place at the edge of the meniscus. This is the same as in Czochralski growth and ribbon growth.

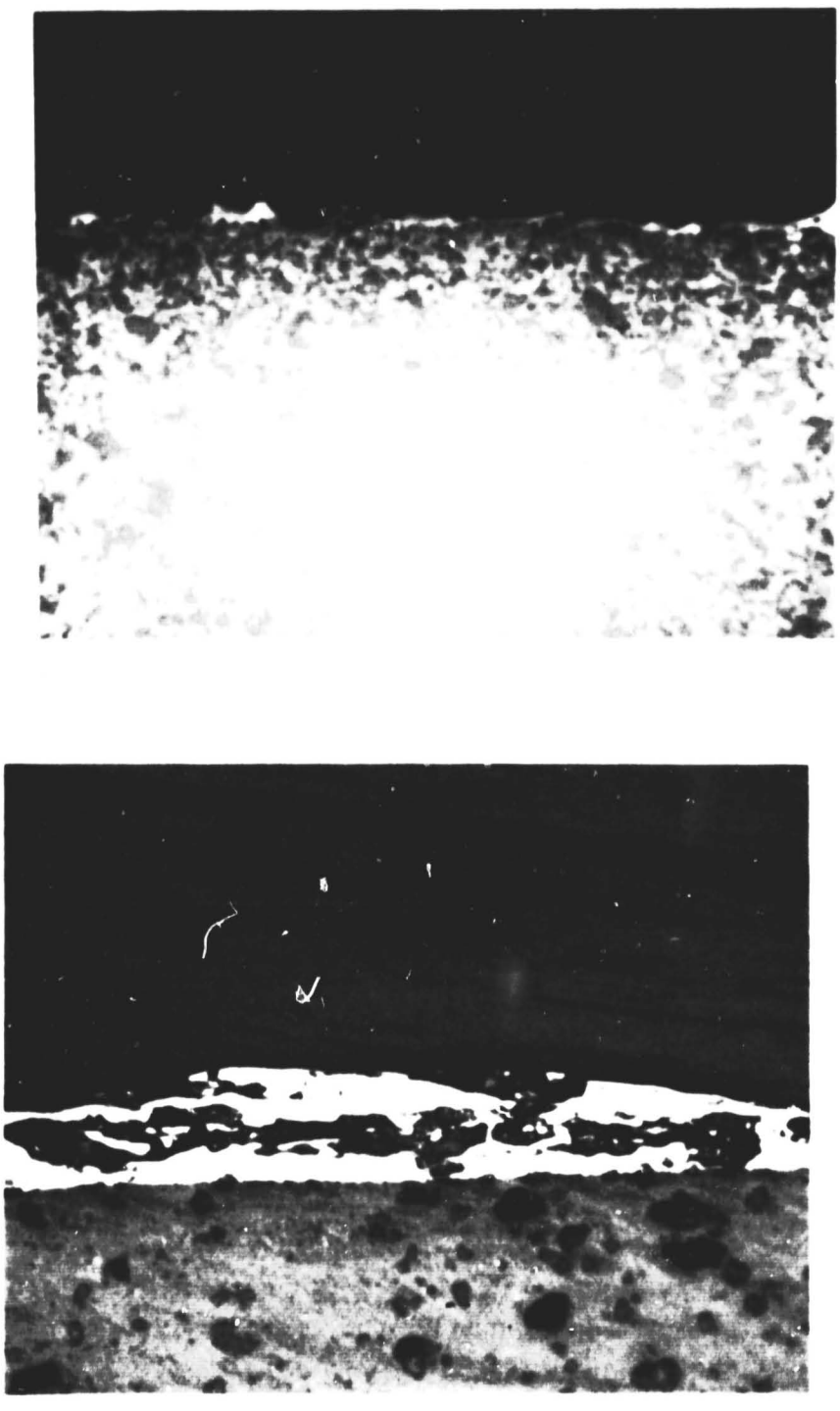


Figure 74. Silicon-alumina interface (top) and silicon-pressed mullite interface (200x).

Figure 75. Seeded silicon sheet growth. The seed is the trapezoidal shape at the top of the photo (Wright etch, 2.5x).

2) The meniscus height is constant over the range of velocities normally used: 2.4 to 6.0 cm/min.

3) The contact angle between the liquid and solid is 11^{o} as in other types of growth from the melt except the ribbon-to-ribbon case.

4) Starting from good conditions of growth, an increase in the melt temperature, T_m, always causes a decrease in thickness. Films can be grown in a melt temperature range of at least 20 to 30K.

5) At a given velocity, T_m can be decreased to a minimum value, T_{mo}, corresponding to maximum thickness. Under these conditions, a few dendrites form at the top of the layer, but these decay within a few millimeters growth.

6) If T_m is further decreased below T_{mo}, dendrites will form and will

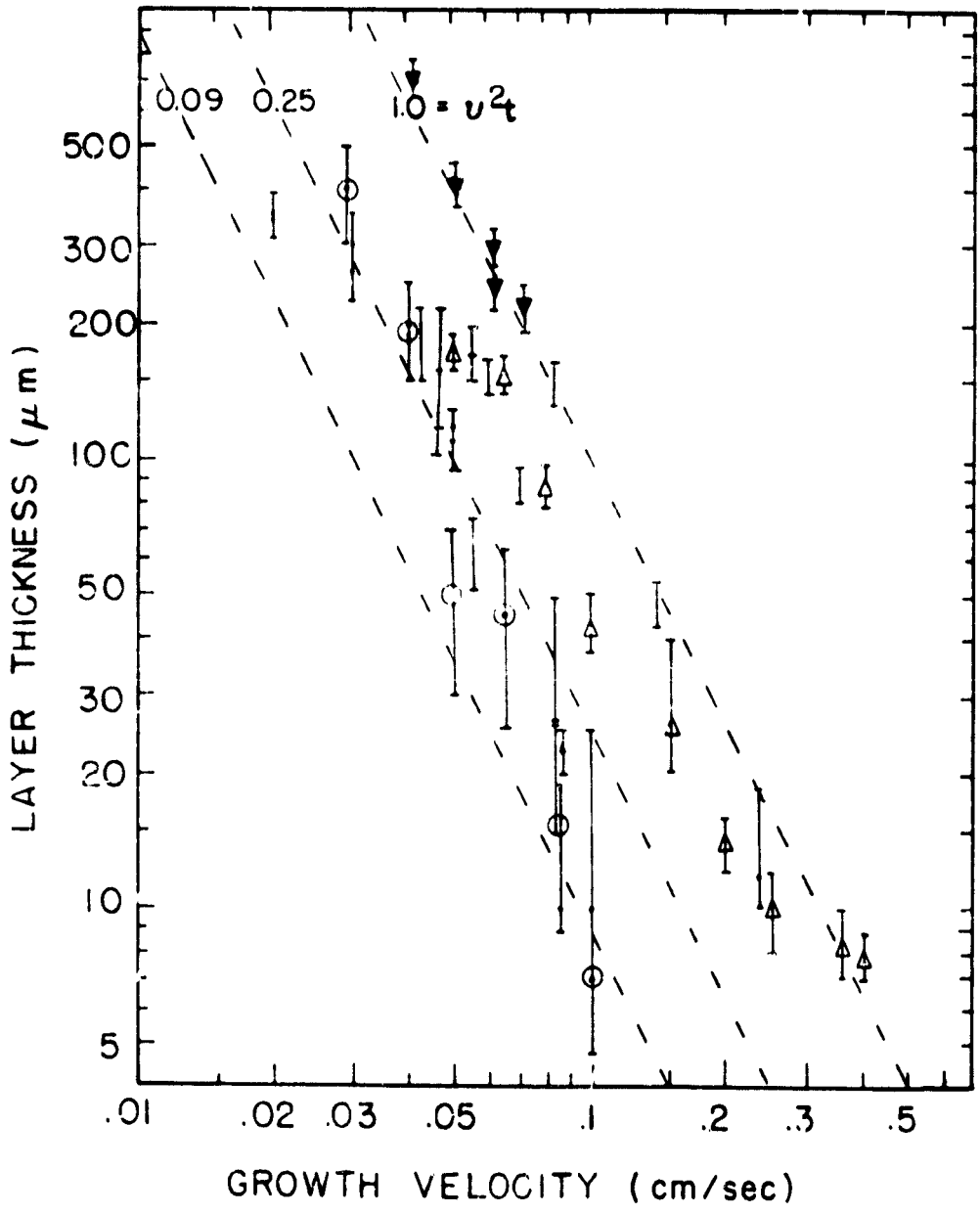


Figure 76. SOC layer thickness, t, as a function of growth speed, v, for a number of dip-coating runs under different conditions. Triangles and circles are used to indicate series of coating runs in which attempts were made to hold the conditions constant.

not decay. The entire range of melt temperatures between dendritic growth to complete disappearance of dendrites is on the order of $3^{o}K$. The center of this range we consider to be the optimum growth temperature at that velocity.

7) If the velocity is increased, the optimum growth temperature, T_{mo}, is increased. Thus, to obtain maximum thickness at a given velocity, the melt temperature must be increased as the velocity is increased to prevent dendrite formation.

8) Width instability has not been observed in SOC growth. This contrasts with the case of EFG where careful design and control are needed to maintain the width.

9) SiC particle formation on the surface of SOC layers has not been observed. At times, proturberances on the surface are observed, but these have always been found to be dendrites, formed under conditions where T_m was just below T_{mo}. Again, this contrasts with the case of EFG ribbon growth, where care must be taken to avoid SiC particle formation.

The above observations, coupled with the results of our thermal analysis of growth, indicate that SOC growth is very similar to EFG, but has some important advantages. The thermal analysis, which applies equally to SOC and other ribbon growth, shows that the v^2t relationship is very general. However, one restriction is that the heat current density (temperature gradient) on the liquid edge of the liquid-solid interface must be negligible compared with vL, the velocity times the latent heat per unit volume.

The condition of nearly zero temperature gradient in the liquid is consistent with the observations listed regarding the optimum melt temperature, T_{mo}. Thus, the analyses and the experimental results lend credibility to each other. In fact, the value of the v^2t product can be calculated quite simply, and agrees with the experimental results.

The theory basically states that the v^2t product is determined completely by the coating function. Thus, we can confidently predict that additional

radiative and convective cooling will enable us to increase the v^2t product by a significant factor.

Slotted Substrate Coverage - To serve as solar cell material, sheet silicon conventionally must have both of its surfaces accessible for electrical contacts. With SOC, contact at the silicon-ceramic interface is only possible via openings in the substrate. Initially, 1mm-diameter hole openings were tried and good silicon coverage was achieved. It was observed, however, that there was considerable perturbation of the layer surface around each hole. A series of long slot openings was then placed in the substrates. In part of these substrates the slots were vertically oriented (parallel to the growth direction), in other substrates the slots were horizontally oriented. As discussed later in this report, in order to minimize series resistance in solar cells made from these layers, it was necessary that these slot openings cover 50% of the coated area.

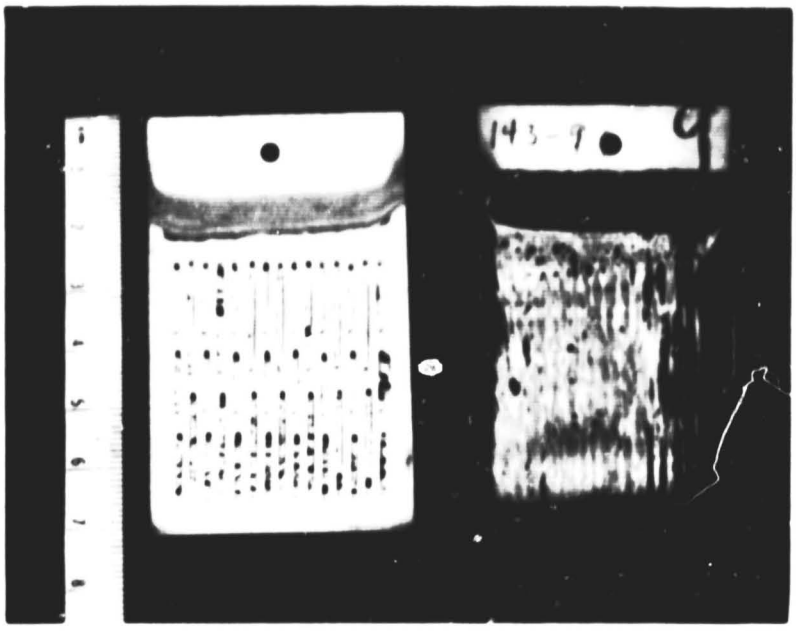
Horizontal slots were found to be more easily bridged by the silicon than the vertical slots. Horizontal and vertical slots that cover 50% of the area were successfully and routinely dip-coated. Figure 77 is a photograph of a vertically slotted substrate in which the slots are over 1mm wide and the ribs are less than 1mm wide. These layers were grown at a speed of 3.6 cm/min. Figure 78 shows a substrate configuration in which the slots were horizontal with the same slot-to-rib ratio. We observed that there is less perturbation of the surface with the horizontal slots, and for this reason this configuration was adopted for the remaining SOC effort.

Back Surface Field Metallization Study - It is generally known that the application of a back surface field (BSF) to the back surface of a solar cell improves its conversion efficiency. With SOC such application is difficult. Nevertheless, it was decided that it may be worthwhile to attempt a BSF application through the slot openings in the substrate.

Different materials were evaluated as back contact materials that would produce the BSF effect when used with the slotted SOC material.

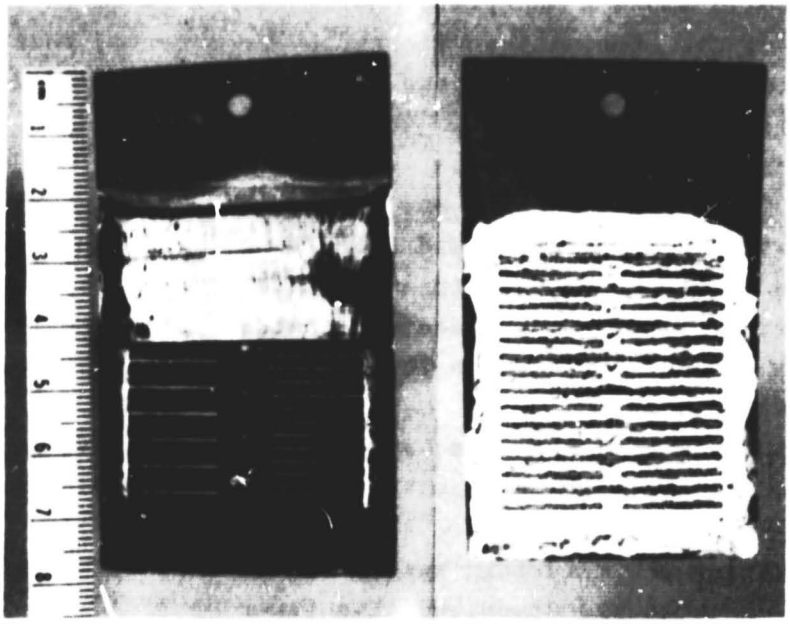
The first of these new materials was an aluminum paste formation. The use of this for BSF contacts was described in a paper by J. A. Thornhill of Spectro Lab.[24] We prepared two paste mixtures which are very similar to the

[24] J. A. Thornhill, "Automated Fabrication of BSF Silicon Solar Cells with Screen-Printed Wraparound Contacts," Spectro Lab, NASA Contract NA53-20029, Final Report, pp. 11-15 (August 1977).



(a) Back surface. (b) Front surface.

Figure 77. Vertically slotted substrate.



(a) Front surface. (b) Back surface.

Figure 78. Horizontally slotted substrate. The back has been coated with solder for a back contact. The lower part of the front surface has been AR coated.

Table 16. Single-crystal diodes with aluminum back contacts.

Wafer No.	Type of Aluminum	Furnace Temp. (°C)	Furnace Time	Max. V_{oc} (V)	Comments
6	Paste	903	60 sec	0.56	Showed shunt and series resistance.
10	Paste	916	40 sec	0.55	Showed shunt and series resistance.
11	Paste	~900	25 sec	0.56	Showed shunt and series resistance.
12	Sputtered	876	30 sec	0.54	Showed shunt and series resistance.
13	Sputtered	825	15 min	0.54	Showed series resistance, but the shunt resistance was much better than observed on the other samples.

Table 17. Slotted SOC diodes with sintered aluminum paste back contacts.

Diode No.	Furnace Temp. (°C)	Furnace Time	V_{oc} (V)	Fill Factor	Comments
1 -13A-2	823	5 min	0.515	0.740	
139-13A-4	823	5 min	0.507	0.744	
139-13A-1	823	5 min	0.321	---	Diode located at the edge of the mullite.
139-13A-3	823	5 min	0.445	---	Crack in the silicon extending toward the diode.

in-house mixture described by Thornhill, one with an average particle size of 9μm and the other an average particle size of 6μm. The second material was also aluminum, but was sputtered on the back surface rather than applied as a paste. Contact resistivity measurements and diodes were made on both paste and sputtered aluminum. The contact resistivity of the fired paste was 0.16 ohm/cm, while the sputtered aluminum was 0.010 ohm/cm. The value for the paste was higher than expected. This may have been due to process conditions.

Diodes were made on both single-crystal and SOC silicon. The results for single-crystal silicon are listed in Table 16 and for the SOC diodes in Table 17. Aluminum samples were sintered in an oxygen/argon atmosphere and all the aluminum paste samples were air-baked at 210 to 250°C for 15 minutes prior to sintering. This paste was made with Reynolds Aluminum 1-131 with an average particle size of 6μm. The improved shunt and series resistance on the SOC diodes in contrast to the shunting effect and high series resistance of the single-crystal diodes may be the result of lower-temperature firing.

The results of this work at this point were inconclusive and it was discontinued due to the loss of personnel involved.

Fast Growth Studies - The SOC economic analysis reveals that a substantial cost advantage is achieved if 100μm-thick layers could be coated at a lineal velocity of 14 cm/min. Theoretical and experimental studies to date had shown that such a coating velocity was not possible with radiative cooling alone. For this reason a second, more versatile dip-coater was constructed to investigate fast growth. To overcome early problems with substrate breakage due to thermal shock upon cooling, an afterheater as shown in Fig. 9 was added to the coater and encouraging progress was made. A series of runs was made with argon gas flowing through the cooling shoes onto unslotted substrates. In all cases, uneven, vertically striped coatings were obtained. The stripes corresponded to the gas openings in the cooling shoes. In some cases the coatings were partially dendritic. The thickest portions of the smooth regions were measured and are shown plotted (as crosses) as a function of growth speed in Fig. 79.

The line drawn on the far left side in Fig. 79 represents a large amount of data taken on dip-coater No. 1 with radiative cooling only. The data follow the relationship $v^{2.9}t = 0.059$. The circles are data taken in

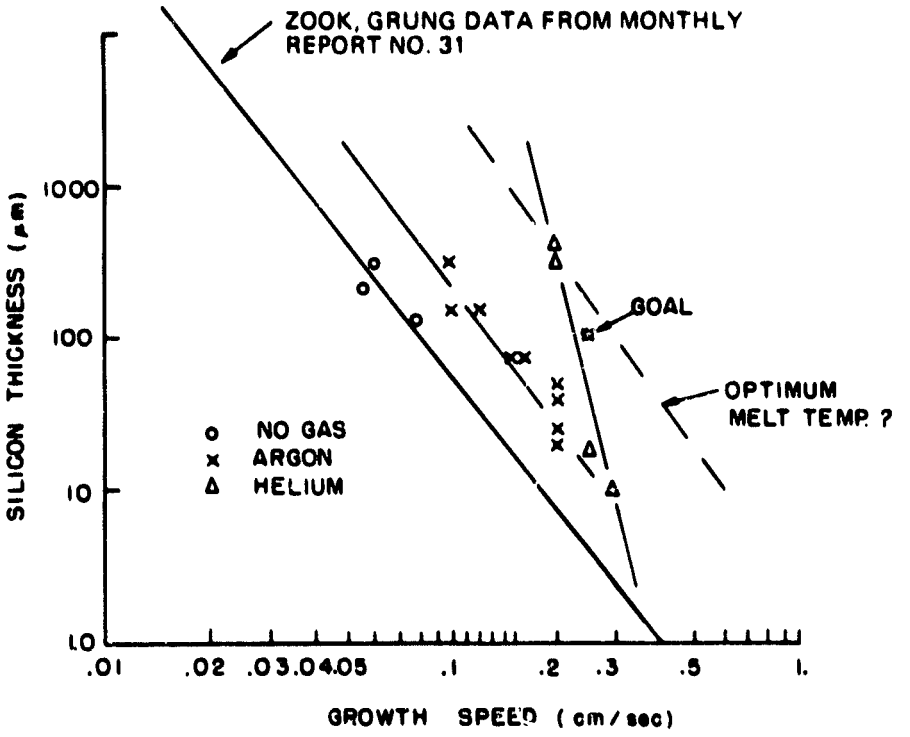
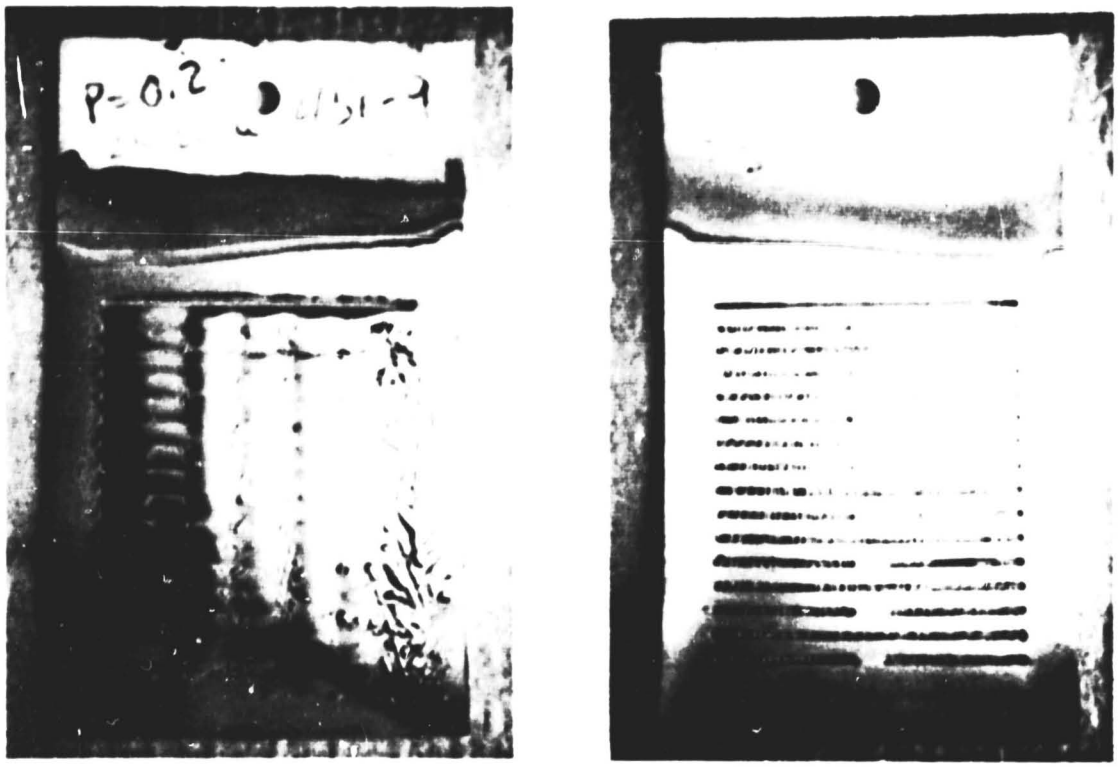


Figure 79. Summary of data obtained with dip-coater No. 2 using an "active" afterheater and helium-gas cooling. The open circles are taken on substrates coated without gas cooling, and the line is a summary of data taken on the other dip coater under the same experimental conditions.

dip-coater No. 2 with radiative cooling only. The agreement between the two coaters is good. The crosses are the data taken with argon flowing through the cooling shoes. The argon data lie on a line roughly parallel to the other and is displaced toward higher v and t. With argon cooling, a smooth coating thickness of 300μm was achieved at a growth speed of 6.0 cm/min, but all coatings produced at 12 cm/min were less than 100μm thick.

A series of runs was then made with helium flowing through the cooling shoes in an effort to get thicker coatings (the thermal conductivity of helium is approximately eight times that of argon). These results are shown as the triangles plotted in Fig. 79. The appearance of the coatings produced under helium was the same as observed previously (i.e., vertical striations corresponding to individual gas jets plus some dendritic

regions). The major difference is that the coatings grown under helium are thicker. Coatings exhibiting smooth regions with thicknesses of 200 and 300μm have been grown at 12 cm/min. An example of a sample with a 200μm-thick coating produced on a slotted substrate at 12 cm/min is shown in Fig. 80. The smooth portion of the coating has thicknesses ranging from 25 to 200μm. Smooth coatings were also grown at 14 and 18 cm/min under helium and the data are plotted in Fig. 79. These data must be considered preliminary because the melt temperatures have not been optimized for the higher-speed growth. As indicated in Fig. 79, a goal of 100μm thick at a growth speed of 14 cm/min appears to be feasible.



(a) Front Side (b) Back Side

Figure 80. Photograph of a slotted substrate coated at 12 cm/min with helium gas directed at (a) the front and (b) the back sides of the substrate. The thicker regions are 200μm thick.

Physical Properties of Dip-Coated Material - When ceramic substrates are carbon coated on one side and then dipped into molten silicon, directional solidification occurs upon withdrawal on the carbon-coated side. With directional solidification, the primary crystallization originates from the liquid-solid interface as opposed to proceeding from the surface of the substrate. Thus, continued nucleation results from previously grown silicon, thereby permitting single crystallites, after a few millimeters of growth, to enlarge in width as well as in length. The films are reasonably uniform over the area and their thickness, as previously mentioned, can be controlled by varying the melt temperature and withdrawal rate. Through the course of this investigation, layer thicknesses from approximately 10μm to 300μm have been grown.

Since the final selection of mullite as a substrate material was made on the basis of thermal expansion coefficient and thermal shock, little, if any, cracking occurs in the substrates or silicon layers.

The crystallographic texture of these SOC layers was determined by x-ray diffraction. The structure[25] is quite similar to that of ribbon.[13,26] The predominant structure is heavily twinned with {111} twin planes perpendicular to the surface and parallel to the <211> growth direction; the surfaces are close to the {110} planes. A photomicrograph of an etched surface of an SOC sample showing twin boundaries is shown in Fig. 81. Note that some areas between twin boundaries are populated with dislocations and others are not. The grains are heavily twinned and the dislocation densities are high, 6×10^6 to 8×10^6 cm^{-2}. According to some theories,[27] the twinned structure is necessary to permit rapid growth.

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[25] J. D. Zook, R. B. Maciolek and J. D. Heaps, "Silicon-on-Ceramic for Low-Cost Solar Cells," IEDM Tech. Digest, IEEE Press (1977), p. 218.

[26] L. C. Garone, C. V. Hari Rao, A. D. Morrison, T. Surek and K. V. Ravi, "Orientation Dependence of Defect Structure in EFG Silicon Ribbons," Appl. Phys. Lett. 29 511 (1976).

[27] M. H. Leipold and R. J. DeAngelis, Proc. of Photovoltaic Solar Energy Conf., Luxembourg, (1977) p. 872.

Figure 81. Photomicrograph of an etched surface of an SOC sample showing twin boundaries and dislocation distribution.

A photomicrograph of a metallographic cross section taken perpendicular to the growth direction is shown in Fig. 82. The twin boundary and dislocation distributions coincide with that observed on the surface. Note that the layer is only one crystal thick and that there is a contiguous interface between the silicon and the mullite substrate.

In the seeded growth experiments, where single-crystal and EFG ribbon material were used to enhance grain growth, it was determined that at the accelerated growth rates of interest in this investigation, seed orientation was a critical factor. Successful seeding was achieved only with seeds having the same orientation as the texture of the rapidly grown films, i.e., {110} <211>. A photograph of an SOC film grown at 2.4 cm/min and seeded using single-crystal silicon ribbon material {110}<211> is shown in Fig. 75. The surface was etched to reveal how the structure of the seed extends into the SOC layer. The use of other seed orientations resulted in the growth being influenced for only a few millimeters before the interface became unstable and nucleation took place, with growth proceeding as if it had not been seeded, i.e., {110} <211>.

millimeters before the interface became unstable and nucleation took place, with growth proceeding as if it has not been seeded, i.e., {110} <211>.

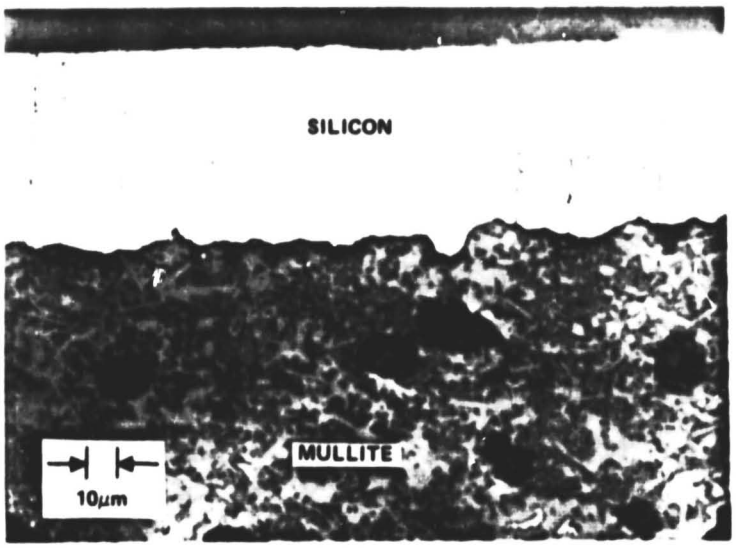


Figure 82. Photomicrograph of a metallographic cross section of an SOC sample taken perpendicular to the growth direction. Note that the layer is only one crystal thick and that a continuous interface exists between the silicon and ceramic.

Electrical Properties of Dip-Coating Material - Early in the program, the silicon melt was doped with boron to a level of 5.65×10^{15} atoms cm^{-3}, corresponding to a resistivity of 2.5 ohms-cm based on a single-crystal mobility. Invariably, however, dip-coated layers ended up with resistivities much lower than 2.5 ohms-cm. It was suspected that the molten silicon was dissolving the mullite substrate, thereby freeing aluminum atoms to contribute to the p-type doping level.

The primary means for determining impurity doping levels was using a four-point resistivity probe. The four-point probe technique gives an accurate measure of resistivity if the thickness of the layer is known, but the carrier concentration is obtained by assuming that the mobility in the polycrystalline layers is the same as in single-crystal silicon. This assumption, in general, is not valid; therefore, three Hall samples were prepared from two dip-coated substrates (MR-1 and MR-7). Of the three samples

prepared from dip-coated layers, two were prepared from substrate MR-7 which had the melt surface solidify around it. This required it to soak in the melt for 9 minutes before remelting was accomplished and temperature equilibrium could be established. In a sense, the samples prepared from MR-7 thus represent a worst-case example as far as time allowed for the substrate to contaminate the silicon coating. The remaining substrate was prepared from MR-1, which represents a more typical time in which the substrate is in contact with the molten silicon.

Measurements were made on these three dipped layers to determine if the resistivity measurements could be used to determine the carrier concentration.

Hall samples were prepared by masking the sample configuration and sandblasting the remaining silicon from the substrate. The samples were about 1cm long and 1 to 2mm wide, with the voltage legs about 5mm apart. Contacts were made by evaporating aluminum and alloying at 750°C for 10 minutes. Electroless nickel was plated over the alloyed aluminum and indium soldered to the nickel. The measurements were made in a standard manner using a d-c field to 2 kilogauss.

The room temperature measurements are summarized in Table 18. The sample designations MR-7-P and MR-7-X refer to the crystalline orientation in the Hall sample, with "P" meaning the long axis of the grains were parallel to the direction of current, and "X" meaning the long axis of the grains were oriented across the sample, perpendicular to the direction of current. As

Table 18. Summary of 300K electrical properties.

Sample No.	Carrier Conc. (cm^{-3})	Resistivity (ohm-cm)	Mobility (cm^2/V sec)
MR-7-P	6.7×10^{16}	0.45	208
MR-7-X	7×10^{16}	0.6	146
MR-1	7.5×10^{16}	0.54	153
Bulk Poly (Melt-8)	1.8×10^{17}	0.24	146

seen in Table 18, these two samples have slightly different mobilities, with the highest mobility being in sample MR-7-P. The mobilities in all three samples are lower than the 250 to 300 cm^2/V-sec expected for single-crystal material with carrier concentrations in the 0.6 to 2 x $10^{17}/cm^3$ range.

The temperature dependencies of carrier concentration, resistivity, and mobility for sample MR-7-X are shown in Figs. 83 and 84. In general, they behave as expected for silicon: the carrier concentration decreases and the resistivity goes through a minimum before increasing as the sample is cooled. The one exception occurs at 77K where the carrier concentration apparently increases over the 85K value. The temperature dependence of the mobility is compared with a single-crystal sample with a carrier concentration of 2 x $10^{17}/cm^3$ in Fig. 84. The notable difference is the sudden drop in mobility in the layers at 77K. No explanation for this decrease is postulated at this time.

The main point to note from these measurements is that the mobility in polycrystalline samples will be lower than in a single-crystal sample with the same doping density. As a result, the resistivity measurements will indicate a higher purity by as much as a factor of 2.

To investigate the source of this excess p-type conductivity in melt 8, a thin wafer was prepared from this melt and an infrared transmission measurement made at a temperature of 10K using an FTS-14 Fourier Transform Spectrometer. The absorption coefficient is shown in Fig. 85 as a function of photon energy in cm^{-1} $\lambda(\mu m) = 1 \times 10^4/K(cm^{-1})$. The prominent absorption lines are labelled according to the standard nomenclature for acceptors in silicon. At the lower energies, three lines due to boron are clearly seen and are labelled 1 through 3. At the higher energies, a number of lines characteristic of aluminum are seen, labelled X1, X3, 1, 2, and 4. The most prominent aluminum line (line 2) is totally absorbing in this particular sample because of the relatively thick sample used at this high carrier concentration.

An estimate of the impurity concentrations of both boron and aluminum can be made from the intensity of the absorption peaks. These are (4 ± 1) x $10^{15}/cm^3$ for the boron and (8 ± 4) x $10^{16}/cm^3$ for the aluminum. The aluminum concentration is more uncertain than our estimate of the boron concentrations, since we did not run a standard with aluminum doping. We had to

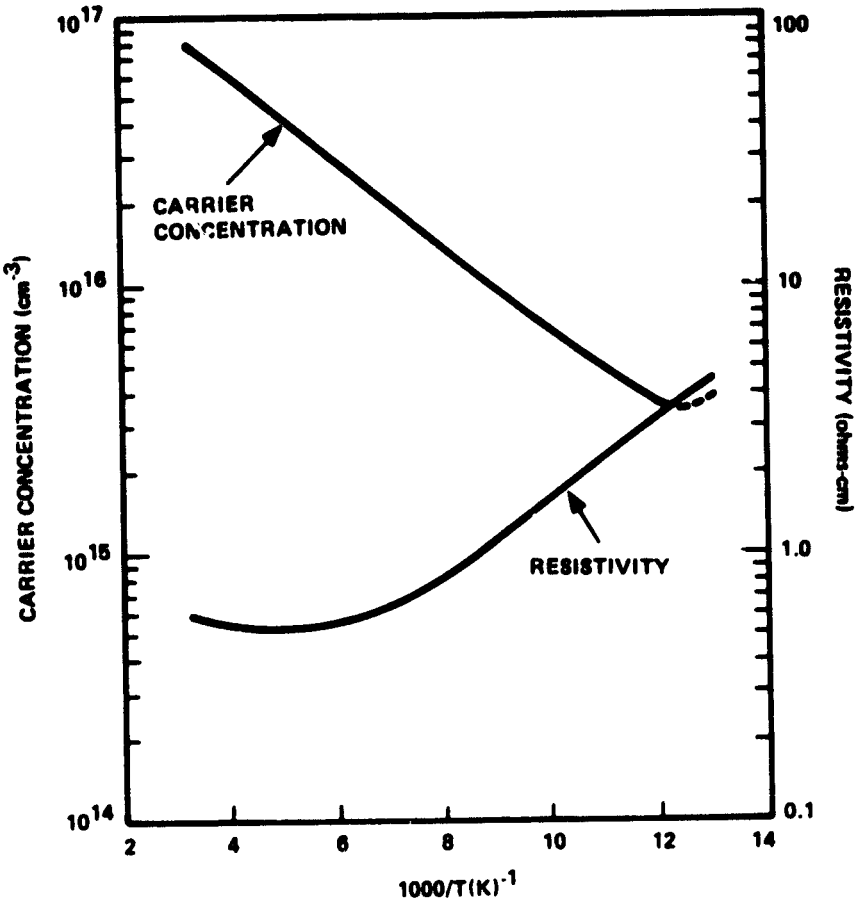


Figure 83. Carrier concentration and resistivity vs. 1000/T (deg K)$^{-1}$ for sample MR-7-X.

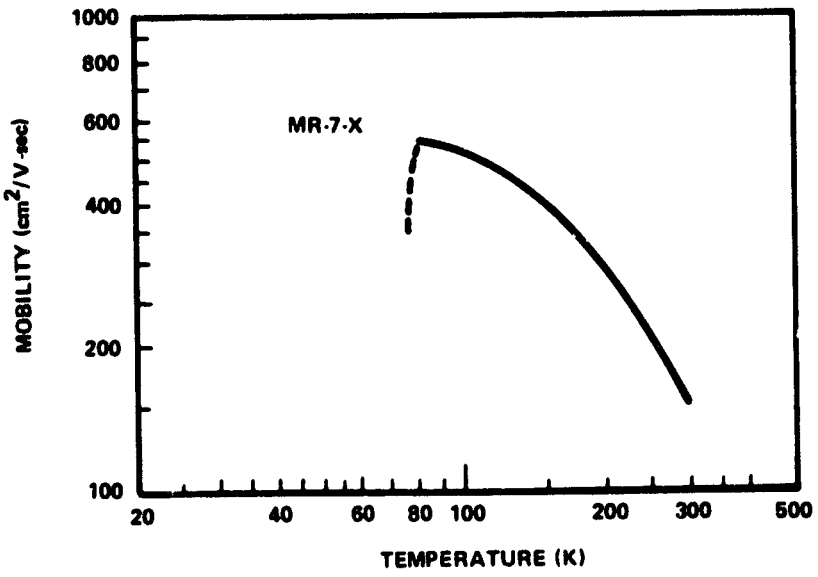


Figure 84. Mobility vs. temperature (K) for sample MR-7-X.

rely on aluminum spectra which have appeared in the literature. The boron concentration in the sample is approximately the amount loaded in the melt, but less than the aluminum.

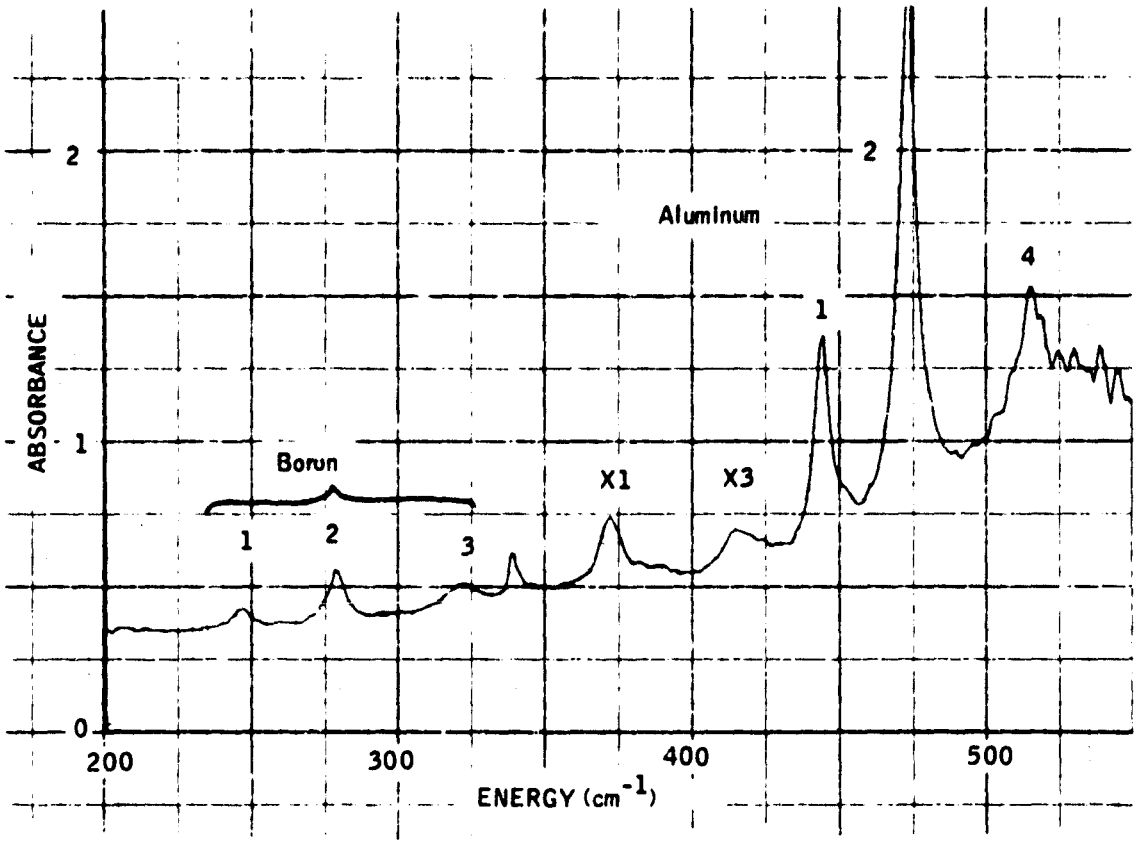


Figure 85. Absorbance spectrum of a polycrystalline silicon sample.

The first and most obvious conclusion to be made from the above measurement is that mullite was, in fact, being dissolved by the molten silicon. This was probably true, but it would have been a mistake not to consider the possibility of some coincidental source caused by uncleanness in the substrate processing technique or the impurities in the carbon coating. Tylan Corporation of Torrance, California, was then requisitioned to coat all surfaces of several mullite substrates with their reportedly impervious glassy carbon coating. Discussions with Tylan were encouraging. Based on their experience with coating impure graphite crucibles, they felt that a Tylan coating would remain intact and that molten silicon would wet it.

The thermal expansion coefficient of mullite was compatible with Tylan's coating and the scale-up cost of the coating process should be modest.

Upon receipt of the "Vitregraph" coated substrates, the extent to which the mullite dissolution could be inhibited was investigated.

The investigative experiments are summarized in Fig. 86, which gives resistivity as a function of time in the melt. Samples were prepared from the tops of solidified melts and resistivity measurements were made, where possible, within single grains of silicon. The top of the solidified melt was selected to be representative of the solidification rates involved in actual dip-coated layers of silicon and thus should more accurately simulate the effects of impurity segregation.

An undoped silicon charge was melted and a 125μm-thick silicon layer was dip-coated on a mullite substrate (MR-45). Following this, an uncarbonized substrate was dipped and soaked in the melt for a period of 63 minutes. This soaking procedure was intended to contaminate the melt. Following this, a third substrate (MR-47) was then also dip-coated with a 125μm-thick layer for the purpose of comparing its resistivity with that of layer MR-45. The respective resistivity levels of these two layers along with that of the melt are shown in Fig. 86. The above experiment with a new silicon charge was repeated with substrates which were fully coated with graphite on all sides and edges. The first dipped substrate (MR-48) was in the melt for 22 minutes. As shown in Fig. 86, the rubbed-on graphite coating neither helps nor hinders the final impurity level of the melt.

Using another undoped silicon charge, five mullite substrates (MR-101 through MR-105) were progressively dip-coated with silicon layers using identical growth conditions. Their respective resistivities, as the melt became progressively contaminated, are also shown in Fig. 86.

Fig. 86 shows that the aluminum impurity level of the melt increases rapidly during the first 2 or 3 minutes of contact time with the substrate, and then increases at a lesser rate, becoming very nearly saturated after an hour of contact time.

The initial rate of dissolution would be proportioned to the amount of exposed surface area, with the rate decreasing as the solution approached saturation.

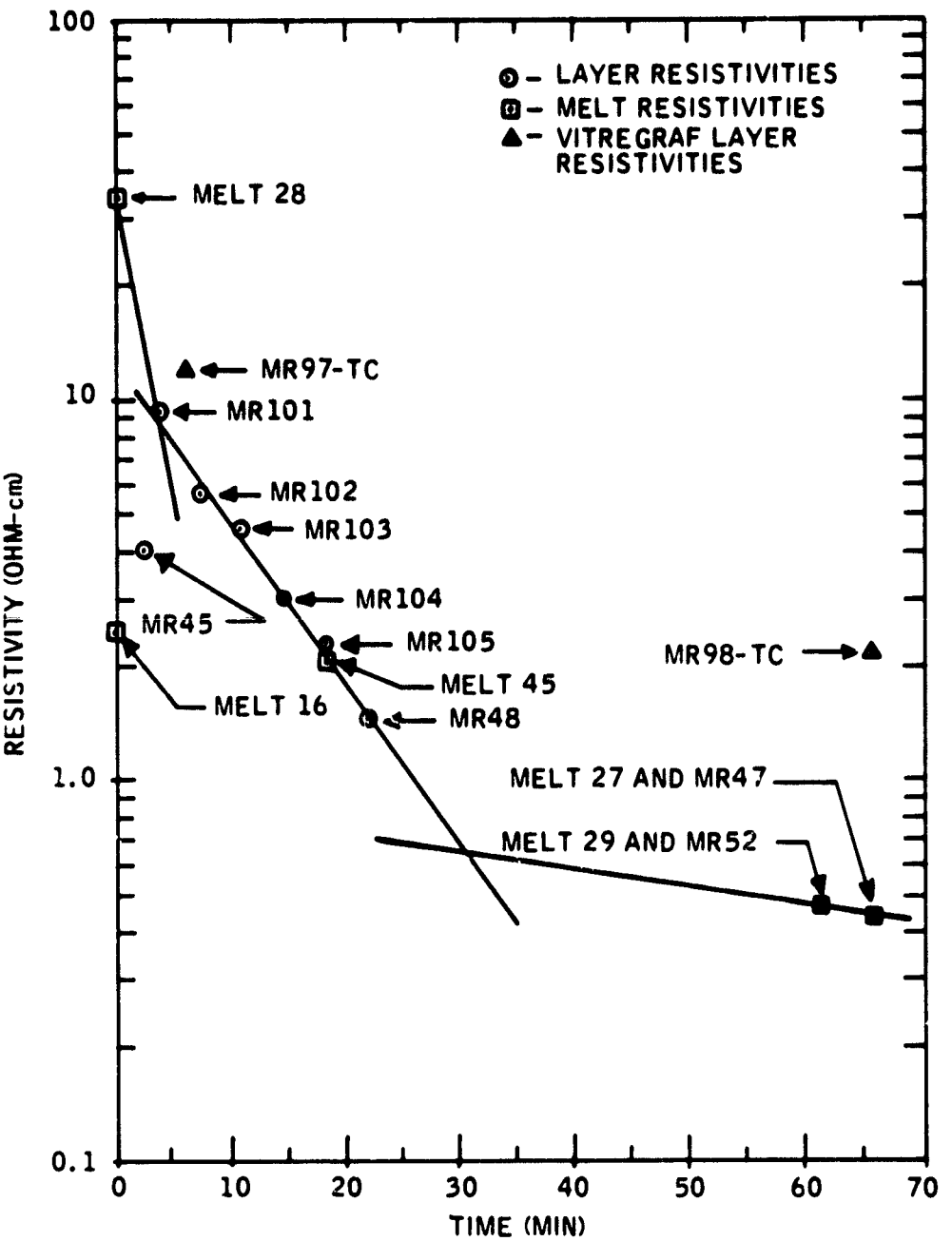


Figure 86. Layer and melt resistivities vs. accumulated time that the undoped melts were exposed to mullite.

The effective surface area of the mullite depends on the surface roughness and on the degree of wetting of the substrate. The saturation solubility of the aluminum is determined by the amount of oxygen in the melt. Because of the quartz crucible, the silicon is saturated with oxygen, limiting the amount of dissolved aluminum to a concentration well below the solubility limit of aluminum itself. Since several chemical reactions are involved, the detailed kinetics are undoubtedly not simple, as indicated by the several slopes in different regions of Fig. 86.

Figure 86 also shows the effect of the vitreous carbon ("Vitregraph") in inhibiting the mullite dissolution rate in molten silicon. Vitreous carbon-coated substrates MR-97-TC and MR-98-TC were successively dip-coated in an undoped silicon melt. Substrate MR-98-TC was allowed to soak in the melt for 1 hour before it was removed with a smooth, uniform silicon layer. MR-97-TC and MR-98-TC layer resistivities are also plotted in Fig. 86 for the purpose of comparing them with the more generally used rubbed-on, graphite-coated substrate silicon layers.

Sectioning of layer MR-78-TC caused portions of the vitreous carbon silicon layer to separate from the substrate. This made it possible to measure the sheet resistance of the silicon layer as well as that of the attached vitreous carbon coating. Since the sheet resistance of the silicon layer was approximately 20 times that of the vitreous carbon, it is evident that some type of conductivity barrier exists between the two. The sheet resistance of vitreous carbon on the uncoated portion of the dip-coated layer was very similar to that attached to the silicon layer, giving further evidence that little, if any, of the vitreous carbon coating was dissolved by the molten silicon after soaking in it for a period of 1 hour.

Evaluation of SOC Material Using LBIC - During the course of this program, a technique was developed to evaluate in detail the various contributions to the short-circuit current of SOC solar cells. This technique, called LBIC (light-beam-induced current) technique, resembles other light-beam scanning techniques but differs somewhat in the details. The technique and results have been described in various SOC Quarterly and Annual Reports and in several publications. Therefore, the purpose of this subsection is only to summarize the highlights. A more complete description is given in Appendix A, which is based on a 1980 Photovoltaic Solar Energy Conference at

Cannes, France. Summaries of LBIC results also were given in SOC Annual Reports Nos. 2, 4, and 5. The basic features of the LBIC experimental technique used at Honeywell are as follows:

- A high-pressure xenon arc lamp is used as a source. It provides peaks at convenient wavelengths in the infrared with a focused spot intensity of about 1 sun.

- The focused spot can be a few micrometers in size, typically 5 x 11μm, measured on the sample.

- The absolute quantum efficiency, Q, is obtained from the ratio of the LBIC current in the sample to the LBIC current in a calibrated, highly uniform silicon photodiode inserted in place of the sample.

- The minority carrier diffusion length, L, is obtained from the absolute quantum efficiency, Q, by solving

$$Q_\lambda = \frac{(1 - R)\,\alpha\lambda L}{1 + \alpha_\lambda L} \qquad (60)$$

  where α is the absorption coefficient at wavelength λ.

- By averaging the values of L obtained for six different wavelengths, an average value of L is obtained. The value of (1 - R) can be selected to minimize the mean square deviation, $\Delta L/L$.

- At the longest wavelengths (approximately 1.0μm), the values of αL tend to be much less than unity, so that the LBIC scan gives a mapping of an effective diffusion length as a function of position, as seen by the above equation.

- LBIC can also be used to evaluate material before processing, by using an electrolyte technique. The signal-to-noise ratio is not as good as in the d-c case, however, since chopped light must be used.

The theory of LBIC response has also been developed, assuming that an effective recombination velocity parameter, S, can be used to describe grain boundary recombination. The analytical results were published in Appl. Phys. Lett. 37, 223 (1980), as well as in SOC Annual Reports Nos. 4 and 5. Some comparisons with the theory are given in Appendix A, as well as in these Annual Reports.

The experimental results of LBIC measurements on a number of SOC samples can be summarized as follows:

- There usually is a characteristic maximum diffusion length, L_{max}. This is evident from the good LBIC response at 0.98μm, and generally occurs in the largest visible grains (greater than 400μm wide). Cross sections of samples at lines where the LBIC scan is known show that the best diffusion lengths occur in grains having high densities of twin boundaries and few dislocations.

- There usually is a characteristic minimum diffusion length, L_{min}, characteristic of the most active grain boundaries. Surprisingly, the depth of the minimum LBIC response at 0.98μm does not depend strongly on the spot size or on obtaining exact focus of the light beam. The minima of the LBIC response tend to be constant, even if the substrate is bowed, so that part of the scan is out of focus. Varying the spot size from 5 to 15μm does not significantly affect the value of the minima. Thus, a "minimum diffusion length" is a fairly well-defined experimental quality for a given SOC cell.

- Different large grains within the same sample may have different diffusion lengths. Even adjacent grains may have values of L differing by 25%.

- SOC material appears to consist of large-grain regions and small-grain regions. The small-grain regions may have a significantly smaller diffusion length than the large-grain regions, especially in processed cells. An example is shown by the LBIC scan in Fig. 87.

- An average diffusion length, L, can be obtained from a single LBIC line scan by electronically integrating and averaging the LBIC signal during a scan.

- The values of L_{max}, L_{min}, and L were found to depend significantly on the boron doping in the sample, with a strong decrease in L value with doping, at least using the "fast cool" processing sequence. The results are shown in Fig. 88.

- The value of L is also found to be a function of processing. Using the electrolyte technique before cell processing and comparing the results with the p-n junction results after thermal diffusion using

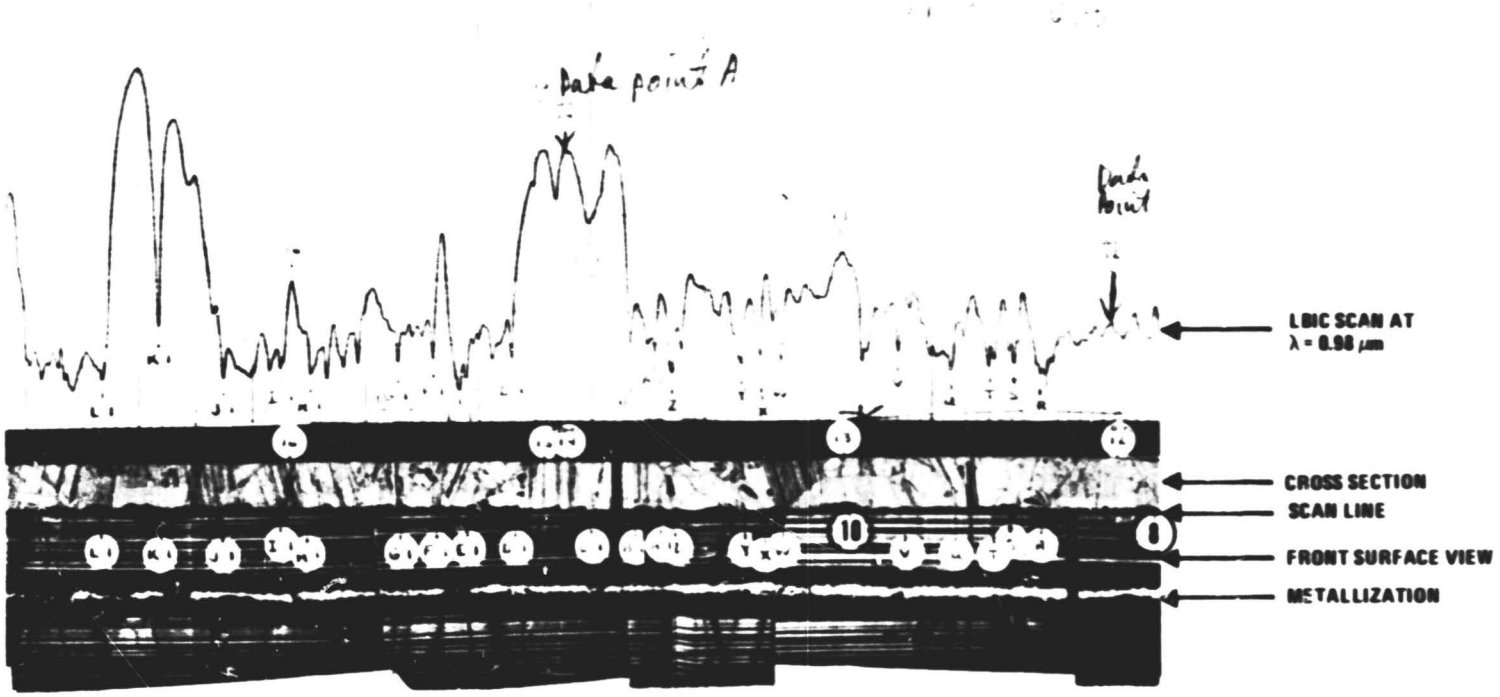


Figure 87. Correlation of LBIC scan with structure. A solar cell was scanned and then cross-sectioned through the scan line. The LBIC scan (upper trace) is at the same magnification as the cross-section (middle photo) and the front surface view (bottom photo). The letters, such as L1 and V, correspond to minima in the trace. The numbers correspond to maxima. The distance between the 10.0 and 8.0 markers is 2.0mm. In the cross-sectional view, the ceramic is on top and the top surface below it is rougher because of inevitable chipping during polishing.

a phosphane gas source the value of L seems to be increased by the diffusion. It is further increased by the "slow cool" post-diffusion, as shown in Fig. 88.* The response within grains as well as the response at grain boundaries is improved.

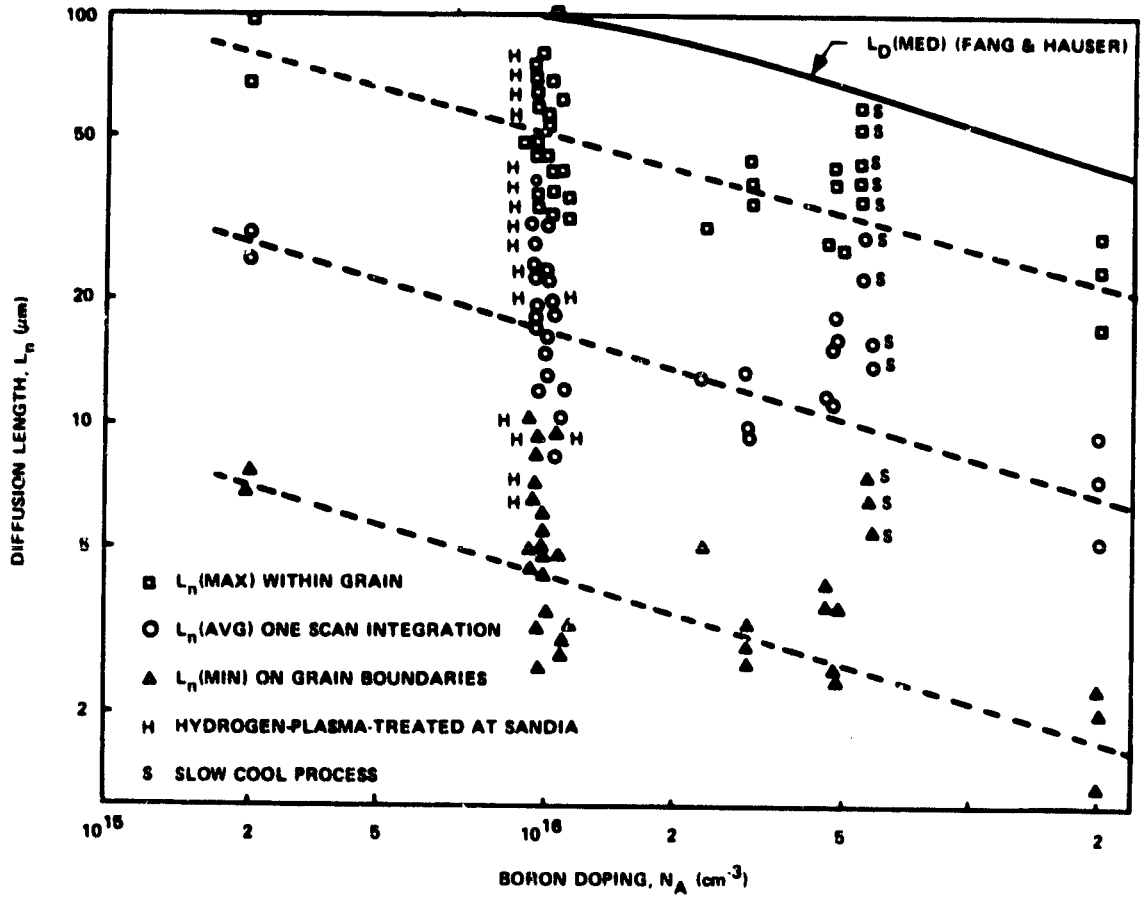


Figure 88. Diffusion length as a function of doping and cell processing.

- Hydrogen passivation performed at Sandia Labs is effective in reducing grain boundary recombination. The details are given in Appendix A.
- The effective diffusion length, or minority-carrier lifetime, is not a function of intensity, either within grains or at grain boundaries. The experiment is described in SOC Annual Report No. 5. Nevertheless, there are some discrepancies in the values of L measured on two

*Slow cooldown, following the phorphorus diffusion, is discussed in the Solar Cell Effort portion of this report.

different systems. The second system illuminates the whole cell, but with much lower intensity. The latter technique gives somewhat higher values (50% higher) of L than the average scan LBIC technique. The discrepancy remains to be resolved.

- There are some grains in which the value of L is almost as low as at the grain boundaries. These regions are largely responsible for lowering the average value of L below the value in the good grains. By correlating a metallographic section with the LBIC scan shown in Fig. 87, these regions can be seen to be high densities of dislocations. Thus, the cause of low L appears to be structural rather than chemical. The largest values of L occur in large grains that are heavily twinned and have few dislocations.

In summary, the LBIC technique has been found to be quite useful in evaluating minority-carrier lifetime effects in SOC material. It is found that the present limitations in efficiency are due to both grain boundaries and defects within grains. The indications are that structural defects (grain boundaries and dislocations) are more important in limiting the present performance of SOC cells than are chemical defects within grains. On this basis we expect that SCIM-coated material with large, heavily twinned grains will produce improved efficiency. Hydrogen passivation, by reducing the electrical activity of grain boundaries and dislocations, appears to be another way to improve efficiency.

SCIM-Coating Results

Introduction - The first problem encountered when SCIM-I became operational was related to substrate breakage. As detailed in the Sheet Silicon Coating Facilities subsection of this report, this problem was corrected by adding appropriate pre- and post-substrate heaters and adjusting the system to achieve a proper longitudinal temperature profile and an adequate transverse temperature gradient along the entire substrate path.

A second and more time-consuming problem at the outset of SCIM-coating was solving a meniscus instability problem which turned out to be related to horizontal coating. This problem is illustrated in Fig. 89. As the substrate passed over the trough, molten silicon wet the substrate and was drawn downstream of the trough before solidification occurred (see t_1). As the substrate continued its motion, this molten layer of silicon thickened (see t_2 through t_6) until it eventually spilled over and annihilated the trough heating element located below.

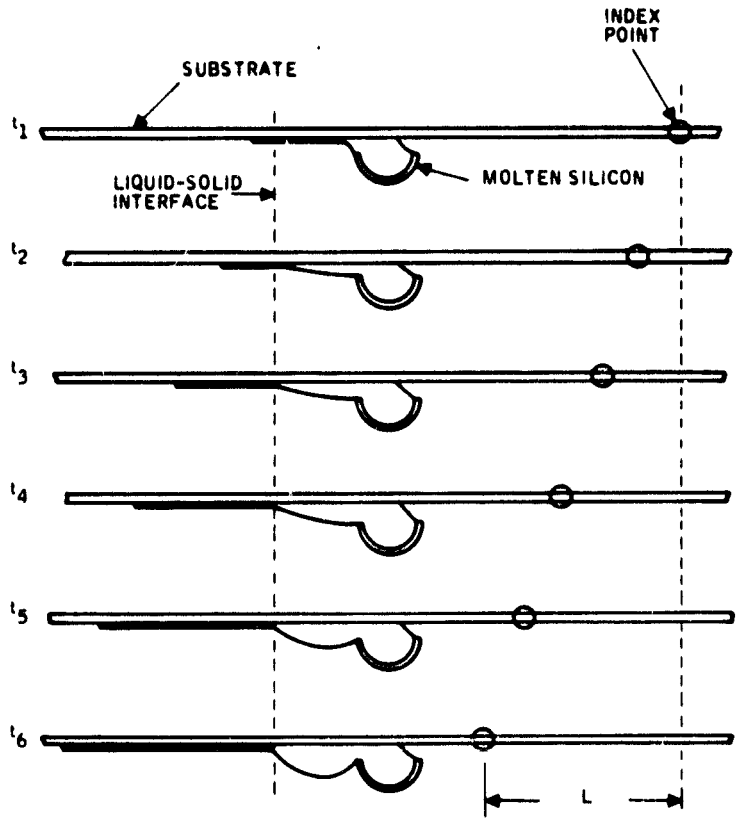


Figure 89. Illustration of molten spillover problem in relation to coating length.

For the most part, the solution of this problem resulted from a Honeywell-sponsored effort along with support from SERI Contract No. XS-9-8119-1 and was reported in the January, 1981, Final Report to SERI.[28] The solution was relatively simple. Meniscus stability was attained by tilting the coater to an angle greater than 10^{o}. Additional modeling was done on growth stability and is discussed later in this subsection.

The design of pre- and post-substrate heaters in SCIM-II borrows heavily on that which was finally successfully used in SCIM-I. The pre- and postheaters in SCIM-II proved to be adequate for fast (greater than 10-cm/min) coating

[28] J. D. Heaps, S. B. Schuldt, B. L. Grung and J. D. Zook, "Supported Growth of Polycrystalline Silicon Sheet on Low-Cost Ceramic, Carbon, or Reusable Substrates," Final Report, SERI Contract XS-9-8119-1 (January 1981).

speeds. The thermal design analysis played an important role in achieving the proper longitudinal profiles needed to prevent substrate warpage and breakage. The actual modifications made to improve this profile are described in the Sheet Silicon Coating Facilities subsection.

SCIM-Coated Silicon Layers - One of the better SCIM-coated layers to come out of SCIM-I is shown in relation to dip-coated samples in Fig. 90. The coating was made on an unslotted mullite (K-modification) substrate which was 5cm wide by 55cm long and 0.1cm thick. The layer, as with dip-coated layers, was relatively smooth and shiny, with very long columnar grains up to 5mm in width. The layer was grown at a coating angle of 20° and a coating rate of 3.6 cm/min. Its nominal thickness was 100μm.

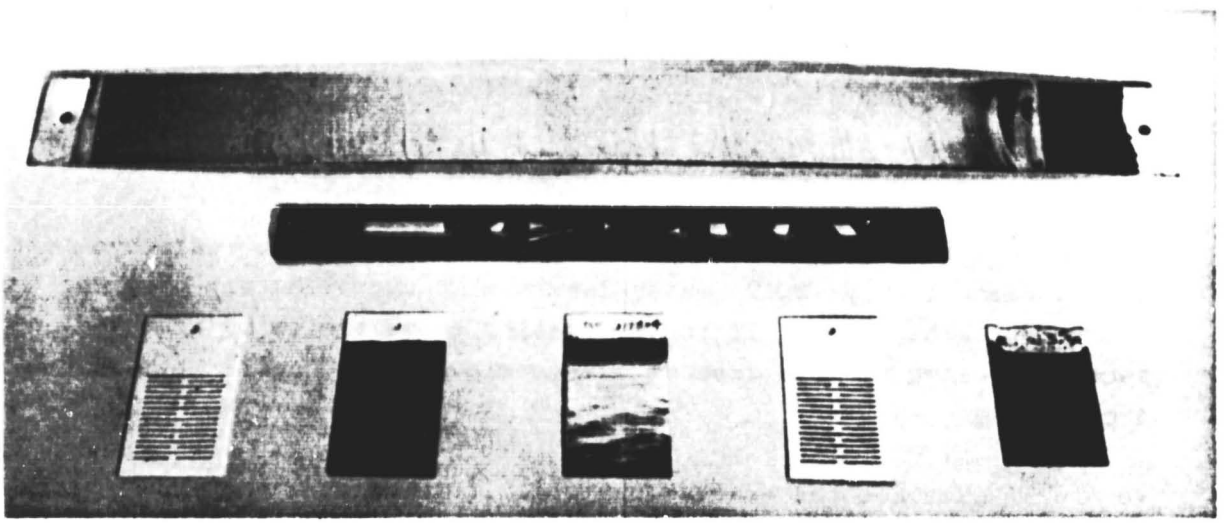


Figure 90. Photograph of SOC sheet silicon showing dip-coated and SCIM-coated substrates.

Later in the program, larger layers were coated onto 10cm x 100cm slotted substrates using SCIM-II. A photograph of one of these coated substrates is shown in Fig. 91. This layer was also grown at a coating angle of 20° but at a lower coating rate of 3 cm/min and its nominal thickness was greater, being approximately 150μm.

SCIM-coated layers, in general, have better developed columnar single-crystal grains which are somewhat wider and significantly longer than

dip-coated layers. This is understandable, since the shorter length of dip-coated substrates terminates the development of many grains which probably would have otherwise been similar to SCIM-coatings.

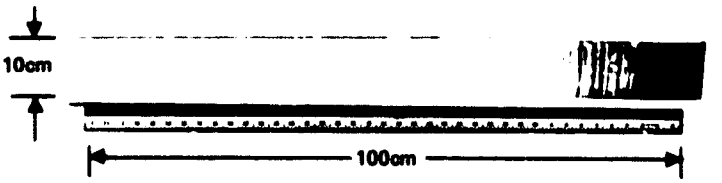


Figure 91. Photograph of a 10cm x 100cm SCIM-coated SOC layer.

SCIM-Coating Growth Parameters - As in dip-coating with radiative heat of fusion removal only, SCIM-coated layers also approximately obey the constant v^2t relationship. Thus, if faster coating rates are to be achieved, convective cooling or some form of asymmetric cooling[28] will have to be implemented.

Figure 92 sketches the coating menisci. It shows that the trough mensicus, as well as the inverted meniscus, is controlled by the displacer. The inverted meniscus is also affected by tilt angle, trough meniscus, and the thermal conditions which position the liquid-solid interface (LSI).

When the tilt angle is 20° and the trough meniscus is horizontal, the inverted meniscus comes up from the trough with its center of curvature on the exit tunnel side of the trough and the LSI is above point A in Fig. 92.

At this same tilt angle, when the trough meniscus is pushed up above the trough, the inverted meniscus goes through a flip-flop condition and becomes S-shaped. The lower portion of the S hangs out over the outside of the trough and threatens to spill onto the heater. Under these threatening conditions the LSI moves out 1 to 2mm so that it is above point B in

Fig. 92. This condition of instability of the inverted meniscus is in a very narrow range of trough meniscus height, whereas the stable (concave) inverted meniscus does not apparently change over a wide range of trough meniscus positions. Menisci observed within the SCIM coater at 10, 15, and 20° tilt angles are in good agreement with the calculated shapes to be discussed.

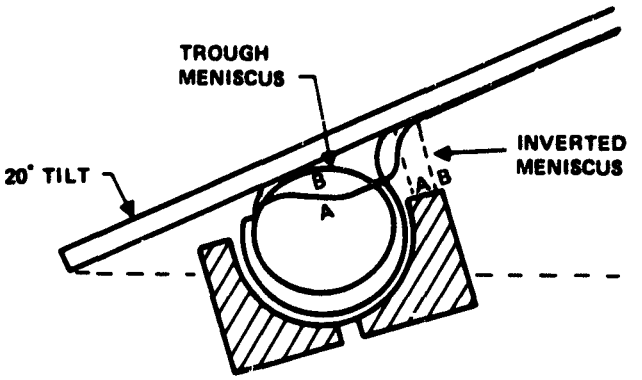


Figure 92. Meniscus shape during coating. The trough meniscus produces a liquid-solid interface at the lettered position. The LSI at "A" and "B" is <2mm apart. "B" can grow layers 100μm thicker than "A" but the inverted meniscus at "B" is unstable at 20° tilt.

A coating problem which has been consistently experienced with the SCIM-II coater is related to a dendritic growth which occurs near the center of the substrate and continues longitudinally along the substrate. The cause of this dendritic growth is not understood, but when an argon gas flow is blown on the inverted meniscus, the dendrite disappears. Figure 93 is a photograph of a 10cm x 100cm silicon coating where argon was periodically administered to the menisci. As can be readily observed, whenever the gas flow was shut off, the dendritic growth reappeared. This dendritic growth was not, however, characteristic of layers coated in the SCIM-I coater. In consideration of this fact, existing differences in the two coaters were reviewed and found to be the following:

1) The superior continuous coating features of SCIM-II cause it to be less gas-tight than SCIM-I.

Figure 93. Silicon coating where argon gas is periodically administered to the meniscus.

2) The trough in SCIM-I remains horizontal irrespective of the coating angle used. SCIM-II initially was designed with a horizontal trough, but was later tilted 10^{o} toward the path of the substrate to enhance meniscus stability.

3) The trough heater in SCIM-I is powered by a filtered (low-ripple) d-c power supply. The supply powering the SCIM-II trough heater, on the other hand, is merely SCR pulsed d-c and, because of large field variations, it imparts mechanical vibrations to the silicon melt.

4) In SCIM-I the substrate preheater extends farther downstream over the trough than is the case in the SCIM-II coater. Here again, SCIM-II was initially constructed similarly, but was later modified in pursuit of a more optimum longitudinal thermal profile.

SCIM-II was made more gas-tight by adding gas jets to entrance and exit gates through which the substrates pass. This modification makes it difficult for air to enter the coater against the outward flow of these jets. Our concern with excess oxygen entering the coater is based on our belief that it generates carbon monoxide which interacts with the melt to produce dendrites because of constitution supercooling. The addition of these gas jets did not, however, improve growth conditions responsible for this dendritic growth.

The orientation of the trough with respect to the coating angle was then altered, but dendritic growth continued. Lastly, near the end of the program, the substrate heater was again extended further downstream. In the runs that followed, considerable improvement in coating uniformity was experienced.

On the basis of a few runs only, it would appear that the longitudinal location of the substrate preheater is at least one of the sensitive parameters contributing to dendritic growth.

Growth Stability - During the course of this work we have learned much about the conditions for stability in supported growth. The reasons for stability in the dip-coating process are discussed in publication titled "Supported Growth of Sheet Silicon from the Melt."[19] The early success of the project was due to the high stability of the meniscus during dip-coating. Because the liquid-solid contact angle is essentially the same for all (non-dendritic) growth conditions, the height of the meniscus is constant. In SCIM-coating, the situation is more complex.

The purpose of this subsection is to present some calculated meniscus shapes that agree quite well with the experimental observations, and to give theoretical arguments that provide a basis for selecting the coating angle of 20^{o} as a preferred condition for SCIM-coating.

The basic SCIM-coating configuration currently used is shown in Fig. 94. In this figure the substrate is inclined at 20^{o} and the substrate thickness, trough size, and meniscus shape are shown to scale. In contrast to dip-coating, where only one meniscus shape is possible, in SCIM-coating an infinite number of meniscus shapes are possible. The method of calculating meniscus shapes and the basic conditions for meniscus stability are described in the Final Report to SERI, on Contract No. XS-9-8119-1.[28] Some calculated meniscus shapes are shown in Fig. 95. In performing the calculations, the meniscus pressure and the contact angle at the trough were used as parameters, but in actual experiment, the substrate angle and height are the parameters, and the contact angle can vary, as shown in Fig. 94.

Figure 94 basically illustrates desirable conditions for uniform thickness. The condition is that the locus of the LSI be perpendicular to the substrate. Then, if the substrate height varies (due to nonflatness, for example), the position of the LSI with respect to the substrate will not vary. Thus, the rate of heat removal, and consequently the thickness, will be constant.

There are also other conditions that are desirable for SCIM-coating. For example, it would be desirable to have a short meniscus to minimize edge

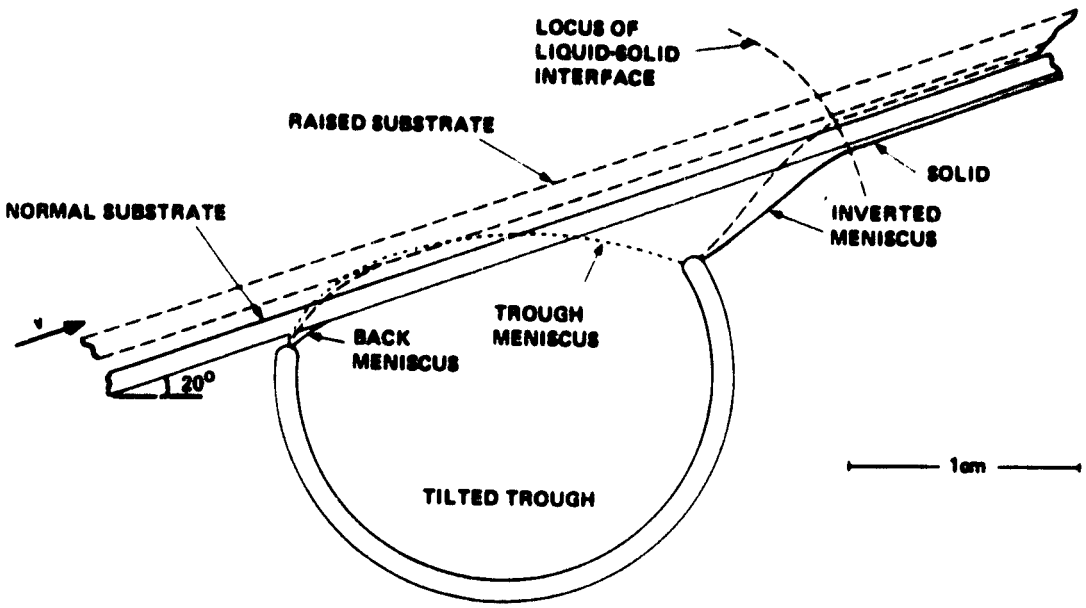


Figure 94. SCIM-coating configuration shown with calculated meniscus shapes for a pressure parameter, P = 0.5. The substrate is moving from left to right at an angle of 20° to horizontal. The position of the liquid-solid interface is determined by the point at which the slope of the meniscus is $20^{\circ} + 11^{\circ}$, where 11° is the contact angle.

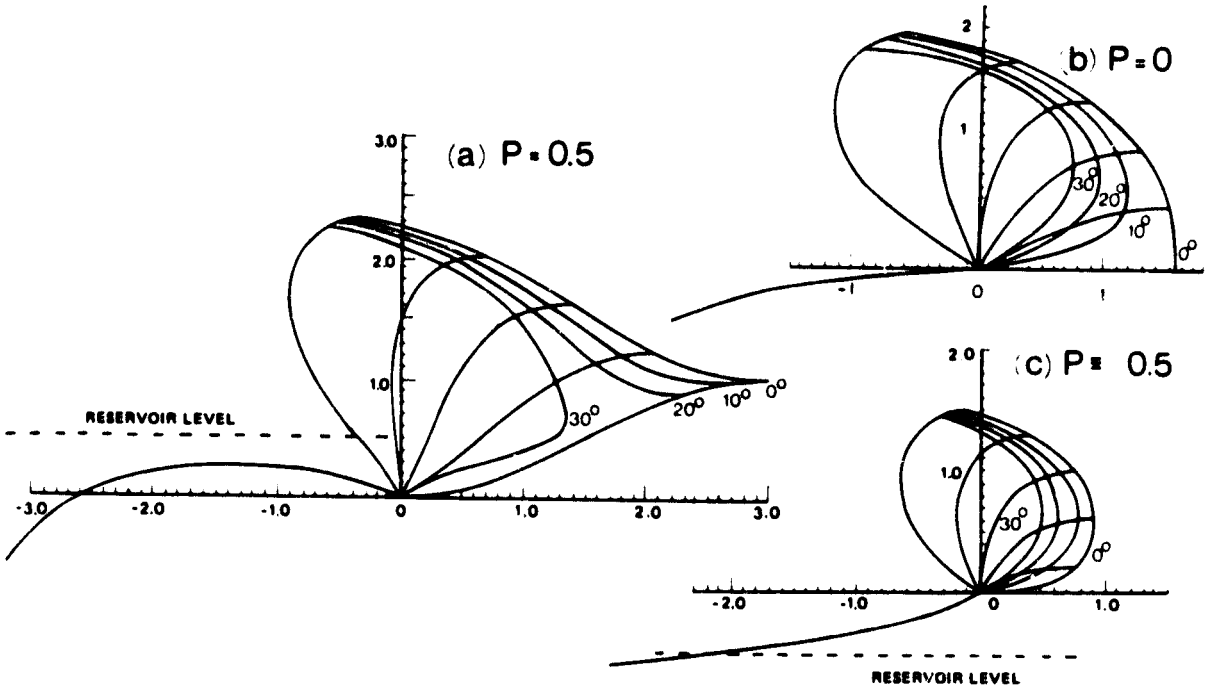


Figure 95. Calculated meniscus shapes and loci of constant slope. The three cases show three meniscus pressures: (a) P = 0.5; (b) P = 0; (c) P = -0.5. The curves labelled from 0° to 30° are loci of constant meniscus slope. The distance scales are dimensionless, with capillarity length as the scaling factor (5.4mm for silicon). The pressure, P, is the melt reservoir level with respect to the lip of the trough.

effects due to curvature of the meniscus at the edge of the substrate. From Fig. 95 it is clear that the shortest menisci are obtained by operating at negative pressure. A complete schematic with negative pressure (i.e., P = -0.5) is shown in Fig. 96. It is clear that a disadvantage of the negative pressure is that the trough meniscus is too low to ensure positive contact at the back meniscus. Figure 94, on the other hand, shows that with sufficient positive pressure, the trough meniscus is higher than the substrate, thus ensuring positive contact at the back meniscus.

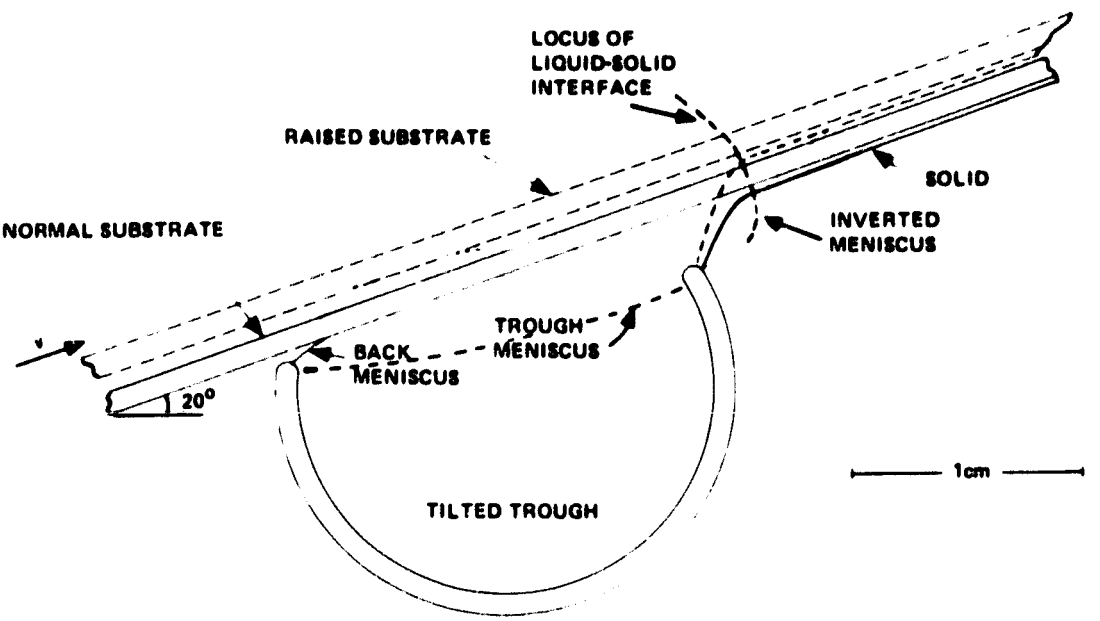


Figure 96. SCIM-coating configuration shown with calculated meniscus shapes for a pressure parameter P = -0.5. For this case, the trough meniscus is too low to contact the substrate. Thus, to achieve initial wetting, the pressure must be increased. It can then be decreased to achieve negative pressure.

From the above considerations, it is clear that the most stable growth condition is that in which the loci of constant meniscus slope have the least curvature, hence the widest range of stable substrate heights. This condition occurs for the case of P = +0.5 with slope = 30° in Fig. 95. This is the special case shown in Fig. 94, corresponding to a substrate slope of $30^{\circ} - 11^{\circ} = 19^{\circ}$. Thus, this is a condition for maximum growth stability, and is advantageous for both the front and back menisci. It is clear from Fig. 94 that the trough must be tilted backwards, as shown, to allow coating to take place at the optimum substrate height.

In summary, the effects of meniscus shape and meniscus stability are very important in SCIM-coating. Because of their complexity, calculations are quite helpful in specifying trough design and conditions for stable growth.

Physical Properties of SCIM Material - Structural characterization of SCIM-coated layers was performed under SERI support.[28] In summary, SCIM-coated layers appear to be structurally identical to dip-coated layers, i.e., the predominant structure is heavily twinned with {111} twin planes perpendicular to the surface and parallel to the <211> growth direction; the surfaces are close to the {110} planes. The grains, however, are generally larger in the SCIM layers but, as with dip-coated layers, they too are generally perpendicular to the layer's surface.

Electrical Properties of SCIM Material - A complete characterization of the electrical properties of SCIM material was never performed. This work could not be satisfactorily performed until the SCIM coating machines were fitted with purified carbon parts. Purified carbon parts could not, on the other hand, be installed until all necessary coater modifications were made to ensure satisfactory coatings.

Preliminary diffusion length (L_n) measurements on SCIM samples did, however, reveal L_n values of about 20μm, which is comparable to the 15 to 40μm values measured in dip-coated material by the same techniques (see Appendix A).

Solar Cell Effort

Fabrication Procedure - The SOC research and development program began as a silicon sheet materials investigation. One method for assessing the quality of the silicon sheet produced was to evaluate the performance of solar cells fabricated from this material. Because of the uniqueness of SOC, conventional fabrication procedures could not be used. That is, because the insulating substrate prevented direct contact to the back surface of the cell, special fabrication procedures had to be developed. These various procedures are described in SOC Annual Reports Nos. 1 through 5 and are summarized here.

First Year - Photodiodes were fabricated on dip-coated SOC material. The best diode had an active-area conversion efficiency, η, of 2.5% (AM1) with no antireflection (AR) coating. Other characteristics of this diode are given in Table 19, along with the corresponding characteristics of the best

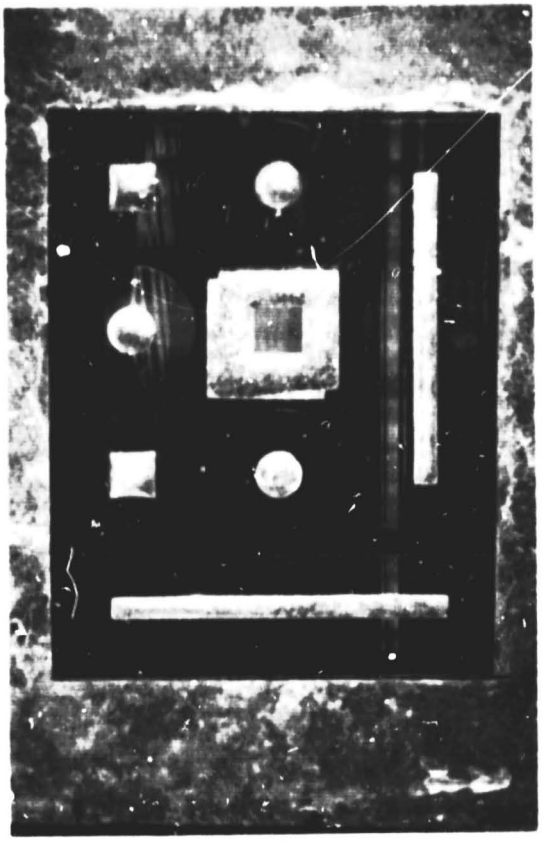
SOC cells fabricated during the second through fifth years. For the 2.5% efficient photodiode, the junction was formed using a P_2O_5 diffusion and a mesa etch process. Electroless nickel was used as the electrical contact to the p-type base region and silver paste was used to contact the diffused layer.

Table 19. Best cell summary data.

Cell Parameter	Year					Units	
	1	2	3	4	5		
η	2.5*	3.86	7.5	10.0	10.54	%	Total-area values
J_{sc}	11.7*	11	23.6	24.2	25.16	mA/cm^2	
V_{oc}	0.38	0.50	0.547	0.556	0.573	V	
FF	0.56	0.697	0.58	0.745	0.731		
A	0.03	1.73	4.1	4.1	5.0	cm^2	
% metal	X	40	10	10	8	%	
COMMENT	Photodiodes. *Active-area values for η and J_{sc} here only.	Interdigitated nonslotted cell.	Slotted SOC cell.	Slotted SOC cell.	Slotted SOC cell.		

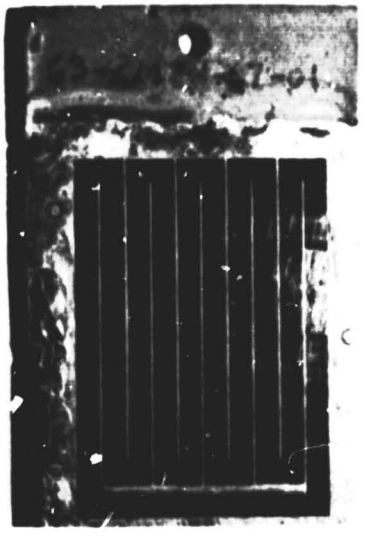
Second Year - Interdigitated SOC cells were fabrication on solid (non-slotted) SOC substrates. As shown in Table 19, the best cell had a total-area conversion efficiency of 3.86%, for a total of $1.73cm^2$. The junction in this cell was formed by a P_2O_5 diffusion. The interdigitated cell pattern was defined by using photoresist and an Fe_2O_3 mask. The cell area was defined by using plasma etching. The base contact was made by using a platinum-silicon contact, followed by nickel and indium solder. The cell patterns are shown in Fig. 97.

Third Year - Slotted substrate SOC cells were developed during this year. The best cell had a conversion efficiency of 7.5% (AM1, AR), for a cell area of $4.08cm^2$. Also developed were new diffusion and AR coating



(a)

(b)



(c)

Figure 97. SOC solar cells. (a) An array of diodes. The central square is a base contact, as well as the surrounding outer region. (b) An interdigitated contact solar cell with 1cm^2 active area. (c) A solar cell with 10cm^2 active area.

technique. For the diffusion process, which used phosphine as the source gas, a more uniform temperature profile was achieved in the furnace and a baffle was added to increase phosphine gas uniformity. The diffusion furnace gas flow rates were also optimized. For the AR coating process a new vacuum system was developed. This (diffusion-pumped) system used a silicon-oxide evaporation source from Vacuum Atmosphere Company.

During the third year, it was also recognized that a serious series resistance could be introduced into the cell using slot openings for back electrical contact purposes. An analysis of parasitic resistance was made and is discussed in Appendix B of this report.

Fourth Year - The efficiencies of SOC cells were improved by optimizing the base layer impurity concentration. The results of the study are indicated by solid lines in Fig. 98. The dashed lines represent earlier data reported in SOC Quarterly Report No. 12. The more recent data indicate that cell performance can be improved if the N_B, is greater than $10^{16}/cm^3$. The recent results differ from the previous results primarily at the low and high base doping concentrations. That is, several new SOC cells were fabricated with concentrations of 2.3×10^{15} and $4.6 \times 10^{16}/cm^3$. It is assumed that the recent results are more accurate than the previous results. In the remainder of this subsection we will refer only to the solid curves in Fig. 98.

Figure 98(a) shows that the open-circuit voltage, V_{oc}, increases linearly as a function of log N_B. For a given value of N_B, the center of the vertical line indicates the average value of V_{oc} and the length of the line is 2σ, where σ is the standard deviation. Thus, for a base doping concentration of $2.3 \times 10^{16}/cm^3$, the average value was 0.536V, with a standard deviation of 0.005V. For the low and high values of N_B, two vertical lines are given. The lower line corresponds to the results of SOC Quarterly Report No. 12 and the upper line to the recent results. The upper lines are sometimes slightly displaced to the right or left so that the various vertical lines do not overlap. The solid line for V_{oc} indicates approximately how the average value of V_{oc} should vary as a function of N_B, based on the recent measurement.

As has been stated, Fig. 98(a) shows that V_{oc} increases linearly as a function of log N_B. This result is consistent with conventional solar cell

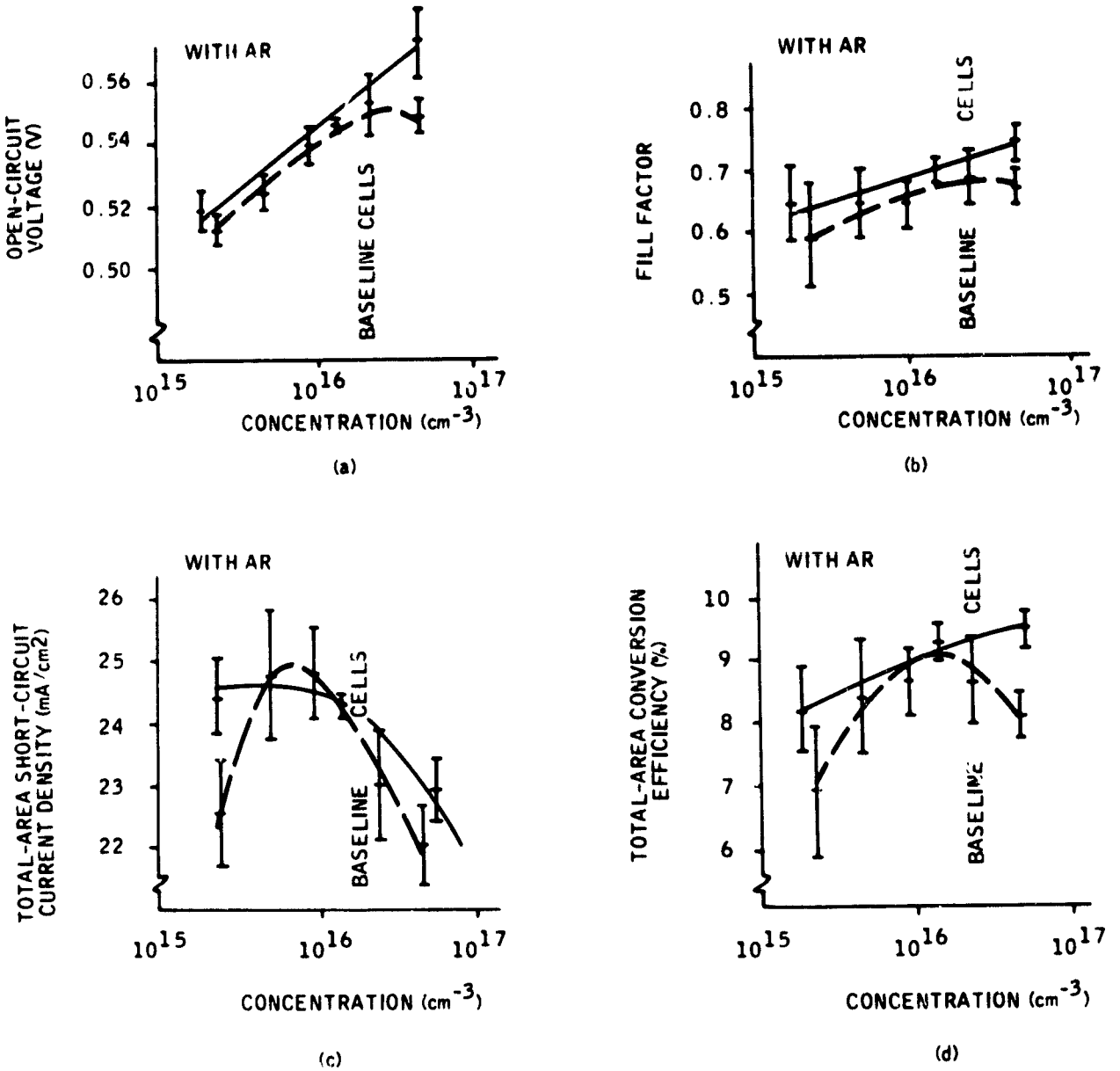


Figure 98. Performance of slotted SOC solar cells as a function of base doping concentration, for cells with AR coating. Dashed lines correspond to results given in SOC Quarterly Report No. 12. Solid lines correspond to results given in SOC Annual Report No. 4.

theory. Figure 98(b) shows that the fill factor, FF, also increases linearly as a function of log N_B. The increase is due primarily to a corresponding decrease in series resistance. Figure 98(c) shows that, as N_B increases, the short-circuit current density, J_{sc}, is relatively constant until $N_B = 10^{16}/cm^3$ and then decreases for higher values of N_B. Finally, Fig. 98(d) shows that the conversion efficiency, η, increases monotonically as N_B increases for the range of values measured.

During the fourth year, photodiodes were fabricated from layers of various thicknesses in an effort to determine how cell performance is affected by film thickness. The results are shown in Fig. 99. It should be noted that all data are without an AR coating. The results indicate that the efficiency increases by about 20% as the silicon thickness increases from 100μm to 200μm.

The best cell fabricated during the fourth year had a total area conversion efficiency, η, of 10% (AM1, AR), for a cell area of $4.1cm^2$.

Fifth Year - Cell performance was improved significantly by using a slow cooldown following the phosphorus diffusion. The diffusion temperature is 850°C for 80 minutes. The diffusion cycle is divided into a 10-minute preheat time, a 60-minute source time, and a 10-minute postheat. The slow cooldown procedure was adopted as a routine practice.

To improve cell performance, a number of process variations were investigated and the principal ones are listed in Table 20. The major results of these experiments were discussed in SOC Quarterly Reports Nos. 14 and 15. These results are summarized below, along with some more recent results:

1) Melt-Current Experiment - Eight SOC cells were fabricated to determine the effect of an electric current through the melt during dip-coating. It was hoped that this current might reduce melt contamination by influencing the transport of impurities from the substrate into the melt. Based on the results of the eight cells, an electric current does not seem to have an effect on melt contamination.

2) No-Doping Experiment - Four SOC cells were fabricated to determine the effects of progressive melt contamination on the sheet resistance of the dip-coated SOC material. For the ninth and twelfth substrates dipped in Run No. 228, the sheet resistance was 770 and 550 ohms/

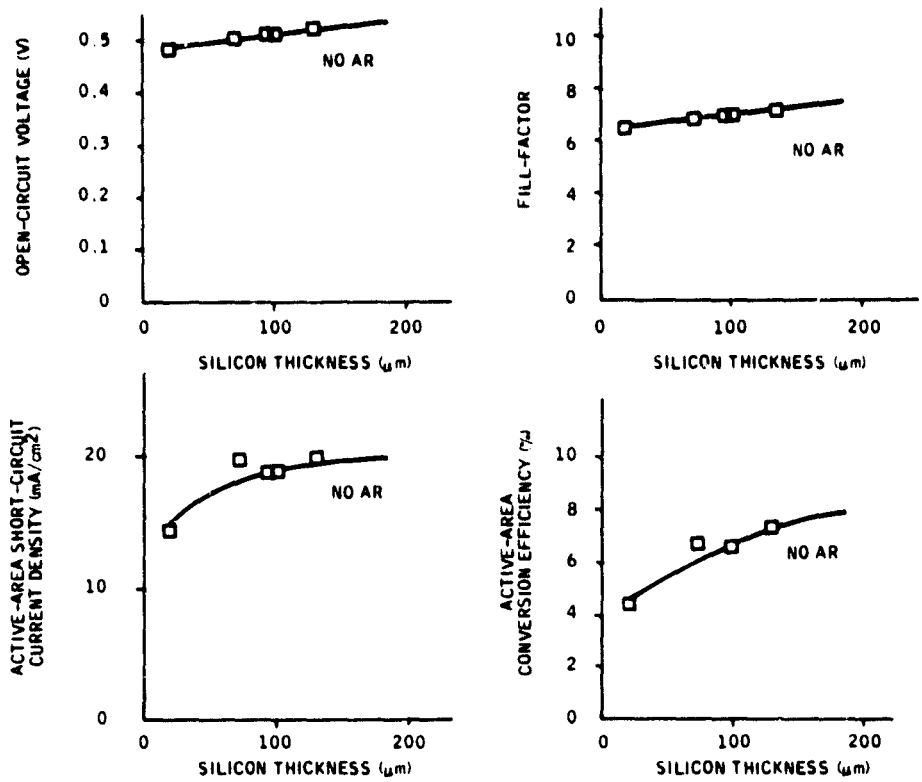


Figure 99. Photodiode characteristics as a function of silicon thickness. The photodiodes were fabricated on unslotted SOC materials grown at various speeds. Squares are experimental data points.

Table 20. Experiments for increasing cell performance.

Item	Experiment	Objectives	Results
1	Melt current	Reduce impurities	No effect
2	No doping	Determine rate of contamination	Graph of ρ vs N
3	Aluminum doping	Determine if aluminum doping improves J_{sc}	Reduces J_{sc}
4	Heavy doping	Determine effect of heavy doping	Reduces J_{sc}
5	Carbon substrate	Measure melt quality	Poor structure
6	Ion-implantation	Increase J_{sc}	Preliminary results
7	Hydrogenation	Increase J_{sc}	Some improvements
8	Two-step	Increase J_{sc}	Some improvements
9	Slow-cool	Increase J_{sc}	Significant improvements
10	Etching	Increase J_{sc}	No improvements

square, respectively. Cells fabricated using these SOC substrates had efficiencies in the range from 4.3 to 6.1% (AM1, no AR). This indicates that the mullite progressively contaminated the melt with a p-type dopant, shown to be aluminum in earlier experiments. Such contamination is a basic problem for the dip-coating technique. A similar problem should not exist for the SCIM-coating technique, since the mullite will not be in direct contact with the silicon melt.

3) Aluminum-Doping Experiment - Eleven SOC cells were fabricated to determine if aluminum doping could produce higher values of J_{sc} for a given doping concentration. The highest J_{sc} is 14.68 mA/cm^2 (AM1, no AR) for an aluminum doping concentration of 2.2 x 10^{16}/cm^3. This value is low compared with an average value of 17 mA/cm^2 for boron-doped samples. Thus, aluminum doping does not seem to produce high values of J_{sc}.

4) Heavy-Doping Experiment - Eight solar cells were fabricated using SOC material with a boron-doping concentration of 10^{18}/cm^3, as compared with the normal concentration of 5 x 10^{16}/cm^3. Our objective was to extend the experimental results given in Fig. 4 of SOC Quarterly Report No. 14 in order to determine the upper limit for the base-doping concentration. The fabricated cells were of poor quality and only the J_{sc} results were of value. The most interesting result was that the average J_{sc} was 19 mA/cm^2, as compared with 21 mA/cm^2, the value associated with the linear regression line given in Fig. 4 of SOC Quarterly Report No. 14. The 19 mA/cm^2 value indicates that Auger recombination begins to limit the performance of SOC cells for base-doping concentrations greater than 10^{18}/cm^3, as expected.

5) Carbon-Substrate Experiment - Several carbon substrates were dipped first in a run in order to learn more about melt contamination from the ceramic substrate. We had planned to make photodiodes on the resulting silicon layers and to compare the performance of these diodes with the performance of corresponding diodes on SOC material. Unfortunately, the grain structure of the silicon layers on the carbon substrates was rather poor and, as a result, we did not complete this experiment.

6) Ion-Implant Experiment - Eight SOC cells were fabricated using ion

implantation and thermal anneal to form the n^+ emitter region. Arsenic was used as the dopant. For one set of SOC cells the annealing temperature was 850°C for 60 minutes. The emitter sheet resistance was approximately 32 ohms/square and the efficiency of one ion-implant/anneal cell was 5.6%, as compared with the 6.7% efficiency of a corresponding cell used for a control. More work needs to be done to determine the proper annealing conditions.

7) Hydrogenation Experiment - Results for this experiment are discussed in the Evaluation of SOC Material subsection of this report.

8) Two-Step Experiment - Eighteen solar cells were fabricated to determine the effects of a two-step diffusion process. The best two-step cell had a total-area conversion efficiency of 10.26% (AM1, AR) for a cell area of $5cm^2$. For one group of cells, the two-step process was similar to the process described by DiStefano and Cuomo,[29] as well as by Lindmayer.[30] This two-step process basically is as follows: First, a low-temperature phosphorus diffusion is used to diffuse phosphorus atoms down grain boundaries using a spin-on diffusion source and diffusion conditions of 600°C for 60 minutes. Second, the initial diffusion source is then removed and the normal high-temperature phosphorus diffusion is used to form the p-n junction. For a second group of cells the initial spin-on source was used for both the low- and high-temperature diffusion. For a third group the order of the two diffusions was interchanged. The latter process seems to produce the highest efficiencies.

9) Slow-Cooldown Experiment - Twenty-seven SOC cells were fabricated using a slow cooldown after the phosphorus diffusion. Typically, the cooling rate was approximately 3°C/min from the diffusion temperature of 850°C to 700°C. The slow cooldown seems to produce a significant increase in cell performance.

10) Etching Experiment - Nineteen cells were fabricated from SOC material that was etched before the phosphorus diffusion. The main idea is to determine if cell performance can be improved by removing impurities that segregate to the silicon surface during growth. Various etches have been used, including KOH etch, Sirtl etch, CP4 etch, and plasma

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[29] DiStefano and Cuomo, Appl. Phys. Lett. 30, 351 (1977).

[30] Lindmayer, 13th IEEE Photovoltaic Specialist's Conf., p. 1096.

etch. In all cases, we have removed approximately, 3μm of material from the surface of the SOC material. None of the etches produced a noticeable increase in cell performance.

During 1980 all SOC cells were fabricated using a well-established and reproducible process. For a group of 74 cells - called the 1980 baseline cells - the conversion efficiency was 9.6% with a standard deviation of 0.5%. This process is described below:

1) Initial Clean - The as received SOC material is first dipped into straight HF for 30 seconds and rinsed in DI water. The silicon surface is scribbed using soap and water and rinsed in DI water. The SOC material is dipped in sulfuric peroxide (H_2SO_4/H_2O_2, 3:1) for 5 minutes and rinsed in DI water. It is then dipped in Aqua Regia (HCl/HNO_3, 3:1) for 5 minutes and rinsed in DI water. Finally, it is dipped in straight HF, rinsed in DI water, and blown dry with dry N_2.

2) Phosphorus Diffusion - The SOC material is baked at 120°C (±10°C) overnight and then placed in a phosphine diffusion furnace for 80 minutes at 850°C. After the diffusion, the SOC material is cooled down at a rate of 3°C/minute from 850°C to 700°C and then withdrawn from the furnace. The sheet resistance is about 45 ohms/square.

3) Back Contact - Photoresist is applied to the front surface and the silicon is etched on the back side in the slot regions, to remove completely the back surface n^+ region formed during the diffusion. About 700Å of platinum is sputter-deposited on the back surface and then sintered at 600°C for 30 minutes to form a PtSi contact. About 2000Å of nickel is sputter-deposited to provide a good surface for soldering.

4) Front Contact - The front metal pattern is defined by using photolithography. About 800Å of titanium is sputter-deposited, followed by 2000Å of nickel. Finally, the whole substrate is dipped in tin-indium solder at 170°C.

5) Mesa Formation - The cell area is defined by using photolithography and by using plasma etching to form a mesa cell structure, with an area of about $5cm^2$.

6) AR Coating - About 600Å of SiO is evaporated on the surface of the cell to complete the SOC cell structure.

Solar Cell Performance - The year-by-year best performance level of cells produced since the inception of this program is given in Table 19. Near the end of this program (December, 1980), the best dip-coated cell had a total-area conversion efficiency, η, of 10.54% (AM1, AR) and the best SCIM-coated cell had an η of 7.6% (AM1, AR). Each cell has a total area of $5cm^2$ and uses a slotted substrate. The current-voltage characteristics of these two cells are given in Figs. 100 and 101.

During 1980, we fabricated approximately 250 SOC cells from dip-coated material. Of these cells, 74 were fabricated under nearly the same condition and the principle characteristics of these cells - which are called the 1980 baseline cells - are listed in Tables 21 and 22. The 10.54% cell noted above is not included in these tables, since this cell was fabricated using a nonstandard fabrication process which consisted of using an H_2/Ar atmosphere during the growth of the SOC material. Distribution graphs for the 1980 baseline cells are given in Figs. 102 and 103, corresponding to conditions before and after AR coating. As can be seen, the average cell efficiency is 9.6% (AM1, AR), with a standard deviation of 0.5%. This deviation indicates that our standard cell fabrication process can produce very reproducible results.

To increase our understanding of the SOC cell, empirical and theoretical modeling was performed. The results of this modeling are summarized here: In Quarterly Report No. 14 we presented a figure showing cell performance as a function of the base doping concentration for the 1979 baseline cells. This figure, which is based on 136 SOC cells, is reproduced here as Fig. 104. The experimental results are indicated by the vertical lines; the calculated results, by the solid curves. These impirical curves can be calculated as follows: First, linear regression is used to determine a relationship between J_{sc} and N_B. The result is

$$J_{sc} = 1.48 \log \left(\frac{9.7 \times 10^{31}}{N_B} \right) \qquad (61)$$

where J_{sc} is short-circuit current density in units of mA/cm^2 and N_B is base layer doping concentration in units of cm^{-3}. Second, linear regression

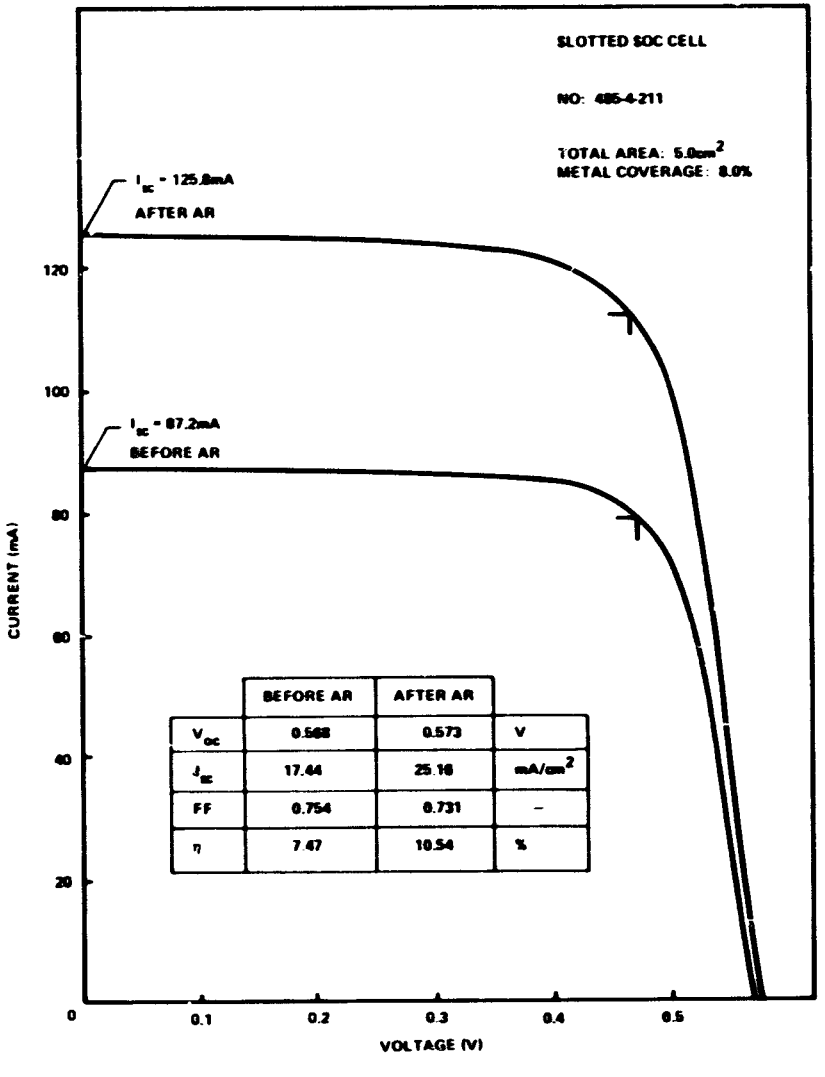


Figure 100. Current-voltage characteristics of a slotted cell fabricated from dip-coated material.

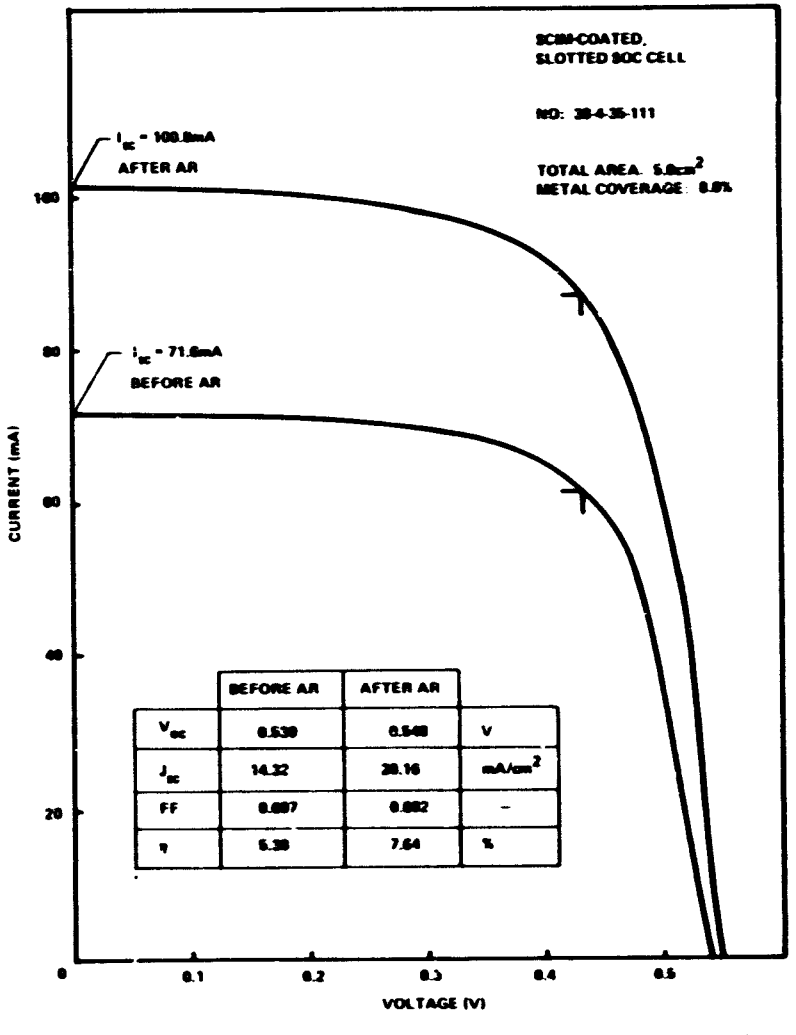


Figure 101. Current-voltage characteristics of a slotted SOC cell fabricated from SCIM-coated material.

Table 21. Conversion efficiencies of the 1980 baseline SOC cells.

Item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/□)	Total Area Conversion Efficiencies Before AR (%)	After AR (%)
1	226 - 3-111	4.7e+016	0.06	0.7	24.0	6.45	9.28
2	226 - 3-211	4.7e+016	0.06	0.8	24.0	6.93	9.63
3	238 - 8-111	5.0e+016	0.06	1.0	29.0	6.85	9.56
4	238 - 8-211	5.0e+016	0.06	0.8	29.0	5.95	8.51
5	241 - 4-111	5.0e+016	0.06	0.7	29.0	6.40	8.77
6	241 - 4-211	5.0e+016	0.06	0.8	29.0	5.57	8.17
7	244 - 3-111	5.0e+016	0.06	0.6	18.0	5.73	8.40
8	244 - 3-211	5.0e+016	0.06	0.8	18.0	7.15	9.75
9	244 -11-111	5.0e+016	0.06	0.7	22.0	6.03	8 43
10	244 -11-211	5.0e+016	0.06	0.8	22.0	7.08	9.79
11	244 -12-111	5.0e+016	0.06	0.7	21.0	6.70	9.42
12	244 -12-211	5.0e+016	0.06	0.8	21.0	5.71	8.50
13	248 - 1-111	5.0e+016	0.06	0.6	25.0	5.92	8.61
14	248 - 1-211	5.0e+016	0.06	0.8	25.0	6.82	9.62
15	248 - 2-111	5.0e+016	0.06	0.7	24.0	6.71	9.42
16	248 - 2-211	5.0e+016	0.06	1.0	24.0	3.93	6.60
17	248 - 4-111	5.0e+016	0.06	0.7	30.0	6.81	9.41
18	248 - 4-211	5.0e+016	0.06	0.9	30.0	7.02	9.94
19	249 - 7-111	5.0e+016	0.06	0.7	20.0	7.07	10.07
20	249 - 7-211	5.0e+016	0.06	0.8	20.0	5.24	8.39
21	251 - 3-111	5.0e+016	0.06	0.9	15.0	7.06	9.90
22	251 - 3-211	5.0e+016	0.06	0.9	15.0	6.28	9.12
23	251 - 8-111	5.0e+016	0.06	0.8	21.0	6.48	9.26
24	251 - 8-211	5.0e+016	0.06	0.7	21.0	6.81	9.78
25	252 - 3-111	5.0e+016	0.06	0.8	14.0	6.89	9.56
26	252 - 3-211	5.0e+016	0.06	0.7	14.0	6.61	9.78
27	252 - 4-111	5.0e+016	0.06	0.8	19.0	6.92	9.87
28	252 - 4-211	5.0e+016	0.06	0.9	19.0	7.06	9.96
29	252 - 6-111	5.0e+016	0.06	0.7	21.0	7.11	9.80
30	252 - 6-211	5.0e+016	0.06	0.7	21.0	7.26	10.12
31	252 - 7-111	5.0e+016	0.06	0.6	25.0	7.00	9.96
32	252 - 7-211	5.0e+016	0.06	0.7	25.0	6.59	9.48
33	252 - 9-111	5.0e+016	0.06	0.8	19.0	7.05	9.80
34	252 - 9-211	5.0e+016	0.06	0.9	19.0	7.16	10.22
35	253 - 3-111	5.0e+016	0.06	0.7	18.0	7.22	10.42
36	253 - 3-211	5.0e+016	0.06	0.7	18.0	7.17	10.38
37	253 - 4-111	5.0e+016	0.06	0.8	22.0	7.19	9.97
38	253 - 4-211	5.0e+016	0.06	1.0	22.0	7.22	9.82
39	254 - 1-111	5.0e+016	0.06	1.4	21.0	6.62	9.15
40	254 - 1-211	5.0e+016	0.06	0.6	21.0	6.92	9.97
41	254 - 6-111	5.0e+016	0.06	0.7	21.0	6.78	10.19
42	254 - 6-211	5.0e+016	0.06	0.7	21.0	6.98	10.11
43	254 - 9-111	5.0e+016	0.06	0.6	26.0	7.08	10.03
44	254 - 9-211	5.0e+016	0.06	0.6	26.0	6.85	9.96
45	255 - 2-111	5.0e+016	0.06	0.8	21.0	6.90	9.58
46	255 - 2-211	5.0e+016	0.06	0.6	21.0	7.09	9.82
47	255 - 5-111	5.0e+016	0.06	0.6	22.0	7.08	9.87
48	255 - 5-211	5.0e+016	0.06	0.7	22.0	7.58	10.21
49	255 - 7-111	5.0e+016	0.06	0.6	27.0	6.97	9.91

Table 21. Conversion efficiencies of the 1980 baseline SOC cells (concluded).

Item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/[])	Total Area Conversion Efficiencies Before AR (%)	After AR (%)
50	255 - 7-211	5.0e+016	0.06	0.7	27.0	6.92	10.03
51	256 - 6-111	5.0e+016	0.06	1.3	52.0	6.92	9.77
52	256 - 6-211	5.0e+016	0.06	1.4	52.0	7.00	9.90
53	257 -13-111	5.0e+016	0.06	0.9	29.0	6.70	9.64
54	257 -13-211	5.0e+016	0.06	1.6	29.0	6.80	9.35
55	258 - 7-111	5.0e+016	0.06	0.9	22.0	6.94	9.52
56	258 - 7-211	5.0e+016	0.06	0.7	22.0	7.16	10.13
57	258 - 8-111	5.0e+016	0.06	1.1	35.0	6.78	9.76
58	258 -12-111	5.0e+016	0.06	0.9	36.0	6.67	9.58
59	258 -12-211	5.0e+016	0.06	1.0	36.0	6.37	9.13
60	473 - 7-211	5.0e+016	0.06	0.8	30.0	7.14	9.82
61	474 - 8-111	5.0e+016	0.06	0.8	23.0	7.10	9.88
62	474 - 8-211	5.0e+016	0.06	0.9	23.0	6.87	9.58
63	474 -10-111	5.0e+016	0.06	1.0	27.0	6.92	9.60
64	474 -10-211	5.0e+016	0.06	1.2	27.0	6.73	9.52
65	474 -11-111	5.0e+016	0.06	0.7	31.0	7.02	10.20
66	474 -11-211	5.0e+016	0.06	0.8	31.0	6.79	9.64
67	475 - 5-111	5.0e+016	0.06	1.5	31.0	6.97	9.73
68	475 - 5-211	5.0e+016	0.06	1.2	31.0	7.36	10.10
69	477 - 7-111	5.0e+016	0.06	0.9	46.0	6.89	9.47
70	477 - 7-211	5.0e+016	0.06	0.9	46.0	6.88	9.33
71	477 -11-111	5.0e+016	0.06	0.9	37.0	6.85	9.75
72	477 -11-211	5.0e+016	0.06	0.9	37.0	7.21	9.86
73	478 -11-111	5.0e+016	0.06	0.9	29.0	6.59	9.72
74	478 -11-211	5.0e+016	0.06	0.8	29.0	6.98	9.86

Table 22. Characteristics of recent AR-coated SOC cells.

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)
1	226 - 3-111-0	80.40	0.551	0.728	16.08	6.45
1	226 - 3-111-1	114.80	0.570	0.709	22.96	9.28 (AR)
2	226 - 3-211-0	83.70	0.554	0.747	16.74	6.93
2	226 - 3-211-1	117.30	0.570	0.719	23.46	9.62 (AR)
3	238 - 8-111-0	82.60	0.556	0.757	16.52	6.95
3	238 - 8-111-1	114.10	0.570	0.735	22.82	9.56 (AR)
4	238 - 8-211-0	82.10	0.546	0.664	16.42	5.95
4	238 - 8-211-1	114.20	0.560	0.665	22.84	8.51 (AR)
5	241 - 4-111-0	78.40	0.554	0.737	15.68	6.40
5	241 - 4-111-1	107.40	0.566	0.721	21.48	8.77 (AR)
6	241 - 4-211-0	77.70	0.536	0.669	15.54	5.57
6	241 - 4-211-1	110.00	0.551	0.674	22.00	8.17 (AR)
7	244 - 3-111-0	81.50	0.552	0.673	16.30	5.73
7	244 - 3-111-1	114.20	0.559	0.658	22.84	8.40 (AR)
8	244 - 3-211-0	82.30	0.563	0.772	16.46	7.15
8	244 - 3-211-1	114.90	0.565	0.751	22.98	9.75 (AR)
9	244 -11-111-0	81.60	0.557	0.663	16.32	6.03
9	244 -11-111-1	110.70	0.568	0.670	22.14	8.43 (AR)
10	244 -11-211-0	83.00	0.562	0.759	16.60	7.08
10	244 -11-211-1	113.60	0.572	0.753	22.72	9.79 (AR)
11	244 -12-111-0	79.60	0.560	0.752	15.92	6.70
11	244 -12-111-1	117.20	0.565	0.711	23.44	9.42 (AR)
12	244 -12-211-0	81.10	0.552	0.638	16.22	5.71
12	244 -12-211-1	117.90	0.560	0.644	23.58	8.50 (AR)
13	248 - 1-111-0	81.00	0.546	0.669	16.20	5.92
13	248 - 1-111-1	111.20	0.561	0.690	22.24	8.61 (AR)
14	248 - 1-211-0	82.40	0.550	0.753	16.48	6.82
14	248 - 1-211-1	113.90	0.567	0.745	22.78	9.62 (AR)
15	248 - 2-111-0	79.40	0.556	0.760	15.88	6.71
15	248 - 2-111-1	115.50	0.568	0.718	23.10	9.42 (AR)
16	248 - 2-211-0	79.60	0.526	0.469	15.92	3.93
16	248 - 2-211-1	116.50	0.548	0.517	23.30	6.60 (AR)
17	248 - 4-111-0	81.30	0.550	0.761	16.26	6.81
17	248 - 4-111-1	111.50	0.563	0.750	22.30	9.41 (AR)
18	248 - 4-211-0	83.50	0.552	0.761	16.70	7.02
18	248 - 4-211-1	115.80	0.566	0.758	23.16	9.94 (AR)
19	249 - 7-111-0	84.10	0.560	0.753	16.82	7.07
19	249 - 7-111-1	121.10	0.575	0.723	24.22	10.07 (AR)

Table 22. Characteristics of recent AR-coated SOC cells (continued).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)
20	249 - 7-211-0	78.50	0.540	0.618	15.70	5.24
20	249 - 7-211-1	120.00	0.560	0.624	24.00	8.39 (AR)
21	251 - 3-111-0	84.40	0.566	0.739	16.88	7.06
21	25. - 3-111-1	120.20	0.575	0.716	24.04	9.90 (AR)
22	251 - 3-211-0	84.80	0.560	0.661	16.96	6.28
22	251 - 3-211-1	121.10	0.570	0.661	24.22	9.12 (AR)
23	251 - 8-111-0	80.00	0.564	0.718	16.00	6.48
23	251 - 8-111-1	120.40	0.568	0.677	24.08	9.26 (AR)
24	251 - 8-211-0	81.60	0.563	0.741	16.32	6.81
24	251 - 8-211-1	122.70	0.567	0.703	24.54	9.78 (AR)
25	252 - 3-111-0	80.20	0.566	0.759	16.04	6.89
25	252 - 3-111-1	117.30	0.572	0.713	23.44	9.56 (AR)
26	252 - 3-211-0	80.10	0.562	0.734	16.02	6.61
26	252 - 3-211-1	120.20	0.570	0.714	24.04	9.78 (AR)
27	252 - 4-111-0	82.30	0.569	0.739	16.46	6.92
27	252 - 4-111-1	118.40	0.575	0.725	23.68	9.87 (AR)
28	252 - 4-211-0	82.90	0.565	0.754	16.48	7.04
28	252 - 4-211-1	120.10	0.571	0.726	24.02	9.96 (AR)
29	252 - 6-111-0	83.50	0.569	0.748	16.70	7.11
29	252 - 6-111-1	119.50	0.579	0.708	23.90	9.80 (AR)
30	252 - 6-211-0	83.80	0.567	0.764	16.76	7.26
30	252 - 6-211-1	119.40	0.578	0.733	23.88	10.12 (AR)
31	252 - 7-111-0	80.70	0.566	0.767	16.14	7.00
31	252 - 7-111-1	120.50	0.577	0.716	24.10	9.96 (AR)
32	252 - 7-211-0	80.20	0.558	0.736	16.04	6.59
32	252 - 7-211-1	120.00	0.570	0.693	24.00	9.48 (AR)
33	252 - 9-111-0	82.60	0.570	0.749	16.52	7.05
33	252 - 9-111-1	116.20	0.580	0.727	23.24	9.80 (AR)
34	25. - 9-211-0	83.60	0.570	0.751	16.72	7.16
34	252 - 9-211-1	122.30	0.578	0.723	24.46	10.22 (AR)
35	253 - 3-111-0	84.80	0.565	0.754	16.96	7.22
35	253 - 3-111-1	123.60	0.573	0.736	24.72	10.42 (AR)
36	253 - 3-211-0	84.80	0.564	0.750	16.96	7.17
36	253 - 3-211-1	125.10	0.572	0.725	25.02	10.38 (AR)
37	253 - 4-111-0	84.30	0.563	0.757	16.86	7.19
37	253 - 4-111-1	119.10	0.578	0.724	23.82	9.97 (AR)

Table 22. Characteristics of recent AR-coated SOC cells (continued).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)
38	253 - 4-211-0	84.80	0.560	0.760	16.96	7.22
38	253 - 4-211-1	121.10	0.574	0.706	24.22	9.82 (AR)
39	254 - 1-111-0	80.30	0.560	0.736	16.06	6.62
39	254 - 1-111-1	118.20	0.569	0.680	23.64	9.15 (AR)
40	254 - 1-211-0	79.00	0.563	0.778	15.80	6.92
40	254 - 1-211-1	119.10	0.570	0.734	23.82	9.97 (AR)
41	254 - 6-111-0	83.40	0.564	0.721	16.68	6.78
41	254 - 6-111-1	119.40	0.572	0.746	23.88	10.19 (AR)
42	254 - 6-211-0	81.40	0.562	0.763	16.28	6.98
42	254 - 6-211-1	117.40	0.567	0.760	23.48	10.11 (AR)
43	254 - 9-111-0	82.70	0.565	0.758	16.54	7.08
43	254 - 9-111-1	117.90	0.580	0.733	23.58	10.03 (AR)
44	254 - 9-211-0	80.90	0.561	0.755	16.18	6.85
44	254 - 9-211-1	119.30	0.575	0.726	23.86	9.96 (AR)
45	255 - 2-111-0	80.20	0.564	0.763	16.04	6.90
45	255 - 2-111-1	112.80	0.573	0.741	22.56	9.58 (AR)
46	255 - 2-211-0	82.80	0.565	0.758	16.56	7.09
46	255 - 2-211-1	114.70	0.573	0.747	22.94	9.82 (AR)
47	255 - 5-111-0	82.30	0.569	0.756	16.46	7.08
47	255 - 5-111-1	119.50	0.575	0.718	23.90	9.87 (AR)
48	255 - 5-211-0	86.00	0.571	0.772	17.20	7.58
48	255 - 5-211-1	120.60	0.577	0.731	24.12	10.21 (AR)
49	255 - 7-111-0	81.70	0.565	0.755	16.34	6.97
49	255 - 7-111-1	116.50	0.571	0.745	23.30	9.91 (AR)
50	255 - 7-211-0	82.10	0.563	0.748	16.42	6.92
50	255 - 7-211-1	116.70	0.573	0.750	23.34	10.03 (AR)
51	256 - 6-111-0	86.00	0.561	0.717	17.20	6.92
51	256 - 6-111-1	126.10	0.574	0.675	25.22	9.77 (AR)
52	256 - 6-211-0	87.80	0.557	0.716	17.56	7.00
52	256 - 6-211-1	125.70	0.573	0.687	25.14	9.90 (AR)
53	257 -13-111-0	83.50	0.551	0.732	16.70	6.79
53	257 -13-111-1	116.10	0.563	0.737	23.22	9.64 (AR)
54	257 -13-211-0	85.40	0.551	0.723	17.08	6.80
54	257 -13-211-1	117.30	0.563	0.708	23.46	9.35 (AR)
55	258 - 7-111-0	83.00	0.560	0.746	16.60	6.94
55	258 - 7-111-1	117.00	0.569	0.715	23.40	9.52 (AR)

Table 22. Characteristics of recent AR-coated SOC cells (concluded).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Total-Area Eff (%)	
56	258 - 7-211-0	84.00	0.561	0.760	16.80	7.16	
56	258 - 7-211-1	117.10	0.570	0.759	23.42	10.13	(AR)
57	258 - 8-111-0	83.50	0.560	0.725	16.70	6.78	
57	256 - 8-111-1	119.40	0.571	0.716	23.88	9.76	(AR)
58	258 -12-111-0	85.00	0.555	0.707	17.00	6.67	
58	258 -12-111-1	119.30	0.567	0.708	23.86	9.58	(AR)
59	258 -12-211-0	84.00	0.549	0.691	16.80	6.37	
59	258 -12-211-1	118.00	0.559	0.692	23.60	9.13	(AR)
60	473 - 7-211-0	85.10	0.563	0.745	17.02	7.14	
60	473 - 7-211-1	121.20	0.574	0.706	24.24	9.82	(AR)
61	474 - 8-111-0	83.60	0.565	0.752	16	7.10	
61	474 - 8-111-1	120.80	0.569	0.719	24.16	9.88	(AR)
62	474 - 8-211-0	81.30	0.561	0.753	16.26	6.87	
62	474 - 8-211-1	119.70	0.565	0.708	23.94	9.58	(AR)
63	474 -10-111-0	82.10	0.560	0.752	16.42	6.92	
63	474 -10-111-1	119.70	0.568	0.706	23.94	9.60	(AR)
64	474 -10-211-0	82.50	0.559	0.730	16.50	6.73	
64	474 -10-211-1	120.30	0.569	0.695	24.06	9.52	(AR)
65	474 -11-111-0	82.10	0.562	0.761	16.42	7.02	
65	474 -11-111-1	116.50	0.573	0.764	23.30	10.20	(AR)
66	474 -11-211-0	80.10	0.559	0.758	16.02	6.79	
66	474 -11-211-1	114.30	0.570	0.749	22.86	9.64	(AR)
67	475 - 5-111-0	87.10	0.564	0.709	17.42	6.97	
67	475 - 5-111-1	119.50	0.575	0.708	23.90	9.73	(AR)
68	475 - 5-211-0	86.50	0.568	0.749	17.30	7.36	
68	475 - 5-211-1	121.10	0.574	0.726	24.22	10.10	(AR)
69	477 - 7-111-0	82.30	0.558	0.750	16.46	6.89	
69	477 - 7-111-1	113.60	0.564	0.739	22.72	9.47	(AR)
70	477 - 7-211-0	84.50	0.558	0.729	16.90	6.88	
70	477 - 7-211-1	114.30	0.563	0.725	22.86	9.33	(AR)
71	477 -11-111-0	82.80	0.557	0.743	16.56	6.85	
71	477 -11-111-1	118.70	0.571	0.719	23.74	9.75	(AR)
72	477 -11-211-0	85.90	0.557	0.753	17.18	7.21	
72	477 -11-211-1	121.00	0.570	0.715	24.20	9.86	(AR)
73	478 -11-111-0	81.90	0.555	0.725	16.38	6.59	
73	478 -11-111-1	116.20	0.570	0.734	23.24	9.72	(AR)
74	478 -11-211-0	82.90	0.559	0.753	16.58	6.98	
74	478 -11-211-1	117.00	0.568	0.742	23.40	9.86	(AR)

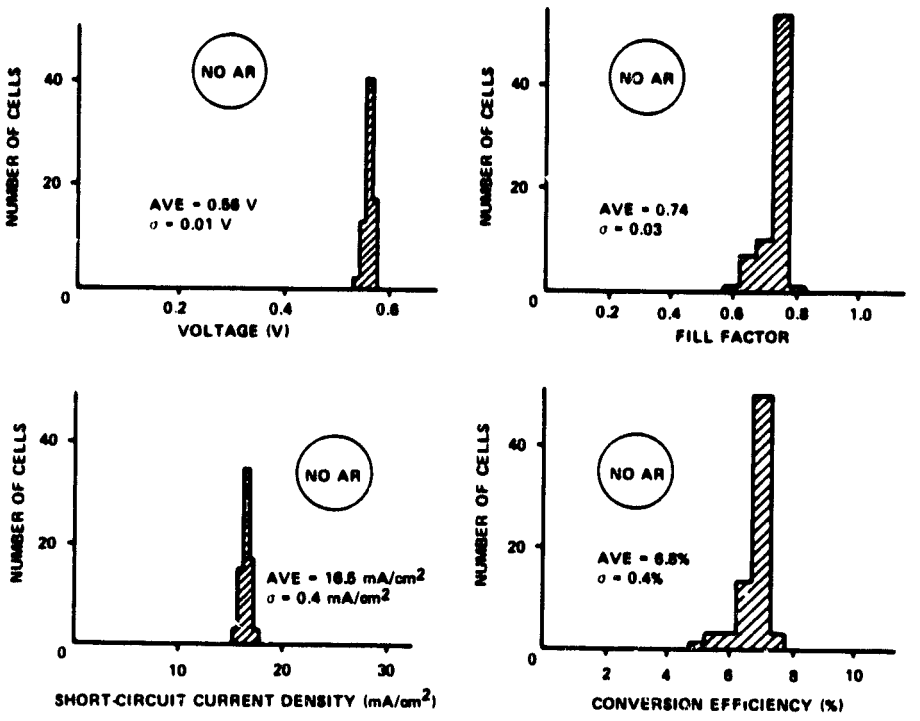


Figure 102. Distribution graphs for the 1980 baseline SOC cells for conditions before AR coating.

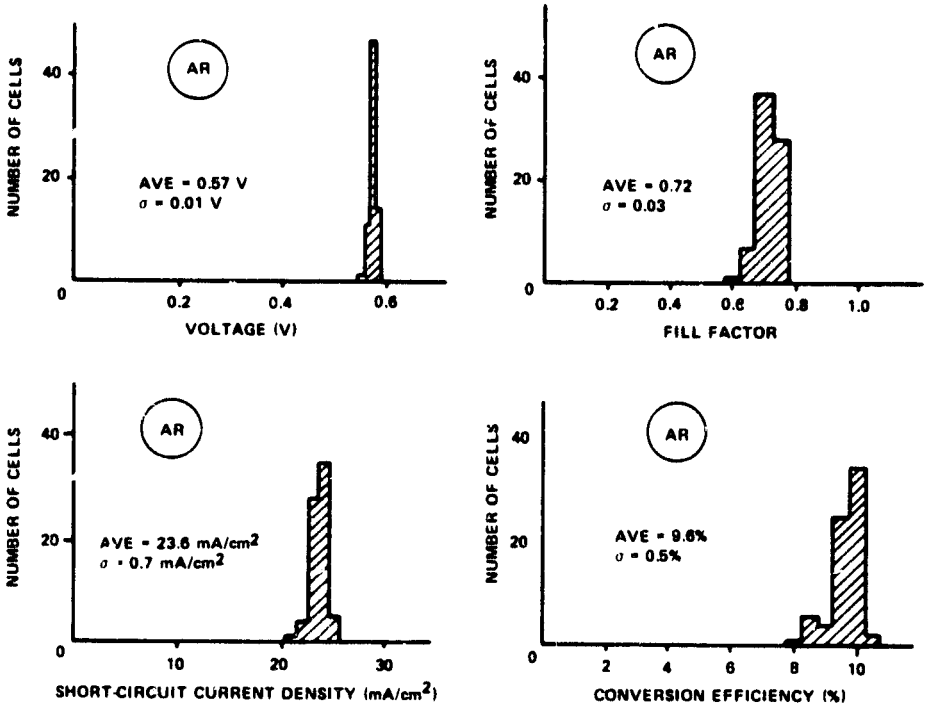


Figure 103. Distribution graphs for the 1980 baseline SOC cells for conditions after AR coating.

is used to determine an empirical relationship between J_{01} and N_B. For the data given in Table 4 of SOC Monthly Report No. 34, the result is

$$J_{01} = \frac{9.6}{N_B^{0.54}} \qquad (62)$$

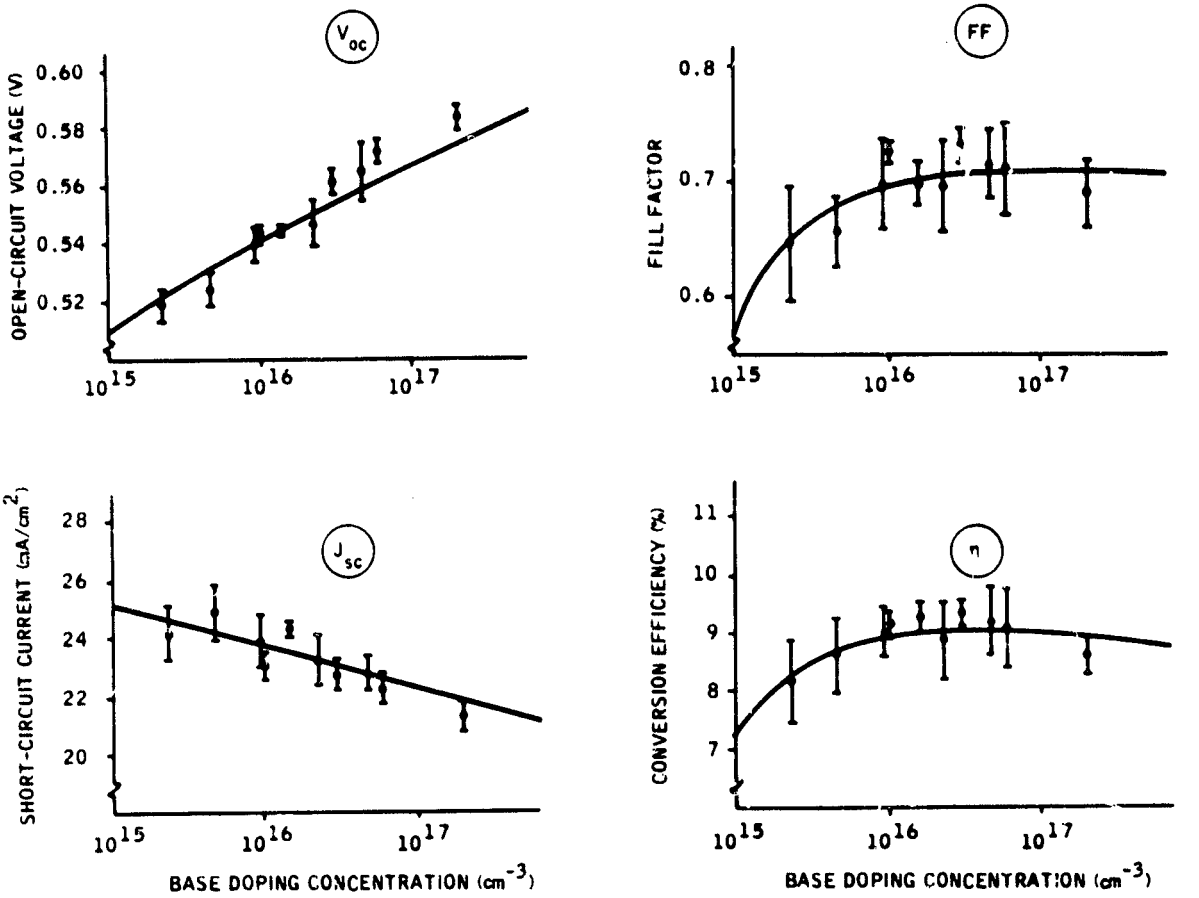


Figure 104. Cell performance as a function of base doping concentration, for the 1979 baseline cells. The characteristics of these cells were reported in SOC Annual Report No. 4 and in SOC Quarterly Report No. 14. Vertical lines are experiment results; solid curves are calculated results.

where J_{01} is reverse-saturation current density in units of mA/cm^2. Third, the theoretical expression for the specific series resistance, R_sA, as given in SOC Quarterly Report No. 12, is used, with an empirical constant of 1.75 added to approximate the measured results. The resulting expression is

$$R_sA = 2.25 + \frac{3.35 \times 10^{15}}{N_B} \tag{63}$$

where R_sA is in units of ohms-cm^2. For Eq. (63) a growth velocity of 3.6 cm/min is assumed. Finally, the current density is assumed to be given by

$$J = J_{01}\left[\exp\left(\frac{q(V - JR_sA)}{kT}\right) - 1\right] + J_{02}\left[\exp\left(\frac{q(V - JR_sA)}{nkT}\right) - 1\right] + \left(\frac{V - JR_sA}{R_{sh}}\right) - J_{sc} \tag{64}$$

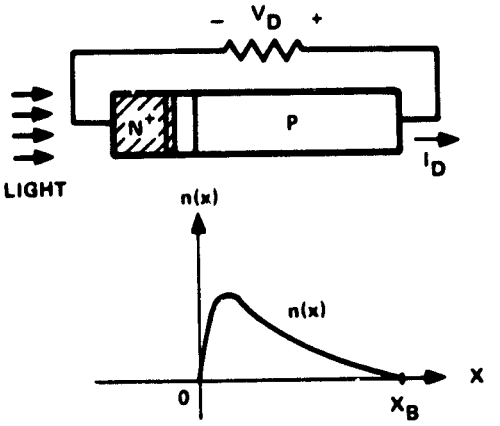
where J_{02} is 10^{-4} mA/cm^2 and n is 2. Equations (61) through (64) give the empirical curves of Fig. 104. Clearly, the empirical curves approximate the experimental results.

Now we turn from empirical modeling to theoretical modeling. Our objective is to understand more completely the performance limitations of SOC cells. In particular, we want to determine a relationship between the short-circuit current, J_{sc}, and the minority-carrier diffusion length, L_{nB}, assuming AM1 conditions.

To begin, we consider only generation in the base region and monochromatic light. These restrictions will be removed as we progress. Moreover, we will assume that the geometry is one-dimensional and that the effects of the grain boundaries can be neglected. In other words, we initially consider an SOC cell structure that approximates a one-dimensional, single-crystal cell structure having a base diffusion length corresponding to that of SOC material. The basic cell configuration is shown in Fig. 105, along with a list of the various parameter values. A list of notation is given in Table 23. With the noted assumptions, conventional semiconductor theory yields the following five equations for low-level conditions:

$$p(0) = \frac{n_i^2}{N_{DE}} \exp\frac{q(-V_{jE})}{kT} \tag{65}$$

$$n(0) = \frac{n_i^2}{N_{AB}} \exp\frac{q(-V_{jE})}{kT} \tag{66}$$



VALUES OF CONSTANTS

$N_{DE} = 10^{20}/cm^3$	$N_{AB} = 5 \times 10^{16}/cm^3$
$\frac{D_{pE}}{L_{pE}} = 2.3 \times 10^4$ cm/sec	$D_{nB} = 23.3$ cm^2/sec
$A = 1$ cm^2	$L_{nB} = 0.005$ cm
$q = 1.6 \times 10^{-19}$ coul	$X_B = 0.02$ cm
$n_i = 1.45 \times 10^{10}/cm^3$	$b_B = 3.06$
$kT/q = 0.0259$ V	

Figure 105. Solar cell configuration and values of constants used in the analysis. The distribution of minority carriers, n(x), is shown at the maximum power point.

Table 23. Notation used for modeling of the SOC cell structure.

Notation	Definition
A	Total surface area, cm^2.
b_B	Defined as D_{nB}/D_{pB}.
D_{nB}	Electron diffusivity in base region, cm^2/sec.
D_{pE}/L_{pE}	Empirical constant for emitter region, cm/sec.
I_D	Total current, mA.
I_{sc}	Short-circuit current, mA.
$I_p(x)$	Hole current, mA.
kT/q	Thermal voltage, V.
L_{nB}	Electron diffusion length in base region, cm.
N_{DE}	Donor concentration in the emitter region, cm^{-3}.
N_{AB}	Acceptor concentration in the base region, cm^{-3}.
n_i	Intrinsic concentration, cm^{-3}.
n(x)	Electron concentration, cm^{-3}.
q	Electrical charge, coul.
V_D	Diode voltage, V.
V_{oc}	Open-circuit voltage.
V_{jE}	Electrostatic potential drop across the emitter-base space-charge region minus the corresponding drop at equilibrium, V.
x	Distance from the boundary between the space charge region and the base region, cm.
X_B	Thickness of the base region, cm.
α	Absorption coefficient, cm^{-1}.

$$V_D = - V_{jE} + R_S I_D \tag{67}$$

$$I_D = qA \frac{D_{pE}}{L_{pE}} p(0) + I_n(0) \tag{68}$$

$$I_n(0) = qAF(1 - R) \frac{\alpha L_{nB}}{(\alpha^2 L_{nB}^2 - 1)} \left\{ \alpha L_{nB} - \frac{\cosh(X_B/L_{nB}) - \exp(-\alpha X_B)}{\sinh(X_B/L_{nB})} \right\}$$

$$- qA_L \frac{D_{nB}}{L_{nB}} n(0) \tag{69}$$

For monochromatic light having a wavelength of 0.882μm, these equations given the current-voltage characteristics shown in Fig. 106. (Also shown are the corresponding current-voltage characteristics for AM1 light conditions, which will be discussed below.) For monochromatic light, the minority carrier profile in the base region is given by

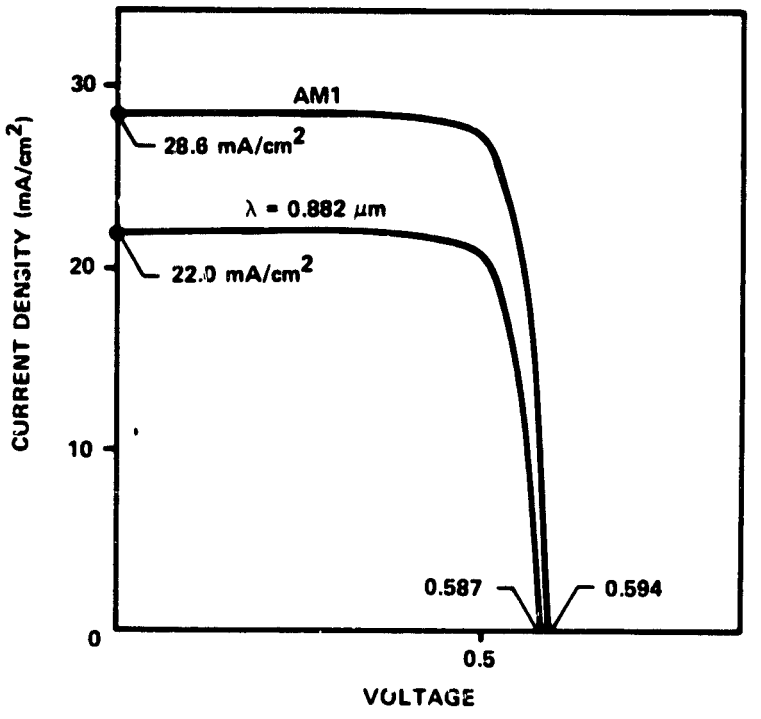


Figure 106. Calculated current-voltage characteristics for monochromatic light of wavelength of 0.882μm and for AM1 light.

$$\frac{n(x)}{N_{AB}} = \left\{\frac{I_n(0)}{qA(D_{nB}/L_{nB})N_{AB}} - \alpha L_p\, Y\right\} \sinh\left(\frac{x}{L_{nB}}\right) + \left\{\frac{n(0)}{N_{AB}} + Y\right\} \cosh\left(\frac{x}{L_{nB}}\right) - Y \sinh(-\alpha x) \tag{70}$$

where

$$Y = \frac{\alpha F(1 - R)\,\tau_{nB}}{(\alpha^2 L_{nB}^2 - 1)N_{AB}} \tag{71}$$

Equation (70) is plotted in Fig. 107 for three values of wavelength. The figures demonstrate the following: As the wavelength increases, the slope at x = 0 decreases, indicating a decrease in collection efficiency. The latter decrease is approximately given by

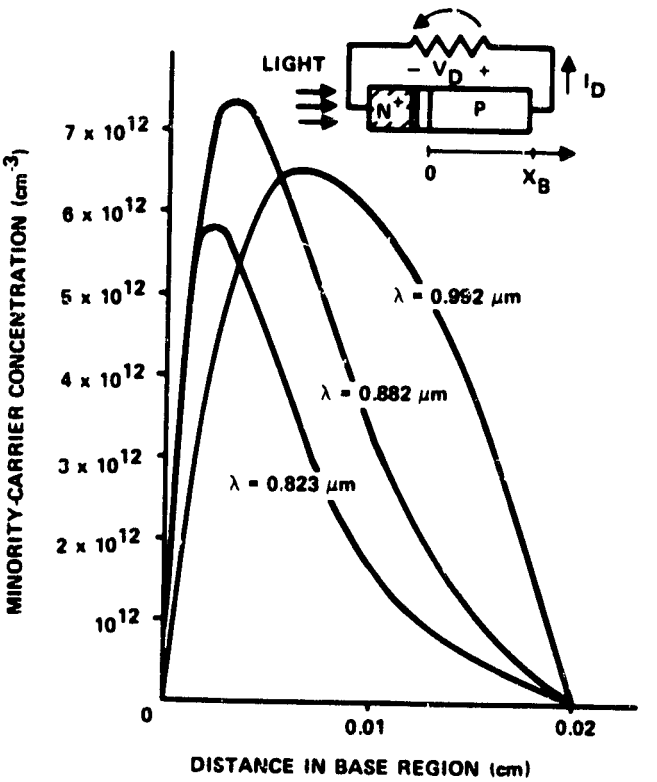


Figure 107. Minority-carrier profiles in the base region for three values of wavelength: 0.823, 0.882, and 0.982μm. The profiles were calculated at the maximum power point.

$$\eta_{col} = \frac{L_{nB}\alpha}{1 + L_{nB}\alpha} \tag{72}$$

which is a well-known approximation. In particular, Eq. (72) is used to evaluate the diffusion length from LBIC measurements of η_{col}.

Now we turn to AM1 conditions. Our primary objective is to calculate a theoretical upper limit for J_{sc} and to compare this value with the measured values of J_{sc} for SOC cells. For AM1 conditions, we must solve the following standard differential equation by numerical methods:

$$\frac{d^2n}{dx^2} - \frac{n(x)}{L_{nB}^2} + \frac{G(x)}{D_{nB}} = 0 \tag{73}$$

where

$$G(x) = \frac{1}{hc} \int_0^\infty \lambda\alpha P(\lambda) \exp\left[-\alpha x\right] d\lambda \tag{74}$$

Here $P(\lambda)$ is the AM1 solar power spectral density given as a function of the photon wavelength, . For Eq. (74) we have assumed that the AR coating is perfect (i.e., R = 0) and that the thickness of the emitter region is negligible. The boundary conditions for Eq. (74) are

$$n(x) = n(0) \text{ at } x = 0 \tag{75}$$

and

$$n(x) = 0 \text{ at } x = X_B \tag{76}$$

Using numerical methods and Eqs. (69) through (72), we can determine a relationship between $I_n(0)$ and n(0), which is the generalization of the monochromatic result expressed by Eq. (69). The generalized relationship can then be used with Eqs. (65) through (69) to give the AM1 current-voltage curve shown in Fig. 106. Figure 108 shows the corresponding minority-carrier profiles for J_{sc}, P_{max}, and V_{oc}.

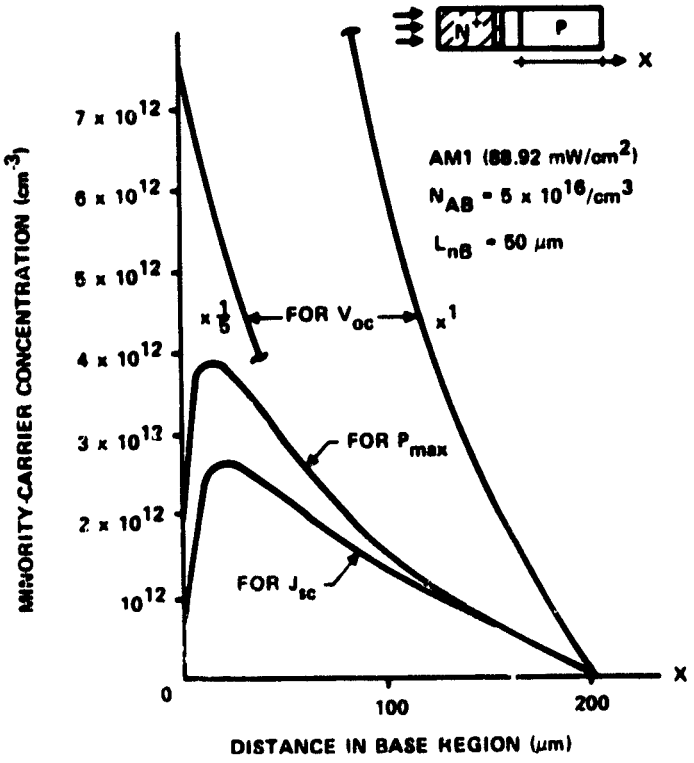


Figure 108. Minority-carrier profiles for J_{sc}, P_{max}, and V_{oc}. The profiles correspond to the AM1 curve given in Fig. 106.

For all calculations, the incident power density, P_{in}, is 88.92 mW/cm^2, which is the accepted value for AM1 sunlight. This value is about 10% lower than the 100-mW/cm^2 value generally used for cell measurements with an ELH lamp. For the figure, the metallization coverage was neglected, which means the J_{sc} is about 10% higher than possible with a typical metallization pattern. The low value of P_{in} approximately compensates for the neglect of the metallization coverage. Thus, AM1 results shown in Fig. 106 approximately represent measurement conditions using an ELH lamp with an incident power density of 100 mW/cm^2.

So for all calculations, we have assumed a diffusion length of 50μm and negligible series resistance. Figure 109 shows the calculated cell characteristics for values of L_{nB} in the range from 10μm to 100μm, where the solid lines correspond to a specific series resistance of 1 ohm-cm^2 and

where the dotted lines correspond to negligible series resistance. For the 1 ohm-cm^2 case, the calculated maximum efficiency is 11.2% for L_{nB} = 25μm 13.3% for L_{nB} = 50μm, and 14.5% for L_{nB} = 100μm. The measured characteristics of the SOC cell shown in Fig. 110 are indicated by squares in Fig. 109. For this cell there is fair agreement between theory and experiment.

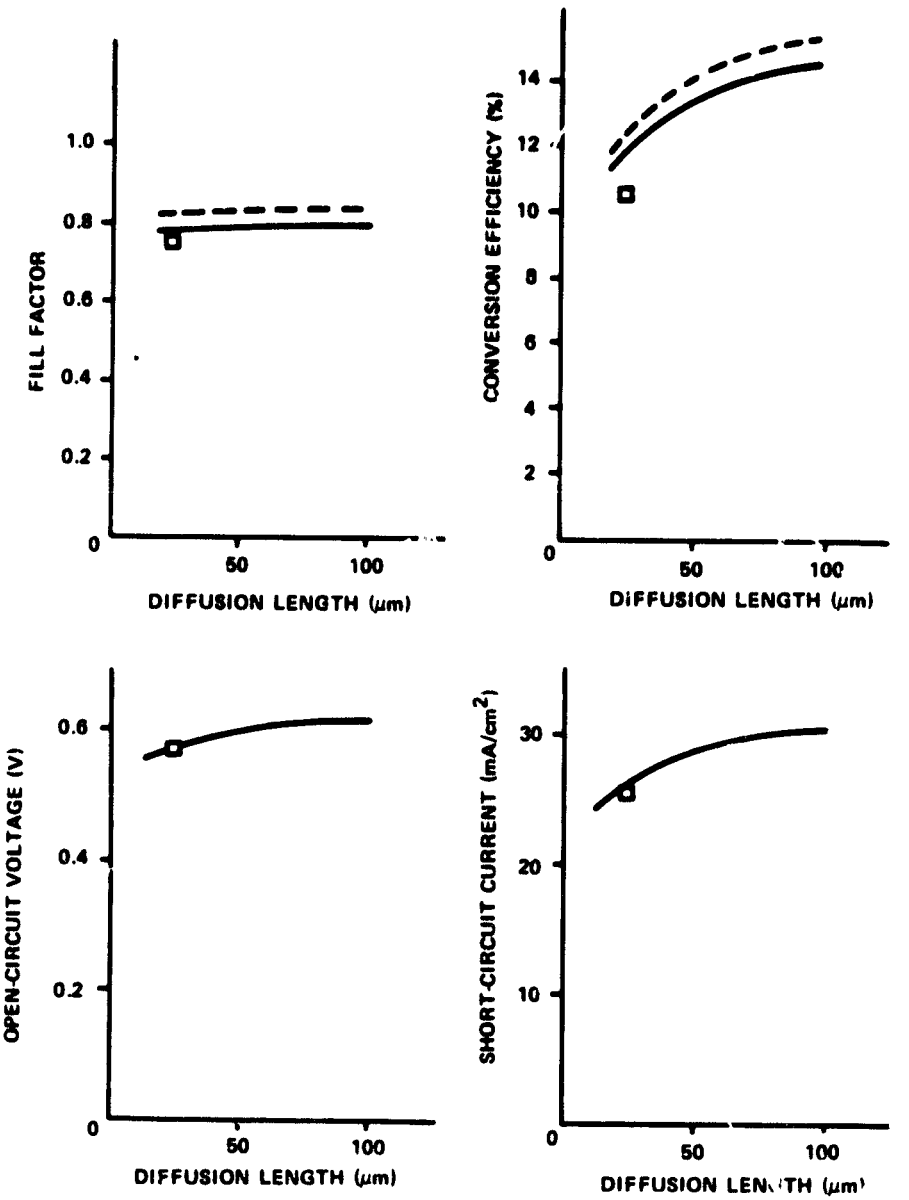


Figure 109. Solar cell characteristics as a function of base diffusion length for a base thickness of 200μm. Dotted lines assume no series resistance, solid lines include 1-ohm/cm^2 specific resistance. The squares in the latter correspond to cell No. 255-5-211-1.

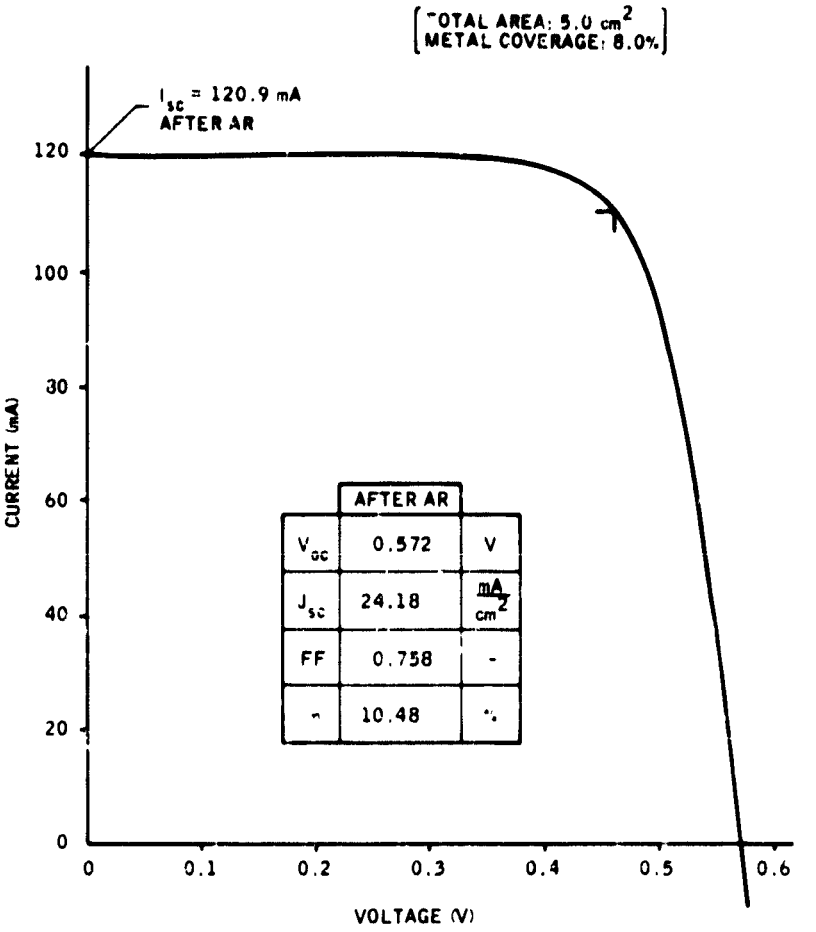


Figure 110. Current-voltage characteristics of cell No. 255-5-211-1.

COST ANALYSIS

Introduction

The cost of silicon-coated ceramic has been determined at least annually by a sequence of different methods. Prior to 1978, our cost estimates were derived according to procedures practiced in one of Honeywell's factories.[31] When the SAMIS methodology and the IPEG formula [32] became available, our own cost procedures were no longer used. Early in 1978, a direct comparison was made using the Honeywell procedure versus the IPEG formula, with the same direct-cost input. The two prices differed by less than 5%, which is within the accuracy of the data. Our most recent estimates, including those contained in this report, are according to the revised IPEG-2 formula.[33] A later revision,[34] only recently available, has not been used in our calculations.

In over 4 years and several iterations of price estimations, the projected production costs for the SOC technology have not changed significantly in equivalent dollars. For example, an added-value requirement of $\$13.01/m^2$ (1980 dollars) was calculated in 1977,[31] compared with the IPEG-2 estimate of $\$12.99/m^2$ reported in this document. A calculation by SAMIS-III based on 1979 data yielded an added value of $\$13.70/m^2$. Some major changes have occurred in the projected technology, particularly in the transition from dip-coating to SCIM-coating. It was reasonable to expect a lower labor intensity for SCIM, which is a continuous process, than for dip-coating, which is a complicated batch operation. However, the labor saving was offset when the orginally projected pulling speed of 1.0 cm/sec was revised to 0.25 cm/sec as a more realistic goal.

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[31] ERDA/JPL 954356-77/3, Annual Report No. 2, published September 30, 1977.

[32] R. W. Aster and R. G. Chamberlain, "IPEG: A precursor and an Adjunct to SAMIS-III, Version One," JPL Document 5101-33, September 10, 1977.

[33] R. W. Aster, "IPEG-2: Improved Price Estimation Guidelines," in JPL Document 5101-142 (December 1979), pp. 355-357.

[34] P. J. Firnett, "Improved IPEG Computer Program User's Guide," JPL Document 5101-156, Rev. A., November 17, 1980.

This subsection presents the cost analysis for SOC, reflecting (a) 1986 target technology, and (b) the technology as it exists today. The analysis of even today's technology is hypothetical, since the following assumed conditions have not yet been proven

- Continuous automated operation at stated duty cycle
- High-volume substrate availability at quoted price
- 92% yield
- Simultaneous coating of two substrates

The required prices are expressed in both dollars per square meter and cents per peak watt. For the latter, we assume a net subsequent processing yield (cell and module production)[35] of (0.95) (0.995) = 0.945. A final graph indicates sheet cost versus efficiency that must be satisfied by our process in order to achieve a 70-cents/W_p module price.

The major economic assumptions will be more clearly understood in terms of the summary process description, which follows next.

Process Summary

Slotted mullite substrates, measuring 12.5cm by 50cm and 1mm thick, are automatically conveyed from the substrate unpacking area to the CARBCOAT equipment. A suspension of pulverized carbon in isopropyl alcohol is applied by roller to one surface of the substrates at a linear speed of 3 cm/sec. Eight substrates (100cm total width) are processed simultaneously for a per-unit throughput of 1.8 m^2/min. Compressed air is used to expedite drying. The process is highly automated, requiring one production operator per eight units. All material handling is automatic.

[35] R. W. Aster, "Price Allocation Guidelines," JPL Document 5101-68, Rev. A, January 15, 1980.

The 12.5cm x 50cm carbonized substrates are automatically coveyed from the CARBCOAT line to the SILCOAT furnaces. The substrates approach the furnaces side-by-side in pairs. A pair of substrates enters a furnace by way of the heating zone, which is roughly 40cm long, so that the carbonized surfaces are facing downwards. The substrates are heated from room temperature to roughly 1420°C in 2.7 minutes, the time it would take for a point on the substrate to transverse the heating zone at 15 cm/min. The coating chamber immediately following is maintained near 1420°C, and molten silicon is applied from a transversely oriented trough to the underside of the substrates. Next is the cooling zone, which is also about 40cm long. Both heating and cooling zones are carefully designed to minimize residual stresses in the coated substrate. For this purpose, it is desirable to maintain constant temperature gradients in the moving substrate in the elastic-plastic transition between 500°C and 1000°C. A separate thermal requirement is imposed immediately following the silicon solidification position, at the beginning of the cooling zone. Normally, active cooling (forced convection plus radiation) would be required here to accommodate the latent heat of fusion at the 15-cm/min linear growth speed; however, passive (radiative) cooling would suffice with an elongated solidification front as in cold-substrate or hot-substrate growth techniques. The present cost analysis assumes passive cooling. A slight positive pressure of inert atmosphere (argon) is maintained in all three zones.

A nominal 7-year life is assumed on the cabinet, substrate drive and support structures, power supplies, and electrical and cooling water connections. Electrical furnace elements, insulation packages, crucibles, and troughs are replaced on a regular weekly shutdown schedule. Preventive maintenance on substrate drive is assumed to take place during these scheduled shutdowns. Scheduled shutdowns are 12 hours per week, allowing for cooling and startup. Only the crucibles are replaced weekly.

The process will be automated to an extent requiring instrument monitoring but no material handling. One operator will monitor 12 furnaces, or 24 substrates in process. The minimal vertical height requirements will permit heating furnaces to be stacked vertically in groups of six.

From SILCOAT, the cooled, coated substrates are conveyed to INSPECT stations, where they are subjected in sequence to two tests called SCAN and RESIST. The equipment for each test has an output of 12 pieces ($0.75m^2$) per minute.

The SCAN equipment monitors the coated surfaces for nonspecular reflection into a cylindrical collector, which would be an indication of a coating gap or some other gross fault. The raster scan used a 2.5mm spot, with transverse deflection provided by rotating mirrors. The sweep speed is 625 cm/sec, or 50 sec/sweep across the panel. Longitudinal displacement of successive sweeps is provided by the 12.5-cm/sec advance. A total of 5 seconds is required: 4 seconds scan plus 1 second between panels. The RESIST equipment makes resistance measurements by means of a four-point probe. The test is performed at four locations on each panel, 1 second each, plus 1 second between panels, totaling 5 seconds per panel. Direct labor is calculated on a piece rate basis and averages out to 0.648 production machine operator and 0.936 inspector for each pair of test machines.

Principal Assumptions for Target Technology*

- Substrates are available at $\$5.78/m^2$, slotted, in 5M m^2/yr quantities. This is according to an IPEG-2 estimate made by a potential vendor in December, 1980.
- The graphite-in-propanol suspension is \$6.96/gal, or $\$0.054/m^2$ as applied, in accordance with the actual experimental data.
- Carbon coating apparatus is \$10,200 per unit net, adjusted for salvage value and removal/installation cost. The useful life is 7 years.
- Carbon coating output is $1.8m^2$/minute.
- Silicon-coating units are \$50,800 net, adjusted for salvage value and removal/installation costs. Useful life is 7 years (See Process Summary).
- Crucible replacement cost is \$80 per week per unit.
- Furnace heating elements are replaced at 6-month intervals at a cost of \$1200 per unit.
- Insulation packages are replaced annually at a cost of \$240 per unit.
- Argon gas consumption is 0.117 ft^3/min., which is about one-sixth of the experimental rate. The reduced figure is the estimated seepage from redesigned entrance and exit ports.
- • Electrical consumption in SILCOAT is calculated to be 3.67kW: 3.39kW required to heat the substrates and silicon and melt the silicon at the stated throughput; plus 0.28kW radiative losses.

*Items marked with two bullets differ from Progress-to-Date technology.

- Polysilicon cost is assumed to be $14/kg.
- SILCOAT duty cycle is 85%. Of the downtime, 7.1% is for scheduled maintenance (Process Summary) and 7.9% is unscheduled maintenance.
- Silicon-coating rate is 0.0368 m^2/min based on two panels coated simultaneously (25cm total width) at an advance speed of 15 cm/min. There is a 1cm gap between panels in the advance direction.
- Production area is reduced by stacking SILCOAT units in vertical groups of six.
- One production machine operator monitors 12 machines (two stacks).
- Inspection requires SCAN and RESIST at $50,800 and $6,100 each, respectively. A useful life of 10 years is assumed for each machine.
- Inspect output is 0.75 m^2/min for each test. Production operator load is based on 0.9 standard hour per 1000 pieces; inspector load is based on 1.3 standard hours per 1000 pieces.
- Inspect yield is 92%. This is the net residue from CARBCOAT, SILCOAT, and INSPECT processes; i.e.:

  (tested and approved SOC panels) ÷ (uncrated substrates) = 0.92

IPEG-2 Estimates for Target Technology

The entries in Table 24 are direct costs for an annual production of 2.5 million square meters of sheet SOC, not adjusted for yield in cell fabrication and subsequent module manufacturing steps. Projected low-cost technology is postulated, as summarized by the listed assumptions.

Table 24. Cost data for target technology.

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	$ 34,358	649	$ 61,805	$ 687,800(a) 15,706,500(b)	$ 14,131
Silicon coating	8,405,947	3969	851,827	1,378,350(c) 8,881,464(d)	252,987
Inspect	501,500	2396	862,491	---	7,345
Total	$8,941,805	7014	$1,776,123	$16,531,650(e) $25,413,114(f)	$274,463

(a) Carbon, (b) substrates, (c) argon, crucibles, furnaces, insulation, (b) polysilicon, (e) excluding silicon, (f) including silicon.

Manufacturing prices estimates are based on the IPEG-2 formula:

$$\text{Price} = \left[\begin{matrix}0.57\\ \text{or}\\ 0.52\end{matrix}\right](\text{EQPT}) + 109(\text{SQFT}) + 2.8\,(\text{DLAB}) + 1.2\,(\text{MAT} + \text{UTIL})\Big] / \text{QUAN} \quad (77)$$

In our case, the EQPT coefficient, 0.52, applies to INSPECT, where the anticipated equipment life is 10 years; the coefficient 0.57 applies to the other two tasks, for which equipment life is 7 years. We have also applied the DLAB coefficient of 2.8 because our direct labor costs do not include fringe benefits. Reduced to price per square meter, the project technology estimates are:

$\$12.99/m^2$ added value
$\$17.25/m^2$, including silicon

For an assumed 11% encapsulated cell efficiency and subsequent processing yields (cell and module fabrication) totaling 94.5%[35], the respective costs on a peak watt basis are:

12.5 cents/W_p added value
16.6 cents/W_p including silicon

The price estimation formula can also be used to calculate price sensitivity data, or price changes resulting from a change in any cost input parameter. For illustration purposes, it is convenient to denote the cost input changes in terms of percent of nominal values. For example, a polysilicon price of \$16/kg would be expressed as:

$$\%_{SIL} = 100 \times \frac{16 - 14}{14} = 14.3\% \quad (78)$$

since the nominal price is \$14/kg. The price sensitivity is given relative to ceramic (CER) and silicon (SIL) costs, silicon coating time (SCT), coating machine cost (CMC), coating operator load (COL), and argon cost (ARG):

$$\begin{aligned}\$ = 17.25 &+ 0.0754\ \%_{CER} + 0.0426\ \%_{SIL}\\ &+ 0.0353\ \%_{SCT} + 0.0192\ \%_{CMC}\\ &+ 0.00954\ \%_{COL} + 0.00083\ T_{ARG}\end{aligned} \quad (79)$$

The sensitivities are the coefficients in Eq. 79, or the slopes of the corresponding graphs in Fig. 111. These graphs, of course, intersect at 0%, giving the nominal sheet value, $\$17.25/m^2$. The largest theoretically possible cost saving is represented by negative 100%, meaning that a particular parameter has zero cost value. Hence, the intercepts on the left-hand vertical axis give the hypothetical sheet price in the zero-coat limit (e.g., the "added-value" is seen as the silicon graph intercept) of $12.99.

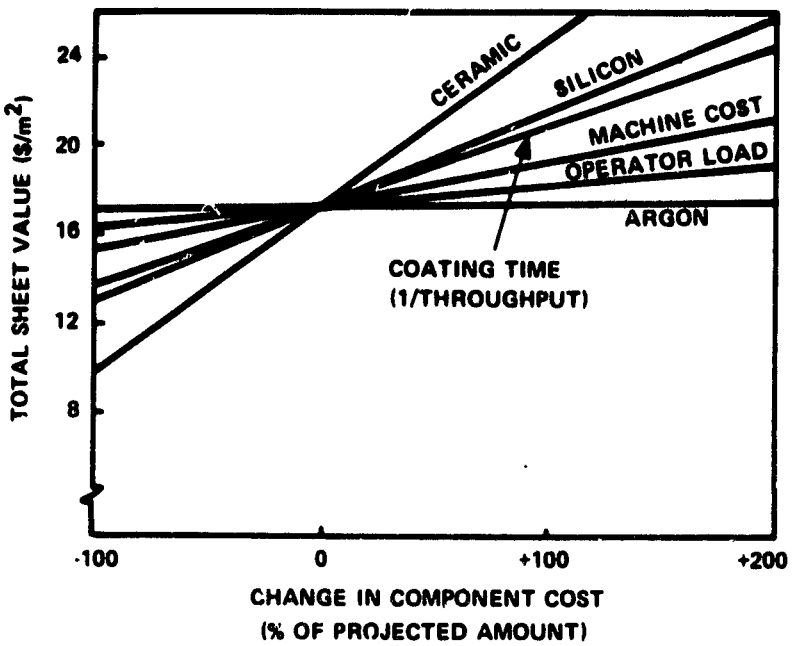

Figure 111. Sensitivity profiles for total sheet value according to projected technology. Abscissa represents relative (%) change in component cost (e.g., +100 and -50 denote doubling halving, respectively).

Progress-To-Date Technology

Another major category of economic analysis deals with progress-to-date technology instead of projected low-cost technology. A number of parameters have been changed to reflect our perception of progress-to-date, particularly with respect to silicon coating throughput and operator load. Throughput is based on a pulling speed of 0.0625 cm/sec, operator load is 0.5, and machines are placed two to a stack instead of six. Compared with projected technology, direct silicon coatings costs are thereby magnified

by the following factors:

- Coating machines x4
- Materials (except Si) x4
- Operators x24
- Floor space x12

Table 25 gives direct costs for progress-to-date technology, with the assumptions according to Table 24 except as modified above.

Table 25. Cost data for progress-to-date technology.

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	$ 34,358	649	$ 61,804	$ 687,800(a) 15,706,500(b)	$ 14,131
Silicon coating	33,623,788	47,628	20,443,848	5,513,400(c) 8,881,464(d)	252,987
Inspect	501,500	2,396	862,491	---	7,345
Total	$34,159,646	50,673	$21,368,144	$21,907,700(e) $30,789,164(f)	$274,463

(a) through (f): See Table 24.

Based on the values of Table 25, the IPEG2 formula yields:

$44.57/m^2 added value
$48.83/m^2, including silicon

For price per peak watt, we assume an encapsulated cell efficiency of 8.4% and a subsequent net processing yield of 94.5%:

56.1 cents/W_p added value
61.5 cents/W_p, including silicon

Price Allocation

A commercial readiness goal of 70 cents per peak watt has been set for the year 1986, to be met by one or more low-cost, flat-plate, solar voltaic concepts that have demonstrated technological readiness by 1982. The JPL Price Allocation Guidelines 35 were developed as a tool for estimating price goals for low-cost sheet silicon technologies, such as Cz ingot and slicing, HEM ingot and slicing, EFG, dendritic web, and SOC. The basic assemption is that a given set of price allocations will have been met by the other major (nonsheet) task categories. These allocations are stated in 1980 dollars per square meter as follows:

- Cell fabrication — $\$21/m^2$ of cells
- Encapsulation materials — $\$14/m^2$ of cells
- Module assembly — $\$14/m^2$ of module

Assuming the remaining prices are for sheet and silicon, an allocation for SOC can be calculated from:

$$\$/W\ (SOC) = \$/W\ total - \$/W\ cell - \$/W_p\ encaps\ materials - \$/W\ mod\ assembly \quad (80)$$

where

$$\$/W\ (SOC) = \$/W_p\ sheet + \$/W_p\ silicon \quad (81)$$

and \$/W (TOTAL) is the total module price, in dollars per peak watt. The price per peak watt can be expressed in terms of the price per m^2, the silicon thickness, t (mils), silicon yield, Y_{si}, cell yield, Y_{cell}, module yield, Y_{mfg}, packing efficiency, η_p, and encapsulated cell efficiency, η_e.

- Silicon:

$$\$/W = \$/kg \left(t \cdot u \cdot D\right)/\left(I \cdot \eta_e \cdot Y_{si} \cdot Y_{cell} \cdot Y_{mfg}\right) \quad (82)$$

- Sheet:

$$\$/W_p = \$/m^2\ sheet/\left(I \cdot \eta_e \cdot Y_{cell} \cdot Y_{mfg}\right) \quad (83)$$

- Cell:

$$\$/W_p = \$/m^2\ cell/\left(I \cdot \eta_e \cdot Y_{mfg}\right) \quad (84)$$

- Encapsulation Materials:

$$\$/W_p = \$/m^2 \text{ module}/\left(I \cdot \eta_e \cdot \eta_p\right) \quad (85)$$

- Module Assembly:

$$\$/W_p = \$/m^2 \text{ module}/\left(I \cdot \eta_e \cdot \eta_p\right) \quad (86)$$

where

Insolation (I) = 1000 W/m^2

Silicon density (D) = 2330 kg/m^2

Unit conversion (u) = 2.54×10^{-5} m/mil.

For SOC, Y_{si} = 0.80 and t = 4 mils. With the suggested values,[5] Y_{cell} = 0.95, Y_{mfg} = 0.995, and silicon cost of \$14/kg, Eq. 80 becomes

$$(0.00106\ \$/m^2 \text{ sheet} + 0.00438)/\eta_e = \$/W_p \text{ total} - (0.0211 + 0.0147 + 0.0147)/\eta_e \quad (87)$$

The left hand side of Eq. 87 is price per peak watt of sheet plus silicon. This equation is solved for the allocated sheet price, giving:

$$\$/m^2 \text{ sheet} = 943(\eta_e)(\$/W_p \text{ total}) - 51.8 \quad (88)$$

Figure 112 is a graph of $\$/m^2$ sheet as a function of η_e for cost goals of 70, 60, and 50 cents per peak watt. For η_e = 0.11, cost allocations are $\$20.82/m^2$ and $\$10.44/m^2$ for 70 cents and 60 cents per peak watt, respectively. Equation 88 can also be used to calculate the required encapsulated cell efficiency to meet a given $\$/W_p$ total, assuming $\$12.99/m^2$ as found from our IPEG-2 analysis of the projected technology:

- 70 cents/W_p requires η_e = 9.8%
- 60 cents/W_p requires η_e = 11.5%
- 50 cents/W_p requires η_e = 13.7%

Summary

The projected added-value cost of SOC is $\$12.99/m^2$, with the substrate material accounting for 58% of this amount and the actual silicon coating process contributing 29%. The remaining 13% is attributable to carbon coating and inspection. Of the silicon coating costs (29%), the relative

amount by the SAMIS categories are:

- Capital Equipment 50%
- Labor 25%
- Materials (non-silicon) 17%
- Manufacturing Space 5%
- Electricity 3%

All of these except electricity (i.e., 28% of the added value) scale inversely as the silicon-coating throughput, which is thus a major cost driver after substrate cost. (See also Fig. 111.)

The $\$12.99/m^2$ figure is consistent with the 70 cents/W_p target, assuming an encapsulated cell efficiency of at least 9.8%. For 60 cents or 50 cents/W_p, the efficiency would be required to be at least 11.5% or 13.7%, respectively.

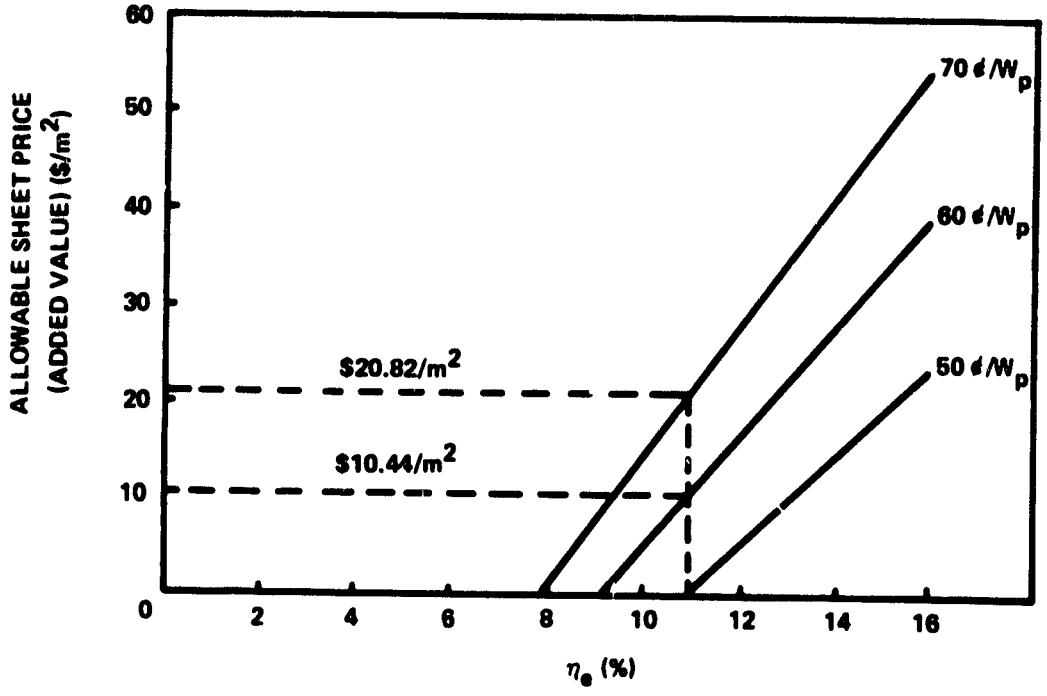

Figure 112. Allocated sheet price vs. encapsulated cell efficiency. Numerical values are shown for $\eta_e = 0.11$.

CONCLUSIONS

From the work performed during this R&D program, we conclude that:

- Silicon sheets of solar-cell quality can be produced by the SOC process, whereby thin layers of silicon are coated onto one surface of large-area ceramic (mullite) substrates.
- Large-area ($1000cm^2$) mullite substrates, which contain slot openings for electrical contact purposes, can be inexpensively produced in large quantities.
- Such substrates can be compositionally modified to obtain a thermal expansion coefficient which is similar to that of silicon. The slight dissimilarity leaves the silicon coating in a state of compression.
- The SOC material can be satisfactorily produced by either a dip-coating or a continuous SCIM-coating process.
- If the coating throughput rate of the SOC silicon sheet process is increased to 350 cm^2/min, the process falls within DOE's 1986 economic goals.
- Carbon can be inexpensively applied to one surface of the substrate using a colloidal carbon suspension.
- Thin SOC layers, by virtue of unidirectional solidification, contain columnar silicon grain as large as 5mm in width and several cm long.
- The single grains are heavily twinned, but the twin boundaries as well as the normal boundaries are, in general, perpendicular to the surface of the layer.
- The SOC coatings are predominately {331} surfaces with a growth direction of <211>. This texture permits {111} twin planes to occur perpendicular to the substrate and propagate as the grain grows. This texture is similar to that observed in EFG ribbon silicon.[26]
- The silicon-ceramic bond is mechanical in nature and has proven to be highly dependable in practice.

- Slot openings in the substrate which are perpendicular to the growth direction can be satisfactorily covered with silicon with very little perturbation of the grain structure.
- The thickness of the layer is inversely related to the melt temperature and is also proportional to the inverse of the coating speed squared when the heat of fusion is removed from the growing layer by radiation alone.
- Experimentally, it was demonstrated that with additional convective cooling, coating rates commensurate with the project's economic goals are achievable.
- The mullite substrates are slightly soluble in molten silicon, causing the melt to become progressively contaminated with the dip-coating process. This is minimized with the SCIM technique by reducing the contact time and area the substate has with the melt.
- The surfaces of SOC coatings are smooth and shiny and need no further preparation other than a standard cleanup procedure prior to forming the p-n junction.
- SOC solar cells can be reproducibly produced with an average conversion efficiency of 9.6% (AM1, AR).
- The slot openings in the ceramic substrates must cover approximately 50% of the total substrate area to avoid the introduction of serious series resistance in the finished solar cell.
- The highest conversion efficiency of a dip-coated SOC cell was 10.54% (AM1, AR).
- The highest conversion efficiency of a SCIM-coated SOC cell was 7.6% (AM1, AR).
- The highest efficiencies were produced with a PH_3 diffusion at 850°C, following by a slow cooldown at about 3°C/min.
- Theoretical modeling of SOC solar cells shows that present cell performance is limited by diffusion length, and that 13% SOC cells are possible with a diffusion length of 50μm.

- The average diffusion length (L) in SOC material is 15 to 25μm. The diffusion length within good grains is three times the average diffusion length, L. Closely spaced grain boundaries, high dislocation densities, and subsurface grain boundaries have been identified as structural causes of the reduction in L.

- Cost estimates of the SOC process are $\$13/m^2$ added value, or $\$17.25/m^2$ including silicon at \$14/kg. Based on 11% module efficiency, this corresponds to a sheet cost of 16.6 cents/W_p. The analysis shows that the cost of ceramic is the largest cost driver in the SOC process.

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APPENDIX A
EVALUATION OF SILICON-ON-CERAMIC MATERIAL FOR LOW-COST SOLAR CELLS*

SUMMARY

In silicon-on-ceramic (SOC) solar cells, the short-circuit current is less than that of single-crystal solar cells because of (1) recombination at the grain boundaries, and (2) recombination within grains. These two effects can be separated by light-beam-induced-current (LBIC) measurements of the short-circuit current using a finely focused scanned beam from a monochromator. At any point on the surface of a cell, an effective minority-carrier diffusion length can be determined from the spectral response at long wavelengths (0.8 to 1.0μm). At each grain boundary, an effective surface recombination velocity can be determined. The LBIC technique was used to evaluate the effectiveness of hydrogen plasma treatment for reducing grain boundary recombination in SOC material.

INTRODUCTION

The silicon-on-ceramic (SOC) process produces thin layers of silicon on inexpensive ceramic substrates.[A-1] Layers are produced by unidirectional solidification of molten silicon, and are polycrystalline with grain widths on the order of a millimeter and lengths of several centimeters. SOC layers have been produced by a dip-coating technique as well as by a "Silicon-Coating with Inverted-Meniscus" (SCIM) technique.[A-2] Solar cells made from SOC material have demonstrated 10.5% conversion efficiencies (AM1), using ELH lamp simulator.

To improve the efficiency of SOC solar cells, it is important to assess the relative importance of grain boundaries and impurities. To separate these two effects, light-beam-induced current (LBIC) measurements of the short-circuit current have been made using a micron-sized light beam from a monochromator. The LBIC measurements are closely related to solar cell performance, since the technique identifies the various spatial and spectral contributions to solar cell current.

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*Paper by J. D. Zook, Honeywell Corporate Technology Center, Bloomington, MN. Published in Proc. of 1980 Photovoltaic Solar Energy Conf., Cannes, France (1980), p. 569.

PROCEDURE

The experimental arrangement is shown in Fig. A-1. The exit slit of a monochromator is focused on a pinhole aperture which in turn is focused on the sample by a 15X, N.A./0.28 reflecting objective. For maximum resolution, the spot width on the sample can be reduced if the image of the exit slit does not fill the pinhole. Viewing of the sample is done with a pellicle beamsplitter and viewing eyepiece. Scanning is done with a motor-driven stage on which the sample is mounted. The absolute spectral quantum efficiency, Q_λ, is determined from the ratio of the sample current to that of a calibrated, highly uniform silicon photodiode inserted in front of the sample.

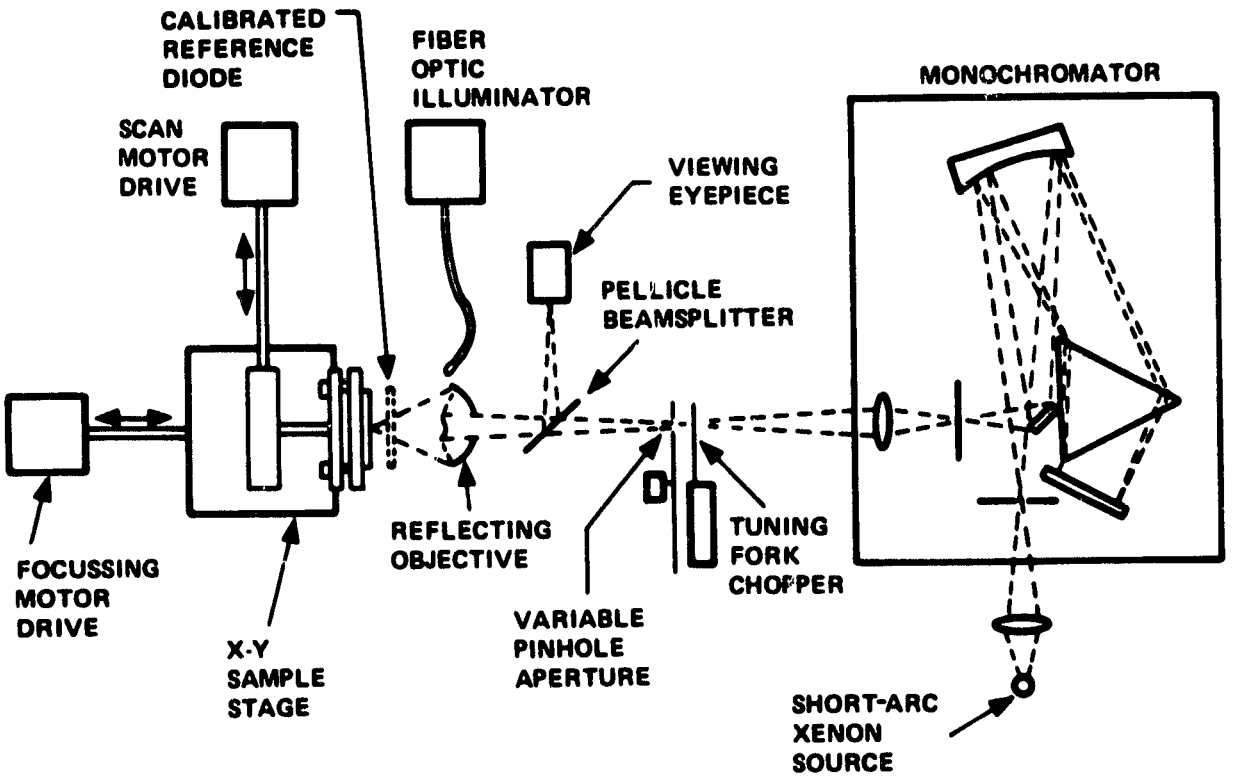

Figure A-1. Schematic design of the LBIC system. The chopper is optional and was not used for the results reported in this paper.

From a knowledge of Q_λ at any given wavelength in the near-IR, the value of minority-carrier diffusion length, L, can be determined. It is convenient to use the peaks in the spectrum of the xenon lamp (see Fig. A-2). For cells

that are thick compared with the penetration of light,[A-3] the quantum efficiency is given by:[A-3]

$$Q = \frac{(1 - R)\,\alpha_\lambda L}{1 + \alpha_\lambda L}$$

where R is reflectivity and α_λ is the absorption coefficient. Unfortunately, R varies from sample to sample because of variations in the oxide thickness. In order to deduce R from the data, the values of L determined at each wavelength are averaged, and the standard deviation of δL is determined. The value of 1 - R is then chosen to give the lowest relative error, $\delta L/L$. This procedure gives reasonable values of R for antireflection-coated (AR) cells as well as for uncoated cells.

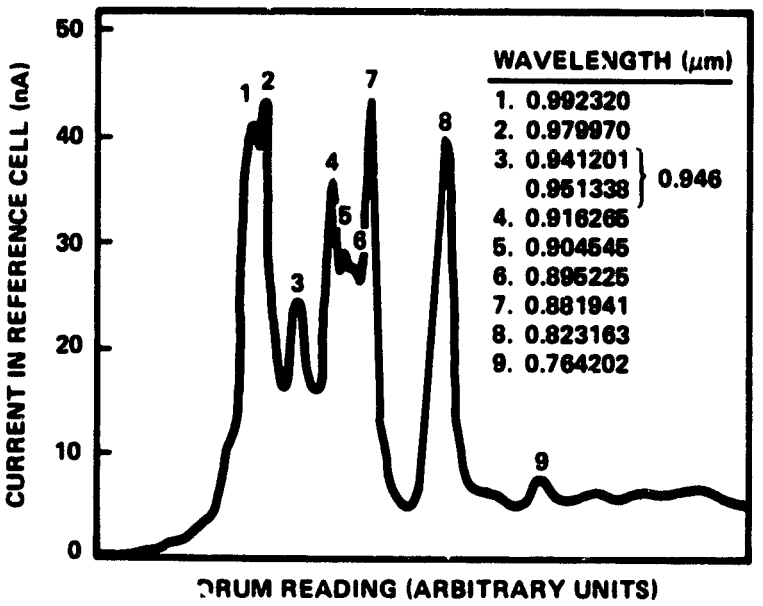

Figure A-2. Spectrum of the 150W xenon lamp used in the experiment. The wavelengths are handbook values for low-pressure xenon discharges.

The value of L depends on the values assumed for α_λ. The most reliable published data in the region of interest (0.76 to 1.0μm) appear to be those of Runyan [A-4] and of Weakliem and Redfield [A-5], whose results do not differ significantly. Average values of α_λ at the strongest peaks of the xenon lamp are given in Table A-1.

Table A-1. Inverse absorption lengths.

λ(μm)	α_λ^{-1}(μm)
0.992	125
0.980	100
0.946	59
0.916	38
0.882	26
0.823	14

At the long wavelengths, $\alpha_\lambda L \ll 1$ in Eq.(A-1)and the LBIC response provide a direct mapping of the effective diffusion length. By integrating the LBIC response for a cross-grain scan (across the narrow dimensions of the grains), an average value, L, can be determined for the whole cell.

RESULTS

LBIC scans of an SOC cell at five wavelengths are shown in Fig. A-3. The scans include four well-isolated grain boundaries. The light spot size was about 5μm x 12μm, with the narrow dimension perpendicular to the grain boundaries to give maximum resolution. Interestingly, the depths of the

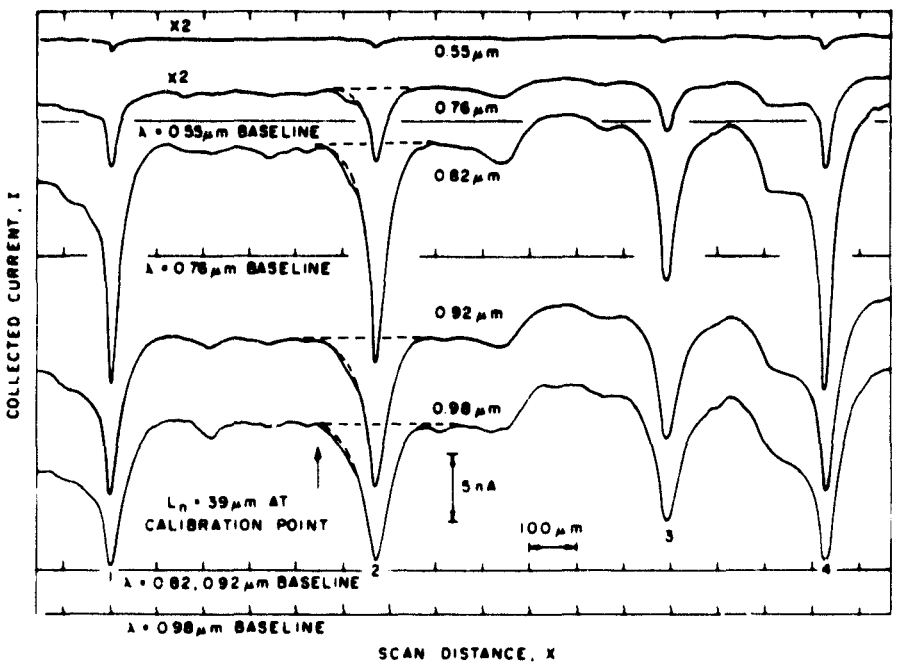

Figure A-3. Typical LBIC scans on SOC material. The dashed lines at grain boundary 2 indicate the limits used in deriving the integrated current loss at the grain boundary.

minima at the grain boundaries are not sensitive to the spot size or shape, as evidenced by the fact that the scan is virtually the same even when the spot is significantly out of focus. The signal-to-noise ratio in the d-c system is greater than 100:1 inside the grains. The intensity of the light spot is between one to two suns for the wavelengths of Table A-1. The value of L = 39μm within a grain was deduced by the procedure given above.

An important issue in modeling grain boundary recombination is the question of linearity of the boundary conditions at the grain boundaries. Because the potential barrier heights at grain boundaries depend on the density of filled traps, it is reasonable to expect that grain boundary recombination velocity, s, might depend on the light intensity.[A-6] An experiment was performed to evaluate the effect of light intensity on grain boundary recombination. The beam was attenuated with neutral-density filters, and the quantum efficiency was measured within grains and at grain boundaries. The result showed no change in Q within grains over the range 0.01 to 10 suns, and about a 10% increase in Q at grain boundaries over the same range. These results imply that s is essentially constant, so that the principle of superposition should be valid. Thus, the short-circuit current of the cell is given by the focused spot (LBIC) response, integrated over the cell area, and over the solar spectrum.

Since s is constant, the analytical theory of LBIC reponse [A-7] is applicable to SOC material. The normalized value of s is given by S = sL/D, where D is the minority-carrier diffusivity. The parameter S can be evaluated by integrating the total loss in current due to a grain boundary.[A-7] For grain boundary 2 in Fig. A-3, this is the area within the dashed lines. The results of the procedure are shown in Fig. A-4. Each data point in Fig. A-4 represents a different wavelength, and each data point is consistent with a value of S = 25, corresponding to $s = 1 \times 10^5$ cm/sec, which is typical of SOC material.

LBIC scans of a number of SOC cells show that there is a characteristic "good-grain" diffusion length, L_{max}, which is dependent on doping and cell processing. We assume that L_{max} provides a measure of the chemical defects density (density of intragrain impurities with deep-level electron states). There is also a characteristic "worst case" grain boundary diffusion length, L_{min}, which is typical of many of the grain boundaries. The value of L_{min} is lower than the value of L at isolated grain boundaries (as in

Fig. A-3), and is typically a factor of 10 or 20 less than the value of L_{max}.

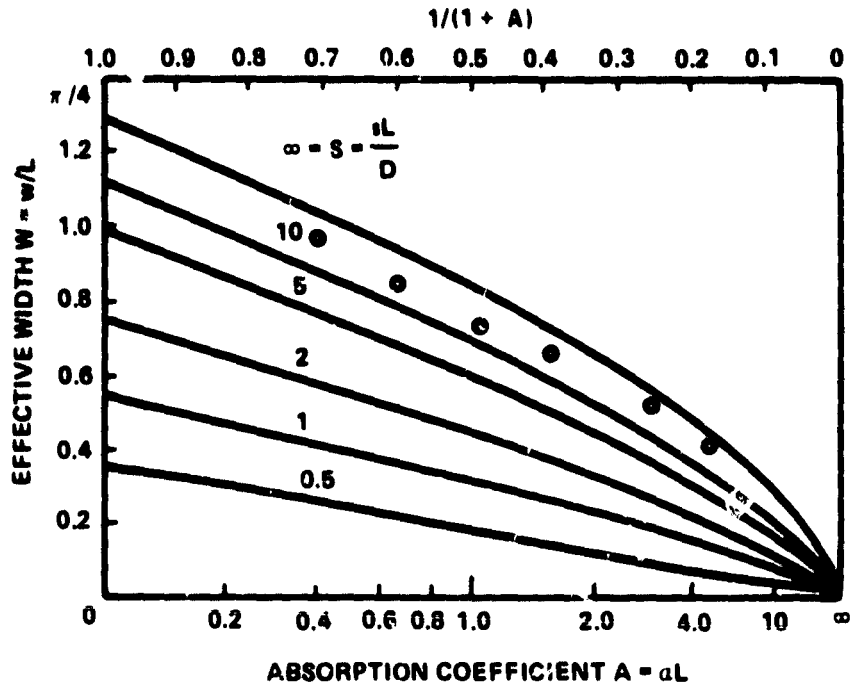

Figure A-4. Effective width, w, of a grain boundary as a function of absorption coefficient, following Ref. A-7. The effective width times the length of the boundary gives the equivalent loss in cell area for the short-circuit current.

Effective diffusion lengths are strongly influenced by structural defects. Low values of L are usually observed in regions having closely spaced grain boundaries that are readily visible on the top surface. In most cells, there are also regions which have an LBIC response lower than that which would be expected by examination of the top surface. In order to understand the reasons for such poor response, samples have been cut, polished, and etched to reveal the subsurface structure. In some cases, this structure reduces the value of L. More frequently, however, the low values of L are associated with high dislocation densities ($>10^5/cm^2$) and dislocation clusters at stacking faults.

The average diffusion length, L, evaluated from the integrated LBIC response, is typically one-third of L_{max}. From the theoretical relationship between L and J_{sc}, it follows that J_{sc} is reduced by 11 to 16% due to structural defects. Typically, this reduction is greater than the reduction due to the difference between L_{max} and the values of L in semiconductor-grade Czoch-

ralski material. Thus, structural defects appear to be more important than chemical defects in limiting the performance of present SOC solar cells.

The LBIC technique has also been used to evaluate grain boundary passivation in SOC material. The hydrogen passivation treatment was performed by C. Seagar and D. Ginley at Sandia Laboratories.[A-8] The LBIC scans before (B) and after (A) hydrogen treatment are shown in Fig. A-5. The overall increase in Q is due to an inadvertant oxide that was present after hydrogenation. It is clear that different degrees of passivation occur at different grain boundaries but that most grain boundaries are significantly

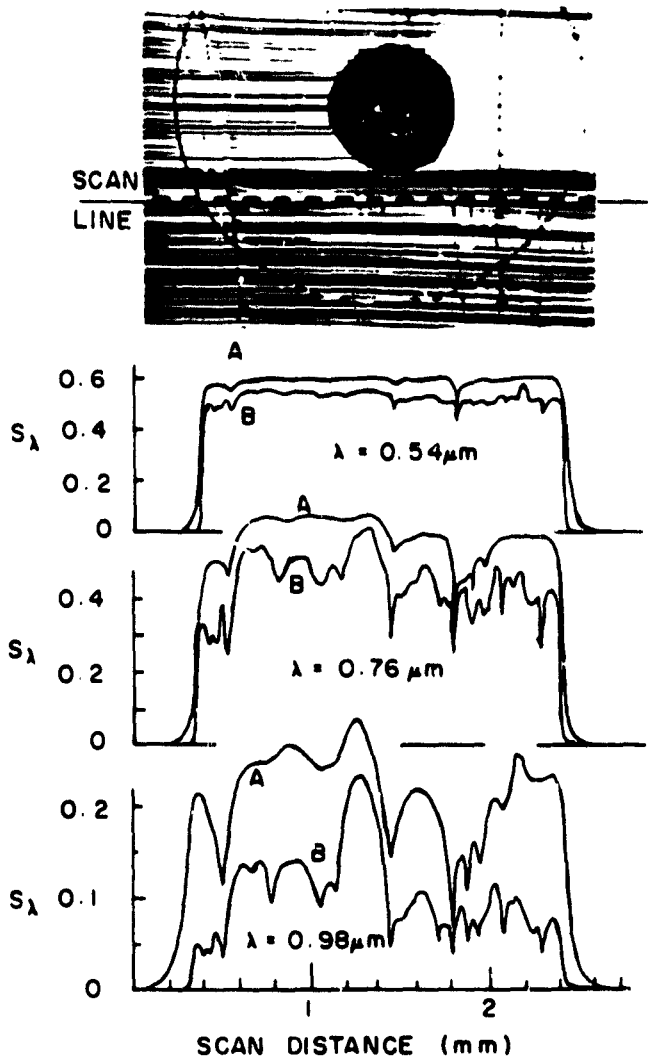

Figure A-5. Effect of hydrogen plasma threatment in LBIC response at three wavelengths. In the photo at the top, the horizontal lines are growth striations; vertical lines are grain boundaries. Scans before AR coating are denoted by B; after, by A.

improved. It is interesting to note that the nonuniformity within a grain is also reduced by hydrogen treatment. Correlations of LBIC response within grains are due to variations in dislocation densities. Thus, hydrogenation apparently also reduces recombination at dislocations.

In summary, the LBIC technique is a useful tool for evaluating diffusion lengths within grains, grain boundary recombination velocities, the effects of processing on cell performance, and the relative importance of structural defects vs. chemical defects in limiting performance of polycrystalline silicon solar cells.

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A-4 W. R. Runyan, Final Report, NASA Grant NGR44-007-016, Southern Methodist University, (1968).

A-5 H. A. Weakliem and D. Redfield, J. Appl. Phys. 50, 1491 (1979).

A-6 H. C. Card and E. S. Yang, IEEE Trans. Elec. Dev. ED-24, 397 (1977).

A-7 J. D. Zook, Appl. Phys. Lett. 37, 223 (1980).

A-8 C. H. Seagar, D. S. Ginley and J. D. Zook, Appl. Phys. Lett. 36, 831 (1980).

APPENDIX B
PARASITIC RESISTANCE ANALYSIS

INTRODUCTION

The integration of our sheet silicon with a nonconducting substrate presents a special problem in making the electrical contacts to the base layer. These connections could be made at the front surface, in which case the active photovoltaic regions would have to be confined to small mesa structures. The relatively high non-active surface fraction would seriously reduce the module efficiency. Back surface contacts are possible only through slots or holes in the substrate. Since these contacts are necessarily stripes or dots rather than continuous area, the photocurrent must traverse a longer average path from the junction to the back contacts. The series resistance of the base layer therefore can not be neglected. The purpose of this appendix is to (a) predict the consequences of parasitic series resistance with respect to the cell efficiency, and (b) estimate a tolerable limit on electrode spacing based on calculated series resistances in the solar cell.

The basic electrical structure of the silicon-on-ceramic (SOC) concept is illustrated in cross section in Fig. B-1. For definiteness, an n^+ on p structure is assumed, giving the cell polarity shown in the figure. The illuminated front surface is provided with regularly spaced striped electrodes which are modeled as a top metallic layer contacting the n^+ diffused layer through an intermediate metal-semiconductor interface. The interface is characterized by a specific contact resistivity, ρ'_c, in ohms-cm^2. Photogenerated minority carriers which diffuse to, and transverse the junction, are responsible for the photocurrent. This photocurrent enters the structure through the interconnected (negative) front contacts, spreads through the diffused layer, crosses the junction, and converges through the base layer to the (positive) back contacts. A carbonized layer on the ceramic substrate is approximately in the plane of the front surface of the substrate, and connections are brought out through slots in the ceramic. This is at variance with an earlier representation (SOC Annual Report No. 2), where it was assumed that the silicon would fill the slots up to the back surface of the substrate and the electrical contacts would be in the plane of that surface. However, our experience with both dip-coated and SCIM-coated substrates has shown the present version to be correct. The spacings of the

two sets of contacts are not necessarily the same. It is presumed throughout the report that the back contact spacing, b, may exceed the front contact spacing, b', and the ratio b/b' can be any positive number. A unit of the periodic structure will be taken as the b x w rectangular area bounded by the lines centered on adjacent back electrodes, and having arbitrary width, w, perpendicular to the plane of Fig. B-1. Current flow is assumed everywhere parallel to the plane of Fig. B-1. This amounts to ignoring the collecting effect of the contact bars which connect the stripes.[B-1]

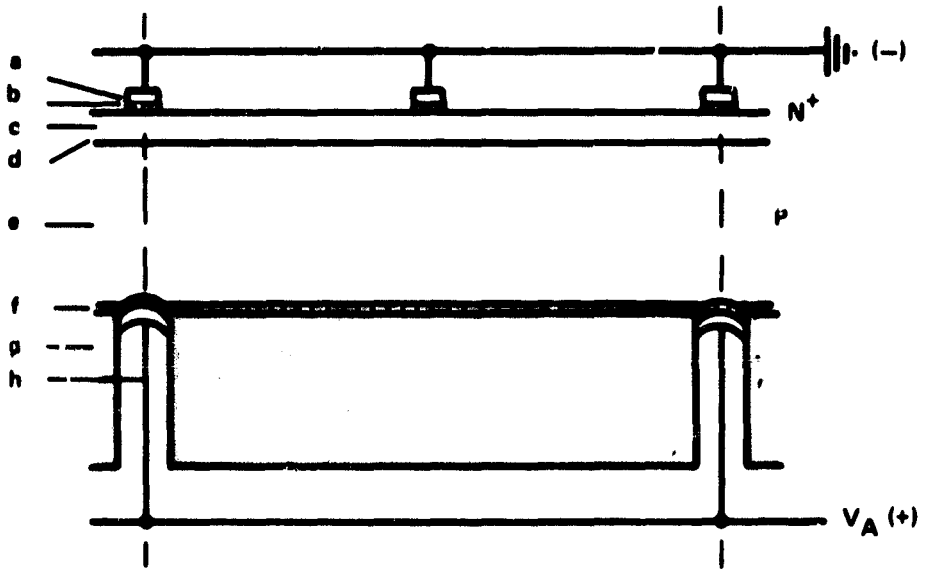


Figure B-1. One unit of the periodic structure of an SOC cell. Features (not drawn to scale): (a) contact metal; (b) metal-semiconductor interface; (c) diffused layer; (d) junction; (e) base layer; (f) carbon layer; (g) ceramic substrate; (h) external connection.

Parasitic resistances occur at contact interfaces and in the front and back (diffused and base) layers. These not only reduce the maximum power available to the load, but shift the maximum power point toward both lower voltage and lower current density. This may be illustrated qualitatively by means of Fig. B-2. The upper curves gives the hypothetical ideal illuminated cell characteristic (no parasitic losses). In this case, the load voltage is the same as the voltage, V_D, across the junction, here assumed to be uniform. Maximum power density (product $V_D J$) is labelled W_o^*. The lower curve represents a particular non-ideal characteristic due to a specific

[B-1] R. J. Handy, "Theoretical Analysis of the Series Resistance of a Solar Cell," Solid State Electronics 10, 765 (1967).

parasitic resistance, R_p. The available load voltage differs from V_D by the series IR drop; i.e., $V_A = V_D - J$ bw R_p. Maximum power density on this curve is labelled W^*.

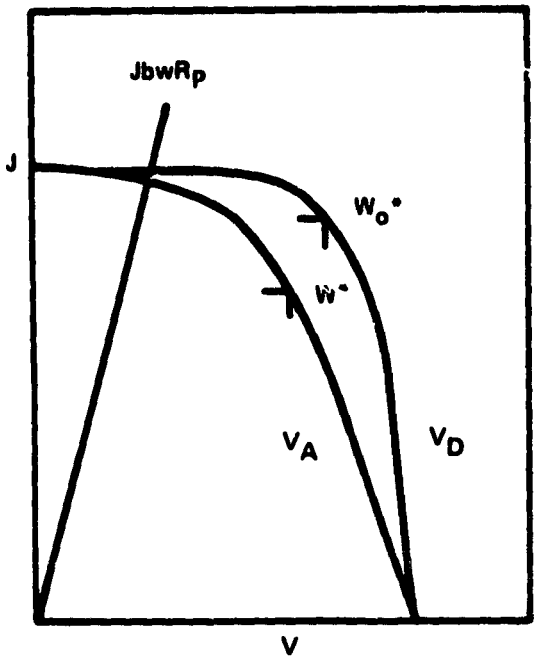


Figure B-2. Determination of optimum solar cell operating point according to lumped model for parasitic resistances.

The foregoing illustration makes use of two assumptions: that the internal resistances can be lumped and that V_D and J are constant along the junction. These assumptions cannot be strictly true due to the obviously distributed nature of the device. The parasitic IR effect varies from a maximum at the middle of a unit to near zero at the ends so that V_D is not exactly constant. Moreover the bulk and contact components of the resistance are not strictly separate because of so-called current crowding in the semiconductor layers near the contacts. Fortunately, if certain reasonable auxiliary conditions are satisfied, the assumptions are justified to a good approximation. Specifically, the dissipated power should be relatively small, and the contact spacings b and b´ should be large compared with the diffused-layer thickness and base-layer thickness, respectively, and the metallized areas should be small fractions of the total area.

In the subsections that follow, an approximate lumped-resistance model is developed and some of its implications with respect to cell performance are discussed.

THE SOLAR CELL JUNCTION PARAMETERS

The illuminated solar cell characteristic (Fig. B-2) is assumed to following the single-exponential model:[B-2]

$$J = J_o - J_1 (e^{AV_D} - 1) \qquad \text{(B-1)}$$

locally at any given point in the junction plane*. J_o is the illuminated short-circuit current density and J_1 the reverse-saturation current density. The parameter A has an ideal theoretical maximum of $q/kT = 38.7$ volt^{-1} but in silicon solar cells is always considerable smaller. J_o, J_1, and A are strongly dependent on the material and junction fabrication technology. The choice of numerical values is therefore somewhat arbitrary and subject to speculation. This should be borne in mind when interpreting the calculated results included in this report. The output may depend critically on the parameters. The present choice is based on short-circuit density = 0.03 a/cm^2, open-circuit voltage = 0.55V, and A = 30. This value of J_o corresponds to AM1 sunlight and is not corrected for reflection losses. J_1 is then found to be

$$J_1 = J_o/(e^{AV_{oc}} - 1) = 2.05 \times 10^{-9} \text{ a/cm}^2 \qquad \text{(B-2)}$$

These parameters yield a power density maximum = 12.9 mW/cm^2 and fill factor = 78%.

[B-2] H. J. Hovel, Solar Cell Semiconductors and Semimetals, Vol. II, K. K. Willardson and A. C. Beer, Eds., Academic Press, N.Y., Chap. 3.

*The depletion-layer width may not be negligible. However, the word "plane" here implies that current passes through the depletion layer perpendicular to its boundaries and with negligible ohmic effects.

POWER DISSIPATION

The ideal performance figures are degraded in practice by series and shunt parasitic resistances and by front electrode masking. The shunt component is not included here, since its causes [B-3] are related more to diode fabrication than to device geometry considerations and should therefore respond to improved processing techniques. Electrode masking is omitted also; if the masked area is not too great, a multiplicative masking factor on J_o should serve this purpose within the accuracy of the model.

Dissipation occurs serially through front contact interfaces (R_c'), front silicon layer (R_L'), back silicon and carbon layers (R_L), and back contact interfaces (R_c). The lumped equivalent circuit for a single-cell unit is shown in Fig. B-3, and total parasitic resistance is $R_p = R_c' + R_L' + R_L + R_c$.

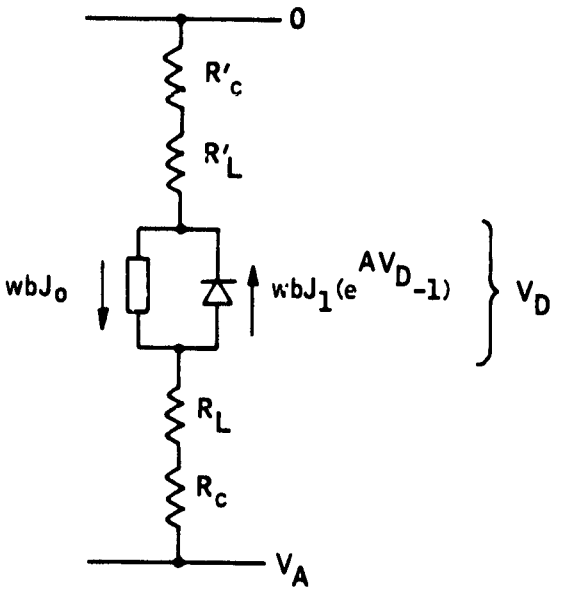


Figure B-3. Lumped components of parasitic resistance of a cell unit.

B-3 Hovel, op. cit., p. 50.

The operating characteristic J vs. V_A for a given R_p (lower curve of Fig. B-2) may be expressed parametrically in terms of the junction voltage, V_D, as

$$J = J_o - J_1 \left(e^{AV_D} - 1\right) \tag{B-3}$$

$$V_A = V_D - bwJR_p, \quad 0 \le V_D \le V_{oc} \tag{B-4}$$

The desired operating point is obtained by maximizing the product JV_A with respect to V_D. This gives the following condition on V_D, which is easily solved numerically:

$$\left\{J_o - J_1\left[e^{AV_D} - 1\right]\right\}\left\{1 + 2J_1 Ae^{AV_D} \cdot bwR_p\right\} - AV_D\, J_1 e^{AV_D} = 0 \tag{B-5}$$

The power density decreases as the cell width b increases for two reasons. First, for a fixed R_p, the cell current increases with b, causing the IR_p drop to increase. Second, R_p itself increases with b. The first effect is demonstrated in Fig. B-4, where maximum available power density is

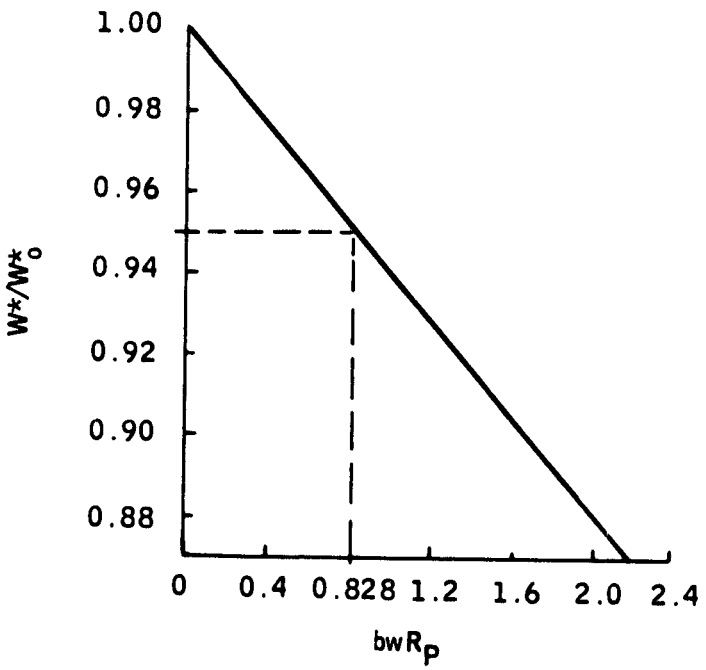


Figure B-4. Maximum available power density (relative) as a function of cell area times R_p

plotted as a fraction of the ideal 12.9 mW/cm^2 (R_p = 0). From this plot, it can be seen that bwR_p must be restricted to 0.83 ohm-cm^2 or less, to keep the relative efficiency from falling below 95%. More specific inferences may be drawn from this arbitrary criterion after the components of R_p have been quantitatively identified.

COMPONENTS OF PARASITIC RESISTANCE

Front Contact Resistance

For convenience, it will be assumed that b/b′ is an integer ≥ 1, so that the front area contains b/b′ (see Fig. B-5) subunits per cell unit. From the symmetry of a subunit, assuming uniform J, it is obvious that the cell current bwJ is shared equally by 2b/b′ half-contacts each with area equal to d′w/2. According to the extended transmission line model (ETLM),[B-4, B-5] the series resistance due to one of these strips is approximately

$$(h'/w) \cdot R_{\square}' \cdot \sqrt{\eta' + 0.2}\ \coth\left\{(d'/2h')/\sqrt{\eta' + 0.2}\right\} \qquad \text{(B-6)}$$

$$\eta' = \rho_c'/\left[(h')^2 R_{\square}'\right]$$

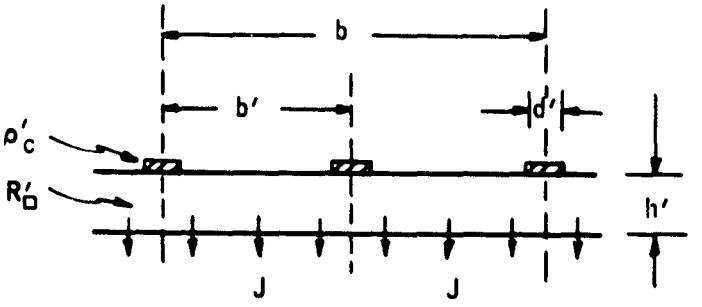


Figure B-5. Front subcell geometry for the case b/b′ = 2 (distorted scale).

B-4 H. H. Berger, "Models for Contacts to Planar Devices," Solid-State Electronics 15, 145 (1972).

B-5 H. H. Berger, "Contact Resistance and Contact Resistivity," J. Electrochem. Soc. 119, 507 (April, 1972).

where $R_{\square}'$ is the sheet resistance (ohms/square) of the n^+ layer and ρ_c' is the specific contact resistivity (ohms-cm^2) of the contact interface. Since the 2b/b' half-contacts are in electrical parallel, the net front contact resistance for the cell unit is

$$R_c' = (b'/2b)(h'/w) \cdot R_{\square}' \cdot \sqrt{\eta' + 0.2} \cdot \coth\left\{(d'/2h')\sqrt{\eta' + 0.2}\right\} \quad (B-7)$$

Front Silicon Layer Resistance

The subunit of area wb' is modeled here as a sheet with current Jwb'/2 entering at each edge and exiting with uniform density, J, through the surface (junction).

If positive current is from left to right and x is the coordinate measured from edge to edge ($0 \le x \le b'$), the sheet current in the present approximation is

$$I(x) = wJ\,(b'/2 - x) \quad (B-8)$$

and the voltage relative to the edges, not including the voltage drop in the contacts, is

$$V(x) = -\frac{1}{w} R_{\square}' \int_0^x I(z)dz = -JR_{\square}'(b'x - x^{2})/2 \quad (B-9)$$

The minus sign is required because positive current flows away from the edges. The power dissipated in the subunit is

$$P' = \int_0^{b'} \left| wJV(x) \right| dx = J^2 R_{\square}' wb'^3/12 \quad (B-10)$$

The front layer resistance is power (for the whole bxw unit) divided by the square of the current:

$$R_L' = (b/b')P'/(wbJ)^2 = \left(\frac{1}{12}\right)\left(\frac{b}{w}\right)\left(\frac{b'}{b}\right)^2 R_{\square}' \quad (B-11)$$

Back Layer Resistance

Because of the direction of current from the junction toward the back contacts, the voltage in the back layer increases toward the center of the unit.

By a one-dimensional model analogous to the one in the preceding subsection, the back surface voltage relative to the silicon side of the back contacts is

$$V(x) = JR_{\square}(bx - x^2)/2 \qquad \text{(B-12)}$$

where $R_{\square}$ is the sheet resistance of the base layer.

Dissipated power is

$$P = J^2 R_{\square} wb^3/12 \qquad \text{(B-13)}$$

and back layer resistance is

$$R_L = \left(\frac{1}{12}\right)\left(\frac{b}{w}\right) R_{\square} \qquad \text{(B-14)}$$

Back Contact Resistance

The analysis of front contact resistance applies also to the back contacts. There are in this case, however, only two half-contacts per unit cell, each with area equal to dw/2. In terms of the base layer thickness, h, sheet resistance, $R_{\square}$, and specific contact resistivity, ρ_c, the back contact resistance is

$$R_c = \left(\frac{1}{2}\right)\left(\frac{h}{w}\right) R_{\square} \sqrt{\eta + 0.2}\ \coth\left\{(d/2h)/\sqrt{\eta + 0.2}\right\} \qquad \text{(B-15)}$$

where $\eta = \rho_c/\left(h^2 R_{\square}\right)$.

ESTIMATION OF CONTACT SPACING

According to Fig. B-4, the area resistance product, bwR_p, should be restricted to the order of 1 ohm-cm^2. Using Eqs. (B-7), (B-11), (B-14), and (B-15), one can calculate bwR_p as a function of b and then estimate maximum allowable b. This will depend on base layer resistivity through both base sheet resistance and back contact resistance, if aluminum contacts are used on p-type silicon. In this case, ρ_c depends upon the silicon bulk resistivity.[B-5] Three different base-layer resistivities are considered: ρ_B = 0.3, 1.0, and 3.0 ohms-cm. The n+ layer is assumed to be 0.3μm thick with a sheet resistance of 50 ohms/square. The front contact length, d′, is 0.3mm, and $\rho_c = 10^{-5}$ ohm-cm^2. The base-layer thickness is 125μm, and the back contact length, d, is 0.8mm in accordance with the substrate slot width. Back contact resistivity[B-5] is $5 \times 10^{-4}\ \rho_B$ ohm-cm^2, where ρ_B is the bulk resistivity

of the p-type silicon. From Eqs. (B-7), (B-11), (B-14), and (B-15), we calculate

$$R_c' = 0.01122/w$$
$$R_L' = 4.17\ b/w$$
$$R_L = 0.0833\ R_\square\ b/w \qquad \text{(B-16)}$$
$$R_c = 0.00306\ R_\square\ /w$$

where $R_\square = \frac{\rho_B}{h} = 24$, 80, and 240 ohms/square.

The total $bwR_p = bw\ (R_c' + R_L' + R_L + R_c)$ is plotted in Fig. B-6. For bwR_p not to exceed 1.0 ohm-cm^2, the slot separation can be as much as 4mm for $R_\square = 24$, but should be held to 2 or 3mm for more lightly doped base material.

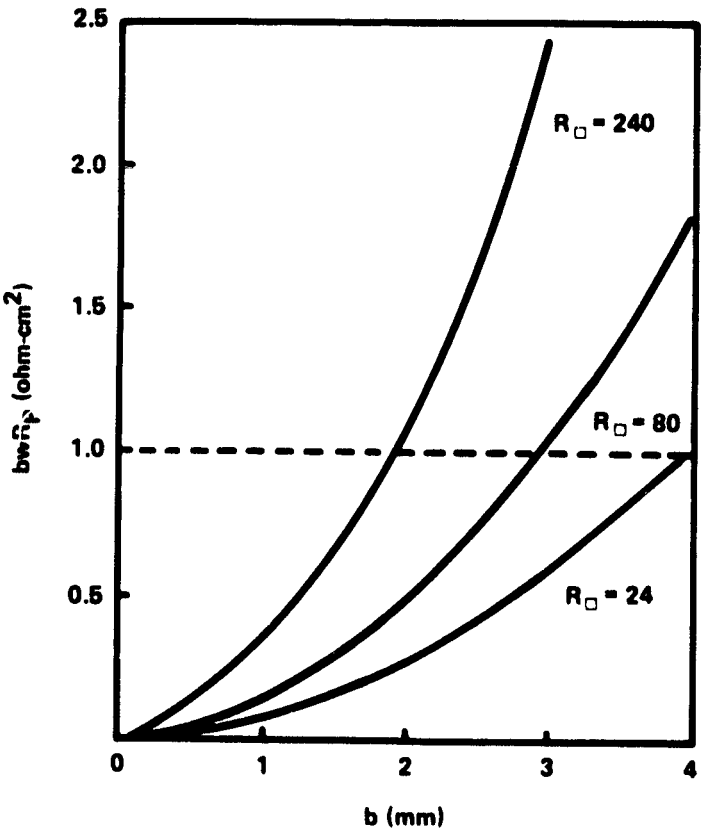


Figure B-6. $bwR_\square$ product vs. b for solar cells made on slotted ceramic substrates.

CIRCULAR CONTACTS

A possible alternative to striped electrodes is a two-dimensional square lattice of small circular electrodes as shown in Fig. B-7. Various methods might be used to produce such a pattern. One method of making small, roughly circular holes in the ceramic, while at the same time creating troughs in the back ceramic surface through which contacts to the holes can be made, is illustrated in Fig. B-8.

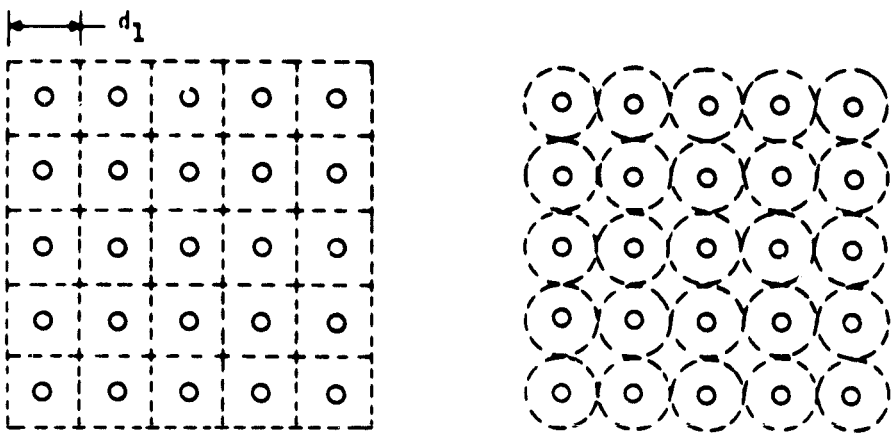


Figure B-7. Partial lattice of electrodes with square basic units (left). In the derivation of Eq. (B-17), the square units are approximated in circles (right).

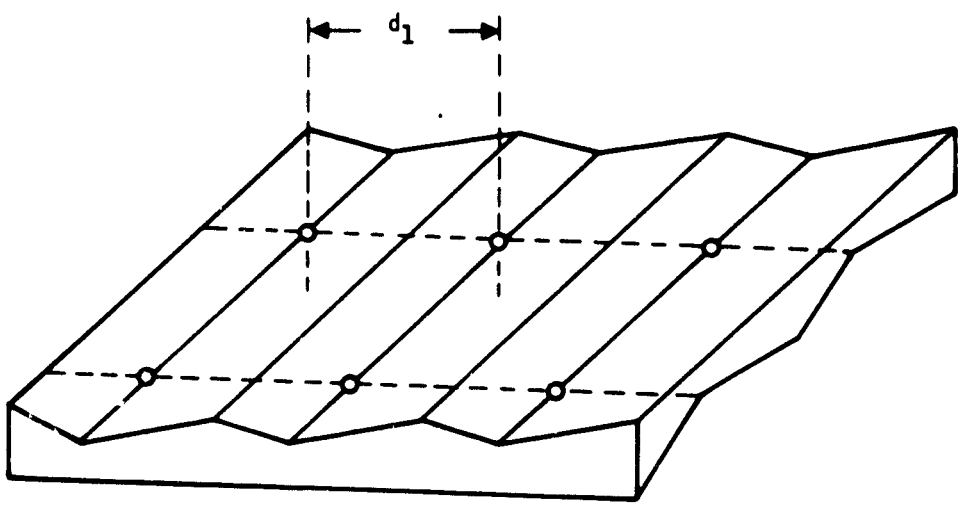


Figure B-8. Holes at the intersection of perpendicular sets of troughs in the front and back ceramic surfaces.

Neglecting variation in the thickness of the silicon layer that might result from such a geometry, we have approximated the square fields of Fig. B-7 as roughly equivalent circular fields in order to estimate the series resistance. If d_o and d_1 are the diameters of contacts and circular fields, respectively, it can be shown that the RA product for an effective sheet resistance, $R_\square$, is:

$$RA = R_\square \left(d_1^2/8\right)\left[\ell n(d_1/d_o) - 1/4\left(1 - d_1^2/d_o^2\right)\left(1 - 3d_1^2/d_o^2\right)\right] \qquad \text{(B-17)}$$

and this equation is plotted in Fig. B-9. One may note, for example, that RA = 1.5 ohms-cm^2 if d_o = 0.3mm, d_1 = 3mm, and $R_\square$ = 50 ohms/square.

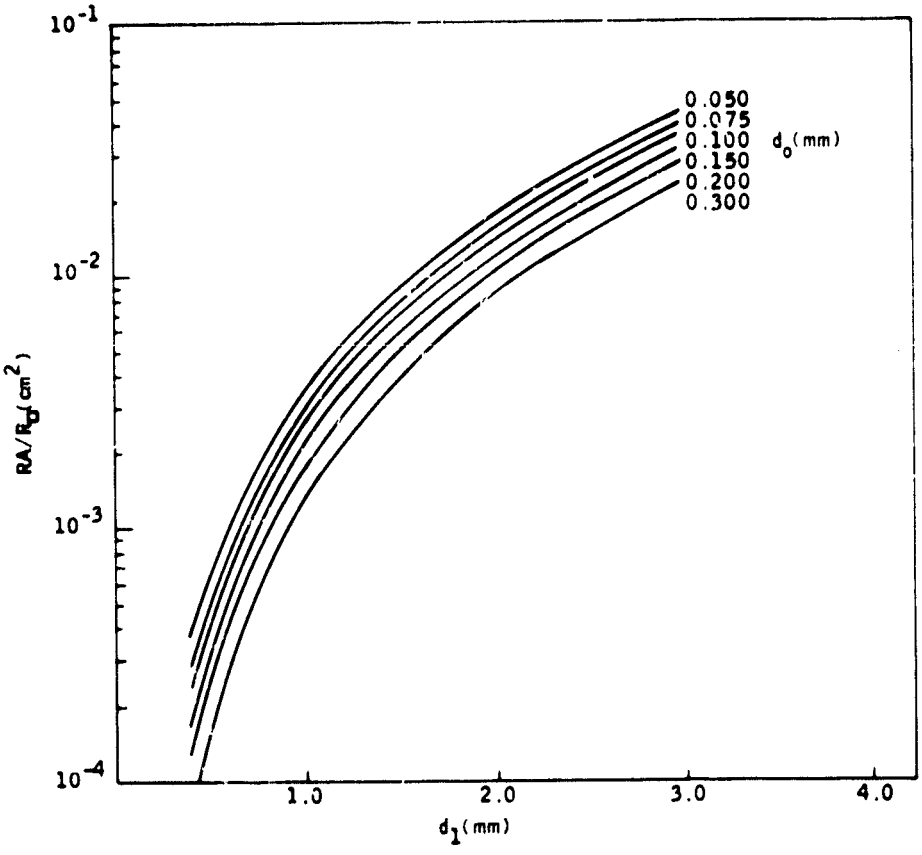


Figure B-9. $RA/R_\square$ from Eq.(B-16) for the circular base field geometry.

The contribution to RA due to contact resistance can be shown to be comparatively small. For this term, we use the transmission line model[B-4] for circular geometries:

$$(RA)_{contact} = \left(\pi d_1^2/4\right)\left(\sqrt{R_\square \rho_c}/d_o\right) J_o(j\alpha d_c/2) \; / \; \left[-jJ_1(j\alpha d_o/2)\right] \qquad \text{(B-18)}$$

where J_o and J_1 are the Bessel functions of orders 0 and 1, respectively, $j = \sqrt{-1}$, ρ_c is the specific constant resistivity, and $\alpha = R_\square / \rho_c$. For $R_\square$ = 50 ohms/square and ρ_c = 0.0005 ohm-cm^2, one finds $(RA)_{contact} \approx 0.2$ ohm-cm^2.

The RA product, including contact resistance, is therefore approximately 1.7 ohms-cm^2, comparing favorably with the striped geometry of equivalent (0.3cm) spacing. For both types of geometry, the RA product will fall rapidly as the spacing is reduced.

APPENDIX C
NOVEL CELL DEVELOPMENT

Because silicon-on-ceramic (SOC) material is on an insulating substrate, it is difficult to fabricate an electrical contact to the base region of the cell. At the start of this work, the base contact was made by using an interdigital electrode pattern on the top surface. This method was obviously undesirable since the pattern covered too much area. Later in the program, a novel high-voltage structure (suggested by Dr. G. Turner of JPL) was investigated as an alternate technique for achieving contact to the base layer as well as providing a higher terminal voltage.

The high-voltage structure is fabricated as follows: Carbon stripes are deposited on a ceramic substrate. The substrate is then dip-coated with silicon so that the carbon stripes are perpendicular to the surface of the melt. The resulting silicon stripes, after diffusing a p-n junction, can be series-connected to form a high-voltage structure. The active area of this structure is only one-half of the total area. To offset this area loss, an integral optical coupler (IOC) is added as illustrated in Fig. C-1.

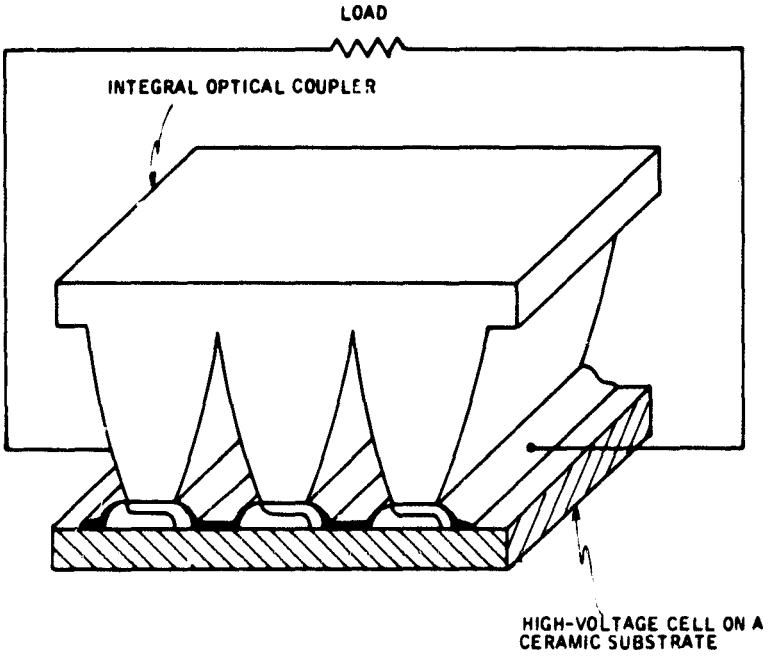


Figure C-1. Combined integral optical coupler high-voltage cell device.

This IOC is a cylindrical, trough-like, dielectric-compound, parabolic concentrator having a concentration ratio of 3. As compared with the interdigital electrode cell, the high-voltage structure allows efficient collection of incident light even though all metal contacts are located on the top surface of the structure. The incident light, of course, is concentrated primarily on the active area. Because the short-circuit current, J_{sc}, of the cell increased by a factor of 2 when the optical coupler was added, the cell was designated the 2X cell."

2X cells fabricated from striped SOC material had conversion efficiencies from 4 to 6% (AM1, no AR coating). The major problem was an undesirably high series resistance.

In parallel with this novel cell study, a slotted-substrate method for contacting the back surface of the cell was developed. This method is discussed in detail in the Technical Discussion section of this report.

In this appendix, the series resistance of the 2X structure and the slotted-substrate structure will be calculated. Cross-sectional views of these devices are shown in Fig. C-2.

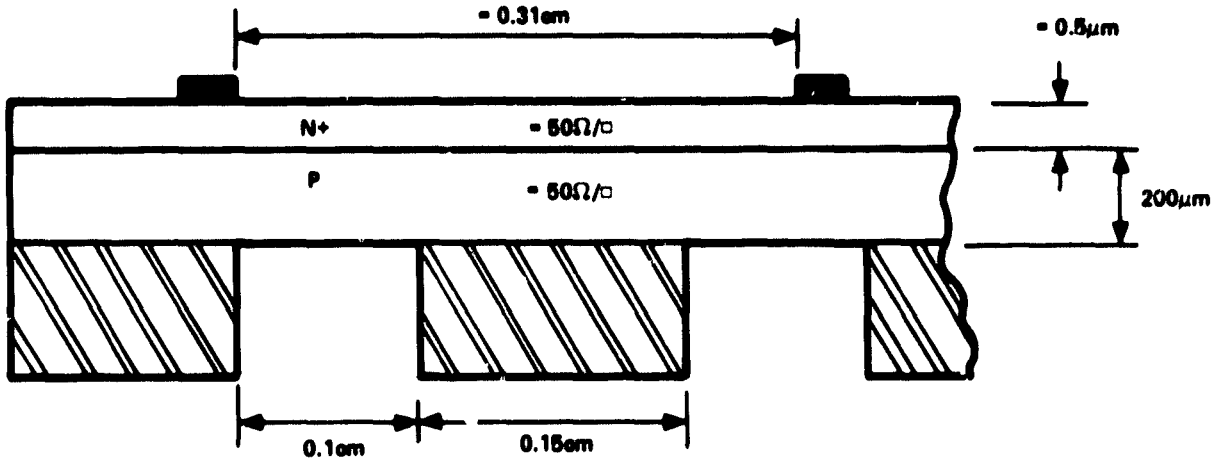
For the slotted-substrate cell, the parasitic series resistance, R_p, can be divided into three components: the front contact resistance, R_c'; the silicon-layer resistance, R_L'; and the back-layer resistance, R_L. The back contact resistance can be neglected. The front-contact resistance, R_c', is assumed to be given by

$$R_c' = R_\ell'/\ell \qquad \text{(C-1)}$$

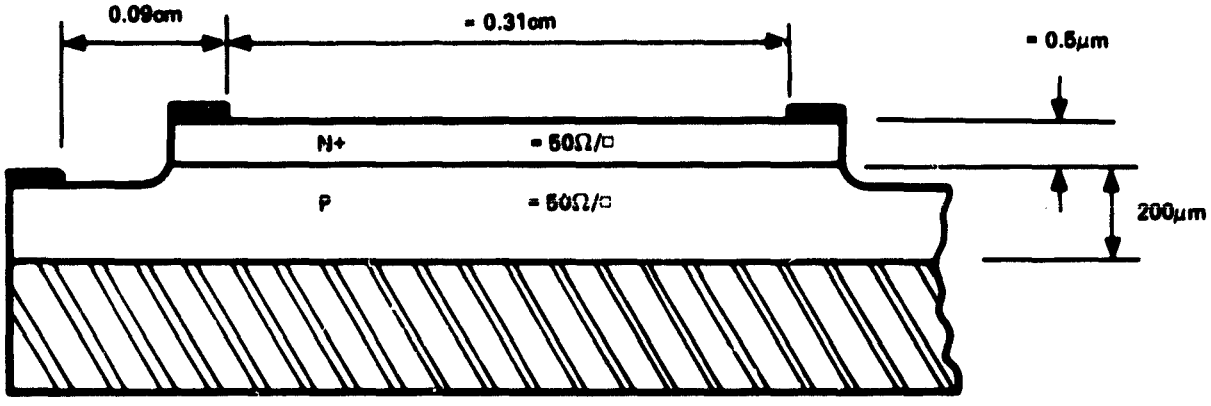
where ℓ is the peripheral length of the emitter metallization pattern and R_ℓ' is the specific contact resistance in ohms-cm. An accurate value of R_ℓ is not known; we assume here that $R_\ell' = 0.3$ ohm/cm. Thus, $R_c' = 0.013$ ohm, since $\ell = 24$cm. The front silicon-layer resistance, R_L', is given by

$$R_L' = \frac{1}{12} R_\square' \left(\frac{b' - k'}{N' w}\right)$$

where $R_\square'$ is the front-layer sheet resistance in ohms/square, b' is the unit cell width, k' is the width of a contact finger, N' is the number of unit cells per solar cell, and w is the width of the solar cell For a typical



(a) Slotted-substrate SOC cell.



(b) 2X SOC cell.

Figure C-2. Cross-sectional drawings of a slotted-substrate SOC cell and a 2X-SOC cell.

SOC cell, $R'_{\square}$ = 50 ohms/square, b' = 0.34cm, k' = 0.03cm, N' = 7.06, and w = 1.7cm, given that R_L' = 0.108 ohm. For the back-layer resistance, R_L, we use the following equation:

$$R_L = \frac{R_{\square}}{(Nb)\,w}\left[\frac{b^2}{12}\left(1 - \frac{d^2}{b}\right)^2 + h^2\left(\frac{b}{d}\right)\right] \qquad \text{(C-3)}$$

where $R_{\square}$ is the sheet resistance of the back layer, b is the center-to-center distance between slots, d is the slot width, h is the thickness of the back layer, N is the number of slots per solar cell, and w is the width of

the solar cell. Thus, (Nb)w is the total area of the solar cell. By making two assumptions, we can rewrite Eq. (C-3) in terms of base doping concentration, N_B, and growth speed, v. First, we assume that base sheet resistivity, which equals $R_\square h$, is inversely proportional to N_B. Thus,

$$R_\square h = K/N_B \tag{C-4}$$

where K is an empirical constant. For SOC material with a base doping concentration, N_B, of $2.3 \times 10^{16}/cm^3$, $R_\square h$ is about 1 ohm-cm, given that $K = 2.3 \times 10^{16}/cm^3$. Second, we assume that the silicon thickness, h, is inversely proportional to the square of the growth velocity, v. Thus,

$$h = K^*/v^2 \tag{C-5}$$

where K* is an empirical constant. For a growth speed of 0.06 cm/sec, h is about 200μm. Thus, K* is about $7.2 \times 10^{-5} cm^3$. For a typical SOC cell, b = 0.25cm, d = 0.1cm, and $(Nb)w = 4.08cm^2$, so that Eqs. (C-3). (C-4), and (C-5) combine to give

$$R_L = \frac{1.49 \times 10^{13}}{N_B} \left(v^2 + \frac{6.912 \times 10^{-6}}{v^2} \right) \tag{C-6}$$

Because the total parasitic resistance, R_p, equals $R_c' + R_L' + R_L$, the specific series resistance, R_pA, is given by

$$R_pA = 0.494 + \frac{6.07 \times 10^{17}}{N_B} \left(v^2 + \frac{6.912 \times 10^{-6}}{v^2} \right) \tag{C-7}$$

since $A = 4.08cm^2$. Equation (C-7) yields the data in Table C-1.

Now we turn to the 2X-cell, which is illustrated in Fig. C-3. The values of R_c' and R_L' are assumed to be double the corresponding values for the slotted-substrate SOC cell. The back-layer resistance, R_L, is given by

$$R_L = \frac{1}{12} R_\square \frac{\ell}{Nw} + \frac{1}{2} R_\square \frac{s}{Nw} \tag{C-8}$$

where R_D is the sheet resistance of the back layer, ℓ is the width of the active region of the unit cell, N is the number of unit cells per solar cell, w is the width of the solar cell, and s is the lateral distance from the edge of the active region to the edge of the base contact. By Fig. C-1, R = 50 ohms/square, ℓ = 0.31cm, N = 4, w = 1.7cm, and s = 0.09cm. Thus, R_L = 0.52 ohm, R_p = 0.76 ohm, and the specific series resistance of the 2X cell is 3.2 ohms-cm^2. This value is too high for high-efficiency cells.

Table C-1. Specific series resistance vs. base doping concentration and thickness

v (cm/sec)	h (μm)	Specific Series Resistance (Ω-cm^2)		
		Base Doping Concentration (cm^{-3})		
		2.3×10^{16}	10^{16}	4.7×10^{15}
0.06	200	0.64	0.83	1.21
0.07	147	0.66	0.88	1.31
0.08	113	0.69	0.95	1.46

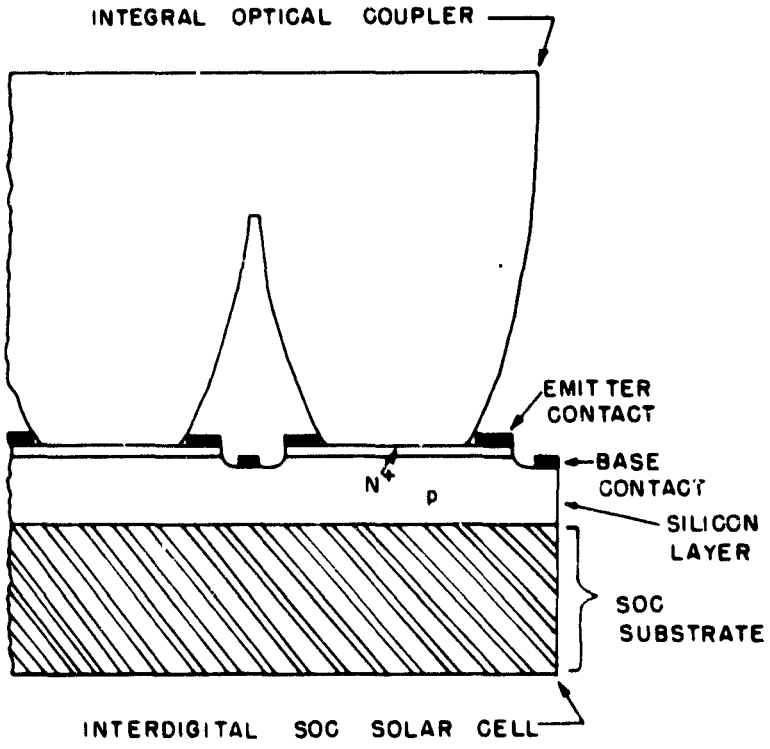


Figure C-3. The 2X-cell.