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# A 10–kW SERIES RESONANT CONVERTER DESIGN, TRANSISTOR CHARACTERIZATION, AND BASE–DRIVE OPTIMIZATION

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16. Abstract

The Westinghouse D60T and developmental D7ST transistors are characterized for use as switches in resonant circuit applications. A base drive circuit to provide the optimal base drive to these transistors under resonant circuit conditions is developed and then used in the design, fabrication and testing of a breadboard, space-borne type 10-kW series resonant converter.

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## TABLE OF CONTENTS

## LIST OF ILLUSTRATIONS

# SECTION 1

## INTRODUCTION

To meet the goals of multi-hundred-kilowatt space power systems planned for the middle and late 1980s, advanced power processing technology is required to convert the power available from solar arrays or other space-borne power sources to the various voltage and/or current levels required by the spacecraft loads. This technology can be built on the series resonant conversion technology that has been brought to a high state of development with the use of thyristors as the basic switching element. However, new technology is needed to increase the power level and improve the performance. The use of transistors in place of the thyristors promises to meet both of these goals. Although present thyristors offer higher power capabilities than transistors, their losses are higher, their operating frequency is limited, and additional protection and commutation circuitry is required.

The present contractual program was established to develop transistorized series resonant conversion technology at the 10-kW power level. As a first step in this development, the switching characteristics of the Westinghouse D60T and developmental D7ST transistors required measurement for sinusoidal collector current conditions. Switching characteristics are normally measured with a resistive load where the collector current has a square-pulse type of waveform. In a resonant converter, however, the current is switched on by the transistor, and thereafter varies as a sinusoid.

It is the unusual condition of half-sinusoid collector current with the transistor in saturation that makes conventionally measured switching parameters unsuitable for dynamic analysis of series resonant circuits. Manufacturers have not, as yet, begun to characterize their power switches for use in this type of application. Therefore, it was first necessary to obtain the proper transistor parameters before proceeding to the design and development of the converter.

The 10-kW power level is the next logical step in the development of series resonant converter technology, which is presently at the 2.5-kW level for space-borne systems. The goals of this program were to develop a single-stage 10-kW converter employing transistors as the switching elements, having an input-voltage range of 230 to 270 Vdc, and output-voltage range of 200 to 500 Vdc, and an output current-limit range of 0 to 20 A.

## SECTION 2

## SUMMARY

Two types of new bipolar switching transistors (the Westinghouse D60T and D7ST) were characterized for use as switches in series resonant inverters and/or converters. They were characterized at 20, 30, 50, and 70% of their rated collector currents (200 A for the D60T and 500 A for the D7ST) and at resonant frequencies of 10, 20, and 40 kHz. The collected data show that the D60T is approximateldy three times faster than the D7ST, having a storage time in the range of 1.5 to 2.0 μsec, as opposed to 5 to 6 μsec for the D7ST. The data also indicate that the D60T gets into hard saturation faster than the D7ST, and that neither is suitable for operation at 70% of its rated collector current at a resonant frequency of 40 kHz. Data were obtained for: base drive parameters to minimize total device dissipation, minimum required base drive as a function of $I_c$, base drive parameters for maximum operating frequency, delay time, rise time, storage time, fall time, saturation voltage, and output capacitance and input capacitance under series resonant conditions.

Using the data obtained in the transistor characterization, a base-drive circuit was designed and tested to provide the optimal base-drive to these transistors when they are used as switches in series resonant applications. This base-drive circuit provides regenerative feedback, a large amplitude leading-edge current pulse, a large amplitude turn-off current pulse, and reverse base-emitter bias during the transistor off-time.

With this base-drive circuit as one of the building blocks, a series resonant converter was designed, fabricated, and tested to operate from a 230 to 270 Vdc input bus, and provide a minimum output power of 10-kW (500 V at 20 Adc). This circuit has a resonant frequency of 25-kHz, an output ripple of 1.5% peak-to-peak, regulation of better than 0.2%, a response time of less than 2 msec, and its output can be either constant voltage or constant current. The electrical efficiency measured was 91% at its full-power level of 500 V and 20 A, and 93.7% at a half-power load of 500 V and 10 A. Full circuit details of the converter are presented, along with the test data.

## SECTION 3

## TRANSISTOR CHARACTERIZATION

Five Westinghouse D60T and five Westinghouse D7ST transistors were tested and characterized for use as switches in a Series Resonant Converter. The tests were performed using the test circuit of Figure 1 for the D60T transistors, and the test circuit of Figure 2 for the D7ST transistors. These test circuits imposed sinusoidal collector current on the transistor under test while allowing the base-drive characteristics to be varied. The base drive consisted of regenerative (or proportional) feedback of the collector current, a leading edge pulse, and a trailing edge pulse. Tables 1 and 2 list the peak collector currents, resonant frequencies, and test-circuit parameters for which the transistors were tested. The D60Ts were not tested at 140 A and 40 kHz and the D7STs were not tested at 350 A and 40 kHz because the saturation voltages were prohibitively high under these conditions (greater than 6 V).

The base-drive parameters that were varied during this testing were the amplitude of the leading-edge pulse, the duration of the leading-edge pulse, the regenerative-feedback turns ratio, and the amplitude of the trailing-edge (negative $I_B$) pulse. The transistors were tested in both a saturated and unsaturated condition. For the unsaturated condition, diode CR4 of Figures 1 and 2 was connected to the collector of the transistor under test and was disconnected for the saturated condition. The peak $I_C$ value listed in Tables 1 and 2, for the unsaturated condition, was actually the peak current in the tank circuit, since under this condition the collector current of the transistor was the sum of the tank current and diode CR4's current. One of the D7ST transistors (number 13) developed a collector-to-emitter short approximately 10 sec after being installed in the test setup; therefore, no data on it is available.

Figure 3 shows some typical base drive waveforms and defines the base drive parameters. The following sections discuss each parameter that was measured and give a summary of the data collected.

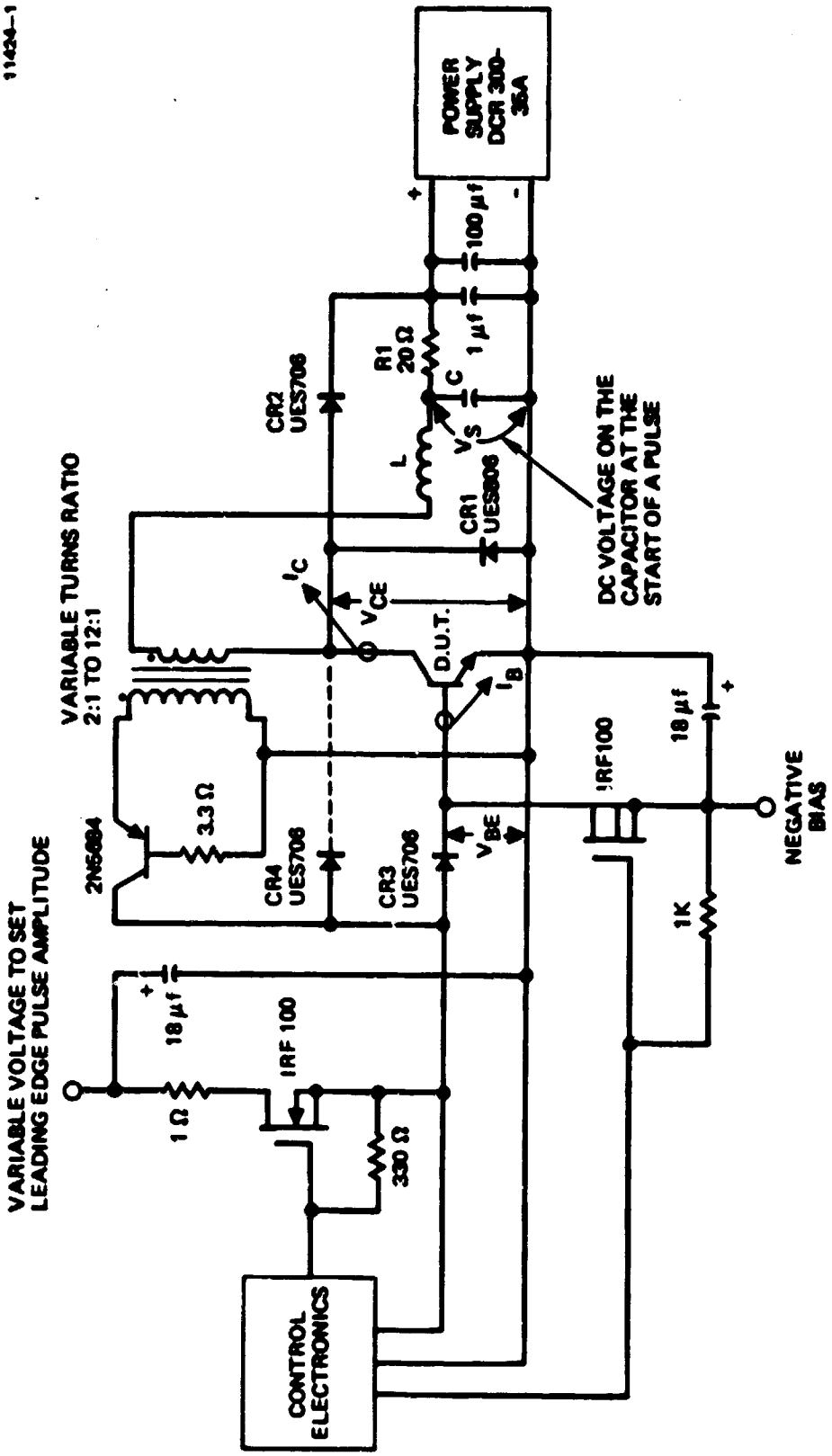


Figure 1. Circuit for testing the D60T transistors.

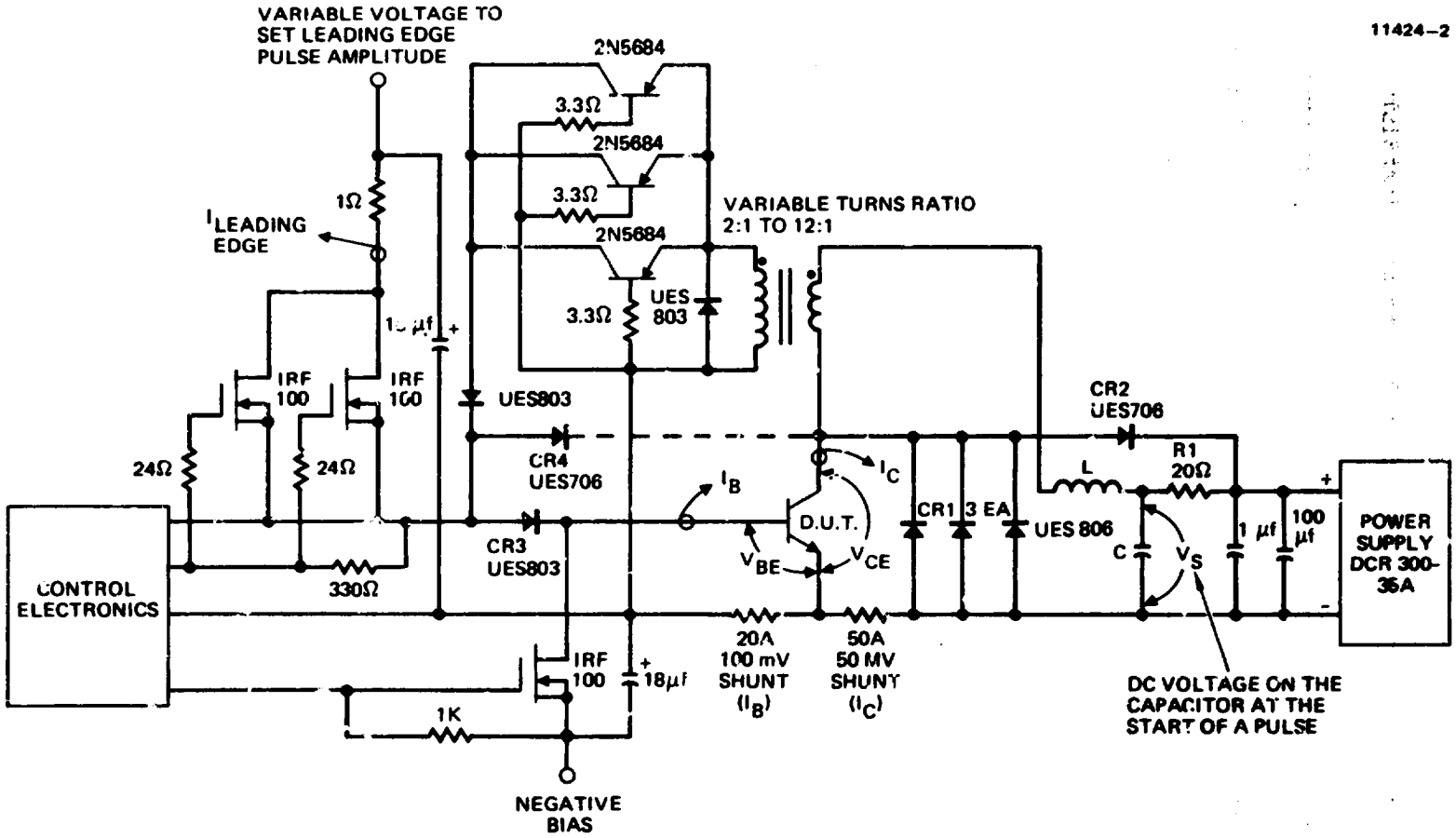


Figure 2. Circuit for testing the D7ST transistors.

TABLE 1. TEST CIRCUIT PARAMETER VALUES FOR THE D60T TRANSISTORS

| Peak Ic, A. | Resonant Frequency, fr, KHz | L μH | C μF | Vs Volts | Rep. Rate kHz |
|---|---|---|---|---|---|
| 40 | 10 | 18.6 | 12 | 50 | 5.0 |
| 60 | 10 | 18.6 | 12 | 75 | 5.0 |
| 100 | 10 | 18.6 | 12 | 135 | 2.5 |
| 140 | 10 | 18.6 | 12 | 180 | 2.5 |
| 40 | 20 | 17.8 | 3 | 95 | 10.0 |
| 60 | 20 | 17.8 | 3 | 145 | 10.0 |
| 100 | 20 | 8.1 | 6 | 130 | 5.0 |
| 140 | 20 | 8.1 | 6 | 185 | 5.0 |
| 40 | 40 | 6.7 | 2 | 80 | 10.0 |
| 60 | 40 | 6.7 | 2 | 120 | 10.0 |
| 100 | 40 | 4.3 | 3 | 140 | 10.0 |

TABLE 2. TEST CIRCUIT PARAMETER VALUES FOR THE D7ST TRANSISTORS

| Peak Ic, Amps | Resonant Frequency, fr, kHz | L, μH | C, μF | Vs Volts | Rep. Rate kHz |
|---|---|---|---|---|---|
| 100 | 10 | 20.5 | 12.100 | 128 | 2.5 |
| 150 | 10 | 20.5 | 12.100 | 190 | 2.5 |
| 250 | 10 | 10.0 | 24.400 | 165 | 1.0 |
| 350 | 10 | 10.0 | 24.400 | 230 | 1.0 |
| 100 | 20 | 10.0 | 6.080 | 130 | 5.0 |
| 150 | 20 | 10.0 | 6.080 | 190 | 5.0 |
| 250 | 20 | 5.0 | 12.100 | 165 | 2.5 |
| 350 | 20 | 5.0 | 12.100 | 240 | 2.5 |
| 100 | 40 | 5.0 | 3.025 | 140 | 10.0 |
| 150 | 40 | 5.0 | 3.025 | 200 | 10.0 |
| 250 | 40 | 2.8 | 6.080 | 170 | 5.0 |

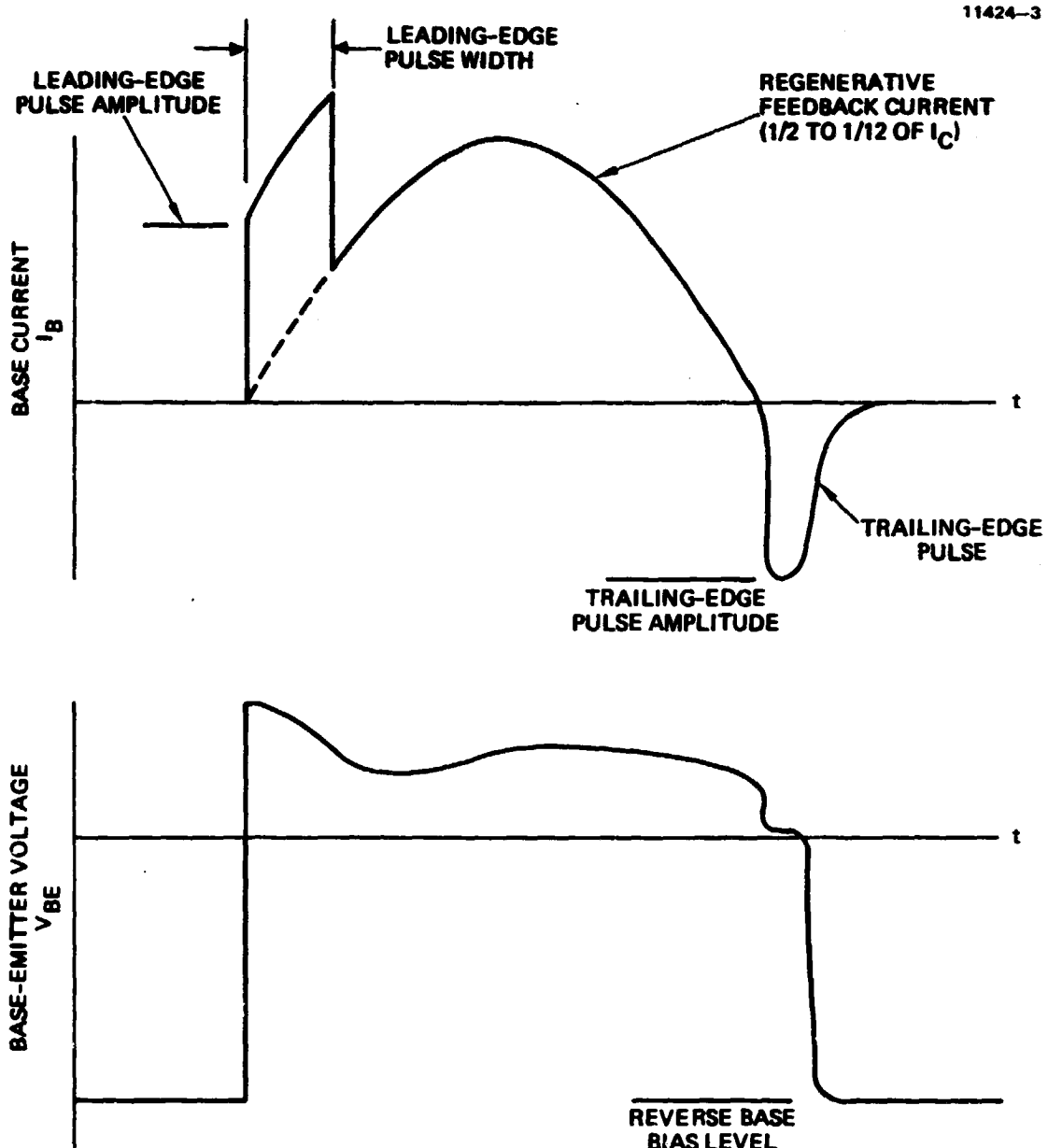


Figure 3. Typical base drive waveforms generated by the test circuits.

## A. BASE-DRIVE TO MINIMIZE TOTAL DEVICE DISSIPATION

The base-drive required to minimize total device dissipation was determined by monitoring the total device dissipation with an electronic power-measuring circuit and varying the various base-drive parameters to obtain the lowest reading. This electronic circuit calculated the average of $(V_{BE} \times I_B) + (V_{CE} \times I_C)$ and was calibrated against a balance-type calorimeter.

Figure 4 is a typical set of curves showing that the minimum power dissipation is nearly independent of the regenerative feedback ratio (forced $\beta$) at the lower current levels and shows a much more pronounced minimum at the higher current levels. Figures 5 and 6 are typical curves that show how the leading-edge pulse duration and leading-edge pulse amplitude varied with the regenerative feedback ratio for minimum device dissipation. The maximum leading-edge pulse amplitude available from the test circuits was 15 A for the D60T transistors and 30 A for the D7ST transistors. The characteristics of the trailing-edge pulse had no measurable effect on the minimum device dissipation. Additional data on a typical D60T and D7ST is presented as Tables A-1 through A-6 of Appendix A. Tables 3 and 4 list the base-drive parameters for the D60T and D70T, respectively, that resulted in minimum total device dissipation. The data for delay time, rise time, storage time, fall time, $V_{CE}$ (SAT), and total device dissipation were taken under these base-drive conditions, and a negative reverse base bias of 7 V for the D60Ts, and 8 V for the D7STs. These negative reverse base bias voltages were chosen since they minimized storage time.

## B. TOTAL DEVICE DISSIPATION

Total device dissipation was measured using the electronic power-measuring circuit which has an accuracy of approximately ±10%. The data presented represent the power that would be dissipated in the transistor for a full-wave-rectified sinusoidal collector current. The maximum power that a transistor would dissipate in a series resonant inverter (SRI) is 50% of the values shown. Figures 7 and 8 show how the power dissipation in a typical D60T and D7ST, respectively, varies with peak collector current and resonant frequency. These figures indicate that the power dissipation for the unsaturated condition with the D60T is considerably higher than for the saturated condition, while the power

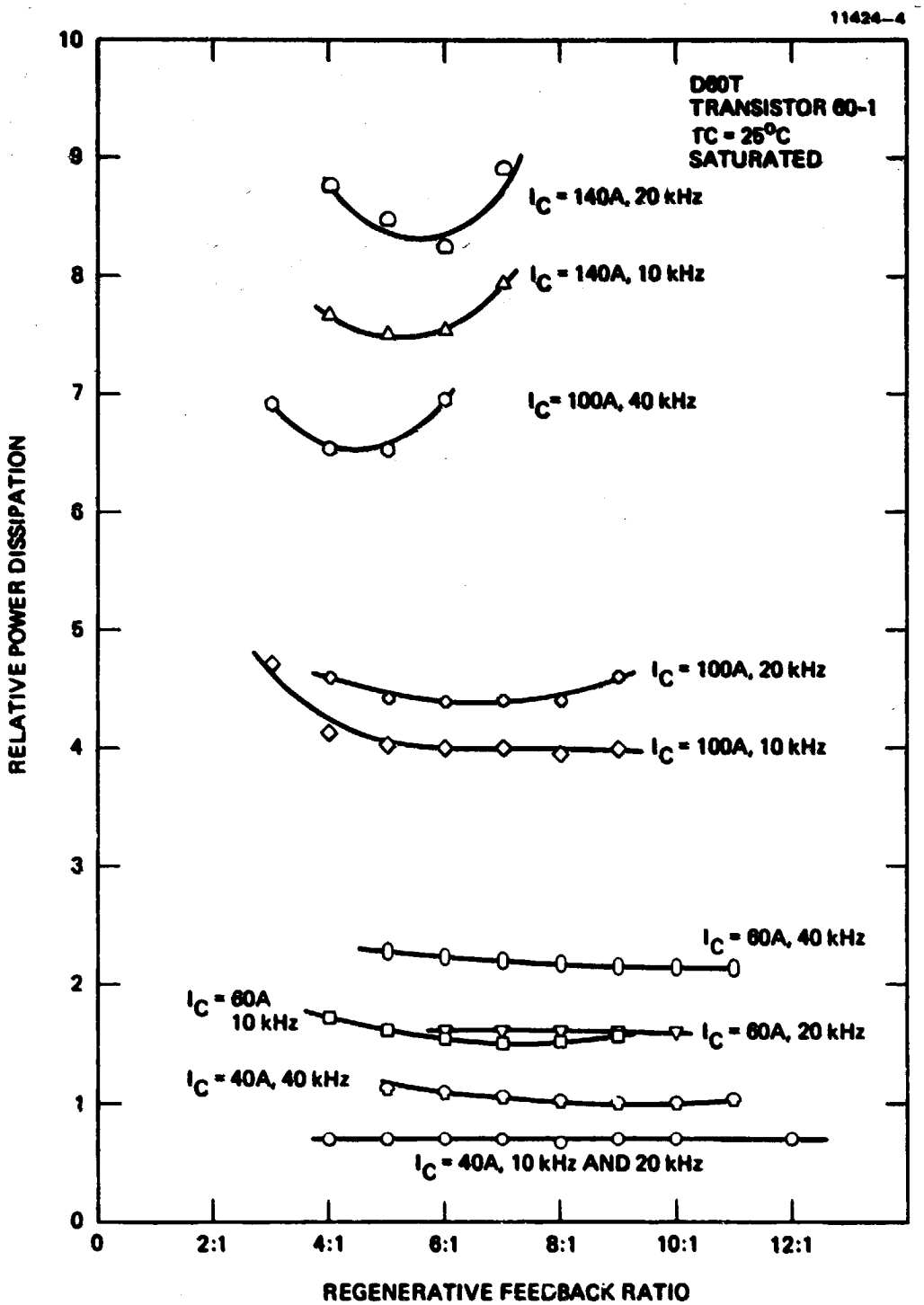


Figure 4. Variation of relative power dissipation with regenerative feedback ratio for a typical D60T transistor

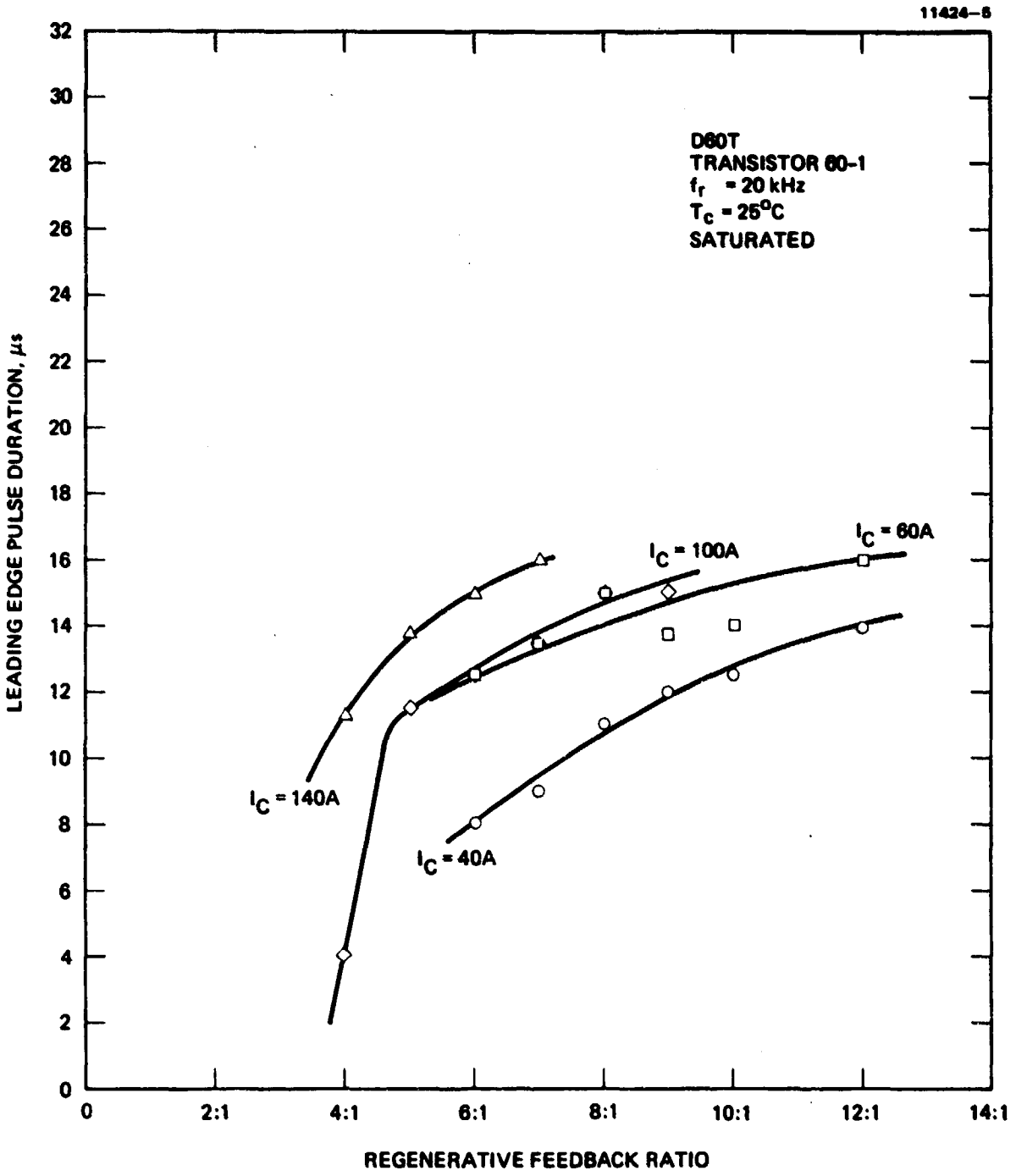


Figure 5. Variation of leading edge pulse duration with regenerative feedback ratio for minimum device dissipation (typical transistor).

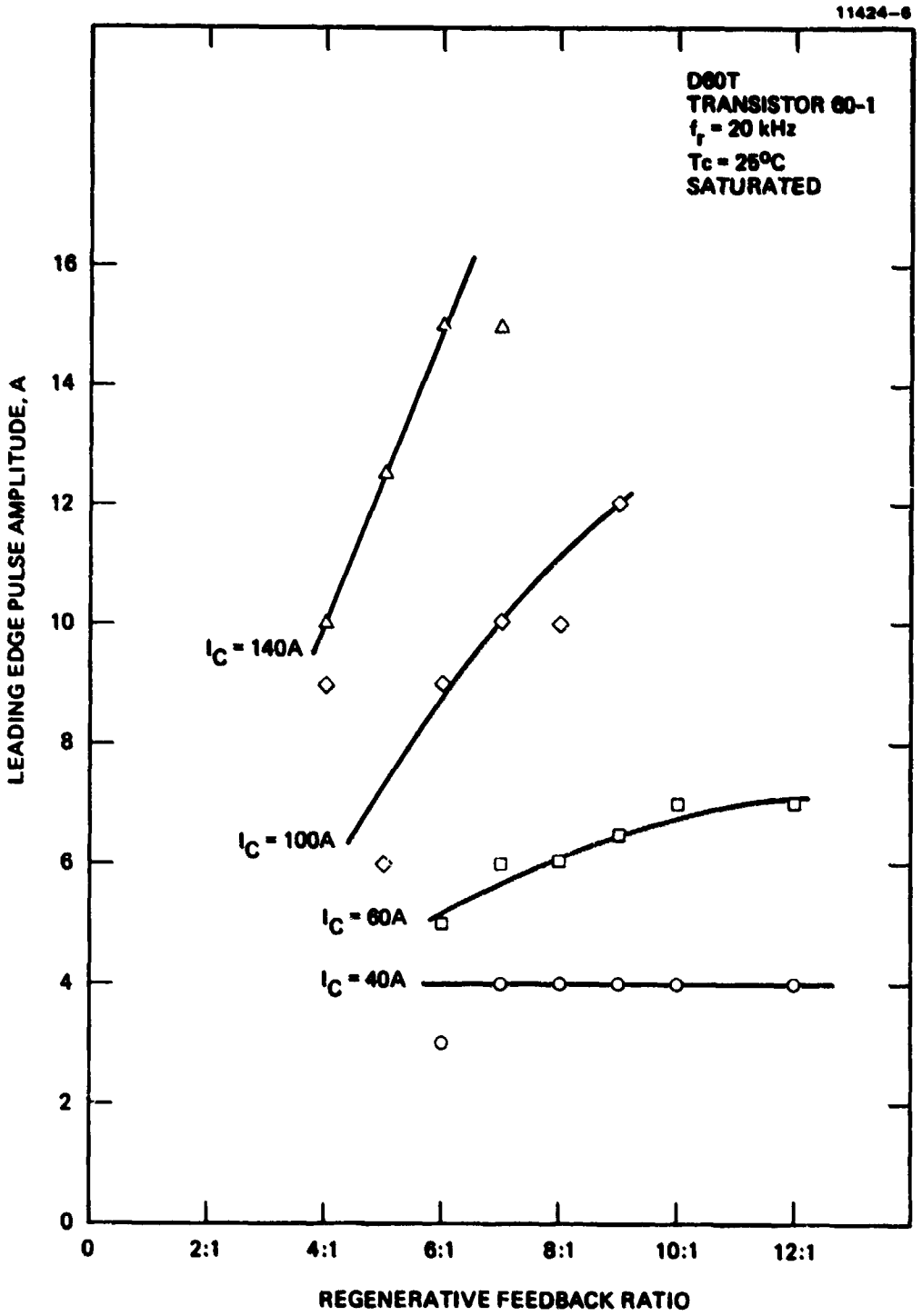


Figure 6. Variation of leading edge pulse amplitude with regenerative feedback ratio for minimum device dissipation (typical transistor).

TABLE 3. BASE DRIVE PARAMETERS FOR MINIMUM TOTAL DEVICE DISSIPATION FOR THE D60T TRANSISTOR

| Peak Ic, Amps | Resonance Frequency, fr, kHz | Saturated | | | Unsaturated | | |
|---|---|---|---|---|---|---|---|
| | | Leading Edge Pulse | | Turns Ratio | Leading Edge Pulse | | Turns Ratio |
| | | Amps | µS | | Amps | µS | |
| 40 | 10 | 2.5 | 32.0 | 8:1 | 7.0 | 6.0 | 6:1 |
| 60 | 10 | 3.0 | 31.0 | 8:1 | 2.0 | 3.0 | 5:1 |
| 100 | 10 | 4.0 | 30.0 | 5:1 | 6.0 | 44.0 | 6:1 |
| 140 | 10 | 6.0 | 30.0 | 4:1 | 4.0 | 44.0 | 3:1 |
| 40 | 20 | 4.0 | 12.5 | 8:1 | 13.0 | 19.0 | 8:1 |
| 60 | 20 | 7.0 | 13.5 | 7:1 | 12.0 | 19.0 | 6:1 |
| 100 | 20 | 11.5 | 14.0 | 7:1 | 5.0 | 20.0 | 4:1 |
| 140 | 20 | 14.5 | 15.0 | 5:1 | 10.0 | 20.0 | 3:1 |
| 40 | 40 | 10.0 | 4.0 | 8:1 | 8.5 | 8.0 | 8:1 |
| 60 | 40 | 11.5 | 5.0 | 8:1 | 12.0 | 8.0 | 8:1 |
| 100 | 40 | 15.0 | 5.5 | 5:1 | 15.0 | 5.5 | 4:1 |

TABLE 4. BASE DRIVE PARAMETERS FOR MINIMUM TOTAL DEVICE DISSIPATION FOR THE D7ST TRANSISTOR

| Peak Ic, Amps | Resonant Frequency, fr, kHz | Saturated | | | Unsaturated | | |
|---|---|---|---|---|---|---|---|
| | | Leading Edge Pulse | | Turns Ratio | Leading Edge Pulse | | Turns Ratio |
| | | Amps | µS | | Amps | µS | |
| 100 | 10 | 7 | 22.0 | 10:1 | 15 | 40.0 | 10:1 |
| 150 | 10 | 12 | 30.0 | 10:1 | 14 | 40.0 | 6:1 |
| 250 | 10 | 20 | 32.0 | 8:1 | 28 | 42.0 | 8:1 |
| 350 | 10 | 16 | 28.0 | 4:1 | 26 | 30.0 | 5:1 |
| 100 | 20 | 15 | 9.0 | 10:1 | 18 | 10.0 | 10:1 |
| 150 | 20 | 22 | 10.5 | 10:1 | 18 | 13.0 | 10:1 |
| 250 | 20 | 28 | 12.0 | 7:1 | 28 | 15.0 | 7:1 |
| 350 | 20 | 30 | 13.0 | 4:1 | 30 | 15.0 | 4:1 |
| 100 | 40 | 24 | 4.0 | 10:1 | 28 | 4.0 | 10:1 |
| 150 | 40 | 30 | 5.0 | 10:1 | 30 | 6.0 | 10:1 |
| 250 | 40 | 30 | 5.5 | 4:1 | 30 | 4.5 | 3:1 |

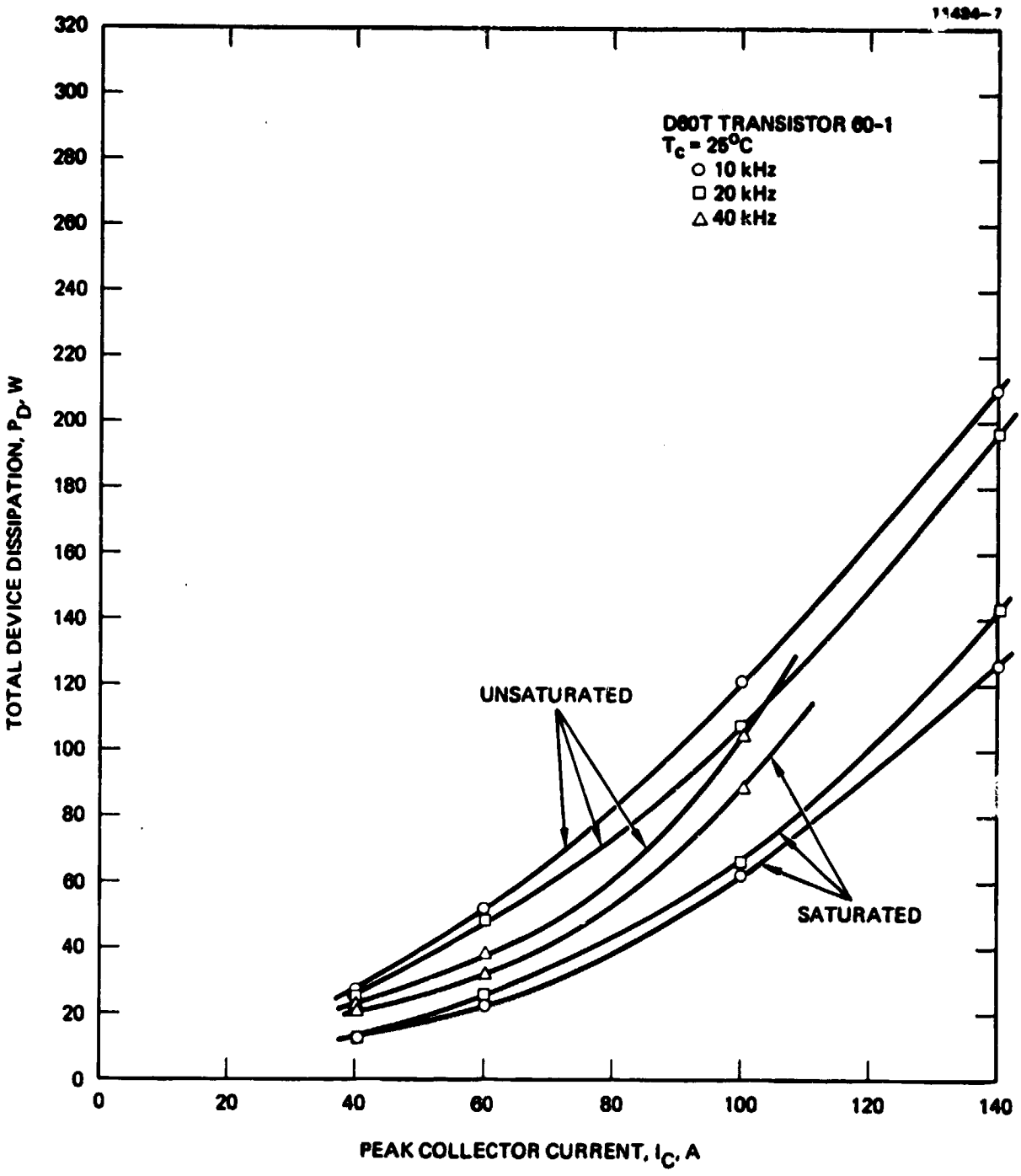


Figure 7. Variation of total device dissipation with peak collector current and resonant frequency for a typical D60T.

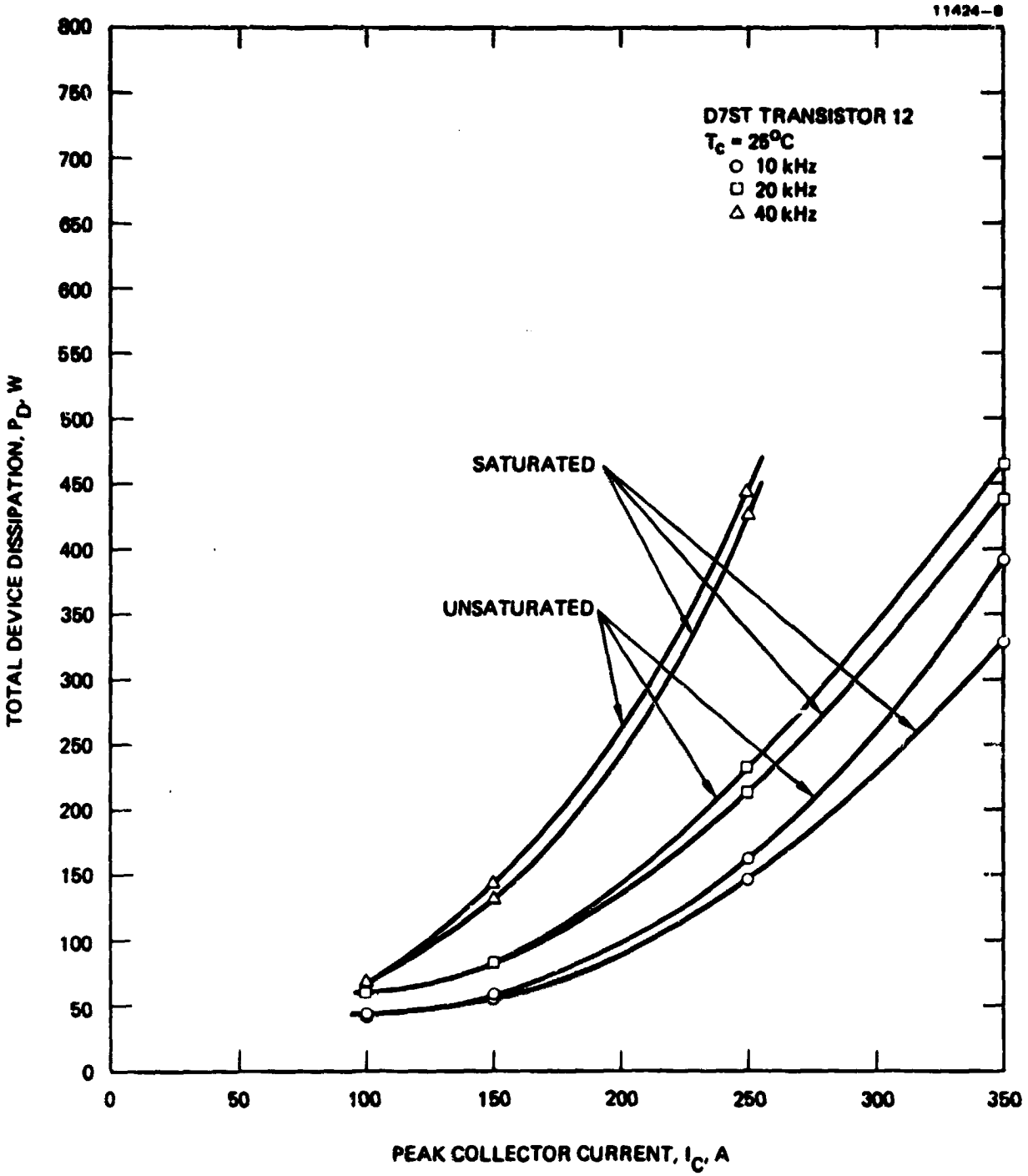


Figure 8. Variation of total device dissipation with peak collector current and resonant frequency for a typical D7ST.

dissipation for the D7ST is almost the same for either condition. This indicates that the D7ST does not have time to get into hard saturation during the collector-current pulse. In general, the total device dissipation increases with increasing peak-collector current and increasing resonant frequency (Figures 7 and 8). The total power dissipations for all of the transistors tested are presented in Tables A-7 and A-8 of Appendix A.

## C. MINIMUM REQUIRED BASE-DRIVE AS A FUNCTION OF $I_C$

Minimum required base-drive current was measured as a function of $I_C$; this ratio represents the current gain ($\beta$) of the transistor for a given saturation voltage over a range of peak collector currents. The saturation voltage was defined as the value of $V_{CE}$ at the time of peak collector current. This test was performed for saturation voltages of 0.75, 1.0, and 2.0 V. Figures 9, 10, and 11 are the curves of $\beta$ versus peak collector current for a typical D60T at resonant frequencies of 10 kHz, 20 kHz, and 40 kHz, respectively. Figures 12, 13, and 14 present the same data for a typical D7ST. All of these curves exhibit a maximum achievable collector current for a given collector-to-emitter voltage. The variation of $\beta$ versus $I_C$ due to changes in the case temperature is shown in Figures 15 and 16 for a typical D60T and D7ST, respectively.

## D. BASE-DRIVE FOR MAXIMUM OPERATING FREQUENCY

Maximum operating frequency for a transistor can be achieved by making the time consumed by switching as short as possible. A switching time is only affected by those base-drive parameters that come into affect prior to the end of the switching time. Therefore, the only parameter that affects delay time and rise time is the amplitude of the leading-edge pulse. The regenerative feedback ratio has no effect since the rise time of the feedback transformer is longer than the delay time and rise time of the transistor. Transistor delay time was measured from the time that the base-to-emitter voltage went positive until the collector-to-emitter voltage had fallen by 10%. Typical waveforms from which delay time was measured are shown in Figure 17(a). The test circuits measured delay time with zero collector current; this is representative of

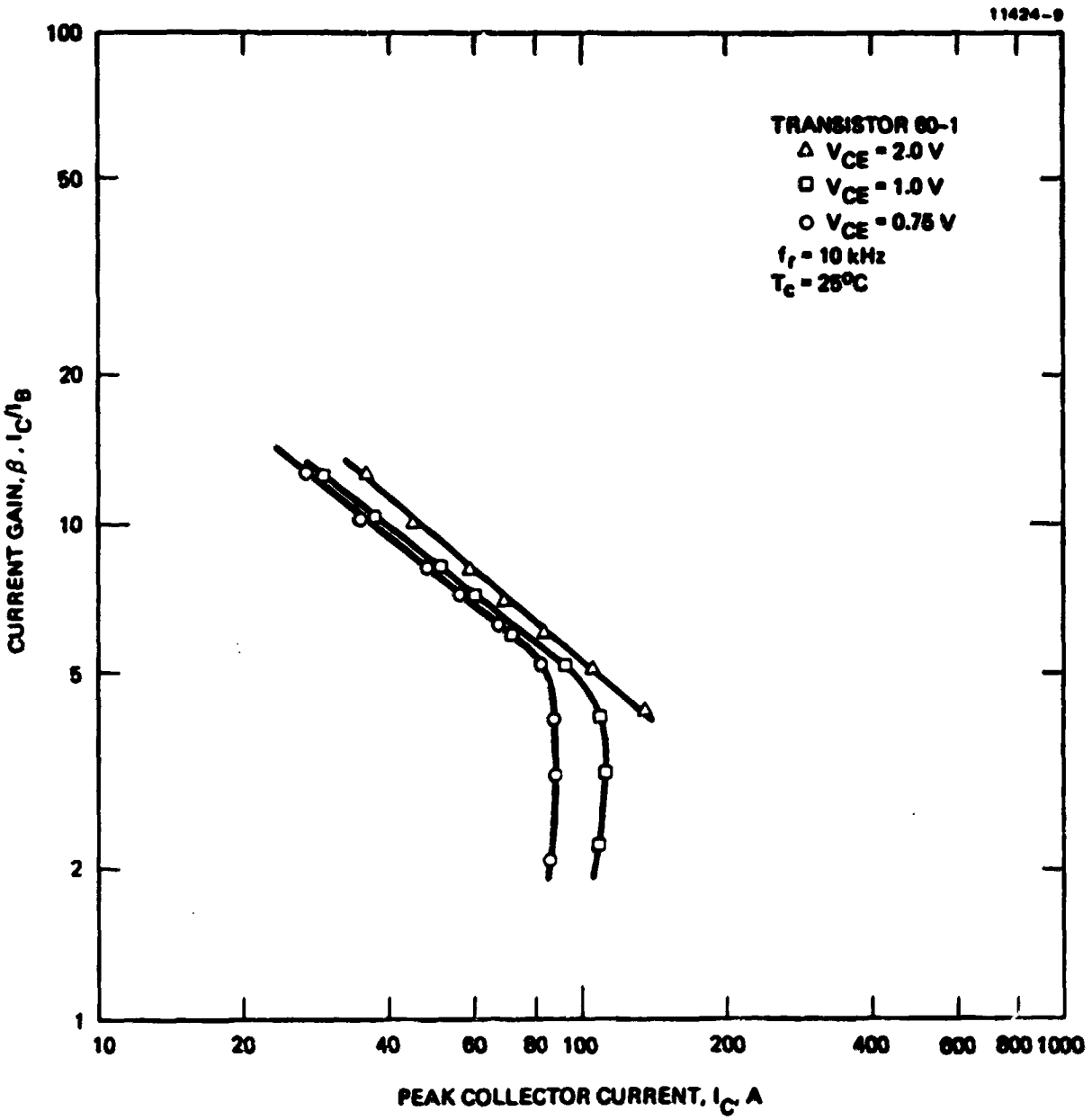


Figure 9. Current gain versus peak collector current for a typical D60T at a resonant frequency of 10 kHz.

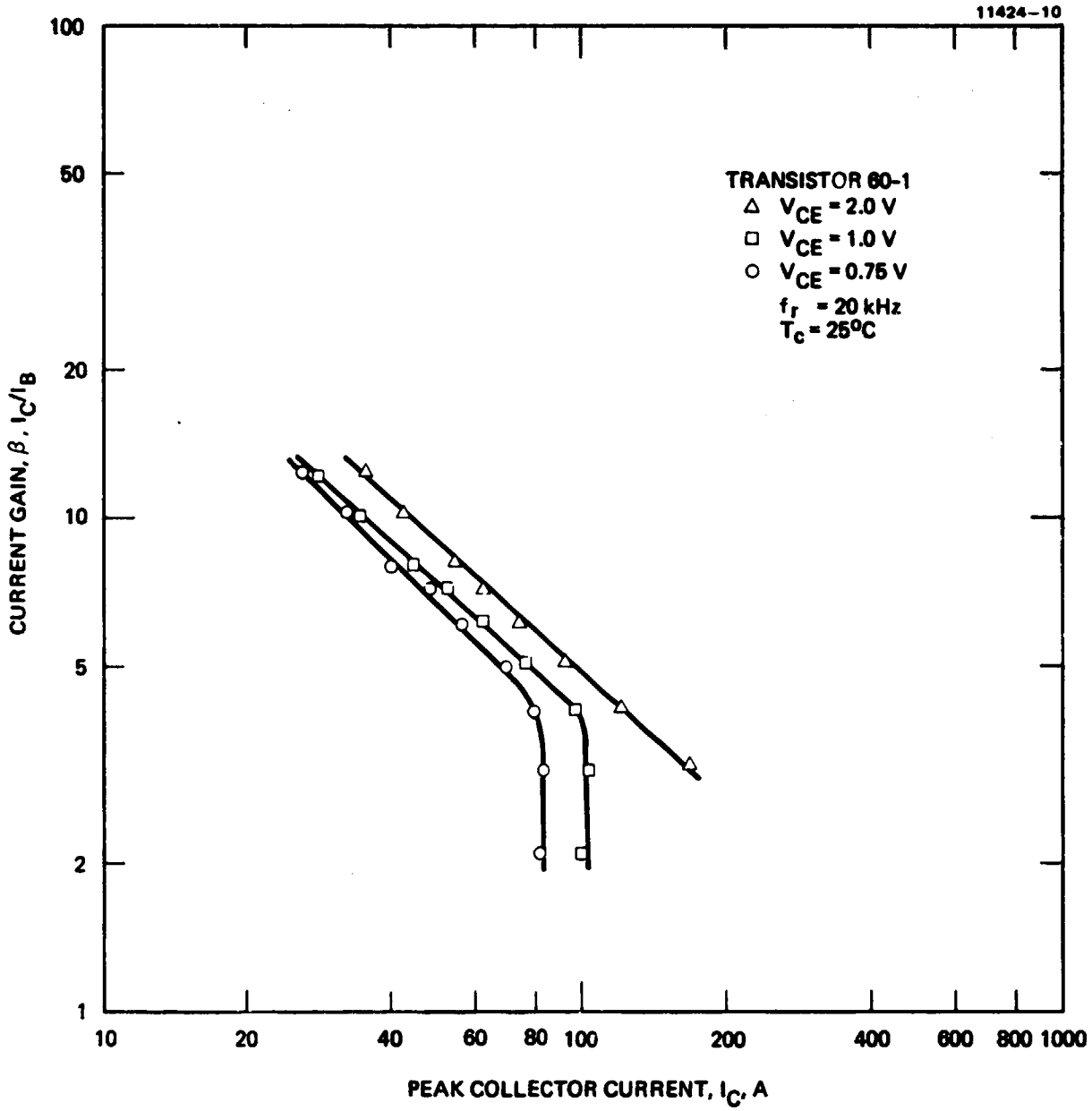


Figure 10. Current gain versus peak collector current for a typical D60T at a resonant frequency of 20 kHz.

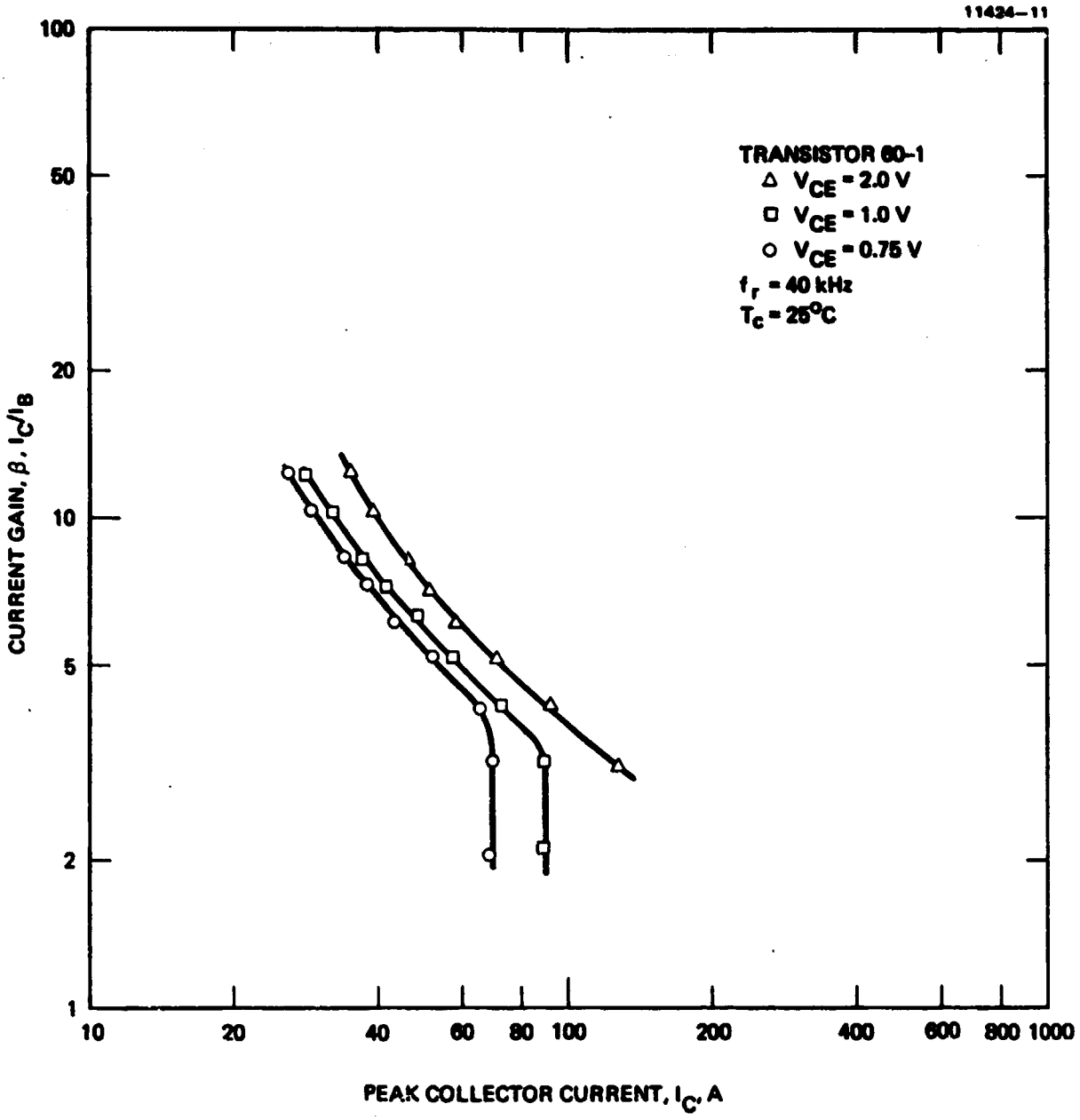


Figure 11. Current gain versus peak collector current for a typical D60T at a resonanc frequency of 40 kHz.

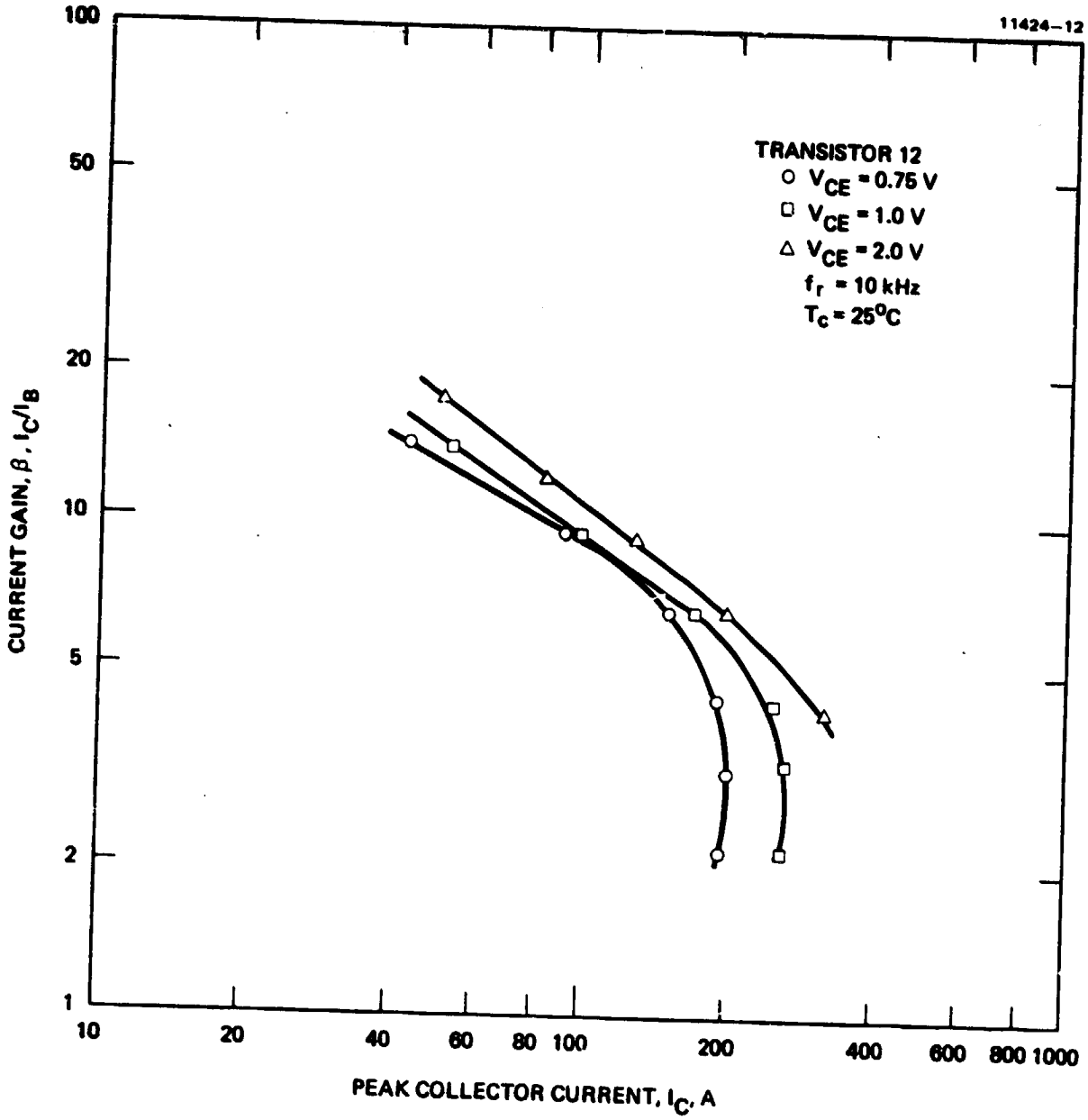


Figure 12. Current gain versus peak collector current for a typical D7ST at a resonant frequency of 10 kHz.

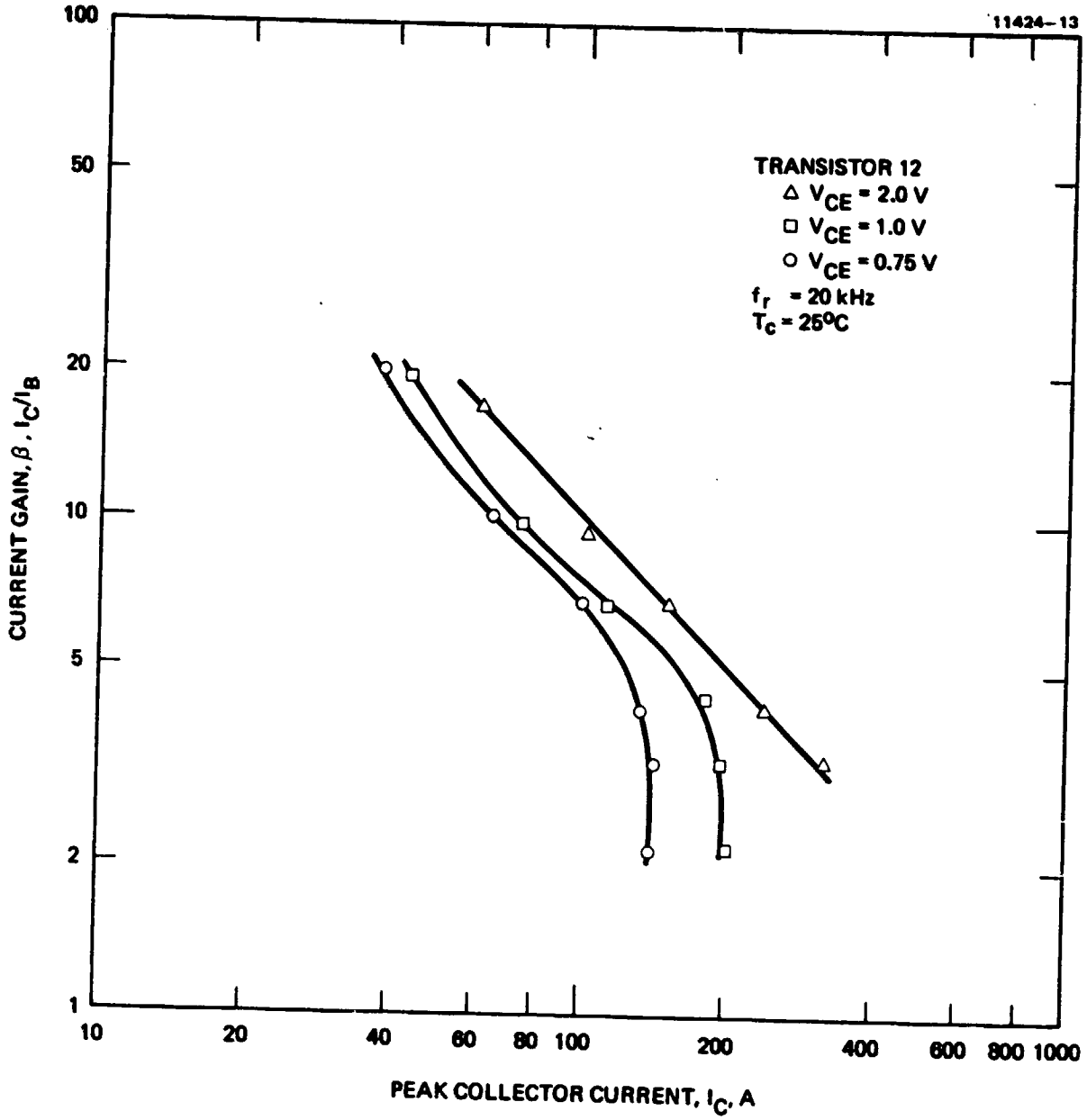


Figure 13. Current gain versus peak collector current for a typical D7ST at a resonant frequency of 20 kHz.

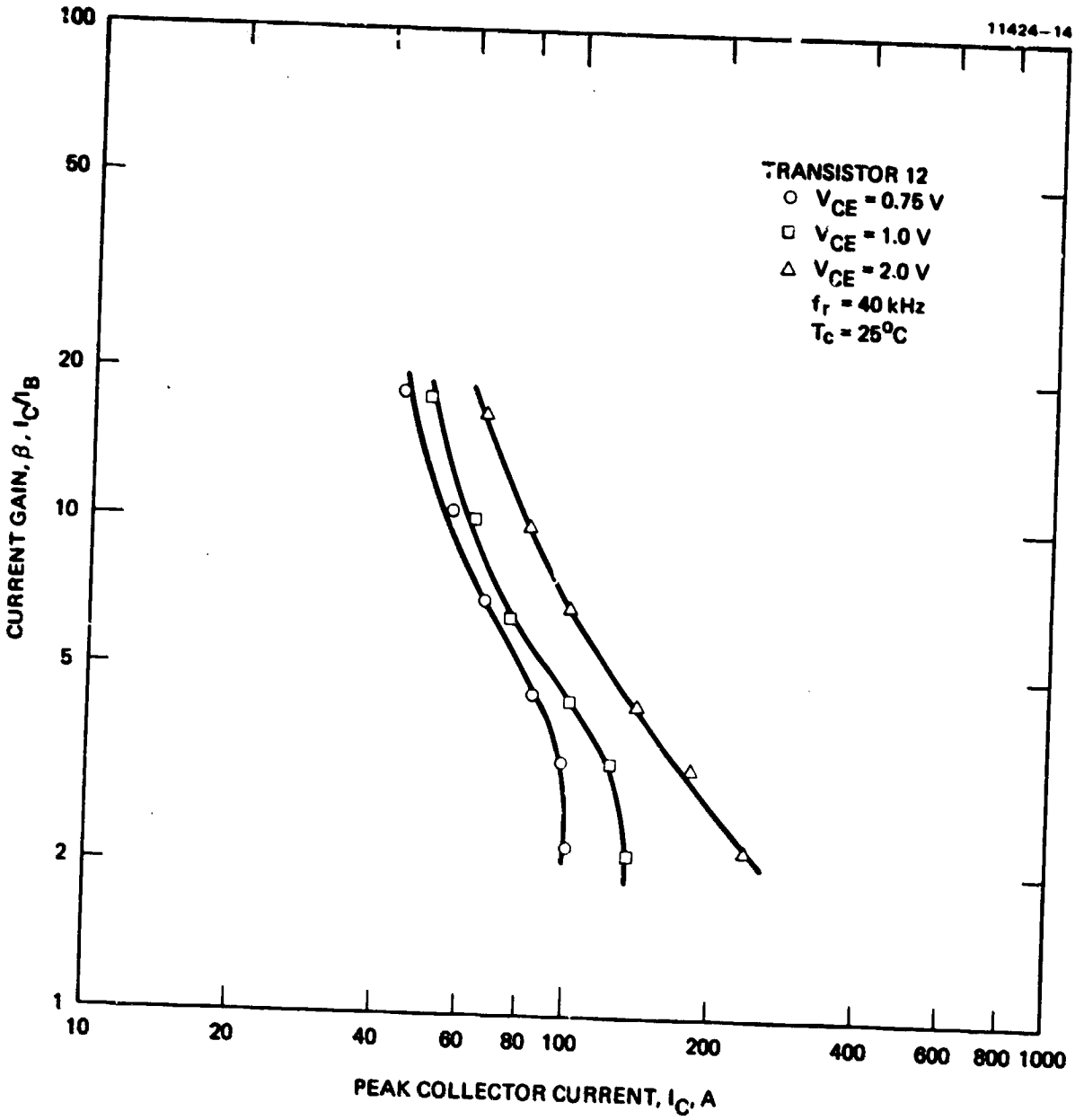


Figure 14. Current gain versus peak collector current for a typical D7ST at a resonant frequency of 40 kHz.

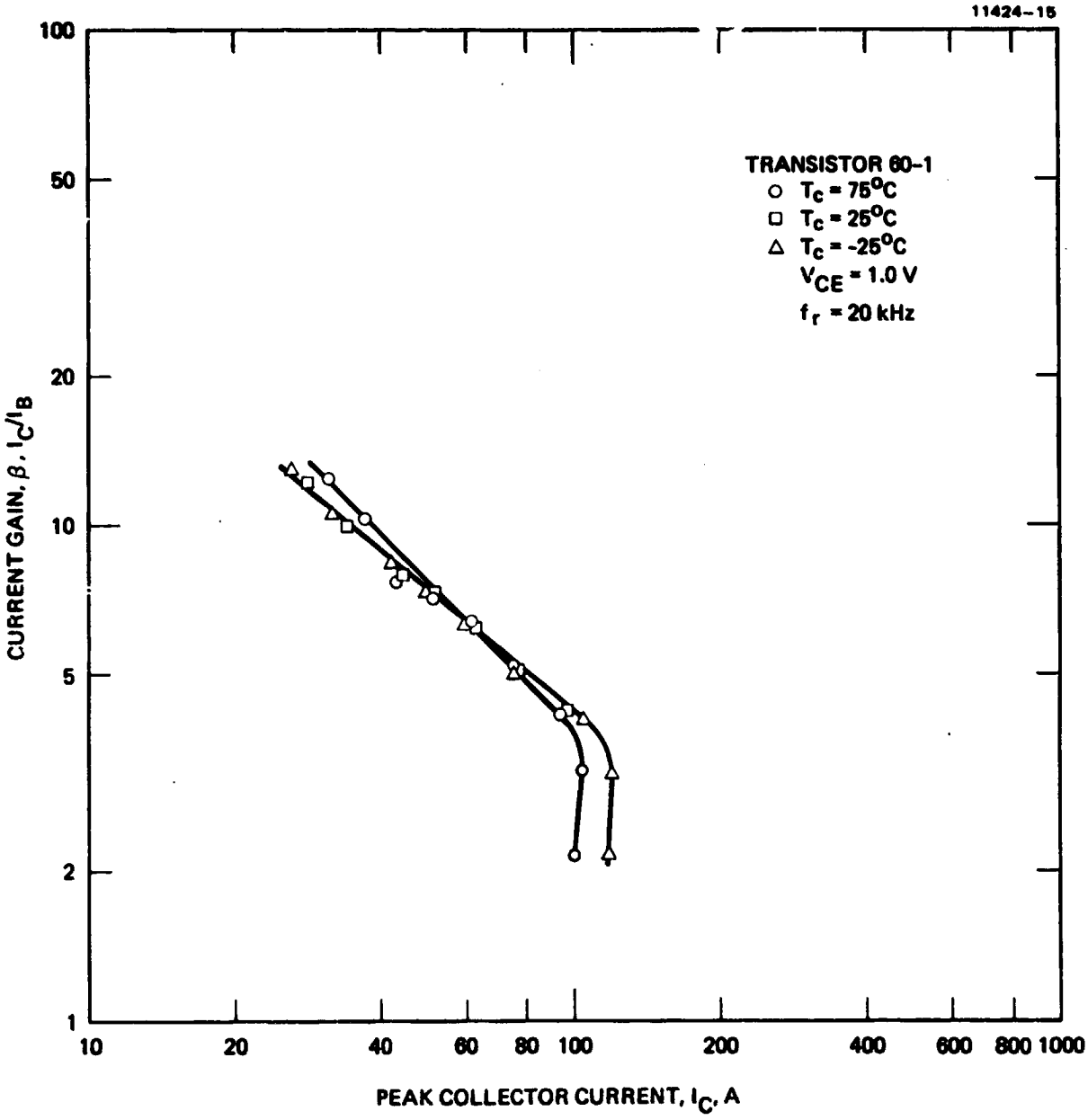


Figure 15. Variation of current gain versus peak collector current at three case temperatures for a typical D60T.

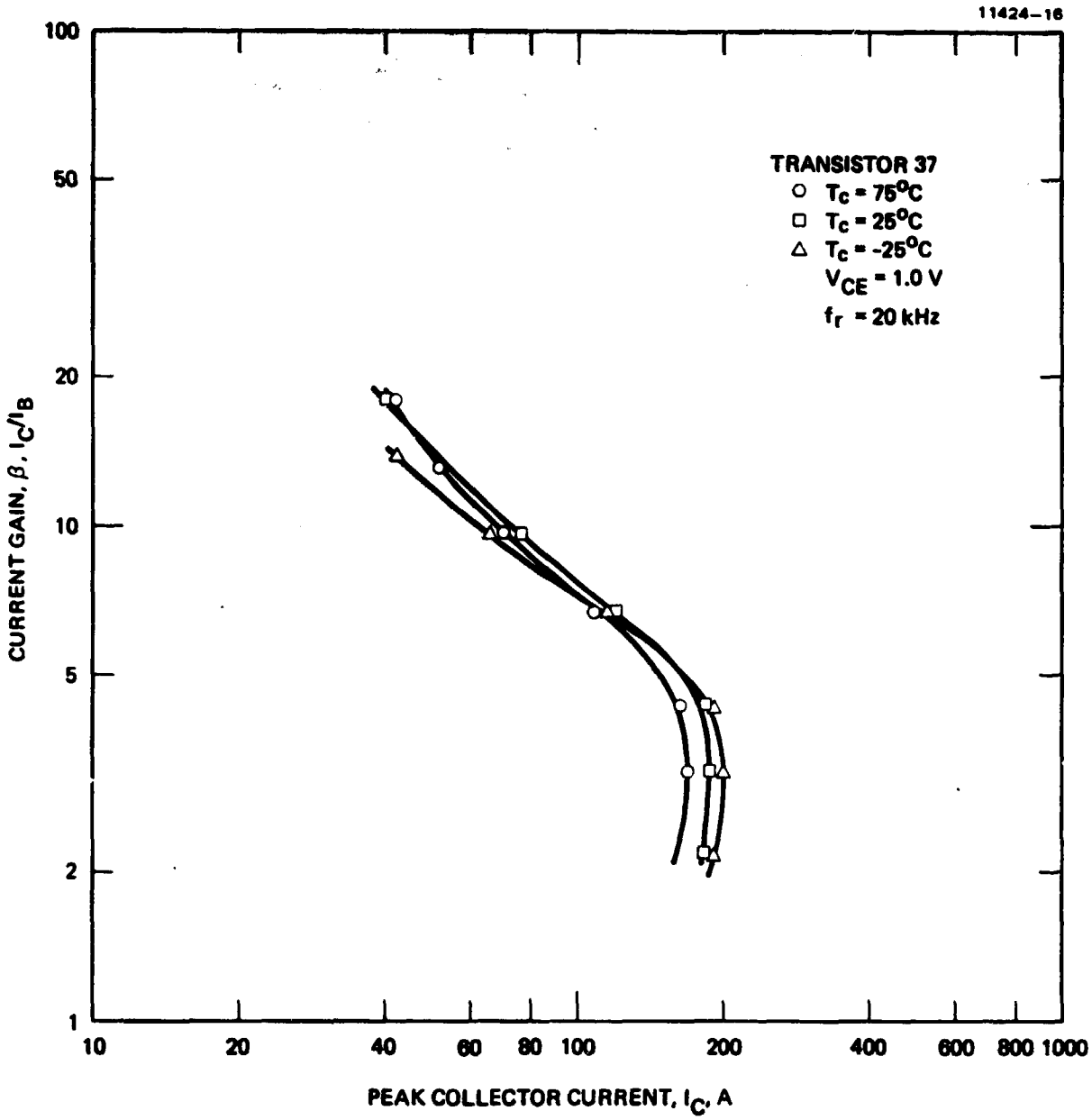


Figure 16. Variation of current gain versus peak collector current at three case temperatures for a typical D7ST.

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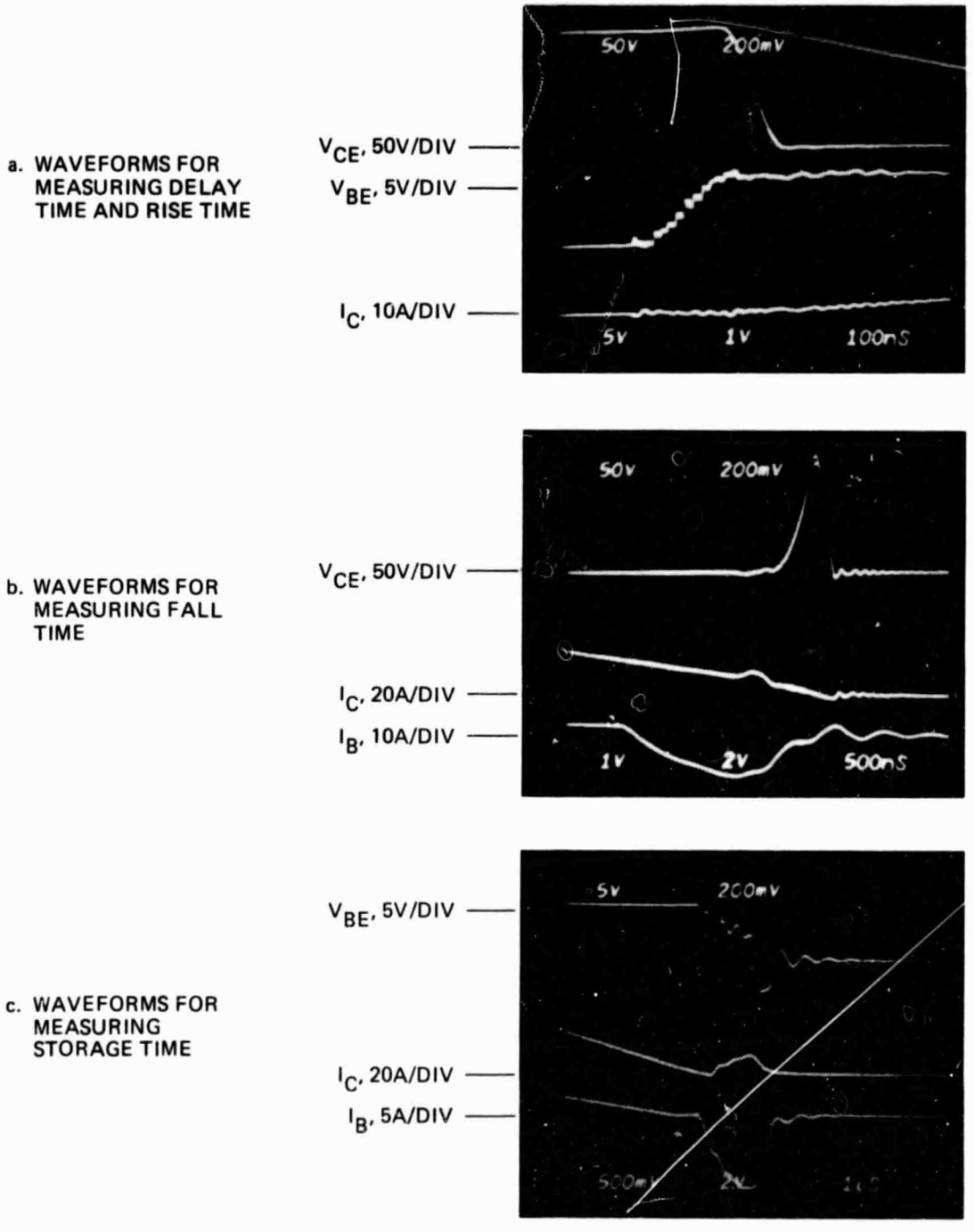


Figure 17. Typical waveforms for measuring switching times (D60T operating saturated at a peak collector current of 60 A and a resonant frequency of 20 kHz).

switching conditions when the tank current is discontinuous in an SRI. When the tank current in an SRI is continuous, the transistors will be turning on into some current and the delay times will be longer than those measured here. Figures 18 and 19 show curves of delay time versus leading-edge pulse amplitude for a typical D60T and D7ST, respectively. These curves are typical for all of the transistors at all three frequencies. Delay times versus leading-edge pulse amplitude, peak collector current, and resonant frequency for all of the transistors tested are listed in Tables A-9 through A-17 of Appendix A.

Rise time was measured as the time required for the collector-to-emitter voltage to fall from its 90% level to its 10% level. Rise time could not be measured using the conventional definition of the time from 10% to 90% on the current waveform, since the collector current was zero at the time of turn-on. Typical waveforms from which rise time was measured are shown in Figure 17(a). Figures 20 and 21 show curves of rise time versus the leading-edge pulse amplitude for a typical D60T and D7ST, respectively. These curves are typical for all of the transistors at all three frequencies and show a decrease in rise time as the leading-edge pulse amplitude increases. Rise times versus leading edge pulse amplitude, peak collector current, and resonant frequency for all of the transistors tested are presented in Tables A-9 through A-17 of Appendix A.

Storage time and fall time can be effected by all of the base-drive parameters, since all of these parameters come into effect prior to these switching times. Fall time was measured by turning the transistor off before the collector current had fallen to zero and then measuring the rise time of the resulting $V_{CE}$ spike. Conventional fall time does not exist in an SRI. The base-drive parameters had very little effect on the artificially induced fall time, and resonant frequency and peak collector current were the only parameters that did affect it. This would tend to indicate that the measured fall time may be more a function of the test circuit than the transistor. Typical waveforms from which fall time was measured are shown in Figure 17(b). Fall times versus feedback turns-ratio, peak collector current, and resonant frequency for all of the transistors tested are listed in Tables A-18 through A-26 of Appendix A.

A very long leading-edge pulse adds to the storage time, and the larger the amplitude of the pulse, the greater the effect. The storage time data were taken with a 5 A, 5-μsec-wide leading-edge pulse and these parameters were not varied.

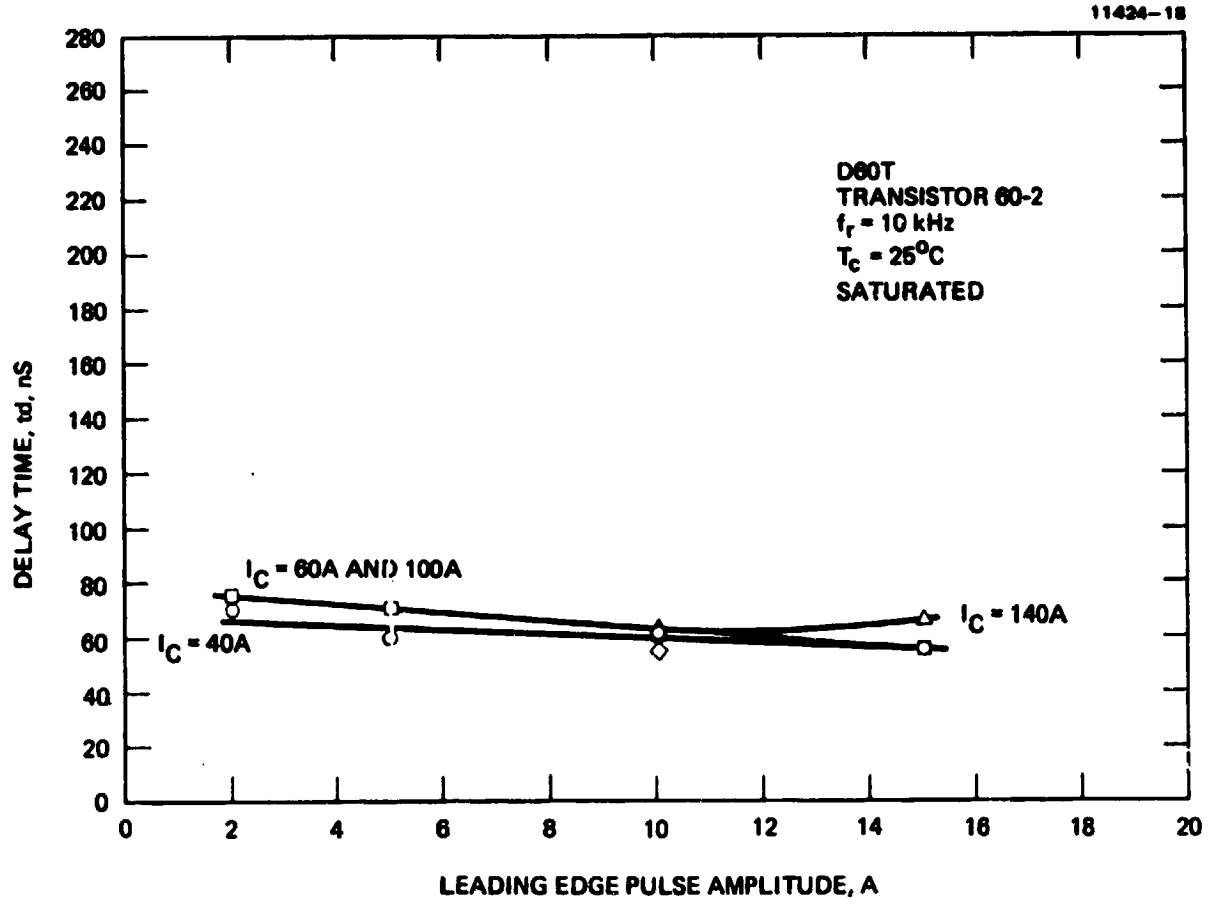


Figure 18. Delay time versus leading edge pulse amplitude for a typical D60T.

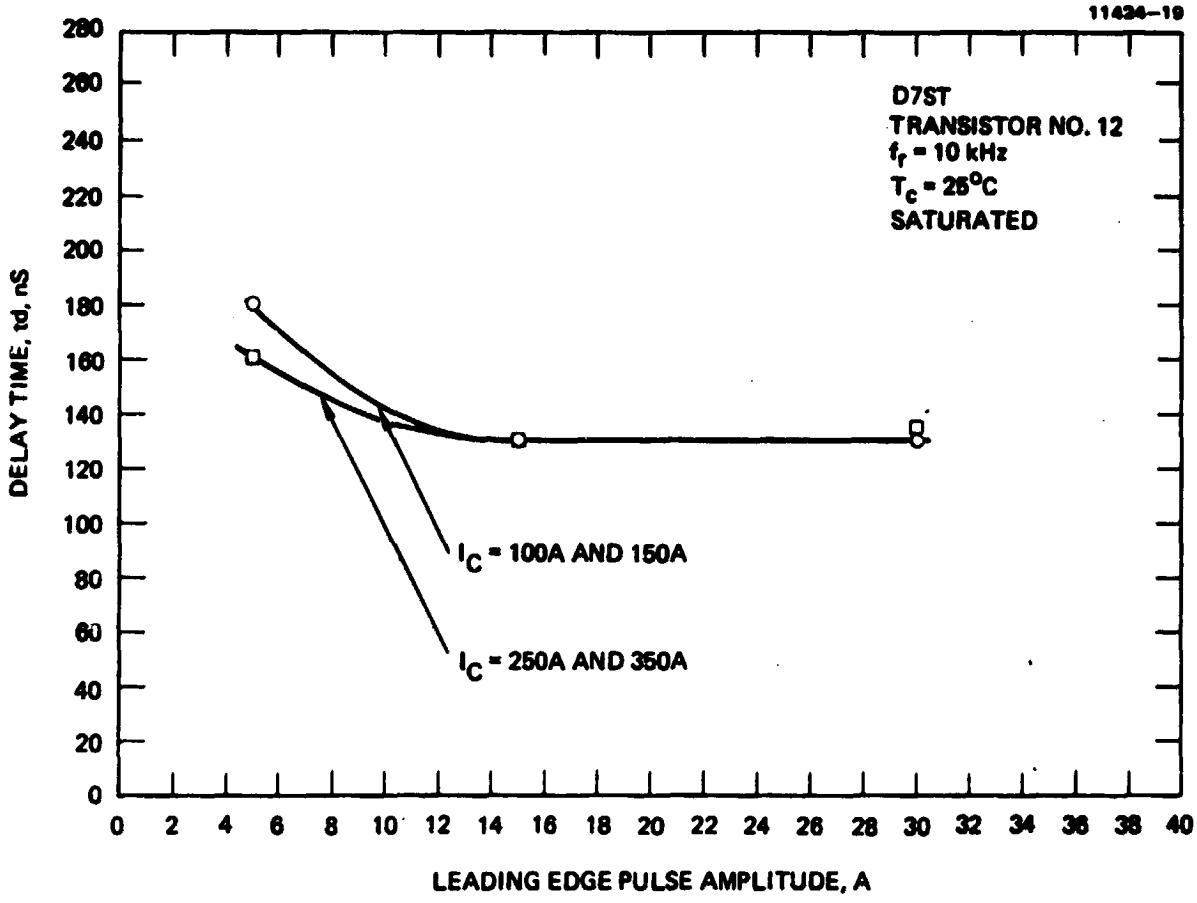


Figure 19. Delay time versus leading edge pulse amplitude for a typical D7ST.

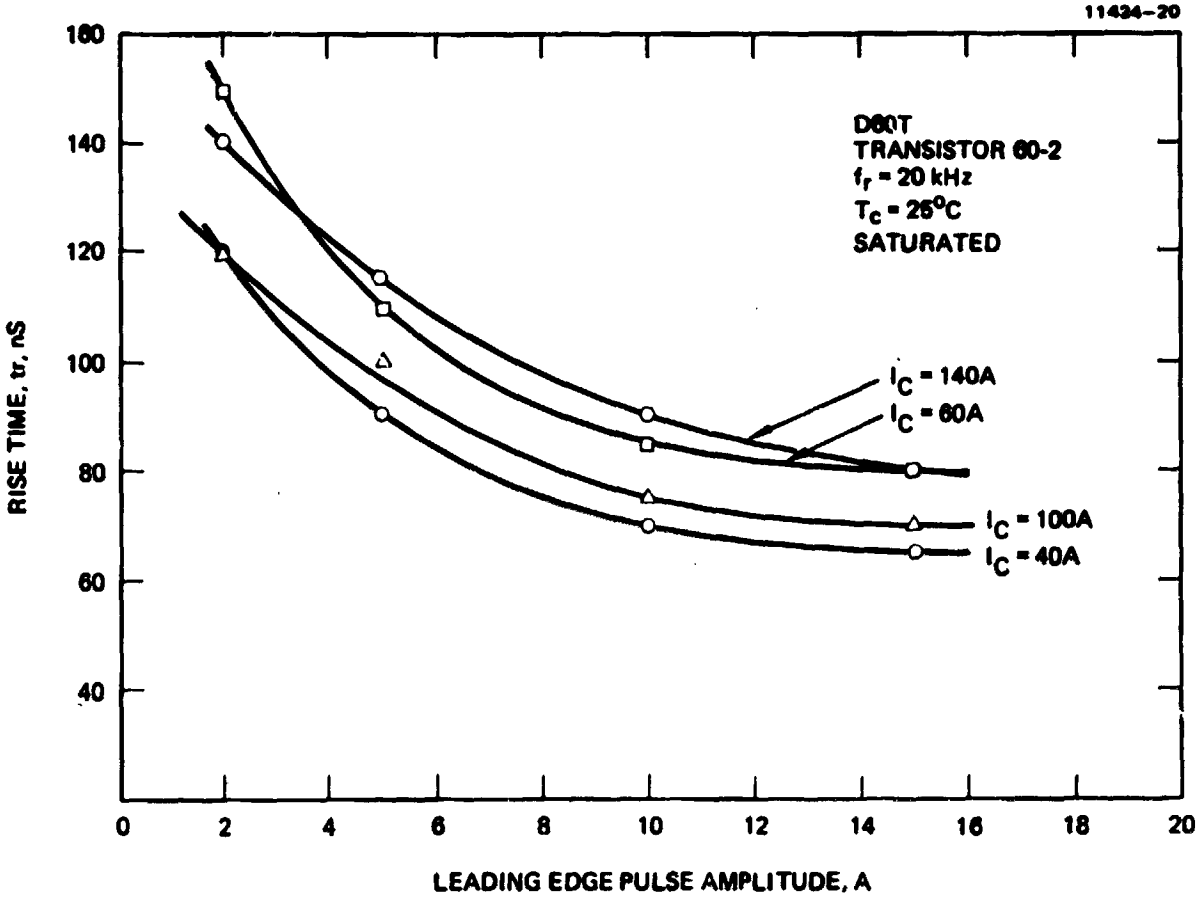


Figure 20. Rise time versus leading edge pulse amplitude for a typical D60T.

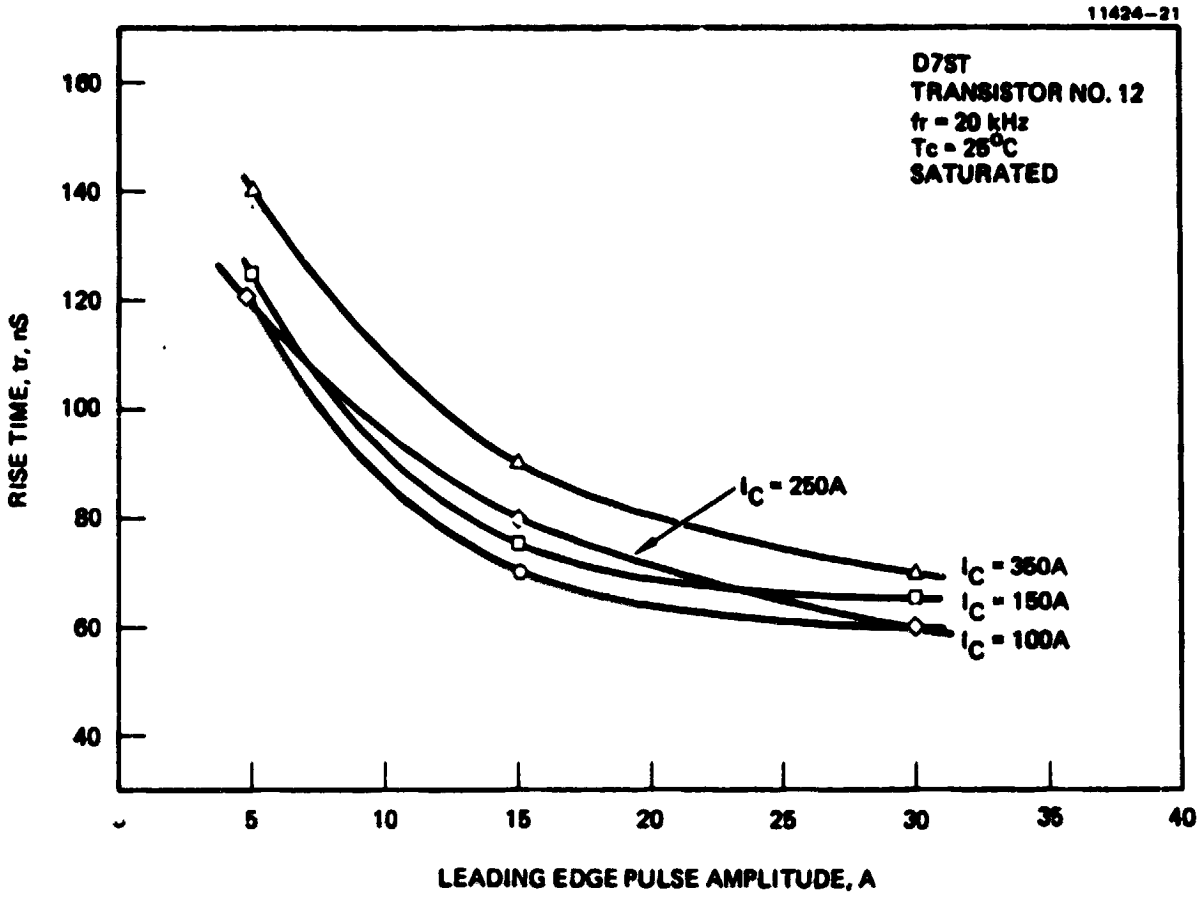


Figure 21. Rise time versus leading edge pulse amplitude for a typical D7ST.

For turn off, the base of the transistor was clamped to a negative voltage by use of an IRF-100 power MOSFET. Therefore, the negative base-current amplitude was a function of this negative voltage, the base resistance of the transistor under test, and the IRF-100 drain-to-source resistance. The only parameter that could be varied was the negative voltage; its effect on storage time is shown in Figure 22 for a D60T transistor and in Figure 23 for a D7ST transistor. A negative 7 V gave the minimum storage time for the D60T transistor, while a negative 8 V was required for the D7ST.

Figures 24 and 25 show a typical variation of storage time with peak collector current and feedback turns-ratio. Storage times versus feedback turns-ratio, peak collector current, and resonant frequency are listed in Tables A-18 through A-26 of Appendix A. In general, the storage time increased with increasing collector current, increasing frequency and decreasing feedback turns-ratio. Typical waveforms from which storage time was measured are shown in Figure 17(c). It was defined as the time between the 10% points on the negative base-current pulse.

## E. SWITCHING TIMES UNDER MINIMUM TOTAL DEVICE DISSIPATION CONDITIONS

Delay time, rise time, storage time, and fall time were measured under the base-drive conditions that resulted in minimum total device dissipation. These base-drive conditions are listed in Tables 3 and 4.

The delay times measured for the D60Ts are given in Table 5. They cover the range of 40 to 80 nsec, with most of them falling in the 60 to 70-nsec range. Delay times covered the range of 100 to 190 nsec for the D7STs, with most of them falling in the 110 to 145-nsec range. Table 6 is a tabulation of the delay times for the D7STs.

The rise times measured for the D60Ts and D7STs are given in Tables 7 and 8, respectively. They cover the range of 60 to 140 nsec for the D60Ts, with most of them falling in the 60 to 90-nsec range. They cover the range of 60 to 115 nsec for the D7STs, with most of them falling in the 60 to 85-nsec range.

The storage times for the D60Ts are given in Table 9. They cover the range of 1.05 to 3.95 μsec for the saturated condition, with most falling in the

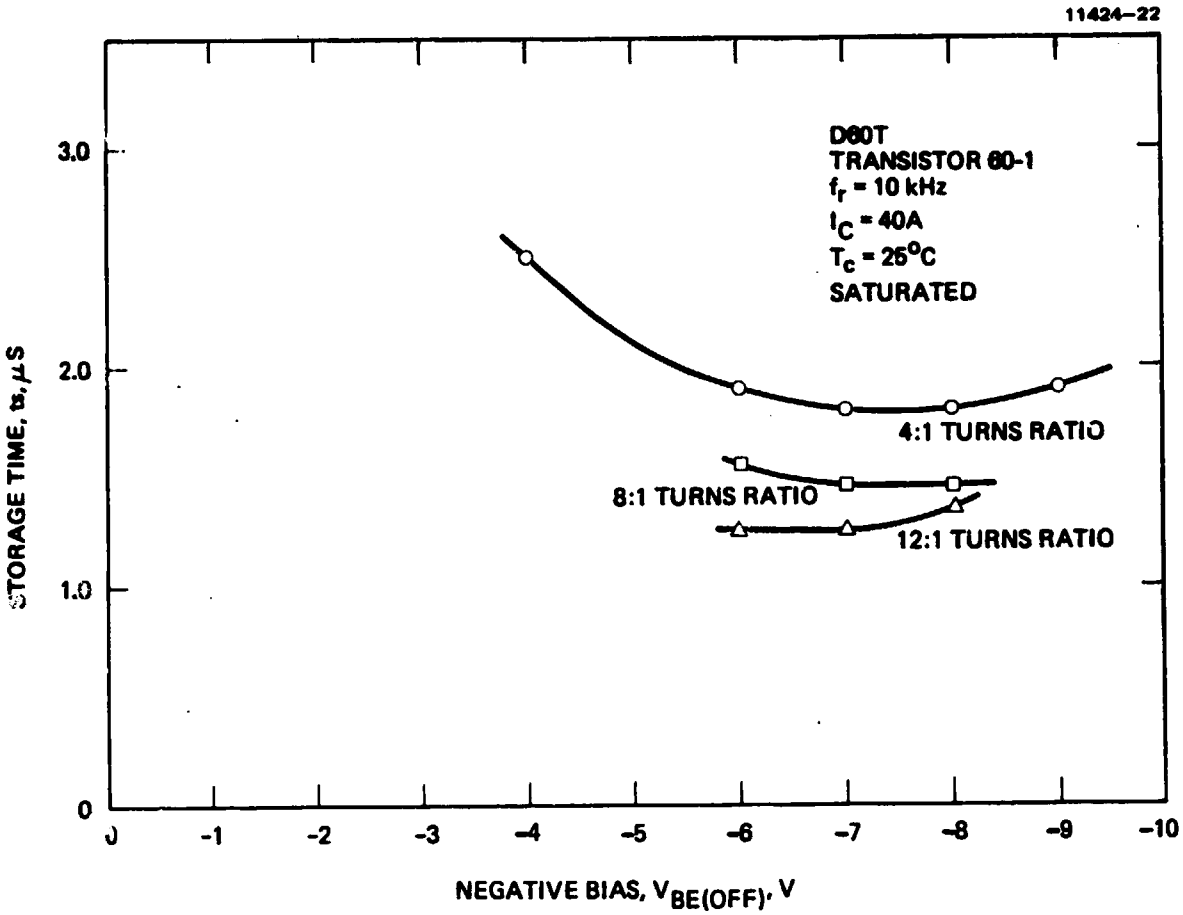


Figure 22. Variation of storage time with negative base bias for a typical D60T.

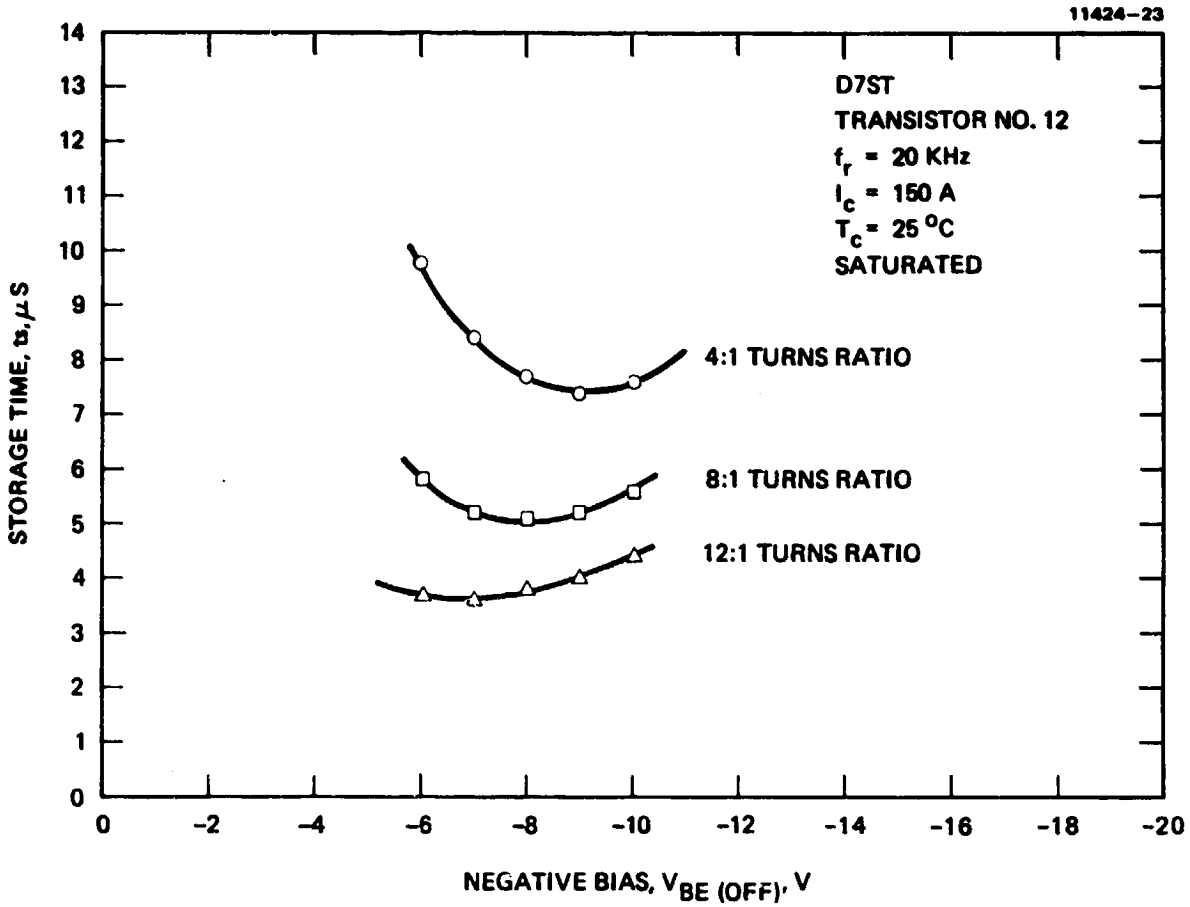


Figure 23. Variation of storage time with negative base bias for a typical D7ST.

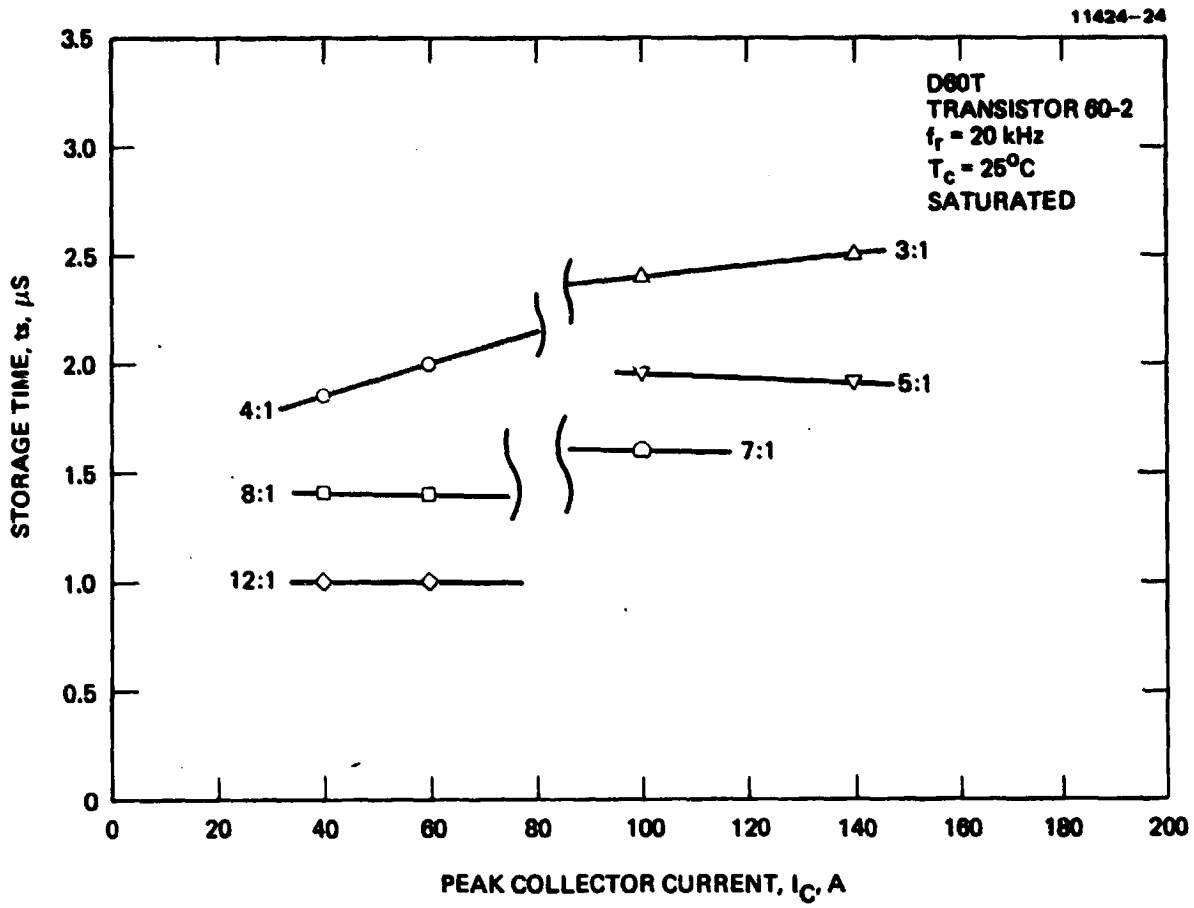


Figure 24. Variation of storage time with peak collector current and regenerative feedback turns ratio for a typical D60T.

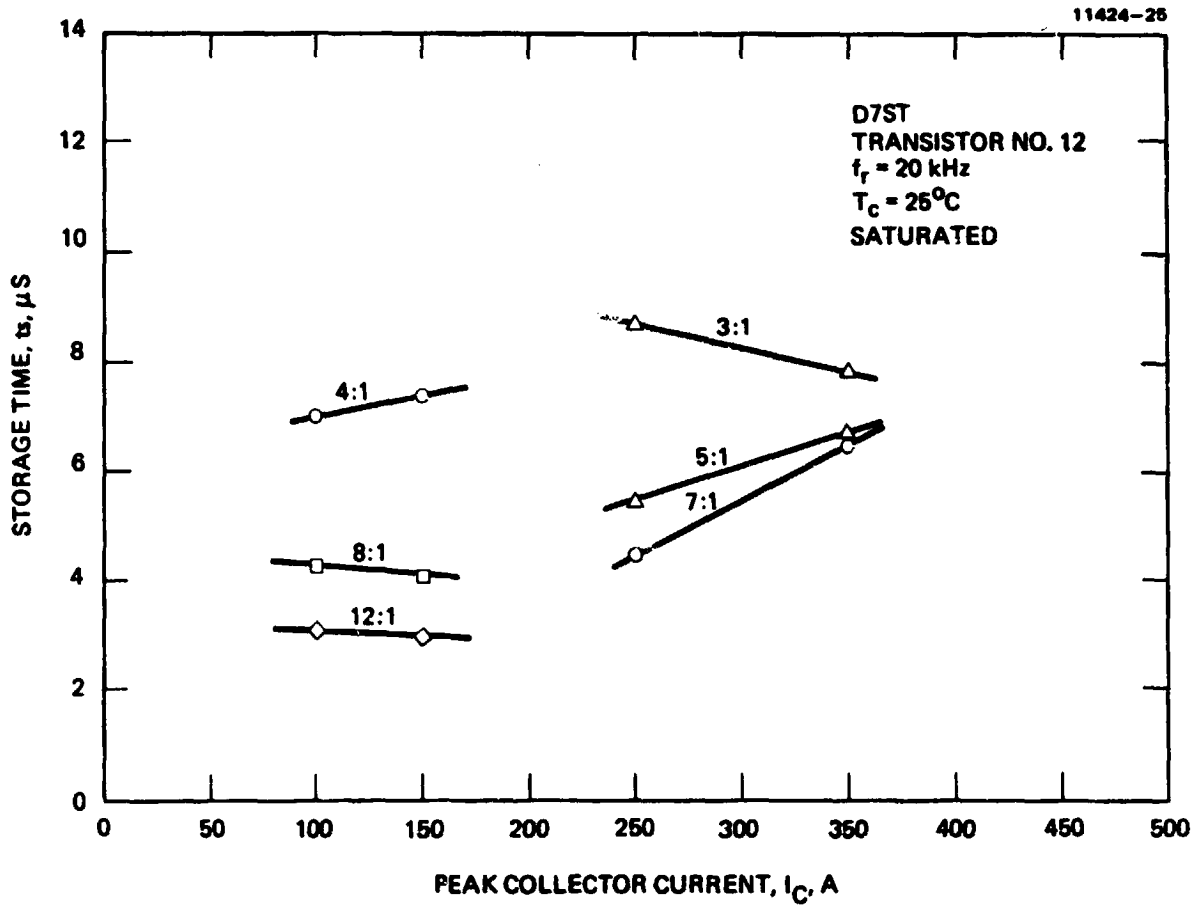


Figure 25. Variation of storage time with peak collector current and regenerative feedback turns ratio for a typical D7ST.

TABLE 5. MEASURED DELAY TIMES FOR THE D60T TRANSISTORS

| Transistor Parameter | | Delay time, td, ns | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | | | |
| 40 | 10 | 65 | 65 | 75 | 65 | 60 | 60 | 60 | 60 | 55 | 60 |
| 40 | 20 | 65 | 60 | 65 | 60 | 70 | 60 | 60 | 60 | 55 | 60 |
| 40 | 40 | 60 | 55 | 65 | 50 | 60 | 55 | 55 | 70 | 55 | 60 |
| 60 | 10 | 65 | 65 | 70 | 65 | 70 | 70 | 80 | 80 | 60 | 70 |
| 60 | 20 | 65 | 65 | 75 | 60 | 65 | 65 | 65 | 65 | 55 | 65 |
| 60 | 40 | 55 | 60 | 65 | 50 | 60 | 55 | 60 | 65 | 60 | 60 |
| 100 | 10 | 65 | 75 | 70 | 60 | 75 | 65 | 65 | 65 | 60 | 65 |
| 100 | 20 | 55 | 60 | 60 | 55 | 60 | 65 | 65 | 70 | 60 | 65 |
| 100 | 40 | 55 | 55 | 60 | 50 | 60 | 55 | 60 | 65 | 50 | 55 |
| 140 | 10 | 60 | 70 | 70 | 60 | 75 | 70 | 75 | 75 | 60 | 75 |
| 140 | 20 | 60 | 60 | 70 | 55 | 65 | 60 | 60 | 70 | 40 | 60 |

TABLE 6. MEASURED DELAY TIMES FOR THE D7ST TRANSISTORS

| Transistor Parameter | | Delay time, td, ns | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | |
| 100 | 10 | 115 | 175 | 180 | 190 | 120 | 155 | 150 | 150 |
| 100 | 20 | 120 | 140 | 140 | 145 | 130 | 150 | 125 | 140 |
| 100 | 40 | 120 | 135 | 120 | 125 | 120 | 130 | 120 | 125 |
| 150 | 10 | 100 | 140 | 170 | 160 | 120 | 150 | 150 | 160 |
| 150 | 20 | 130 | 135 | 135 | 130 | 130 | 150 | 130 | 140 |
| 150 | 40 | 125 | 135 | 120 | 120 | 135 | 130 | 110 | 120 |
| 250 | 10 | 125 | 135 | 140 | 135 | 125 | 135 | 125 | 125 |
| 250 | 20 | 130 | 130 | 115 | 125 | 135 | 130 | 115 | 125 |
| 250 | 40 | 135 | 120 | 110 | 115 | 130 | 125 | 115 | 115 |
| 350 | 10 | 120 | 145 | 145 | 140 | 130 | 135 | 120 | 125 |
| 350 | 20 | 125 | 135 | 120 | 125 | 120 | 125 | 115 | 120 |

TABLE 7. MEASURED RISE TIMES FOR THE D60T TRANSISTORS

| Transistor Parameter | | Rise time, tr, ns | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | | | |
| 40 | 10 | 90 | 90 | 80 | 80 | 70 | 75 | 70 | 60 | 70 | 65 |
| 40 | 20 | 100 | 95 | 85 | 90 | 85 | 70 | 65 | 60 | 65 | 65 |
| 40 | 40 | 65 | 65 | 60 | 65 | 65 | 75 | 75 | 65 | 65 | 65 |
| 60 | 10 | 95 | 90 | 75 | 105 | 80 | 140 | 115 | 90 | 105 | 90 |
| 60 | 20 | 100 | 90 | 85 | 90 | 85 | 85 | 80 | 75 | 80 | 80 |
| 60 | 40 | 80 | 75 | 75 | 75 | 75 | 80 | 75 | 70 | 85 | 70 |
| 100 | 10 | 115 | 100 | 80 | 95 | 90 | 100 | 100 | 90 | 90 | 90 |
| 100 | 20 | 80 | 70 | 65 | 80 | 70 | 100 | 95 | 90 | 90 | 95 |
| 100 | 40 | 80 | 70 | 70 | 65 | 65 | 75 | 75 | 70 | 65 | 70 |
| 140 | 10 | 100 | 95 | 90 | 90 | 85 | 130 | 110 | 94 | 100 | 100 |
| 140 | 20 | 90 | 80 | 70 | 75 | 75 | 100 | 90 | 80 | 80 | 80 |

TABLE 8. MEASURED RISE TIMES FOR THE D7ST TRANSISTORS

| Transistor Parameter | | Rise time, tr, ns | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | |
| 100 | 10 | 100 | 100 | 100 | 115 | 75 | 75 | 80 | 80 |
| 100 | 20 | 70 | 70 | 70 | 80 | 70 | 70 | 70 | 80 |
| 100 | 40 | 60 | 60 | 65 | 65 | 60 | 60 | 60 | 65 |
| 150 | 10 | 85 | 85 | 95 | 100 | 85 | 90 | 95 | 100 |
| 150 | 20 | 70 | 70 | 70 | 75 | 80 | 80 | 80 | 85 |
| 150 | 40 | 60 | 60 | 60 | | 65 | 60 | 65 | 70 |
| 250 | 10 | 75 | 80 | 70 | 80 | 60 | 60 | 80 | 70 |
| 250 | 20 | 60 | 70 | 65 | 70 | 65 | 65 | 65 | 80 |
| 250 | 40 | 65 | 65 | 65 | 85 | 65 | 65 | 60 | 80 |
| 350 | 10 | 90 | 95 | 100 | 90 | 75 | 75 | 85 | 80 |
| 350 | 20 | 70 | 70 | 75 | 80 | 70 | 75 | 75 | 75 |

TABLE 9. MEASURED STORAGE TIMES FOR THE D60T TRANSISTORS

| Transistor Parameter | | Storage time, ts, μs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | | | |
| 40 | 10 | 1.35 | 1.20 | 1.50 | 1.45 | 1.05 | 0.38 | 0.36 | 0.35 | 0.40 | 0.30 |
| 40 | 20 | 1.62 | 1.40 | 1.85 | 2.40 | 1.05 | 0.68 | 0.60 | 0.90 | 0.90 | 0.44 |
| 40 | 40 | 1.80 | 1.55 | 1.93 | 2.30 | 1.45 | 0.72 | 0.77 | 1.0 | 1.15 | 0.68 |
| 60 | 10 | 1.35 | 1.20 | 1.55 | 1.50 | 1.05 | 0.40 | 0.40 | 0.44 | 0.60 | 0.37 |
| 60 | 20 | 1.80 | 1.60 | 1.95 | 2.40 | 1.25 | 0.68 | 0.64 | 0.95 | 1.10 | 0.60 |
| 60 | 40 | 1.80 | 1.57 | 1.95 | 2.35 | 1.40 | 1.00 | 0.83 | 1.15 | 1.20 | 0.76 |
| 100 | 10 | 2.05 | 1.80 | 2.20 | 2.60 | 1.60 | 0.62 | 0.58 | 0.80 | 0.94 | 0.60 |
| 100 | 20 | 1.87 | 1.65 | 2.00 | 2.55 | 1.45 | 0.92 | 0.80 | 1.07 | 1.20 | 0.84 |
| 100 | 40 | 2.15 | 1.90 | 2.35 | 2.80 | 1.80 | 1.32 | 1.17 | 1.45 | 1.60 | 1.08 |
| 140 | 10 | 2.35 | 2.00 | 2.50 | 3.05 | 1.80 | 0.70 | 0.64 | 0.75 | 1.06 | 0.60 |
| 140 | 20 | 2.48 | 1.90 | 2.40 | 3.95 | 1.75 | 1.08 | 0.98 | 1.40 | 1.55 | 1.00 |

1.05 to 2.5-μsec range, and the range of 0.3 to 1.6 μsec for the unsaturated condition, with most falling in the range of 0.3 to 1.0 μsec. The storage times for the D7STs are given in Table 10. They cover the range of 2.8 to 6.7 μsec for the saturated condition, with most falling in the 3.0 to 6.5-μsec range, and the range of 1.4 to 6.7 μsec for the unsaturated condition, with most falling in the range of 2.0 to 5.0 μsec.

The fall times measured for the D60Ts and D7STs are given in Tables 11 and 12, respectively. They cover the range of 120 to 500 nsec for the D60Ts, with most of them falling in the 150 to 400-nsec range. They cover the range of 180 to 640 nsec for the D7STs, with most of them falling in the 220 to 400-nsec range.

From a comparison of these data with the data for the value of base-drive required to maximize operating frequency, it can be determined that the transistors can be operated under the base-drive conditions that produce minimum total device dissipation without compromising the maximum operating frequency.

## F. COLLECTOR-TO-EMITTER VOLTAGE ($V_{CE}$)

The collector-to-emitter voltage ($V_{CE}$) falls quickly from the value of $V_s$ to near zero at turn-on, as shown in Figure 17(a) (which is typical of all test points). After this initial drop in voltage, $V_{CE}$ varies, as shown in Figure 26 during the transistor on-time. The variation of the average $V_{CE}$ (SAT) with peak collector current and resonant frequency is shown in Figures 27 and 28 for the D60Ts and D7STs, respectively. The saturation voltage was defined as the collector-to-emitter voltage at the time of peak collector current. The saturation voltages were measured for the transistors under the base-drive conditions that minimized total device dissipation and are given in Tables 13 and 14.

Saturation voltages measured under these conditions are the optimum tradeoff between base-drive power and collector-emitter dissipation. The saturation voltage increased as either the peak collector current or resonant frequency increased (Figures 27 and 28).

TABLE 10. MEASURED STORAGE TIMES FOR THE D7ST TRANSISTORS

| Transistor Parameter | | Storage time, ts, μs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | |
| 100 | 10 | 3.9 | 2.8 | 4.3 | 3.9 | 1.6 | 1.4 | 1.9 | 1.4 |
| 100 | 20 | 4.3 | 3.0 | 4.6 | 4.4 | 2.8 | 2.1 | 3.0 | 2.6 |
| 100 | 40 | 4.1 | 3.5 | 4.4 | 3.9 | 3.4 | 3.0 | 3.6 | 3.1 |
| 150 | 10 | 4.3 | 2.9 | 4.6 | 4.3 | 2.0 | 1.6 | 2.0 | 1.6 |
| 150 | 20 | 4.4 | 3.3 | 4.6 | 4.3 | 3.0 | 2.3 | 3.4 | 2.9 |
| 150 | 40 | 4.3 | 3.7 | 4.6 | 4.8 | 4.2 | 3.5 | 4.3 | 4.1 |
| 250 | 10 | 4.4 | 3.4 | 4.9 | 4.8 | 2.3 | 2.1 | 2.5 | 2.4 |
| 250 | 20 | 4.8 | 3.9 | 5.3 | 5.1 | 3.5 | 2.8 | 4.0 | 3.4 |
| 250 | 40 | 6.3 | 5.0 | 6.7 | 6.4 | 5.2 | 5.0 | 6.7 | 5.2 |
| 350 | 10 | 6.5 | 4.7 | 6.4 | 6.2 | 2.7 | 2.7 | 2.9 | 2.8 |
| 350 | 20 | 6.9 | 5.0 | 6.9 | 6.4 | 4.5 | 3.7 | 4.8 | 4.1 |

TABLE 11. MEASURED FALL TIMES FOR THE D60T TRANSISTORS

| Transistor Parameter | | Fall time, $t_f$, ns | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | | | |
| 40 | 10 | 340 | 350 | 370 | 460 | 350 | 210 | 240 | 200 | 200 | 220 |
| 40 | 20 | 360 | 330 | 380 | 460 | 340 | 270 | 210 | 330 | 300 | 200 |
| 40 | 40 | 270 | 280 | 300 | 260 | 260 | 240 | 190 | 220 | 210 | 160 |
| 60 | 10 | 380 | 300 | 360 | 480 | 330 | 180 | 210 | 190 | 240 | 200 |
| 60 | 20 | 360 | 320 | 380 | 440 | 350 | 200 | 200 | 250 | 300 | 190 |
| 60 | 40 | 240 | 230 | 240 | 170 | 220 | 170 | 160 | 170 | 160 | 150 |
| 100 | 10 | 360 | 350 | 380 | 500 | 370 | 180 | 160 | 220 | 280 | 170 |
| 100 | 20 | 260 | 250 | 260 | 180 | 150 | 160 | 160 | 180 | 120 | 160 |
| 100 | 40 | 200 | 160 | - | - | 200 | 210 | 180 | 200 | 120 | 180 |
| 140 | 10 | 280 | 300 | 300 | 280 | 350 | 200 | 190 | 200 | 205 | 160 |
| 140 | 20 | - | 180 | 120 | - | 240 | 220 | 180 | 180 | 140 | 200 |

TABLE 12. MEASURED FALL TIMES FOR THE D7ST TRANSISTORS

| Transistor Parameter | | Fall time, $t_f$, ns | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonance Frequency fr, kHz | | | | | | | | |
| 100 | 10 | 600 | 460 | 640 | 600 | 270 | 220 | 350 | 210 |
| 100 | 20 | 400 | 310 | 400 | 400 | 320 | 210 | 340 | 300 |
| 100 | 40 | 230 | 210 | 220 | 210 | 240 | 200 | 240 | 200 |
| 150 | 10 | 550 | 400 | 530 | 550 | 290 | 180 | 320 | 260 |
| 150 | 20 | 320 | 250 | 320 | 230 | 290 | 200 | 270 | 230 |
| 150 | 40 | 300 | 260 | 280 | 220 | 320 | 270 | 300 | 240 |
| 250 | 10 | 330 | 280 | 340 | 310 | 270 | 260 | 250 | 240 |
| 250 | 20 | 350 | 330 | 270 | 320 | 440 | 310 | 390 | 360 |
| 250 | 40 | - | - | - | - | - | - | - | - |
| 350 | 10 | - | - | - | - | 280 | 280 | 270 | 270 |
| 350 | 20 | - | - | - | - | - | - | - | - |

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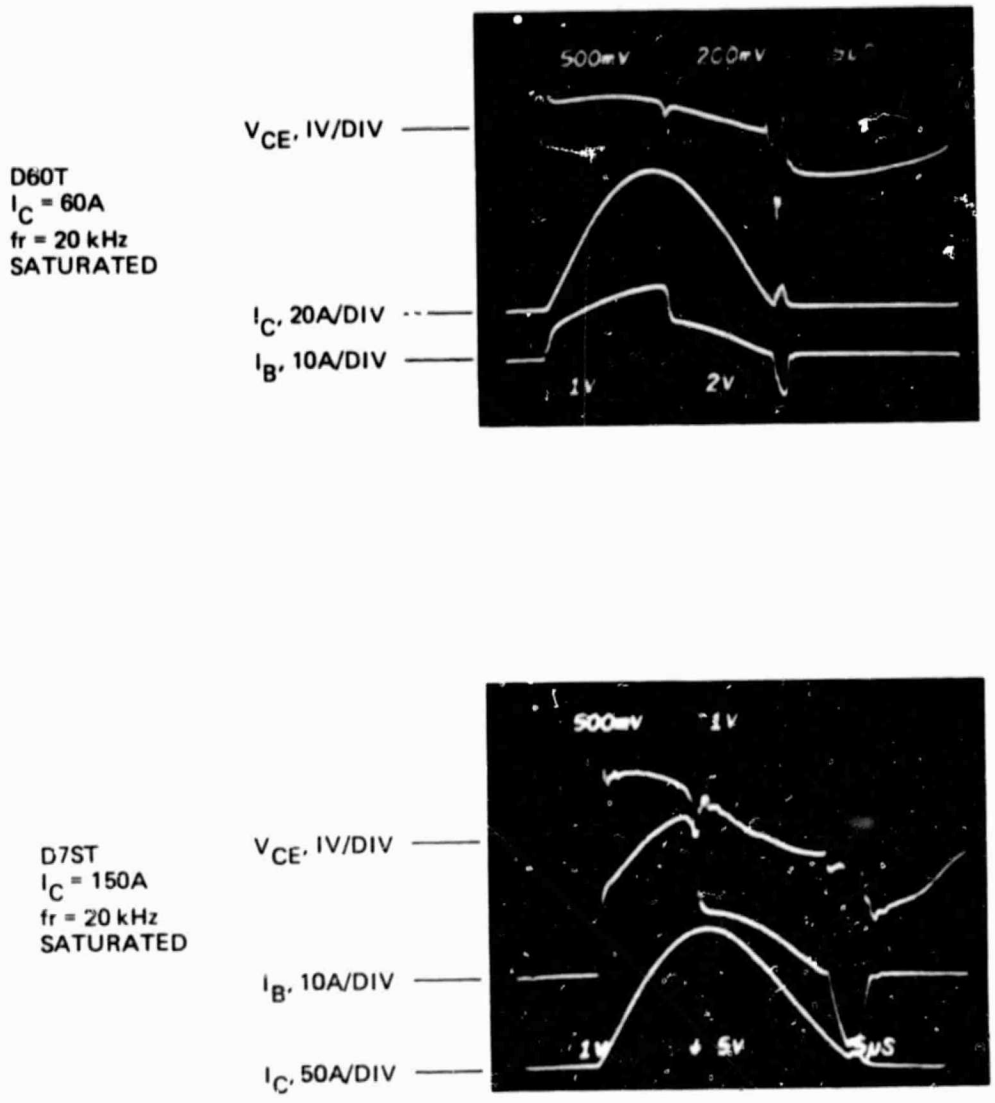



Figure 26. Typical waveforms of saturation voltage for the D60Ts and D7STs.

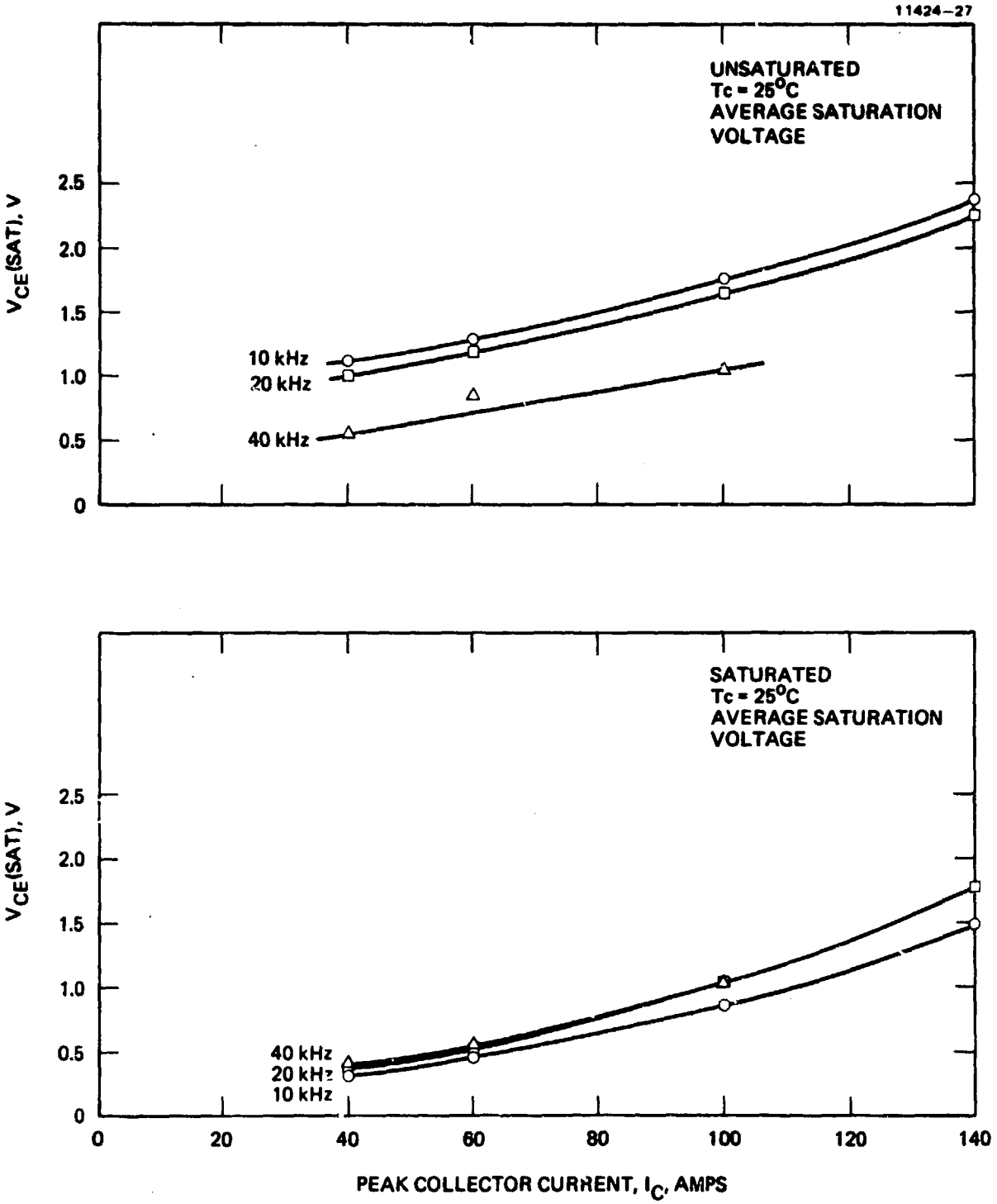



Figure 27. Variation of saturation voltage with peak collector current and resonant frequency for the D60Ts (average of five transistors).

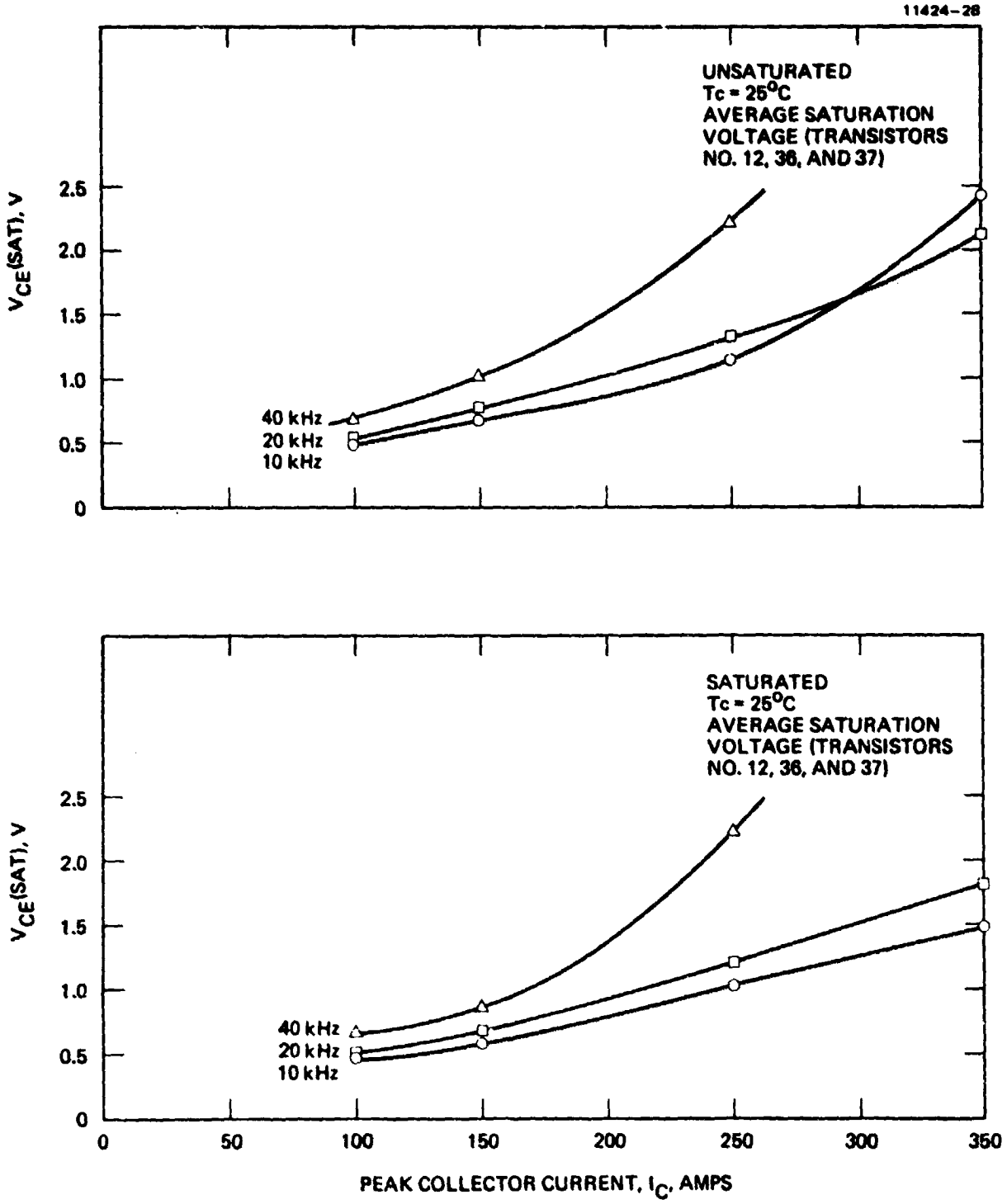



Figure 28. Variation of saturation voltage with peak collector current and resonant frequency for the D7STs (average of three transistors).

TABLE 13. MEASURED SATURATION VOLTAGES FOR THE D60T TRANSISTORS

| Transistor Parameter | | $V_{ce\ (sat)}$, v | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | | | |
| 40 | 10 | 0.34 | 0.30 | 0.30 | 0.32 | 0.34 | 1.15 | 1.10 | 1.10 | 1.10 | 1.15 |
| 40 | 20 | 0.40 | 0.32 | 0.30 | 0.35 | 0.36 | 0.64 | 0.85 | 0.90 | 1.05 | 1.20 |
| 40 | 40 | 0.40 | 0.40 | 0.37 | 0.40 | 0.43 | 0.56 | 0.52 | 0.54 | 0.62 | 0.60 |
| 60 | 10 | 0.52 | 0.49 | 0.44 | 0.75 | 0.66 | 1.35 | 1.35 | 1.25 | 1.30 | 1.35 |
| 60 | 20 | 0.54 | 0.48 | 0.48 | 0.60 | 0.55 | 0.92 | 1.10 | 1.15 | 1.30 | 1.40 |
| 60 | 40 | 0.56 | 0.56 | 0.52 | 0.60 | 0.58 | 0.77 | 0.70 | 0.94 | 1.00 | 0.78 |
| 100 | 10 | 0.90 | 0.84 | 0.74 | 0.85 | 0.96 | 1.90 | 1.75 | 1.65 | 1.85 | 1.85 |
| 100 | 20 | 1.00 | 0.88 | 0.88 | 1.10 | 0.96 | 1.65 | 1.60 | 1.60 | 1.60 | 1.70 |
| 100 | 40 | 0.96 | 0.88 | 0.84 | 1.10 | 1.00 | 1.00 | 1.00 | 1.00 | 1.30 | 1.10 |
| 140 | 10 | 1.35 | 1.35 | 1.25 | 1.80 | 1.80 | 2.20 | 2.23 | 2.15 | 2.40 | 2.50 |
| 140 | 20 | 1.60 | 1.50 | 1.40 | 2.10 | 1.85 | 1.70 | 2.05 | 2.00 | 2.40 | 2.50 |

TABLE 14. MEASURED SATURATION VOLTAGES FOR THE D7ST TRANSISTORS

| Transistor Parameter | | $V_{ce\ (sat)}$, v | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonant Frequency fr, kHz | | | | | | | | |
| 100 | 10 | 0.44 | 0.64 | 0.40 | 0.42 | 0.51 | 0.56 | 0.46 | 0.50 |
| 100 | 20 | 0.48 | 0.60 | 0.49 | 0.50 | 0.52 | 0.56 | 0.52 | 0.54 |
| 100 | 40 | 0.64 | 0.68 | 0.64 | 0.68 | 0.66 | 0.70 | 0.64 | 0.70 |
| 150 | 10 | 0.57 | 0.73 | 0.55 | 0.56 | 0.64 | 0.72 | 0.65 | 0.68 |
| 150 | 20 | 0.70 | 0.73 | 0.64 | 0.72 | 0.76 | 0.84 | 0.77 | 0.83 |
| 150 | 40 | 0.92 | 0.92 | 0.76 | 0.88 | 1.04 | 1.00 | 0.96 | 0.94 |
| 250 | 10 | 1.04 | 2.70 | 1.02 | 1.04 | 1.02 | 1.67 | 1.12 | 1.24 |
| 250 | 20 | 1.20 | 1.54 | 1.16 | 1.28 | 1.30 | 1.60 | 1.20 | 1.40 |
| 250 | 40 | 2.10 | 2.50 | 2.00 | 2.60 | 2.00 | 3.20 | 2.20 | 2.30 |
| 350 | 10 | 1.26 | 2.80 | 1.54 | 1.60 | 2.20 | 3.90 | 2.20 | 2.60 |
| 350 | 20 | 1.70 | 2.40 | 1.70 | 2.00 | 1.90 | 2.50 | 2.00 | 2.30 |

## G. OUTPUT CAPACITANCE, $C_{OB}$

The construction of high-power transistors necessarily requires the use of a large-area junction to handle the high currents. Large-area junctions result in a very undesirable characteristic (i.e., large junction capacitances). Published data for the D60T give a small-signal, 1-MHz measurement of $C_{OB}$, which does not accurately depict the nonlinear character of $C_{OB}$ on a large-signal basis such as will be encountered in high-power inverter applications. As shown in Figure 29, $C_{OB}$ appears as a capacitor connected between the collector and base of transistor, $Q_2$. Its effect is particularly detrimental when $Q_2$ is in its OFF state and $Q_1$ is switched ON. The turn-on of $Q_1$ causes a voltage transient across $C_{OB}$ of $Q_2$, and, according to the relationship

$$i_{CB} = \frac{dV}{dt} C_{OB} \quad , \tag{1}$$

a current is injected into the base that, if not properly suppressed, will turn $Q_2$ on and be multiplied by the gain ($\beta$) of $Q_2$. This current transient, at the time when collector voltage is high, is sufficient to cause significant power dissipation when operating at high frequencies and is a dV/dt limitation on the transistor.

The test circuit of Figure 29 was used to measure the output capacitance of the D60Ts and D7STs. The drive sequence for $Q_1$ and $Q_2$ was asymmetrical with both $Q_1$ and $Q_2$ off for long periods. Load resistor $R_L$ guaranteed that the $Q_2$ collector voltage was held at zero during $Q_1$ off-times. $Q_1$ was then turned on while $Q_2$ was held off by the negative bias connected to the bottom of $R_B$. The injected base current ($i_{CB}$) flowed through $R_B$ and was measured with a calibrated current probe, while the $Q_2$ collector voltage transition (dV/dt) was measured with a voltage probe. Collector-to-base capacitance ($C_{ob}$) was then calculated from

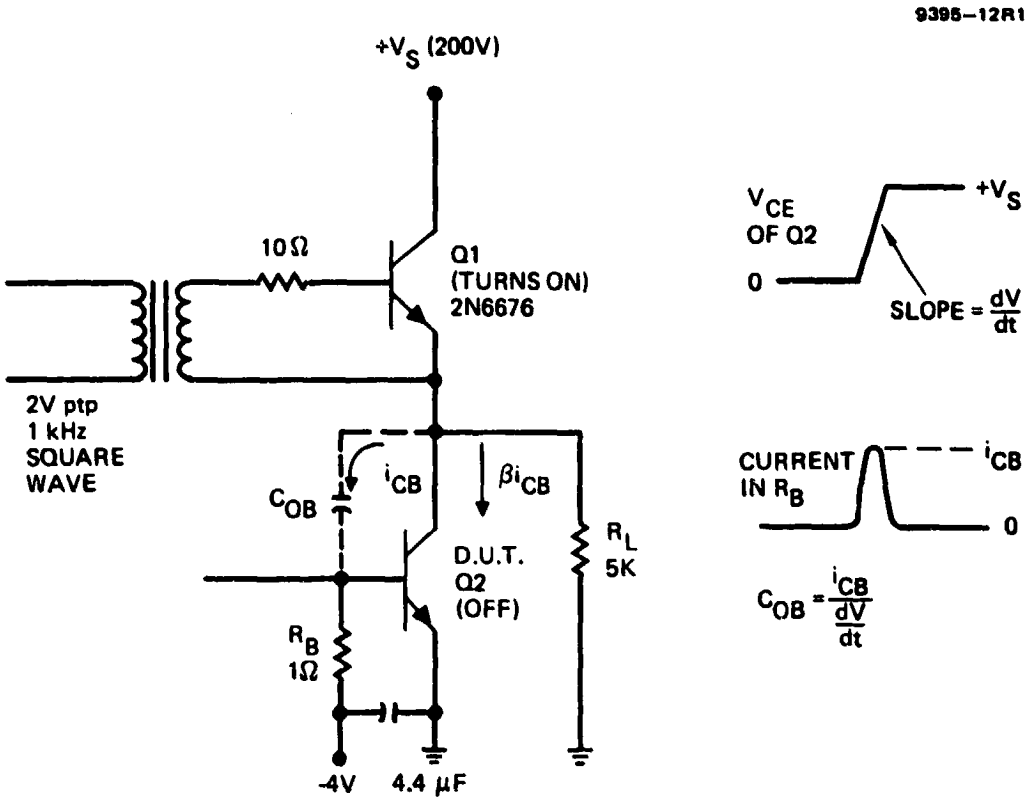



Figure 29. Test circuit to measure $C_{OB}$ of a transistor.

$$C_{OB} = \frac{i_{CB}}{dV/dt} \quad . \qquad (2)$$

The output capacitances of the transistors tested are given in Table 15 and averaged 2140 pF for the D60Ts, and 3696 pF for the D7STs.

TABLE 15. Output Capacitance ($C_{OB}$) of the D60T and D7ST Transistors Tested

| Transistor Type | D60T | | | | | D7ST | | | |
|---|---|---|---|---|---|---|---|---|---|
| Transistor Number | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 12 | 15 | 36 | 37 |
| $C_{OB}$, pF | 2320 | 2140 | 2050 | 2126 | 2079 | 3710 | 3834 | 3465 | 3774 |

H. INPUT CAPACITANCE, $C_{IB}$

The maximum operating frequency of a switching transistor is a direct function of the time required to charge (delay time) and discharge (storage time) the base-to-emitter capacitance ($C_{IB}$). To properly design the base-drive circuit to adequately handle the peak-base-drive currents required, a worst-case value for $C_{IB}$ is required. The base-emitter capacitance was measured with the test circuit shown in Figure 30. This test was performed with the collector open, which eliminates parallel effects from $C_{OB}$. The open collector should approximate operation in an SRI since the collector current in an SRI will be zero at the time of turn-off.

In Figure 30, $Q_1$ (the DUT) was turned ON by a pulse ($V_g$) from the pulse generator. This pulse also turned $Q_2$ OFF. After the base of $Q_1$ had been fully charged, $V_g$ reverse biased D1 and turned $Q_2$ ON. $Q_2$ is a constant current source and drew a constant value of $i_B$ from the base emitter junction of $Q_1$. After the excess charge had been removed, $V_{BE}$ fell at a relatively constant rate ($dV_{BE}/dt$). From the relationship

$$\frac{dV_{BE}}{dt} = \frac{i_B}{C_{IB}} \tag{3}$$

it follows that

$$C_{IB} = \frac{i_B}{dV_{BE}/dt} \quad . \tag{4}$$

The input capacitances of the transistors tested are given in Table 16 and averaged 76,100 pF for the D60Ts and 118,500 pF for the D7STs.

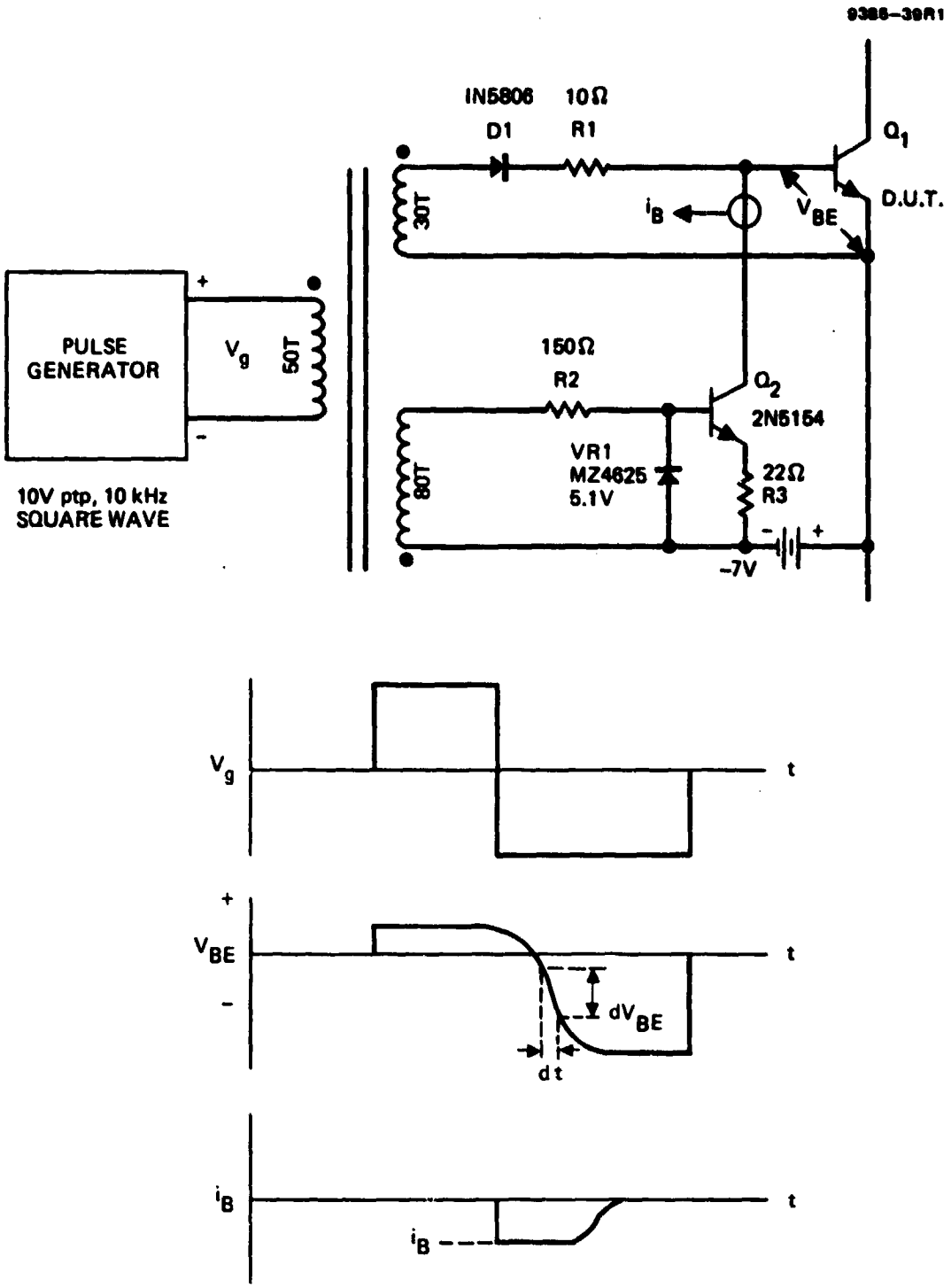



Figure 30. Test circuit and waveforms for measuring $C_{ib}$ of a transistor.

TABLE 16. Input Capacitance ($C_{IB}$) of the D60T and D7ST Transistors Tested

| Transistor Type | D60T | | | | | D7ST | | | |
|---|---|---|---|---|---|---|---|---|---|
| Transistor Number | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 12 | 15 | 36 | 37 |
| $C_{IB}$, pF | 71,560 | 73,180 | 81,000 | 87,400 | 67,500 | 96,800 | 112,500 | 126,500 | 138,000 |

## SECTION 4

## BASE-DRIVE DEVELOPMENT

A base-drive strategy was developed for both the D60T and D7ST transistors for when they are used as switches on SRIs. The strategy is the same for both types of transistors and is described in the following section.

### A. STRATEGY

The strategy developed to drive both the D60T and D7ST transistors is as follows. Regenerative (or proportional) feedback of the collector current is used since it minimizes the required power from the rest of the base-drive circuitry. At the same time, the transistor is maintained at a constant $\beta$ (except during the leading-edge pulse) which saves on base-drive power. The base current is allowed to go to zero as the collector current goes to zero, which minimizes the storage time. The base-drive parameters from the transistor characterization that resulted in minimum total device dissipation are employed, and the base-emitter junction is kept reverse biased during the transistor off-time, which eliminates dV/dt turn-on caused by $C_{OB}$.

### B. REQUIREMENTS

A study of the data obtained in the transistor characterization indicates that it is not practical to operate either the D60T or the D7ST transistors at 70% of their rated currents and a resonant frequency of 40 kHz. It was not possible to get either transistor into saturation under these conditions. The long storage time (6 to 7 μsec) for the D7ST transistor also limits its usefulness at 40 kHz. Therefore, the maximum practical operating frequency (resonant frequency) for these transistors at high currents is in the 20 to 25 kHz range. The base-drive circuit was developed for 25 kHz.

Data taken on the D60T transistors at 20 kHz and 100 A show that the minimum device dissipation occurs at a regenerative feedback ratio of 7:1, with a leading-edge pulse of 12 A amplitude and 15 μsec width. The required

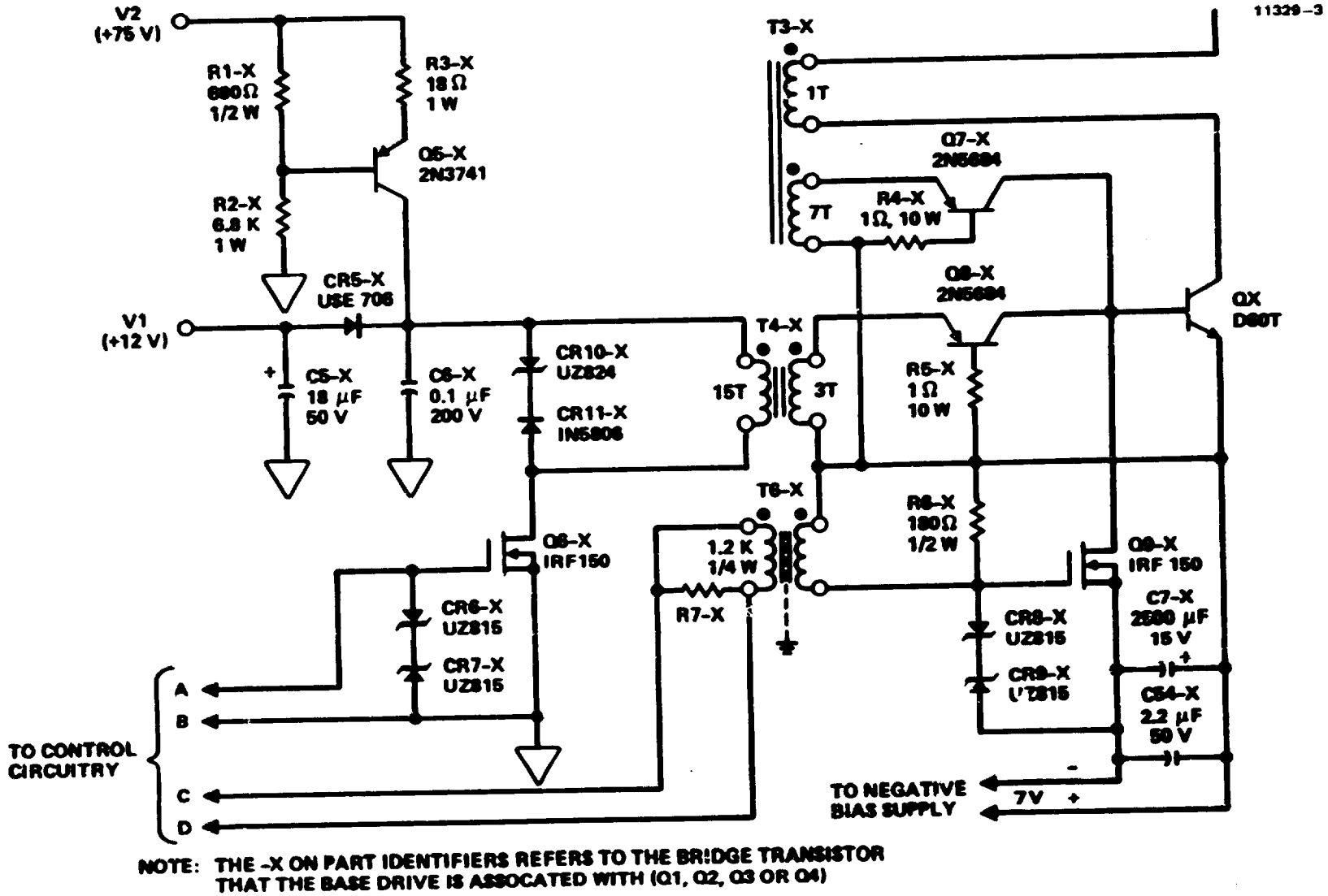
base-drive at 25 kHz should be the same regenerative feedback ratio of 7:1, and a leading-edge pulse of 12 A amplitude that is 12 μsec wide (reduced from 15 μsec by the ratio of 20 kHz to 25 kHz). Data taken on the D7ST transistors at 20 kHz and 250 A show that the minimum device dissipation occurs at a regenerative feedback ratio of 10:1, with a leading-edge pulse of 30 A amplitude and 12.5 μsec width. The required base-drive at 25 kHz should be the same regenerative feedback ratio of 10:1, with a leading-edge pulse of 30 A amplitude and 10 μsec width (reduced from 12.5 μsec by the ratio of 20 kHz to 25 kHz).

It is important that the leading-edge pulse have a rise time of 1 μsec or less in order to minimize the turn-on time and get the transistor into saturation quickly. The turn-off pulse (negative $I_B$ pulse) needs to be large in amplitude in order to minimize the storage time, which will then allow for maximum utilization of the series resonant tank.

## C. CIRCUIT DEVELOPMENT

Conventional transformer coupled base-drive circuits will not provide a 30 A pulse with a rise time of 1 μsec or less because of the leakage inductance of the transformer, base-emitter inductance of the transistor, and stray inductance of the wiring. Direct switching of the 30 A current pulse into the base was considered, but rejected because of the poor efficiency (less than 50%) for that type of base-drive. It was decided to use a transformer-coupled base-drive circuit and overcome the inductance problem by "brute forcing" it with voltage.

The circuit of Figure 31 was developed to provide a 30 A pulse with a rise time of 1 μsec or less and a 7:1 (10:1 for the D7ST) regenerative feedback ratio. Referring to Figure 31, $Q_5$-X forms a constant-current source that charges capacitor $C_6$-X to the voltage potential of $V_2$. When $Q_6$-X is turned on to apply a leading-edge pulse to QX, the high voltage charge ($V_2$ = 75 V) on $C_6$-X is applied to the primary of $T_4$-X. This high voltage overcomes the effect of the leakage inductance of $T_4$-X, the stray wiring inductance, and the base-emitter inductance of QX, allowing the base current to rise to 30 A in approximately 1 μsec. After the charge on $C_6$-X has decayed




NOTE: THE -X ON PART IDENTIFIERS REFERS TO THE BRIDGE TRANSISTOR THAT THE BASE DRIVE IS ASSOCATED WITH (Q1, Q2, Q3 OR Q4)

Figure 31. 10-kW base drive circuitry.

to potential $V_1$ (12 V), the remainder of the leading-edge pulse is supplied from $V_1$ through $CR_5$-X. The width of the leading edge pulse is controlled by the on-time of $Q_6$-X.

The regenerative feedback is supplied by transformer $T_3$-X. A separate transformer is used for the regenerative feedback so that the leakage inductance of $T_4$-X (supplying the leading-edge pulse) can be minimized. Transistors $Q_7$-X and $Q_8$-X are used to isolate the transformers so that the base of QX can be held at a negative bias during the time that it is turned-off. $Q_9$-X supplies the turn-off pulse to the base of QX, and holds it at the negative bias level of -7 V. $T_6$-X is used to provide an isolated turn-off pulse to $Q_9$-X during the on-time of QX.

## D. TESTING

The base-drive design was tested using the test setup shown in Figure 32, which is a half-bridge SRI with a zero impedance load and resonant frequency of 25-kHz. The amplitude of the tank current was controlled by varying $V_S$, and the duty cycle of $Q_1$ and $Q_2$ was varied by way of the control circuit. The test setup was operated without any tank circuit feedback.

### 1. D60T Transistors

Transistor 60-5 was installed as $Q_1$ and 60-4 was installed as $Q_2$. The turns-ratios of T3-1 and T3-2 were set at 7:1, and V1 and V2 of Figure 31 were adjusted to give a leading edge pulse amplitude of 12 A. The leading edge pulse duration was set at 12 μsec by the control circuit, and the tank current was adjusted for 100 A peak. The tank current, $Q_2$ collector current, and $Q_2$ base current are shown in Figure 33(a). The base current and base-emitter voltage are shown in Figure 33(b) for the same conditions, while Figure 33(c) shows the base current, tank current, and saturation voltage. These oscilloscope traces show a saturation voltage of 1.5 V and a storage time of 1.5 μsec, which is in good agreement with the transistor characterization data.

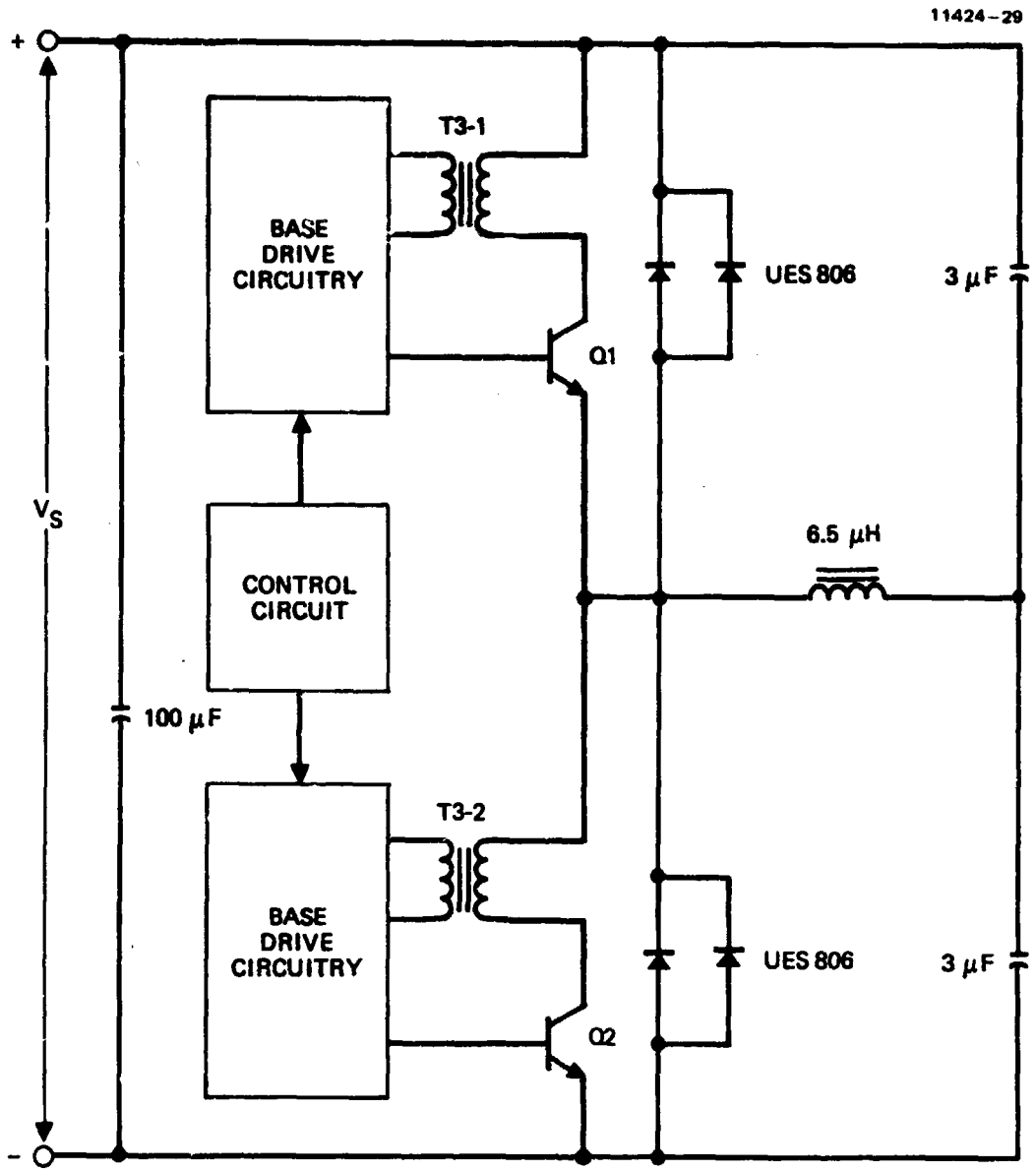



Figure 32. Test setup for testing the base-drive circuitry.

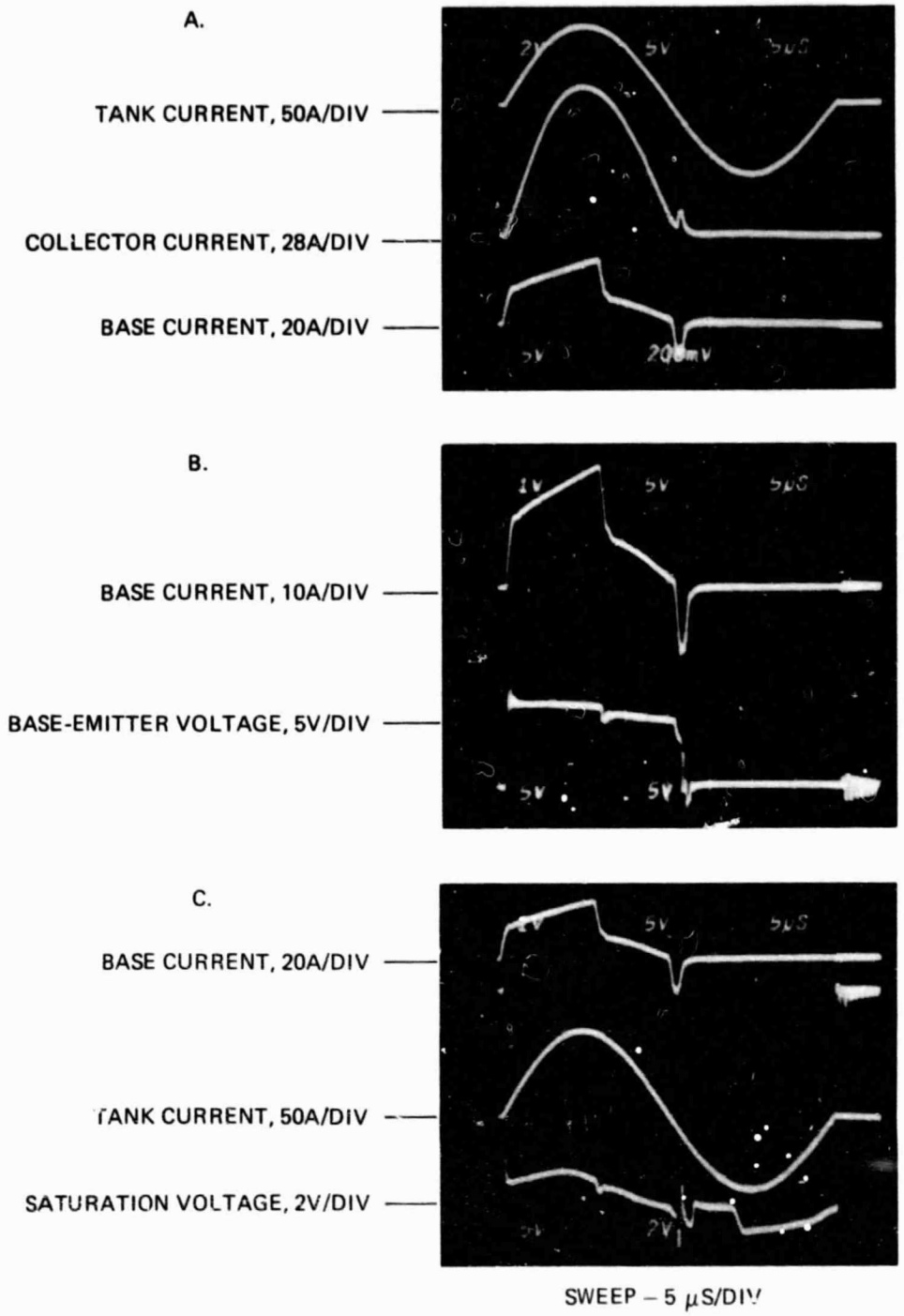



Figure 33. D60T transistor waveforms during test of the base-drive circuit.

## 2. D7ST Transistors

Transistor number 36 was installed as $Q_1$ and number 12 was installed as $Q_2$ (Figure 32). The turns-ratios of T3-1 and T3-2 were set at 10:1, and V1 and V2 of Figure 31 were adjusted to give a leading edge pulse amplitude of 30 A. The leading edge pulse duration was set at 10 μsec by the control circuit and the tank current was adjusted for 250 A peak. The tank current, $Q_2$ collector current, and $Q_2$ base current are shown in Figure 34(a). The base current and base-emitter voltage are shown in Figure 34(b), which shows a storage time of approximately 3 μsec. Figure 34(c) shows the base current, tank current, and saturation voltage for a peak tank current of 150 A. The saturation voltage under these conditions is approximately 1.2 V. Figure 35(a) shows that the saturation voltage increased to approximately 2.3 V as the peak tank current increased to 200 A. When the peak tank current was increased to 250 A the saturation voltage increased to 9 V, as shown in Figure 35(b), indicating that the transistor did not have enough base-drive even though the transistor characterization data indicate that the base-drive should have been adequate. Reducing the T3-1 and T3-2 turns-ratios to 8:1 dropped the saturation voltage to 5 V. By increasing V1 of Figure 31 until the base current at the time of peak collector current was 70 A, the saturation voltage was reduced to approximately 2 V (Figure 35(c)).

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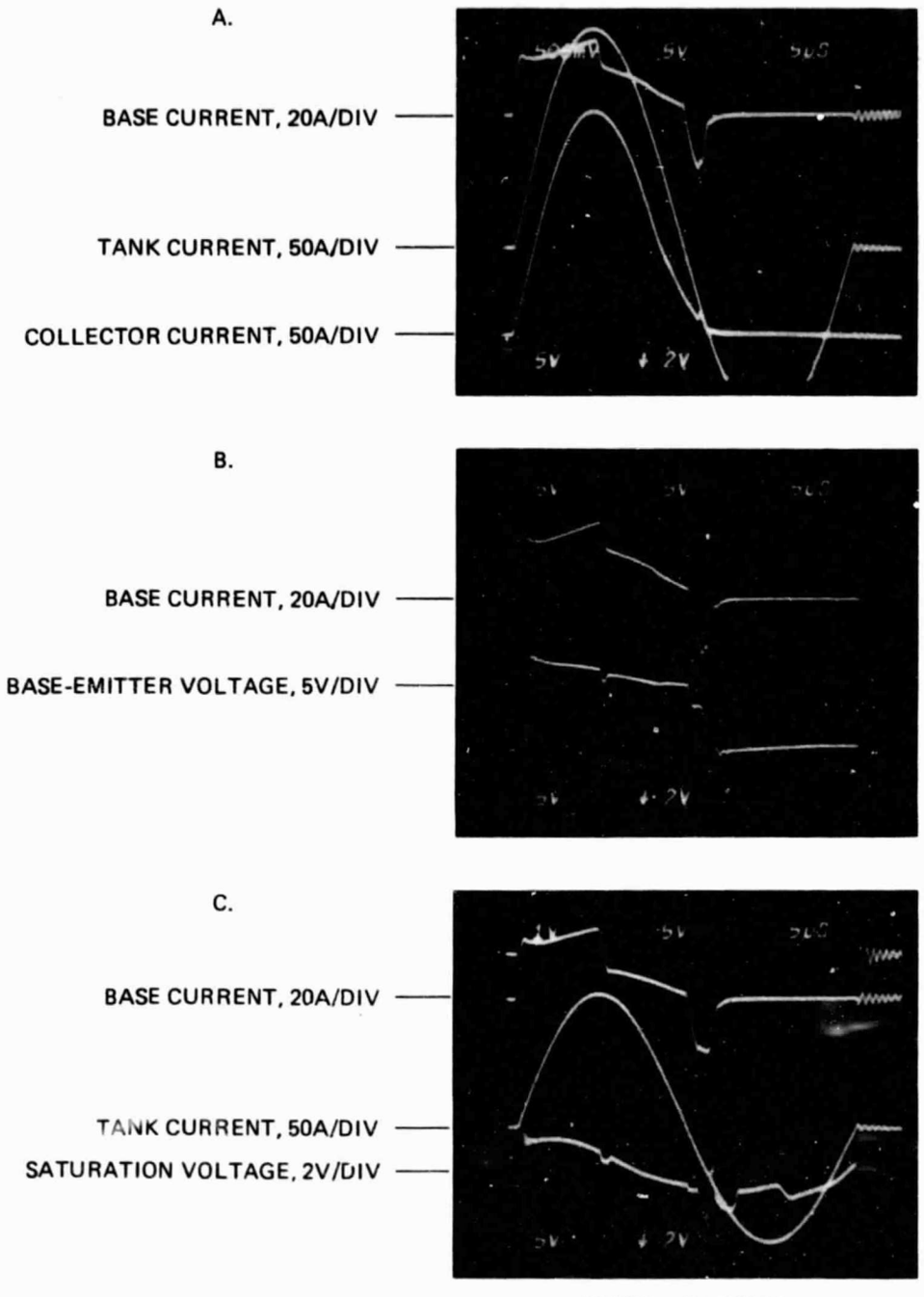


Figure 34. D7ST transistor waveforms during test of the base drive circuit.

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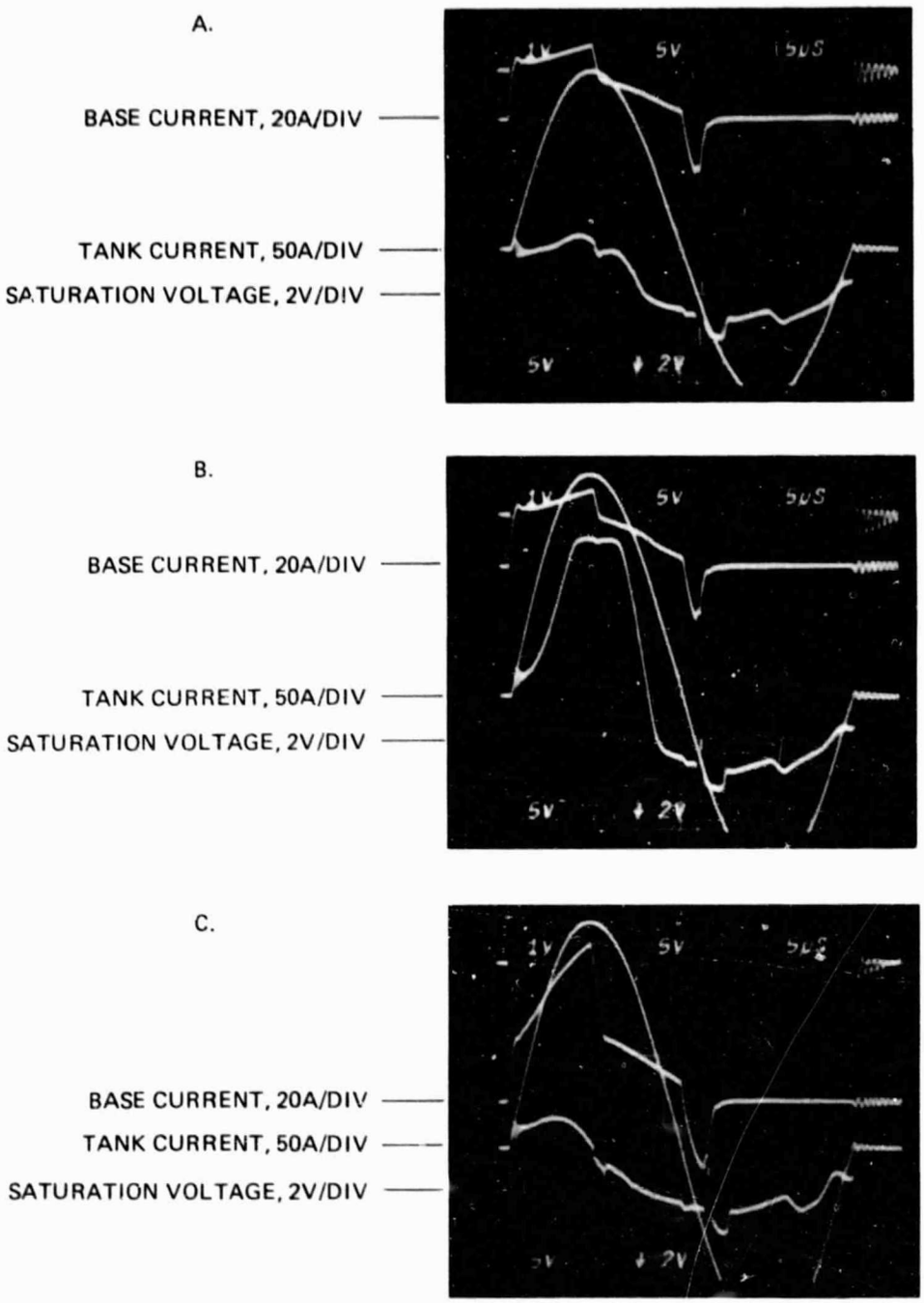



Figure 35. D7ST transistor saturation voltage variation for different base currents.

# SECTION 5

# CONVERTER DESIGN

The 10-kW series resonant converter was designed to meet the following specifications:

- Resonant frequency — 25 kHz
- Main bus voltage — 230 to 270 Vdc
- Output voltage — variable from 200 to 500 Vdc.
- Output current limit — adjustable from 0 to 20 A
- Output power — 10-kW minimum at 500 Vdc output
- Input power — 208 Vac ±10%, 3$\phi$, 60 Hz, 4 wire
- Output voltage regulation — ±2% for input voltage variations of ±10% and/or load variations between 10% and full load current
- Output ripple — less than 1% rms
- Remote voltage sensing — terminals provided on the rear of the chassis
- Isolation — all output terminals are isolated from the chassis, and either the positive or negative terminal may be floated ±100 Vdc from chassis ground.
- Mode indication — a local and remote indication is supplied to indicate when the inverter is in the current-limited mode
- Meters — output voltage and current meters on the front panel
- AC power control — a front panel switch for control power and front panel breaker for the main power
- Cooling — forced air
- Mounting — standard 19-in. EIA rack.

The decision was made to use the D60T transistor as the basic switch for this design because of its shorter storage time and because of the very limited availability of the D7ST transistors. The use of the D60T transistors at the 10-kW level requires a full-bridge circuit which uses twice as many switches as a half-bridge (4 versus 2), but results in a peak tank current that is

one-half that for a half-bridge. The lower peak tank current gives rise to a more efficient design because of lower $I^2R$ losses and lower transistor saturation voltages.

The major features of the design are discussed in the following sections.

## A. BRIDGE AND TANK CIRCUITRY

A schematic of the bridge and tank circuitry is shown in Figure 36. Transistors Q1 through Q4 are the four switches of the full-bridge, and T3-1 through T3-4 provide the regenerative feedback base drive for these transistors. SR1 and SR2 are saturable reactors that limit the di/dt that Q1 through Q4 see, allowing these transistors to saturate quickly, and thereby reduce power losses. SR1 and SR2 saturate in approximately 500 nsec, after which they are effectively out of the circuit. Diodes CR1 through CR4 provide the paths for returning excess energy in the tank circuit to the source. Diodes CR54-1 through CR54-4 were added to suppress voltage spikes caused by SR1, SR2, and stray wiring inductance. They are mounted as close to Q1 through Q4 as possible, as are C3 and C4, which provide a low impedance AC clamp for CR54-1 through CR54-4 to work into.

The series resonant tank is composed of C1, L1, T1, and T2. C1 is made from four polypropylene capacitors in parallel and has a total capacitance of 0.875 μF. Capacitor C1 resonates with the inductance of L1 and the primary leakage inductance of T1 at a resonate frequency of 25-kHz. L1 was fabricated by winding 18 turns of 165/30 (16,500 circular mils) Litz wire on an Indiana General-type 8200 ferrite core with a 12.9 $cm^2$ cross sectional area. Ferrite was used for both L1 and T1 because of its lower losses. The design of these components could be further improved by using Ceramic Magnetics Inc. type MN60L ferrite instead of the Indiana General type 8200. T1 is used to remove energy from the tank circuit and supply it to the load. The primary of T1 was wound with 18 turns of 165/30 Litz wire and each of the two secondaries was wound with 24 turns of two 150/36 Litz wires in parallel (a total of 7500 circular mils). The core used was the same as for L1. T2 is a current transformer that provides a tank-current feedback-signal to the control circuit.

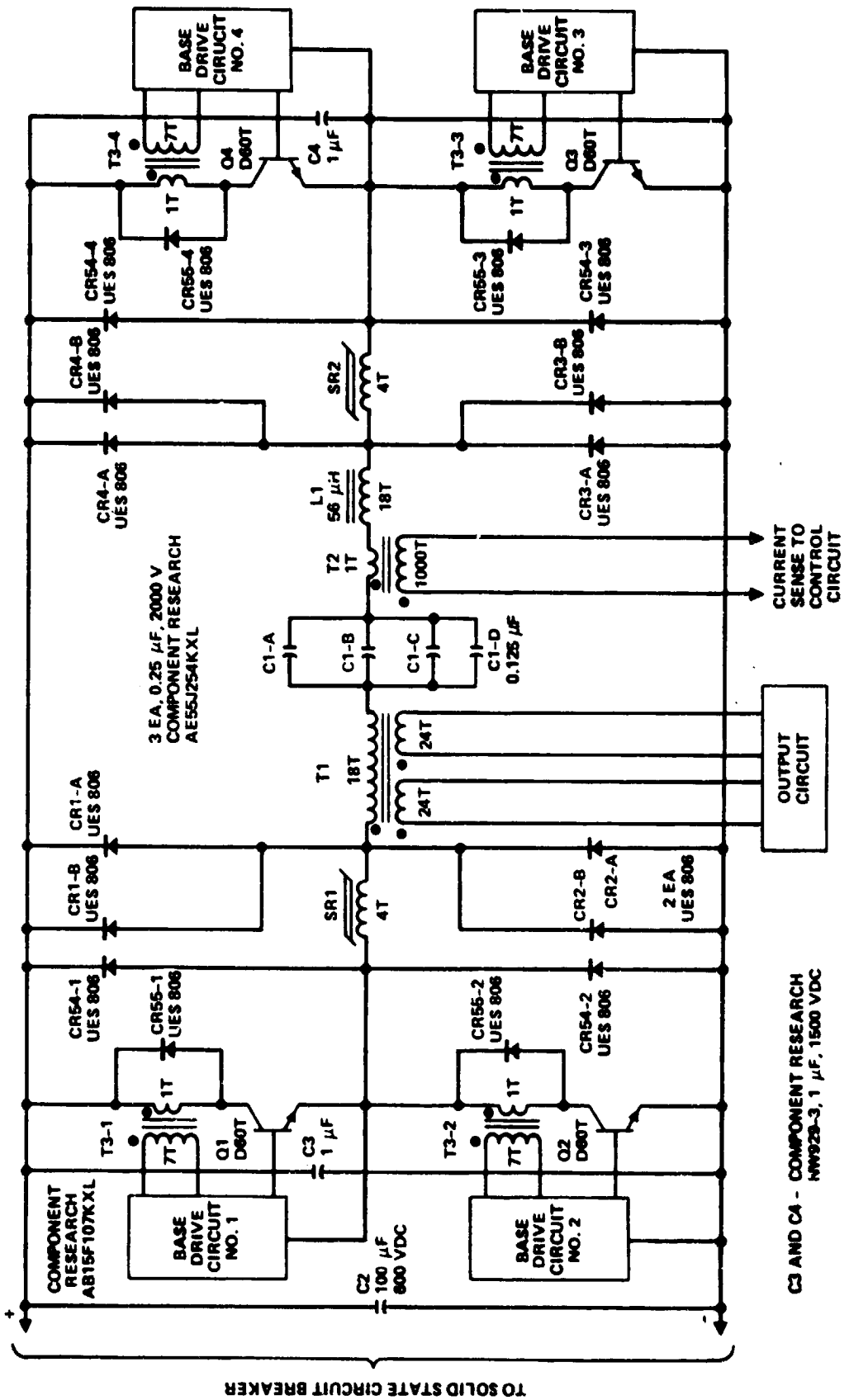



Figure 36. 10-kW bridge and tank circuitry.

## B. OUTPUT CIRCUIT

The schematic of the output circuitry is shown in Figure 37. The AC current supplied by T1 is rectified by two full-bridge circuits, CR12 through CR15, and CR16 through CR19. The split secondary on T1 is a convenient method of stacking the rectifiers in series to handle the output voltage. The rectified current is filtered by C8-A through C8-D, measured by M1, and then supplied to the output. The output voltage is measured by M2 and sensed as a feedback-signal for the control circuit by R10 through R14 and R17. R15, R16, and C9 are added to form a lead-lag network for compensating the voltage control loop.

## C. BASE DRIVE CIRCUIT

The base drive schematic was presented (Figure 31) and discussed in Section 4.

## D CONTROL CIRCUIT

The control circuit schematic is shown in Figures 38(a) through 38(d). The output voltage feedback-signal is isolated from the floating output by isolation amplifier AR1. This feedback signal is then compared against the output voltage reference signal (from R28) and the difference integrated by the feedback around AR2. R25 forms a lead network with C10 for loop compensation. The integrator is confined to the normal operating range by the clamp circuit comprised of R24, R27, CR20, and VR6. Comparator U16 senses when the output voltage is more than 25 V higher than the referenced level and immediately phases the inverter off until the output voltage drops down to the referenced level. This keeps the output voltage under control during transient conditions.

The average output current is related to the average current in the series resonant tank circuit by the turns ratio of T1. Therefore, the average tank current can be sensed and used to control the output current while at the same time protecting the bridge and tank circuit components. The tank current is

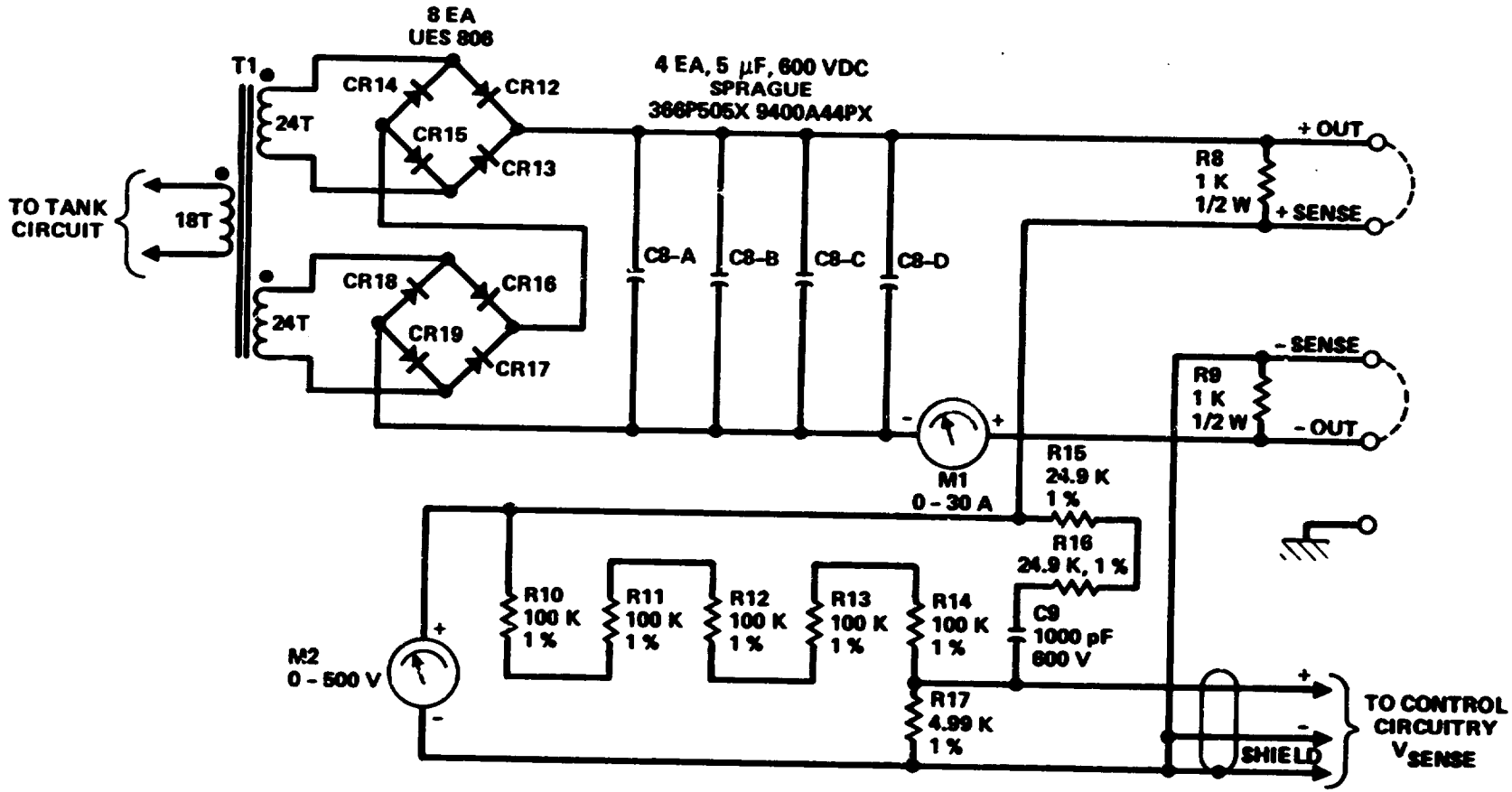



Figure 37. 10-kW output circuitry.

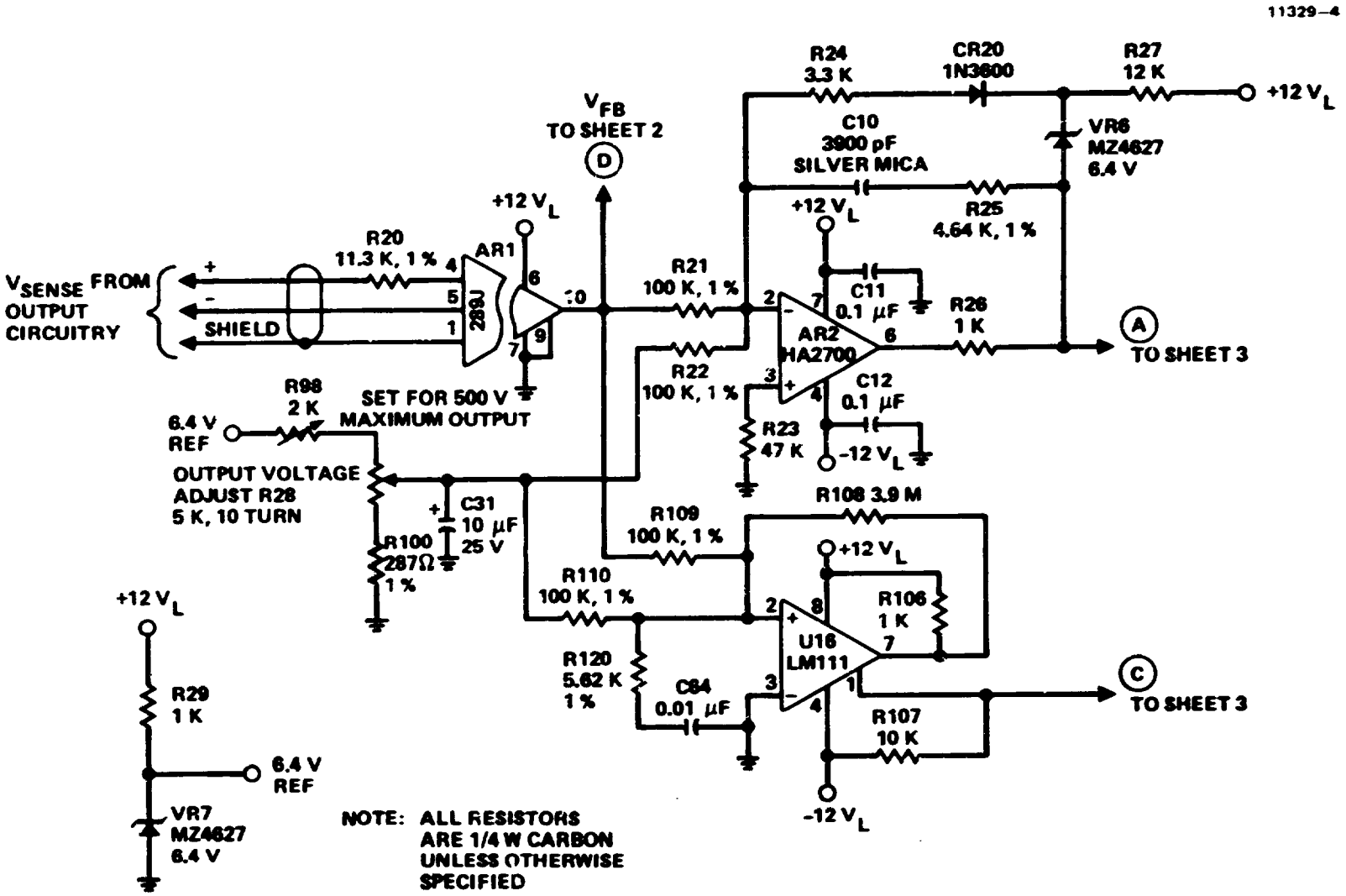



Figure 38(a). 10-kW control circuitry (output voltage feedback).

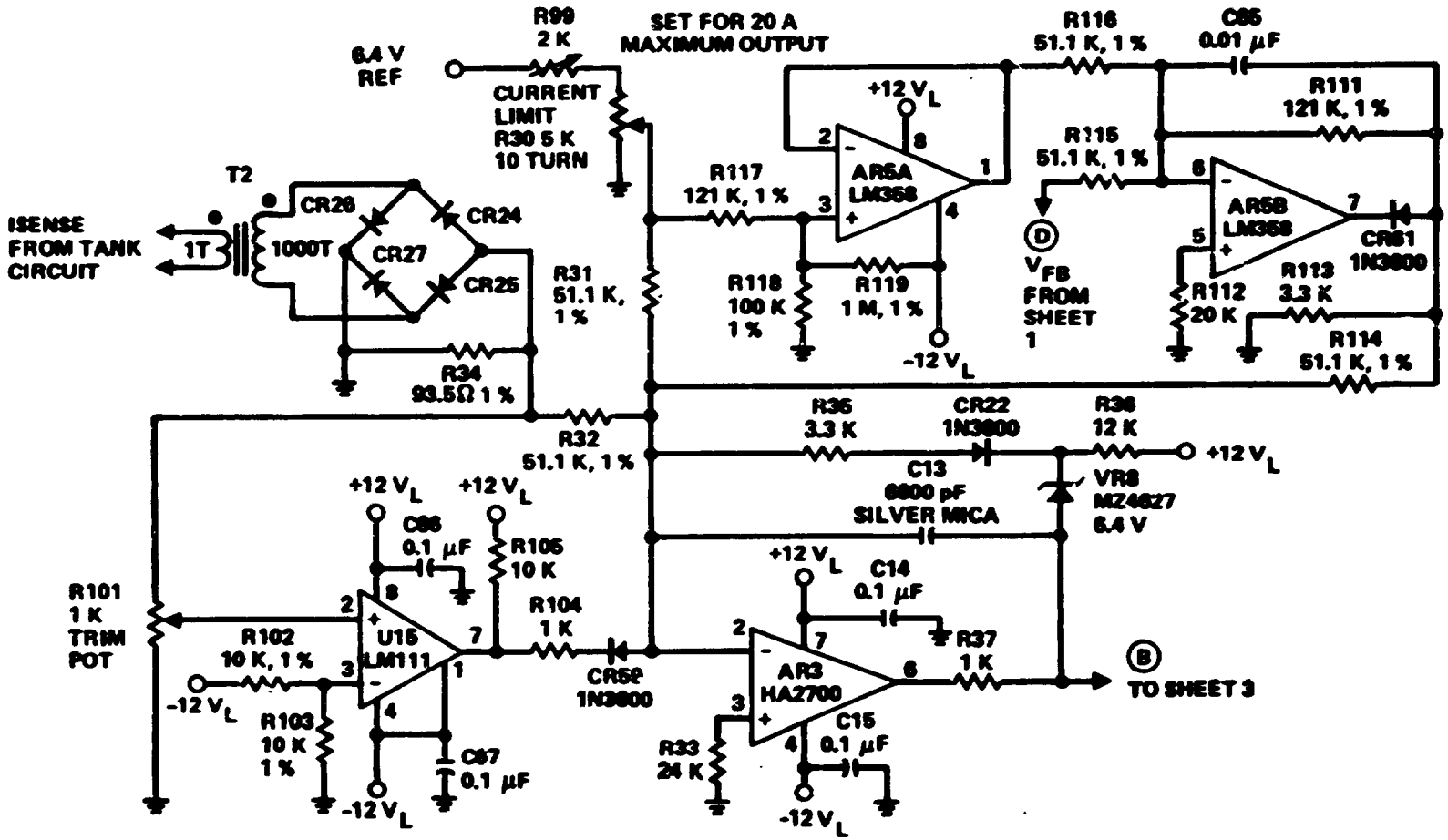



Figure 38(b). 10-kW control circuitry (tank current feedback).

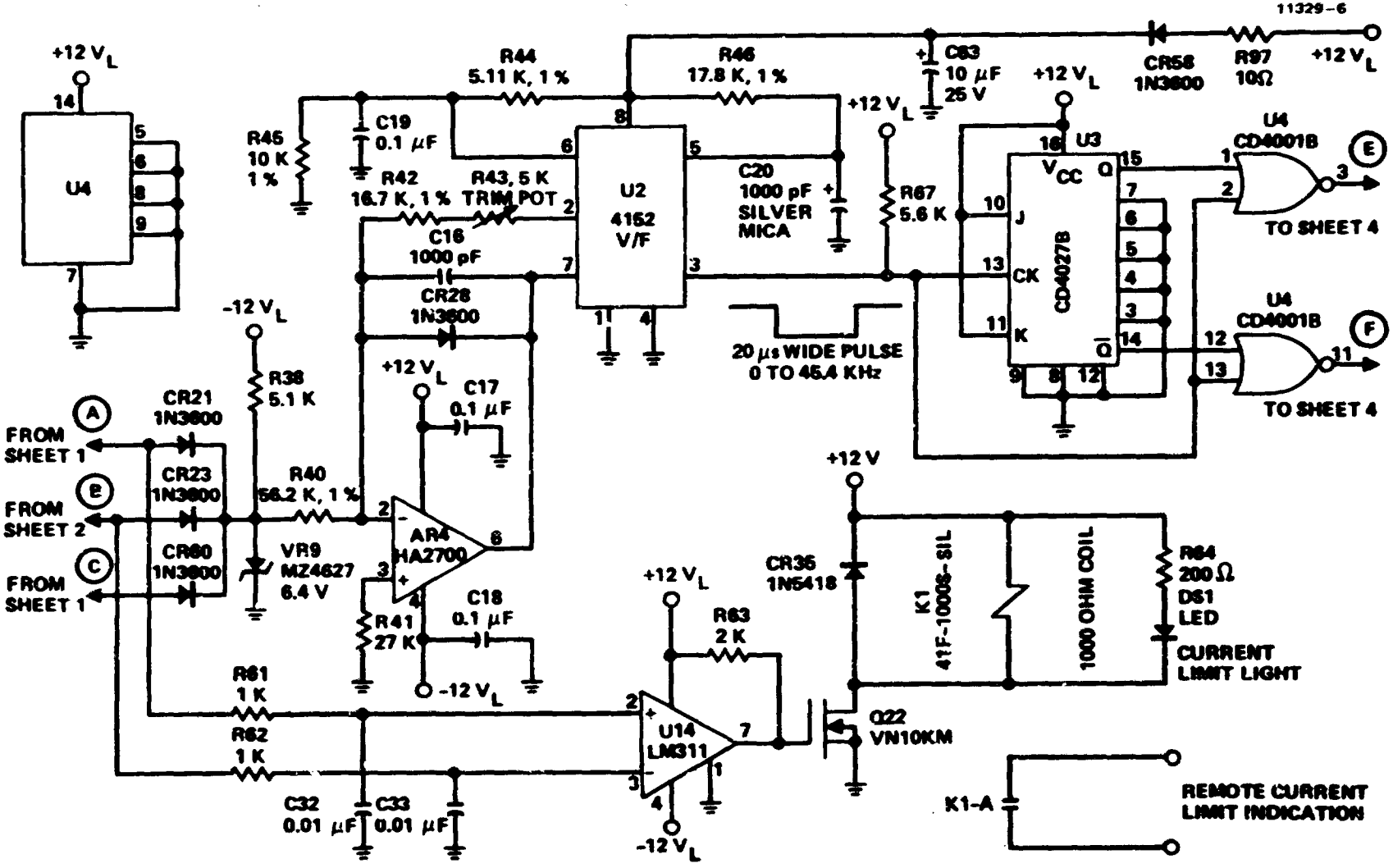



Figure 38(c). 10-kW control circuitry (V/F conversion).

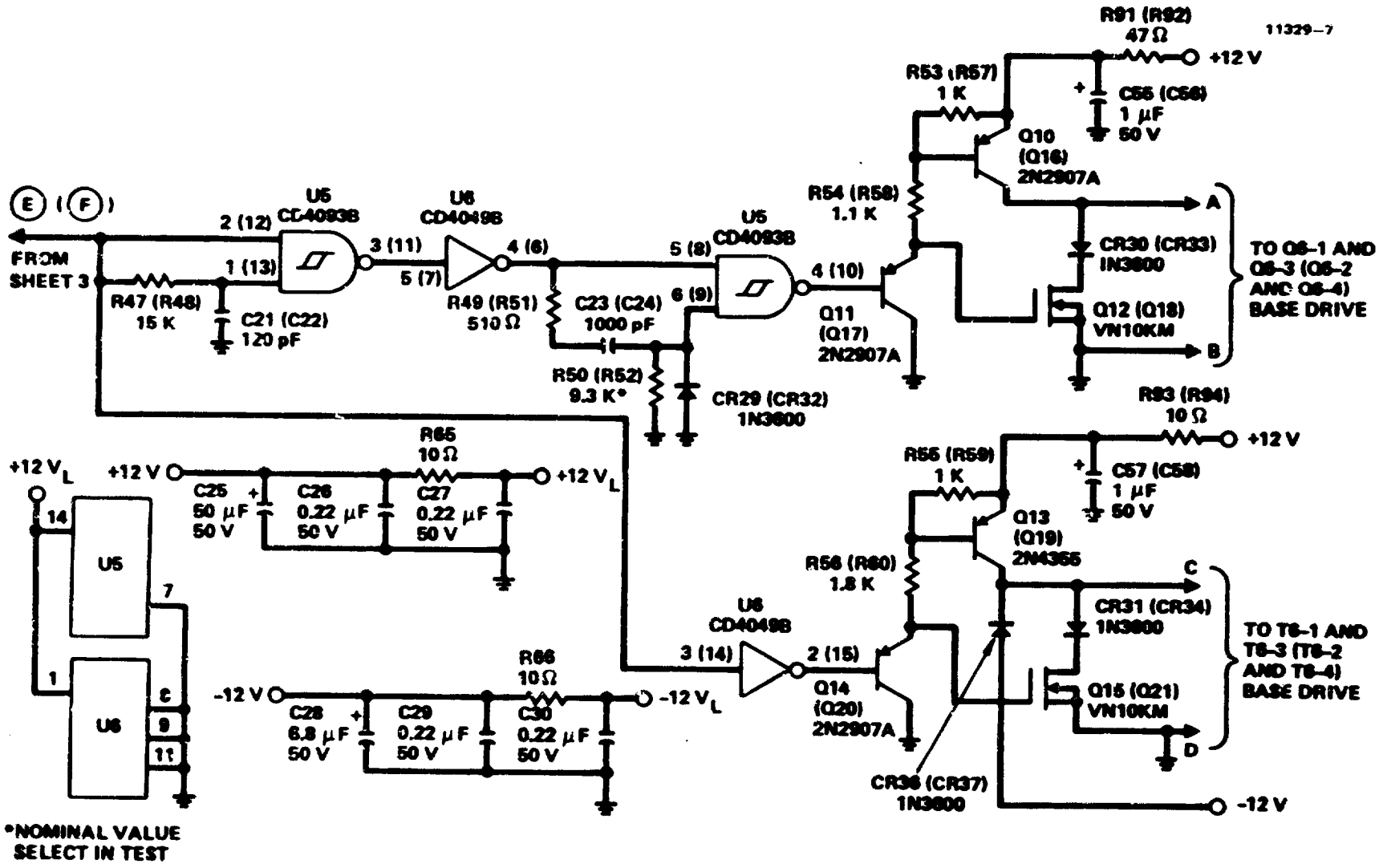



Figure 38(d). 10-kW control circuitry (base-drive timing).

sensed by current transformer T2, rectified by CR24 through CR27, and converted to a voltage by R34. This voltage is then compared against the output current reference-signal (from R30) and the difference integrated by AR3. This integrator is also confined to the normal operating range by a clamp circuit comprised of R35, R36, CR22, and VR8. AR5A and AR5B sense when the output voltage has fallen below a certain level (determined by the output current reference-signal (150 V for a reference level of 20 A) and then linearly phase the output current back to 6 A as the output voltage falls to zero. The static output operating envelope produced in this manner is shown in Figure 39. Comparator U15 senses when the peak tank current exceeds 120 A and immediately resets the integrator (AR3) to zero, which in turn phases the inverter off. The integrator can immediately start to integrate back up and phase the inverter back on to the referenced set point. This comparator limits the peak tank current and protects the components of the bridge and tank circuitry during transient conditions. Currents are limited to a peak value of 120 A and the voltage on resonate capacitor C1 is limited to 1200 V.

The outputs from the voltage and current feedback circuits are diode-OR'd to the input of the voltage-to-frequency (V/F) converter. The diode-OR'd functions control by limiting how far R38 is allowed to phase on the inverter, while VR9 provides a maximum limit to which the inverter can be phased on. The actual V/F converter, U2, uses AR4 to improve linearity, operating range, and response time, while U3, a flip-flop, alternately allows the pulse output of U2 to be applied to the base-drive for opposite sides of the bridge by way of the steering gates (U4). Comparator U14 senses whether the voltage loop or the current loop has control of the system and closes relay contact K1-A and turns front panel light DS1 on when the current loop has control.

The output pulse from the steering gates is inverted by U6 and applied to the interface circuit composed of Q13, Q14, and Q15. This circuit drives T6-X (Figure 31) which turns Q9-X off, permitting QX to be turned-on. The trailing edge of the pulse turns Q9-X back on, starting the turn-off of QX. The output pulse from the steering gates is also delayed for approximately 1 μsec by R47 and C21. This delay allows time for Q9-X to be turned-off and also provides a means for balancing both halves of the tank current if necessary by varying this delay time slightly. The delayed pulse is inverted by U6 and shortened

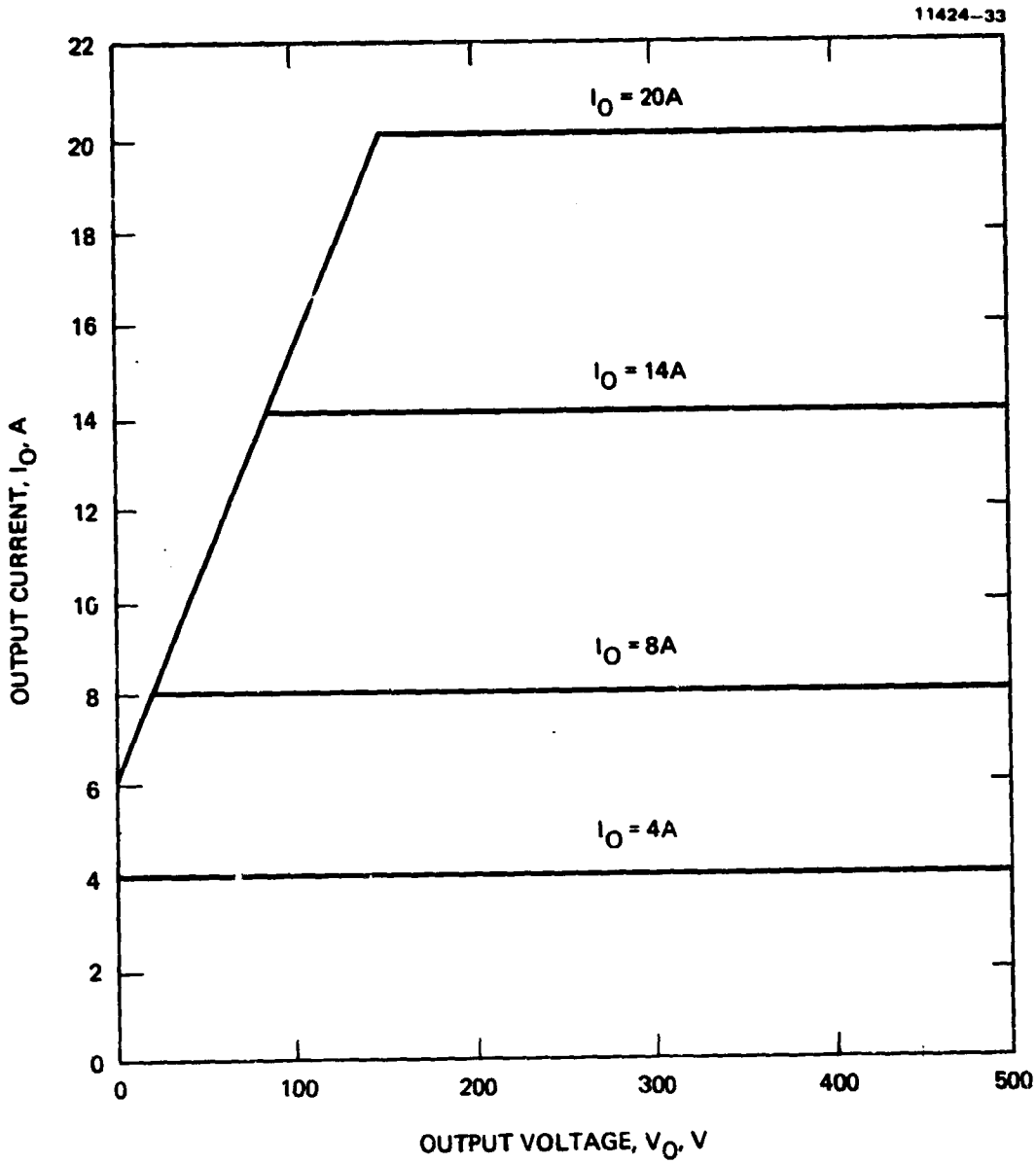



Figure 39. 10-kW SRI output operating envelope.

by R49, R50, and C23 to the width required for the leading-edge base-drive pulse. This shortened pulse is applied to the interface circuit composed of Q10, Q11, and Q12 which turns Q6-X (Figure 31) on and off.

## E. SOLID-STATE DC INPUT CIRCUIT BREAKER

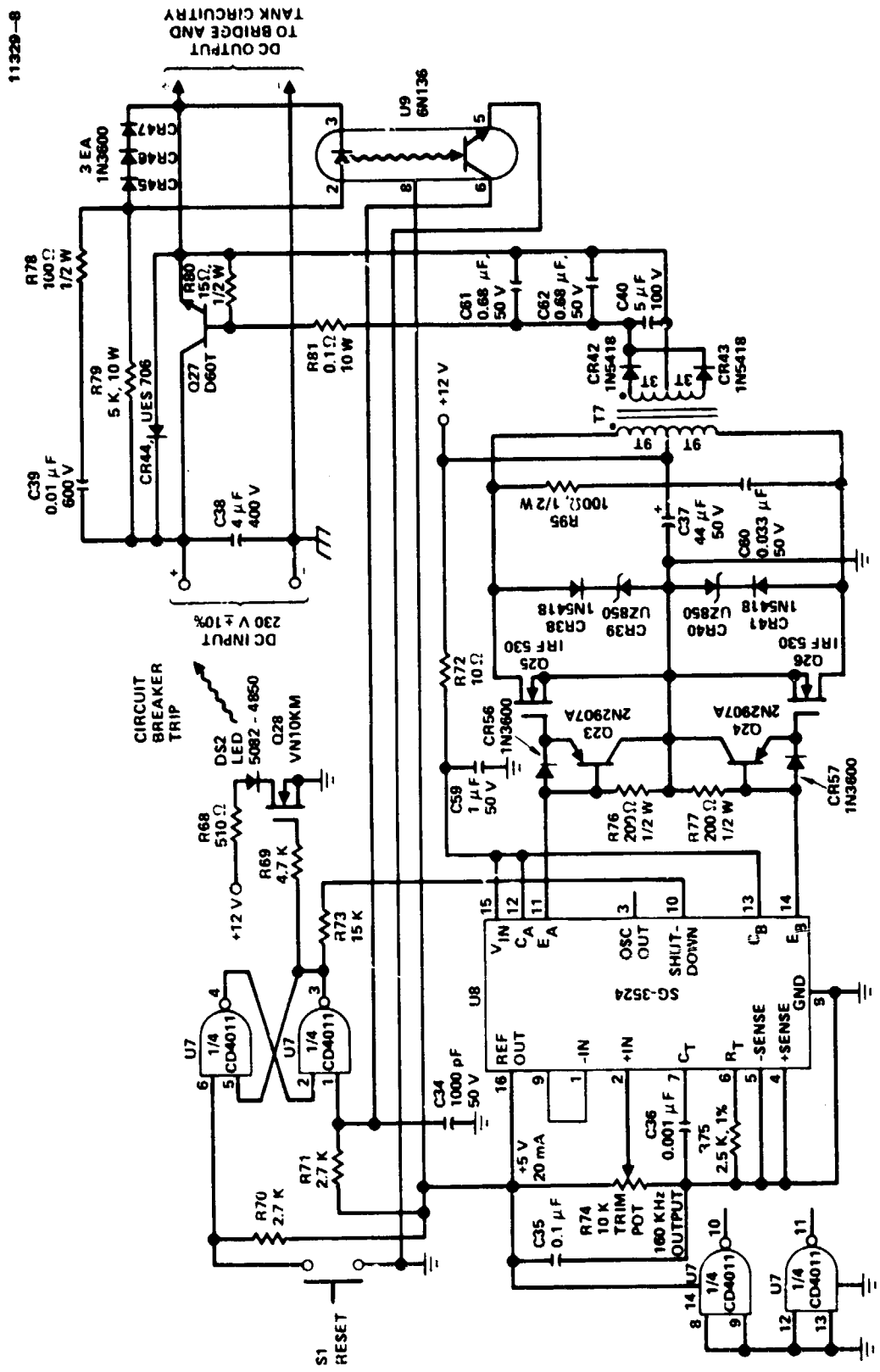
The main DC bus for the inverter is protected by a solid-state circuit breaker that trips if the line current exceeds 60 A. The switch used in this circuit breaker is a D60T transistor (Q27 of Figure 40) that is driven by a small free running inverter operating at 160 kHz. The inverter consists of U8, Q25, Q26, and T7 of Figure 40. The output of this inverter is rectified by CR42 and CR43, filtered by C40, C61, and C62, and used as the base-drive for Q27. The output level of the inverter is varied by R74, which is used to adjust the base-drive of Q27 so that it will come out of saturation at 60 A. When Q27 comes out of saturation, the optical coupler (U9) turns on, setting the flip-flop (U7). When U7 is set, the inverter turns-off, which removes the base-drive from Q27, causing Q27 to turn off within 10 μsec after coming out of saturation. Pushbutton S1 is used to reset the flip-flop, turning the circuit breaker back on.

## F. MAIN BUS SUPPLY

The main bus supply is a commercially purchased, unregulated, 60 Hz supply with an LC output filter. The output of this supply varies over the range of 230 to 270 Vdc as the line and load vary. T2, T3, and associated components (Figure 41) were added to this commercial supply to provide unregulated power for the housekeeping supplies.

## G. HOUSEKEEPING SUPPLIES

A schematic of the housekeeping supplies is shown in Figure 42. Regulation is provided by standard, commercially available 3-terminal regulators that produce outputs of +12 V, -12 V, and +75 V.




NOTE: RESISTORS ARE 1/4 W, 5% CARBON
UNLESS OTHERWISE SPECIFIED.

Figure 40. 10-kW solid-state DC input circuit breaker.

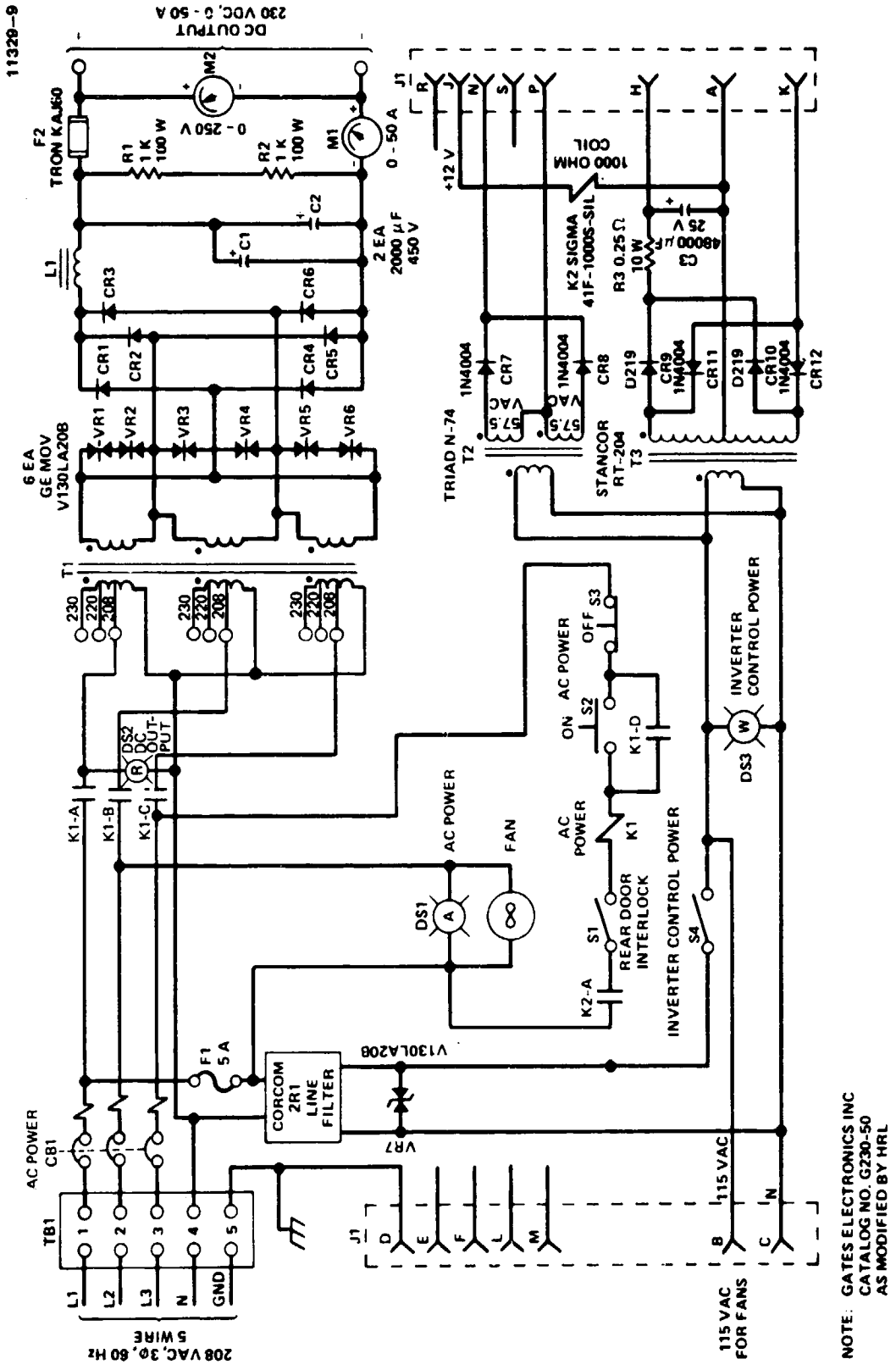



Figure 41. 10-kW DC power source.

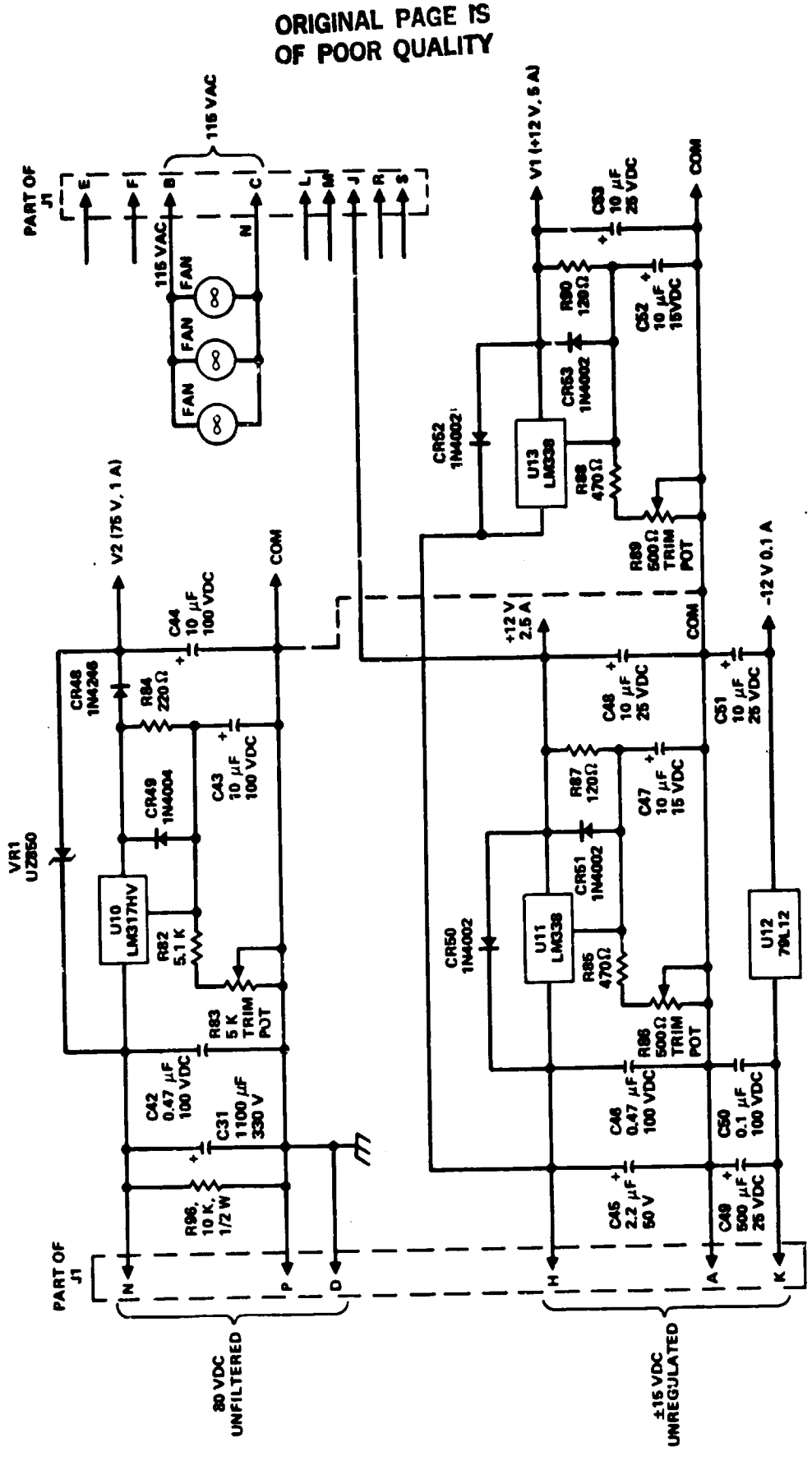



Figure 42. 10-kW housekeeping supplies.

## H. NEGATIVE BIAS SUPPLY

Each of the base drive circuits requires an isolated negative 8 V for use as the negative bias during the time that the transistors (Q1 through Q4 of Figure 36) are off. These negative bias voltages are supplied by the free-running inverter of Figure 43. The inverter operates at 25 kHz and has four isolated outputs. This is a low power inverter and the 10 A current pulses required during turn-off of Q1 through Q4 are provided by C7-X of Figure 31.

## I. MECHANICAL

The 10-kW converter was designed to be used in a laboratory type environment with forced air as the cooling medium. It was divided into two separate chassis, so that the power supply to generate the main DC bus power could be separated from the actual series resonant converter for convenience reasons. The chassis containing the DC bus supply is free-standing and is 55.9 cm x 49.5 cm x 38.1 cm (22 in. x 19.5 in. x 15 in.).

The actual series resonant converter, shown in Figure 44, is contained in a rack-mountable chassis that is 48.25 cm x 31.1 cm x 46 cm (19 in. x 12.25 in. x 18 in.). It weighs 52 kg (115 lb) and can be mounted at a convenient height for operation of its controls and reading of the meters. This chassis is connected to the power supply chassis by two cables, one for the main DC bus power and one for controls and housekeeping power.

Figure 45 is an interior view of the inverter showing the locations of the D60T and commutating diode heat sinks, output rectifiers, control circuitry, base-drive, series resonant capacitor, output transformer, and series resonant inductor. The input capacitor, output capacitor, housekeeping supplies and fans are mounted in the bottom of the chassis and cannot be seen in this photograph.

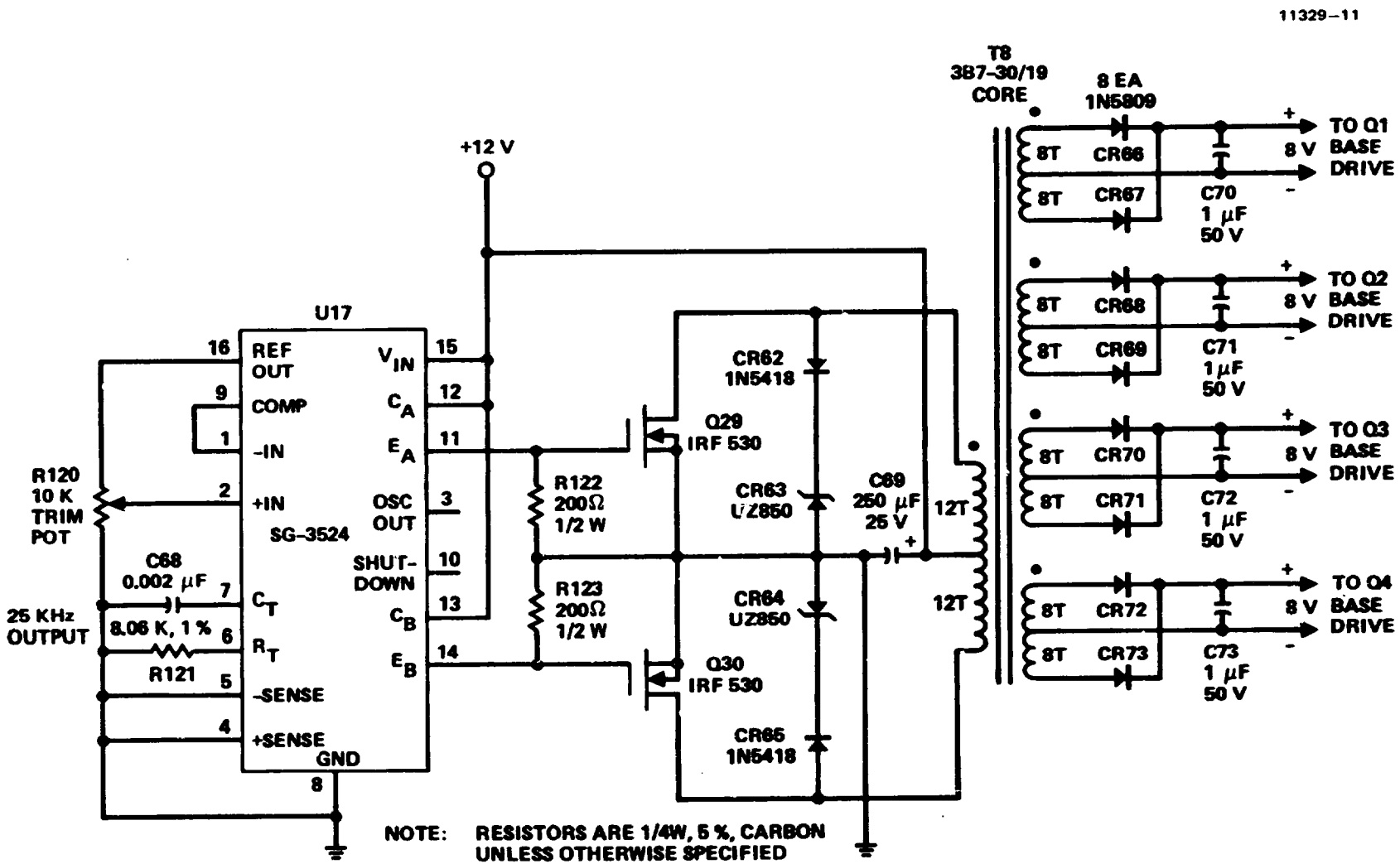



Figure 43. 10-kW negative bias supply.

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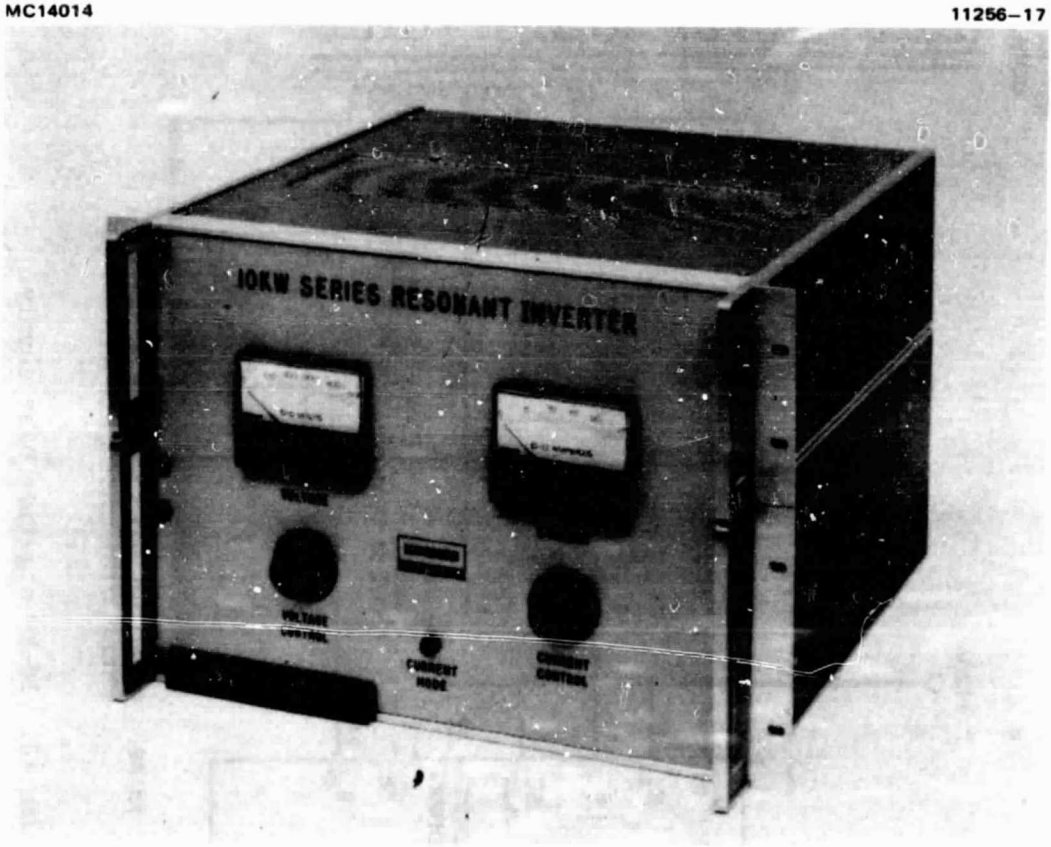


Figure 44. 10-kW series resonant inverter.

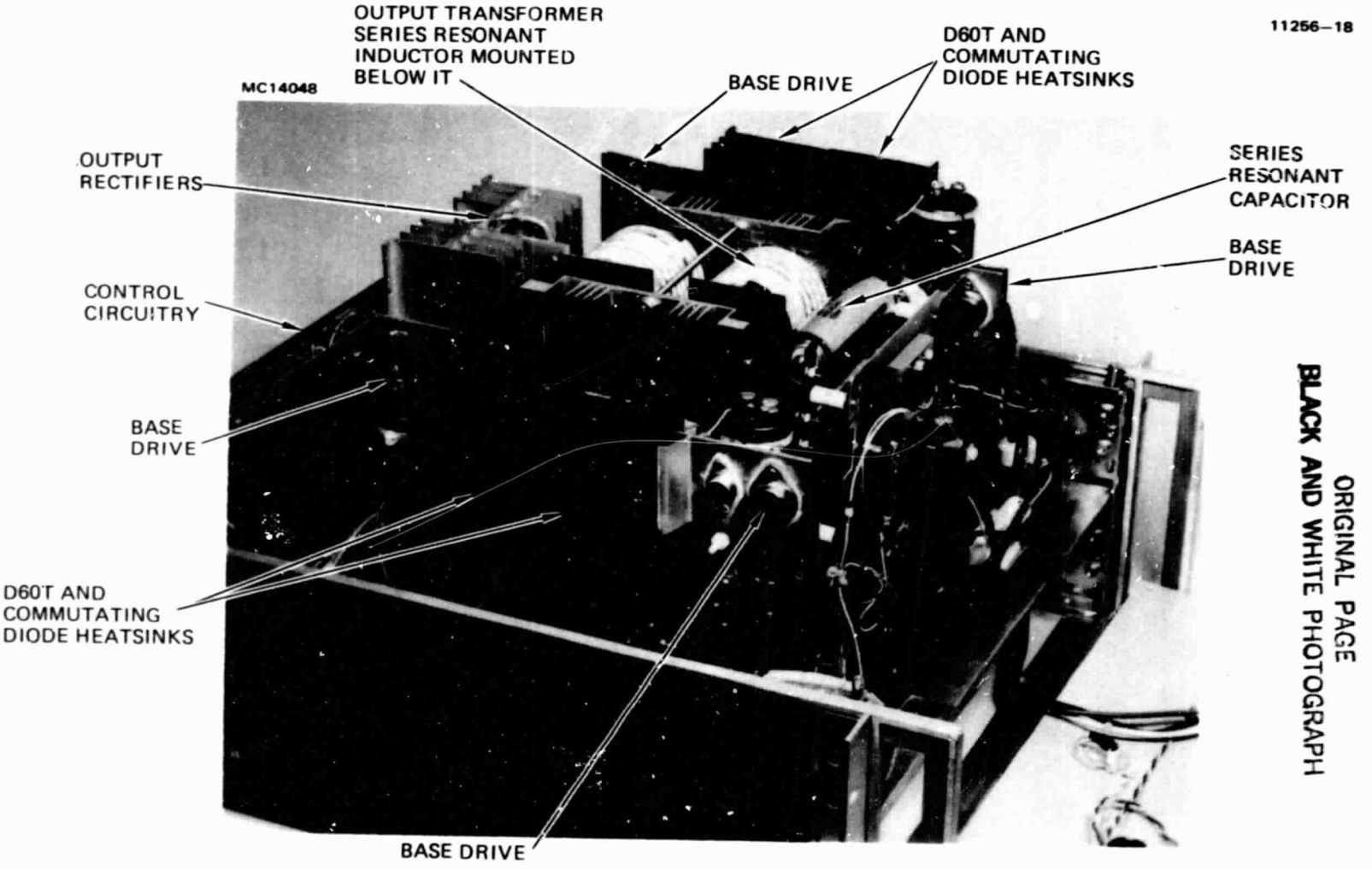


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Figure 45. Interior view of the 10-kW series resonant inverter.

## SECTION 6

## TESTING

The 10-kW converter that was designed and fabricated was also tested under a variety of conditions to determine its operational characteristics. The parameters tested for were stability, steady-state waveforms, output ripple, regulation, transient waveforms, and efficiency. The test results for each of these parameters are discussed in the following sections.

### A. STABILITY

The voltage and the current control loops both have integrators in their forward loops to provide very high DC gain, necessary for good regulation. In addition to the integrator, the voltage control loop has a lead-lag network on the output voltage divider and a lead network as part of the integrator for loop compensation. The Bode plots for this loop for a variety of output conditions are shown in Figures 46 and 47. These figures show the bandwidth increasing and the stability decreasing as either the output voltage increases or the load resistance decreases. The worst case gain margin is 10 dB, and the worse case phase margin is 65 deg.

The current control loop does not have any compensation in addition to the integrator. The Bode plots for this loop for a variety of conditions are shown in Figure 48. The bandwidth and the stability of this loop are fairly constant for the conditions tested with a worst case gain margin of 15 dB and a worst case phase margin of 90 deg.

### B. STEADY-STATE WAVEFORMS

Photographs of oscilloscope traces of the major current and voltage waveforms in the inverter were taken for three output conditions corresponding to when the tank current is discontinuous, the diodes conduct for approximately 0.75 $\pi$, and the inverter is phased almost full-on. The first set of these photographs (Figure 49) shows the tank current and resonant capacitor (C1 of

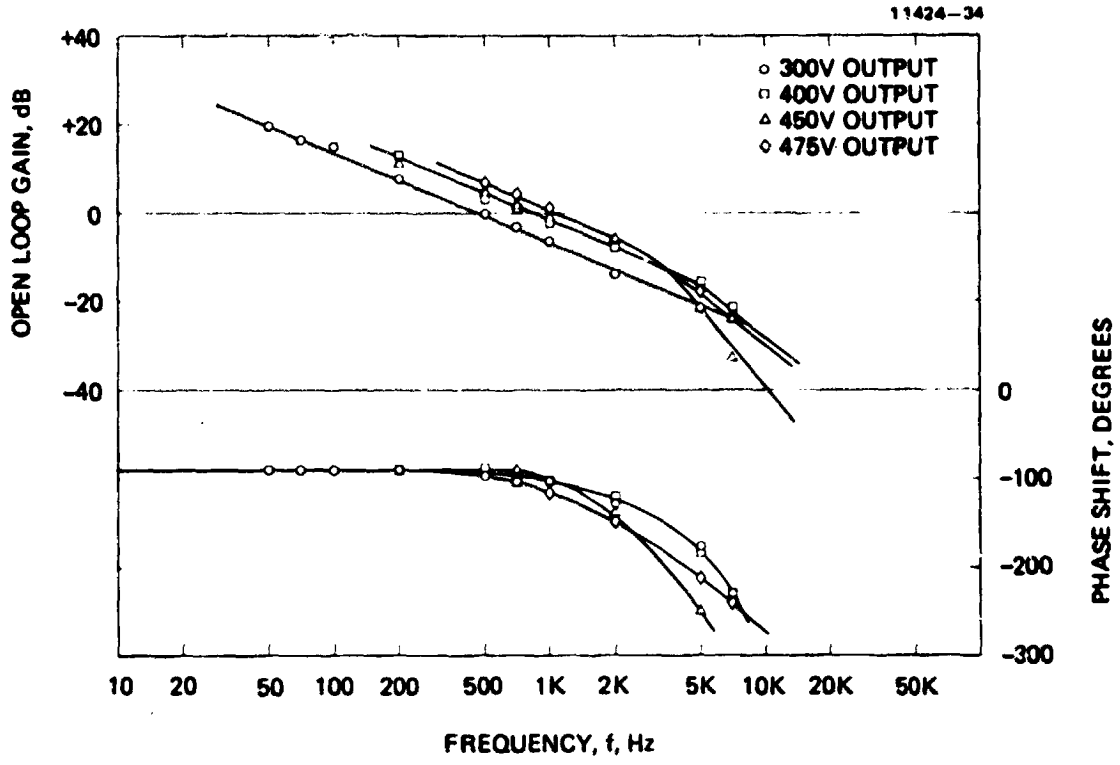


Figure 46. Bode plots of the 10-kW SRI voltage control loop with a 25 Ω load.

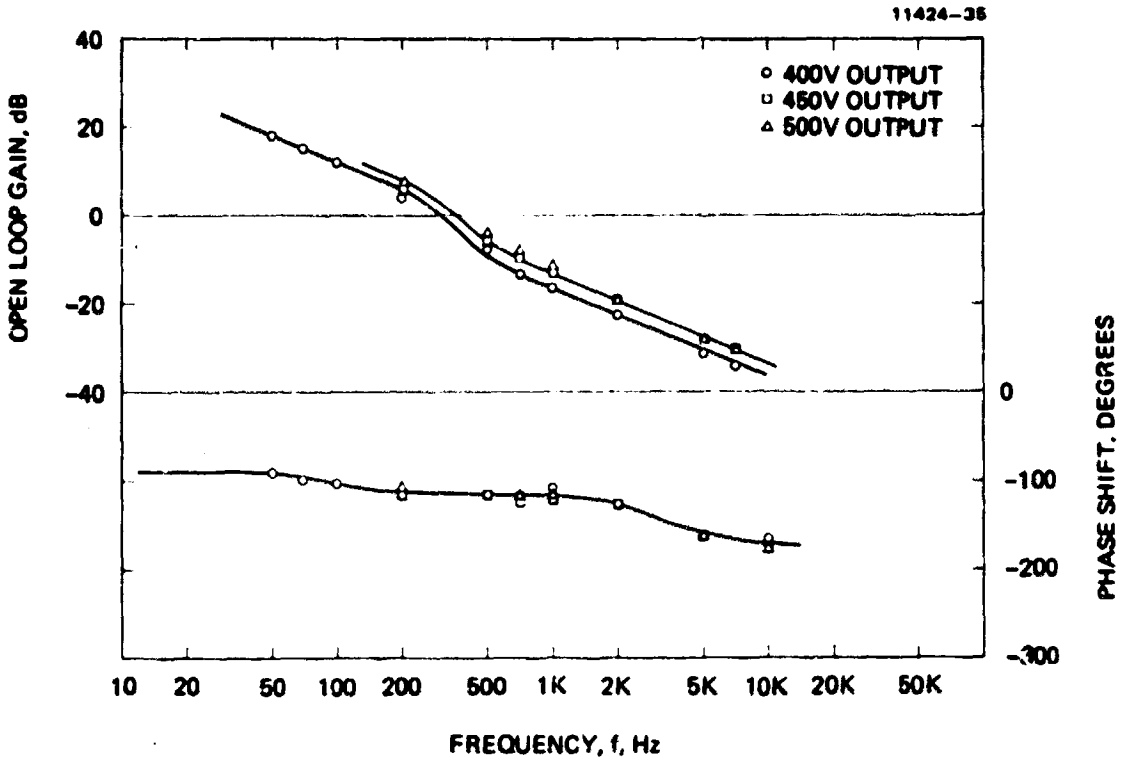


Figure 47. Bode plots of the 10-kW SRI voltage control loop with a 50 Ω load.

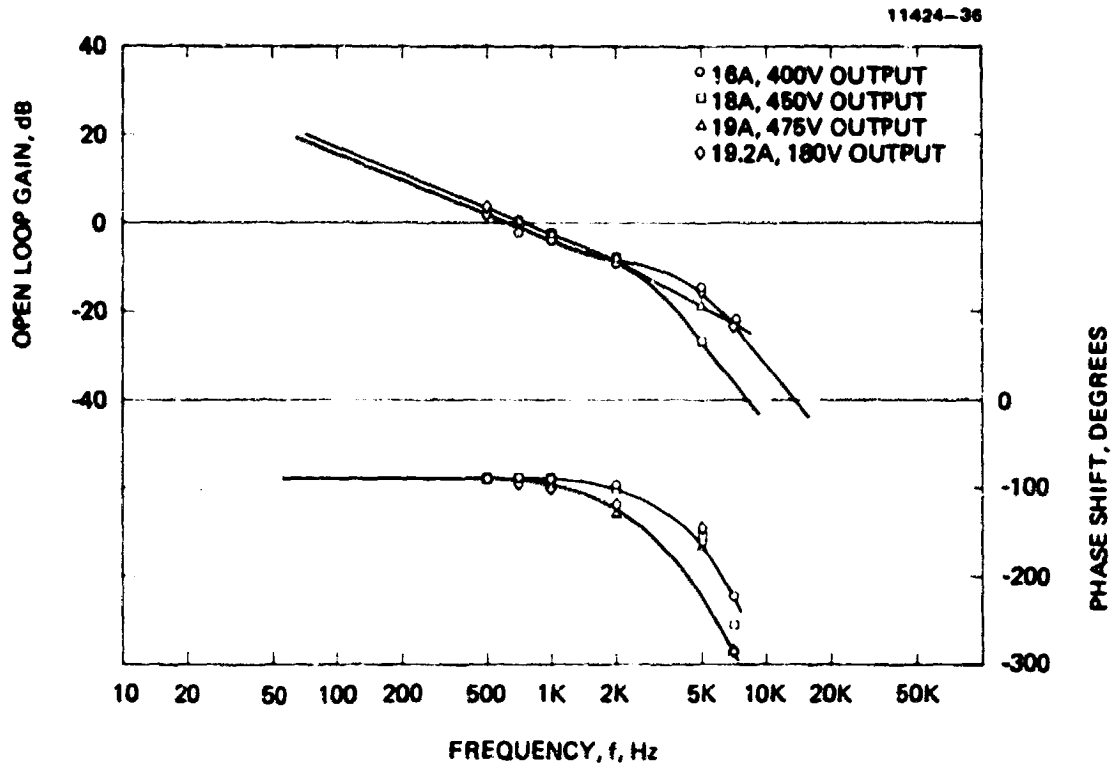


Figure 48. Bode plots of the 10-kW SRI current control loop.

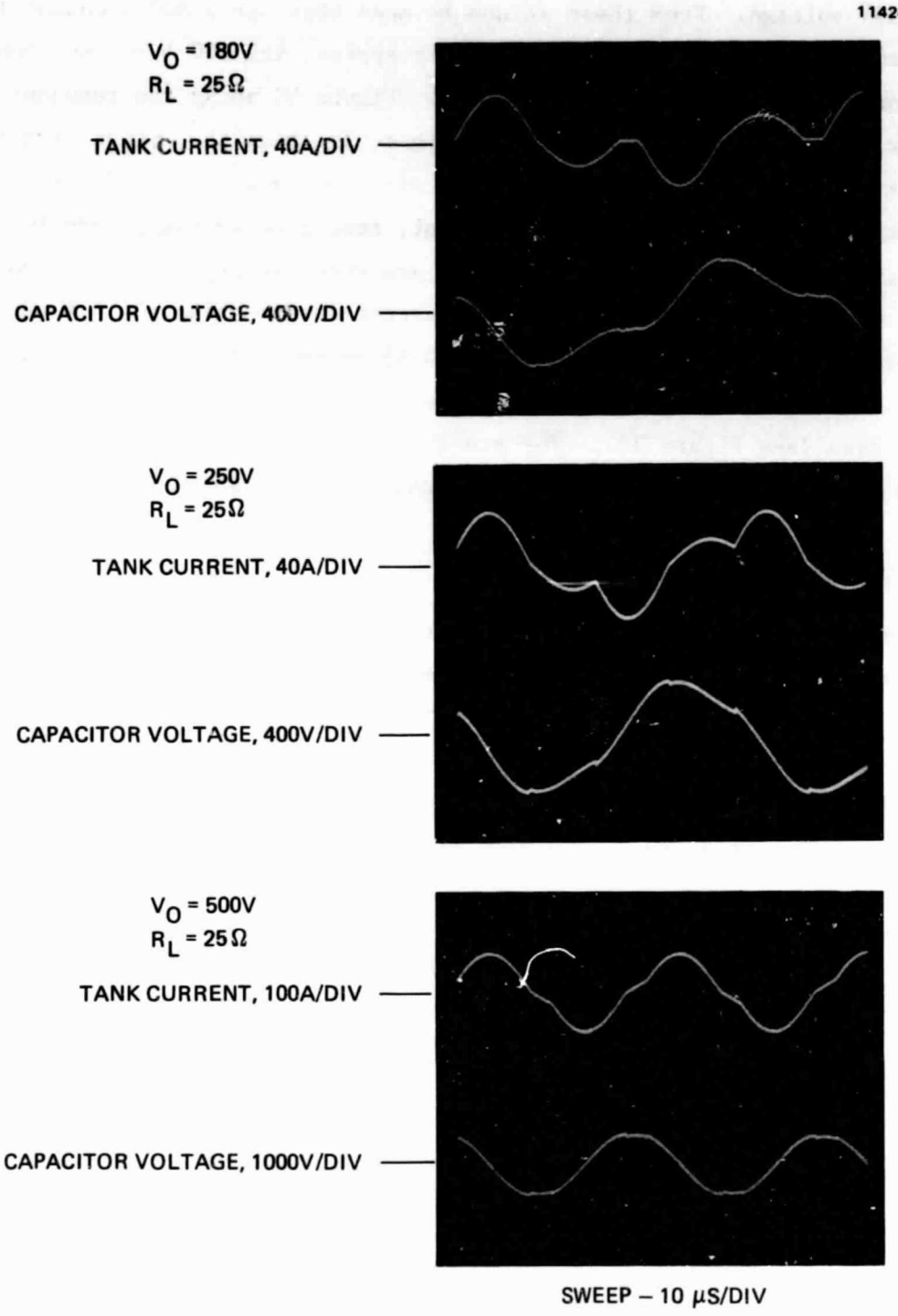


Figure 49. Steady-state tank current and resonant capacitor voltage for different load conditions.



C-2

Figure 36) voltage. From these it can be seen that for a 500 V output into a 25-Ω load (10-kW) the peak tank current is approaching 100 A and the peak capacitor voltage is approximately 700 V. Figure 50 shows the resonant inductor (L1 of Figure 36) voltage and Figure 51 shows the output transformer (T1 of Figure 36) primary voltage, along with the tank current for the same three output conditions. The tank current, capacitor voltage, inductor voltage, and transformer primary voltage are shown in Figure 52 for short circuit output conditions. The output current is approximately 6 A under this condition (with the control pot set at 20 A) because of the current cutback feature of the control circuitry that starts to function as the output voltage goes to zero (see Figure 39). The steady-state base current and base-emitter voltage waveaforms for the 10-kW output condition are shown in Figure 53.

## C. OUTPUT RIPPLE

The output ripple for three different output voltages and a 25 Ω load is shown in Figure 54, while Figure 55 shows the condition for two different open circuit output voltages. The open circuit, 327 V condition, produced the largest peak-to-peak ripple observed. This ripple data is summarized in Table 17. The peak-to-peak ripple could be reduced by adding more output capacitance, but this would also decrease the bandwidth of the frequency response.

TABLE 17. Output Ripple of the 10-kW Converter

| Output Voltage, $V_o$, V | Output Load $R_L$, Ω | Output Ripple, Peak-to-Peak | |
|---|---|---|---|
| | | Volts | % of $V_o$ |
| 180 | 25 | 4.0 | 2.2 |
| 250 | 25 | 4.5 | 1.8 |
| 500 | 25 | 4.5 | 0.9 |
| 327 | ∞ | 34 | 10.4 |
| 500 | ∞ | 25 | 5.0 |

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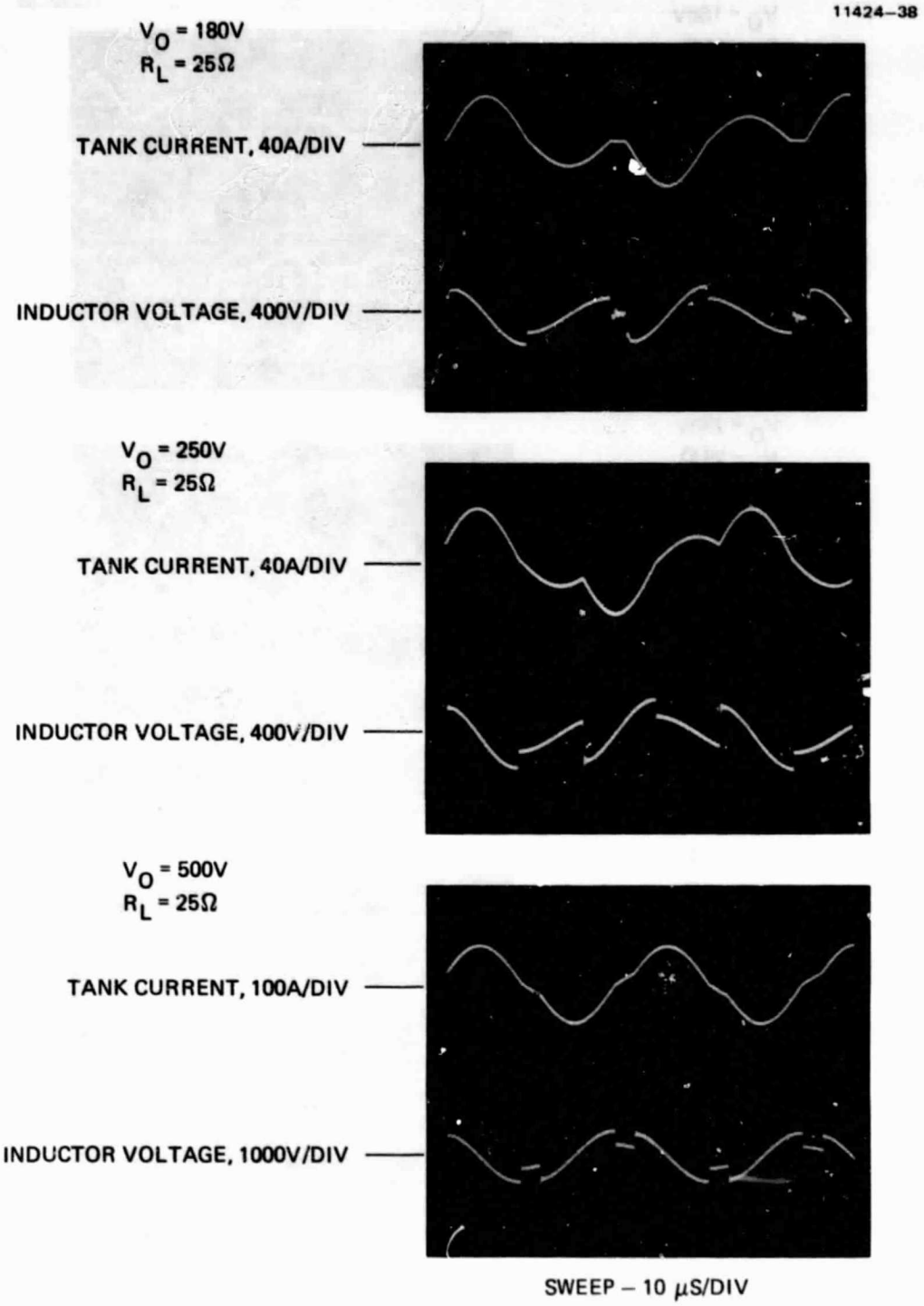


Figure 50. Steady-state tank current and resonant inductor voltage for different load conditions.

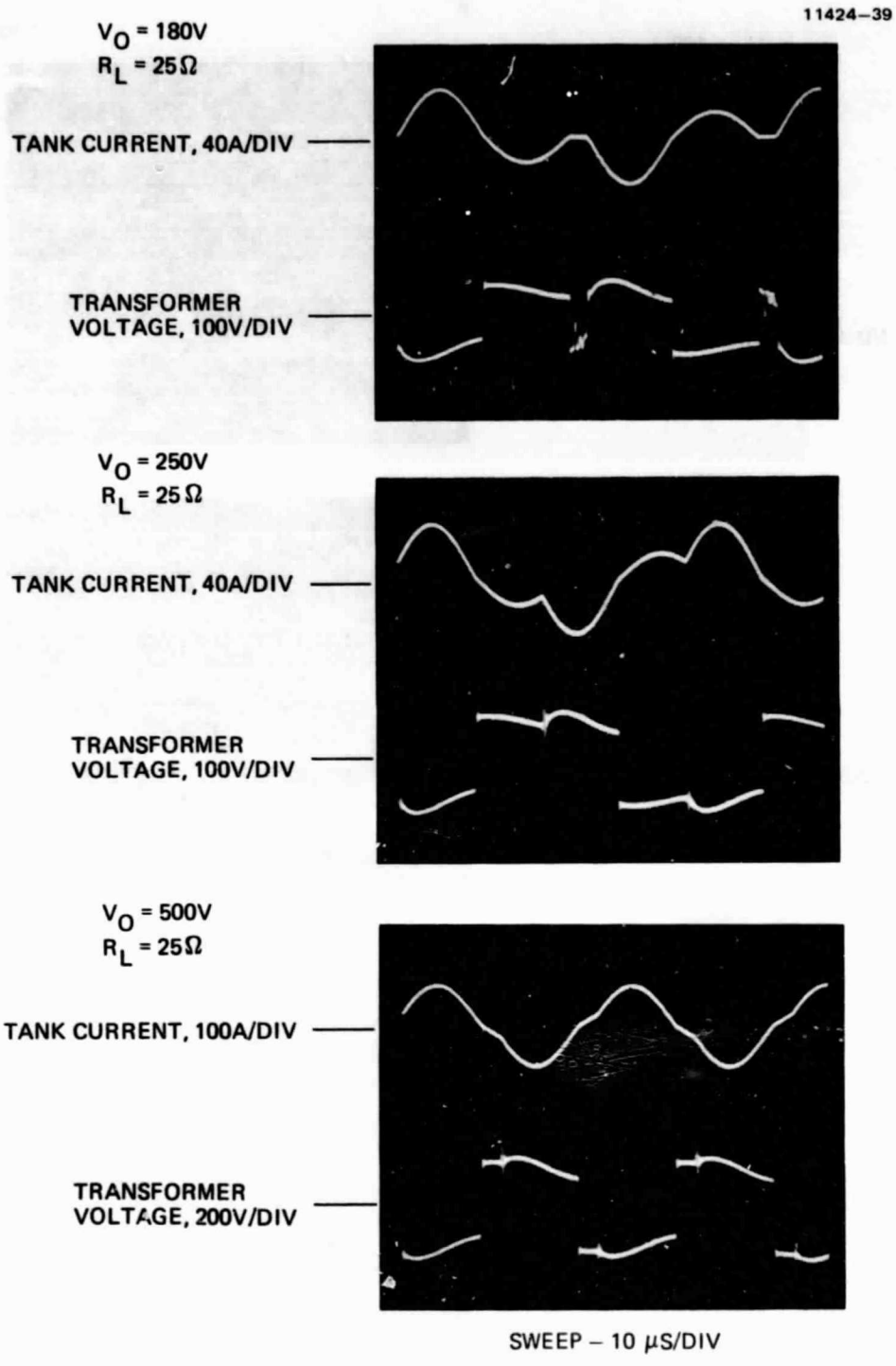


Figure 51. Steady-state tank current and output transformer primary voltage for different output conditions.

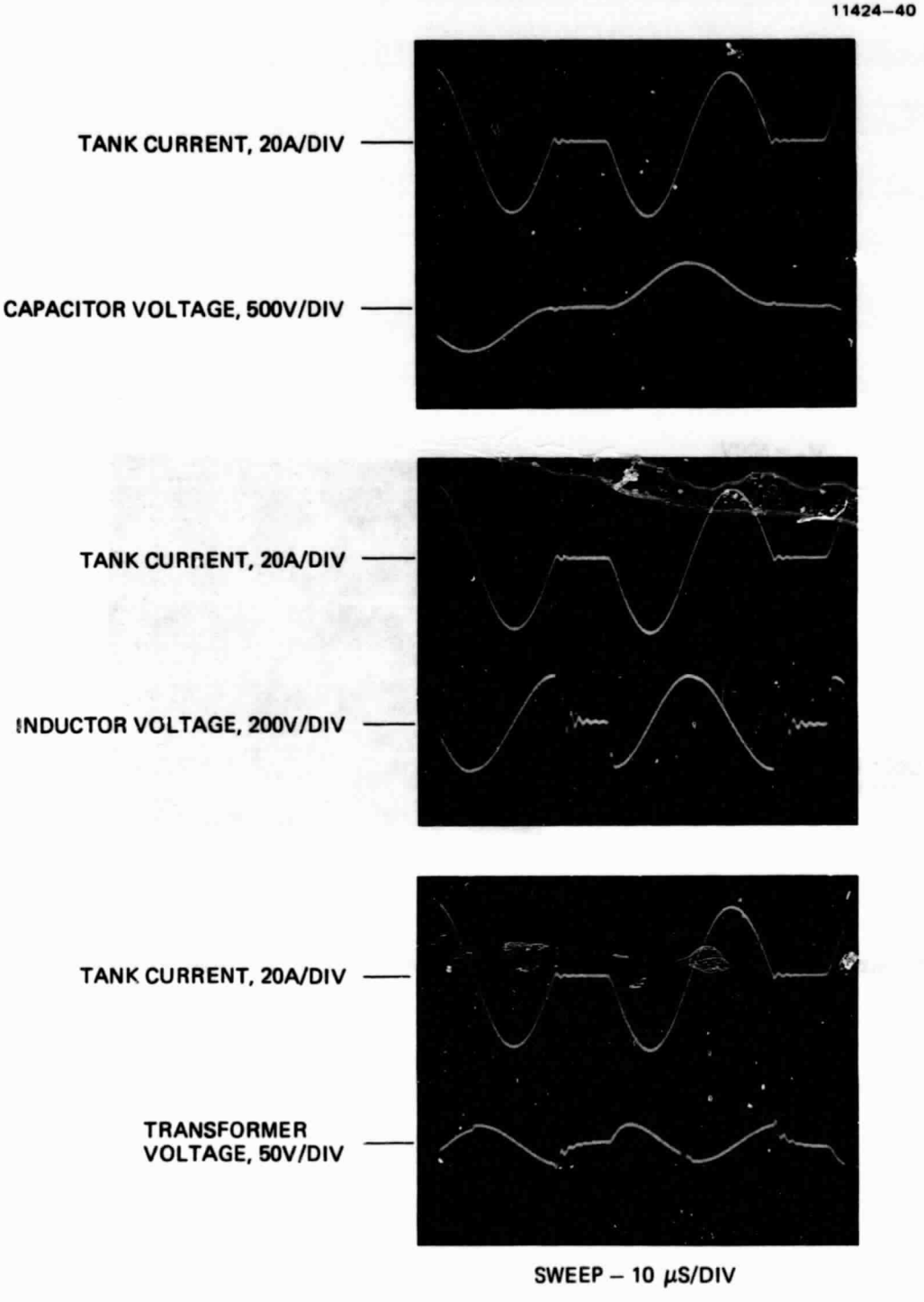


Figure 52. Steady-state tank circuit waveforms for short circuit output conditions.

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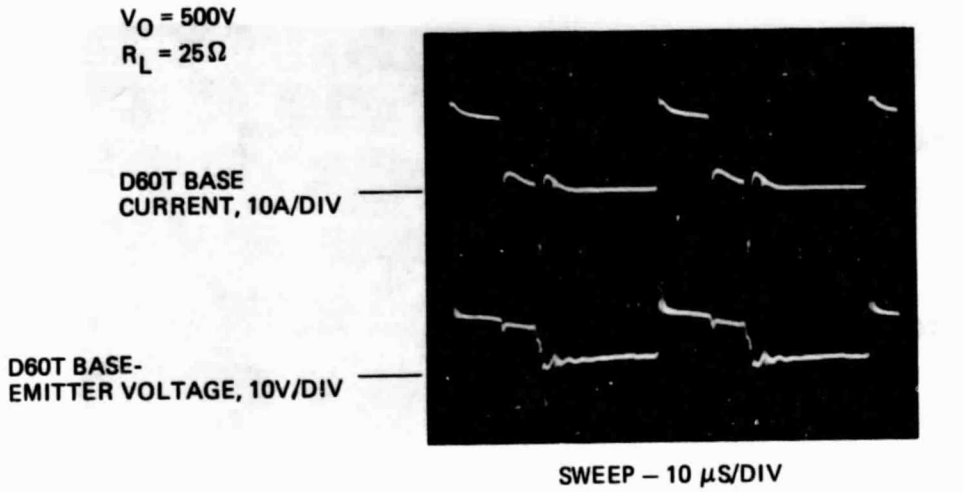


Figure 53. D60T base current and base-emitter voltage waveforms for full load conditions.

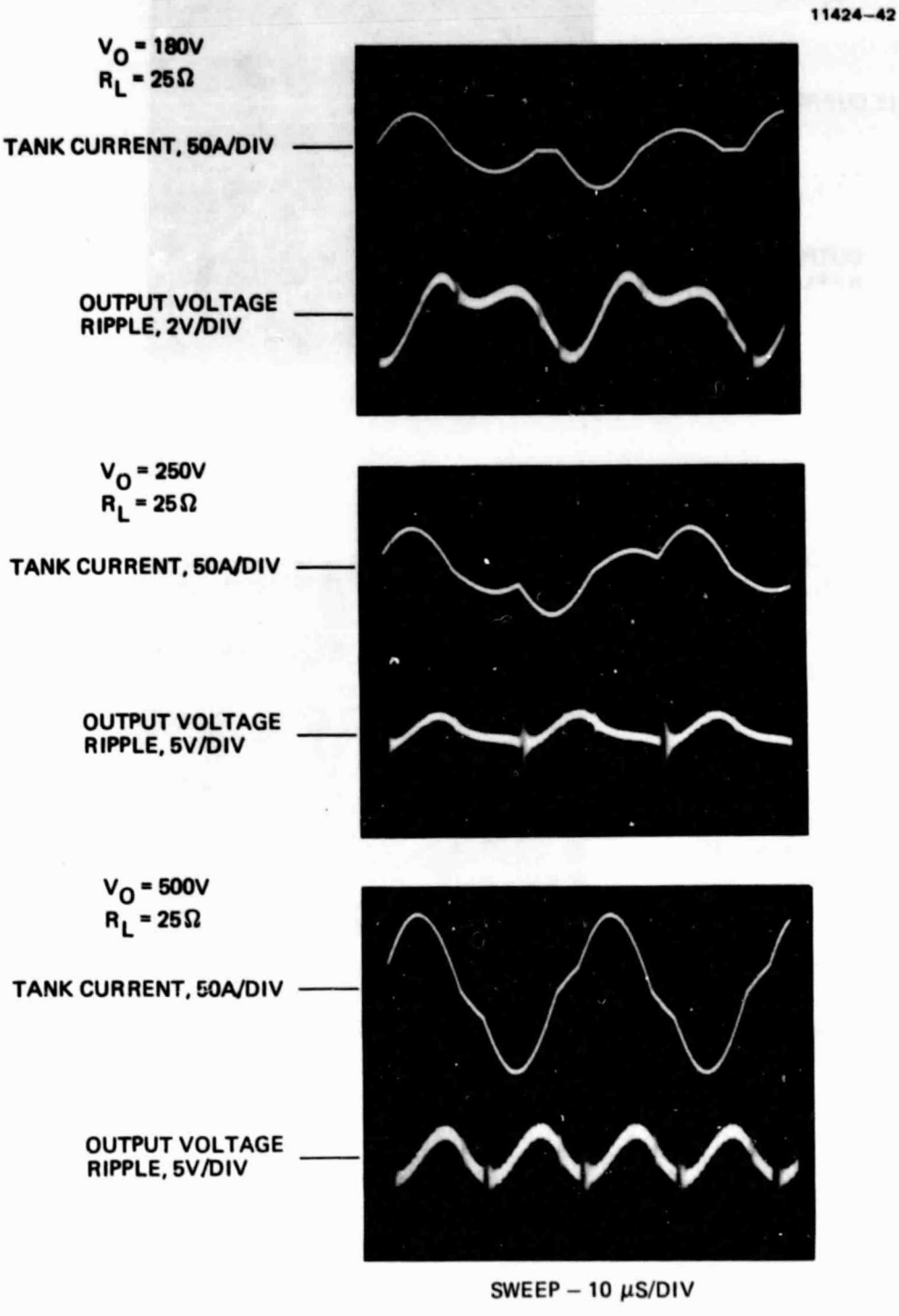


**Figure 54.** Output voltage ripple with a 25 Ω load at different output voltage levels.

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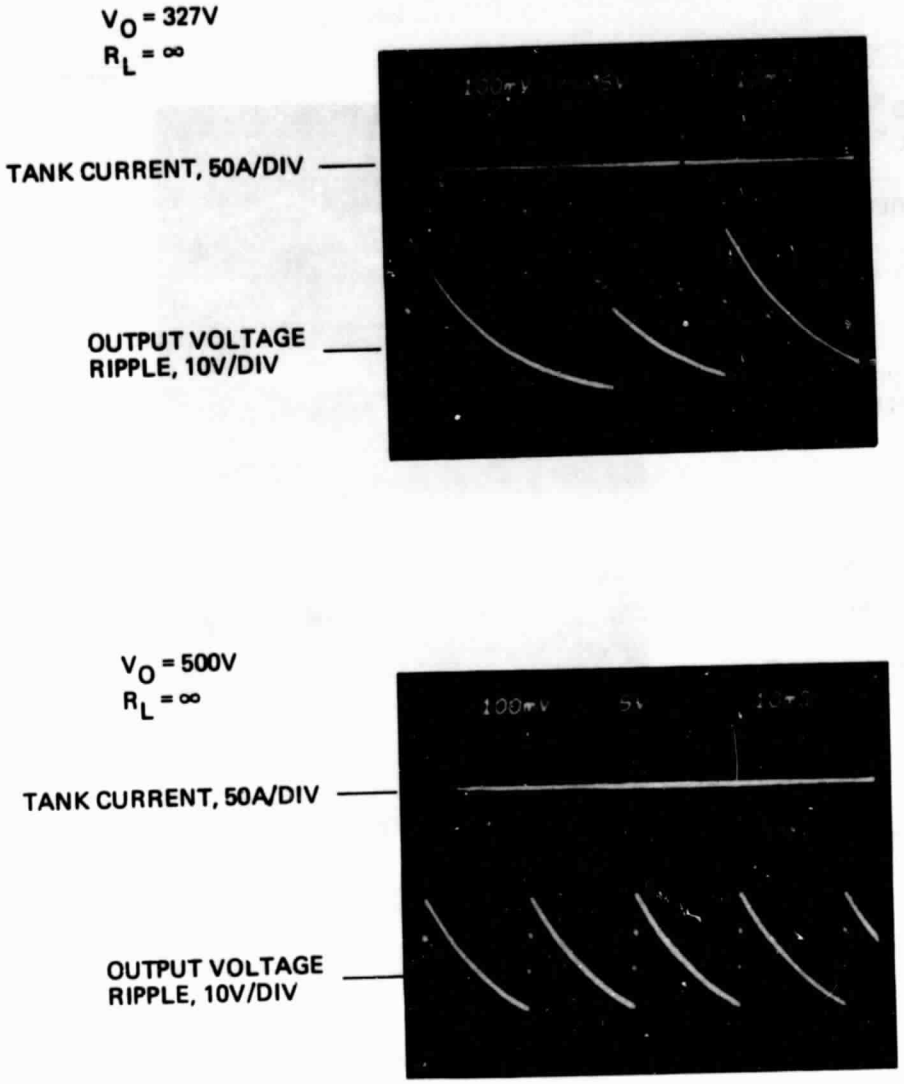


Figure 55. Output voltage ripple under open circuit conditions.

## D. LINE AND LOAD REGULATION

The line and load regulation measurements are presented in Table 18. They show that the regulation is better than or equal to 1 V.

TABLE 18. Line and load Regulation Measurement Data

| Line Regulation | | | Load Regulation | | |
|---|---|---|---|---|---|
| Input Voltage V | Output Voltage, $V_o$, V | Output Current, $I_o$, A | Load Resistance, $R_L$, Ω | Output Voltage, $V_o$, V | Output Current, $I_o$, A |
| | | | 1000 | 200 | 0.2 |
| 243 | 350 | 10 | 10 | 200 | 20 |
| | | | 1000 | 350 | 0.35 |
| 258 | 350 | 10 | 17.5 | 350 | 20 |
| | | | 1000 | 400 | 0.4 |
| 271 | 349 | 10 | 25 | 400 | 16 |

## E. TRANSIENT LINE AND LOAD TESTS

The inverter was tested for its response during turn-on of the main bus supply and for load transients of the operating point to short circuit, short circuit to the operating point, operating point to open circuit, open circuit to the operating point, open circuit to short circuit, and short circuit to open circuit.

The circuit shown in Figure 56 was used when we wanted a closing switch to generate load transients, while the circuit shown in Figure 57 was used when we wanted an opening switch. The SCR of Figure 56 was turned back off by programming the output of the inverter to zero current. We used R2 only when short circuiting the output of the inverter and it provided a limit on the maximum surge current. The GTO SCR of Figure 57 could not be used both as a closing switch and an opening switch because of its low surge-current rating (220 A). It was turned-on while the inverter was off, and then the inverter was brought on to the operating test point.

Figure 58 shows the tank current, input bus current, output voltage, and input voltage as the main bus supply is turned-on and the inverter comes up to an operating point of 500 V and 10 A. These traces are typical of all the turn-on transients tested and show that these parameters are well behaved during the turn-on.

The tank current and resonant capacitor voltage response to a load transient of 500 V at 20 A to short circuit is shown in Figure 59. This was the response before the peak tank current limiting circuitry (U15 and associated components of Figure 38(b)) was added to the control circuit, and shows the tank current peaking at 190 A and the capacitor voltage peaking at 1700 V. These peak levels were unacceptably high and therefore the circuit was modified. Figure 60 shows the response of the tank current and capacitor voltage to the same transient condition after the peak tank current limiting circuitry was added. The tank current is now limited to 120 A and the capacitor voltage to 1000 V, which are acceptable levels.

The tank current and output voltage response to a load transient of short circuit to open circuit (350 V setpoint) is shown in Figure 61. The tank current response is acceptable, but the output voltage overshoots the

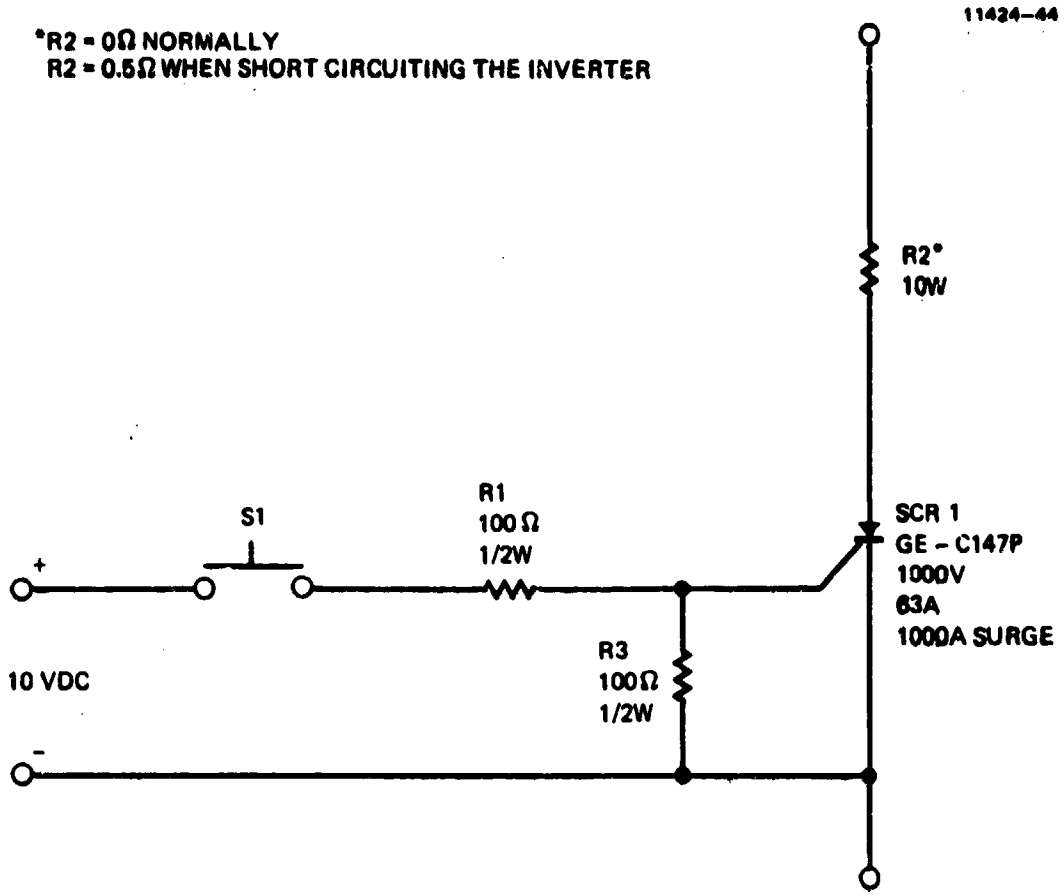


Figure 56. Circuit used to provide a closing switch for transient load testing.

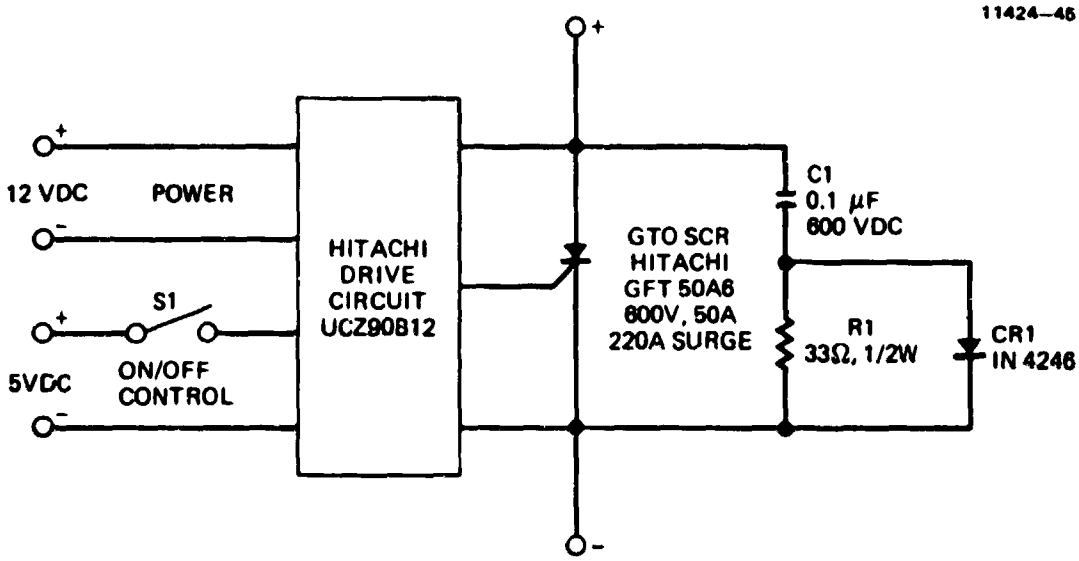


Figure 57. Circuit used to provide an opening switch for transient load testing.

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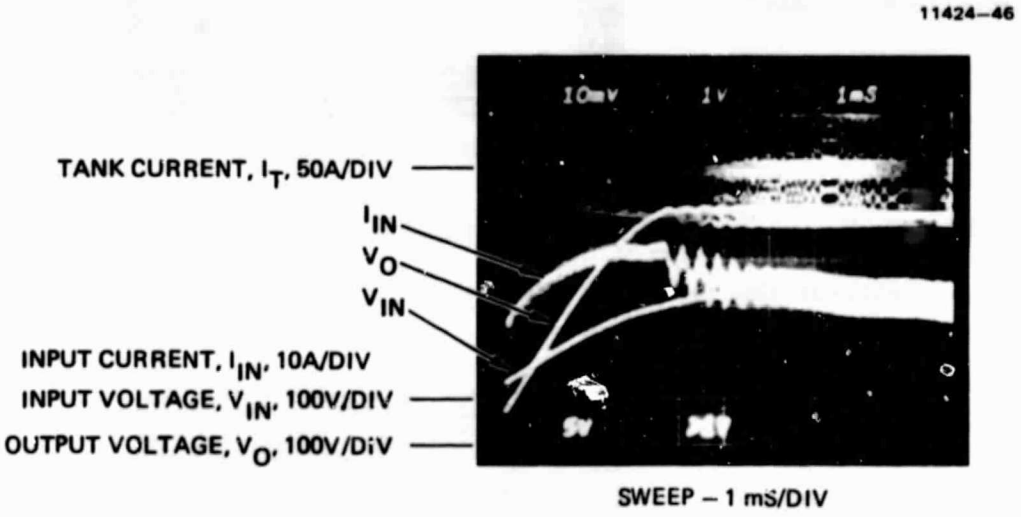


Figure 58. Tank current, input current, input voltage, and output voltage during a typical turn-on transient.

11424-47

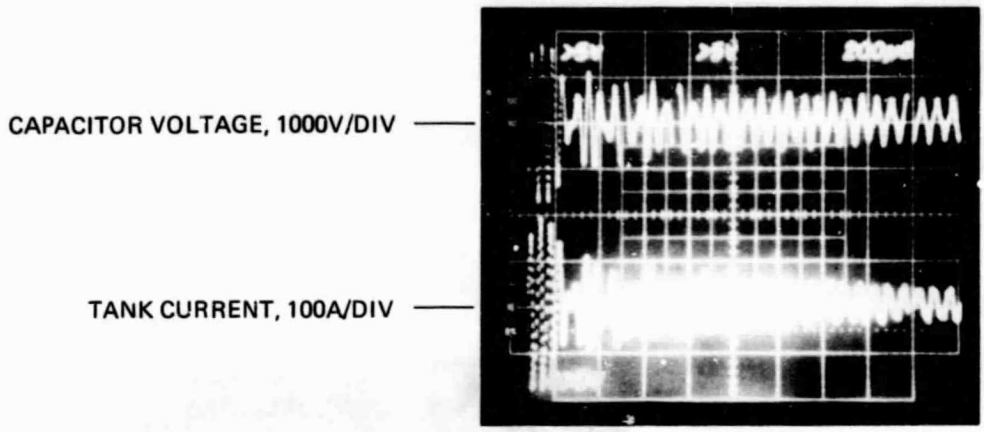


Figure 59. Tank current and resonant capacitor voltage response to a load transient of 500 V at 20 A to short circuit without the peak tank current limiting circuitry.

11424-48

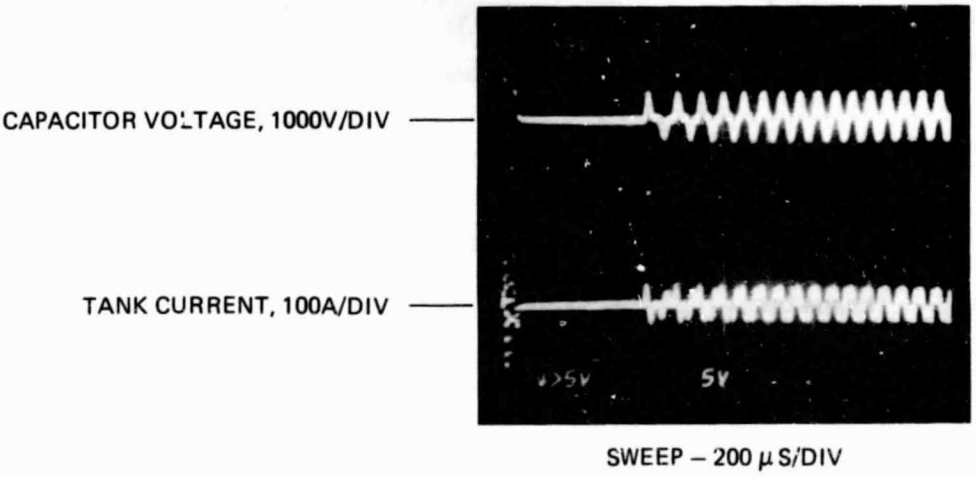


Figure 60. Tank current and resonant capacitor voltage response to a load transient of 500 V at 20 A to short circuit with the peak tank current limiting circuitry.

11424-49

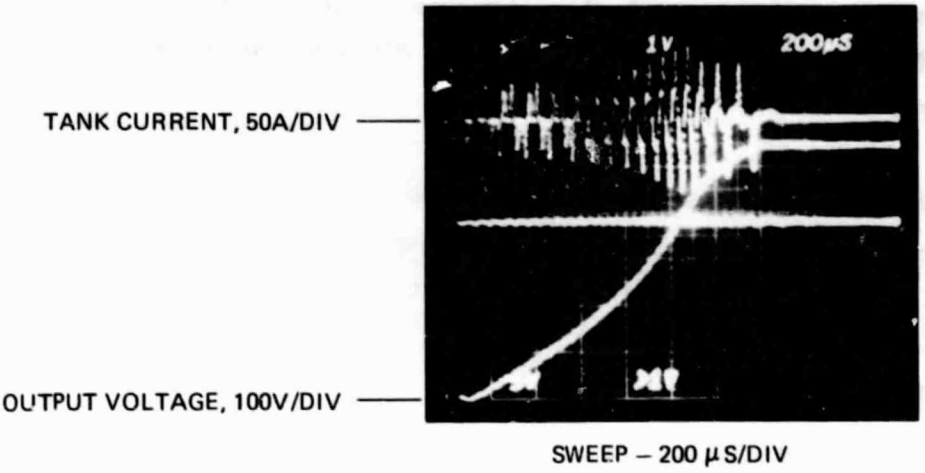


Figure 61. The tank current and output voltage response to a load transient of short circuit to open circuit (350 V setpoint) with original output voltage limiting.

11424-50

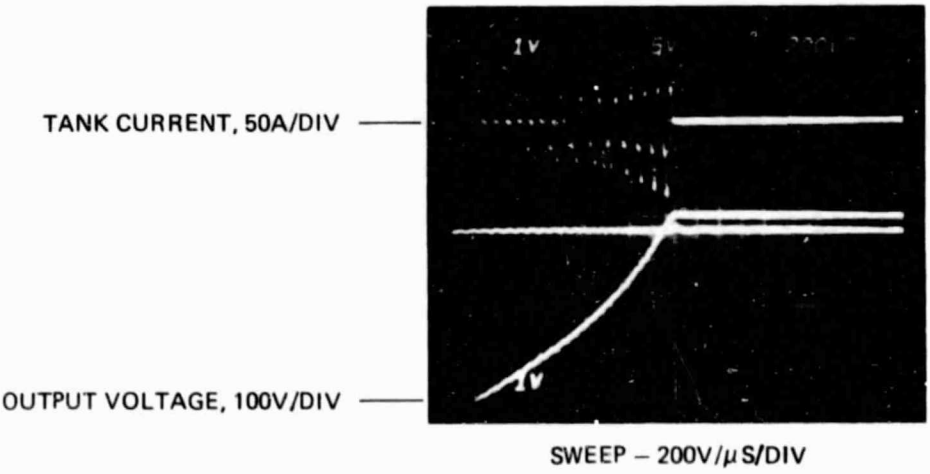


Figure 62. The tank current and output voltage response to a load transient of short circuit to open circuit (350 V setpoint) with improved output voltage limiting.

350 V setpoint by 200 V, which is unacceptable. The output voltage limiting circuitry at this time was a fixed level (≈550 V), optically coupled circuit that phased the V/F converter back when the output voltage exceeded 550 V. This circuitry was eliminated and a circuit (U16 and associated components of Figure 38(a)) whose trip level is a function of the programmed setpoint was added. The response of the output voltage to the same transient condition after this change in the control circuitry was incorporated is shown in Figure 62. The output voltage overshoots the 350 V setpoint by only 50 V with this circuitry.

Figures 63, 64, 65, and 66 show typical responses to load transients of short circuit to the operating point (500 V at 10 A), operating point (450 V at 18 A) to open circuit, open circuit to the operating point (500 V, 20 A), and open circuit (500 V) to short circuit, respectively.

## F. EFFICIENCY MEASUREMENTS

The efficiency of the inverter was measured under static conditions while operating into a resistive load. The efficiency versus output power for loads of 25 Ω and 50 Ω is shown in Figure 67. This figure shows that the efficiency is almost constant for output powers above the 2-kW level. These curves represent the efficiency of the main DC input-power bus to the output of the inverter and the data from which they were drawn is given in Table 19.

Tables 20 and 21 list the power draw of the various drive and control circuitry functions associated with the inverter for loads of 25 Ω and 50 Ω, respectively. These tables show that the power draw by these various functions increases as the output power increases, except for the solid-state circuit breaker and the -12 V control, which remain constant.

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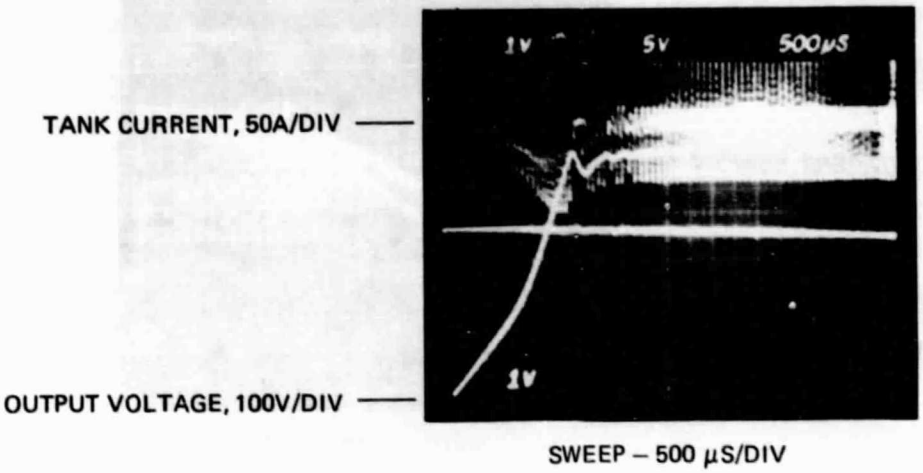


Figure 63. Tank current and output voltage response to a load transient of short circuit to the operating point (500 V at 10 A).

11424-52

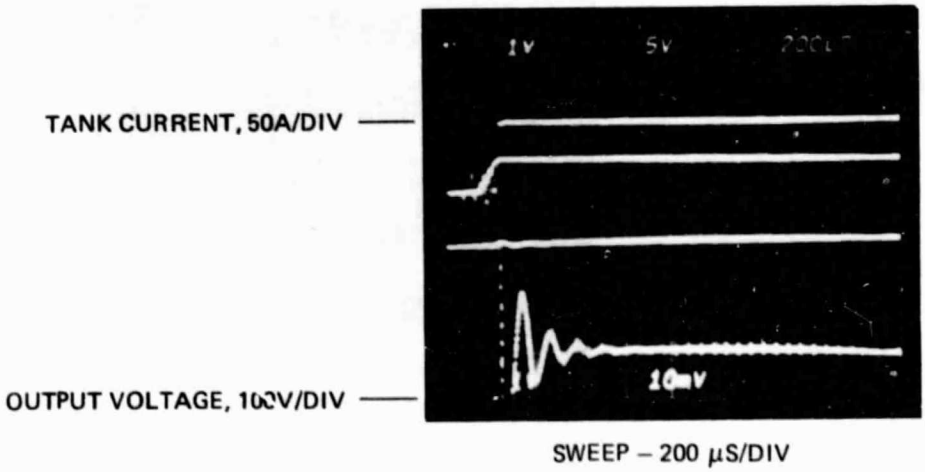


Figure 64. Tank current and output voltage response to a load transient of the operating point (450 V at 18 A) to open circuit.

11424-53

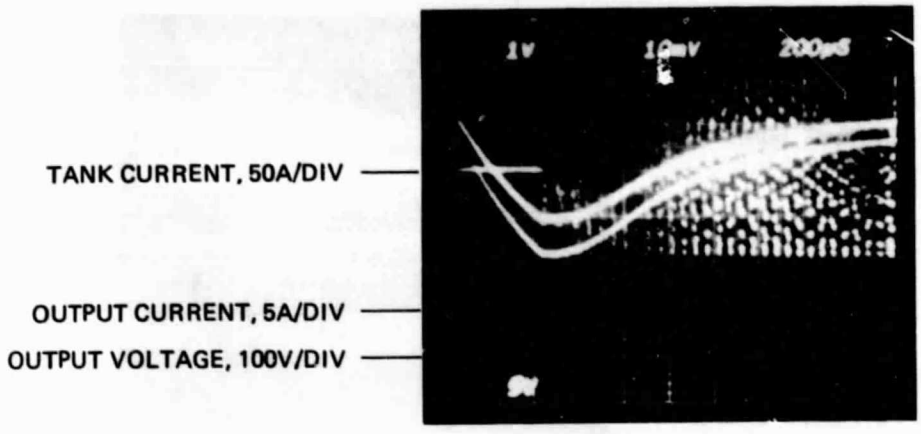


Figure 65. Tank current, output current, and output voltage response to a load transient of open circuit to the operating point (500 V at 20 A).

11424-54

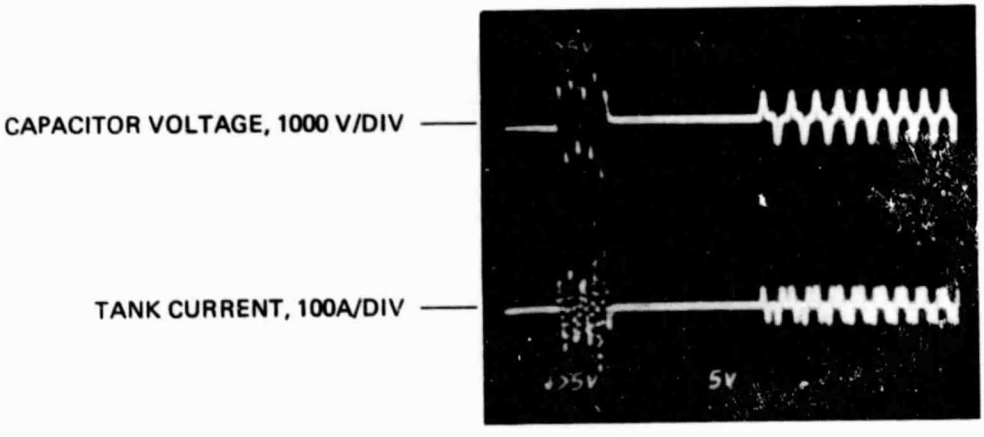


Figure 66. Tank current and resonant capacitor voltage response to a load transient of open circuit (500 V) to short circuit.

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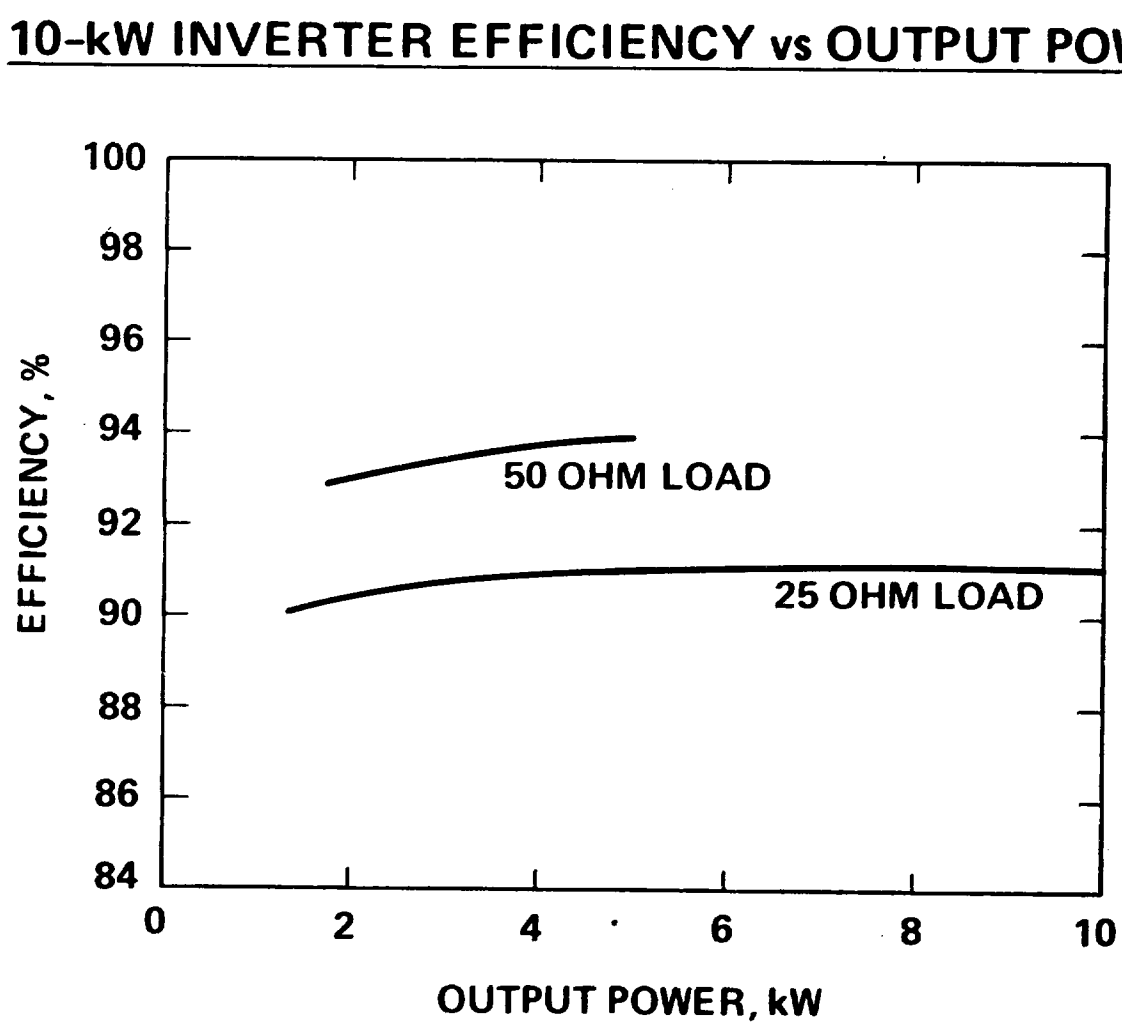


Figure 67. Efficiency versus output power for the 10-kW inverter.

TABLE 19. EFFICIENCY DATA FOR THE 10-kW INVERTER

| Efficiency Data | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $V_{IN}$, V | $I_{IN}$, A | $P_{IN}$, W | $R_L$, Ω | $V_o$, V | $I_o$, A | $P_o$, W | $P_{LOSS}$, W | EFF., % |
| 258 | 6.90 | 1,780 | 25 | 200 | 8.04 | 1,608 | 172 | 90.32 |
| 255 | 10.90 | 2,780 | 25 | 250 | 10.08 | 2,520 | 260 | 90.66 |
| 252 | 15.80 | 3,982 | 25 | 300 | 12.06 | 3,618 | 364 | 90.86 |
| 249 | 21.70 | 5,403 | 25 | 350 | 14.04 | 4,914 | 489 | 90.94 |
| 244 | 28.80 | 7,027 | 25 | 400 | 15.96 | 6,384 | 643 | 90.84 |
| 241 | 32.90 | 7,929 | 25 | 425 | 17.16 | 7,217 | 712 | 91.01 |
| 238 | 37.10 | 8,830 | 25 | 450 | 17.88 | 8,046 | 784 | 91.12 |
| 235 | 41.80 | 9,823 | 25 | 475 | 18.84 | 8,949 | 874 | 91.10 |
| 232 | 46.90 | 10,881 | 25 | 500 | 19.80 | 9,900 | 981 | 90.98 |
| 257 | 9.84 | 2,529 | 50 | 350 | 6.73 | 2,356 | 173 | 93.16 |
| 253 | 16.40 | 4,143 | 50 | 450 | 8.62 | 3,881 | 262 | 93.67 |

TABLE 20. POWER DRAWN BY THE VARIOUS DRIVE AND CONTROL CIRCUITRY FUNCTIONS FOR A LOAD OF 25 OHMS AND 11 POWER LEVELS

| Output Conditions | | | Drive and Control Circuitry Power Draw, W | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_o$, V | $I_o$, A | $P_o$, W | Base Drive (12 V) | Base Drive (75 V) | Negative Bias Supply | Solid-State Circuit Breaker | Control (+12 V) | Control (-12 V) | Total |
| 100 | 4.05 | 405 | 11.48 | 23.22 | 4.45 | 26.33 | 0.19 | 0.11 | 66.58 |
| 200 | 8.10 | 1,620 | 22.23 | 43.44 | 8.53 | 25.97 | 1.47 | 0.12 | 101.77 |
| 250 | 10.50 | 2,513 | 25.37 | 48.69 | 9.86 | 25.73 | 1.69 | 0.12 | 111.45 |
| 300 | 12.00 | 3,600 | 27.18 | 53.93 | 11.30 | 25.13 | 1.81 | 0.12 | 119.47 |
| 350 | 13.98 | 4,893 | 28.99 | 56.92 | 13.10 | 24.88 | 1.93 | 0.12 | 125.95 |
| 400 | 15.87 | 6,348 | 29.60 | 59.92 | 14.90 | 24.40 | 2.05 | 0.12 | 130.99 |
| 425 | 16.83 | 7,153 | 30.20 | 61.42 | 15.87 | 24.28 | 2.11 | 0.12 | 134.00 |
| 450 | 17.79 | 8,006 | 30.20 | 63.67 | 16.95 | 24.16 | 2.17 | 9.12 | 137.27 |
| 475 | 18.72 | 8,892 | 30.80 | 64.41 | 17.73 | 24.14 | 2.23 | 0.12 | 139.44 |
| 500 | 19.65 | 9,825 | 31.17 | 66.66 | 18.84 | 23.92 | 2.29 | 0.12 | 143.00 |
| 511 | 20.07 | 10,256 | 31.41 | 67.41 | 19.23 | 23.92 | 2.84 | 0.12 | 144.93 |

TABLE 21. POWER DRAWN BY THE VARIOUS DRIVE AND CONTROL CIRCUITRY FUNCTIONS FOR A LOAD OF 50 OHMS AND 7 POWER LEVELS

| Output Conditions | | | Drive and Control Circuitry Power Draw, W | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $V_o$, V | $I_o$, A | $P_o$, W | Base Drive (12 V) | Base Drive (75 V) | Negative Bias Supply | Solid-State Circuit Breaker | Control (+12 V) | Control (-12 V) | Total |
| 100 | 1.98 | 198 | 5.44 | 13.48 | 2.64 | 26.09 | 0.75 | 0.12 | 48.52 |
| 200 | 3.90 | 780 | 10.87 | 22.47 | 4.69 | 25.97 | 0.99 | 0.12 | 65.11 |
| 300 | 5.82 | 1,746 | 16.31 | 33.71 | 6.92 | 25.73 | 1.21 | 0.12 | 84.04 |
| 350 | 6.78 | 2,373 | 19.33 | 37.45 | 8.17 | 25.61 | 1.33 | 0.12 | 92.01 |
| 400 | 7.68 | 3,972 | 21.74 | 42.69 | 9.26 | 25.37 | 1.45 | 0.12 | 100.63 |
| 450 | 8.64 | 3,888 | 23.56 | 46.44 | 10.34 | 25.37 | 1.57 | 0.12 | 107.39 |
| 500 | 9.57 | 4,785 | 24.76 | 48.69 | 11.42 | 25.37 | 1.69 | 0.12 | 112.05 |

## SECTION 7

## CONCLUSIONS AND RECOMMENDATIONS

Two types of new bipolar switching transistors (the Westinghouse D60T and D7ST) have been characterized for use as switches in Series Resonant Inverters and/or Converters. The D60T is approximately three times faster than the D7ST, having a storage time in the range of 1.5 to 2.0 μsec, as opposed to 5 to 6 μsec for the D7ST.

The base-drive requirements to optimize total device dissipation and maximize operating frequency were determined by a parametric study of the base-drive parameters. A base-drive circuit employing regenerative feedback, a large amplitude leading-edge current-pulse, a large amplitude turn-off current-pulse, and reverse base bias during the transistor off-time was developed to provide these optimum base-drive requirements.

The suitability of the D60T to function as a switch in a series resonant converter was demonstrated by the successful development and testing of a 10-kW, full-bridge series resonant converter. The unit achieved an electrical efficiency of 91% at its full power level of 500 V and 20 A, and an efficiency of 93.7% at a half power load of 500 V and 10 A.

There are no inherent problems that would prevent this 10-kW design from being upgraded to a space-qualified status. The major effort to do this would be in the areas of qualifying the D60T transistors, qualifying the series resonant capacitors, and thermal-vacuum packaging of the entire unit.

Based on the performance of this 10-kW unit employing D60T transistors it appears feasible to produce a 25-kW series resonant converter by use of the D7ST transistor with its 2.5 times higher current rating. The longer storage time of the D7ST may, however, cause some performance penalty in the area of efficiency. Future work in the area of transistor development should be to reduce the storage time and to provide better device packages. The inductance of the base, collector, and emitter leads is a major problem with the present packages because of the high current levels (hundreds of amps) involved.

# APPENDIX A

## ADDITIONAL TRANSISTOR CHARACTERIZATION DATA

TABLE A-1. RELATIVE POWER DISSIPATION VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D60T (No. 60-1)

| Parameter | | Relative Power Dissipation | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 40 | 10 | - | 0.70 | 0.68 | 0.68 | 0.69 | 0.67 | 0.71 | 1.92 | 1.86 | 1.87 | 1.85 | 1.89 | 1.89 | 1.93 |
| 40 | 20 | - | - | - | 0.76 | 0.73 | 0.73 | 0.73 | - | 1.66 | - | 1.64 | - | 1.64 | 1.63 |
| 40 | 40 | - | - | 1.12 | 1.08 | 1.04 | 1.02 | 1.00 | - | 1.34 | - | 1.28 | - | 1.28 | 1.26 |
| 60 | 10 | - | 1.70 | 1.58 | 1.53 | 1.51 | 1.54 | - | 3.33 | 3.26 | 3.24 | 3.27 | - | 3.28 | - |
| 60 | 20 | - | - | - | 1.61 | 1.58 | 1.57 | 1.57 | - | 2.86 | - | 2.86 | - | 2.86 | 2.88 |
| 60 | 40 | - | - | 2.30 | 2.20 | 2.18 | 2.18 | 2.14 | - | 2.44 | 2.50 | 2.48 | - | 2.46 | 2.48 |
| 100 | 10 | 4.70 | 4.12 | 4.02 | 4.00 | 4.04 | 3.94 | - | 7.58 | 7.44 | 7.36 | 7.34 | 7.34 | 7.36 | 7.36 |
| 100 | 20 | - | 4.56 | 4.42 | 4.42 | 4.42 | 4.40 | - | 6.40 | 6.44 | - | 6.48 | - | 6.50 | 6.56 |
| 100 | 40 | 6.88 | 6.54 | 6.54 | 6.96 | - | - | - | 6.70 | 6.42 | 6.48 | 6.56 | - | 6.60 | - |
| 140 | 10 | - | 7.68 | 7.52 | 7.52 | 7.98 | - | - | 10.36 | 10.34 | 10.38 | 10.54 | - | - | - |
| 140 | 20 | - | 8.76 | 8.46 | 8.26 | 8.92 | - | - | 10.16 | 10.26 | 10.38 | 10.52 | - | - | - |

TABLE A-2. LEADING EDGE PULSE DURATION VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D60T (No. 60-1)

| Parameter | | Leading Edge Pulse Duration, μs | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 40 | 10 | - | 6.5 | 14.0 | 23.0 | 24.0 | 31.0 | 37.0 | - | 4.0 | 6.0 | 6.0 | 7.0 | 6.0 | 48.0 |
| 40 | 20 | - | - | - | 8.0 | 9.0 | 11.0 | 12.5 | - | 19.0 | - | 18.4 | - | 19.0 | 18.0 |
| 40 | 40 | - | - | 3.0 | 4.0 | 3.8 | 4.0 | 5.4 | - | 7.1 | - | 8.2 | - | 7.2 | 7.1 |
| 60 | 10 | - | 2.0 | 3.0 | 15.5 | 28.0 | 29.5 | 34.0 | 2.0 | 2.0 | 3.0 | 2.5 | - | 47.0 | - |
| 60 | 20 | - | - | - | 12.5 | 13.5 | 15.0 | 14.0 | - | 18.7 | - | 18.9 | - | 19.5 | 19.4 |
| 60 | 40 | - | - | 3.4 | 5.1 | 6.0 | 6.0 | 6.0 | - | 2.6 | 3.4 | 7.7 | - | 6.9 | 8.2 |
| 100 | 10 | 3.0 | 3.0 | 27.5 | 31.0 | 33.0 | 34.0 | - | 2.0 | 2.0 | 45.0 | 45.0 | 44.0 | 44.0 | 44.0 |
| 100 | 20 | - | 4.0 | 11.5 | 12.5 | 13.4 | 15.0 | - | 21.0 | 20.0 | - | 19.0 | - | 19.5 | 19.2 |
| 100 | 40 | 2.0 | 3.5 | 5.3 | 6.4 | - | - | - | 2.5 | 4.7 | 5.8 | 7.2 | - | 7.6 | - |
| 140 | 10 | - | 27.0 | 31.5 | 34.0 | 35.0 | - | - | 42.0 | 41.0 | 41.0 | 42.0 | - | - | - |
| 140 | 20 | - | 11.3 | 13.8 | 15.0 | 16.0 | - | - | 21.4 | 21.5 | 21.0 | 20.0 | - | - | - |

TABLE A-3. LEADING EDGE PULSE AMPLITUDE VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D60T (No. 60-1)

| Parameter | | Leading Edge Pulse Amplitude, A | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 | 3:1 | 4:1 | 5:1 | 6:1 | 7:1 | 8:1 | 10:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 40 | 10 | - | 3 | 2 | 2.0 | 3 | 2 | 3 | - | 6 | 7 | 8 | 9 | 7 | 2 |
| 40 | 20 | - | - | - | 3.0 | 4 | 4 | 4 | - | 7 | - | 8 | - | 11 | 13 |
| 40 | 40 | - | - | 4 | 4.0 | 5 | 6 | 6 | - | 5 | - | 6 | - | 9 | 10 |
| 60 | 10 | - | 2 | 3 | 3.5 | 2 | 3 | - | 2 | 2 | 2 | 6 | - | 3 | - |
| 60 | 20 | - | - | - | 5.0 | 6 | 6 | 7 | - | 14 | - | 15 | - | 15 | 15 |
| 60 | 40 | - | - | 7 | 7.0 | 8 | 8 | 9 | - | 15 | 15 | 10 | - | 14 | 11 |
| 100 | 10 | 3 | 3 | 3 | 5.0 | 7 | 8 | - | 2 | 2 | 2 | 6 | 7 | 9 | 11 |
| 100 | 20 | - | 9 | 6 | 9.0 | 10 | 10 | - | 3 | 5 | - | 12 | - | 15 | 15 |
| 100 | 40 | 15 | 15 | 15 | 15.0 | - | - | - | 15 | 15 | 15 | 15 | - | 15 | - |
| 140 | 10 | - | 4 | 9 | 13.0 | 15 | - | - | 10 | 14 | 15 | 15 | - | - | - |
| 140 | 20 | - | 10 | 13 | 15.0 | 15 | - | - | 8 | 14 | 15 | 15 | - | - | - |

TABLE A-4. RELATIVE POWER DISSIPATION VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D7ST (No. 12)

| Parameter | | Relative Power Dissipation | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 100 | 10 | - | 0.39 | - | 0.34 | 0.33 | 0.31 | 0.32 | - | 0.42 | - | 0.42 | 0.40 | 0.40 | 0.40 |
| 100 | 20 | - | 0.62 | - | 0.56 | 0.54 | 0.52 | 0.51 | - | 0.60 | - | 0.55 | 0.54 | 0.54 | 0.52 |
| 100 | 40 | - | 0.82 | - | 0.72 | 0.71 | 0.70 | 0.67 | - | 0.79 | - | 0.73 | 0.72 | 0.70 | 0.70 |
| 150 | 10 | - | 0.69 | - | 0.63 | 0.62 | 0.61 | 0.60 | - | 0.77 | - | 0.74 | 0.73 | 0.73 | 0.72 |
| 150 | 20 | - | 1.16 | - | 1.04 | 1.01 | 1.00 | 1.00 | - | 1.11 | - | 1.03 | 1.02 | 1.00 | 1.01 |
| 150 | 40 | - | 1.65 | - | 1.56 | 1.52 | 1.54 | 1.51 | - | 1.64 | - | 1.58 | 1.55 | 1.54 | 1.49 |
| 250 | 10 | - | 1.68 | - | 1.65 | 1.55 | 1.55 | 1.53 | - | 1.85 | - | 1.80 | 1.80 | 1.83 | 1.83 |
| 250 | 20 | - | 2.34 | - | 2.16 | 2.16 | 2.20 | 2.34 | - | 2.40 | - | 2.32 | 2.26 | 2.32 | 2.46 |
| 250 | 40 | 5.92 | 5.92 | 5.16 | 5.76 | 6.48 | - | - | 5.52 | 4.84 | 5.44 | 6.20 | - | - | - |
| 350 | 10 | 3.55 | 3.40 | 3.28 | 3.50 | - | - | - | 3.80 | 3.70 | 3.70 | 3.78 | - | - | - |
| 350 | 20 | 5.08 | 4.96 | 6.00 | 7.76 | - | - | - | 5.04 | 5.04 | 5.72 | 7.00 | - | - | - |

## TABLE A-5. LEADING EDGE PULSE DURATION VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D7ST (No. 12)

| Parameter | | Leading Edge Pulse Duration, μs | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 100 | 10 | - | 6.0 | - | 8.0 | 11.0 | 18.0 | 27.0 | - | 37.0 | - | 38.0 | 34.0 | 34.0 | 35.0 |
| 100 | 20 | - | 5.0 | - | 6.0 | 6.5 | 7.2 | 9.2 | - | 4.0 | - | 6.5 | 8.5 | 10.5 | 11.5 |
| 100 | 40 | - | 2.2 | - | 2.9 | 3.7 | 4.2 | 3.8 | - | 2.9 | - | 3.0 | 4.1 | 4.4 | 5.2 |
| 150 | 10 | - | 3.0 | - | 13.0 | 30.0 | 32.0 | 31.0 | - | 30.0 | - | 38.0 | 37.0 | 38.0 | 37.0 |
| 150 | 20 | - | 4.8 | - | 6.8 | 8.0 | 9.5 | 10.0 | - | 4.0 | - | 7.5 | 11.0 | 12.5 | 12.5 |
| 150 | 40 | - | 3.8 | - | 3.8 | 4.2 | 4.5 | 5.0 | - | 3.5 | - | 3.8 | 4.5 | 5.2 | 5.3 |
| 250 | 10 | - | 5.0 | - | 27.0 | 30.0 | 31.0 | 34.0 | - | 18.0 | - | 42.0 | 42.0 | 42.0 | 44.0 |
| 250 | 20 | - | 8.0 | - | 11.0 | 13.0 | 14.5 | 15.5 | - | 7.0 | - | 13.0 | 15.5 | 16.0 | 17.5 |
| 250 | 40 | 4.0 | 4.8 | 5.2 | 7.1 | - | - | - | 4.0 | 5.5 | 7.1 | 8.2 | - | - | - |
| 350 | 10 | 8.0 | 27.0 | 30.0 | 33.0 | - | - | - | 16.0 | 24.0 | 30.0 | 32.0 | - | - | - |
| 350 | 20 | 8.0 | 13.0 | 14.5 | 17.0 | - | - | - | 9.5 | 15.0 | 18.0 | 18.0 | - | - | - |

TABLE A-6. LEADING EDGE PULSE AMPLITUDE VERSUS REGENERATIVE FEEDBACK TURNS RATIO FOR A TYPICAL D7ST (No. 12)

| Parameter | | Leading Edge Pulse Amplitude, A | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | | | Unsaturated | | | | | | |
| Turns Ratio | | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 | 3:1 | 4:1 | 5:1 | 6:1 | 8:1 | 10:1 | 12:1 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | | | | | |
| 100 | 10 | - | 8 | - | 8 | 10 | 8 | 8 | - | 4 | - | 10 | 14 | 16 | 16 |
| 100 | 20 | - | 8 | - | 14 | 14 | 16 | 16 | - | 14 | - | 12 | 14 | 12 | 14 |
| 100 | 40 | - | 20 | - | 24 | 22 | 22 | 28 | - | 22 | - | 22 | 18 | 18 | 18 |
| 150 | 10 | - | 10 | - | 8 | 8 | 12 | 12 | - | 5 | - | 12 | 16 | 16 | 20 |
| 150 | 20 | - | 18 | - | 20 | 24 | 24 | 24 | - | 18 | - | 18 | 18 | 18 | 20 |
| 150 | 40 | - | 26 | - | 30 | 30 | 30 | 30 | - | 26 | - | 30 | 30 | 30 | 30 |
| 250 | 10 | - | 8 | - | 16 | 24 | 26 | 28 | - | 8 | - | 20 | 28 | 30 | 30 |
| 250 | 20 | - | 24 | - | 30 | 0 | 30 | 30 | - | 24 | - | 28 | 30 | 30 | 30 |
| 250 | 40 | 28 | 30 | 30 | 30 | - | - | - | 30 | 30 | 30 | 30 | - | - | - |
| 350 | 10 | 8 | 16 | 30 | 30 | - | - | - | 10 | 24 | 26 | 30 | - | - | - |
| 350 | 20 | 30 | 30 | 30 | 30 | - | - | - | 30 | 30 | 30 | 30 | - | - | - |

TABLE A-7. TOTAL DEVICE DISSIPATION VERSUS PEAK COLLECTOR CURRENT AND RESONANT FREQUENCY FOR THE D60Ts

| Parameter | | Total Device Dissipation, W | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | | Unsaturated | | | | |
| Transistor Number | | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 | 60-1 | 60-2 | 60-3 | 60-4 | 60-5 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | | | |
| 40 | 10 | 13.2 | 12.8 | 12.6 | 12.8 | 13.2 | 27.6 | 27.2 | 27.6 | 26.4 | 28.0 |
| 40 | 20 | 13.6 | 13.6 | 13.6 | 13.6 | 14.2 | 26.4 | 26.4 | 25.6 | 25.6 | 28.0 |
| 40 | 40 | 21.4 | 20.6 | 20.6 | 21.4 | 21.4 | 24.4 | 23.3 | 23.7 | 23.7 | 24.8 |
| 60 | 10 | 22.4 | 22.4 | 20.4 | 22.0 | 23.6 | 52.0 | 52.0 | 49.2 | 51.2 | 52.0 |
| 60 | 20 | 25.6 | 25.2 | 24.2 | 25.6 | 26.8 | 48.0 | 46.8 | 43.2 | 47.6 | 48.0 |
| 60 | 40 | 31.8 | 30.7 | 30.3 | 32.6 | 31.8 | 37.9 | 37.1 | 36.4 | 40.2 | 38.6 |
| 100 | 10 | 62.4 | 58.4 | 57.6 | 60.0 | 62.4 | 121.0 | 116.0 | 112.0 | 116.0 | 112.0 |
| 100 | 20 | 67.2 | 65.6 | 60.8 | 67.2 | 68.0 | 108.0 | 107.0 | 99.0 | 111.0 | 109.0 |
| 100 | 40 | 88.8 | 84.3 | 79.9 | 97.8 | 88.1 | 105.0 | 100.0 | 94.0 | 116.0 | 105.0 |
| 140 | 10 | 126.0 | 126.0 | 128.0 | 136.0 | 142.0 | 210.0 | 216.0 | 195.0 | 227.0 | 216.0 |
| 140 | 20 | 143.0 | 145.0 | 131.0 | 168.0 | 158.0 | 197.0 | 204.0 | 178.0 | 226.0 | 211.0 |

TABLE A-8. TOTAL DEVICE DISSIPATION VERSUS PEAK COLLECTOR CURRENT AND RESONANT FREQUENCY FOR THE D7STs

| Parameter | | Total Device Dissipation, W | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Circuit Configuration | | Saturated | | | | Unsaturated | | | |
| Transistor Number | | 12 | 15 | 36 | 37 | 12 | 15 | 36 | 37 |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | | | | | | | | |
| 100 | 10 | 40.2 | 47.2 | 38.8 | 41.6 | 43.2 | 48.4 | 43.2 | 50.0 |
| 100 | 20 | 57.6 | 56.8 | 56.4 | 59.2 | 58.4 | 61.6 | 56.8 | 59.2 |
| 100 | 40 | 65.6 | 72.8 | 69.6 | 80.0 | 64.8 | 80.4 | 74.4 | 87.2 |
| 150 | 10 | 56.6 | 61.6 | 53.2 | 60.8 | 64.0 | 79.2 | 64.8 | 79.2 |
| 150 | 20 | 83.2 | 83.2 | 80.0 | 99.2 | 83.2 | 90.4 | 82.4 | 92.0 |
| 150 | 40 | 142.0 | 171.0 | 160.0 | 187.0 | 130.0 | 173.0 | 171.0 | 194.0 |
| 250 | 10 | 147.0 | 206.0 | 136.0 | 158.0 | 160.0 | 180.0 | 164.0 | 204.0 |
| 250 | 20 | 214.0 | 258.0 | 211.0 | 240.0 | 232.0 | 234.0 | 222.0 | 259.0 |
| 250 | 40 | 443.0 | 426.0 | 419.0 | 477.0 | 426.0 | 410.0 | 410.0 | 458.0 |
| 350 | 10 | 322.0 | 366.0 | 328.0 | 414.0 | 388.0 | 486.0 | 420.0 | 526.0 |
| 350 | 20 | 435.0 | 480.0 | 464.0 | 531.0 | 461.0 | 501.0 | 490.0 | 560.0 |

TABLE A-9. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D60T NUMBER 60-1

| Circuit Configuration | | Transistor 60-1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | | | Unsaturated | | | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 2 | | 5 | | 10 | | 15 | | 2 | | 5 | | 10 | | 15 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 40 | 10 | 80 | 120 | 65 | 80 | 65 | 55 | 60 | 50 | 65 | 100 | 65 | 75 | 55 | 60 | 55 | 55 |
| 40 | 20 | 75 | 130 | 70 | 95 | 60 | 80 | 55 | 65 | 65 | 130 | 60 | 90 | 55 | 80 | 55 | 70 |
| 40 | 40 | 60 | 105 | 55 | 80 | 50 | 65 | 50 | 55 | 65 | 105 | 60 | 85 | 55 | 70 | 55 | 60 |
| 60 | 10 | 80 | 130 | 75 | 90 | 60 | 60 | 60 | 50 | 60 | 110 | 65 | 85 | 55 | 65 | 55 | 60 |
| 60 | 20 | 80 | 160 | 70 | 110 | 60 | 90 | 60 | 80 | 75 | 150 | 70 | 120 | 60 | 95 | 55 | 80 |
| 60 | 40 | 65 | 150 | 55 | 100 | 50 | 80 | 50 | 70 | 75 | 150 | 65 | 110 | 55 | 85 | 50 | 80 |
| 100 | 10 | 85 | 160 | 70 | 110 | 60 | 80 | 60 | 70 | 70 | 140 | 65 | 105 | 55 | 80 | 60 | 75 |
| 100 | 20 | 80 | 130 | 70 | 100 | 60 | 80 | 65 | 75 | 60 | 130 | 65 | 105 | 60 | 80 | 55 | 75 |
| 100 | 40 | 70 | 130 | 65 | 100 | 55 | 80 | 60 | 75 | 65 | 140 | 70 | 110 | 55 | 85 | 55 | 80 |
| 140 | 10 | 95 | 180 | 80 | 125 | 70 | 95 | 65 | 80 | 80 | 160 | 75 | 120 | 65 | 95 | 60 | 80 |
| 140 | 20 | 75 | 150 | 70 | 120 | 60 | 90 | 65 | 80 | 75 | 150 | 70 | 120 | 60 | 100 | 60 | 85 |

TABLE A-10. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D60T NUMBER 60-2

| Circuit Configuration | | Transistor 60-2 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | | | Unsaturated | | | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 2 | | 5 | | 10 | | 15 | | 2 | | 5 | | 10 | | 15 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 40 | 10 | 70 | 90 | 60 | 170 | 60 | 55 | 55 | 50 | 65 | 100 | 60 | 70 | 55 | 55 | 55 | 50 |
| 40 | 20 | 80 | 120 | 65 | 90 | 55 | 70 | 60 | 65 | 75 | 120 | 60 | 90 | 60 | 70 | 55 | 65 |
| 40 | 40 | 70 | 110 | 60 | 80 | 55 | 65 | 50 | 55 | 70 | 105 | 60 | 80 | 60 | 65 | 55 | 60 |
| 60 | 10 | 75 | 100 | 70 | 75 | 60 | 60 | 55 | 55 | 75 | 110 | 65 | 80 | 60 | 65 | 55 | 55 |
| 60 | 20 | 80 | 150 | 70 | 110 | 60 | 85 | 60 | 80 | 75 | 140 | 60 | 105 | 65 | 85 | 60 | 75 |
| 60 | 40 | 70 | 140 | 60 | 100 | 60 | 80 | 55 | 70 | 70 | 140 | 60 | 100 | 60 | 85 | 55 | 75 |
| 100 | 10 | 75 | 125 | 70 | 100 | 55 | 85 | 60 | 65 | 60 | 130 | 50 | 100 | 55 | 85 | 50 | 75 |
| 100 | 20 | 65 | 120 | 65 | 100 | 60 | 75 | 55 | 70 | 65 | 125 | 55 | 100 | 60 | 80 | 55 | 70 |
| 100 | 40 | 70 | 130 | 65 | 100 | 60 | 80 | 60 | 70 | 65 | 125 | 65 | 100 | 60 | 80 | 60 | 70 |
| 140 | 10 | 75 | 140 | 70 | 110 | 60 | 90 | 65 | 80 | 60 | 150 | 60 | 110 | 60 | 90 | 50 | 80 |
| 140 | 20 | 80 | 140 | 70 | 115 | 60 | 90 | 60 | 80 | 70 | 150 | 60 | 110 | 60 | 90 | 5[illegible] | 80 |

TABLE A-11. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D60T NUMBER 60-3

| Circuit Configuration | | Transistor 60-3 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | | | Unsaturated | | | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 2 | | 5 | | 10 | | 15 | | 2 | | 5 | | 10 | | 15 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 40 | 10 | 75 | 85 | 55 | 65 | 60 | 55 | 50 | 50 | 75 | 95 | 60 | 65 | 60 | 60 | 50 | 50 |
| 40 | 20 | 80 | 110 | 60 | 80 | 65 | 65 | 55 | 60 | 80 | 105 | 65 | 80 | 65 | 70 | 60 | 60 |
| 40 | 40 | 75 | 100 | 60 | 75 | 60 | 60 | 55 | 50 | 70 | 90 | 60 | 75 | 60 | 65 | 50 | 60 |
| 60 | 10 | 75 | 95 | 60 | 75 | 60 | 65 | 55 | 50 | 75 | 100 | 65 | 75 | 70 | 60 | 55 | 55 |
| 60 | 20 | 80 | 135 | 70 | 95 | 65 | 80 | 60 | 70 | 80 | 130 | 70 | 100 | 65 | 80 | 60 | 70 |
| 60 | 40 | 70 | 130 | 65 | 95 | 60 | 75 | 60 | 65 | 70 | 130 | 60 | 100 | 60 | 80 | 55 | 75 |
| 100 | 10 | 75 | 110 | 65 | 85 | 60 | 75 | 55 | 65 | 75 | 120 | 65 | 95 | 60 | 75 | 55 | 65 |
| 100 | 20 | 60 | 110 | 60 | 90 | 60 | 75 | 55 | 65 | 70 | 110 | 65 | 90 | 60 | 80 | 60 | 70 |
| 100 | 40 | 65 | 115 | 60 | 85 | 60 | 75 | 60 | 65 | 60 | 115 | 65 | 90 | 65 | 75 | 60 | 70 |
| 140 | 10 | 75 | 130 | 70 | 100 | 60 | 80 | 60 | 70 | 80 | 130 | 65 | 105 | 60 | 85 | 60 | 75 |
| 140 | 20 | 65 | 125 | 60 | 100 | 65 | 80 | 55 | 70 | 70 | 130 | 65 | 100 | 65 | 80 | 60 | 75 |

TABLE A-12. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D60T NUMBER 60-4

| Circuit Configuration | | Transistor 60-4 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | | | Unsaturated | | | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 2 | | 5 | | 10 | | 15 | | 2 | | 5 | | 10 | | 15 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 40 | 10 | 65 | 85 | 60 | 60 | 50 | 50 | 50 | 50 | 55 | 95 | 50 | 70 | 45 | 55 | 45 | 50 |
| 40 | 20 | 70 | 110 | 60 | 80 | 55 | 65 | 50 | 60 | 70 | 115 | 70 | 90 | 60 | 70 | 60 | 65 |
| 40 | 40 | 70 | 95 | 60 | 70 | 55 | 60 | 50 | 55 | 70 | 90 | 65 | 75 | 60 | 60 | 55 | 55 |
| 60 | 10 | 70 | 95 | 60 | 80 | 55 | 55 | 50 | 50 | 60 | 100 | 55 | 75 | 50 | 60 | 40 | 50 |
| 60 | 20 | 65 | 140 | 60 | 100 | 60 | 80 | 55 | 70 | 75 | 135 | 70 | 100 | 60 | 80 | 60 | 75 |
| 60 | 40 | 70 | 125 | 55 | 100 | 50 | 80 | 50 | 70 | 70 | 125 | 60 | 100 | 55 | 80 | 55 | 70 |
| 100 | 10 | 70 | 120 | 65 | 90 | 60 | 70 | 55 | 65 | 70 | 135 | 70 | 100 | 60 | 80 | 55 | 75 |
| 100 | 20 | 65 | 105 | 60 | 85 | 60 | 70 | 50 | 60 | 65 | 115 | 65 | 95 | 60 | 80 | 60 | 65 |
| 100 | 40 | 60 | 110 | 60 | 90 | 50 | 80 | 45 | 70 | 65 | 110 | 65 | 90 | 55 | 80 | 55 | 75 |
| 140 | 10 | 75 | 140 | 70 | 100 | 60 | 80 | 55 | 75 | 80 | 135 | 75 | 105 | 60 | 85 | 65 | 80 |
| 140 | 20 | 65 | 130 | 65 | 100 | 60 | 80 | 55 | 70 | 70 | 135 | 70 | 105 | 60 | 85 | 60 | 75 |

TABLE A-13. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D60T NUMBER 60-5

| Circuit Configuration | | Transistor 60-5 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | | | Unsaturated | | | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 2 | | 5 | | 10 | | 15 | | 2 | | 5 | | 10 | | 15 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 40 | 10 | 80 | 80 | 75 | 65 | 60 | 55 | 60 | 50 | 80 | 85 | 75 | 65 | 65 | 50 | 65 | 50 |
| 40 | 20 | 80 | 105 | 75 | 85 | 65 | 70 | 60 | 60 | 80 | 110 | 75 | 85 | 60 | 70 | 60 | 60 |
| 40 | 40 | 75 | 90 | 75 | 70 | 60 | 60 | 65 | 55 | 70 | 85 | 70 | 75 | 60 | 60 | 60 | 55 |
| 60 | 10 | 75 | 90 | 65 | 75 | 60 | 60 | 60 | 55 | 80 | 95 | 75 | 75 | 60 | 60 | 60 | 55 |
| 60 | 20 | 80 | 125 | 75 | 100 | 60 | 80 | 60 | 75 | 80 | 130 | 75 | 100 | 65 | 80 | 65 | 70 |
| 60 | 40 | 80 | 115 | 75 | 95 | 60 | 80 | 60 | 65 | 75 | 120 | 70 | 95 | 60 | 80 | 65 | 65 |
| 100 | 10 | 80 | 105 | 75 | 85 | 60 | 70 | 65 | 70 | 80 | 110 | 70 | 90 | 65 | 75 | 65 | 70 |
| 100 | 20 | 90 | 105 | 70 | 85 | 60 | 75 | 60 | 70 | 70 | 105 | 70 | 85 | 60 | 75 | 65 | 70 |
| 100 | 40 | 70 | 105 | 75 | 90 | 60 | 75 | 65 | 65 | 70 | 110 | 75 | 85 | 60 | 75 | 65 | 65 |
| 140 | 10 | 80 | 125 | 80 | 100 | 65 | 80 | 70 | 75 | 85 | 125 | 75 | 100 | 65 | 90 | 70 | 75 |
| 140 | 20 | 75 | 120 | 70 | 95 | 60 | 80 | 70 | 75 | 70 | 125 | 75 | 100 | 65 | 85 | 65 | 80 |

TABLE A-14. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D7ST NUMBER 12

| Circuit Configuration | | Transistor 12 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 5 | | 15 | | 30 | | 5 | | 15 | | 30 | |
| eak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 100 | 10 | 180 | 115 | 130 | 70 | 130 | 60 | 180 | 115 | 120 | 75 | 135 | 60 |
| 100 | 20 | 180 | 120 | 125 | 70 | 130 | 60 | 180 | 120 | 130 | 70 | 135 | 55 |
| 100 | 40 | 190 | 115 | 120 | 65 | 130 | 55 | 180 | 110 | 120 | 70 | 130 | 60 |
| 150 | 10 | 180 | 115 | 130 | 70 | 130 | 60 | 180 | 120 | 130 | 75 | 125 | 60 |
| 150 | 20 | 180 | 125 | 125 | 75 | 140 | 65 | 180 | 135 | 130 | 80 | 135 | 65 |
| 150 | 40 | 170 | 130 | 125 | 80 | 135 | 60 | 180 | 130 | 130 | 80 | 130 | 60 |
| 250 | 10 | 160 | 110 | 130 | 75 | 135 | 60 | 165 | 115 | 135 | 75 | 140 | 60 |
| 250 | 20 | 170 | 120 | 130 | 80 | 120 | 60 | 180 | 130 | 135 | 80 | 130 | 65 |
| 250 | 40 | 160 | 160 | 125 | 80 | 130 | 65 | 160 | 150 | 130 | 90 | 130 | 75 |
| 350 | 10 | 160 | 140 | 130 | 90 | 130 | 65 | 170 | 155 | 135 | 90 | 135 | 70 |
| 350 | 20 | 170 | 140 | 130 | 90 | 135 | 70 | 150 | 140 | 130 | 95 | 135 | 75 |

TABLE A-15. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D7ST NUMBER 15

| Circuit Configuration | | Transistor 15 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 5 | | 15 | | 30 | | 5 | | 15 | | 30 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 100 | 10 | 170 | 120 | 135 | 65 | 120 | 55 | 170 | 125 | 140 | 70 | 125 | 55 |
| 100 | 20 | 150 | 110 | 140 | 70 | 130 | 55 | 160 | 115 | 150 | 65 | 120 | 55 |
| 100 | 40 | 160 | 110 | 140 | 70 | 125 | 50 | 170 | 120 | 155 | 70 | 125 | 50 |
| 150 | 10 | 170 | 130 | 140 | 75 | 125 | 60 | 180 | 140 | 145 | 80 | 125 | 60 |
| 150 | 20 | 170 | 140 | 145 | 80 | 130 | 60 | 170 | 140 | 150 | 85 | 130 | 65 |
| 150 | 40 | 170 | 135 | 130 | 80 | 130 | 60 | 170 | 140 | 140 | 80 | 125 | 60 |
| 250 | 10 | 180 | 130 | 145 | 80 | 125 | 60 | 165 | 135 | 140 | 80 | 130 | 65 |
| 250 | 20 | 150 | 130 | 140 | 80 | 130 | 55 | 160 | 130 | 140 | 80 | 130 | 60 |
| 250 | 40 | 150 | 135 | 145 | 80 | 120 | 60 | 165 | 150 | 140 | 85 | 125 | 65 |
| 350 | 10 | 165 | 145 | 140 | 90 | 125 | 70 | 170 | 160 | 145 | 95 | 130 | 75 |
| 350 | 20 | 160 | 140 | 140 | 90 | 135 | 65 | 160 | 150 | 160 | 100 | 130 | 75 |

TABLE A-16. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D7ST NUMBER 36

| Circuit Configuration | | Transistor 36 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 5 | | 15 | | 30 | | 5 | | 15 | | 30 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 100 | 10 | 165 | 120 | 140 | 70 | 110 | 60 | 160 | 130 | 140 | 75 | 110 | 60 |
| 100 | 20 | 160 | 130 | 140 | 70 | 110 | 55 | 160 | 130 | 140 | 75 | 120 | 55 |
| 100 | 40 | 170 | 130 | 140 | 80 | 120 | 60 | 160 | 130 | 140 | 75 | 120 | 60 |
| 150 | 10 | 160 | 140 | 145 | 85 | 120 | 60 | 170 | 140 | 140 | 90 | 115 | 65 |
| 150 | 20 | 170 | 140 | 135 | 80 | 120 | 60 | 165 | 140 | 140 | 85 | 110 | 60 |
| 150 | 40 | 160 | 140 | 140 | 85 | 120 | 65 | 160 | 160 | 140 | 85 | 130 | 60 |
| 250 | 10 | 145 | 140 | 125 | 75 | 115 | 60 | 150 | 140 | 135 | 85 | 115 | 70 |
| 250 | 20 | 160 | 140 | 130 | 85 | 115 | 65 | 150 | 140 | 135 | 90 | 110 | 65 |
| 250 | 40 | 150 | 140 | 130 | 80 | 120 | 70 | 150 | 140 | 135 | 90 | 120 | 75 |
| 350 | 10 | 160 | 155 | 145 | 95 | 110 | 70 | 170 | 170 | 140 | 100 | 125 | 80 |
| 350 | 20 | 140 | 160 | 140 | 90 | 120 | 75 | 145 | 160 | 135 | 95 | 120 | 80 |

TABLE A-17. DELAY TIME AND RISE TIME VERSUS LEADING-EDGE PULSE AMPLITUDE FOR D7ST NUMBER 37

| Circuit Configuration | | Transistor 37 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Leading Edge Pulse Amplitude, Amps | | 5 | | 15 | | 30 | | 5 | | 15 | | 30 | |
| Peak Ic, Amps | Resonant Frequency, fr, kHz | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns | td ns | tr ns |
| 100 | 10 | 200 | 140 | 135 | 80 | 130 | 60 | 190 | 140 | 140 | 85 | 120 | 80 |
| 100 | 20 | 180 | 140 | 140 | 80 | 115 | 60 | 200 | 160 | 130 | 85 | 120 | 65 |
| 100 | 40 | 200 | 130 | 145 | 80 | 125 | 60 | 200 | 150 | 140 | 80 | 120 | 65 |
| 150 | 10 | 190 | 160 | 150 | 85 | 125 | 65 | 190 | 165 | 150 | 95 | 130 | 70 |
| 150 | 20 | 200 | 160 | 145 | 90 | 120 | 65 | 200 | 180 | 140 | 90 | 125 | 70 |
| 150 | 40 | 180 | 140 | 140 | 80 | 130 | 85 | 190 | 160 | 145 | 85 | 130 | 65 |
| 250 | 10 | 180 | 160 | 135 | 85 | 120 | 70 | 180 | 160 | 140 | 90 | 130 | 70 |
| 250 | 20 | 170 | 150 | 135 | 95 | 110 | 70 | 160 | 160 | 135 | 95 | 120 | 70 |
| 250 | 40 | 160 | 160 | 130 | 95 | 110 | 70 | 170 | 170 | 125 | 95 | 115 | 80 |
| 350 | 10 | 180 | 190 | 135 | 100 | 125 | 80 | 175 | 200 | 135 | 110 | 125 | 85 |
| 350 | 20 | 180 | 170 | 130 | 100 | 115 | 75 | 175 | 180 | 140 | 110 | 125 | 85 |

TABLE A-18. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D60T NUMBER 60-1

| Circuit Configuration | | Transistor 60-1 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 40 | 10 | 400 | 1.8 | 400 | 1.4 | 380 | 1.0 | 220 | 0.43 | 210 | 0.36 | 220 | 0.36 |
| 40 | 20 | 400 | 2.2 | 380 | 1.6 | 320 | 1.2 | 160 | 0.48 | 160 | 0.48 | 160 | 0.5 |
| 40 | 40 | 260 | 2.25 | 280 | 1.5 | 230 | 1.2 | 190 | 0.78 | 180 | 0.7 | 170 | 0.68 |
| 60 | 10 | 400 | 2.2 | 420 | 1.6 | 420 | 1.2 | 200 | 0.44 | 190 | 0.46 | 240 | 0.64 |
| 60 | 20 | 380 | 2.4 | 380 | 1.5 | 320 | 1.2 | 160 | 0.62 | 160 | 0.62 | 180 | 0.65 |
| 60 | 40 | 200 | 2.8 | 200 | 1.5 | 190 | 1.1 | 160 | 0.95 | 160 | 0.87 | 160 | 0.8 |
| 100 | 10 | - | 2.6 | 360 | 2.1 | 380 | 1.8 | - | 0.6 | 200 | 0.6 | 210 | 0.65 |
| 100 | 20 | - | 2.8 | 260 | 2.2 | 260 | 1.6 | - | 0.86 | 180 | 0.88 | 190 | 1.04 |
| 100 | 40 | - | 3.1 | 160 | 2.0 | 110 | 1.8 | - | 1.6 | 160 | 1.43 | 120 | 1.4 |
| 140 | 10 | - | 2.9 | 220 | 2.4 | - | - | - | 0.77 | 210 | 0.87 | - | - |
| 140 | 20 | - | 3.0 | 120 | 2.3 | - | - | - | 1.2 | 120 | 1.4 | - | - |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 40 | 4:1 | 8:1 | 12:1 |
| 60 | 4:1 | 8:1 | 12:1 |
| 100 | 3:1 | 5:1 | 7:1 |
| 140 | 3:1 | 5:1 | 7:1 |

TABLE A-19. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D60T NUMBER 60-2

| Circuit Configuration | | Transistor 60-2 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 40 | 10 | 400 | 1.6 | 340 | 1.15 | 350 | 0.9 | 220 | 0.42 | 220 | 0.38 | 240 | 0.36 |
| 40 | 20 | 340 | 1.85 | 320 | 1.4 | 400 | 1.0 | 180 | 0.42 | 200 | 0.45 | 160 | 0.45 |
| 40 | 40 | 280 | 2.0 | 280 | 1.48 | 300 | 1.2 | 160 | 0.72 | 150 | 0.64 | 140 | 0.62 |
| 60 | 10 | 380 | 1.7 | 360 | 1.3 | 360 | 0.95 | 180 | 0.42 | 180 | 0.42 | 220 | 0.54 |
| 60 | 20 | 310 | 2.0 | 440 | 1.4 | 340 | 1.0 | 180 | 0.57 | 200 | 0.59 | 200 | 0.72 |
| 60 | 40 | 220 | 2.1 | 230 | 1.35 | 200 | 1.05 | 150 | 0.86 | 150 | 0.78 | 150 | 0.75 |
| 100 | 10 | - | 2.0 | 360 | 1.75 | 360 | 1.6 | - | 0.59 | 160 | 0.52 | 170 | 0.59 |
| 100 | 20 | - | 2.4 | 250 | 1.95 | 280 | 1.6 | - | 0.82 | 170 | 0.8 | 180 | 0.94 |
| 100 | 40 | - | 2.5 | 160 | 1.85 | 160 | 1.55 | - | 1.35 | 180 | 1.25 | 160 | 1.3 |
| 140 | 10 | - | 2.25 | 330 | 1.9 | - | - | - | 0.69 | 170 | 0.74 | - | - |
| 140 | 20 | - | 2.5 | 120 | 1.9 | - | - | - | 1.1 | 100 | 1.3 | - | - |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 40 | 4:1 | 8:1 | 12:1 |
| 60 | 4:1 | 8:1 | 12:1 |
| 100 | 3:1 | 5:1 | 7:1 |
| 140 | 3:1 | 5:1 | 7:1 |

TABLE A-20. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D60T NUMBER 60-3

| Circuit Configuration | | Transistor 60-3 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 40 | 10 | 380 | 1.9 | 370 | 1.5 | 360 | 1.2 | 200 | 0.48 | 200 | 0.42 | 200 | 0.38 |
| 40 | 20 | 350 | 2.35 | 340 | 1.7 | 330 | 1.35 | 160 | 0.62 | 160 | 0.58 | 170 | 0.62 |
| 40 | 40 | 280 | 2.5 | 280 | 1.8 | 250 | 1.45 | 180 | 1.0 | 150 | 0.86 | 160 | 0.84 |
| 60 | 10 | 360 | 2.2 | 370 | 1.6 | 360 | 1.35 | 160 | 0.52 | 170 | 0.52 | 200 | 0.68 |
| 60 | 20 | 330 | 2.4 | 320 | 1.7 | 300 | 1.3 | 200 | 0.78 | 200 | 0.82 | 240 | 0.92 |
| 60 | 40 | 200 | 2.6 | 220 | 1.6 | 200 | 1.25 | 170 | 1.12 | 160 | 1.02 | 150 | 0.93 |
| 100 | 10 | - | 2.65 | 360 | 2.2 | 360 | 1.9 | - | 0.8 | 190 | 0.74 | 200 | 0.82 |
| 100 | 20 | - | 2.9 | 250 | 2.4 | 250 | 1.9 | - | 1.06 | 160 | 1.01 | 190 | 1.12 |
| 100 | 40 | - | 3.0 | 80 | 2.2 | 80 | 2.1 | - | 1.8 | 120 | 1.6 | 120 | 1.65 |
| 140 | 10 | - | 2.8 | 320 | 2.5 | - | - | - | 0.92 | 180 | 1.0 | - | - |
| 140 | 20 | - | 3.0 | - | 2.5 | - | - | - | 1.35 | 80 | 1.5 | - | - |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 40 | 4:1 | 8:1 | 12:1 |
| 60 | 4:1 | 8:1 | 12:1 |
| 100 | 3:1 | 5:1 | 7:1 |
| 140 | 3:1 | 5:1 | 7:1 |

TABLE A-21. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D60T NUMBER 60-4

| Circuit Configuration | | Transistor 60-4 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 40 | 10 | 520 | 2.3 | 450 | 1.5 | 400 | 1.2 | 190 | 0.48 | 180 | 0.5 | 200 | 0.46 |
| 40 | 20 | 500 | 2.6 | 430 | 2.1 | 380 | 1.3 | 230 | 0.82 | 220 | 0.75 | 220 | 0.74 |
| 40 | 40 | 250 | 2.9 | 260 | 2.1 | 240 | 1.4 | 160 | 1.12 | 160 | 0.96 | 160 | 0.92 |
| 60 | 10 | 520 | 2.5 | 460 | 2.0 | 400 | 1.3 | 230 | 0.68 | 210 | 0.68 | 240 | 0.75 |
| 60 | 20 | 410 | 2.9 | 420 | 2.1 | 360 | 1.3 | 260 | 0.96 | 260 | 0.98 | 240 | 0.97 |
| 60 | 40 | 160 | 3.0 | 160 | 2.1 | 160 | 1.25 | 150 | 1.24 | 140 | 1.14 | 130 | 1.0 |
| 100 | 10 | - | 3.0 | 480 | 2.7 | 460 | 2.3 | - | 0.92 | 240 | 0.92 | 260 | 0.98 |
| 100 | 20 | - | 3.6 | 170 | 2.9 | 200 | 2.4 | - | 1.2 | 120 | 1.2 | 140 | 1.3 |
| 100 | 40 | - | 3.8 | - | 2.9 | 120 | 2.7 | - | 1.95 | 120 | 1.7 | 100 | 1.75 |
| 140 | 10 | - | 3.4 | 320 | 3.1 | - | - | - | 1.06 | 210 | 1.25 | - | - |
| 140 | 20 | - | 3.8 | - | 3.5 | - | - | - | 1.6 | - | 1.7 | - | - |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 40 | 4:1 | 8:1 | 12:1 |
| 60 | 4:1 | 8:1 | 12:1 |
| 100 | 3:1 | 5:1 | 7:1 |
| 140 | 3:1 | 5:1 | 7:1 |

TABLE A-22. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D60T NUMBER 60-5

| Circuit Configuration | | Transistor 60-5 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 40 | 10 | 380 | 1.4 | 360 | 1.1 | 330 | 0.8 | 230 | 0.4 | 230 | 0.4 | 240 | 0.36 |
| 40 | 20 | 400 | 1.75 | 360 | 1.25 | 300 | 0.95 | 160 | 0.5 | 170 | 0.46 | 170 | 0.47 |
| 40 | 40 | 280 | 1.9 | 260 | 1.4 | 230 | 1.1 | 150 | 0.77 | 140 | 0.7 | 130 | 0.66 |
| 60 | 10 | 360 | 1.6 | 370 | 1.15 | 340 | 0.9 | 200 | 0.42 | 200 | 0.44 | 200 | 0.54 |
| 60 | 20 | 360 | 1.85 | 330 | 1.3 | 280 | 1.0 | 160 | 0.62 | 180 | 0.63 | 200 | 0.73 |
| 60 | 40 | 210 | 1.95 | 220 | 1.3 | 1.0 | 1.0 | 160 | 0.88 | 150 | 0.8 | 140 | 0.77 |
| 100 | 10 | - | 1.9 | 380 | 1.6 | 380 | 1.4 | - | 0.58 | 160 | 0.58 | 180 | 0.62 |
| 100 | 20 | - | 2.2 | 250 | 1.7 | 240 | 1.4 | - | 0.82 | 160 | 0.8 | 190 | 0.95 |
| 100 | 40 | - | 2.35 | 150 | 1.75 | 170 | 1.45 | - | 1.38 | 180 | 1.3 | 150 | 1.25 |
| 140 | 10 | - | 2.05 | 360 | 1.75 | - | - | - | 0.7 | 200 | 0.77 | - | - |
| 140 | 20 | - | 2.2 | 120 | 1.8 | - | - | - | 1.12 | 130 | 1.3 | | |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 40 | 4:1 | 8:1 | 12:1 |
| 60 | 4:1 | 8:1 | 12:1 |
| 100 | 3:1 | 5:1 | 7:1 |
| 140 | 3:1 | 5:1 | 7:1 |

TABLE A-23. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D7ST NUMBER 12

| Circuit Configuration | | Transistor 12 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 100 | 10 | 500 | 7.8 | 650 | 4.6 | 500 | 2.9 | 230 | 1.6 | 240 | 1.5 | 280 | 1.8 |
| 100 | 20 | 300 | 7.0 | 380 | 4.3 | 300 | 3.1 | 370 | 4.0 | 240 | 2.1 | 230 | 2.1 |
| 100 | 40 | - | 6.1 | 210 | 4.2 | 200 | 3.3 | 230 | 4.8 | 220 | 3.4 | 200 | 2.9 |
| 150 | 10 | 400 | 7.5 | 550 | 4.3 | 450 | 2.7 | 220 | 1.6 | 250 | 1.7 | 320 | 2.0 |
| 150 | 20 | 260 | 7.4 | 300 | 4.1 | 230 | 3.0 | 330 | 4.2 | 250 | 2.8 | 230 | 2.4 |
| 150 | 40 | - | 6.0 | 280 | 3.9 | 240 | 3.3 | - | 4.9 | 280 | 3.5 | 230 | 3.1 |
| 250 | 10 | - | 8.5 | 320 | 5.9 | 340 | 4.5 | 260 | 2.6 | 230 | 2.2 | 250 | 2.5 |
| 250 | 20 | - | 8.7 | 270 | 5.5 | 330 | 4.5 | - | 5.6 | 360 | 4.0 | 350 | 3.7 |
| 250 | 40 | - | 8.0 | - | 5.4 | 150 | 4.4 | - | 6.7 | - | 4.8 | 150 | 4.1 |
| 350 | 10 | - | 8.6 | 370 | 6.1 | 370 | 5.3 | 340 | 2.8 | 350 | 3.1 | 370 | 3.6 |
| 350 | 20 | - | 7.8 | - | 6.7 | 240 | 6.5 | - | 5.3 | - | 4.9 | 180 | 4.9 |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 100 | 4:1 | 8:1 | 12:1 |
| 150 | 4:1 | 8:1 | 12:1 |
| 250 | 3:1 | 5:1 | 7:1 |
| 350 | 3:1 | 5:1 | 7:1 |

TABLE A-24. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D7ST NUMBER 15

| Circuit Configuration | | Transistor 15 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 100 | 10 | 550 | 4.5 | 460 | 3.3 | 350 | 2.4 | 220 | 2.1 | 220 | 1.8 | 250 | 1.9 |
| 100 | 20 | 310 | 4.6 | 320 | 3.3 | 250 | 2.5 | 300 | 3.0 | 220 | 2.3 | 210 | 2.3 |
| 100 | 40 | 220 | 4.6 | 210 | 3.6 | 210 | 3.2 | 220 | 3.9 | 200 | 3.1 | 200 | 2.8 |
| 150 | 10 | 450 | 4.8 | 450 | 3.3 | 330 | 2.5 | 230 | 2.0 | 230 | 2.3 | 250 | 2.3 |
| 150 | 20 | 270 | 4.8 | 260 | 3.5 | 220 | 2.7 | 270 | 3.2 | 220 | 2.8 | 210 | 2.7 |
| 150 | 40 | - | 4.7 | 230 | 3.7 | 220 | 3.2 | - | 4.2 | 230 | 3.4 | 210 | 3.0 |
| 250 | 10 | - | 5.2 | 320 | 4.2 | 280 | 3.6 | 230 | 2.3 | 220 | 2.4 | 250 | 2.7 |
| 250 | 20 | - | 5.7 | 250 | 4.5 | 280 | 3.9 | 400 | 3.9 | 360 | 3.5 | 310 | 3.4 |
| 250 | 40 | - | 5.4 | - | 4.4 | 240 | 3.9 | - | 5.2 | - | 4.3 | 240 | 3.9 |
| 350 | 10 | - | 5.5 | 380 | 4.6 | 320 | 4.1 | 320 | 2.9 | 330 | 3.2 | 300 | 3.5 |
| 350 | 20 | - | 5.9 | - | 4.9 | - | 4.5 | - | 5.0 | - | 4.7 | - | 4.4 |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 100 | 4 1 | 8:1 | 12:1 |
| 150 | 4:1 | 8:1 | 12:1 |
| 250 | 3:1 | 5:1 | 7:1 |
| 350 | 3:1 | 5:1 | 7:1 |

TABLE A-25. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D7ST NUMBER 36

| Circuit Configuration | | Transistor 36 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 100 | 10 | 500 | 7.3 | 600 | 5.4 | 650 | 4.4 | 300 | 1.9 | 260 | 1.7 | 270 | 1.7 |
| 100 | 20 | 280 | 7.4 | 360 | 5.6 | 400 | 4.8 | 400 | 4.4 | 380 | 3.6 | 360 | 3.3 |
| 100 | 40 | - | 6.0 | 220 | 4.4 | 220 | 3.7 | 240 | 4.9 | 230 | 3.6 | 230 | 3.1 |
| 150 | 10 | 440 | 6.8 | 500 | 5.0 | 500 | 3.7 | 260 | 1.9 | 290 | 1.9 | 280 | 1.8 |
| 150 | 20 | - | 7.2 | 310 | 5.2 | 280 | 4.2 | 320 | 4.7 | 270 | 3.5 | 250 | 2.7 |
| 150 | 40 | - | 6.1 | 300 | 4.1 | 270 | 3.5 | - | 5.1 | 280 | 3.7 | 260 | 3.2 |
| 250 | 10 | - | 7.1 | 250 | 5.9 | 360 | 4.8 | 250 | 2.3 | 230 | 2.4 | 230 | 2.4 |
| 250 | 20 | - | 6.9 | - | 6.2 | 300 | 5.0 | - | 5.4 | 500 | 4.0 | 400 | 3.5 |
| 250 | 40 | - | 7.8 | - | 5.6 | - | 4.6 | - | 6.5 | - | 4.7 | - | 4.3 |
| 350 | 10 | - | 7.0 | 400 | 6.0 | 330 | 5.2 | 300 | 2.9 | 300 | 2.9 | 340 | 3.2 |
| 350 | 20 | - | 8.2 | - | 6.6 | - | 5.8 | - | 5.3 | - | 4.6 | 180 | 4.6 |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 100 | 4:1 | 8:1 | 12:1 |
| 150 | 4:1 | 8:1 | 12:1 |
| 250 | 3:1 | 5:1 | 7:1 |
| 350 | 3:1 | 5:1 | 7:1 |

TABLE A-26. FALL TIME AND STORAGE TIME VERSUS TURNS-RATIO FOR D7ST NUMBER 37

| Circuit Configuration | | Transistor 37 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Saturated | | | | | | Unsaturated | | | | | |
| Turns Ratio | | A* | | B* | | C* | | A* | | B* | | C* | |
| Peak Ic, Amps | Resonant Frequency fr, kHz | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | tf ns | ts µs | ts ns | ts µs |
| 100 | 10 | 500 | 6.7 | 600 | 5.1 | 620 | 4.2 | 300 | 2.2 | 280 | 1.7 | 260 | 1.7 |
| 100 | 20 | 320 | 7.0 | 360 | 5.3 | 370 | 4.5 | 380 | 4.4 | 330 | 3.3 | [illegible]0 | 3.1 |
| 100 | 40 | - | 5.8 | 220 | 4.2 | 220 | 3.5 | 230 | 4.9 | 220 | 3.4 | 210 | 3.0 |
| 150 | 10 | 450 | 6.5 | 500 | 4.8 | 500 | 3.5 | 250 | 1.7 | 270 | 1.8 | 270 | 1.8 |
| 150 | 20 | - | 6.8 | 300 | 5.0 | 300 | 4.1 | 340 | 4.3 | 250 | 3.2 | 220 | 2.6 |
| 150 | 40 | - | 6.1 | 280 | 4.1 | 220 | 3.5 | - | 4.8 | 280 | 3.6 | 240 | 3.1 |
| 250 | 10 | - | 6.8 | 300 | 5.7 | 300 | 4.7 | 220 | 2.2 | 220 | 2.3 | 210 | 2.3 |
| 250 | 20 | - | 7.3 | - | 6.0 | 350 | 5.0 | - | 4.7 | 420 | 3.6 | 360 | 3.4 |
| 250 | 40 | - | 7.4 | - | 5.4 | - | 4.5 | - | 6.7 | - | 4.9 | - | 4.3 |
| 350 | 10 | - | 6.6 | 330 | 5.6 | 350 | 5.0 | 300 | 3.0 | 300 | 2.9 | 360 | 3.3 |
| 350 | 20 | - | 7.2 | - | 6.3 | 230 | 6.4 | - | 5.5 | - | 5.4 | 280 | 5.0 |

*

| Peak Ic | A | B | C |
|---|---|---|---|
| 100 | 4:1 | 8:1 | 12:1 |
| 150 | 4:1 | 8:1 | 12:1 |
| 250 | 3:1 | 5:1 | 7:1 |
| 350 | 3:1 | 5:1 | 7:1 |