8103-26

(NASA-CR-167504) MODERATE TEMPERATURE DETECTOR DEVELOPMENT Final Technical Report, Sep. 1979 - May 1980 (Honeywell Electro-Optics Center) 45 p HC A03/MF A01 CSCL 20F G3/74

N82-17998

Unclas
08821

MODERATE TEMPERATURE DETECTOR DEVELOPMENT

by

J.W.Marcinkus, R.J. Briggs and A.K. Sood

FINAL TECHNICAL REPORT

Contract NAS9-15250

National Aeronautics and Space Administration

Lyndon B. Johnson Space Center

Houston, Texas 77058

DECEMBER 1981

8103-26

MODERATE TEMPERATURE DETECTOR DEVELOPMENT

by

J.W. Marciniec, R.J. Briggs, and A.K. Sood

Final Technical Report

Contract NAS9-15250

National Aeronautics and Space Administration
Lyndon B. Johnson Space Center
Houston, Texas 77058

December, 1981

FOREWORD AND ACKNOWLEDGEMENTS

This is the final technical report for Contract NAS9-15250, Modification 5S, entitled "Moderate Temperature Detector Development, Phase IV." The work was performed at the Honeywell Electro-Optics Operations in Lexington, Massachusetts during the period from September, 1979 through May, 1980.

The NASA Technical Monitor for this program was Mr. J.R. Woodfill.

The principal investigator for Honeywell was Mr. J.W. Marciniec and the program manager was Dr. A.K. Sood. Device processing was carried out by Jane Hamel and device testing was done by Robert Minich.

The authors acknowledge the technical contributions of Mr. S.P. Tobin and Dr. P.H. Zimmermann.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

SECTION 1
INTRODUCTION

1.1 BACKGROUND

Detection of infrared radiation in the 8 to 12-micrometer spectral band has found widespread application during the past two decades for a variety of space, military and industrial applications. The atmospheric transmission window at 8 to 12 micrometers combined with the occurrence at approximately 10 micrometers of the peak in the spectral power distribution for emission from a 300 K blackbody radiator, have made this band important for collection of thermal information about the earth from a satellite.

For satellite-based applications, the operating temperature of the detector is of critical importance. For multi-spectral sensors, the visible channels may be operated at ambient temperature and the channels in the 1.5 to 2.5-micrometer spectral region may be operated at 193-250 K. However, detectors for the 8 to 14-micrometer channel require cooling to 60-90 K. On the one hand, as the operating temperature is increased, the detector sensitivity decreases rapidly. On the other hand, severe size, power and weight constraints for space operation dictate as high an operating temperature as possible. Thus, development of infrared detectors which are capable of operating at elevated temperatures with adequate sensitivity has substantial payoff in terms of sensor weight, cost, and lifetime.

1.2 SUMMARY OF THE PREVIOUS PROGRAM

An earlier theoretical and analytical program was carried out to define the most promising technical approach for development of 8 to 12-micrometer infrared quantum detectors operating at elevated temperatures. In achieving this objective, three tasks were undertaken:

- Determine the theoretical limit to performance of both thermal and quantum detectors for 8 to 12-micrometer infrared detection.

- Identify candidate detector materials and determine material parameters.

- Determine the present status of both quantum and thermal detectors, isolate the parameters limiting performance, and assess the feasibility of achieving performance at the theoretical limit.

Details of this study have been presented in the final report for the NASA/JSC Phase I Program.[1] The fundamental conclusion reached in the analysis of signal and noise in quantum detectors was that the ultimate limit to detectivity in a quantum detector depended only on the wavelength, temperature, and material index of refraction n. This ultimate limit could be met only if radiative, rather than Auger, recombination was the dominant recombination process. Thus, in evaluating semiconductor material classes for fundamental potential to achieve the theoretical limit to D^*, the following criteria should be used:

- Auger recombination should be weak or negligible relative to radiative recombination.

- If above requirement is satisfied, then the material should have the lowest possible index of refraction.

The best suited material based on these criteria is $Hg_{0.8}Cd_{0.2}Te$. For $Hg_{0.8}Cd_{0.2}Te$ Auger recombination is dominant in nondegenerate n-type and lightly doped p-type. In heavily doped p-type radiative recombination is dominant up to 190 K. Thus, p-type (Hg,Cd)Te appears to be the best candidate on a theoretical limit to D^* for elevated temperature operation.

It was also determined that the best device design for (Hg,Cd)Te for elevated temperature operation is n^+ on p. The factors limiting the R_0A product are the p-side lifetime τ_e and L_e (minority carrier diffusion

length) for a given base carrier concentration. Further improvement in R_0A could be realized by using the "electrically reflecting backside contact" which could be achieved by fabricating n^+-p-p^+ structures.

The n^+-p-p^+ configuration consists of a thin (less than 0.5 μm) ion implanted n^+-region on a p-layer which has a thickness on the order of or less than a minority-carrier diffusion length. On the opposite side of this p-layer is a thin ion implanted p^+-region which forms a p^+-p "high-low" junction. Nearly all absorption of the incident infrared radiation occurs within the p-layer. For wavelengths appreciably less than the cutoff wavelength, the absorption coefficient is above 1000 cm^{-1}. Hence, the p-region in n^+-p structure need not be thicker than roughly 10 micrometers to absorb most of the radiation, as any additional thickness of the base region would contribute to noise current. So to maximize the S/N ratio for a detector, the p-region should be as thin as possible while still thick enough to absorb most of the radiation. Of course, if it is then thinner than a diffusion length, which it usually will be, the back contact is within "range" of the junction as a possible source of carriers to be extracted by the junction.

A p^+-p (or n^+-n) contact can be thought of as an electrical reflector of minority carriers. This is because there is a potential barrier to the flow of minority carriers at such a contact, and minority carriers hitting the barrier are "reflected". In contrast, a purely metallic contact, at which the quasi-fermi levels in the semiconductor come together, acts as a sink for minority carriers.

1.3 GOAL AND OBJECTIVE OF THIS PROGRAM

The objective of this phase of the program was to refine the basic technology developed in Phase II and III of this program for application in fabricating n^+-p-p^+ junction photodiodes. Since the operating temperature ranges between 100-145 K, and the photodiodes are diffusion current limited at these temperatures, the bulk of the task was to develop techniques needed for fabricating a p-p^+ junction, or any other approach which is capable of producing low surface recombination velocities at the back surface.

SECTION 2
THEORETICAL CONSIDERATIONS FOR P-SIDE BACKSIDE REFLECTING CONTACT

2.1 PHOTODIODE PERFORMANCE CHARACTERIZATION

The performance of a detector is usually characterized by its detectivity D^*_λ, which is the signal to noise ratio normalized to unit area and unit incident power. It can be expressed by

$$D^*_\lambda = \frac{R_i \sqrt{A}}{i_{EQ}} \tag{1}$$

where R_i is the current responsivity, $A = A_{OPT}$ is the optical area, and i_{EQ} is the equivalent noise current density. The responsivity is determined by the quantum efficiency η and wavelength λ, and is given by

$$R_i = \frac{\eta q \lambda}{hc} \tag{2}$$

where h,c, and q have their standard values.

The noise sources contributing to the equivalent noise current density are Johnson noise due to the junction resistance R_o, background induced noise current, and 1/f noise i_f, and the noise associated with the buffer amplifier. These give

$$i^2_{EQ} = 2\eta q^2 \phi_B A + \frac{4kT}{R_o} + i^2_{1/f} + i^2_n \text{ (amp)} \tag{3}$$

where ϕ_B is the background flux and k is Boltzmann's constant.

2.2 PHOTODIODE DIFFUSION AND G-R CURRENTS

Currents resulting from several mechanisms may limit n^+ on p photodiode performance for any given temperature and cutoff wavelength. Although the forward and reverse currents cancel for the mechanism at zero bias, the associated noise does not.[2] At higher temperatures performance may be limited either by diffusion of thermally generated current, bulk space charge region G-R current, or surface G-R current. This section demonstrates how to distinguish the three currents using their characteristic temperature and voltage dependences.

At higher temperatures the dominant current arises from diffusion of thermally generated electrons from the p-side of the junction and thermally generated holes from the n-side to the junction. This so-called diffusion current is proportional to the number of minority carriers on each side of the junction. Since the volume from which diffusion current may arise is much larger on the p-side than on the n-side and the number of minority carriers is much larger, the diffusion currents for n^+ on p photodiodes are almost all from the p-side. The diffusion current I_D and zero bias impedance R_o can be expressed in the planar approximation as:[3]

$$I_D = I_{SAT}(e^{qV/kT} - 1) \tag{4}$$

$$I_{SAT} = A_J \frac{n_i^2}{N_A} \frac{kT\mu_e}{L_e} \tag{5}$$

$$R_o\,(diff) = \frac{kT}{qI_{SAT}} \tag{6}$$

where A_J = junction area

n_i = intrinsic carrier concentration

N_A = acceptor concentration

L_e = minority carrier electron diffusion length

μ_e = minority carrier electron mobility

τ_e = minority carrier lifetime

A second current mechanism results from thermal generation and recombination (G-R) of electron-hole pairs in the region of the junction between the n and p sides which is depleted of both types of minority carriers. This so-called space charge G-R current is proportional to the intrinsic carrier concentration n_i. This G-R current and associated limitation to R_o are given by:[4]

$$I_{GR} = I_{OGR} \frac{2 \sinh (qV/2kT)}{\sqrt{1 - V/V_{bi}}} f(b) \tag{7}$$

$$R_o(G\text{-}R) = \frac{kT}{qI_{OGR} f(b)} \tag{8}$$

where

$$b = e^{-qV/2kT} \cosh \varepsilon_t \tag{9}$$

$$f(b) = \int_0^\infty \frac{du}{1 + 2bu + u^2} \tag{10}$$

Also

$$I_{OGR} = \frac{n_i W_o A_J}{\tau_o} \frac{kT}{V_{bi}} \tag{11}$$

or

$$I_{OGR} = n_i S_o W_o P_J \frac{kT}{V_{bi}} \tag{12}$$

for depletion layer or surface G-R, respectively. Here V_{bi} is the depletion built in voltage, W_o is the depletion width at zero bias, $\tau_o = \sqrt{\tau_{no} \tau_{po}}$ is the effective depletion layer lifetime, P_J is the junction perimeter, and S_o is the surface recombination velocity inside the depletion region where it intersects the semiconductor surface. For the most effective G-R center, at zero bias $b = \cosh \varepsilon_t = 1$ and $f(b) = 1$.

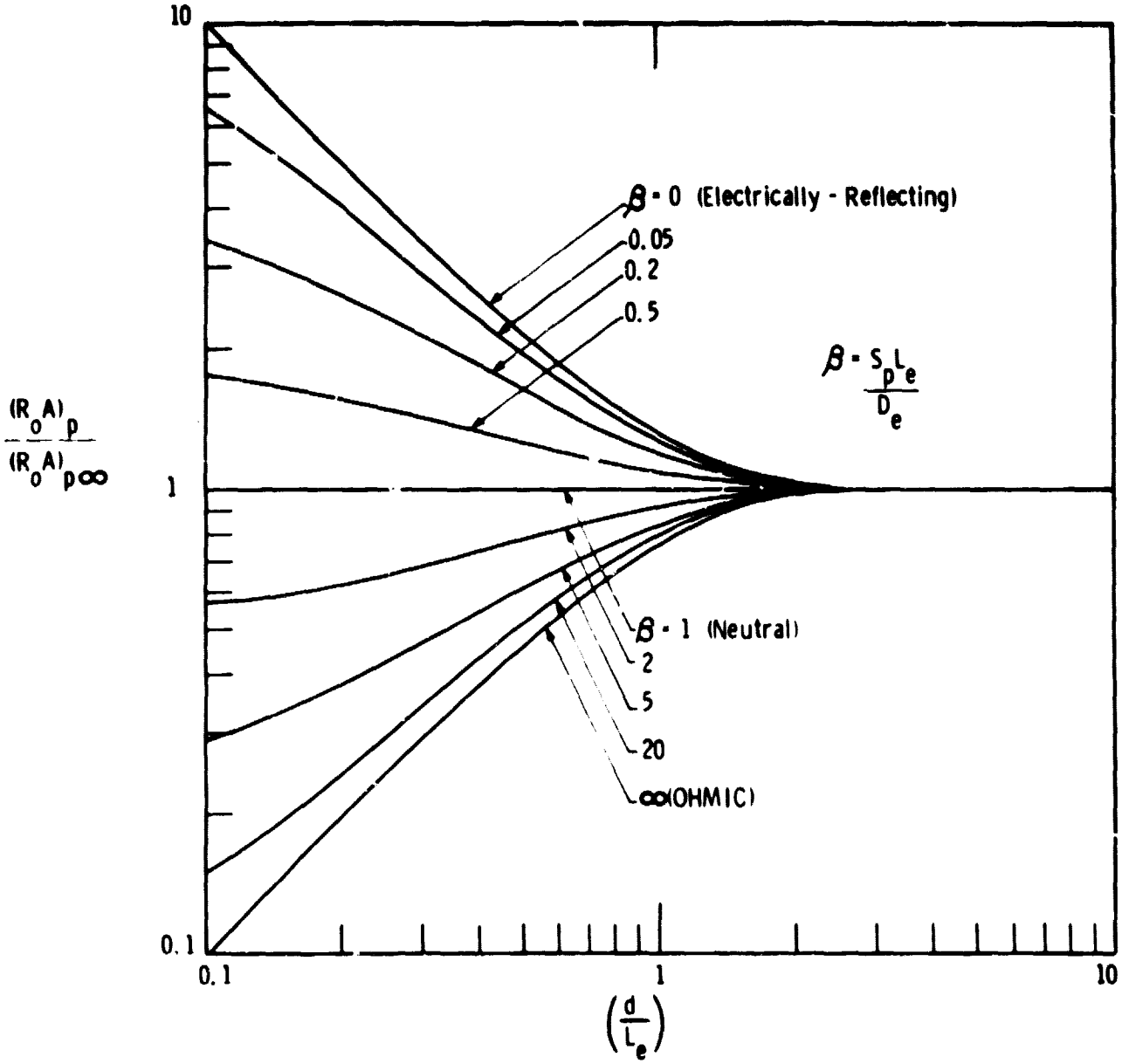

Figure 1. The Effect on R_oA for Various Types of Boundaries Within a Diffusion Length of the Space Charge Region as Described by Equation 3

The temperature dependences of both current mechanisms are almost entirely due to the intrinsic carrier concentration. Since R_0A (diff) α n_i^{-2} and P_0A (G-R) α n_i^{-1}, performance should be limited by diffusion currents at higher temperature and at somewhat lower temperatures by generation-recombination currents.

For thin diodes having p-side thickness and about the same order of magnitude as L_e, Equations (5) and (6) give:[5,6]

$$R_0A\ (\text{thin}) = \frac{N_A}{qn_i^2} \frac{L_e}{\mu_e} \frac{1 + \beta \tanh (d/Le)}{\beta + \tanh (d/Le)} \qquad (13)$$

where $\beta = S_p \tau_e / L_e$ for p-side surface recombination velocity S_p.

Notice that if $\beta \ll 1$ the last term reduces to coth (d/L_e), if $\beta \gg 1$ the last term reduces to tanh (d/L_e), and if $\beta = 1$ the last term is unity. The consequences of this last term are illustrated in Figure 1 for several values of β. As can be seen in the figure improvements in R_0A by device thinning require $\beta \ll 1$; if β is greater than one, in fact, reduction in R_0A will result by device thinning. If the desired condition of $\beta = 0$ is obtained, then Equation 13 is given by the form usually presented:

$$R_0A\ (\text{thin}) = \frac{N_A}{qn_i^2} \frac{L_e}{\mu_e} \coth (d/L_e) \qquad (14)$$

which again reduces to the thick diode equation for $d \gg L_e$.

2.3 BACKSIDE FORMATION APPROACHES

Three approaches of forming the so called p-side reflecting boundary ($\beta \ll 1$ in Figure 1) have been considered:

- surface depletion by anodization (n^+-p-p^- structure)
- surface accumulation by implantation (n^+-p-p^+ structure)
- bandgap increase (n^+-p-p heterojunction)

2.3.1 Anodization

Anodization was reported by Beck and Sanborn[7] to strongly accumulate the surface of n-type, x = 0.3 and x = 0.4 $Hg_{1-x}Cd_xTe$ and to invert the surface of p-type $Hg_{0.7}Cd_{0.3}Te$ as determined from MIS C-V characteristics. Similar results were reported from $Hg_{0.8}Cd_{0.2}Te$ on Army Contract DAAG46-74-C-0142. When applied onto the back side the inverted p surface will result in a space charge region under the surface, similar to that at the p^+n junction. This space charge region will be depleted of minority carriers and should act as a boundary for the diffusion. The associated recombination velocity S_p for the interface should be low because the surface preparation is a low temperature equilibrium process and because the interface has been removed somewhat from the surface. The feasibility of obtaining the thin diode diffusion advantage using this technique of anodization should be determined before pursuing any of the other approaches.

2.3.2 Phosphorus Implantation

Use of phosphorus implantation to form the p^+-p hi-lo junction and boron implantation to form the n^+p junction has been reported during earlier phases of this program. Data for R_0 at 145 K for linear arrays of the n^+-p-p^+ photodiodes with tapered variation in thickness of the p-region were reported to fit

$$R_0A = (R_0A)_\infty \coth (d/L_e) \qquad (15)$$

for L_e = 25 μm and $(R_0A)_\infty$ chosen for each array to fit the data. The values of $(R_0A)_\infty$ are all lower than the best values reported for n^+p photodiodes formed on thick p-regions.

2.3.3 Graded Bandgap Concept

The graded bandgap transition between a p-type $Hg_{0.7}Cd_{0.3}Te$ LPE layer and its CdTe substrate was used to form the p-side reflecting boundary by

Lanir et al.[8] for the case of boron implanted n^+ on p photodiodes. An EBIC line scan perpendicular to the junction yielded a minority carrier diffusion length of 60 μm and was interpreted to have a value of β for Equation (3) of about 0.05 at 80 K and 210 K. Similar results would be expected if the bandgap of bulk material were increased somewhat near the surface. Preliminary low temperature Cd interdiffusion experiments to increase the bandgap near the surface for bulk $Hg_{0.8}Cd_{0.2}Te$ are being attempted on another program.

SECTION 3
EXPERIMENTAL

3.1 FABRICATION PROCEDURES FOR DEVICES WITH BACKSIDE REFLECTING CONTACTS

As indicated in the preceding theoretical discussion, if a backside reflecting contact is incorporated into a device, creating an n^+-p-p^+ structure, and the bulk p-region is thinned to less than a diffusion length L_e, the diffusion current will be decreased. This will then appear as an increase in the zero bias impedance (R_0) of the device. This effect is only applicable in the diffusion limited regime.

The backside treatment chosen for use on this program was the anodic oxide, for reasons indicated in Section 2. Prior to anodic oxide growth on the (111)-oriented (Hg,Cd)Te wafer, an etch was performed to determine the A (metal) and B (Te) faces of the wafer. All diodes were formed by boron ion implantation on the A face. This has been seen to yield devices with lower leakage characteristics than those formed on the B face.[9]

After the revealing etch, the B face was polished and etched to remove any damage from previous processing steps. Following a thorough cleaning procedure, the sample was anodized using a constant current source in a 10% 0.1 M KOH in ethylene glycol anodizing solution. The final oxide thickness was approximately 900 Å. In order to protect the oxide from damage during further processing steps, the oxide was coated with a ZnS layer approximately 3000 Å thick.

In order to investigate the effect of bulk p-region thickness on the diode R_0, devices of varying thickness were fabricated from each wafer processed. This was accomplished by cutting the wafer into four or five pieces, and epoxying each piece onto a separate Si carrier substrate. The samples were then polished and etched to different p-region thicknesses. Following the polishing procedure, the samples were all etched in Br:CH_3OH to remove the

polishing damage. The front surfaces were passivated with sputtered ZnS, and then implanted with boron ions at 100 keV to a level of 1×10^{13} ions/cm^2, through a photoresist mask. A post implantation damage anneal was carried out at 150°C for 2 hours. Following this, the top p-side contact of evaporated gold was applied and an additional insulating layer of ZnS was sputtered. Contact holes were then etched and indium metallization evaporated for contact to the n-side and gold wire bonding. A schematic of this process is shown in Figure 2. An important part of this procedure is that all sections of the wafer received critical process steps (i.e., ZnS passivation, ion implantation, post-implantation anneal) together. This helped to ensure no variations from sample to sample due to process-induced effects. Thus, the result of different bulk p-region thicknesses could be better identified.

The array configuration for the diodes fabricated on this program is shown in Figure 3. This configuration allowed many tests to be performed to evaluate the device properties such as the (Hg,Cd)Te/ZnS interface properties and minority carrier diffusion length. To evaluate the (Hg,Cd)Te/ZnS surface properties, four metal-insulator-semiconductor (MIS) structures were formed on each array. These allowed C-V measurements to be made which provided information on the quality of the interface. The data were then correlated with device performance (e.g., R_0 and reverse leakage current). Minority carrier diffusion length measurements could be accurately made due to the 4 mil spacing between the diode active regions. This prevented any electrical interaction between the elements in the event of long minority carrier diffusion lengths. The results of these measurements, as well as other tests conducted, will be presented in the next section.

A summary of the wafers used for diode fabrication on this program is shown in Table 1. These wafers were chosen because of the magnitude of their base acceptor concentration (N_A). Since the diffusion limited performance of R_0 increases approximately in direct proportion to base acceptor concentration, the likelihood of the onset of tunneling currents also greatly increases. From previous experience, $N_A = 1\text{-}2 \times 10^{16}$ cm^{-3} is a reasonable compromise.

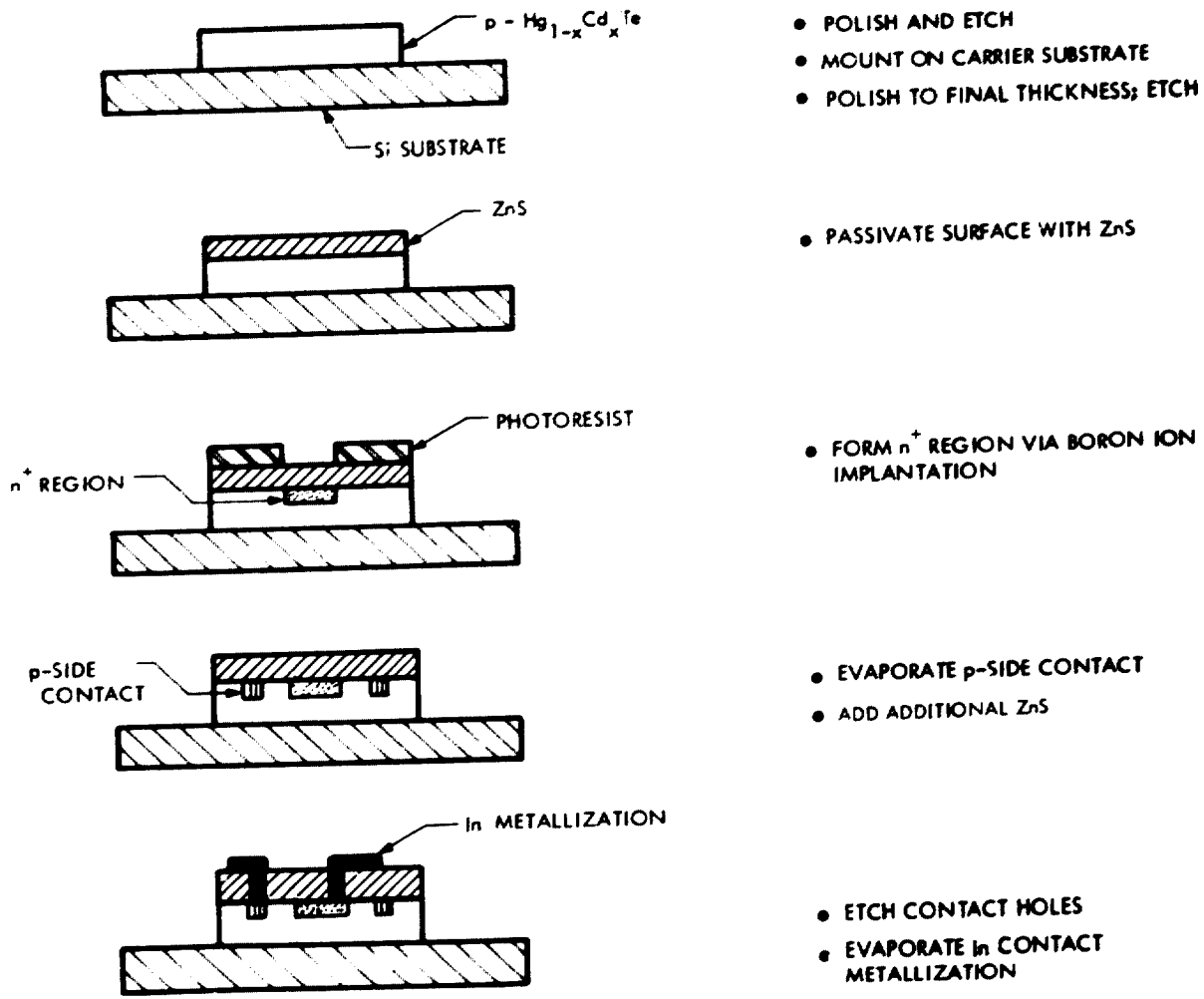

Figure 2. n^+ on p $Hg_{0.8}Cd_{0.2}Te$ Junction Photodiode Fabrication Steps

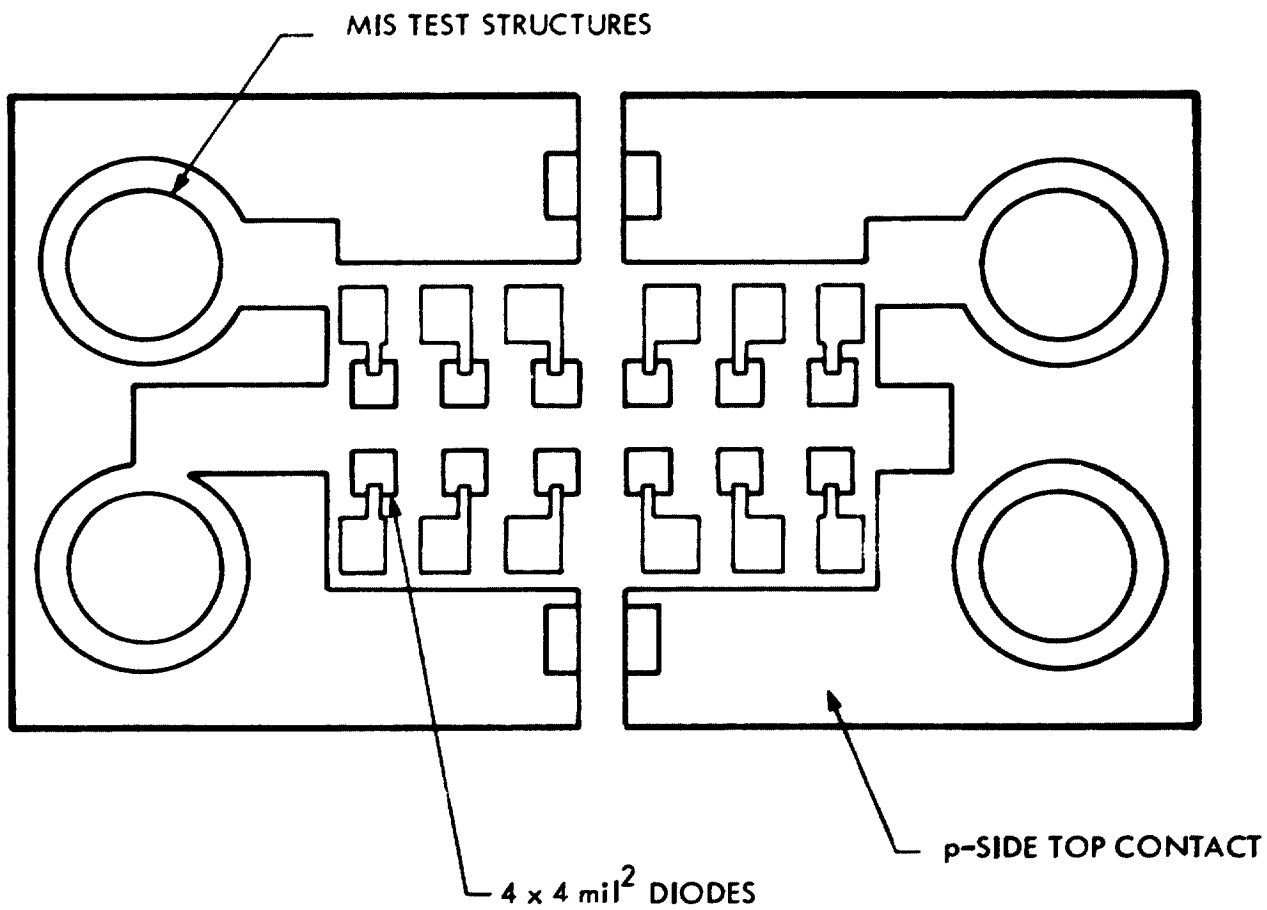

Figure 3. Schematic of NASA/JSC Test Array

Table 1. SUMMARY OF WAFERS USED FOR DIODE FABRICATION

WAFER	λ_{co}(80K) (μm)	λ_{co}(145K) (μm)	N_A(cm^{-3})
90579 S27-47(111)-6	11.4	9.4	1.4×10^{16}
90579 S27-47(111)-4	10.7	9.0	1.4×10^{16}
90579 S75-55(111)-5	11.8	9.6	1.8×10^{16}
30779 S60-85(111)-5	11.0	9.1	1.1×10^{16} (4×10^{15} cm^{-3} Cu)
30779 S60-85(111)-11	11.6	9.5	1.3×10^{16} (4×10^{15} cm^{-3} Cu)

3.2 DEVICE CHARACTERIZATION

We will now present the results of measurements carried out on the devices fabricated on this program. All the devices to be discussed had an anodic oxide grown on the back surface in the manner indicated in the previous section, and were thinned to various p-region thicknesses.

Initially, the devices were characterized by measuring the zero bias impedance (R_0) as a function of temperature. As was seen in Section 2.2, this allows the limiting current mechanisms to be determined. Using the expressions from Section 2.2, the R_0 vs. reciprocal temperature data were modeled. Results from arrays fabricated on wafer 90579 S75-55(111)-5 are presented in Figures 4 through 6. The diodes are clearly diffusion limited above T = 100K, at which point the g-r contribution begins to cause a deviation from the diffusion limit. The theoretical diffusion limit is indicated on each graph. The diffusion length of minority electrons ranges from 10 to 20 μm as determined from the model fit; direct measurements of diffusion length will be discussed shortly.

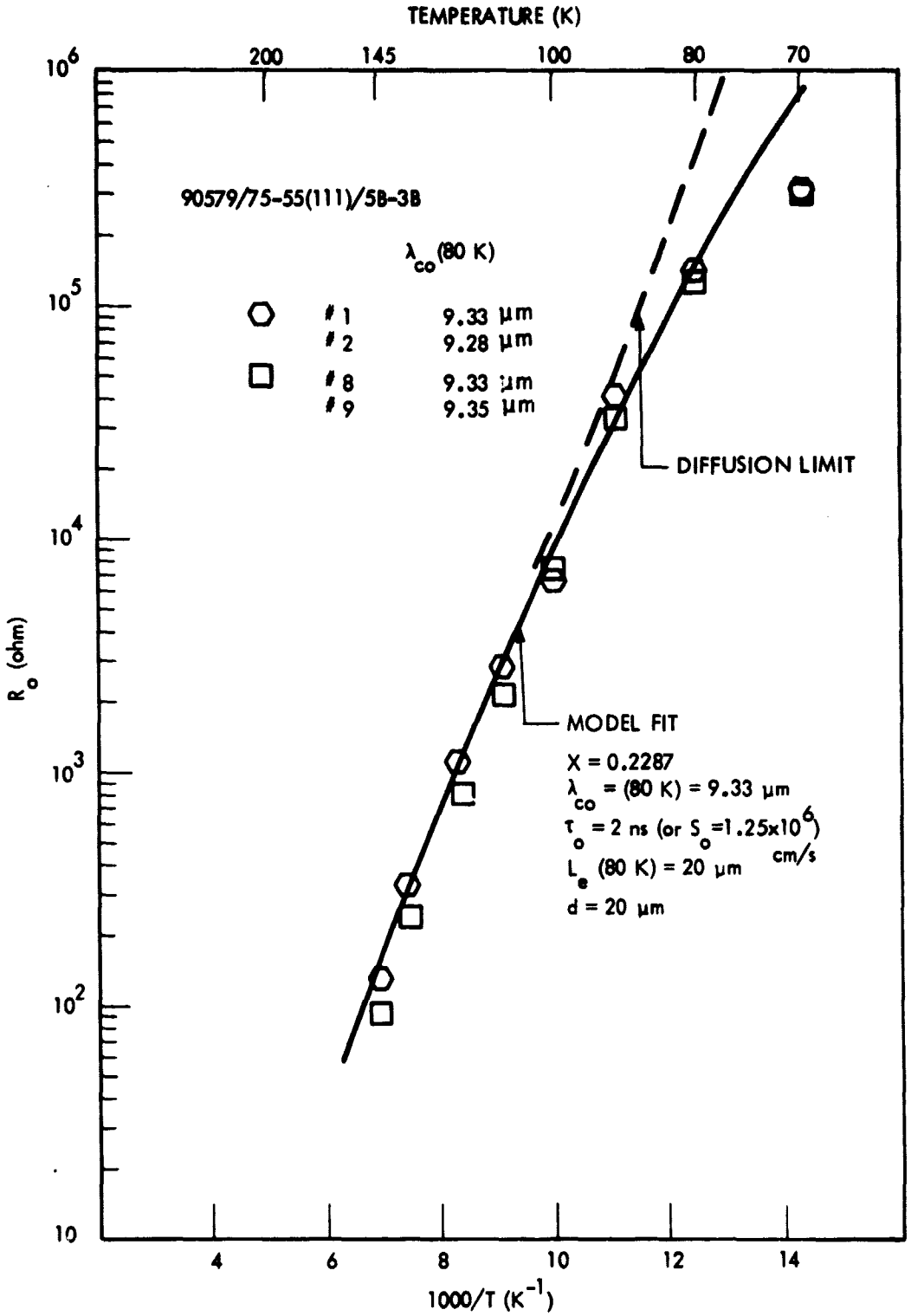

Figure 4. R_0 vs 1000/T Measurements for Array 90579 S75-55 (111)-5B 3B

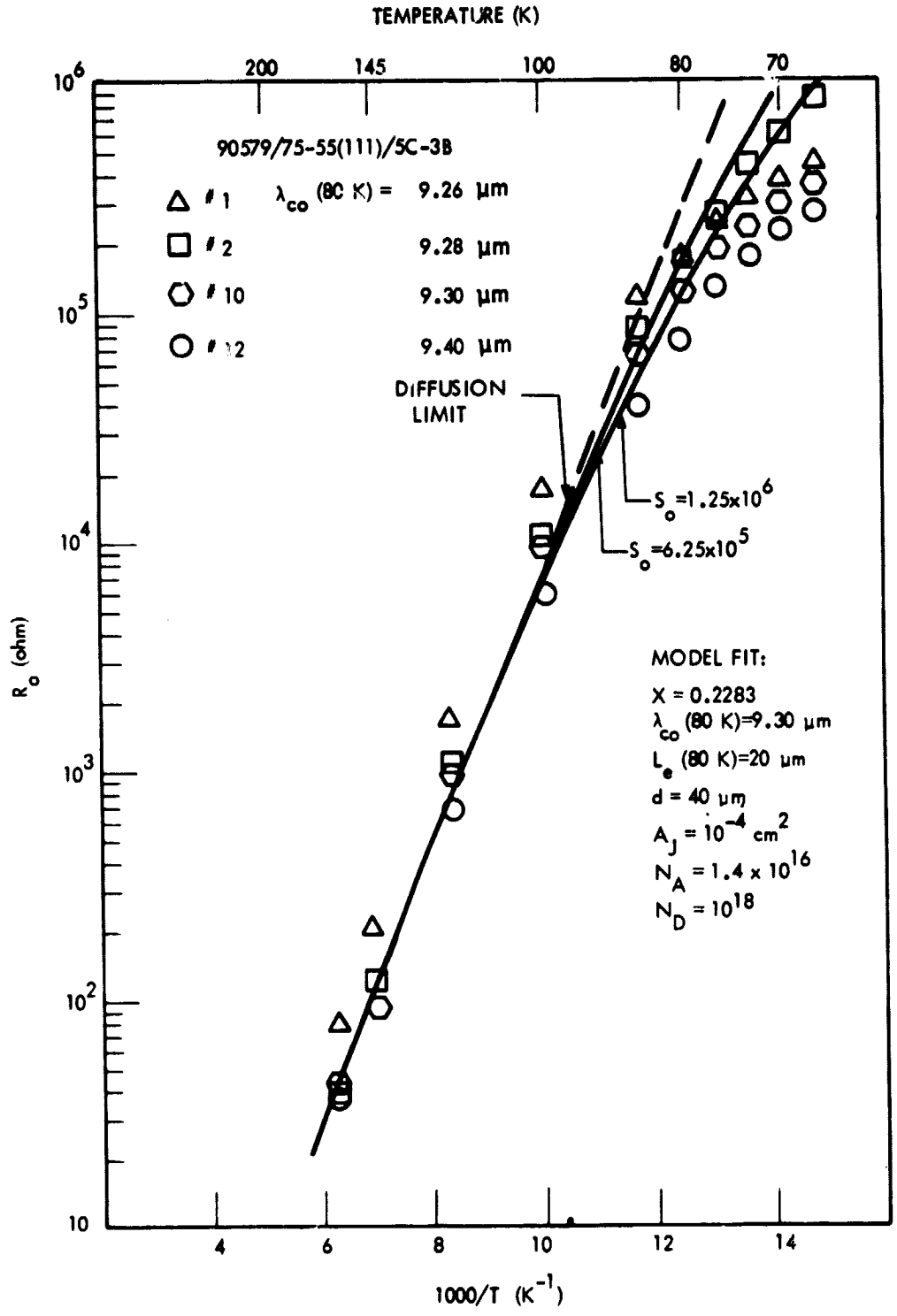

Figure 5. R_0 vs 1000/T Measurements for Array 90579 S75-55(111)-5C 3B

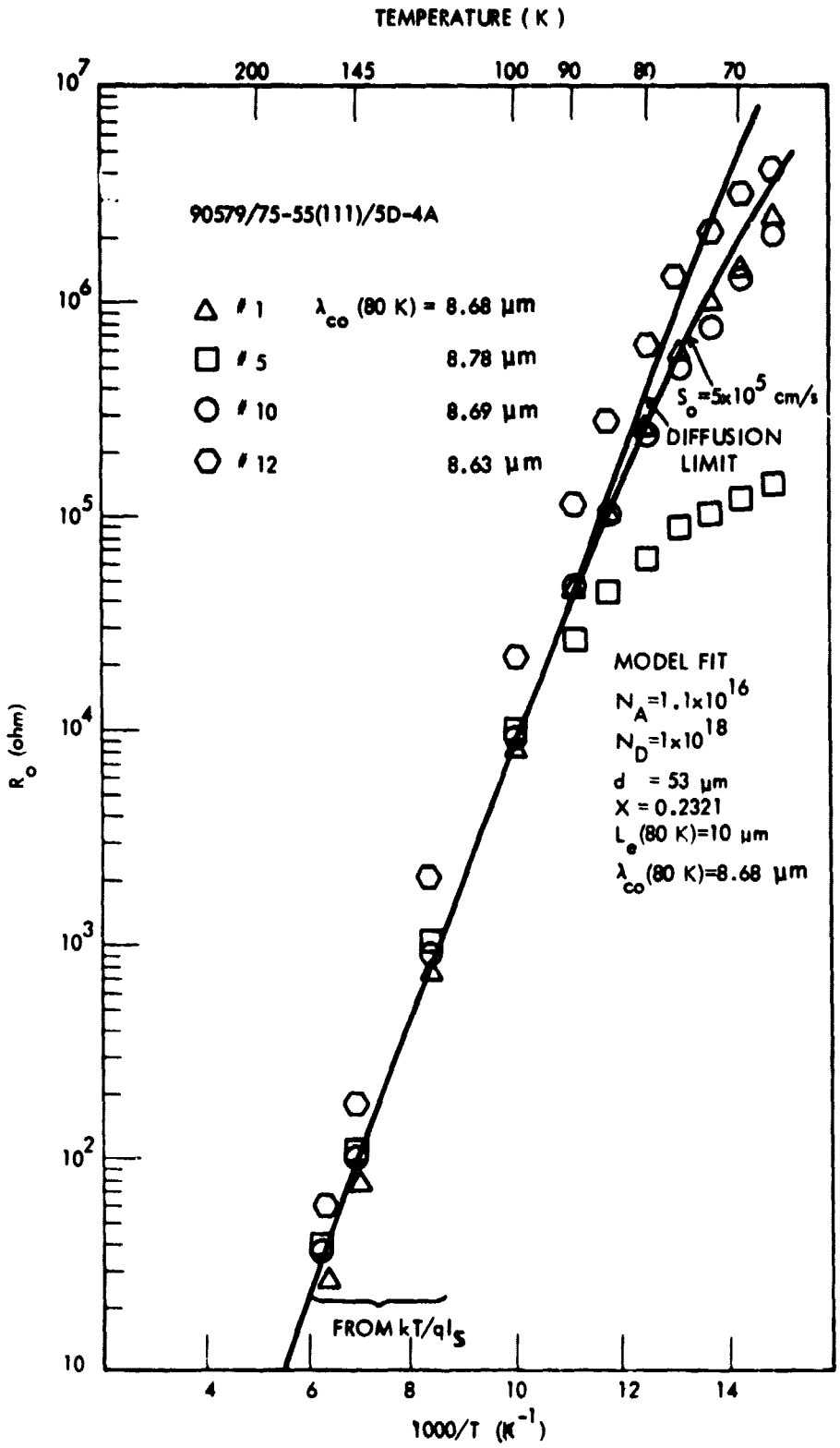

Figure 6. R_0 vs 1000/T Measurements for Array 90579 S75-55(111)-5D 4A

By combining Equations 8 and 11, it can be seen that the R_o is sensitive to the effective depletion layer lifetime, τ_o:

$$R_o (G\text{-}R) = \frac{V_{bi}\,\tau_o}{q n_i W_o A_J f(b)} \tag{16}$$

The values of τ_o obtained from the subject arrays range from 2 to 5 ns at 80 K. If the currents are due to surface G-R this lifetime could also be interpreted as an effective surface recombination velocity in the depletion region (not to be confused with the surface recombination velocity in the field region between diodes), by eliminating I_{OGR} from Equations 11 and 12:

$$S_o = \frac{A_J}{P_J \cdot \tau_o} \tag{17}$$

where P_J is the junction perimeter. This then could be used as a figure of merit for the surface quality. The deviation from the model fit observed at low temperatures ($T < 80$ K) is probably due to the onset of a surface leakage current component or a tunneling current component.

Before the subject of R_o is left, a word should be said about the procedure for measuring R_o at higher temperatures. As the cutoff wavelength increases, the diffusion limit is reduced, which can lead to problems in interpreting the high temperature ($T > 125$ K) R_o data. This occurs as the magnitude of the R_o becomes comparable to the series resistance. If the series resistance is not well known, it is necesary to find the R_o by other means. Since at these higher temperatures the diode performance is limited by diffusion current, we can use expressions 4 and 6 to describe the current and associated R_o. Thus by measuring the saturation current of the diode at high temperatures from I-V characteristics, the diffusion limited R_o can be calculated. Figures 4 through 6 demonstrate the agreement obtained between the diffusion limited predicted by theory and the data when this procedure is used.

In addition to characterizing the temperature dependence of R_o, detailed current voltage (I-V) measurements were carried out and the data modeled. Equations 4 and 7 were used to model the data, and results are shown in Figures 7 and 8 for the arrays whose temperature dependence of R_o are presented in Figures 4 and 5. An important result of this modeling was the calculation of a value for the "zero bias G-R current" I_{OGR} (see Equation 7). Solving Equation 12 for S_o yields:

$$S_o = \frac{I_{OGR}\, V_{bi}}{n_i\, kT\, W_o\, P_J} \tag{18}$$

Thus, using I_{OGR} obtained from the I-V modeling, we obtained a surface recombination velocity in the depletion region, if the G-R currents are surface related. As can be seen in Figures 7 and 8, the model fits the data between +50 mV and -60 mV. The slight deviation of the model from the data for V < -40 mV in Figure 7 is due to an additional current component, possibly tunneling. This fit is obtained by including series resistance (R_s) from 100-175Ω in the forward characteristic. The values of I_{OGR} obtained lead to S_o values ranging from 1.5 - 3.5 x 10^5 cm/s. When compared with the S_o values obtained from R_o vs 1/T modeling shown in Figure 5 and 6, we find reasonable agreement. These results are summarized in Table 2.

Table 2. SUMMARY OF S_o FOR TWO ARRAYS FROM WAFER 90579 S75-55(111)-5 USING TWO MODELING TECHNIQUES. T = 80 K

Diode #	S_o (R_o Modeling, cm/s)	S_o (I-V Modeling, cm/s)
5C 3B #4	6.3 x 10^5	3.5 x 10^5
5D 4A #12	5.0 x 10^5	1.5 x 10^5

Using either R_o or I-V analysis techniques to determine S_o yielded values of S_o ranging from 5 x 10^5 to 12.5 x 10^5 cm/s. This indicates varying amounts of G-R current. At T = 145 K, where the devices are clearly diffusion limited, the R_o values are comparable. At T = 80 K, however, the

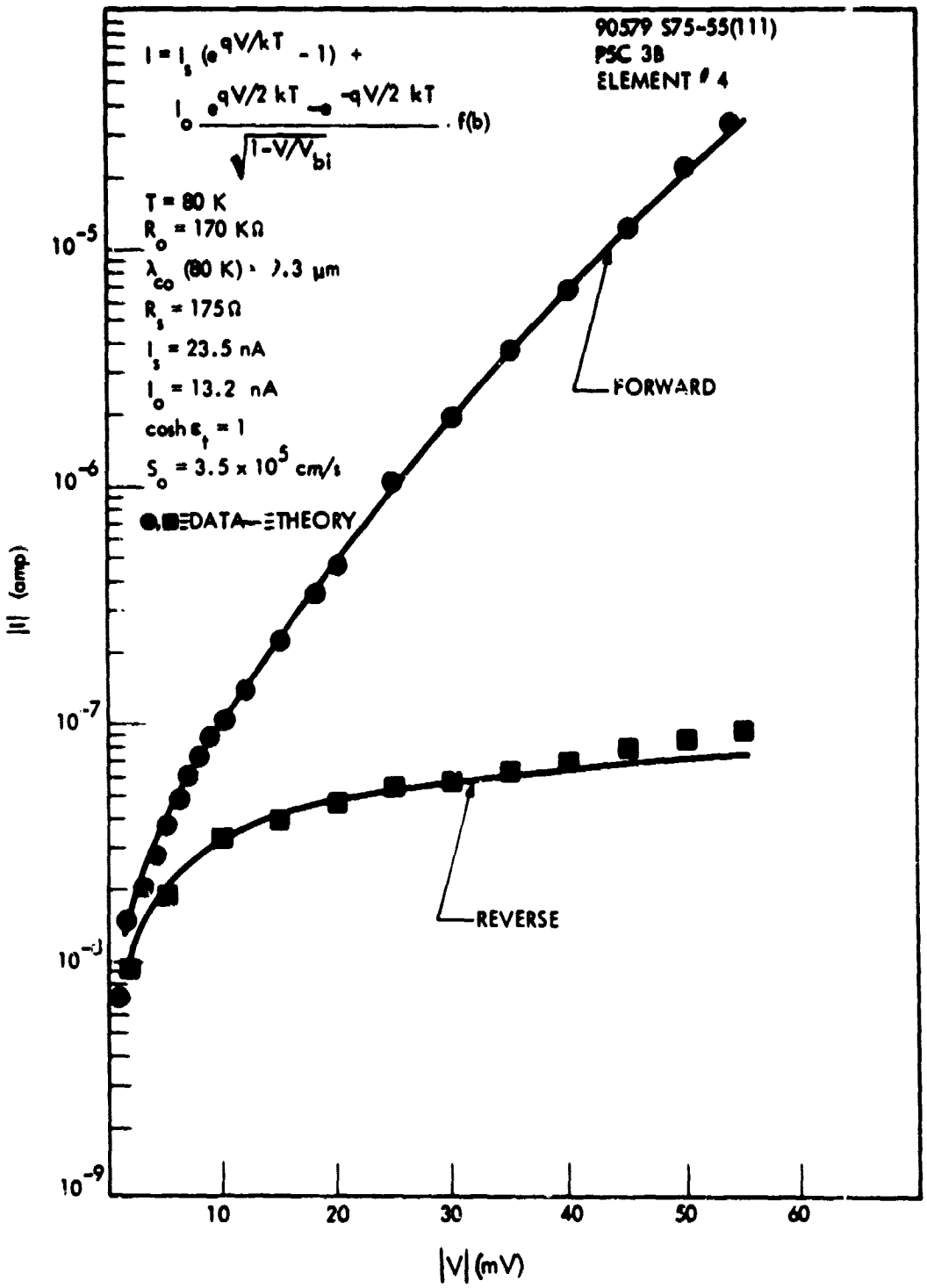

Figure 7. Forward and Reverse Current-Voltage Modeling for Diode 90579 S75-55(111)-5C-3B, el #4

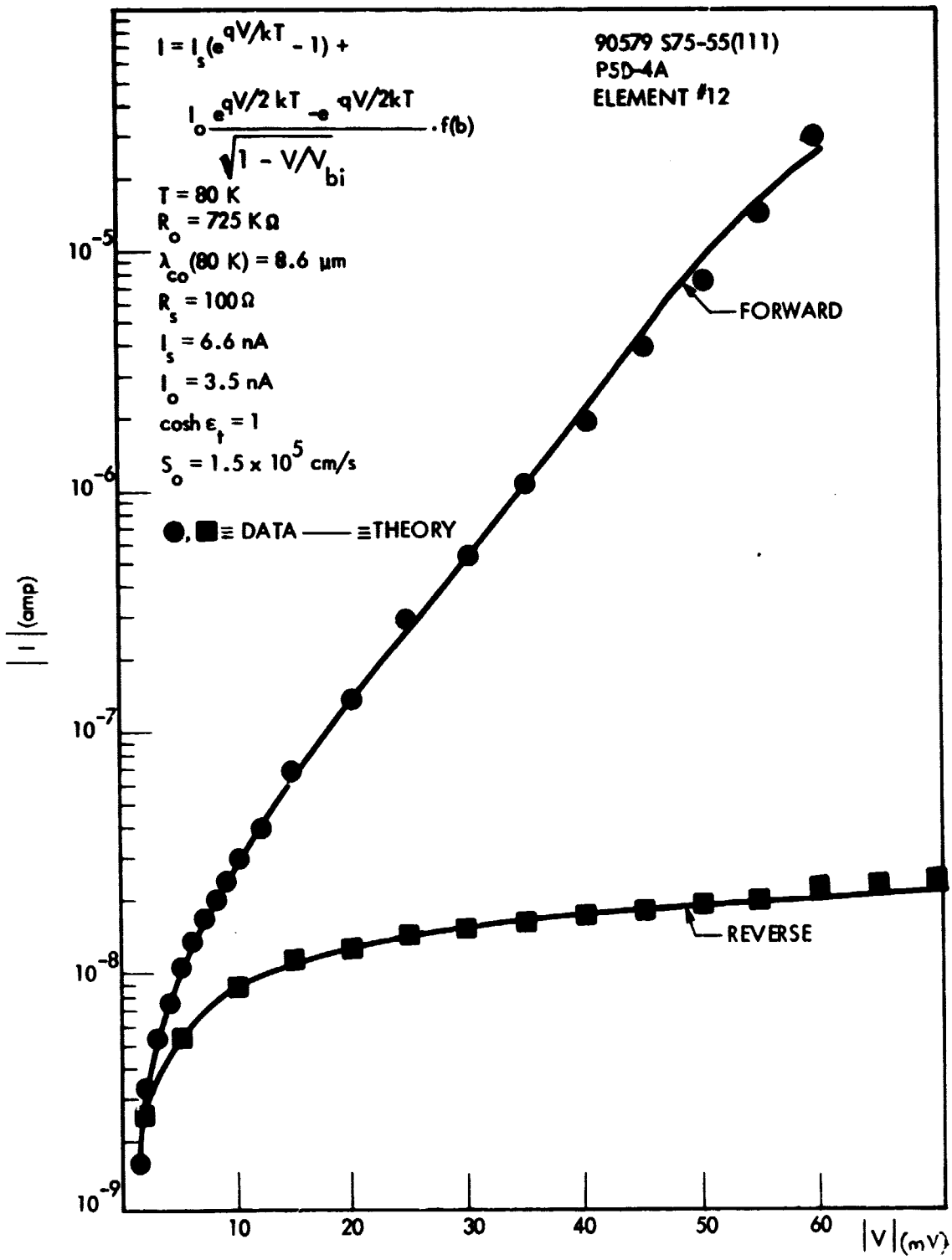

Figure 8. Forward and Reverse Current-Voltage Modeling for Diode 90579 S75-55(111)-5D 4A, el #12

R_0 values show some deviation from each other. Since the devices are almost completely G-R limited at this temperature, variations in the G-R current are influencing the R_0. Now, if the G-R current originated in the bulk, we would expect similar low temperature results from one device to another, in much the same manner that the bulk diffusion limited performances were similar. Therefore, the variations in G-R current are probably from generation-recombination at the surface in the surface depletion region, and S_0 can indeed be related to the surface quality. These results are summarized in Table 3 below.

Table 3. SUMMARY OF PERFORMANCE DATA FOR ARRAYS FABRICATED FROM WAFER 90579 S75-55(111)-5

ARRAY	λ_{co} (80 K) (μm)	R_0 (145 K) (Ω)	R_0 (80 K) (Ω)	S_0 (80 K) (cm/s)
5B-3B	9.3	118	1.35×10^5	1.25×10^6
5C-3B	9.3	115	1.07×10^5	6.25×10^5
5D-4A	8.7	114	2.05×10^5	5.00×10^5

The best value of S_0 seen on devices fabricated on this program was $S_0 \sim 1.5 \times 10^5$ cm/s, and was seen to correlate with the quality of the device processing. Samples which had values of S_0 from $1\text{-}10 \times 10^6$ cm/s were found to have had problems during processing, such as mechanical damage and chemical residues on the surface. Reduction in these processing problems has allowed devices with $S_0 \leq 1 \times 10^{15}$ cm/s to be fabricated more routinely.

The I-V model was also used to calculate the R_0 of a diode by summing in parallel the contributions from the diffusion limited and G-R limited R_0's, i.e.,

$$R_0\,(\text{tot})^{-1} = R_0\,(\text{diff})^{-1} + R_0\,(\text{G-R})^{-1} \tag{19}$$

The expressions for R_0 (diff) and R_0 (G-R) employed in this analysis are:

$$R_0\,(\text{diff}) = \frac{kT}{qI_{SAT}} \tag{6}$$

and

$$R_o\ (G\text{-}R) = \frac{kT}{qI_{OGR}f(b)} \qquad (8)$$

The results of calculations carried out in this manner are summarized in Table 4 for the two diodes listed earlier. The values for I_S and I_{OGR} were obtained from the modeling procedure, and are seen to result in excellent agreement with the measured values.

Table 4. CALCULATED AND MEASURED R_o FOR DEVICES FABRICATED FROM WAFER 90579 S75-55(111)-5. T = 80 K

DIODE #	R_o (diff) (Ω)	R_o (G-R) (Ω)	R_o (tot) (Ω)	R_o (meas) (Ω)
5C 3B #4	293 K	522 K	188 K	170 K
5D 4A #12	1.05M	1.97M	683 K	725 K

Although these devices will be operated at T = 150 K, where their performance is limited by bulk diffusion current, surface quality must be maintained to ensure reproducible performance. In order to monitor the quality of the final $Hg_{0.8}Cd_{0.2}Te$/ZnS interface, Metal-Insulator-Semiconductor (MIS) structures were incorporated onto each diode array, as indicated in Figure 3. Figures 9 and 10 present capacitance-voltage (C-V) results from two MIS structures. Immediately evident is what appears to be low-frequency type behavior, which indicates significant minority carrier generation at the HCT/ZnS interface. However, closer examination of the data suggests that the interface is departing slightly from the low frequency limit and is behaving in an intermediate frequency manner. The slight increase of the MIS conductance (G) in inversion (positive gate voltages) as compared to its value in accumulation (negative gate voltages) shows this departure away from low frequency type behavior. This departure indicates a minority carrier generation rate less than that observed in the low frequency limit. Also note the position of the

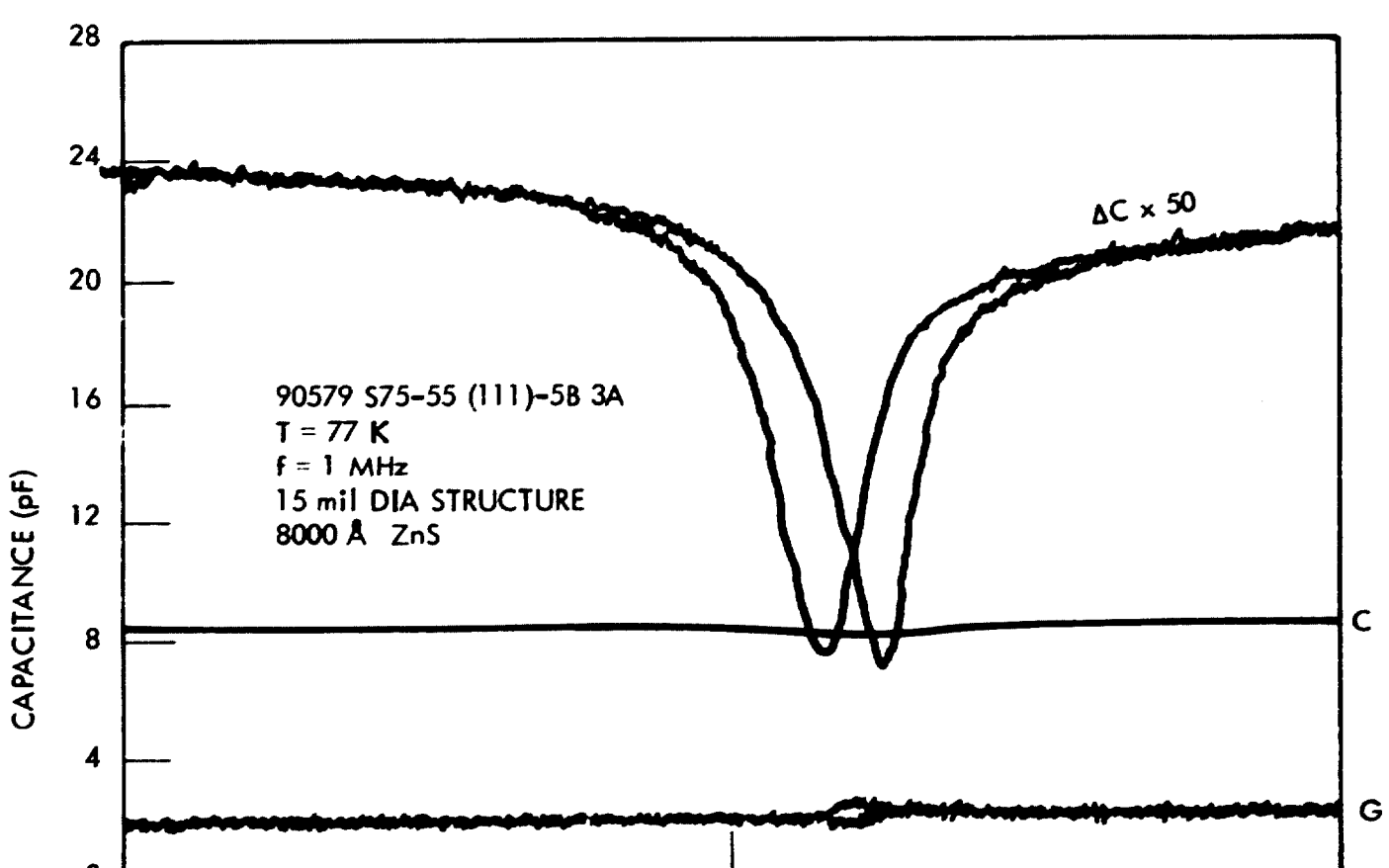

Figure 9. C-V Characteristic for ZnS/ $Hg_{1-x}Cd_xTe$ Interface for Diodes with Good Performance

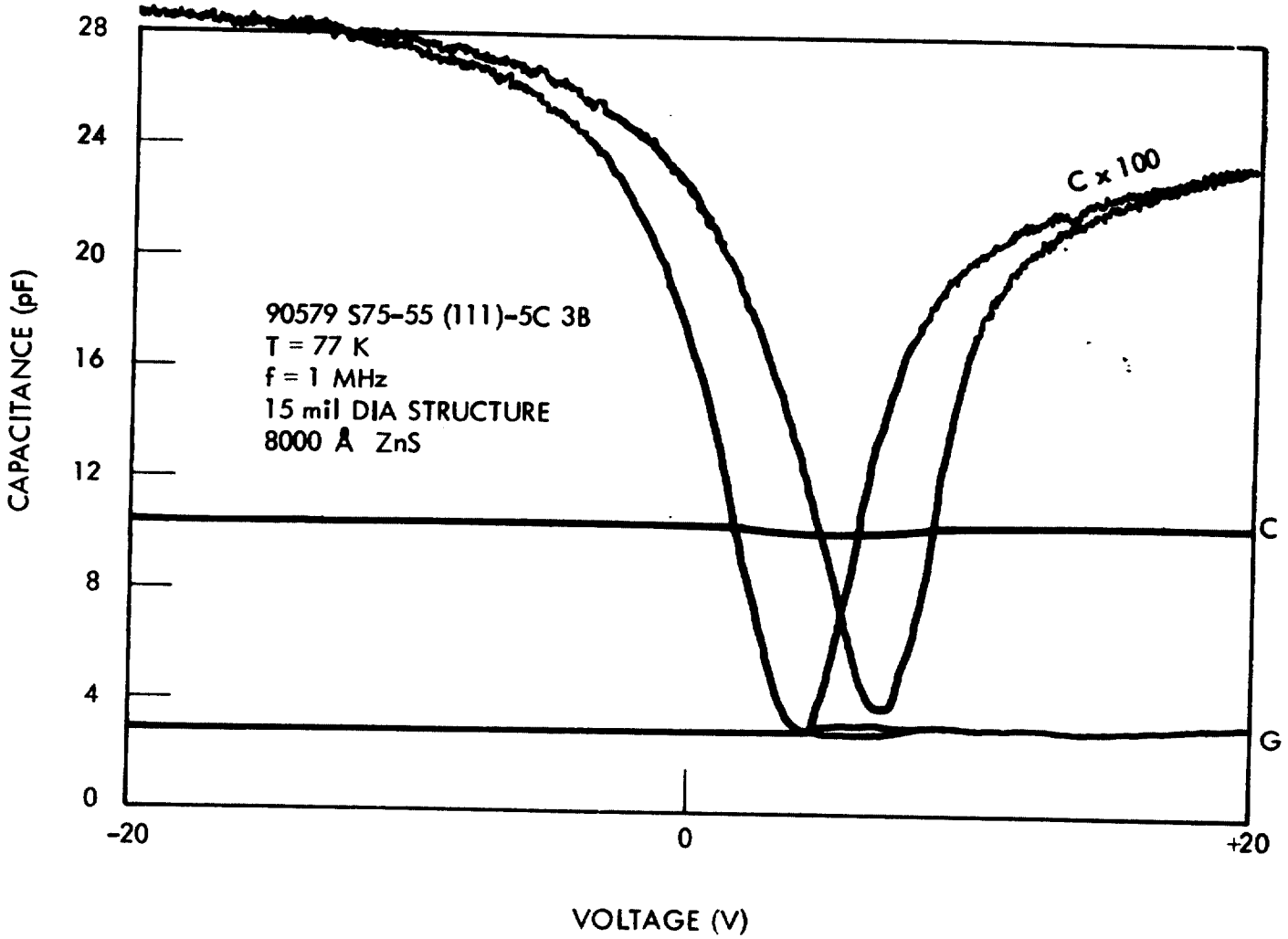

Figure 10. C-V Characteristic for ZnS/ $Hg_{1-x}Cd_xTe$ Interface for Diodes with Good Performance

C-V curve with respect to the zero gate voltage. This position indicates a surface potential which is near flatband. Previous work carried out at Honeywell has shown that optimum device performance is obtained when the surface potential produces a surface condition which is near flatband or slightly depleted.[10] This means that these devices have been processed in a manner which produces acceptable surface conditions.

As an example of the usefulness of MIS evaluation of surface conditions, Figure 11 presents C-V data for a sample which encountered problems during fabrication. During the deposition of the insulating ZnS layer, vacuum integrity problems developed in the sputtering system. The MIS C-V data obtained from this sample drastically depart from ideal behavior. The diode data show resistor like behavior, even at low temperatures, where series resistance is not a problem. In view of the very non-ideal MIS C-V characteristics, this resistive behavior is probably due to surface shunting.

Knowledge of the minority carrier diffusion length (L_e) is necessary for proper analysis of the data obtained from thin, backside contact diodes, because

$$\frac{R_0A}{R_0A_\infty} \propto \coth (d/L_e), \tag{20}$$

where d is the bulk region thickness, R_0A is measured for a device with $d \leq L_e$, and R_0A_∞ is measured for a device with $d \gg L_e$. To measure the minority carrier diffusion length, the output of a 500 K blackbody was focused to a 1 mil spot and positioned on the detector array. As the spot passed over the diode into the surrounding bulk material, the photoinduced current was measured. Since the diffusion length is defined as the distance over which the electron concentration drops to 1/e of its initial value, we can relate the measured signal to the diffusion length, i.e.,

$$I \propto e^{-x/L_e} \tag{21}$$

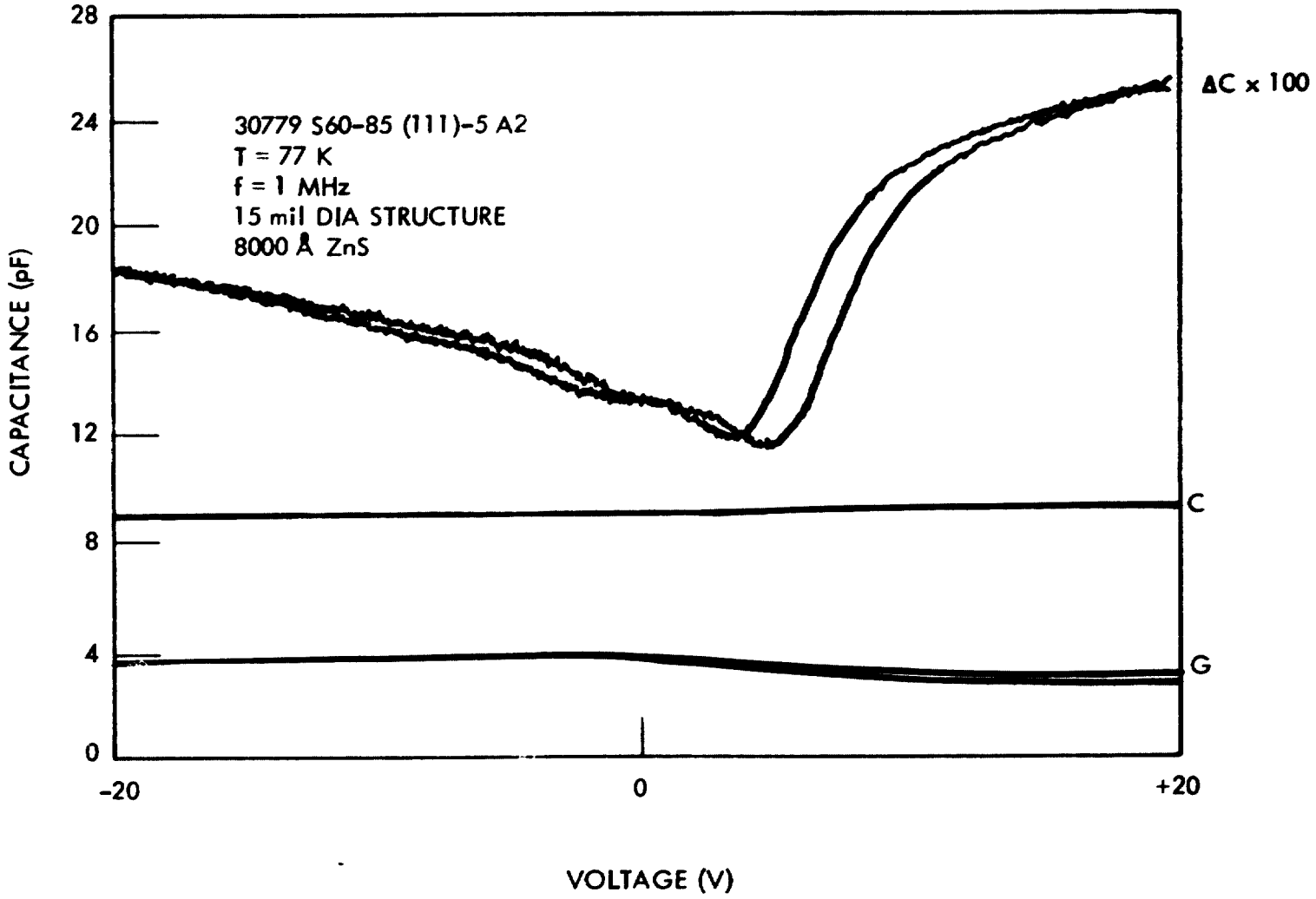

Figure 11. C-V Characteristic for ZnS/ $Hg_{1-x}Cd_xTe$ Interface for Diodes with Poor Performance

Thus by measuring the current a few mils away from the junction, a value for L_e was obtained from the relation:

$$L_e = \frac{x_2 - x_1}{\ln\left(I(x_2)/I(x_1)\right)} \tag{22}$$

where x_1 and x_2 are two positions of the spot outside the junction area, and $I(x_1)$ and $I(x_2)$ are the signal currents measured at these points. This method of measuring the diffusion length establishes a lower limit for L_e. If surface recombination effects are substantial a certain percentage of the electrons could recombine at the surface before being collected by the junction. This would appear as a decrease in current for a given point, and hence as a decrease in measured L_e.

Diffusion length values obtained by this technique are shown in Figures 12 through 14. The expression for diffusion length is given by:

$$L_e = \sqrt{\frac{\mu_e \tau_e kT}{q}} \tag{23}$$

indicating that the diffusion length will vary with $T^{0.5}$, and the temperature dependences of $\mu^{0.5}$ will also contribute. Recent work carried out at Honeywell has shown that, in the temperature range $80 < T < 150$ K, L_e varies only slightly.[11] This is due to the combined effect of the temperature dependences of μ_e and τ_e. Therefore, it is not surprising to see the agreement in L_e for the data in Figures 12 and 13 at T = 80 K with Figure 14 at T = 120 K. Even though the devices are not diffusion current limited at T = 80 K, the photogenerated current produced in the diffusion length measurement is still collected by diffusion of the electrons. Thus, the data obtained at T = 80 K will be valid for use in determining the effect of thinning the bulk region of the diode in conjunction with a back surface treatment.

In order to determine the effect of the back surface preparation procedure, data at T = 145 K will now be considered. As was shown earlier, at this temperature the diodes are diffusion limited. In Figure 15 are shown the R_o (145 K) vs λ_{co} (80 K) data for arrays with four different thicknesses,

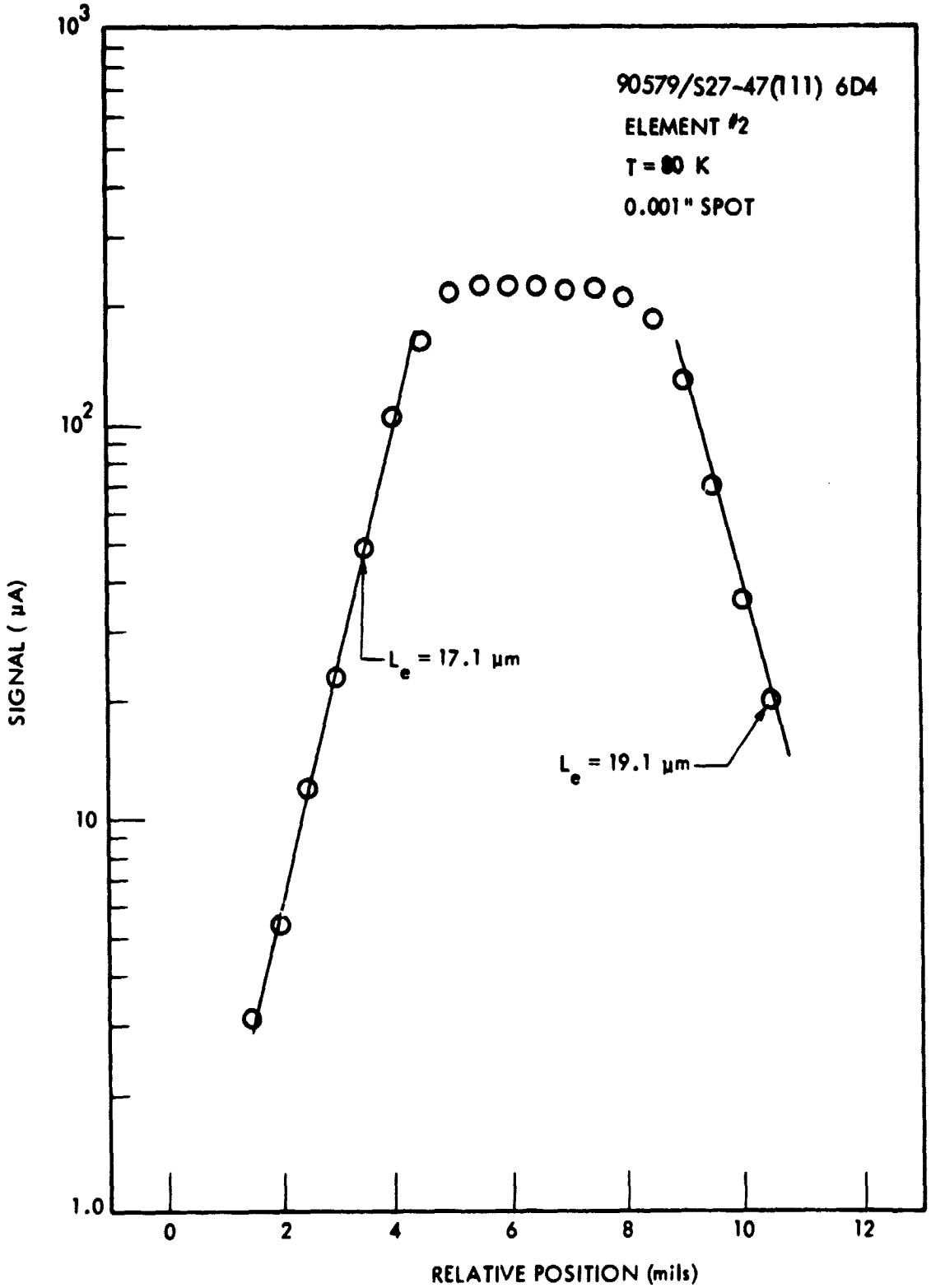

Figure 12. Line Scan for Diffusion Length Measurement for Diode 90579 S75-55(111)-5B 3B, el #2

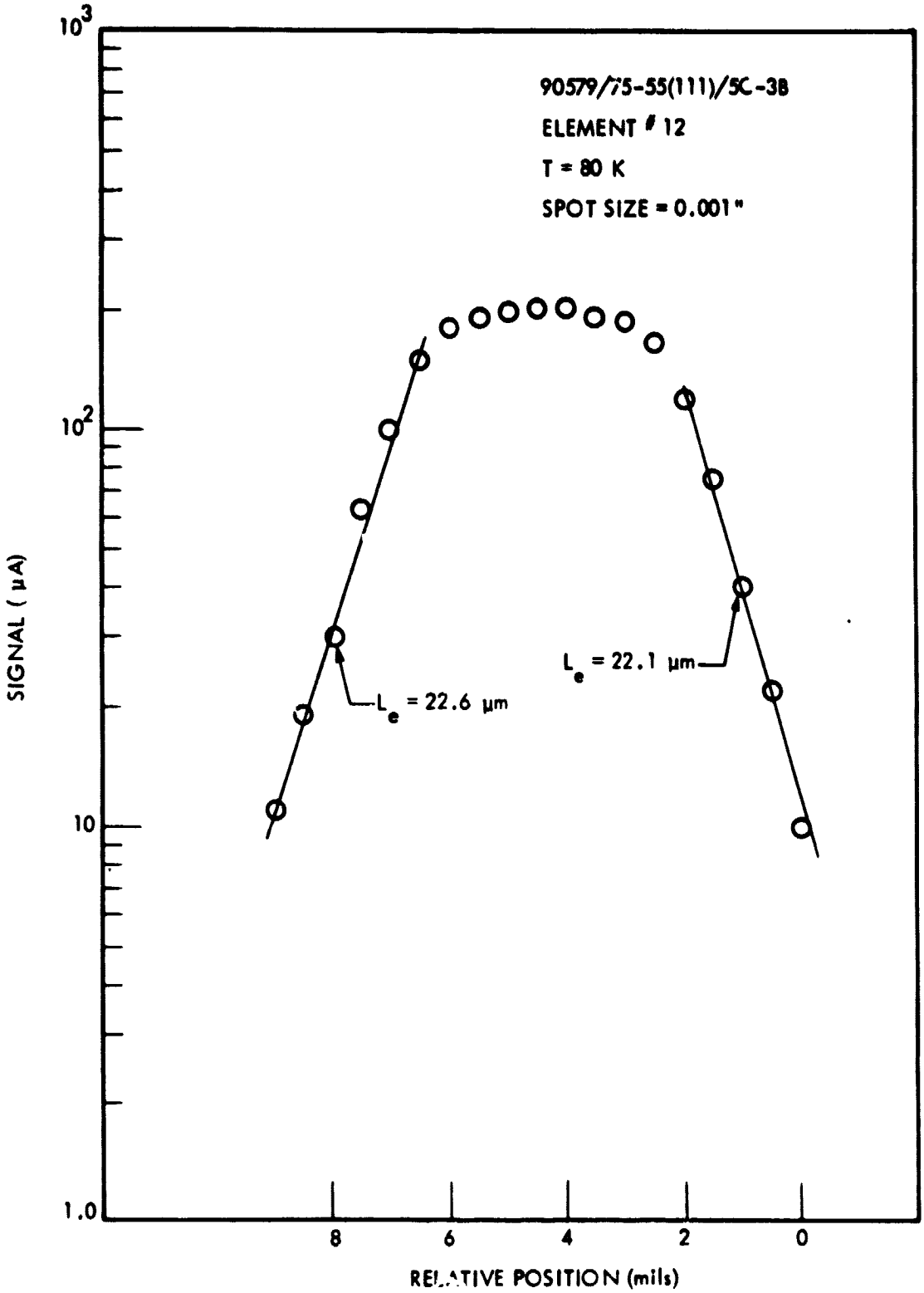

Figure 13. Line Scan for Diffusion Length Measurement for Diode 90579 S75-55(111)-5C 3B, el #12

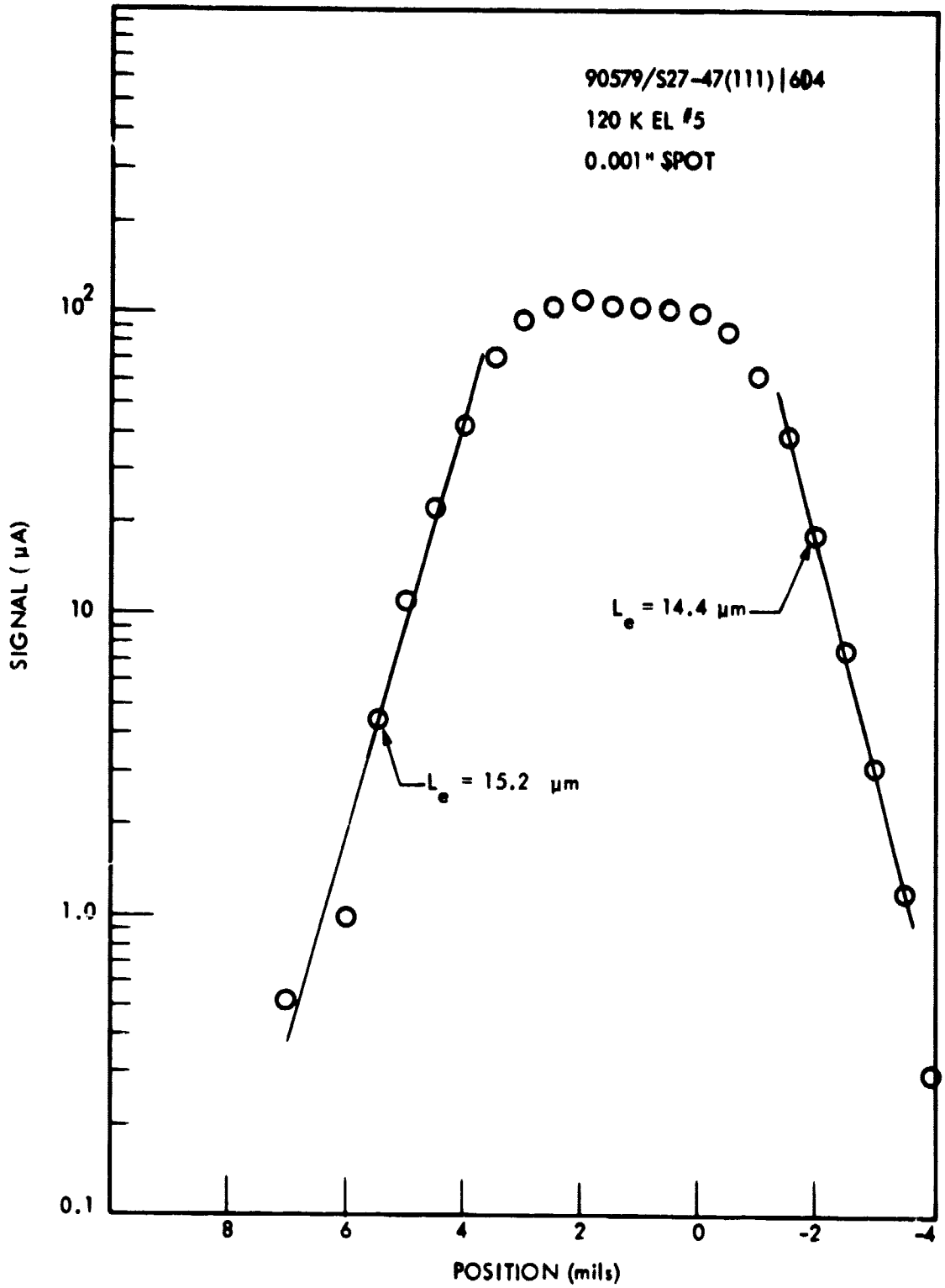

Figure 14. Line Scan for Diffusion Length Measurement for Diode 90579 S75-55(111)-6 D4, el #5

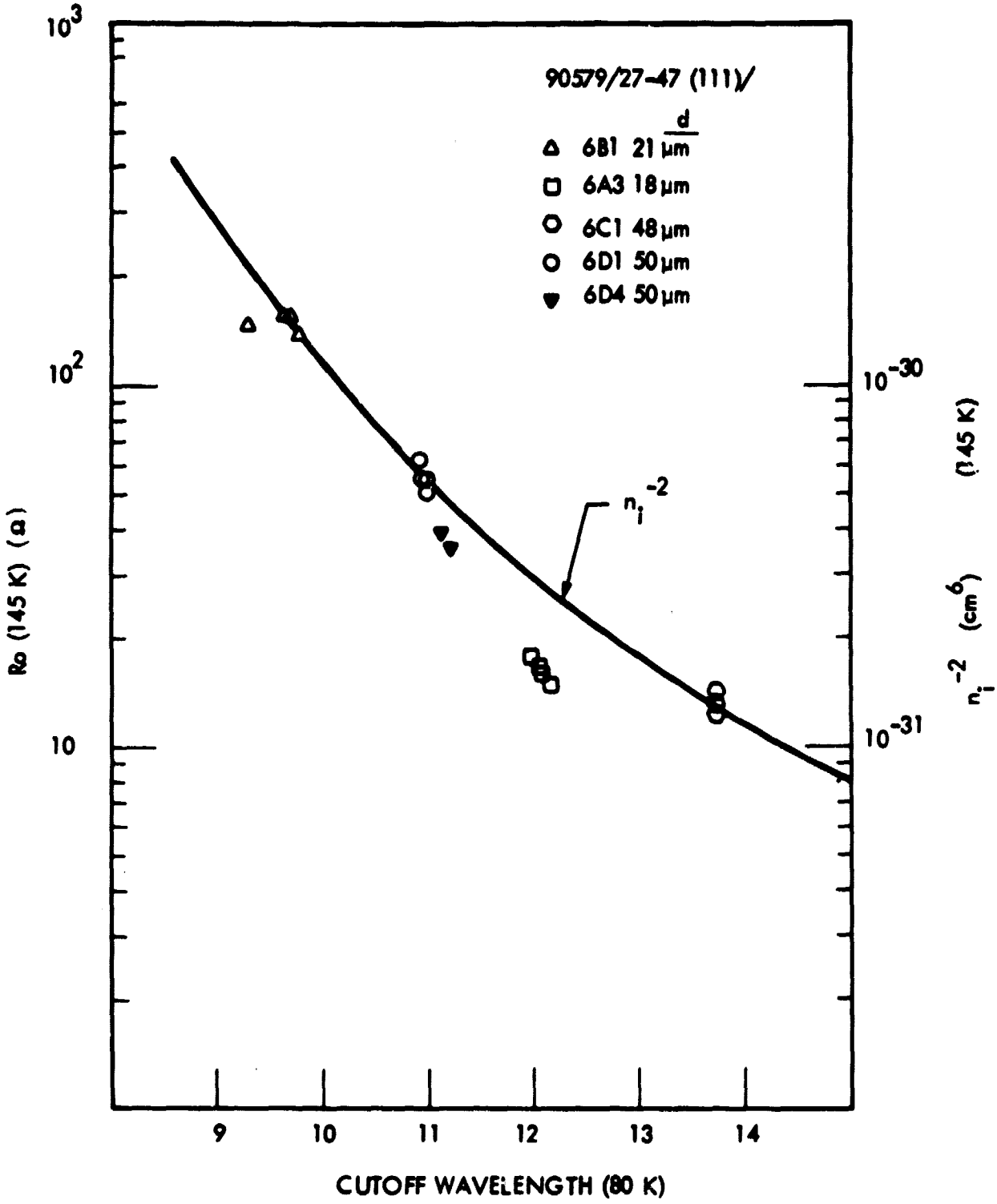

Figure 15. Zero Bias Impedance (R_0) Versus Cutoff Wavelength (λ_{CO}) Showing both Experimental Data and Diffusion Limited Theoretical Curve

with each array having different cutoff wavelength. These arrays were all fabricated simultaneously on the same substrate, and the variation in cutoff wavelength was due to substantial compositional gradients. In order to normalize the data with respect to cutoff wavelength, the reciprocal of n_i^2 at 145 K is plotted vs cutoff wavelength.

Since the devices are diffusion limited, their R_o values will be proportional to n_i^{-2}. Thus, a comparison betwen the magnitude of R_o can be conveniently carried out. As can be seen in Figure 15, the data from all but one of the arrays follow the n_i^{-2} curve, indicating no deviation from bulk diffusion limited behavior. Listed in Figure 15 are the thicknesses of the arrays. The measured diffusion length for array #6 D4 was L_e - 15 μm. If we assume that this is the diffusion length for the other arrays, also, we see that an increase of 20% over the "infinitely thick" diode is the maximum that can be expected (cf. Equation 20). Had there been some advantages from the back surface, array #6B1 would have exceeded the "thick" diffusion limited by 13%, and array #6A3 would have had a 20% increase. It is conceivable that the decrease in performance for array #6A3 was due to excess charge generation at the back surface, and diffusion of these charges to the junction causing a decrease in the measured R_o. That this is not the full explanation can be seen by the following analysis. The data for array #6A3 are approximately 60% below the diffusion limit suggested by the other arrays. Thus, R_oA/R_oA_∞ ~0.6 (cf. Equation 20). The ratio of d/L_e = 1.2. Using Figure 1 (which plots (R_oA/R_oA_∞) vs d/L_e with surface condition as a parameter), β would have to be greater than infinity to describe the data in terms of deleterious back surface effects. Even an ohmic contact ($\beta = \infty$) would not describe the deviation observed. Thus, this departure from the bulk diffusion limit cannot be caused solely by a poor back surface, but is likely due to large variation in the material properties, i.e. shorter lifetime and electron diffusion length. These variations in material properties as well as thicknesses of the p-side being large compared with electron diffusion length did not allow proper assessment of the effect the anodic oxidation of the back surface has on the device performance.

The compositional uniformity for wafer 90579 S75-55(111)-5 was quite good. Therefore, a plot such as that shown in Figure 15 was not necessary for data comparison. To normalize the measured data of array #5D-4A to those of array #5B-3B and #5C-3B, a factor of .62 is used. This accounts for the change in measured cutoff wavelength (through n_i^{-2}). Although the plot in Figure 16 seems to indicate an increase in R_o as the d/L_e ratio is decreased, the normal experimental error and lack of smaller d/L_e ratios prevented a firm conclusion regarding the benefit of the back surface preparation from being reacned. The data are listed in Table 5.

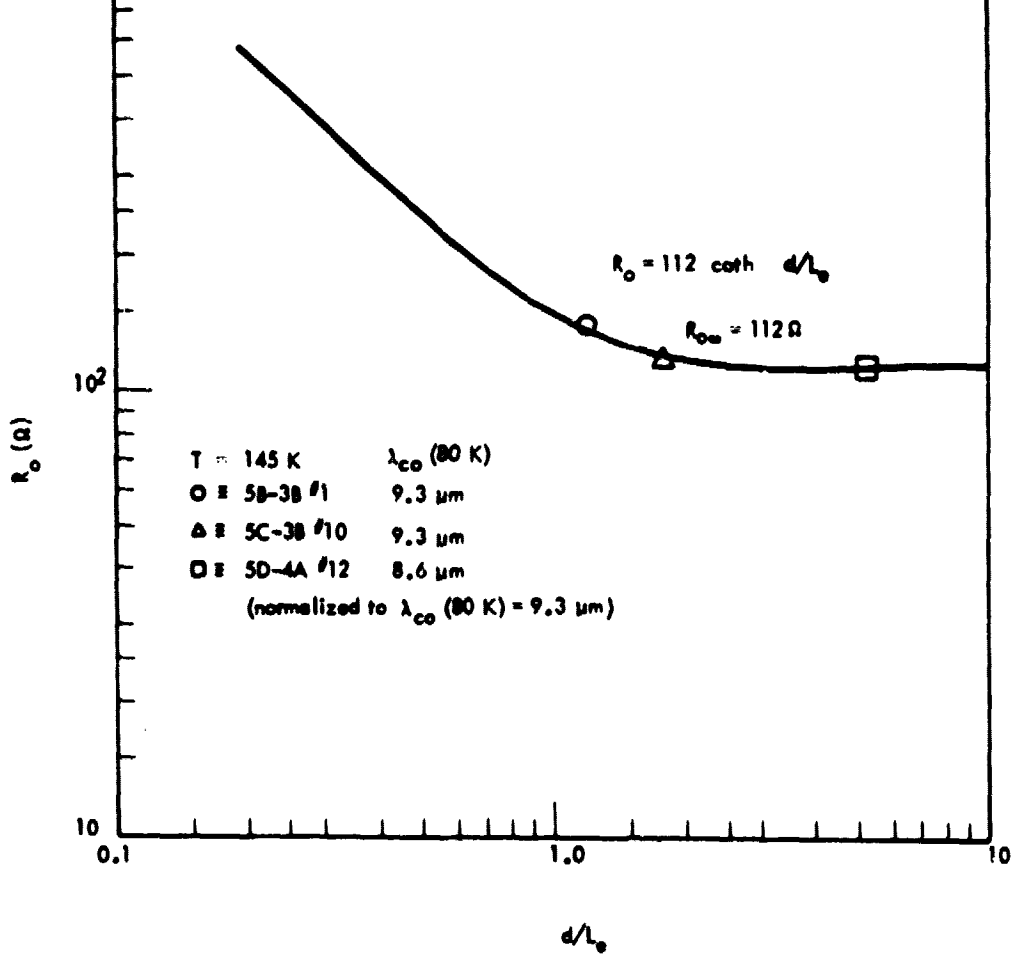

Figure 16. R_o vs d/L_e for Three Arrays from Wafer 90579 S75-55(111)-5

Table 5. SUMMARY OF DEVICE DATA FOR 3 ARRAYS OF DIFFERENT THICKNESSES FROM WAFER 90579 S75-55(111)-5

DIODE	λ_{co} (80 K)	d (μm)	L_e (μm)	$\coth \frac{d}{L_e}$	R_o (145, Norm) Ω	R_o (theo) Ω
5B 3B #1	9.3	20	18.1	1.19	138	133
5C 3B #10	9.3	40	22	1.05	115	117.6
5D 4A #12	8.6	53	10*	5.3	112	112

*L_e obtained from model fit.

SECTION 4
SUMMARY AND CONCLUSIONS

The major conclusions arrived at upon completion of the program can be summarized as follows:

- Variable thickness diodes were fabricated with a back surface anodic oxide to investigate the effect of this back surface preparation on the diffusion limited zero bias impedance (R_0). It was expected that this preparation would result in an increase in the diffusion limited R_0, but no unambiguous increase in R_0 was observed. This was due to the short minority carrier diffusion lengths in the fabricated diodes. As seen in Equation 14 and Figure 1, for a significant increase in R_0 to occur, the relation $d/L_e < 0.5$ must be satisfied. Since this condition was not met, it was not possible to determine whether or not the anodic oxide preparation was having an effect on the diodes' performance. This does not rule out anodic oxidation as a viable back surface preparation for providing a backside reflecting contact, and further work with thinner diodes or material having longer minority carrier diffusion lengths is necessary to precisely determine the results of the treatment.

- An I-V modeling technique was refined to thoroughly model the I-V characteristics of the diodes, and thus gain an understanding of the origin of the current mechanisms comprising the junction current. This technique allowed the separation of the diffusion and G-R contributions to the junction current, and successfully explained the I-V characteristics of these photodiodes. Using the zero bias G-R current (I_{OGR}) obtained from the model, values for the surface recombination

velocity in the depletion region (S_0) were obtained. This information was used to monitor surface quality, and hence led to improvements in the device performance.

- By implementing better surface damage removal techniques, depletion region surface recombination velocities of $S_0 \sim 1 \times 10^5$ cm/s were obtained, representing an improvement of over an order of magnitude above previous results. This is an important step towards fabricating photodiodes with high performance and greater uniformity.

REFERENCES

1. "Detection of Long Wavelength Infrared at Moderate Temperatures," Final Technical Report, NASA Johnson Space Center Contract NAS9-14180, Mod. 5S, April, 1977.

2. A. Van der Ziel, Advances in Electronics and Electron Devices. Vol. 46, Edited by L. Marton, Academic Press (New York, 1978), p. 313.

3. W. Shockley, Bell System Tecn. J. 28, (1949).

4. C.T. Sah, R.N. Noyce, and W. Shockley, Proce. IRE 45, 1228 (1957).

5. R.W. Dutton and R.J Whittier, IEEE Trans. Elec. Dw. ED-16, 458 (1969)

6. M.B. Reine, A.K. Sood, and T.J. Tredwell, "Photovoltaic Infrared Detectors, "Mercury Cadmium Telluride, Volume 18 of Semiconductors and Semimetals, edited by R.K. Willardson and A.C. Beer, Academic Press, New York (1980).

7. J.D. Beck and G. Sanborn, "(Hg,Cd)Te Trapping and Surface Processing," Final Report for Air Force Materials Laboratory Contract F33615-76-C-5070, AFML-TR-79-4046, Volume I.

8. M. Lamir, S.H. Shin, and A.H.B. Vanderwyck, Appl. Phys. Lett. 34, 50(1979); M. Lanir and S.H. Shin, J. Appl. Phys., to be published.

9. J.F. Shanley and L.C. Perry, "Infrared Heterodyne Photodiode Development and Characterization," Final Report for Ballistic Missile Defense Advanced Technology Center Contract DASG60-77-C-0081.

10. Work performed on AMMRC Contract DAAG46-79-C-0037, P00002.

11. D.L. Polla, S.P. Tobin, M.B. Reine, and A.K. Sood, "Experimental Determination of Minority Carrier Liretime and Recombination Mechanisms in p-type $Hg_{1-x}Cd_xTe$," to be published in J. App. Phys, 52 (1981).