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by

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Abstract

A 20-element monolithic InSb charge-coupled device (CCD) detector array was measured under low-background conditions to assess its potential for orbital astronomical applications. At a temperature of 64 K, previous results for charge transfer efficiency (CTE) were reproduced, and a sensitivity of about $2x10^{-15}$ joules was measured. At 27 and 6 K, extended integration times were achieved, but CTE was substantially degraded. The noise was approximately 6000 charges, which was in excess of the level where statistical fluctuations from the illumination could be detected. A telescope demonstration was performed, showing that the array sensitivity and difficulty of operation were not substantially different from laboratory levels. Ways in which the device could be improved for astronomical applications are discussed.

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I. Introduction

The device we tested is an experimental monolithic four-phase InSb charge coupled device (CCD) with 20 detector elements arranged in a linear array. The CCD was fabricated by Santa Barbara Research Center (SBRC) under contract to NASA Langley. The device is pictured in Figure 1. It consists of 20 InSb photocapacitors, each coupled via a transfer gate to a surface-channel CCD (SCCD) four-phase shift register. The photocapacitors are 32.5μm by 35μm, spaced on 50μm centers. An integral InSb output diode is used to read the collected charge via two silicon 3N163 FETs operated in the floating diffusion mode. The device also has an input diode which is used to provide a "fat zero" during operation in the photo mode, and for inputting a pulse train into the CCD for tuning up the transfer prior to photo-mode operation. "Fat zero" is a constant amount of charge that is injected continuously to improve signal charge transfer by filling trapping sites with charge.

The array includes up to nine clocks (designated by ϕ_1, ϕ_2, ϕ_3, ϕ_4, ϕ_T, ϕ_P, ϕ_{ID}, ϕ_{RST}, ϕ_{IB}) and six dc voltages (designated by V_{SC}, V_{CS}, V_{DD}, V_{SS}, V_{REF}, V_{OG}) to adjust simultaneously. Optimizing CCD performance is difficult since the trapping properties of the oxide-InSb region are bias-dependent and hence variable, producing hysteresis (ref. R. Thom, SBRC). Fortunately, only a few clocks and voltages are critical at any one time, although missing the proper setting by a few tenths of a volt on two of these can result in no transfer at all. A complicating factor is that the proper voltage settings from one week may not be optimum the next week, and finding an operating point can occupy many hours.

The electrical schematic for the CCD is shown in Figure 2. The shift register section of the device has 82 gates divided into cyclic four phase clocks, ϕ_1 through ϕ_4. Bias for the photodiodes is provided by ϕ_P, and accumulated signal charge is clocked into the shift register by the transfer gate clock ϕ_T. Charge is read out via an output diode connected to the two MOSFETs. One FET empties the charge accumulated under the output diode via a reset clock, ϕ_{RST}, which has a fixed drain bias V_{REF}. The second FET is a source follower with drain bias V_{DD} and source bias V_{SS}. The output gate (OG) is biased on to allow charge transfer to the output diode. A channel stop bias,

V_{CS}, defines the output diode and the charge transfer paths in the CCD. Charge can be electrically injected into the shift register through an input diode, (ID) which is clocked by V_{IB}, and metered by V_{SC}.

Our testing program is oriented towards astronomical applications from space platforms. For any device to be useful for observational astronomy, it must have certain attributes. If the device is to be used for photometry, its response must be linear (or at least one must be able to calibrate out the nonlinearities) and stable with time. If the device is used as an area imager or as the detector in a spectrometer, it must preserve the image when read out (i.e., have good transfer characteristics), and be able to integrate for long times. (For an excellent statement of astronomical array requirements, see Lynds (1980).) The InSb SCCD we tested was deficient in all of these categories when operated under very low background conditions. However, we realize that this is a first-generation device, and we were more concerned with characterizing the device, understanding it, and then suggesting improvements which would make it a viable astronomical tool. In the following sections we will discuss how we tested this device, our test results, and the conclusions we reached on its future applications.

II.   Test Setup

A.   Dewar

1.   Optical

The optical system was designed to produce low-background illumination on the array through attenuation of the external blackbody flux and reduction of photon leakage. Two aluminum radiation shields were attached to the Infrared Laboratories HD-3(8) dewar cold plate which restricted the field of view to f/20.3 and which supported the 2.7μm, 0.031μm-bandwidth interference filter (Figure 3). The overall system transmission was estimated to be 0.66 at 2.7μm, which produced the flux shown in Figure 4 on each detector.

The calculated background flux was 8×10^8 ph/cm^{2}sec (7×10^{-16} W). To reduce stray radiation, the insides of the shields were blackened with

3M Black Velvet paint, and the attachment joints were sealed with indium gaskets. Wiring on the cold plate was routed through shallow, crooked channels which were plugged with indium at the points where they entered the shields. Reducing the background entering the dewar by placing LN_2 in the field of view produced no change in signal, indicating that external scattered radiation was not a problem.

Silicon diode thermometers were used to monitor cold plate and array temperatures. The array thermometer was bonded to the ceramic package, about 1 cm away from the CCD. At equilibrium, the array temperature was ≤ 1 K above cold plate temperature.

2. Electrical

Two 61-pin Microdot hermetic connectors were used on the dewar outer shell. Signal and dc levels were routed through one of these; clocked lines were routed through the other. Twisted pairs of 0.13mm (5 mil) manganin wire were used on all array leads. Leakage currents in the connectors were measured to be $\leq 10^{-14}$ amps.

The array was mounted in a 40-pin dual in-line package. A zero insertion-force latching socket was used in the dewar to hold the package. A cooling path to the array was provided by strapping the unused socket pins to the cold plate with copper wire.

B. Electronics

A block diagram of the electronics is shown in Figure 5. The periodic clocking waveforms were produced with an Interface Technology RS-648C programmable word generator, controlled by a master square-wave generator. A 20-step program in the word generator produced the proper duty cycles and phasing for the nine clocked inputs. The four-phase clocking diagram is shown in Figure 6. These inputs were set to the desired voltage levels by circuitry which allowed adjustment of the amplitudes, offsets, and ramping of the clocks. A counter circuit was included which allowed variable integration times. The array could be read out cyclically or with an adjustable time delay between read

cycles. The ϕ_T pulse, which initiated readout, was also sent to a sample-and-hold stage to synchronize sampling of the readout.

A variable-gain, 100 kHz-bandwidth buffer amplifier was mounted on the dewar wall to drive the output signals over the cabling. The sample-and-hold was capable of acquiring each sample in < 2µsec. A capability for sampling once or twice per output waveform for correlated double sampling (White et al., 1974) was included, with the sample locations independently variable. A "bucket select" circuit was also built to enable sampling of only one detector per frame. This single-channel sample was then analyzed by an FFT spectrum analyzer, lock-in amplifier, and oscilloscope. The signal was also digitized by a Micronetworks 5212 12-bit analog-to-digital converter for further digital processing by a Hewlett Packard 9825A calculator. With the buffer amplifier input shorted, the noise level of the sampling system was measured to be about $2\mu V/Hz^{1/2}$, which was less than 1/10 the array noise levels. Also, correlated double sampling of the waveforms produced a reduction of at most 20% in noise, indicating that feedthrough noise components were small.

C. Calculator System

The HP-9825A was used to compute average voltage (signal) and standard deviation (noise) for each detector. The output of the A/D was fed into the 9825A in a direct-memory-access mode. Each readout cycle of the array was placed in memory in sequence, until the selected number of points had been transferred. It was found that consistent noise results could be computed when the sample size per detector was >50.

III. Test Results

A. Electrical Considerations

1. Leakage.

Electrical leakage tests were performed with the InSb array placed in its dewar mounting. A Keithley 742 electrometer capable of measuring 10^{-16} amps at bias voltages up to ±30 volts provided a more-than-adequate

measurement capability. Tests were run at 77 and 300 K giving leakages between the pins and ground of a few $\times 10^{-14}$ amps for all gates at 0V bias. A bias of -9V increased the leakage by a factor of 20-40. Temperature independent leakage could not be a characteristic of the device. The leakage was traced to the silicone rubber spacers in the Microdot 61-pin connectors, which were removed while measuring the currents reported above. There appear to be no anomalously high leakages associated with the device itself.

2. Output Diode.

The characteristic curve of the output diode was measured at 65 K. Surprisingly, the flat region of the diode I-V curve, where current is essentially constant, was not nearly as evident as that shown in the manufacturer's earlier report (Thom et al., 1980b). Figures 7, 8, 9 show the diode characteristic over three dynamic ranges. The diode curve in Figure 7 goes below zero amps at zero bias with an R_0 = 18.3MΩ (R_0A = 458Ωcm^2). The fact that a significant current is seen in Figure 7 at zero bias is most likely due to a thermocouple voltage. This could have shifted the curves a few mV to the right. Photoactivity alone could not have accounted for a current of this magnitude, since the device areas are quite small.

3. Output Capacitance.

The capacitive load (C_0) of the CCD is the sum of the stray capacitance and signal MOSFET input capacitance. C_0 was measured with an HP 6435A ac ammeter included in the reset drain line. The reset clock amplitude was used to effect a change in reset source voltage. A change of Δv in the reset voltage causes a change Δi in the reset current at the signal MOSFET input gate. The reset FET only affects the measurement through its gain G (assumed to be 0.9 ± 0.1). The clock duty time t_d is the product of the clock period (t) and duty cycle (d): $t_d = t \times d$. The expression for C_0 is then

$$C_0 = t_d G \ (\Delta i/\Delta v).$$

From measurment, t_d = 25μsec and ($\Delta i/\Delta v$) = 159 nA/V, giving C_0 = 3.5 pF $\pm$ 15%. The uncertainty is dominated by the measurement accuracy of Δi (+ 7%) and the

uncertainty of G ($\pm$ 10%). SBRC estimated a value of C_0 = 6.1 pF (Thom et al., 1980b) for the total output capacitance from the observed output voltage swing and a calculation of the charge being transferred. They subsequently measured C_0 with a capacitive bridge technique, and found it to be 3.7 pF (Thom et al., 1979, 1980a). Our results, obtained by monitoring reset drain current, corroborates their measurement.

B. Charge Transfer Efficiency (CTE)

The charge transfer efficiency is a measure of how much charge is moved from one gate to the next in the CCD shift register. ϵ =1-CTE is the fraction of charge lost in a single transfer. In this device there are 82 transfers between the input diode and output diode, so if ϵ is lost in each transfer, $1 - (1-\epsilon)^{82}$ will be lost in traversing the entire CCD. The method we used for determining CTE was taken from Thom et al., 1980b. Using their notation, the CTE = $(B/A)^{1/n}$ where B = magnitude of the first output pulse, A = maximum value of the pulse train, and n = number of transfers. This formulation only applies to a pulse train, and gives the average CTE for each transfer. For this device, the CTE is typically 0.987, and at best is 0.994. This means that typically 67% of the input charge from detector 20 is lost while traversing the CCD, while detector 1 suffers no significant loss. Most of the lost charge is left behind and comes out in subsequent pulses even with fat zero injection. This would be problematic for imaging since signals are smeared out and information is lost.

In practice, the CTE is optimized by injecting a pulse train into the CCD via the input diode and adjusting the clocks and voltages while watching the output on an oscilloscope. An example of the output is shown in Figure 10, with the operating temperature 27.2 K. An example of the best CTE performance is seen in Figure 11. This performance was obtained in mid-1979, at 64 K. Since there are a number of clocks and voltages to adjust and since the CCD will operate with the voltage clocks set to a multitude of values, it is never obvious that the CCD is operating in its optimum mode. In many cases it is clear that it is operating in a local maximum of the CTE.

The CTE is affected in several ways, which are illustrated by examining the operation of the device. Charge is transferred from one gate to the next by creating a potential well under the second gate and collapsing the well under the first gate. The voltage on the first gate is ramped off since the carriers (holes in this case) have a finite diffusion time. Charge that is not transferred by the time the gate is turned off can be lost to the substrate or laterally out the sides of the multiplexer. This device is a surface-channel CCD, meaning that the potential wells are created at the surface of the InSb substrate. Irregularities in the oxide thickness cause trapping sites at the SiO_2/InSb interface. These sites are filled by the first charge transferred through the CCD and by the dc level (fat zero) injected into the CCD. However, charge is not held statically in these sites, and the spectrum of reemission time constants contributes to the noise. Trapping accounts for the charge lost in the first pulse, and trapping with subsequent release smears the signal (Séquin and Tompsett, 1975).

The temperature of the device also affects the CTE. At temperatures above 80 K, high thermal-generation currents preclude operation of the device. As the temperature is lowered, effects of tunneling and thermal dark current are reduced. Most of the measurements of this device were made at 64 K. The CTE is roughly independent of temperature between 64 and 77 K and was ≤ 0.992. At 51 K and 27 K, the CTE was $\leq .987$ and at 6.7 K it was $\leq .975$. Since the device is difficult to optimize, it is not clear at what temperature the CTE gets noticeably worse. It doesn't decline much (if at all) between 77 K and 27 K, but was clearly poor when the CCD was cooled to 6.7 K. At lower temperatures, greater (i.e., more negative) potentials on the clocked gates were required to sustain charge transfer. Tests at both SBRC and Ames showed that the 64 K device threshold voltages shifted by about -1 V at helium temperatures. Clock potentials had to be adjusted by significantly more than 1 V at these temperatures, indicating to us that the surface hole mobility decreases with temperature in this range.

We have observed a degradation of CTE with time. A CTE of 0.994 at 64 K was achieved early in the test program, but recently we have not been able to achieve levels as good as 0.99. A recent CTE value was 0.983 at 50 K. This degradation is apparently due to a change in the various non-uniform charge

trapping mechanisms previously discussed for this device (Thom et al., 1979). It tends to discount the explanation that trapping is caused by oxide granularity (same ref.), since it is hard to conceive of gross changes in granularity over time.

C. Noise

The effective interface state noise, N_{IS}, associated with ε can be calculated from

$$N_{IS} = (\Delta N_{SS}^2)^{1/2} = (k\,T\,A_S\,N_{SS}\,\ln 2)^{1/2}$$

where $N_{SS} = \varepsilon / \left(\frac{\gamma q kT \ln (p+1)}{C_{ox}\,\Delta\psi_s} \right)$ (Séquin and Tompsett, 1975), $\gamma = (A_S - A_{FZ})/A_S$ is the fat zero removal factor , A_S is the gate area swept out by the charge packet, A_{FZ} is the gate area swept out by fat zero, N_{SS} is the effective surface state density, k is Boltzmann's constant, p is the number of phases (4), C_{ox} is the gate oxide capacitance, and $\Delta\psi_s$ is the change in surface potential at the CCD gate due to injected signal which is chosen to be that at full well capacity (0.6V). At T=50.5 K, $N_{SS} = 5.6 \times 10^{12}/cm^2$ eV and $N_{IS} = 471$ charges. N_{IS} is larger than the MOSFET channel noise N_M calculated from $N_M = (kTC_0/2)$ where C_0 is the capacitive burden. For $C_0 = 3.5pF$, $N_M = 218$ charges.

At all times noise in this device is dominated either by pickup (60 Hz) or when pickup is minimal, by the MOSFET output amplifiers. As 60 Hz pickup is not inherent to the device, but is introduced by the measurement system, we will not discuss it other than to mention that because of the aliasing effect introduced by digital sampling techniques, (i.e., because the device is clocked and read out), severe precautions must be exercised by the experimenter in eliminating all pickup.

For most of the noise measurements either of two noise measurement systems is used. One is the 9825A calculator with A/D converter running with an unlimited electrical bandwidth. Because the device is dominated by 1/f type noise, bandwidth limiting is not required. The other system is a Nicolet 446A FFT Spectrum Analyzer with either an Ithaco 4211 bandpass filter or an Ithaco

1201 low-noise preamp. The former system yielded only rms noise voltages while the latter gave both rms noise and spectral noise voltage density.

The most illuminating noise measurements were those made as a function of temperature, when turning the output gate (V_{OG}) on and off. This procedure separates the effects of the InSb/SiO$_2$ CCD gates from those of the output amplifiers which are Si/SiO$_2$ MOSFET amplifiers. The results are given in Table 1. In the useful range of operating temperatures (< 60 K) the noise is dominated by the noise of the output MOSFETs. Figure 12a is a log-log plot of noise vs. frequency with V_{OG} = 0 volts, and therefore represents the noise spectrum of the output circuit. Figure 12b is the same plot with V_{OG} on, so that the CCD is transferring charge to the output circuit. (Note that in Figure 12 the integrated noise in the output section of the array (1030μV) was measured to be higher than that of the entire array system (970μV). This is attributed to a shifted operating point for the output FET. In other tests it was found that the output-section noise was less than system noise). Aside from the 5 Hz noise peak (aliased 60 Hz), the two plots are the same. Most of the noise is at low frequencies, although the rise to low frequencies is slower than 1/f. The minimum at 120 Hz is due to the digital sampling of the output.

The best measured noise voltage V_n was about 160μV rms, which corresponds to 3500 charges. However, on most occasions, due to the device's sensitivity to clock settings and dc potentials, the noise level was in the range of 5000-6000 charges. This noise level is far in excess of the statistical fluctuations one would expect to see from a nearly-full well being read out by an ideal noiseless amplifier. If Q_S is the charge generated by a signal in the well, then the output signal level is $V_O = Q_S/C_O$. The well capacity $Q_{S_{max}}$ is

$$Q_{S_{max}} = C_O V_{O_{sat}} = 3.5 \text{ pF} \times 25 \text{ mV} = 8.75 \times 10^{-14} \text{ coul.,}$$

so, $N_{S_{max}} = 5.5 \times 10^5$ charges

and, $\sqrt{N_{S_{max}}} = 740$ charges << 6000 charges = $V_n C_O$.

$V_{o,sat}$ can be as much as 50m⋅⋅ under certain tuning conditions which would raise the values of $N_{s_{max}}$ correspondingly.

Because 1/f noise dominates the readout of the CCD at low frequencies, it is apparent that long integration times will cause the readout noise to increase and to preclude improvements of S/N ratio with increasing integration times. This will cause the S/N ratio of faint objects which require long integration times to be inferior to that which would have been deduced on the basis of a bright object which can be read out at a faster rate.

D. Responsivity

Detector response was measured at three temperatures, 64, 27.2, and 6.9 K. To compare the three measurements, we calculate the responsivity (R) in amps per watt as observed on the CCD output. First we note that

$$V_o = \frac{gQ_o}{C_o}$$

where V_o = output voltage, g = FET gain = 0.9, and Q_o = output charge. The output current is $I_o = Q_o/t$ where t = integration time. So, the responsivity R is

$$R = I_o/P = \frac{V_o C_o}{g} \frac{1}{tP}$$

where P = power on the detector. The measurements were:

$$R = 0.31 \text{ A/W at 64 K}$$
$$= 0.35 \text{ A/W at 27.2 K}$$
$$= 0.47 \text{ A/W at 6.9 K}$$

The quantum efficiency, η, can also be calculated from the measured response V_o and photon flux, $\dot{N}$, on the detector.

$$\eta_{meas} = \frac{C_o V_o f_s}{\dot{N}q} = 0.38 \qquad \text{at 6.9 K and for a 673 K}$$

blackbody, where f_s is the sampling frequency ($f_s = 1/t$), and q is the elementary charge. Another method of calculating the quantum efficiency is to compare the measured responsivity with the theoretical value:

$$R_{th} = 0.804 \lambda \, (\Gamma \eta_{th}) \text{ in amps/watt}$$

where λ is the wavelength in μm and Γ is the photocapacitor charge collection efficiency. At 2.7μm, $R_{th} = 1.96$ A/W for $\eta = 1$ and $\Gamma = .9$. Then $R_{meas}/R_{th} = \eta$. In the listing above R_{meas} varies with temperature from .31 to .47 A/W. Using R_{meas} (6.9 K), $\eta = 24\%$ which is lower than expected. There is a loss factor, A_d, of 0.67 which arises from the low output diode resistance. Correction for this factor raises η to between 28 and 36%.

Detector response versus photobias (most negative value of ϕ_P clock) was also measured and shown in Figure 13. While integrating, the photobias is held at a dc level and clocked "off" during transfer of the charge to the CCD shift register to aid in pushing out all the charge. Response increases approximately linearly with increasing bias, until saturation of the well is reached. Then, the measured response falls off as dark current rapidly fills the wells. Performance is also affected by the value of the off voltage. Best response was measured for a bias of -5 volts and an "off" voltage of -3 volts.

Measurements of the uniformity of responsivity across the array were attempted, but the poor CTE effectively smeared out this information. Thom et al. (1980a) present data showing the NEP of all detectors falling within ± 36% of the average; the standard deviation of their distribution was 17% of the average. Our measurements appeared to be quite consistent with these results.

The normal readout mode is to set the output diode to a negative potential with the reset FET and ϕ_{RST}, and then detect the positive charge carriers as they are clocked into the output diode. One problem is that a large feedthrough pulse occurs when ϕ_{RST} clocks off, which fills a large fraction of the well under the output diode. We found that the output voltage was limited to 50mV with ϕ_{RST} on, but it could be twice as large if ϕ_{RST} were off. This is due to the absence of a reverse bias flatband region for the output diode. The

low diode resistance under large reverse bias contributes to low voltage response to the CCD output charge.

E. Dark Current

We examined the origin of the dark current, i_D, by measuring its magnitude with respect to different gate voltages. Dark current polarity was independent of any parameter which was varied, indicating that electrical leakage did not contribute to the dark current. ϕ_P and ϕ_T were the only voltages which significantly affected i_D. Photons were not a concern as the IR filter limited photo-generated carriers in the substrate to insignificant levels ($<10^7$/sec).

Dark current generation in the substrate has a minimum value for the device in the 30 to 50 K temperature range. At higher temperatures, thermal generation of carriers is the dominant mechanism; at lower temperatures, thermal generation is insignificant. The CCD works in the electrical configuration without much degradation in performance down to at least 5 K, yet significantly increased dark current at 5 K is observed in the optical mode. In Table 2 we indicate the dark current at a tuned operating point for various temperatures. At each temperature the dark current is found to be linear versus integration time.

F. Linearity, Stability, Crosstalk, Fill and Spill Input, Fat Zero

Three device characteristics which are important for astronomical applications are linearity, stability, and crosstalk. We made rough evaluations of each of these properties and found that only the linearity was acceptable for low background applications.

Linearity was checked by looking at a blackbody source for various integration times. Since the input power was constant, the CCD output should have been a linearly increasing function of time. This is observed (Figure 14) for integration times for which the photocapacitors' wells were less than half full. For wells more than half full, the response was nonlinear.

Stability with time was checked by looking at a blackbody source for several hours and measuring the signal at intervals of roughly one hour. In general, the stability was reasonably good; we could usually keep the CCD tuned up for a few hours at a time. However, on occasion, both the dc level and the signal level varied so drastically that by the end of the test (four hours), the signal had disappeared. The likely cause of this poor performance was drift in the clock and dc voltages by small amounts, and an operating point where the device was extremely sensitive to a few of the clock and d.c. voltages.

Electrical crosstalk is high due to poor charge transfer efficiency. With the best CTE observed (.994), 40% of the charge is lost in traversing the length of the CCD, and this lost charge is picked up by the following pulses. More typically CTE = .987, and 67% of the original charge was lost and mixed with subsequent pulses. This means that for most of the output pulses, only 1/3 of the output signal is original information, and 2/3 is crosstalk from other channels. Optical crosstalk was evaluated in the telescope test and found to be small (see Section G below).

We tried a fill-and-spill input technique (Tompsett and Zimany, 1973) for injecting fat zero into the CCD. This should be a more accurate method of metering the fat zero signal than the clocking method we generally used, and could reduce noise due to changing fat zero levels if it is a problem. We saw no improvement with the fill-and-spill input since we were MOSFET noise dominated and could not detect fluctuations in the transferred charge.

The amount of fat zero was varied to examine the effect on CTE. SBRC had reported that a fat zero of 12% of full well capacity was sufficient to fill all the trapping states which would degrade the CTE. We did not notice any further CTE improvement with fat zero set above 15% of well capacity.

G.   Telescope Test

The CCD was mounted on the NASA/Univ. of Arizona 60" telescope on Mt. Lemmon, AZ, to compare its performance with that of an optimized single InSb detector system. The two systems are described in Table 3, and the image of α Lyra on the array is shown in Figure 15. We used a borosilicate glass lens

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with a 7mm focal length to reimage the incoming f/20 beam to f/4. We estimate that 30% of the image fell on detector 5, and that the lens attenuated the signal by a factor of 2. Thus, to compare the two systems, the S/N for the CCD should be multiplied by 6 to give S/N = 500. This is 40x worse than the optimized single detector. The CCD noise we measure is a factor of two more than for the background limited system, which is the practical limit one would attain if the output MOSFET noise were reduced. The greatest factor comes from the large output capacitance of the MOSFETs relative to the CCD gates. This is 0.2 pF for the CCD gates vs. 3.5 pF for the output MOSFETs, which results in a signal voltage loss of 18x. Since the noise comes from the output MOSFETs also, this results in a S/N loss of 18x. These two factors combine to give a factor of 36, which is close to the observed factor of 40. We conclude that the detectors on this device are good, but the CCD readout requires substantial improvement.

We calculated the NEP of the CCD using the following assumptions:

α Lyra flux at 2.1μm = 3.8×10^{-14} W/cm^2 μm (Johnson, 1966)
$\Delta\lambda$ = 0.2μm
Telescope Area = 1.8×10^4 cm^2
System transmission = 0.2
Chopper efficiency = 0.5
Fraction of spot area on detector = 0.3.

Using these values,

Power on detector = 4.2×10^{-12} W.

Since S/N = 84 in 1 second, NEP = 7×10^{-14} W/$\sqrt{Hz}$. For a comparison with our earlier measurements at 2.7μm, the wavelength dependence of responsivity must be included. Assuming a first-power responsivity dependence,

$$NEP_{2.7} = (7 \times 10^{-14})(\frac{2.1}{2.7}) = 5.4 \times 10^{-14} \text{ W/}\sqrt{Hz}.$$

This is somewhat worse than our laboratory results of 4×10^{-15} W/$\sqrt{Hz}$, which were measured at 50 Hz. The difference in NEPs is reconciled in large part by low-frequency operating point (2 Hz) used at Mt. Lemmon. This is in a regime where 1/f noise is dominant. Other contributing factors include the uncertainties in the above calculation, the limited time available for optimization on the telescope, and elevated background noise due to humid

observing conditions. Optical crosstalk was checked on the telescope by looking at the focused image of α Lyra on the array. As can be seen from the sharp cut-on of the signal between channels 4 and 5 in Figure 14, there is no indication of any crosstalk greater than 10%. The signal in channel 4 is most likely due to spillover of the star's image, i.e., the image size was larger than the pixel size. The larger signals in channels 6 and 7 are a combination of illumination from α Lyra and smearing of the image due to poor CTE. Imaging near the CCD's last detectors (15-20) produced heavily smeared images.

IV. Device Characterization

A. Figure of Merit

When we speak about the figure of merit for this device or any similar device, we must keep in mind whether we wish to characterize the detectors or the integrated CCD device. From a user standpoint, detectors are a component of the entire device which yields a responsivity R_D , but not, as we have seen, a noise quantity inherent to the detector itself. The noise is rather a characteristic of the FET readout. With this device, there is no way to break in at the detector-CCD interface and extract a detector characteristic. This situation can best be kept clearly in mind by specifying a hybrid figure of merit for all such devices. Rather than NEP we will define and use the parameter NEΠ.

For this device, the detector responsivity is given by

$$R_D = \frac{C_W V_O}{gtP}$$

in coul/joule (or amps/watt), as the photocapacitive detectors are inherently charge integrating devices. This is in marked contrast to the normal photoconductors and diodes which are current generating devices. Here, C_W is the well capacitance. This response to the signal is then read out into the output FET capacitance by the CCD, so there are gain factors due to the FET, which as usual, has a gain of

$$A_F = \frac{g_m R_s}{1 + g_d R_d} \sim = 0.9,$$

and a capacitive gain $A_C = C_W/C_0 = 0.2 \text{ pF}/3.5 \text{ pF} = 0.057$, where g_m is the mutual transconductance, g_d is the drain transconductance, R_s is the source resistor value, and R_d is the drain resistor value. The CTE gain, A_{CTE}, varies from 0.98 for the detector closest to the output diode, to 0.34 for the detector furthest from it, since $A_{CTE} = (CTE)^n$, where n is the number of transfers between the detector and output diode.

The hybrid device responsivity is quite a bit less than the photodetector's native responsivity, i.e., $R_{eff} = R_D \ (A_F A_C A_{CTE} A_d) \cong (0.009) R_D$ for the detector with n=82. So, the "gain" actually turns out to be a loss factor of 104. The most conspicuous portion of this loss is A_C.

For this device the noise read out is the integrated noise or baseband noise. This means that the readout integrates the spectral noise density $e*(f)$ from 0 to f_s, if the device is properly sampled. The noise is read out as a voltage

$$V_n = \left\{ \int_0^{f_s} \left[e*(f) \, \frac{\sin{(\pi f/f_s)}}{(\pi f/f_s)} \right]^2 df \right\}^{1/2}$$

This voltage can be converted to electrons per readout by multiplying by C_0/qA_F.

Our measurements of integrated noise indicate that this quantity is fixed, independent of clock frequency or integration time. Under all conditions, we obtain about 6000 charges of read noise. In this limit, where noise is totally dominated by the readout process, one can define a device figure of merit

$$NEI = \frac{C_0 V_n}{R_{eff}},$$

with the dimension, joules or watt-seconds. This is essentially the conventional NEP expression without the $\sqrt{2/t}$ noise bandwidth term. Again, it must be kept in mind that NEI is not a detector figure of merit, but one appropriate in an integrating array in which the responsivity is determined (in

part) by the detector material, and the noise is determined entirely by the readout device.

Laboratory measurements of NEπ at three temperatures yielded:

$$NE\pi = 1.9 \times 10^{-15} \text{ Ws at 65 K}$$
$$= 2.4 \times 10^{-15} \text{ Ws at 27 K}$$
$$= 2.5 \times 10^{-15} \text{ Ws at 6.7 K}$$

B. Improvements

There are several improvements required before this device would be usable for low background astronomy. The typical noise measured on the device is about 6000 charges. If the detector noise is statistical, then the noise should be approximately 1000 charges for a full well since the measured well size is about 10^6 charges. Thus, the readout noise is six times larger than the expected detector noise. The readout noise must be reduced to the point where it does not contribute significantly to the detector noise before integration increases the signal-to-noise.

Better CTE and ease of operation are important for making this device usable. To reduce the electrical crosstalk to 1%, the CTE (for 82 transfers) should be 0.9999. Such CTE's are common in silicon CCD devices, and are probably attainable in InSb after some development. Existing silicon CCDs are apparently not as sensitive to clock and voltage parameters as is this InSb device, so improvement in ease of operation seems possible.

Lower dark currents are also a necessity, especially when integrating on faint signals. Ideally, one wants to integrate until the wells under the detectors are at least half full. Such times could be hours for faint objects. The present device cannot integrate for more than a few tens of seconds before the wells are filled by the dark current. SBRC reported in Thom et al., 1980a, that they have significantly better InSb in which they have measured much lower dark currents.

Improvement in readout performance can be obtained by using monolithic InSb MOSFETs, or a floating gate readout. The present device has a floating gate which is normally connected to ϕ_2, which might be adapted for this purpose. The gain factor A_c might be increased about a factor of two. Charge sensitivities as high as 3.5μV/electron have been reported (Séquin and Tompsett, 1975) in silicon devices. As this is a non-destructive readout, multiple readout averages can be used to advantage under low background conditions, where multiple readout time is much less than the long integration time.

V.   Conclusions

The InSb array's well size is not large enough to observe well statistics ($\sqrt{N}$ noise). The output noise was dominated by 1/f noise. In this case, the S/N ratio for faint sources is independent of integration time (Dobrov, 1980). This is a serious problem in any device using MOS-CCD technology. Theoretical considerations indicate less intrinsic noise from buried channel devices, so they should be considered for any application requiring low-level signal detection (Lynds, 1980).

$\sqrt{N}$ statistics might be seen at higher clock frequencies, where the 1/f component of noise no longer dominates. Then the device could be photon fluctuation limited for bright sources. There are certainly applications for devices of this sensitivity, for example, high background photometry or earth resource photometry. Most astronomical applications would require long integrations because of the low source brightnesses encountered. As no increase in S/N can be achieved with a 1/f noise dominated device there is no great advantage to using this array rather than an optimized single InSb photodetector. There are certain advantages which this array does offer, such as integrated detector readout structure and monolithic construction, but in astronomy these are not the most important criteria.

For astronomical applications, we would recommend that in future efforts in InSb array technology consideration be given to a buried channel CCD structure in InSb. Hybridized Si buried channel CCD devices are probably not compatible with InSb photodetectors as the latter works best at 30 K, whereas the former works best at temperatures in excess of 77 K. Such a hybrid device

might be constructed to operate well at 50 K. Si MOS CCD's would be unsatisfactory (although they would probably be better than the present "monolithic" device) because they too are 1/f noise limited.

Acknowledgments

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Table 1

Noise vs. Temperature

	rms Output Noise Voltage* (μV)	
Chip Temperature (K)	V_{OG} On	V_{OG} Off
50	873	815
7	970	1030
7 (ϕ_{RST} off)	1022	568

*Integrated noise from 0 to 200 Hz.

Table 2

Dark Signal vs. Temperature

	DETECTOR BIAS OFF		DETECTOR BIAS ON	
T of Chip (K)	Dark Voltage (mV)	Integration Time (sec)	Dark Voltage (mV)	Integration Time (sec)
7	-	-	50	0.2
32	30	16	50	1.6
50	-	-	50	3
54	-	-	50	0.12

Table 3

	InSb CCD	Optimized Single InSb Detector
System parameters:	10% spectral resolution filter Centered at 2.1μm Gain = 40 Glass reimaging lens, f/20 →f/4	2% spectral resolution CVF Set at 2μm Gain = 1 Fabry optics
Signal on α Lyra:	30mV in 40 msec. integration time.	500mV
Noise on Sky:	9mV/$\sqrt{Hz}$ (225μV/$\sqrt{Hz}$ with gain removed).	50μV/$\sqrt{Hz}$ (125μV/$\sqrt{Hz}$ at 10% resolution).
S/N at 10% Spectral Resolution in one second:	84	2×10^4
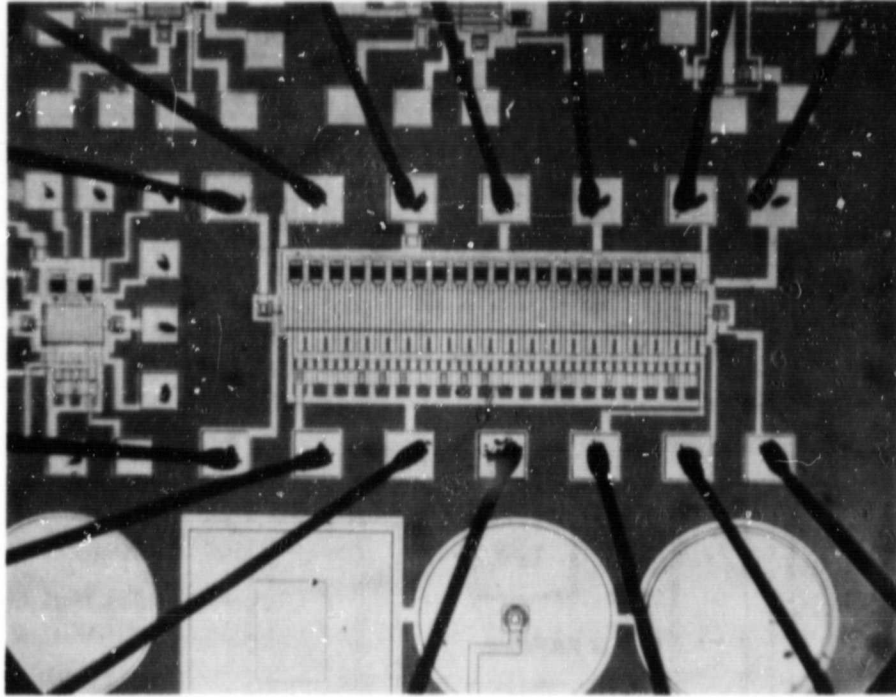
Fig. 1: A photograph of the 20-element CCD is shown. The large squares with wires are bonding pads. The small dark squares on the right are the photodetectors, and the horizontal bands in the middle are the CCD gates. Each detector element is 32.5μm by 35μm.
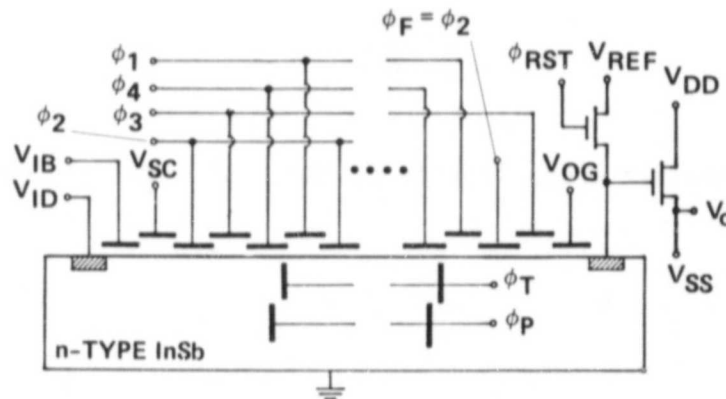
Fig. 2: This is an electrical schematic of the 20-element CCD. The notation is explained in the text. The representation of ϕ_T and ϕ_P is schematic; in actuality the T and P gates are on the same level as the other gates, but out of the plane of the paper. (Thom et al., 1979).

77K SHIELD

LN$_2$, LNa, OR LHa

ELECTRICAL FEED THROUGH

COLD BAFFLE

← 3 mm →

DETECTOR ARRAY

RADIATION SHIELD

FILTER/ APERTURE COMBINATION – VARIABLE (LINEAR MOTION)

SALT WINDOW (CnF$_2$)

CHOPPER
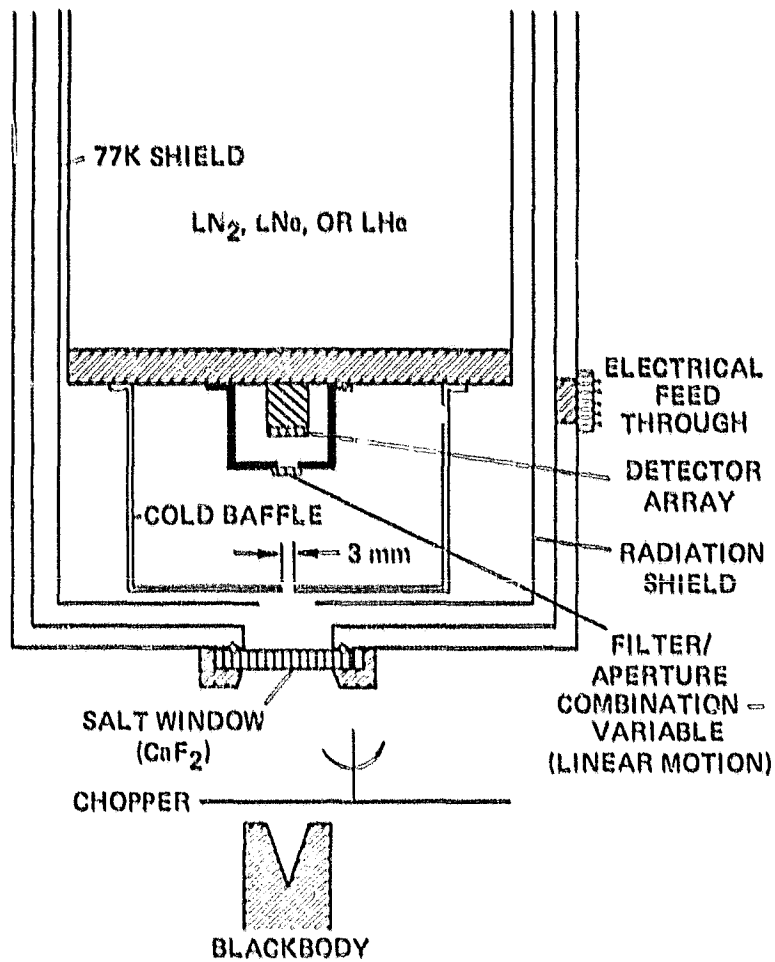
BLACKBODY

Fig. 3:   A schematic cross-section of the test dewar and optical arrangement.
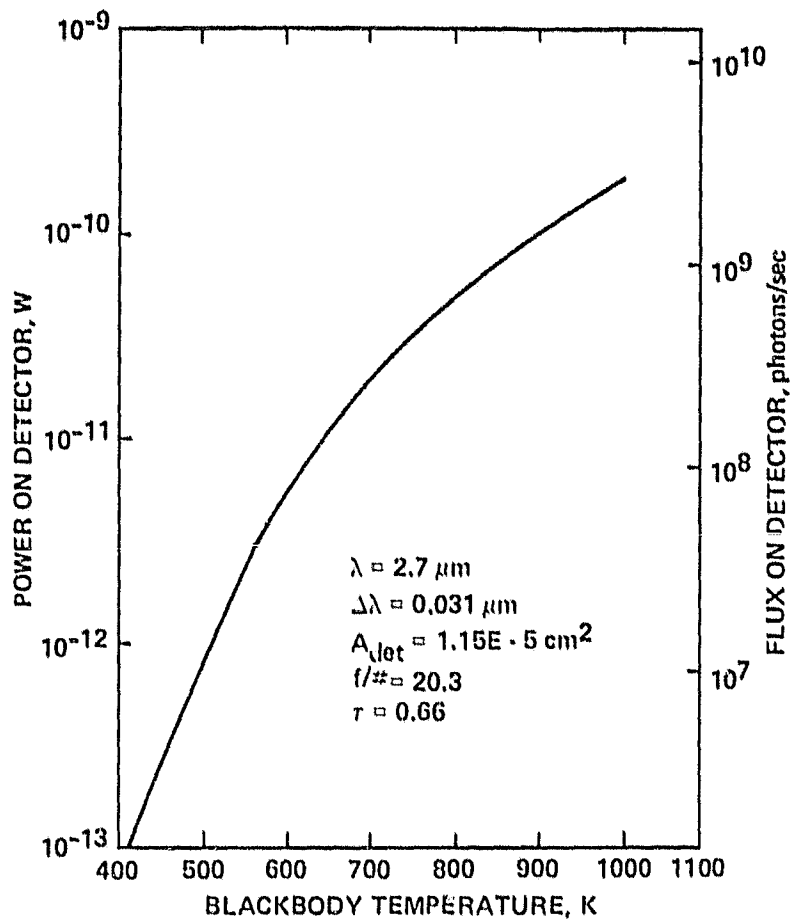
Fig. 4: Radiant power on a detector element as a function of temperature from the blackbody source indicated in Fig. 3.
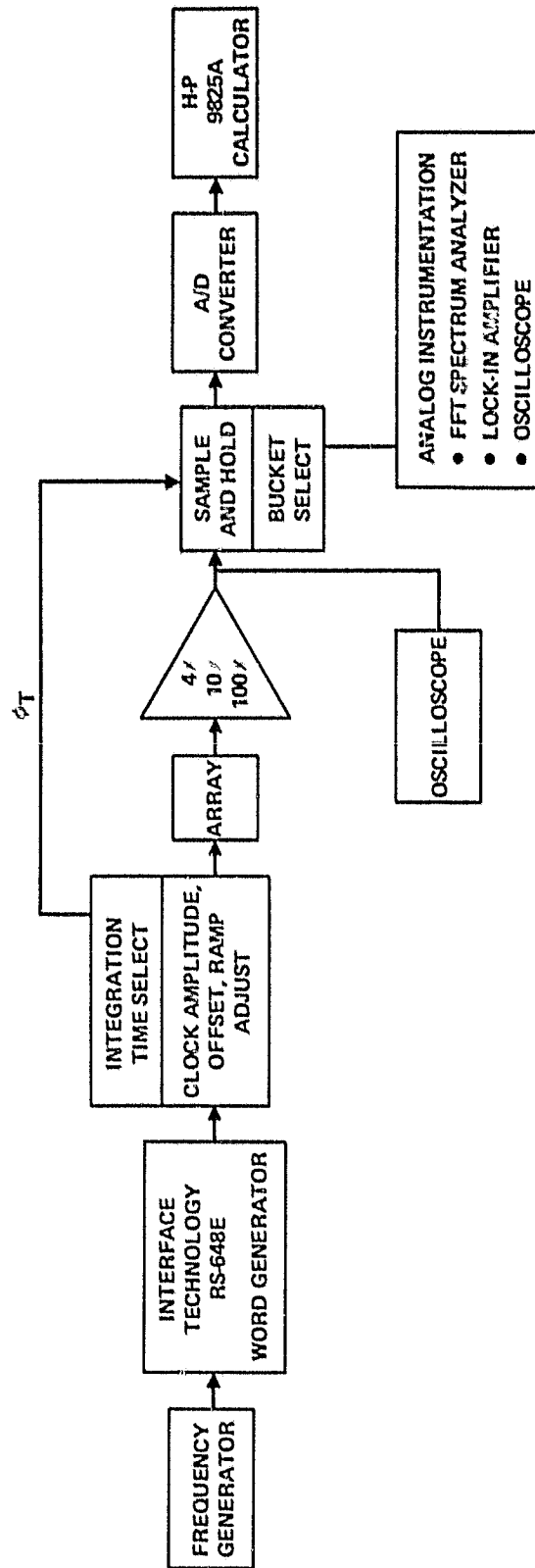
Fig. 5: The electronic block diagram of the test setup.
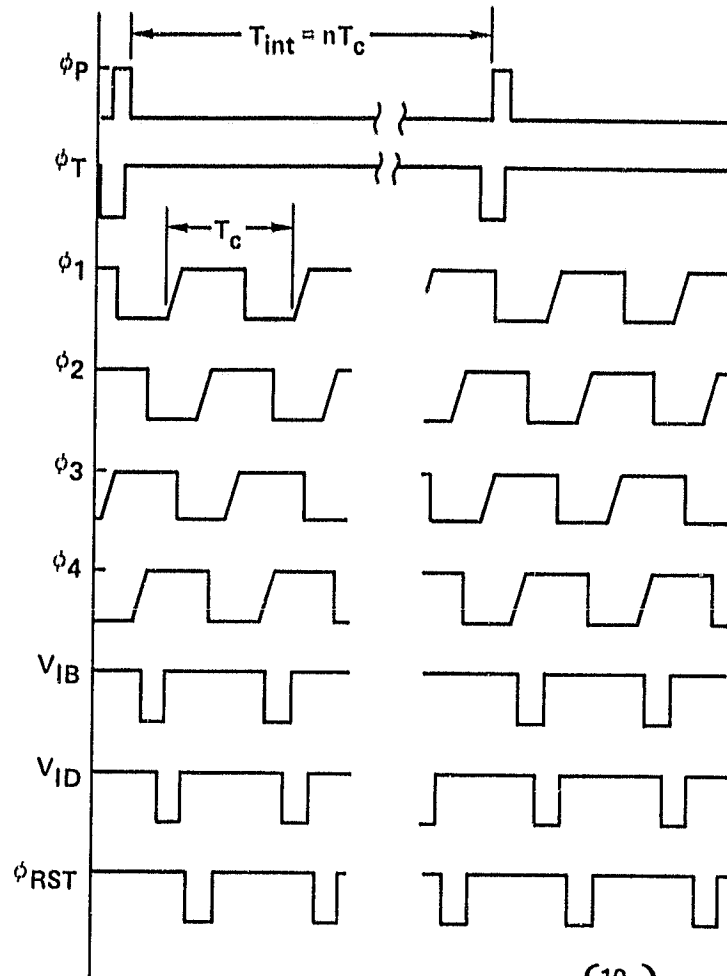
Fig. 6:   Clock timing diagram for the CCD.

Fig. 7

Fig. 8
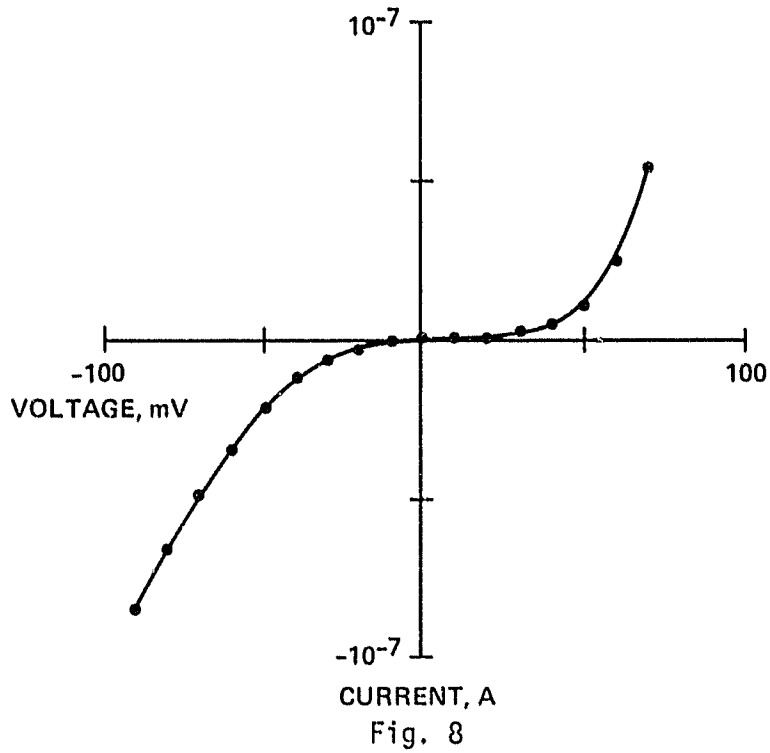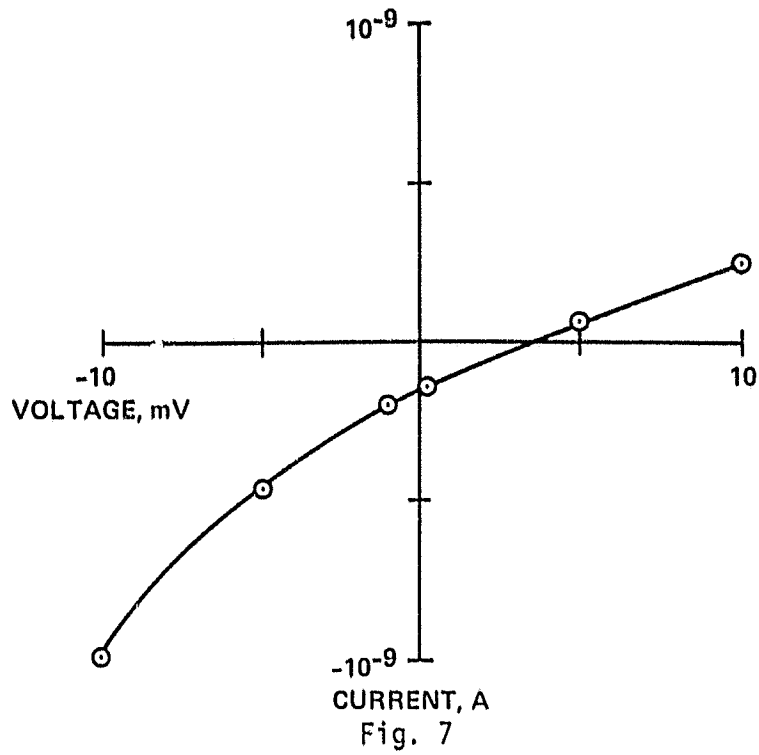
Fig. 7-8: I-V curves for the CCD output diode in 2 dynamic ranges. The
non-zero current at zero volts indicates slight photoactivity in the
output diode. Chip temperature = 65K.
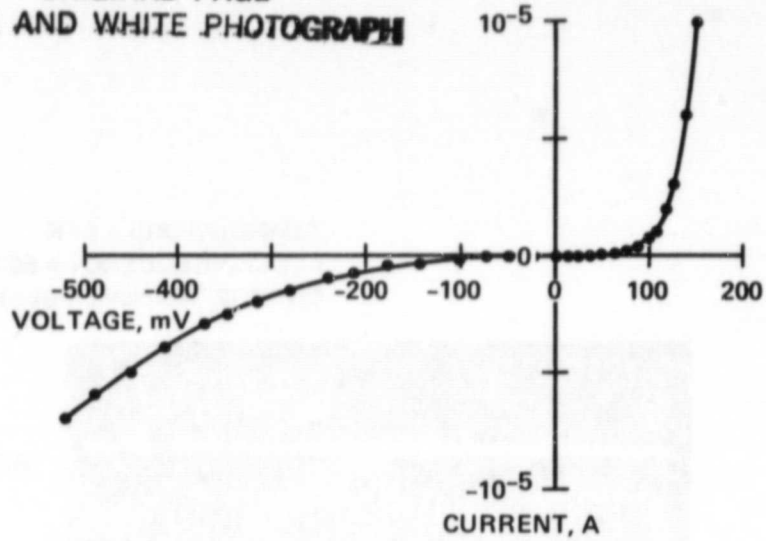
Fig. 9:   I-V curves for the CCD output diode over the range -500 to +200 mV.
Chip temperature = 65K.

InSb CCD ARRAY OPERATION/ELECTRICAL MODE

TEMPERATURE = 27.2 K
CLOCK FREQUENCY = 5 kHz
CHARGE TRANSFER EFFICIENCY = 0.984

INPUT PULSES
5 V/cm

OUTPUT PULSES
10 mV/cm

|←—1 msec/cm
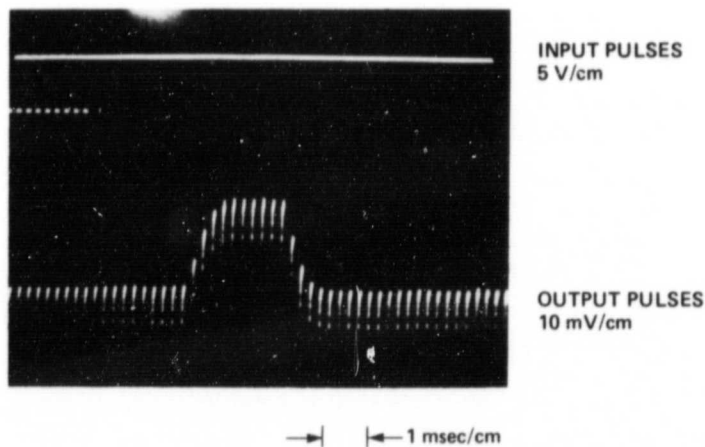
Fig. 10:   Typical CCD pulse train output at 27.2 K.

TEMPERATURE = 64 K
CLOCK FREQUENCY = 50 kHz
CHARGE TRANSFER EFFICIENCY = 0.994

INPUT PULSES
5 V/cm

OUTPUT PULSES
10 mV/cm

|←→| 100 μsec/cm
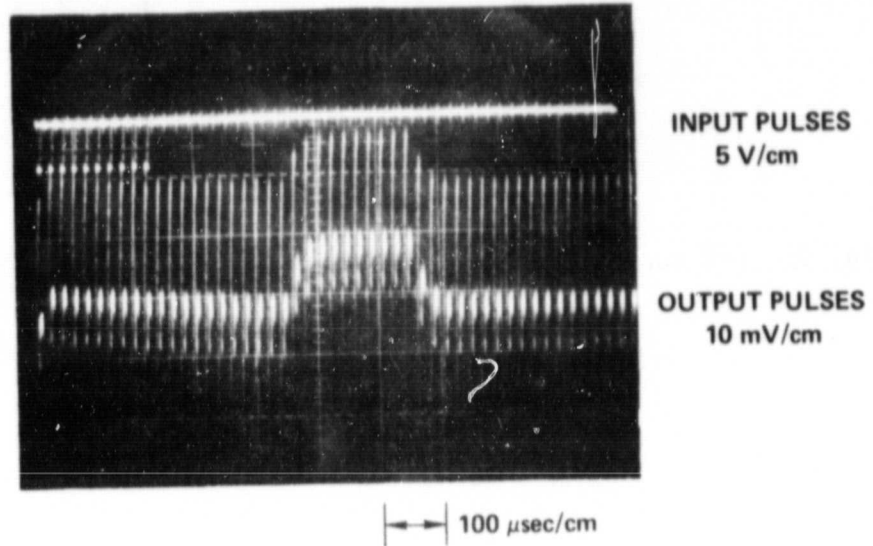
Fig. 11:   Best CCD pulse train output, at 64 K.
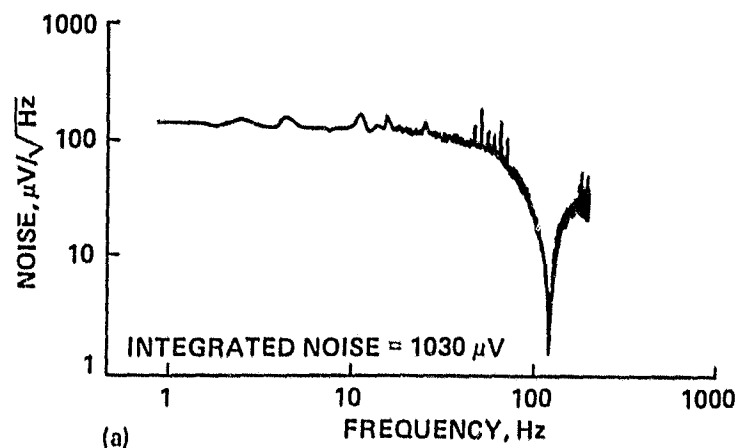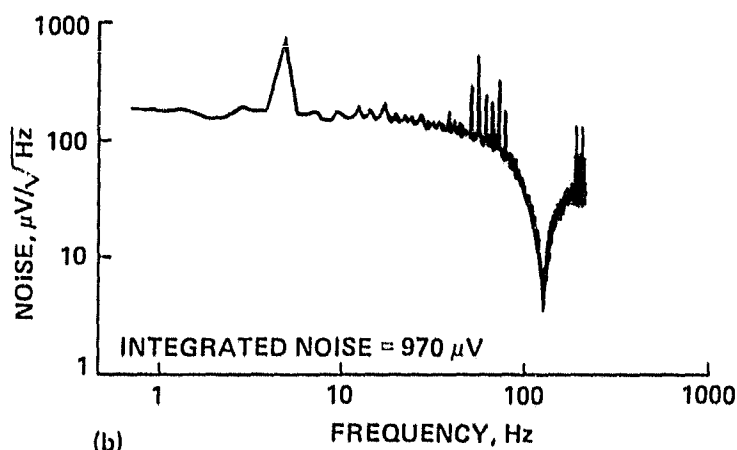
Fig. 12: Noise of CCD vs. frequency with CCD output gate off and on. The ˌ
were obtained under the following operating conditions: Temp. = 7 K,
clock frequency = 10 kHz, V_{REF} = -5.33V, ϕ_{RST} = -3.0 to -5.0V,
ϕ_p off, CTE = .987. The noise peak around 5 Hz is at a beat
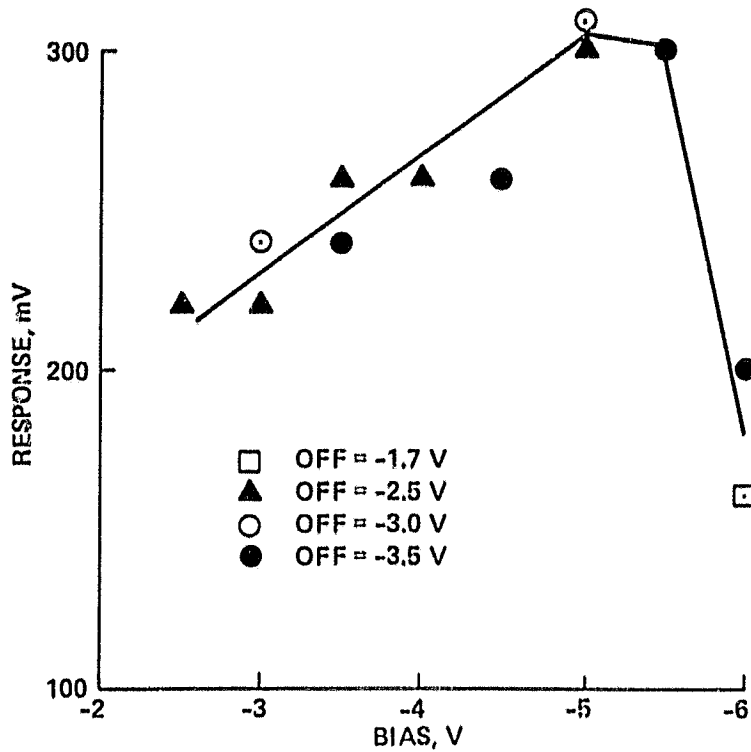frequency with 60 Hz pickup.

Fig. 13: Response of photodetectors to a constant blackbody signal vs. bias on the detectors. The term bias refers to the most-negative potential in the ϕ_p clock cycle. ϕ_p is clocked to a less-negative potential during charge transfer to the CCD, and these values are listed as OFF.
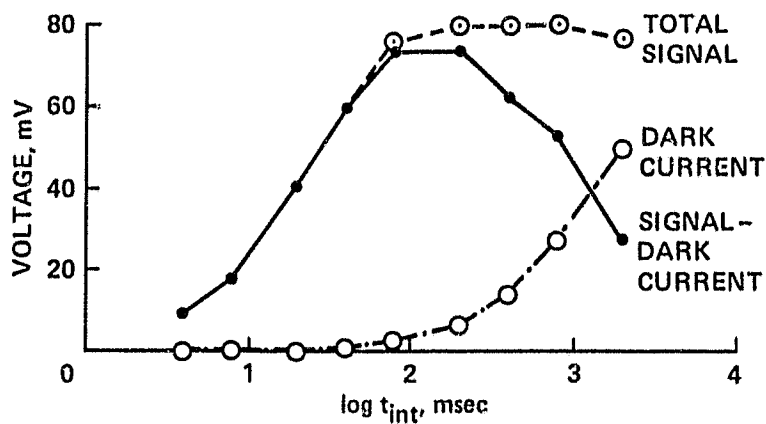

Fig. 14: CCD signal and dark current at 51 K as a function of integration time. The wells are full at 80 mV.

SYSTEM GAIN = 40
FREQ. = 10 kHz
INTEGRATION TIME = 40 msec
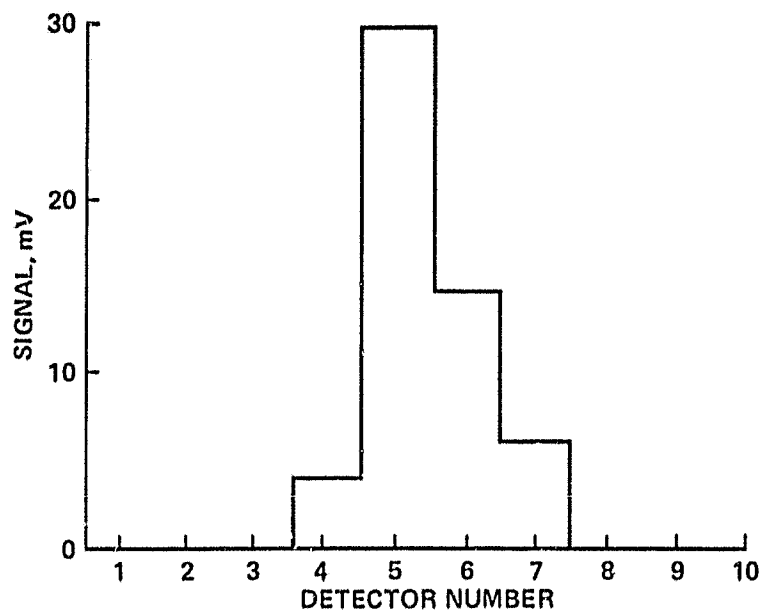**NOISE** = 9 mV/$\sqrt{\text{Hz}}$

Fig. 15: Response of CCD to the focused image of α Lyra at the NASA/U. of A. Mt. Lemmon 60" telescope.