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Final Report - Multiplexed Extrinsic Silicon Detector Array

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Final Report - Multiplexed Extrinsic Silicon Detector Array

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Section 1

INTRODUCTION

This program was undertaken to design, develop, and test multiplexed extrinsic silicon detector arrays (MESDAs) with their associated cryogenic and ambient-temperature electronics for delivery to Ames Research Center of the National Aeronautics and Space Administration and to Kitt Peak National Observatory for evaluation in astronomical applications.

Each array consists of two parallel rows of accumulation-mode charge-injection devices (AMCIDs) configured in a single bismuth-doped silicon chip. The cryogenic electronics consist of (a) timing and multiplexing circuitry for use in array addressing, and (b) impedance-matching circuitry for use in preamplifying the signals detected by each detector element. The ambient-temperature electronics encompass the components used to drive the timing circuitry, to amplify and demultiplex the signals, and to control the system.

Five arrays with their cryogenic electronics, and three ambient-temperature electronics control units, were delivered under this program.

Section 2

DESIGN

The MESDA system, shown diagramatically in Figure 1*, is composed of the detector array, some focal-plane cryogenic electronics, and ambient-temperature electronics for timing and drive use and for processing the signals of both linear arrays.

2.1 DETECTOR ARRAY

Each array consists of two parallel rows of AMCIDs fabricated in a Si:Bi wafer. For each row, a transparent electrode forms a common readout-bus line on the front (incident) surface. Sixty-four gates over a native-oxide thickness of about 0.2 micrometer form the storage and injection gates on the back of the wafer. Figure 2 presents a cross-sectional view at one of the gates.

During accumulation, a positive bias is applied to the gate to store the photogenerated charge carriers (electrons). During readout, the gates are biased negatively to inject the electrons back into the substrate to the readout-bus line. The bus line is connected to the gate of a p-channel enhancement-mode cryogenic MOSFET operated in the source-follower mode. The stored charge is seen as a voltage change on the source of the MOSFET after readout.

The artwork for the front-surface metalization is shown in Figure 3. It includes a mask, electrically isolated from the readout-bus line, that defines the pixel area in one dimension. This mask, called the "top guard", is grounded to prevent crosstalk between the two rows. The metalization between the two rows is 0.25 mm wide.

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*All figures are presented at the end of the report text.

The artwork for the back-surface metalization incorporates gates and a guard electrode, called the "bottom guard", to define the pixel area in the orthogonal dimension. Each gate is about 0.18 mm square. The original artwork (Figure 4) was revised because charge accumulated under the gate of one array could spill over to the corresponding gate of the other array, causing crosstalk. This artwork was used on only one of the delivered arrays [designated as Serial No. (SN) 8101]. The other four delivered arrays, made with the revised artwork (Figure 5), have guard electrodes that completely enclose each gate electrode, thereby preventing crosstalk between the two rows.

The front side of each array is indium-soldered to the inside surface of a 32-mm-square 24-pin nickel-plated Kovar butterfly case as shown in Figures 6, 7, and 8. The case is slotted to provide access to the front side of the chip. Each case has three holes for feedthroughs used to connect the two readout-bus lines to the gates of the two cryogenic MOSFETs and to connect the top guard to one of the feedthrough pins of the case. The Kitt Peak cases (Figures 7 and 8) have an additional hole for spectral-analysis purposes.

2.2 CRYOGENIC ELECTRONICS

2.2.1 Preamplifier

Inside each case a cryogenic preamplifier is provided for each of the two readout rows. Each preamplifier consists of a low-noise p-channel enhancement-mode MOSFET operated as a source follower with a load resistor that has a resistance of about 3.2×10^7 ohms at 10 K. The MOSFET gain is about 0.80. Both preamplifiers are mounted on a sapphire substrate that has gold stripes for wirebonding purposes. The preamplifiers are wirebonded to the feedthrough pins of the Kovar cases with the pins as identified in Figures 6, 7, and 8.

2.2.2 Scanning Electronics

On the inside of each microelectronics case is a board for the electronics that multiplexes the injection (read) pulses to the 64 pairs of

gates. As shown in Figure 9, the board consists of a 4-bit up/down-counter chip (the MM54C193) and four 4-line to 16-line decoders (MM54C154) that are powered by external store (positive) and read (negative) voltages. All are complementary MOS (CMOS) chips, which require minimal power for operation. External clock pulses load the bits to the counter in the up direction while an external reset pulse clears the counter. External enable pulses are needed to trigger the decoders.

A timing diagram for one read frame is shown in Figure 10. The external clock causes the counter to count in the up direction on all four decoder chips. There is no output on the decoders, however, until enable pulses are applied to the enable inputs of each decoder. The enable pulses are externally clocked sequentially through the four decoder chips--i.e., the enable pulses are applied as follows: on the first chip during the first 16 clock pulses, on the second chip during the second 16 clock pulses, etc.

2.2.3 Heater and Temperature Sensor

Also provided in each microelectronics case are a 100-ohm wire-wound resistor that can be used to heat the case, and a 5.6-kilohm carbon-glass resistor used as a temperature sensor. Calibrations for each temperature sensor are given in Section 4.4. If the heater is employed, then either the case or the heat sink to which it is attached must be isolated thermally from the cold finger of the Dewar vessel. Stainless steel screws and washers can provide the required thermal resistance.

2.3 AMBIENT-TEMPERATURE ELECTRONICS

The ambient electronics consist of two entities--a signal-conditioning amplifier (SCA) and an electronics control unit (ECU).

2.3.1 Signal-Conditioning Amplifier

This equipment was designed around the 5534 operational amplifier. It is shown schematically in Figure 11, and a component layout is presented in Figure 12. Two amplifiers, one for each channel, were constructed in a cast-aluminum case to permit placement at close proximity to the test Dewar

containing the MESDA array. Each SCA has a gain of 200 from 700 Hz to 50 kHz. Included in the aluminum case are the source supplies for the two cryogenic MOSFETs.

2.3.2 Electronics Control Unit

The ECU contains the bulk of the ambient-temperature electronics. It provides the timing and drive functions for the scanner, the sample-and-hold circuitry used in measuring the AMCID output, and the controls for the focal plane electronics. The major components are identified in Figure 13, and Section 4 describes the operation of the unit in detail.

2.3.2.1 Timing and Drive

The timing and drive circuitry is on Boards 1, 2, and 3. (Figures 14 and 15 present schematics for Boards 1 and 2.) A pulse generator provides the clock input for the 4040 counter (IC1). By selecting N = 0 to 7, the 4051 multiplexer (IC4) divides the clock-pulse frequency by 2^N. The resultant clock is fed into the 74C193 4-bit counter (IC7) and is then sent via the 4035 shift register (IC14), the 4011 quad NAND gates (IC16), and the two DG303 analog switches to generate enable pulses for the cryogenic scanner.

The output of IC7 is also fed into the 74C154 4-bit to 16-bit decoder (IC8), which is always enabled. The outputs of this decoder are sent to the 4067 16-channel multiplexer (IC6). By choosing 1 of 16 positions on a selector switch, the digital-synchronizing pulse is selected on that pixel. The output of IC4 is also sent to two more 4040 clocks (IC2 and IC3), whose outputs are routed to the inputs of another 4067 multiplexer (IC5). By selecting M = 0 to 15, a delay time is introduced before the 74LS76 dual J-K flip-flop (IC11) is loaded. This delay time is (2^M-1) times the time for one readout frame. The integration time is thus the sum of the read and delay times—i.e., $\left[2^N + 2^N(2^M-1)\right]$ times clock time = $2^M\,2^N$ times clock time.

The 4051 multiplexer (IC17) is used to select which of the four groups the SYNC SELECT is synchronized to.

One 75451 dual AND driver (IC23) is used to provide digital synchronization and another (IC24) is used to provide dc-restore and sample-and-hold (S/H) pulses for the S/H circuitry. Further details are provided in paragraph 2.3.2.2, below.

A potentiometer on Board 3 is connected to IC19 to vary the width of the read-enable pulse. Another potentiometer on Board 3 is connected to IC22 to vary the delay in the S/H pulse.

A 7400 quad NAND gate (IC13) is used as an OR gate to allow the S/H circuit to function on all the pixels (S/H ALL) or on just one pixel (S/H SELECT).

2.3.2.2 Sample and Hold

Figure 16 presents a timing diagram for the S/H function. The dc-restore pulse sets a reference level for measurements. The S/H pulse can be delayed to any part of the read-enable pulse. Here it is appropriate to define Δs as the time interval between the end of the dc-restore pulse and the end of the S/H pulse, as illustrated in Figure 16.

The S/H circuitry is shown schematically in Figure 17, and a component layout is presented in Figure 18. The dc-restore and S/H pulses from the timing and drive functions are coupled to the S/H circuitry with the HPL 2630 optical isolator (U6). The digital synchronizer is used to produce analog synchronization via another HPL 2630 optical isolator (U7). Electrical isolation of the analog and digital electronics is crucial for maintaining low noise in the output stages. A pair of HA2425 sample-and-hold operational amplifiers (U1 and U2) provide the S/H function, while LH0002 current amplifiers (U3 and U4) can drive an output of 200 mA with a 50-ohm load.

2.3.2.3 Focal Plane Control

The ECU also contains the controls for two of the focal plane components—the heater and the bottom-guard voltage. The heater power is tapped off the -15 V supply as shown in Figure 17. The bottom-guard voltage is powered from the analog voltage supply on the back panel.

Section 3

TESTING AND PERFORMANCE

For test and evaluation purposes it is convenient to partition a MESDA system between the ambient electronics and the cryogenic AMCID arrays.

3.1 NOISE IN AMBIENT ELECTRONICS

After the first AMCID-array/SCA/ECU set was constructed, noise spectra and signals were measured with amplifier bandwidths of 30, 50, and 80 kHz and with Δs (as defined in paragraph 2.3.2.2) set to 10, 12, and 14 microseconds, in order to determine the optimum amplifier configuration. A typical plot is shown in Figure 19. Table 1, below, summarizes the signal, noise, and signal-to-noise ratio (S/N) data. The MOSFET gate capacitance is 5.7 pF. On the basis of the results, a compromise 50-kHz bandwidth was selected for all three amplifiers. It can be seen that operation at lower backgrounds may benefit from the use of smaller Δs values to minimize noise.

Noise spectra of the warm electronics were measured with the S/H input and the amplifier input shorted. Typical data are shown in Figure 20; they indicate that the noise contributions of the S/H circuit and the amplifier are significantly smaller than those of the cryogenic preamplifier (see Figure 19).

3.2 DETECTOR ARRAY

3.2.1 Responsivity

The infrared response of each detector array was checked under low-background conditions using an indium antimonide light-emitting diode (LED) source. Whenever possible, response was measured as a function of LED current [i.e., photon (ph) fluxes (ϕ)], temperature, store voltage (V_S), read voltage (V_R), guard voltage (V_G), integration time, Δs, and sampling frequency (F_s). Because no satisfactorily responsive arrays were fabricated until

TABLE 1 SIGNAL AND NOISE FOR FIRST AMCID-ARRAY/SCA/ECU SET

Parameter	Values at Indicated Amplifier Bandwidths		
	30 kHz	50 kHz	80 kHz
Δs = 10 μsec			
Signal, V	7.4×10^{-3}	9.0×10^{-3}	1.0×10^{-2}
Noise, V	6.0×10^{-5}	7.5×10^{-5}	9.0×10^{-5}
S/N	122.3	120	111
Δs = 12 μsec			
Signal, V	7.2×10^{-3}	8.8×10^{-3}	8.9×10^{-3}
Noise, V	6.5×10^{-5}	1×10^{-4}	1×10^{-4}
S/N	111	88	89
Δs = 14 μsec			
Signal, V	7.0×10^{-3}	8.0×10^{-3}	8.0×10^{-3}
Noise, V	8.0×10^{-5}	1.0×10^{-4}	1.1×10^{-4}
S/N	88	80	72.7
Average Noise <e>, electrons/sample			
Δs = 10	193	241	290
Δs = 12	209	322	322
Δs = 14	257	322	354

several months after the originally scheduled delivery dates, early delivery of these working arrays became of paramount importance, and only cursory checks were made on most of the arrays. Figures 21 through 25 present typical data for the five arrays. Table 2, below, summarizes the average current responsivity (R_I, in amperes/watt), and the operability of all pixels (gate pairs).

3.2.2 Noise

Under low-background conditions the limiting noise is that of the cryogenic preamplifier. Because all output MOSFETs were selected for their very low noise characteristics, the cryopreamplifier noise is dominated by the Johnson noise of the load resistors. The fact that all the load resistors were selected to have nearly identical values caused the limiting noise

of all the arrays to be likewise nearly identical. The noise shown in Figure 19 is thus typical of all the MESDA arrays.

TABLE 2 AVERAGE RESPONSIVITY AND OPERABILITY OF MESDA AMCID PIXELS

AMCID SN	Array SN	Average R_I (A/W)	Operability of Pixels
8101	225-9.6-7	1.0	Gate pairs 25, 26, and 60 inoperative
8106	225-7.7-2	1.2	All gate pairs operative
8107	299-6.7-4	0.8	Gate pairs 1, 22, 26, 41, 54, 56, 60, and 63 inoperative
8108	225-7.7-4	0.4	All gate pairs operative
8115	225-8.0-4	0.9	Gate pairs 24 and 64 inoperative

3.2.3 Relative Spectral Response

The relative spectral responses of the MESDA arrays were not directly measured. A typical relative spectral response for Si:Bi detector material is shown in Figure 26.

Section 4

ECU DESCRIPTION AND MESDA OPERATION

4.1 ELECTRONICS CONTROL UNIT

The ECU contains the electronics for the timing-and-drive (T/D) circuits, MOSFET preamplifiers, heater, and S/H circuits. It can be rack-mounted and requires power from two dual supplies (±15 volts, 500 mA). A pulse generator is also required for the T/D circuits. The ECU features are identified in Tables 3, 4, and 5, following.

4.2 INITIAL CHECKOUT

4.2.1 On-Focal-Plane Electronics (Cryogenic)

The scanner cannot be checked at room temperature because the detector is grounded to the can, which prevents the observation of read pulses through the preamplifier.

The preamplifiers can be checked by providing the source voltage to them and measuring that voltage. In proper operation the source voltage drops to about 4.5 V.

4.2.2 Ambient-Temperature Electronics

The array is not required to be at cryogenic temperatures in order to check out the T/D and S/H circuitry. The procedural steps are as outlined below.

4.2.2.1 Front Panel of ECU

a. Power Check: With none of the BNC connectors connected to the control panel, set the two external power supplies to ±15 V and switch the power-supply meter function to read currents. Now connect the digital power suppplies to the appropriate double GR connectors. The current draw on the +15 V supply should be about 260 mA; for the -15 V supply it should

TABLE 3 FRONT PANEL OF ECU

Label	Purpose/Function/Description
BNC Connectors	
CLOCK IN	Brings in timing pulses from an external pulse generator (2 microseconds to 50% duty cycle).
READ CLOCK	Sends timing pulses into the cryogenic counter.
RESET	Sends reset pulses to the cryogenic counter that are synchronized with the first pixel.
EN 1 (or EN 2 or EN 3 or EN 4)	Sends enable pulses to the decoder chip for the 1st (or 2nd or 3rd or 4th) group of 16 pixels.
STORE	Provides store voltage for the counter and decoder chips.
READ	Provides read voltage for the counter and decoder chips.
OUTPUT SYNC	Brings out a pulse synchronized with the digital electronics at the pixel chosen by the SYNC SELECT switch.
SAMPLE AND HOLD INPUT 1 (or 2)	Sends the output of Amplifier 1 (or 2) into the sample-and-hold circuit.
SAMPLE AND HOLD OUTPUT 1 (or 2)	Extracts the output of Sample and Hold Circuit 1 (or 2) for analysis.
TM	Takes the output of the temperature monitor to the digital volt-ohmmeter.
SYNC	Is synchronized with the digital electronics through an optical isolator.
Switches	
2^N	An 8-position thumbwheel switch used to set the interval between read pulses of successive pixels. This interval is 2^N times the base time set by the master clock (external pulse generator).

(continued)

TABLE 3 FRONT PANEL OF ECU (CONT.)

Label	Purpose/Function/Description
Switches (cont.)	
2^M	A 16-position thumbwheel switch used to set the interval between the last read pulse of a readout and the first read pulse of the next readout. This interval is (2^M-1) times the base time. Therefore, the total integration time is 2^N x (2^M-1) x base time.
P (or S)	Used to select parallel-mode (or serial-mode) readout.
EN 1 (or EN 2, 3, or 4)	Sends an enable pulse to the 1st (or 2nd, 3rd, or 4th) group of 16 pixels when reading out in the parallel mode. In the serial mode, these are overridden so that all groups are enabled sequentially.
RESET	Used to reset the counter to the beginning when an interruption is desired in a long integration-time interval.
S/H SELECT (or S/H ALL)	Switches on the sample-and-hold circuitry on a selected pixel (or on all pixels). In the SELECT mode, the pixel is the one indicated by the SYNC SELECT switch.
SYNC SELECT	A dual thumbwheel switch (one 4-position and another 16-position) used to select the pixel to which a synchronization pulse is synchronized. The second number displayed indicates the pixel group (1 through 4) and the first indicates a pixel (1 through 16) in that group.
HEATER OFF	Turns on or off (up or down) the power to the resistance heater in the Kovar can.
Potentiometer	
HEATER	Used to adjust the power supplied to the heater to regulate the temperature of the Kovar can.

TABLE 4 REAR PANEL OF ECU

Label	Purpose/Function/Description
BNC Connectors	
HT	Supplies power to the heater.
TM	Connects the temperature monitor to the control panel.
GD	Supplies bias (+15 V to -15 V) to any guard.
DC Rest.	A test point used to bring out the dc-restore pulse.
S/H	A test point used to bring out the sample-and-hold pulse.
Double General Radio (GR) Connectors	
+15A (-15A)	Used to connect a +15V(-15V) 100-200 mA supply for the analog circuitry.
+15D (-15D)	Used to connect a +15V(-15V) 100-200 mA supply for the digital electronics.
Unlabeled Winchester Connector	Used to connect the control box to the SCA.
Potentiometer	
GD ADJ	Adjusts the voltage supplied at the guard.

TABLE 5 ECU INTERIOR*

Label	Purpose/Function/Description
BNC Connector	
S/H	Used for looking at the sample-and-hold input after it has been dc-restored.
Switch	
1-ADJ/ONE (2-ADJ/ONE)	In the ADJ position, switches a gain potentiometer into the sample-and-hold circuitry for Channel 1 (or 2). The gain is adjustable from 1.5 to 2.0 times. In the ONE position, the gain is unity.
Potentiometers	
READ PW	Used in adjusting the read-pulse width.
S/H DELAY	Adjusts the delay of the sample-and-hold pulse.
1 (2)	Adjusts the sample-and-hold gain when in the ADJ mode.
*See Figure 13.	

be about 40 mA. Next connect the analog power supply. With the preamplifiers in operation, the current draw should be about 120 and 25 mA for the +15 and -15 V supplies, respectively.

b. STORE and READ Check: Connect the STORE output to a digital voltmeter (DVM) and adjust to +2.00 Vdc. Connect the READ output to the DVM and adjust to -2.00 Vdc.

c. READ CLOCK Check: Now connect an external clock ($\sim$5 V square-wave pulse at 64 kHz) to CLOCK IN. Connect the READ CLOCK output to an oscilloscope synchronized with the external clock. With N = 0 and M = 0, which gives the fastest integration time, the output should be 1- to 1.5-microsecond pulses of $\pm$2.00-Vdc height at 15.6-microsecond intervals.

d. RESET Check: Next connect the RESET output to the oscilloscope and synchronize internally. Because the reset pulse should come just before the first pulse, this output should be $\pm$2.00 Vdc, be 1 to 15 microseconds wide, and occur at 1-millisecond intervals.

e. OUTPUT SYNC Check: Next set SYNC SELECT to 1-1 and synchronize with the reset pulse. Look at the output of the OUTPUT SYNC (digital synchronization). Verify that this is a positive pulse going from ground to +2.0 Vdc, is 1 to 1.5 microseconds wide, and occurs at 1-millisecond intervals.

f. SYNC Check: Next verify that the (analog) SYNC is a negative pulse going from +5.0 Vdc to ground, is 1 to 1.5 microseconds wide, and occurs at 1-millisecond intervals.

g. EN Check: Next synchronize the oscilloscope with the OUTPUT SYNC and look at the enable pulses. Looking at EN 1 with the read-pulse-width (READ PW) control fully counterclockwise, the output should occur at 15.6-microsecond intervals, with the group of 16 pulses repeating at 1-millisecond intervals. The same should be true for EN 2, EN 3, and EN 4.

h. SYNC SELECT Check: Keeping the output of EN 4 connected to the oscilloscope and synchronized with the OUTPUT SYNC, change the SYNC SELECT setting to 16-4 (16th pixel of 4th group). A single pulse should be seen. Change the SYNC SELECT to 15-4; two pulses should be displayed. Continue reducing the first number of SYNC SELECT by increments of unity and observe that one pulse is added each time until 1-4 is selected. This procedure should display all 16 pulses of the fourth group.

i. 2^N and 2^M Control Check: With N and M set at 0-0, change SYNC SELECT to 1-1. Connect the EN 1 and RESET outputs to the oscilloscope to display alternately. Synchronize to OUTPUT SYNC. The time between the reset pulse and the first read pulse should be about 2 microseconds. Adjust the sweep of the oscilloscope to display two complete frames. Now change N to 1; the read time should double and (because the delay is unchanged) the total time for the entire frame will double. Consequently, only one complete frame will be seen in the time that two frames were seen before. Now change N and M to 0-1. The read time should be the same as for 0-0, but the delay time will be equal to the total read time ($2^M - 1 = 1$). The first train of read pulses will thus occur in the same time interval as when N,M = 0-0, but there will be a delay interval to replace the second train of N,M = 0-0.

j. DC-Restored S/H Input Check: Connect the EN 1 output to S/H inputs 1 and 2. With the oscilloscope synchronized to the analog SYNC, monitor the S/H BNC connectors inside the control panel. The read pulses should be 0 to -4 V.

k. S/H Slew Rate Check: With the S/H switch on the front panel in the S/H ALL position, increase the read-pulse width to 6 microseconds. Adjust the S/H pulse to sample where the read pulse reaches its maximum negative voltage. Now, looking at the S/H outputs, the output should go from 0 to -4 V within about 1 microsecond. The slew rate is about 5 to 8 V/microsecond. The output-voltage level should also return to zero after the previous read pulse.

4.2.2.2 **Rear and Interior of ECU**

The outputs in these locations can also be checked without the array and scanning electronics:

a. HT Check: Connect to a DVM. With the HEATER switch on the front panel in the up position, a potential of -15 V should be measured.

b. GD Check: Connect to a DVM. The voltage should be adjustable from -15 to +15 V by turning the guard (GD) control to its two extremes.

c. DC Rest. Check: Compare the dc-restore pulse with the read pulse, using an oscilloscope. The pulse width should be 1.0 to 1.5 microseconds, with a height of about 2.0 V. The dc-restore pulse should be set about 100 nanoseconds before each read pulse.

d. S/H Check: Compare the S/H pulse with the read pulse. The pulse width should be 2.0 to 2.5 microseconds, with a height of about 2.0 V. The S/H pulse can be set at 2 to 30 microseconds from the read pulse or at the start of the next read pulse, whichever is a shorter period.

4.3 **OPERATION**

4.3.1 **General Procedures**

After the initial checkout has shown that the ECU is operating properly, the following must be adjusted to the proper operating conditions:

a. The frequency of the pulse generator
b. The store voltage (STORE) } Do not exceed a 15-V
c. The read voltage (READ) } differential!
d. The read-pulse width (READ PW) ≈2 microseconds.

The following items are then connected to a cooled Dewar vessel containing the array: RESET; EN 1, EN 2, EN 3, EN 4; STORE; READ; and (on the back panel) HT and TM.

The timing pulses are monitored by means of one of the enable inputs. Here the digital OUTPUT SYNC should be used.

The preamplifiers are connected to the SCA. The common drain and the two loads are grounded. The power cable from the back of the ECU is connected to the SCA. The two sources are connected to the inputs (IN) of the SCA. The source voltage can be monitored here; it should be about 4.5 V. The outputs (OUT) of the SCA are connected to an oscilloscope in order to monitor the read pulses of the MESDA. The analog SYNC should be used to synchronize the oscilloscope.

Presuming that the operation is still proper, the outputs of the SCA are connected to the S/H inputs. The S/H BNC connectors on the sample-and-hold board are connected to the oscilloscope so that the dc-restored sample-and-hold inputs may be monitored. The S/H delay is adjusted with the S/H DELAY potentiometer to the desired amount. The S/H outputs are then connected to the oscilloscope or to other data-collecting equipment for measurements.

At this point the sampling rate may be adjusted. The temperature of the array should be monitored, because higher sampling rates result in higher heat loads.

4.3.2 Precautions

It is emphasized that the differential values of the store and read voltages must not exceed 15 V or the scanner may latch up.

The READ CLOCK must always be connected last and be disconnected first, to prevent possible CMOS-chip destruction.

To maintain separate grounds for the analog and digital electronics, the OUTPUT SYNC should be used when digital electronics are monitored and SYNC (near the HEATER OFF switch) should be used when analog electronics are monitored.

4.4 TEMPERATURE-SENSOR CALIBRATION

The temperature sensors are carbon-glass resistors with nominal room-temperature resistances of 5.6 kilohms. Each was calibrated at cryogenic temperatures. The results are presented in Table 6.

TABLE 6 CALIBRATION OF TEMPERATURE SENSORS FOR MESDA AMCIDs

Part or Temp (K)	Resistance (kilohms) for Indicated Serial Nos.				
Array SN	225-9.6-7	225-7.7-2	299-6.7-4	225-7.7-4	225-8.0-4
AMCID SN	8101	8106	8107	8108	8115
Temp Sensor SN	188	190	189	197	201
7	121.2	118.0	120.1	122.6	118.5
8	92.1	89.7	91.5	93.2	90.1
9	73.7	71.8	73.3	74.6	72.1
10	61.2	59.7	61.0	62.0	59.9
11	52.3	51.0	52.2	52.9	51.2
12	45.6	44.5	45.6	46.2	44.7
13	40.5	39.6	40.5	41.1	39.8
14	36.5	35.7	36.6	37.0	35.8
15	33.3	32.5	33.4	33.8	32.7
16	30.6	29.9	30.7	31.1	30.1
17	28.4	27.8	28.5	28.9	27.9
18	26.6	26.0	26.7	27.0	26.1
19	25.0	24.4	25.1	25.4	24.5
20	23.6	23.1	23.7	24.0	23.2

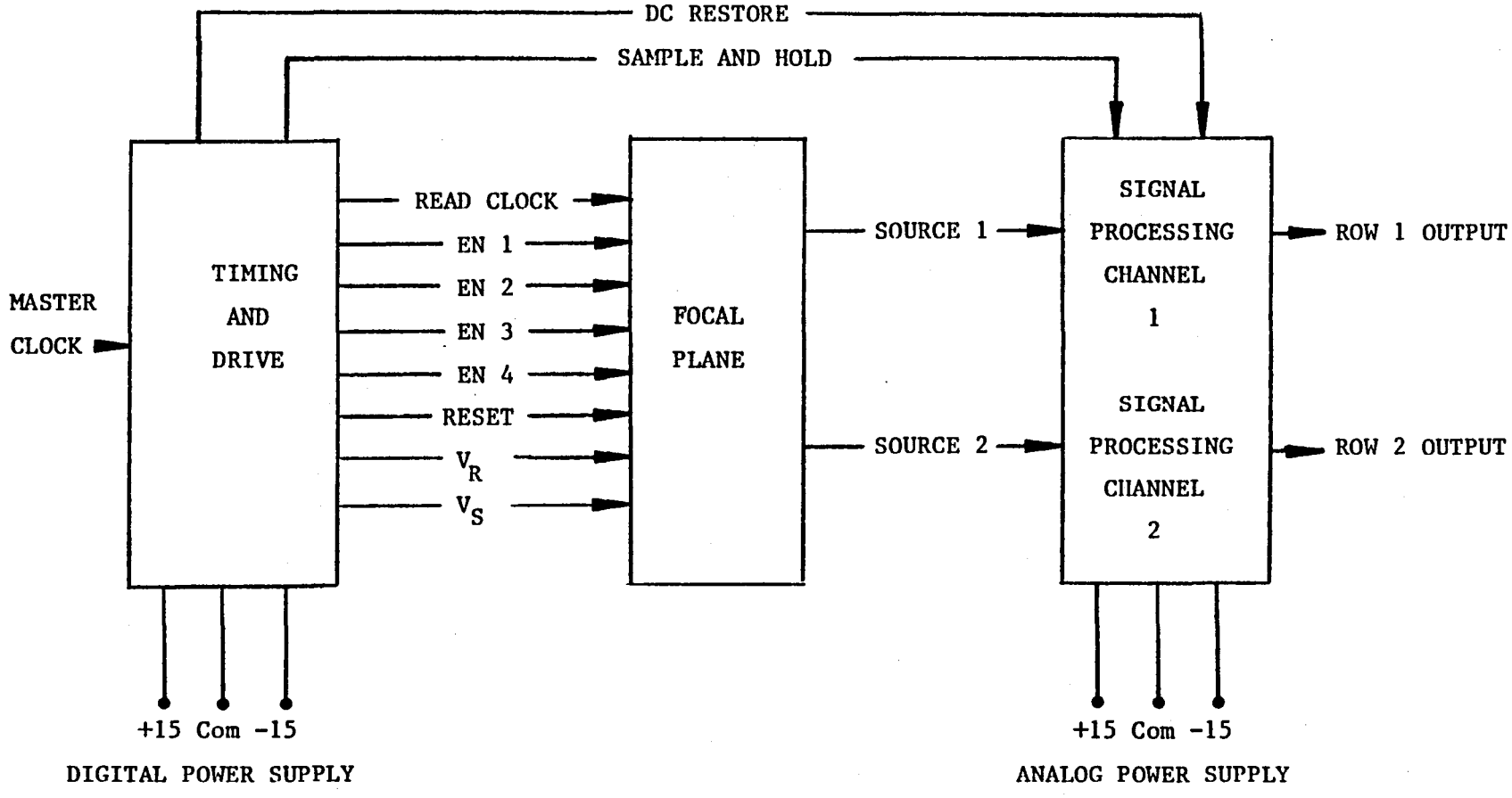


FIGURE 1. MESDA AMCID SYSTEM

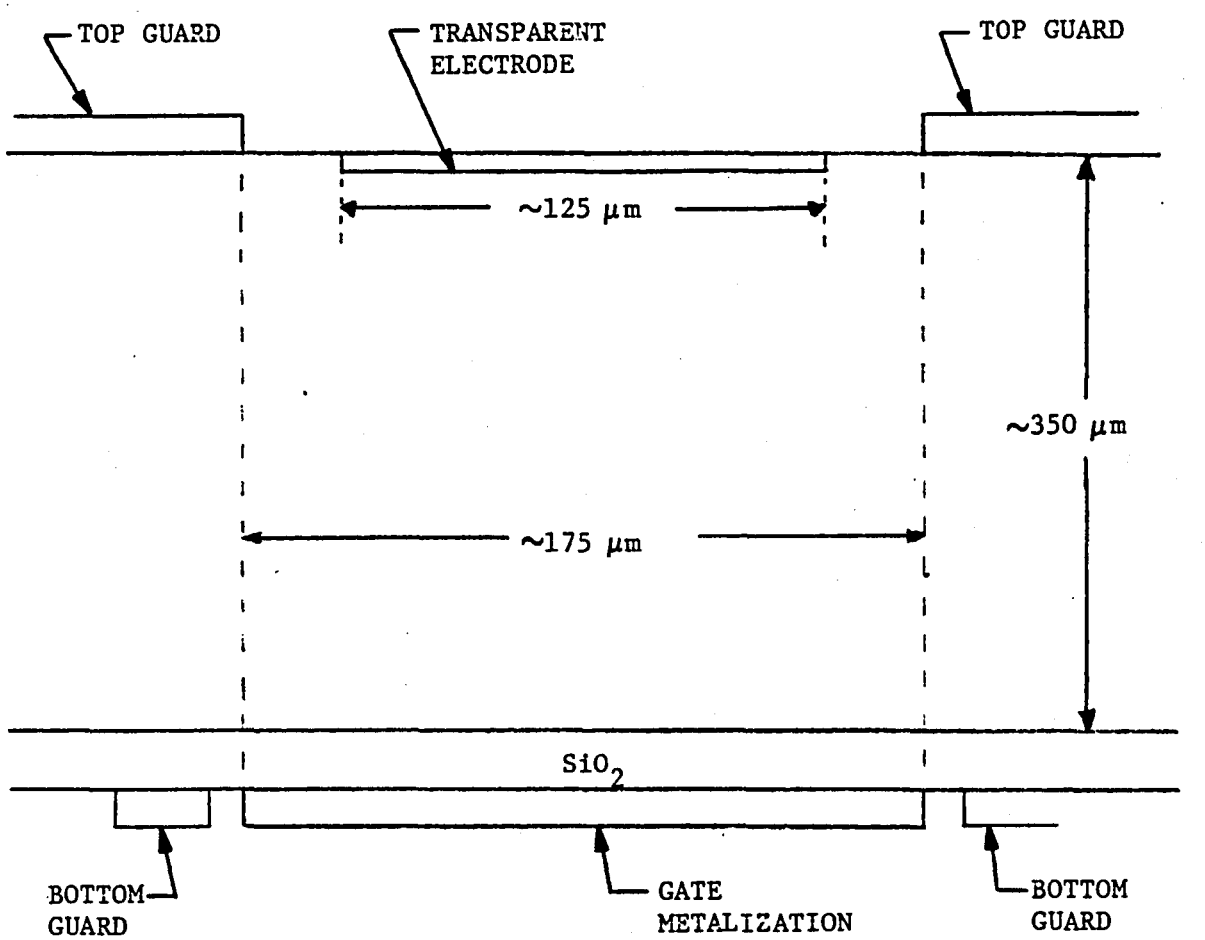


FIGURE 2. CROSS SECTION OF SINGLE CID CELL

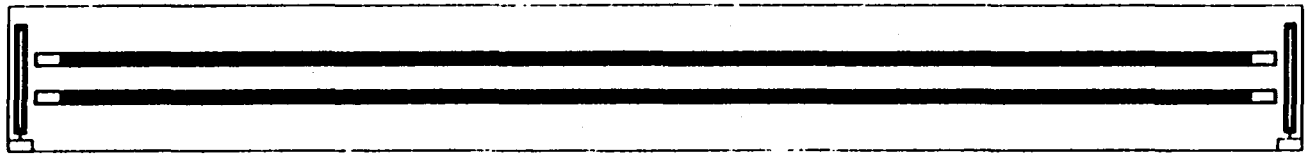


FIGURE 3. ARTWORK FOR FRONT-SURFACE METALIZATION

FIGURE 4. ORIGINAL ARTWORK FOR BACK-SURFACE METALIZATION

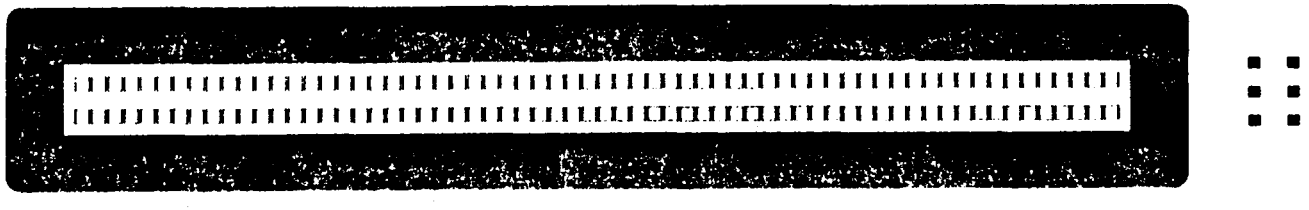


FIGURE 5. REVISED ARTWORK FOR BACK-SURFACE METALIZATION

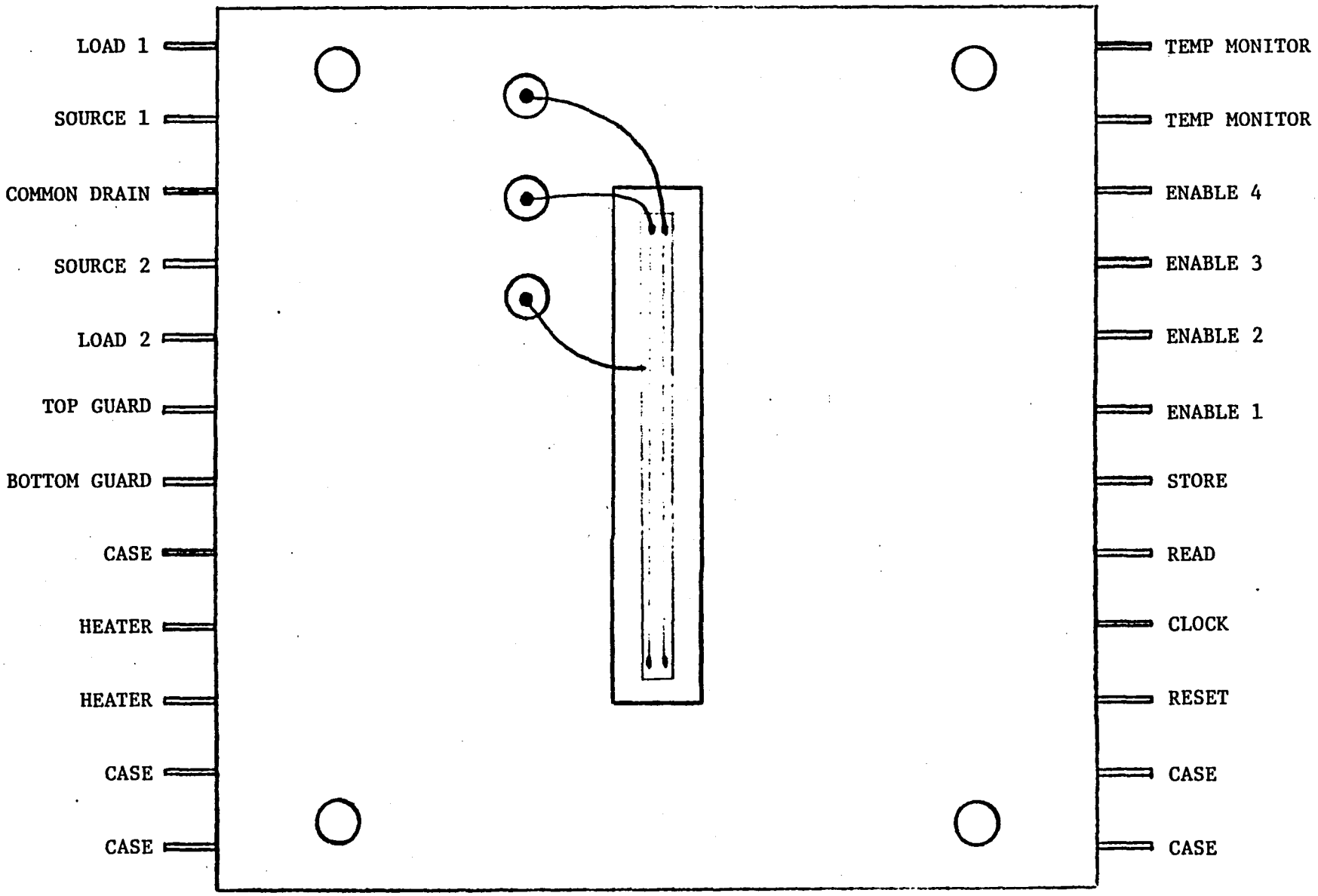


FIGURE 6. ARRAY IN MICROELECTRONICS CASE, SN 8101, 8106, AND 8107

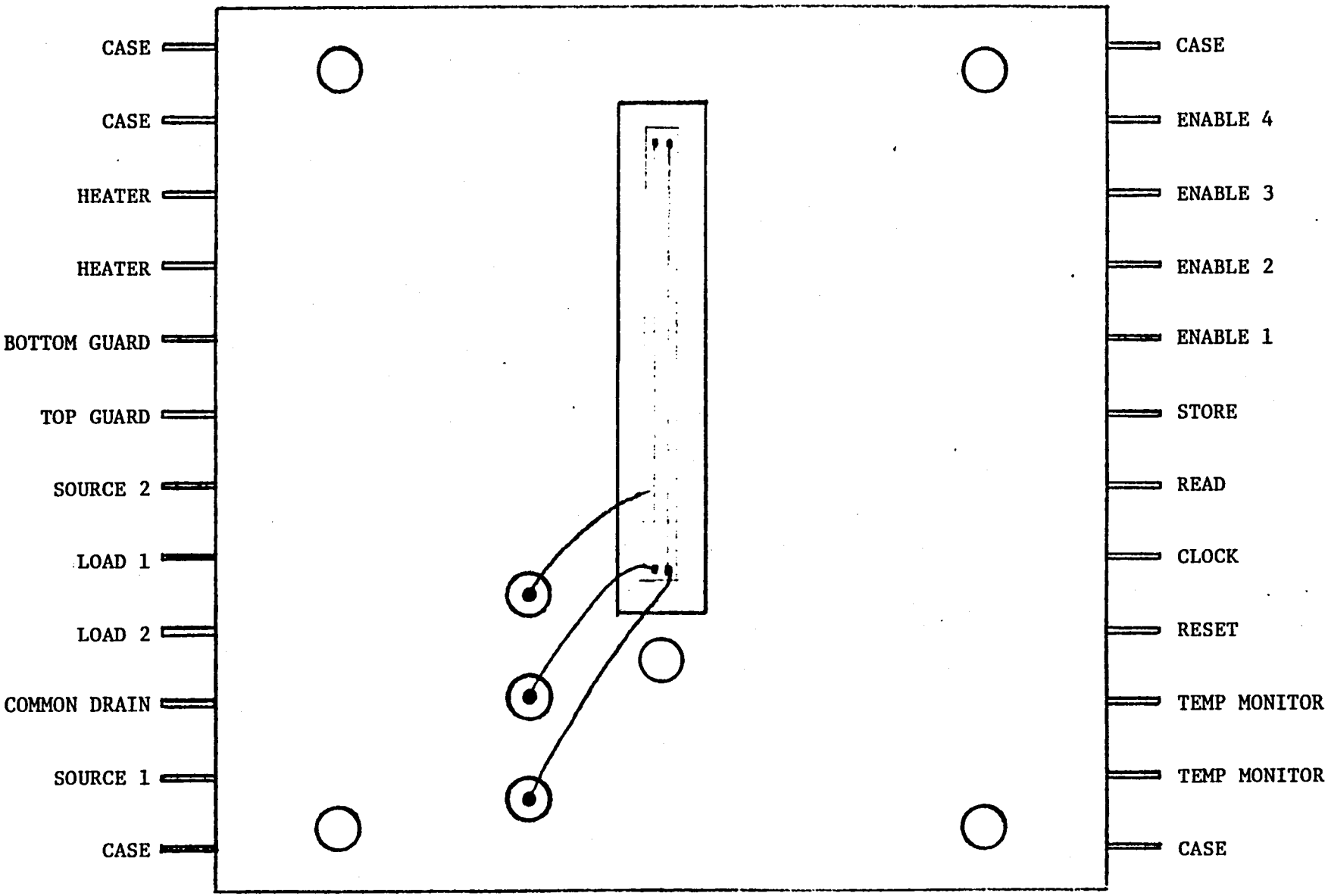


FIGURE 7. ARRAY IN MICROELECTRONICS CASE, SN 8108

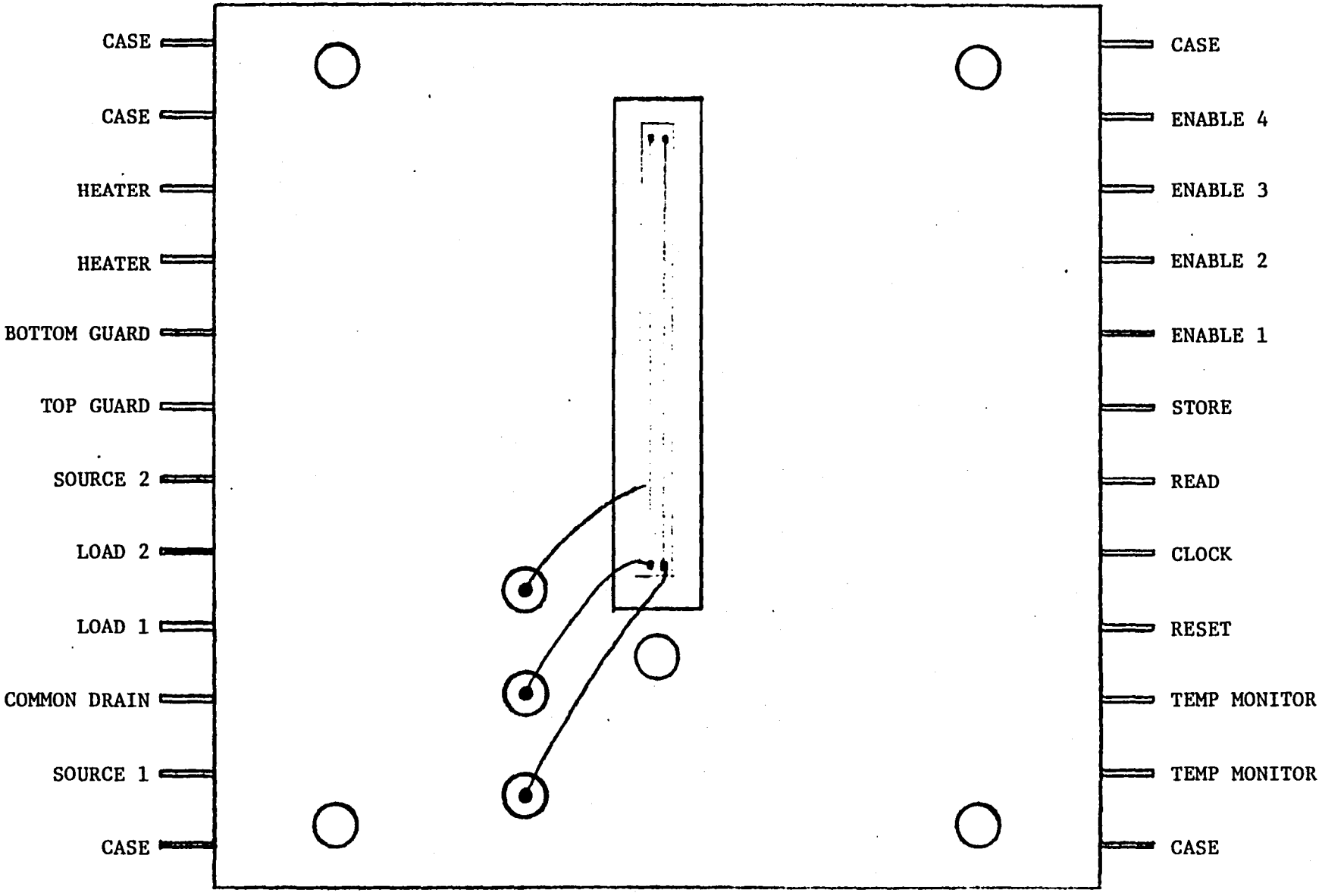


FIGURE 8. ARRAY IN MICROELECTRONICS CASE, SN 8115

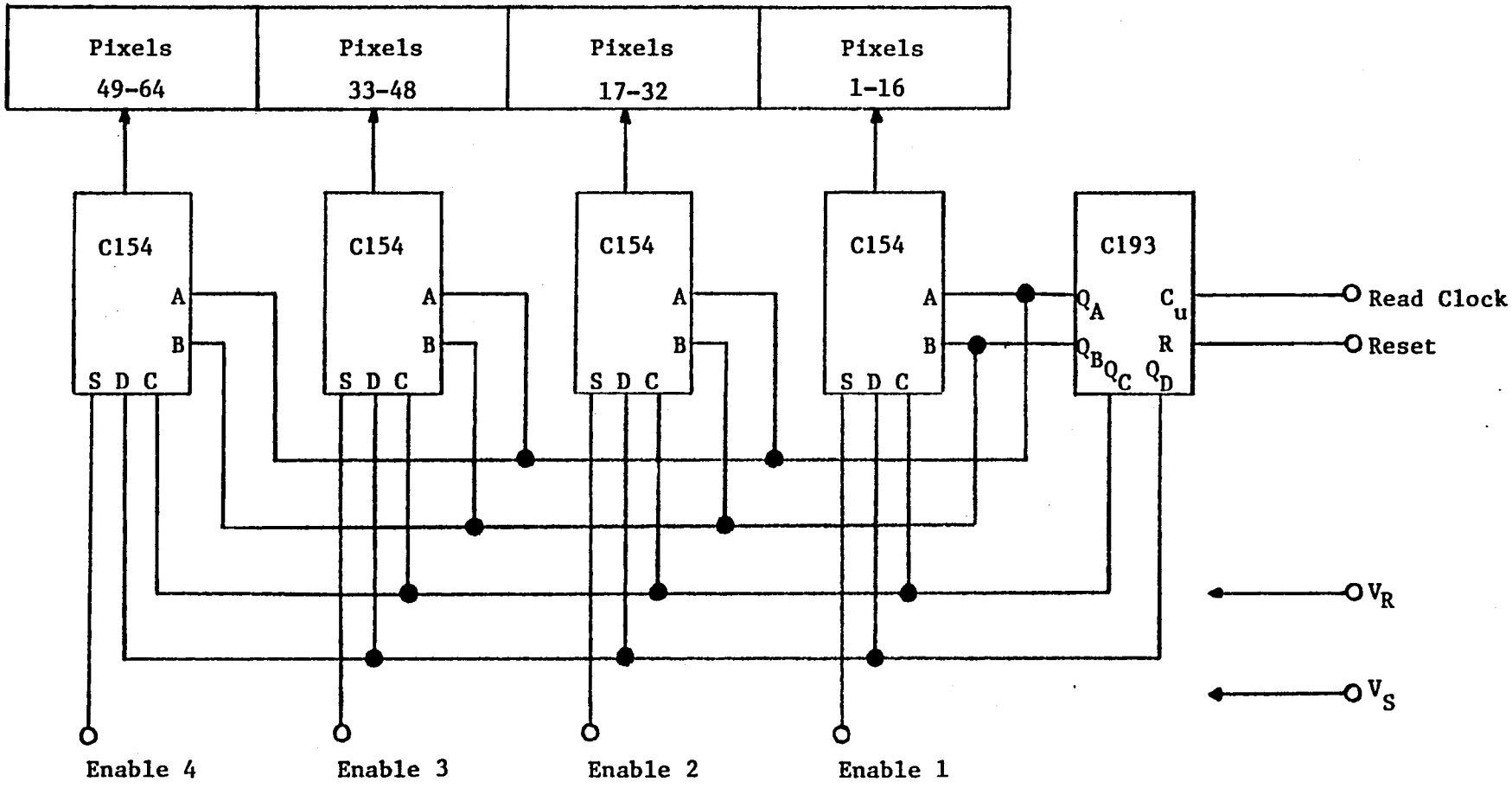


FIGURE 9. ON-FOCAL-PLANE SCANNING ELECTRONICS

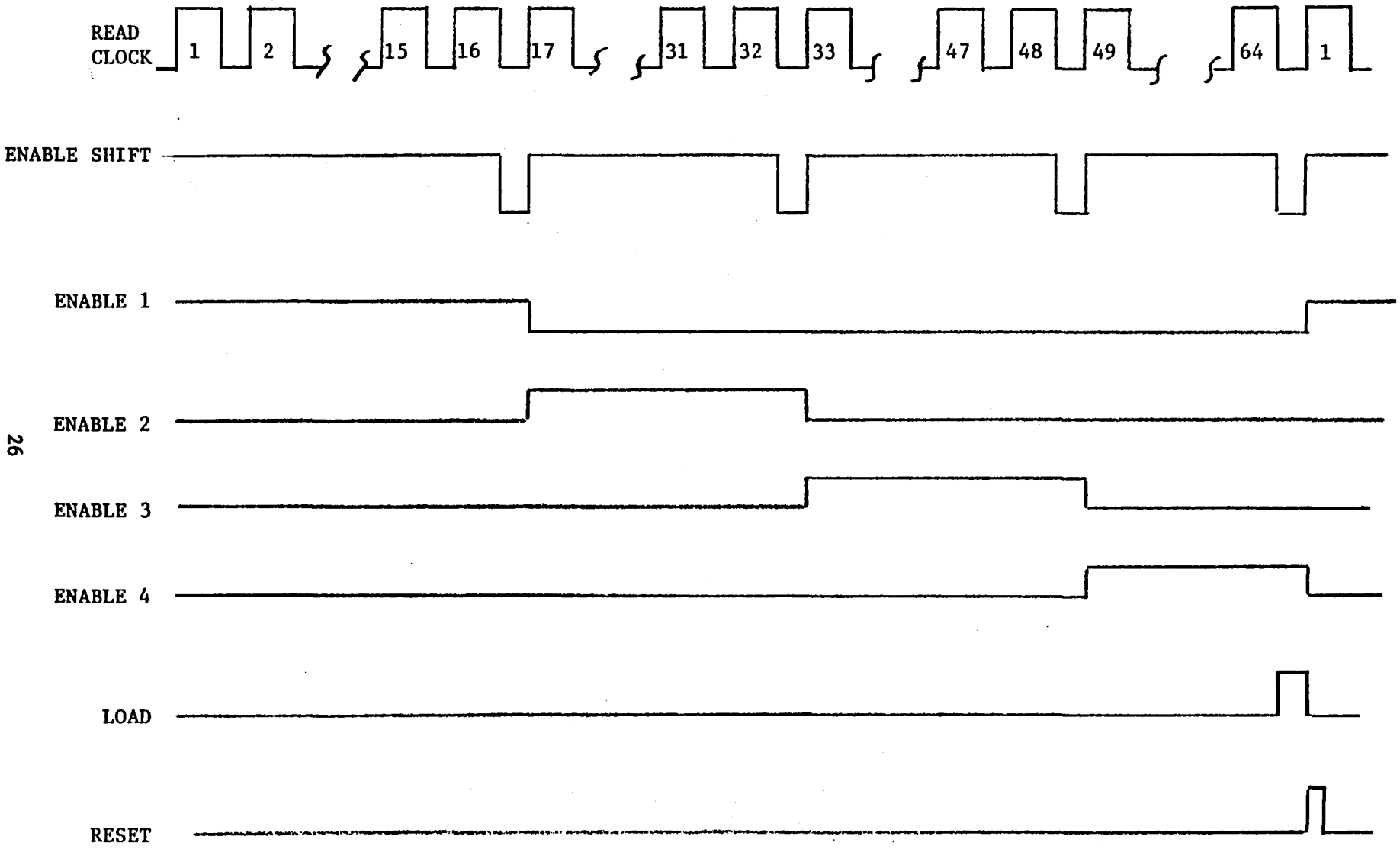


FIGURE 10. TIMING DIAGRAM FOR ONE READ FRAME

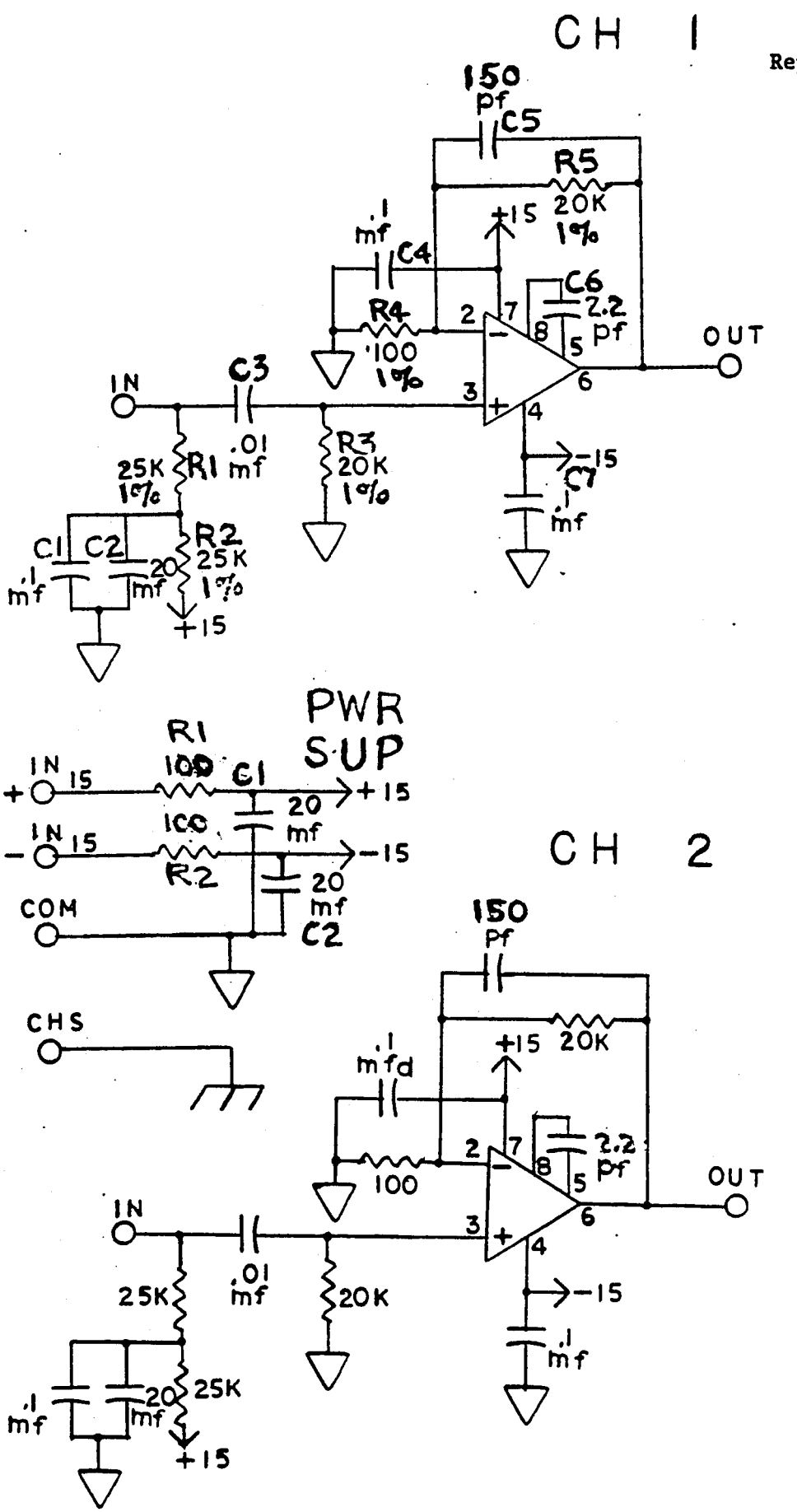


FIGURE 11. SIGNAL-CONDITIONING AMPLIFIER, SCHEMATIC

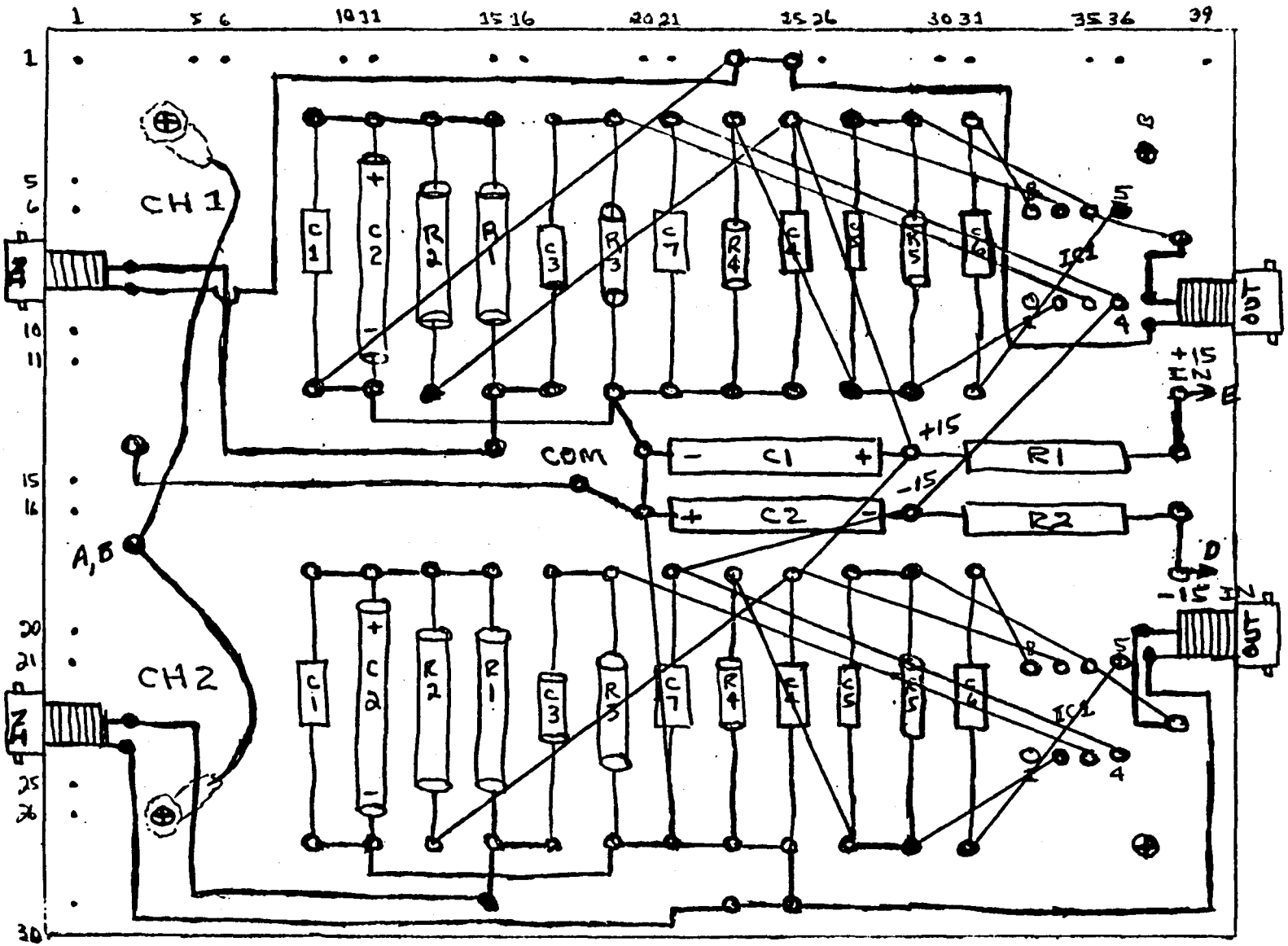
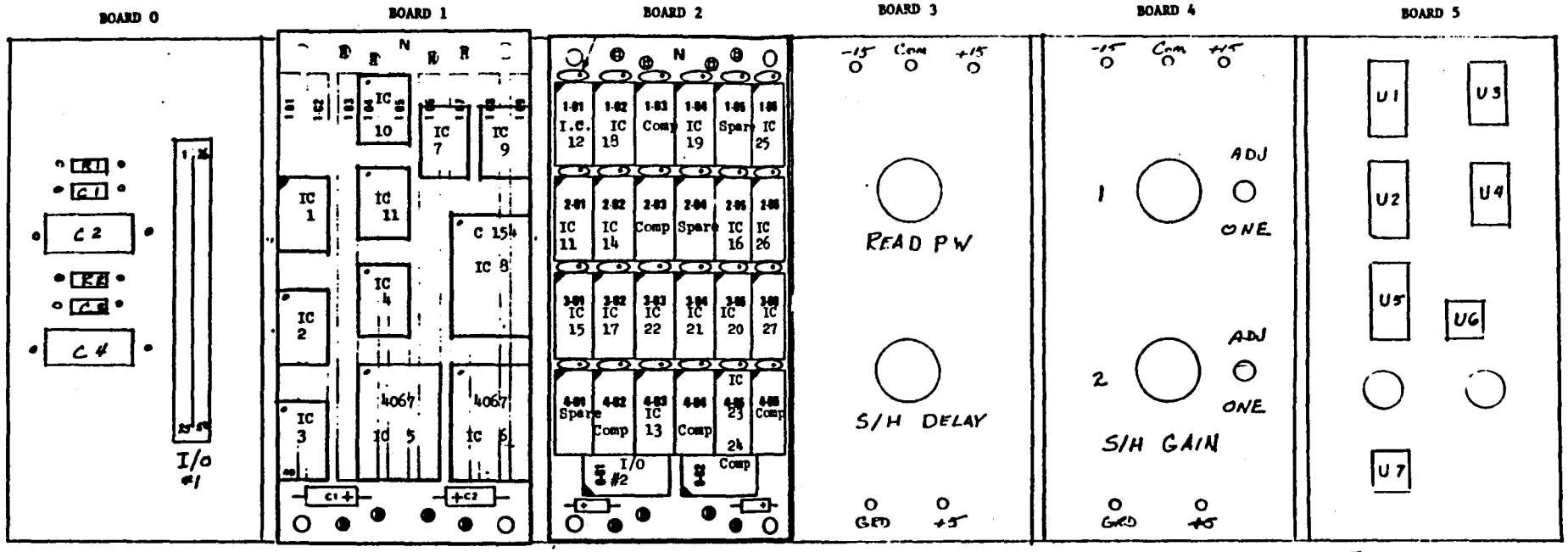


FIGURE 12. COMPONENT LAYOUT FOR SIGNAL-CONDITIONING AMPLIFIER



COMP.	VALUE
R 1,2	1K
C 1,3	0.1mF
C 2,4	100mF

IC#	DEVICE	Pin#1
1	4040	11
2	4040	22
3	4040	33
4	4051	19
5	4067	29
6	4067	29
7	74C193	3
8	74C154	14
9	4050	3
10	4049	1
COMP	914C103X	10

IC#	DEVICE
11	74LS76
12,13	74LS00
14	4035
15	4050
16	4011
17	4051
18-22	74LS123
23,24	75451
25,26,27	DG 303

I.C.#	Device
U1	HA 2425
U2	HA 2425
U3	LH0002
U4	LH0002
U5	DG 308
U6	HPL 2630
U7	HPL 2630

FIGURE 13. COMPONENT LAYOUT FOR AMBIENT-TEMPERATURE ELECTRONICS

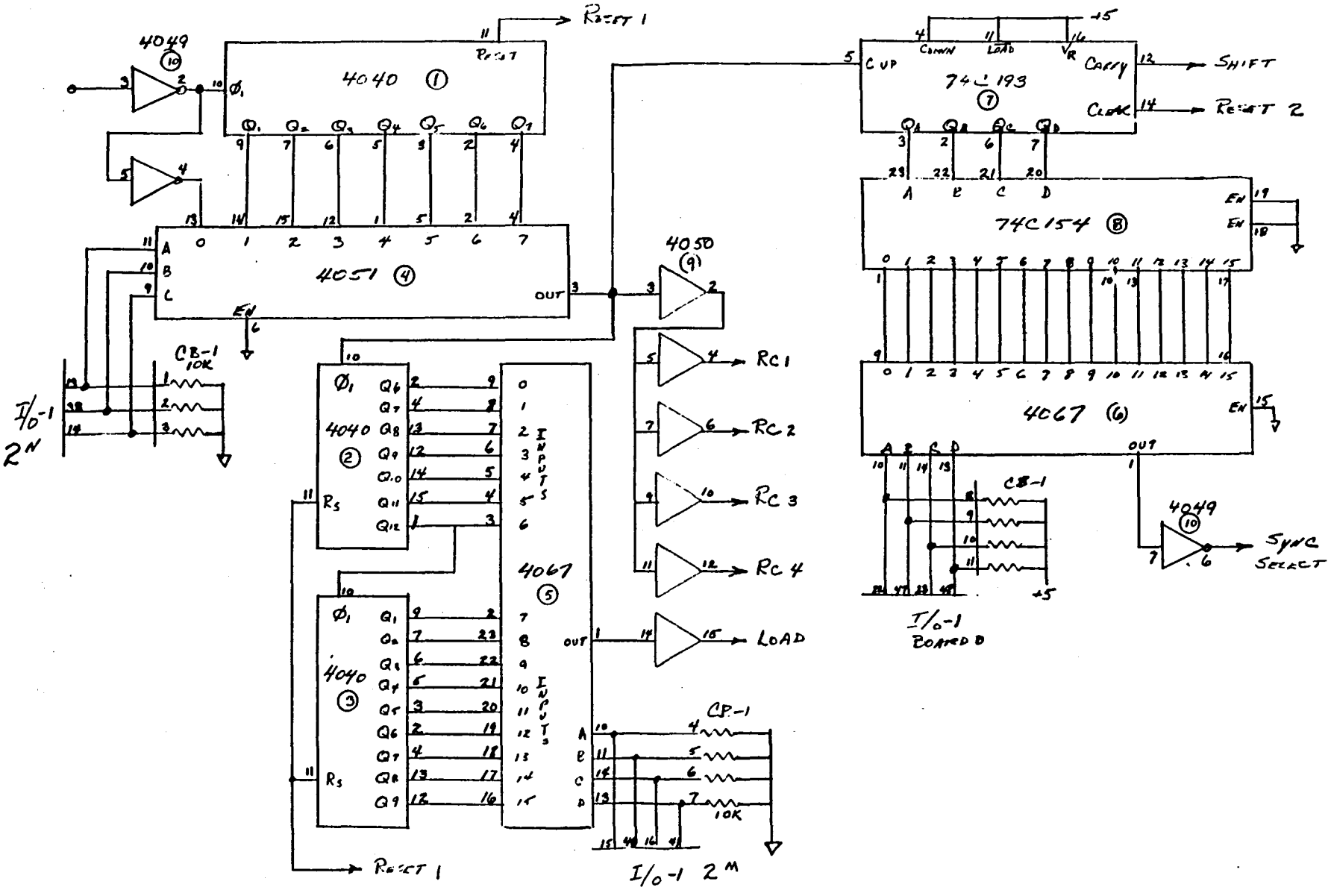


FIGURE 14. SCHEMATIC FOR TIMING AND DRIVE CIRCUIT BOARD 1

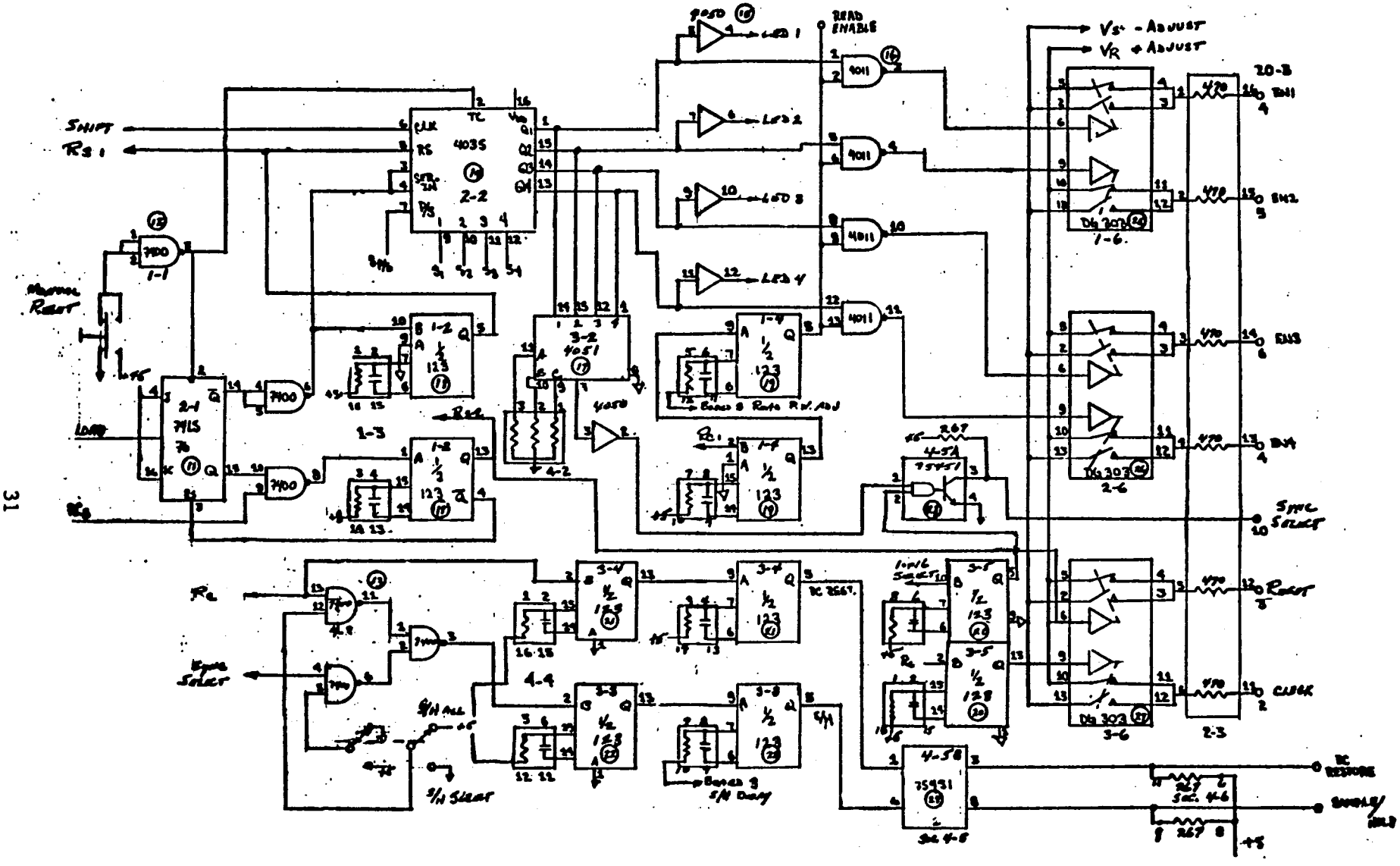


FIGURE 15. SCHEMATIC FOR TIMING AND DRIVE CIRCUIT BOARD 2

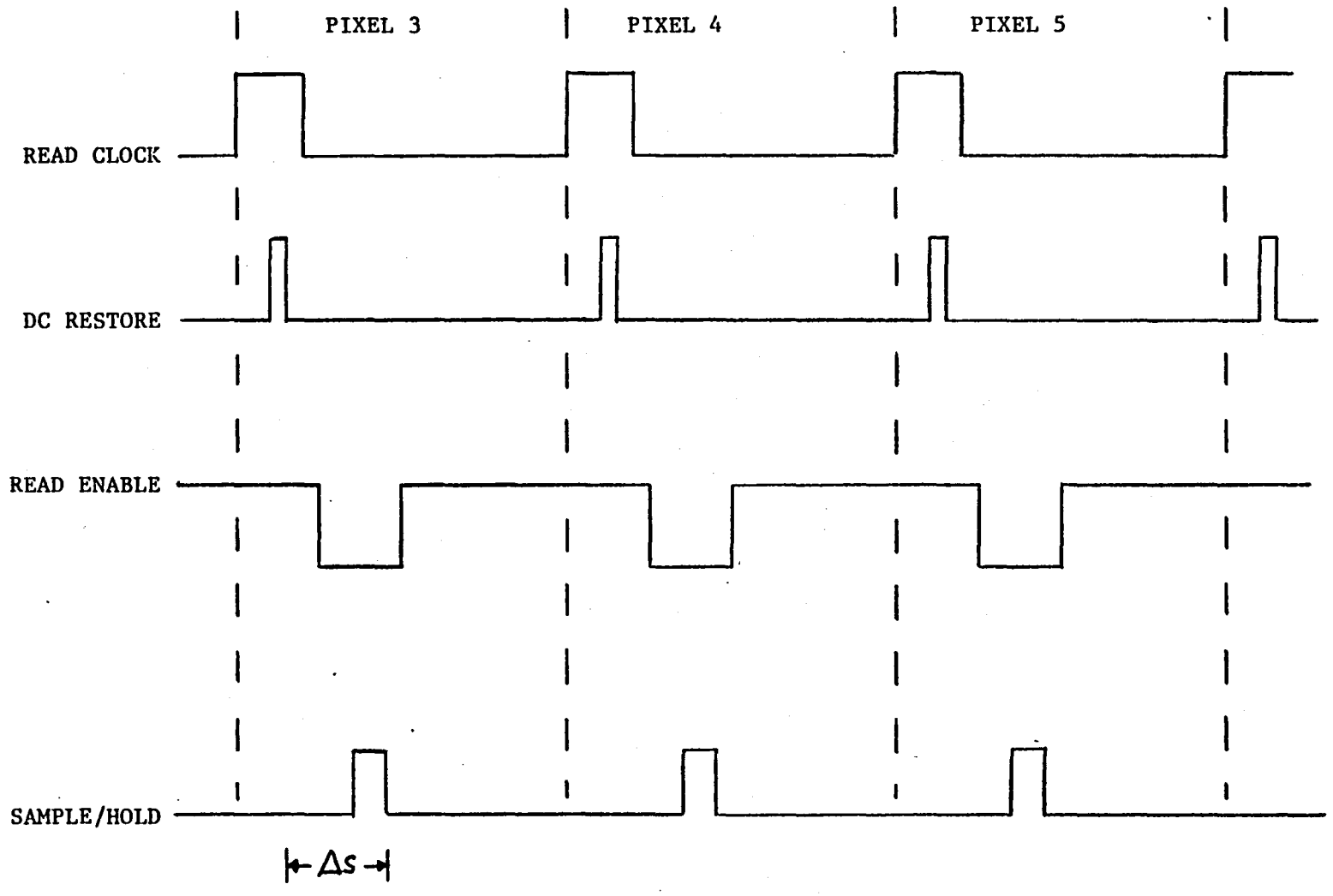


FIGURE 16. TYPICAL TIMING DIAGRAM FOR MESDA S/H CIRCUIT

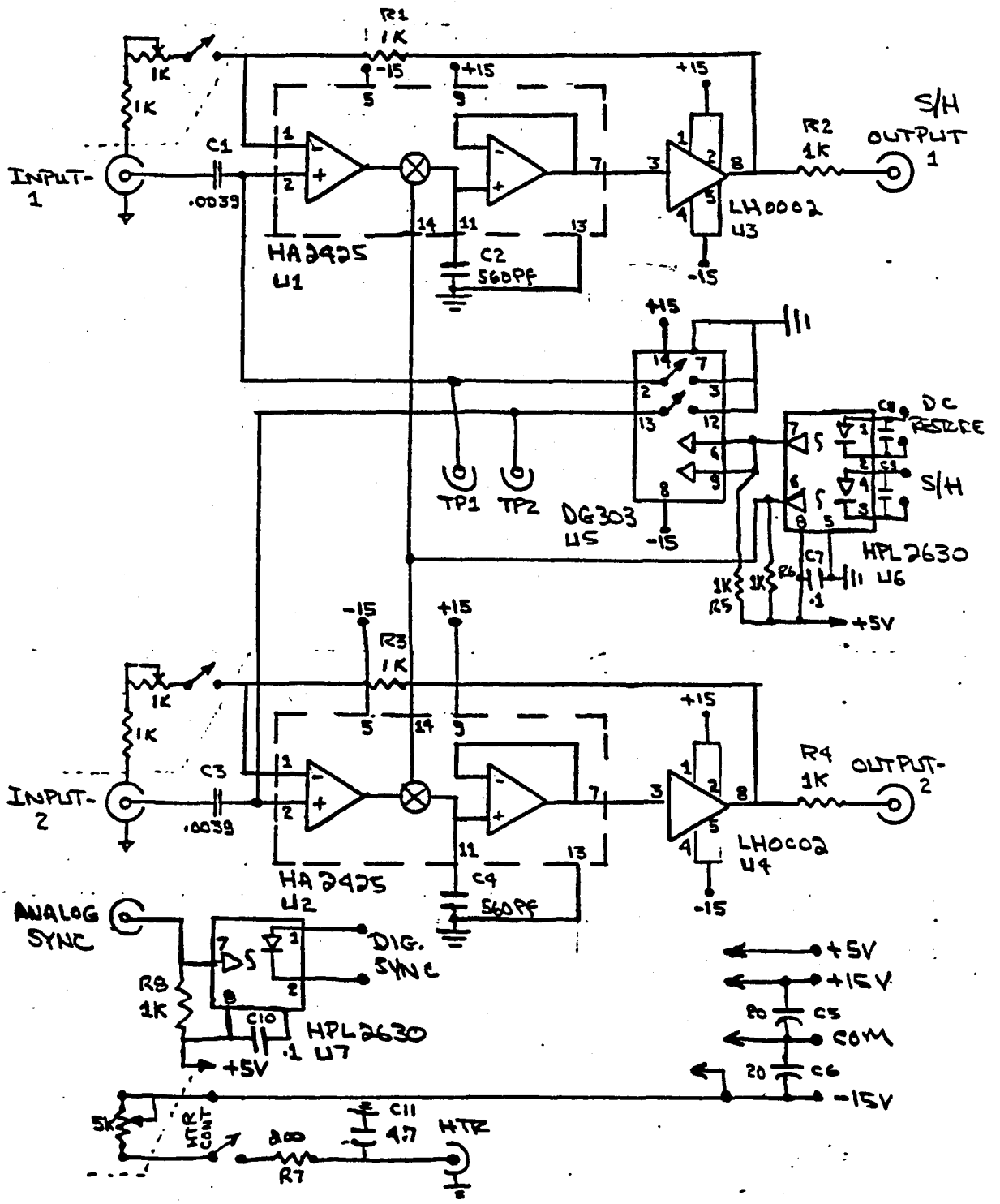


FIGURE 17. S/H CIRCUIT, SCHEMATIC

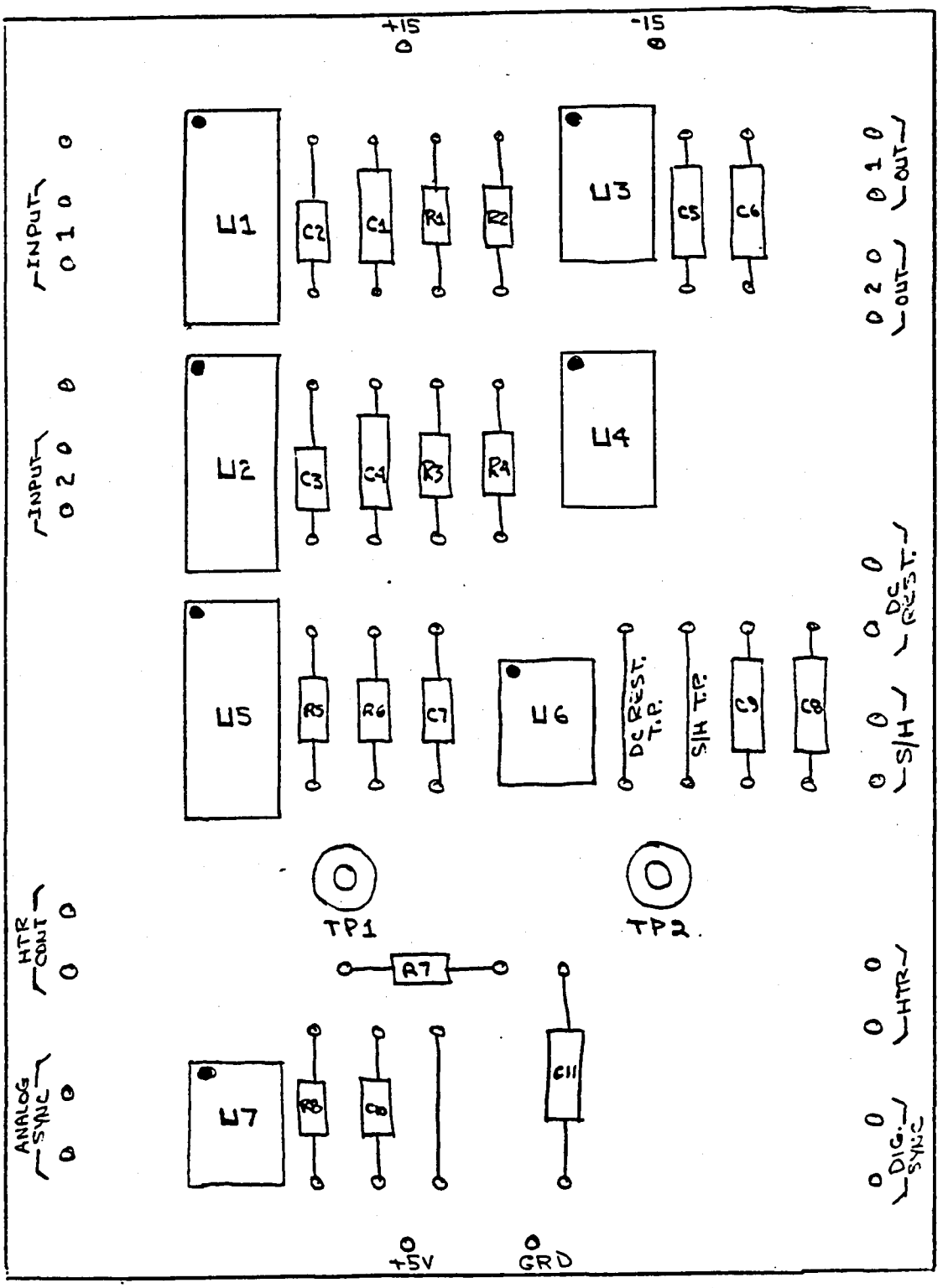


FIGURE 18. COMPONENT LAYOUT FOR S/H BOARD

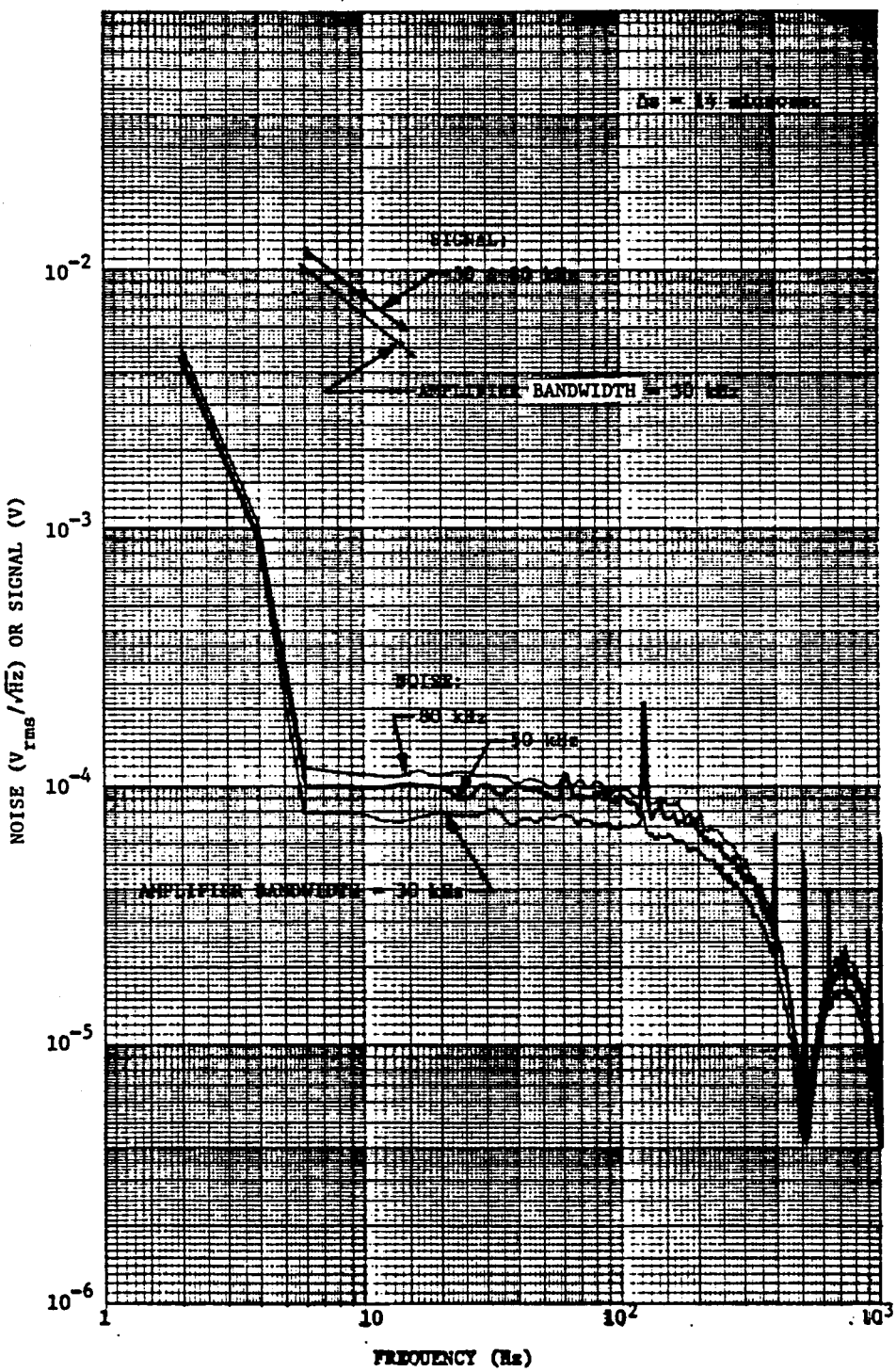


FIGURE 19. SIGNAL AND NOISE SPECTRA FOR FIRST AMCID-ARRAY/SCA/ECU SET

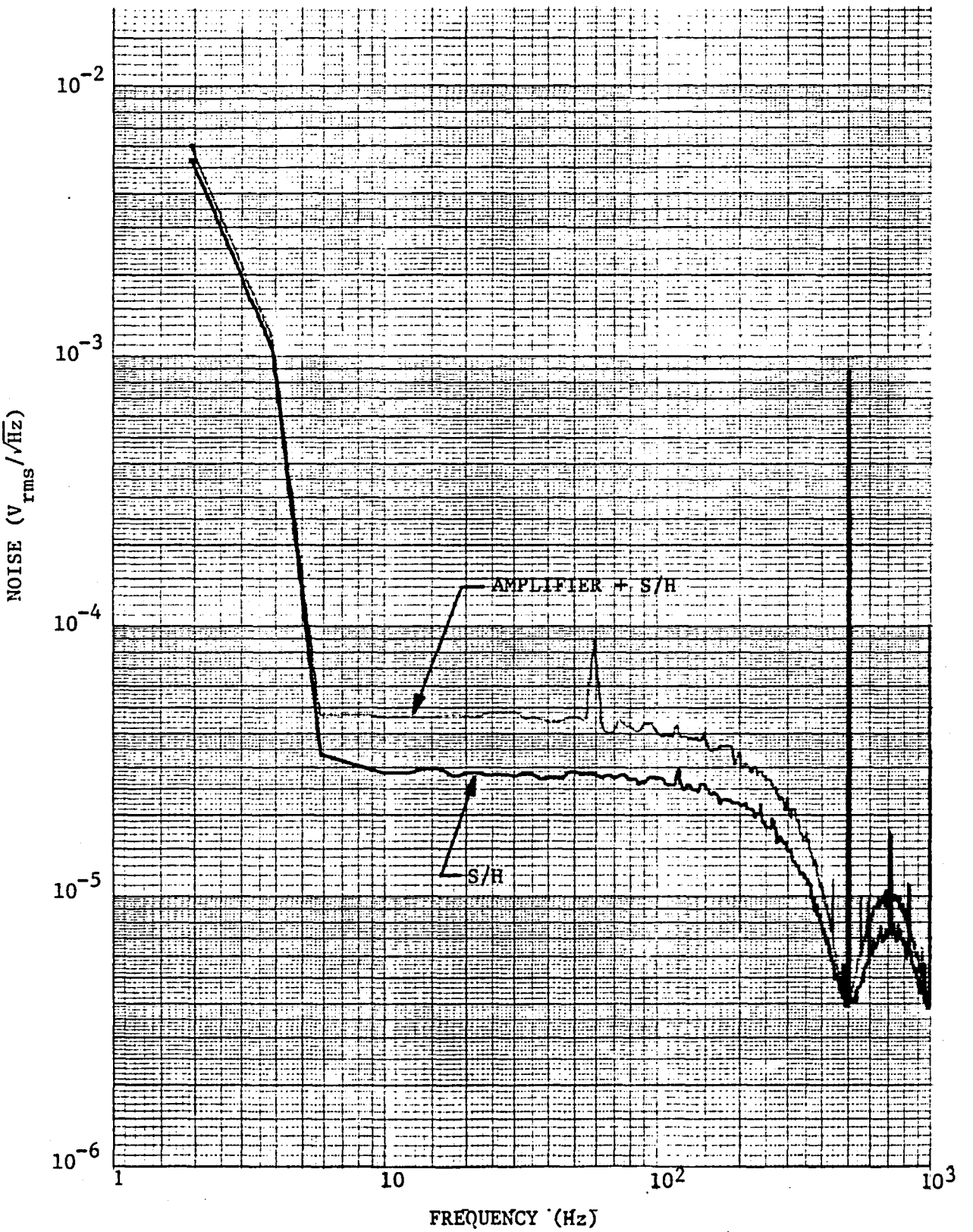


FIGURE 20. NOISE SPECTRA FOR AMCID SN 8101

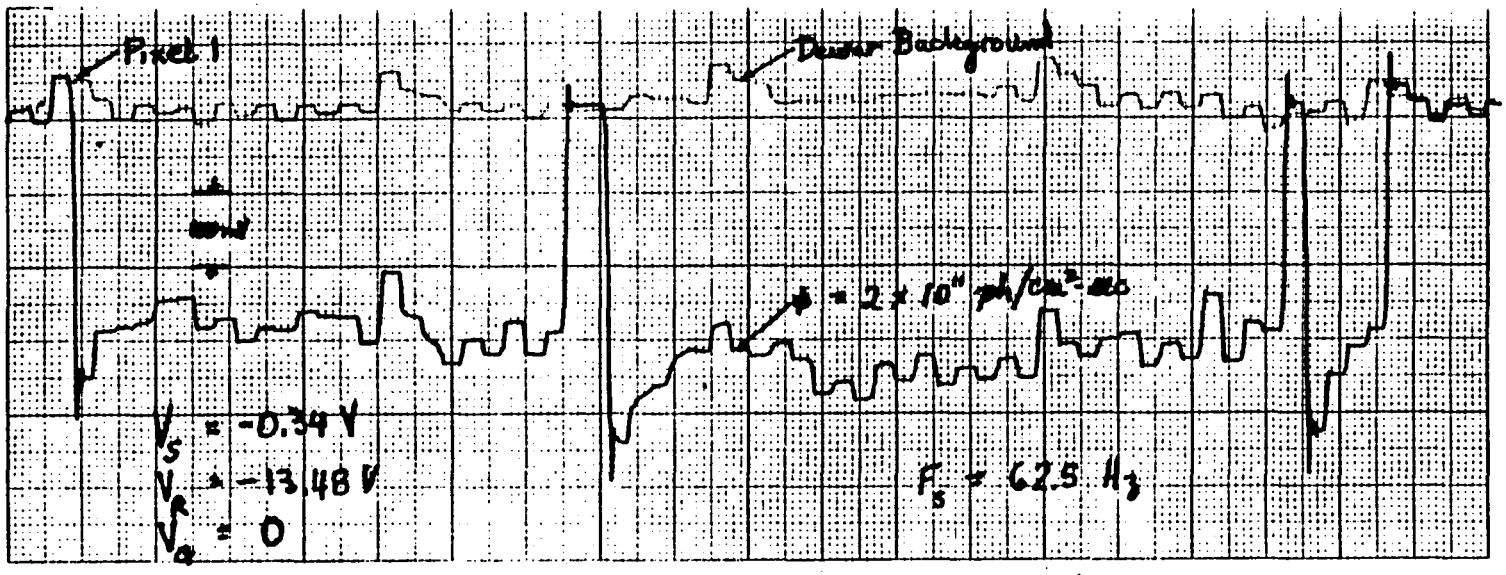


FIGURE 21. RESPONSE OF AMCID SN 8101

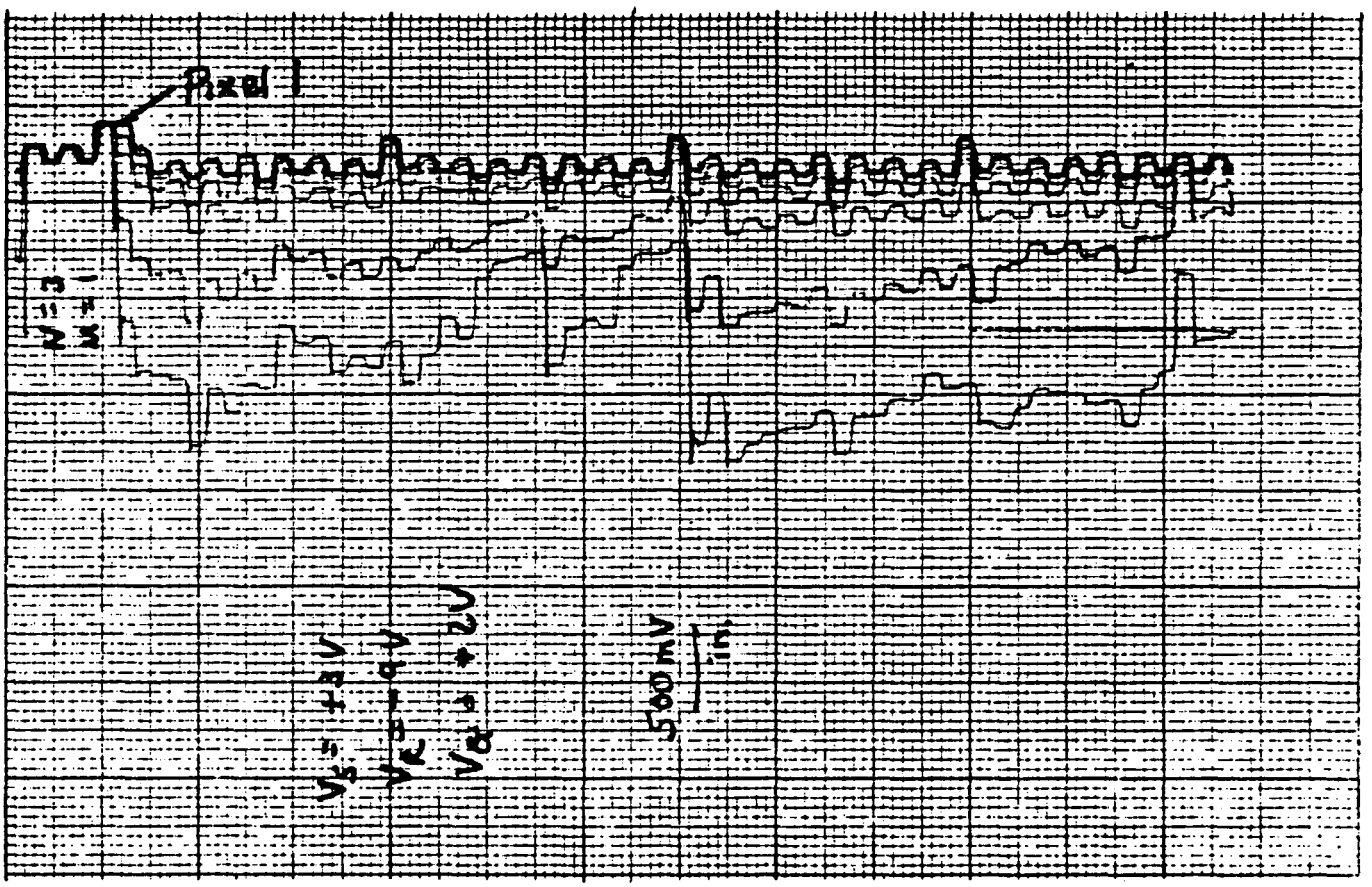


FIGURE 22. RESPONSE OF AMCID SN 8106 TO DIFFERENT LED CURRENTS

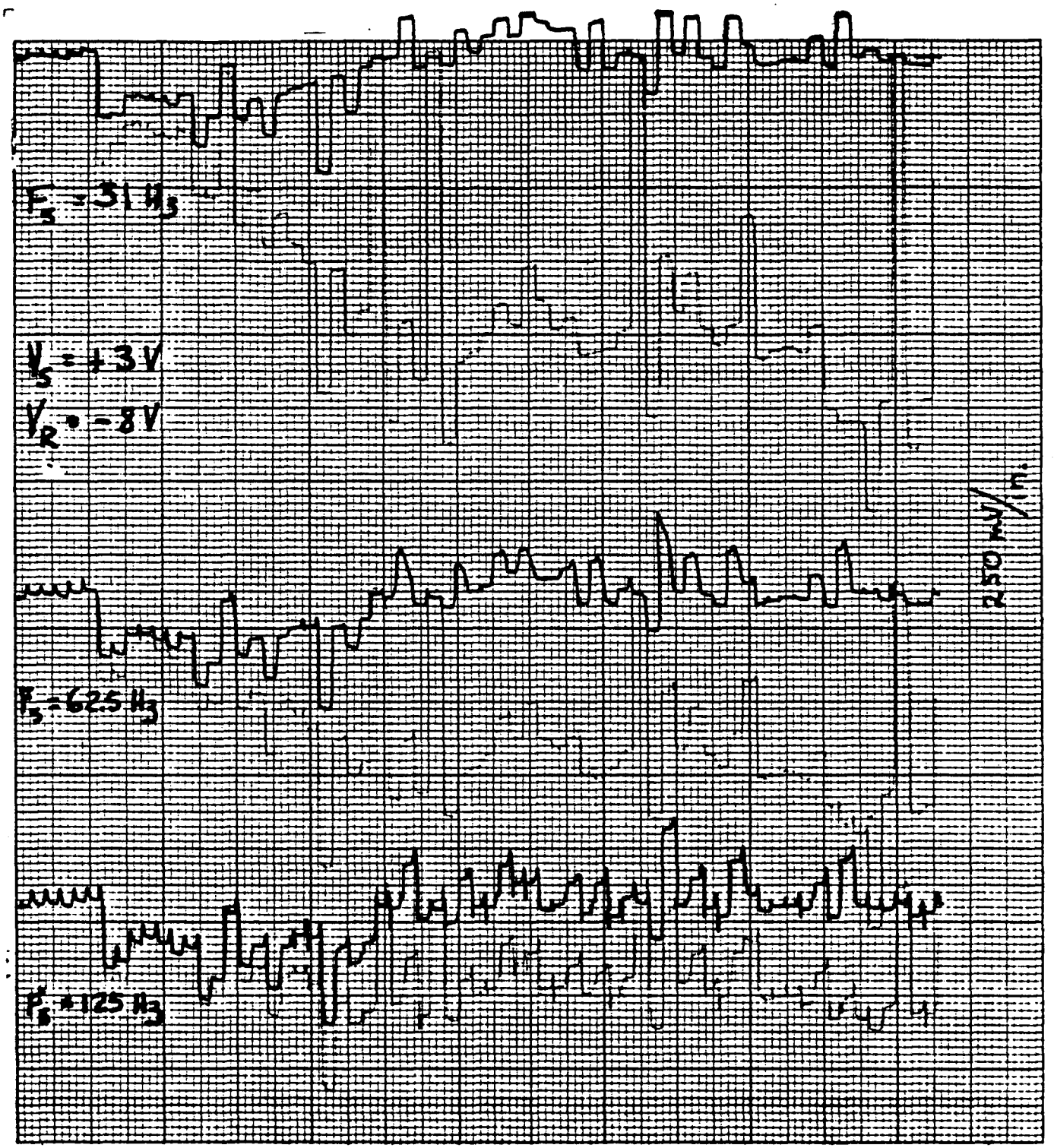


FIGURE 23. RESPONSE OF AMCID SN 8107 AT DIFFERENT SAMPLING RATES

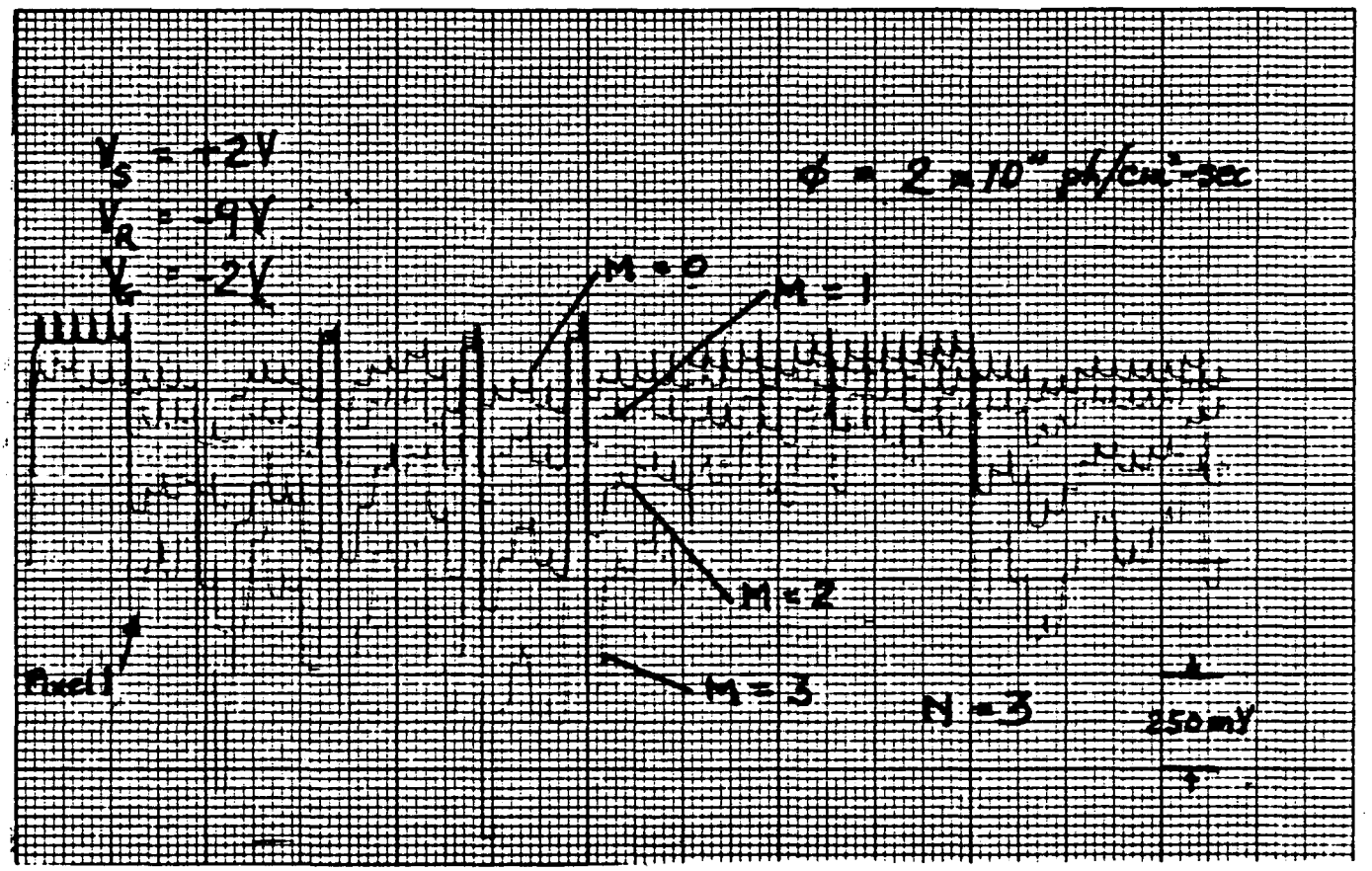


FIGURE 24. RESPONSE OF AMCID SN 8108 AT DIFFERENT SAMPLING RATES

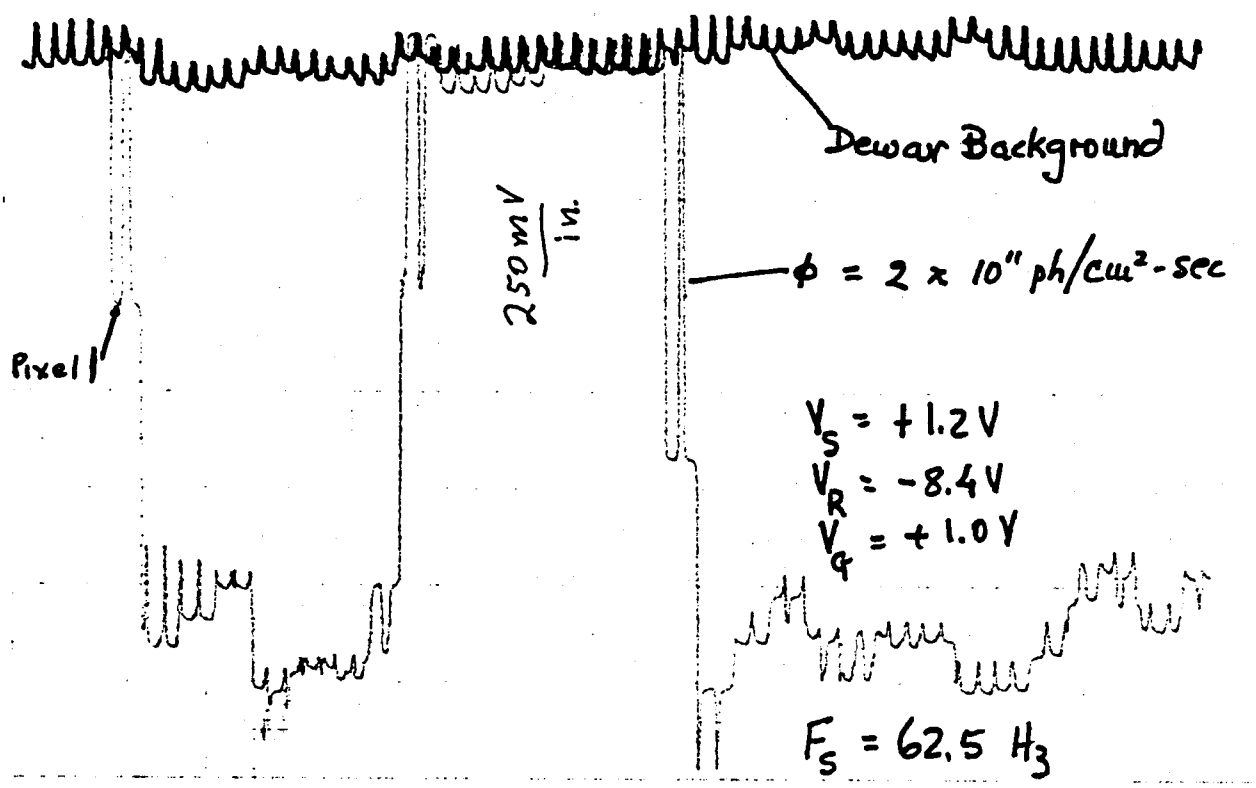


FIGURE 25. RESPONSE OF AMCID SN 8115
(Before Decoder No. 2 Was Repaired)

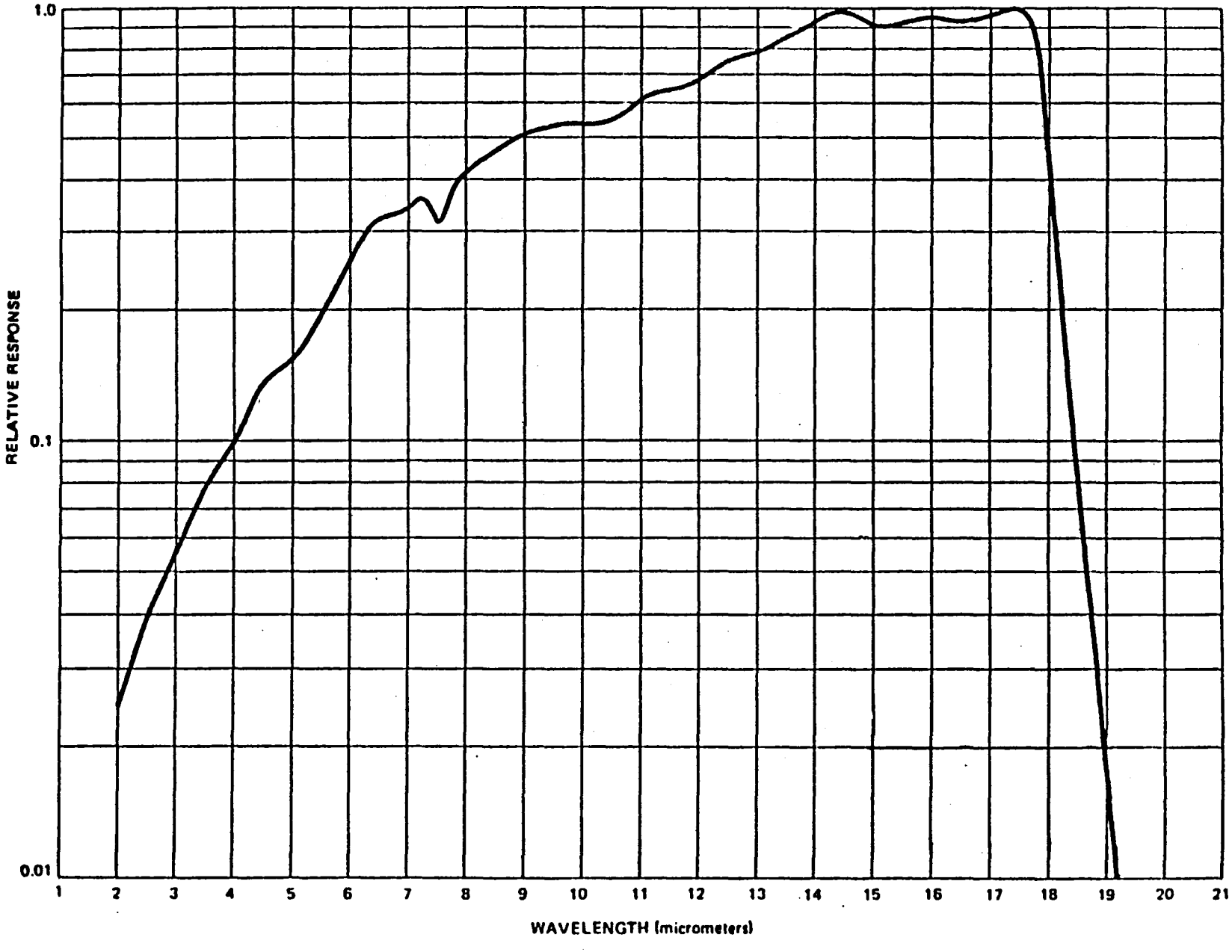


FIGURE 26. TYPICAL SPECTRAL RESPONSE FOR Si:Bi DETECTOR

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15. Supplementary Notes

Technical Monitor: Charles M. Winget, Mail Stop 239-7, NASA Ames Research Center, Moffett Field, CA 94035 (415) 965-5753 or FTS 448-5753

16. Abstract

This report covers work by Aeroject ElectroSystems Company (AESC) on the development and testing of multiplexed extrinsic silicon detector arrays (MESDAs) for infrared astronomical applications. The work was performed under National Aeronautics and Space Administration (NASA) Contract NAS2-10643 for the Ames Research Center and Kitt Peak National Observatory during the period from May 1980 through January 1982.

The AESC design and fabrication efforts for detector arrays and cryogenic electronics were directed by Dr. James F. Yee, and for ambient-temperature electronics by Robert R. Quaintance. Both collaborated in MESDA system testing, and together they acknowledge the contributions of Dr. Christopher M. Parry in many helpful discussions throughout the program.

In addition, dialogues with and the cooperation of Dr. Craig McCreight of NASA-Ames and Dr. Fred Gillette of Kitt Peak are greatly appreciated.

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