NASA CONTRACTOR REPORT 166321



# Design, Production, and Testing of Field Effect Transistors

N. Sclar





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# Design, Production, and Testing of Field Effect Transistors

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# FOREWORD

The work reported in this Technical Report was performed under NASA contract NAS2-10920 on the program entitled, "Design, Production and Testing of Field Effect Transistors." This work was performed by the Science Center of Rockwell International at Anaheim, California.

The work was monitored and directed by the NASA-Ames Research Center. Dr. John H. Goebel, Code N244-7, served as the technical monitor. The following Rockwell personnel contributed to the work that is described in this report: N. Sclar (Project Engineer and Principal Investigator); P.C. Karulkar (Wafer Processing); J.E. Cooper (Die Packaging); D.L. Rawlins and J.C. Pickel (Device Measurements).

This report covers work encompassing the period from March 24, 1981 to January 23, 1982.

# 1.0 INTRODUCTION

Over the past several years, long wavelength extrinsic silicon detectors have been developed in response to ballistic missile defense requirements. High performance detectors are now available which are at or approach background radiation limitations at the low backgrounds of space. The silicon detectors provide spectral response out to about 30 μm. These detectors are complemented by germanium extrinsic detectors with reduced but similar performance but whose response extends to about 100 μm and, if they are under stress, to about 200 μm. Since fundamental cosmic phenomena provide emission at these wavelengths, these detectors provide useful application to space borne infrared astronomy.

To operate effectively, both species of detectors must be cooled into the liquid helium temperature range. At these temperatures and space backgrounds, the detectors achieve high values of resistance. This complicates the extraction of signal from these detectors without unacceptable RC response time degradation since connecting cabling aggregate capacitances of 50 pfd or more. This problem has been redressed, in part, by positioning high values of load resistors and a MOSFET preamplifier on the same low temperature or cryogenic heat sink as the detectors. One of the possible signal processing approaches is shown in Fig. 1.1 which is also known as the constant voltage mode. The load resistor is placed in series with the detector to share an applied constant voltage bias. Exposure of the detector to an infrared flux causes a decrease in its resistance and a redistribution of the shared voltage which is then sensed by the MOSFET preamplifier. The preamplifier is operated in a source-follower mode and acts as an impedance converter with gain near unity. Its low impedance output permits signal processing without the major degradation which would be expected without its use.

Various specialized forms of the basic circuit of Fig. 1.1 are in use depending on the specific system application. The transimpedance amplifier

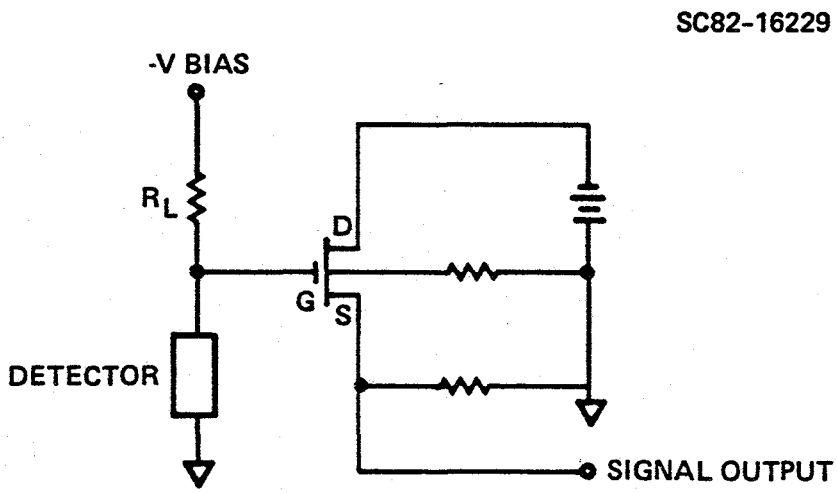



Fig. 1.1 Detector signal processor using constant voltage mode.

mode, also known as the constant current mode, is shown in Fig. 1.2. The operational amplifier shown is positioned off the cryogenic heat sink. Its output closes a negative feedback loop to the load resistor and detector supplying a constant energizing current. It compensates the effect of the small but finite input capacitance of the MOSFET (dependent on the operational amplifier open circuit gain) and thus permits higher frequency performance than is possible with the voltage mode.

A balanced MOSFET circuit approach applicable to low frequencies is shown in Fig. 1.3. This circuit employs a MOSFET reference element and obtains difference signals for sensing. The reference balances the dc offset normally inherent with the use of MOSFETs and thus permits near dc operation. This circuit is used with the IRAS (Infrared Astronomy Satellite) program sponsored by NASA.

Each of the circuits discussed utilizes a load resistor and one or more MOSFET preamplifiers at the low temperature of the detector. While the detector has been optimized with respect to its low temperature properties, no comparable effort has so far been expended for the load resistor and MOSFET preamplifier. Indeed, the present choices for these elements are based largely on empirical measurement studies, in which components originally designed for room temperature operation were compared and selected for best relative performance at low temperatures. Since the critical low temperature merit factor for these devices is unknown, extensive low temperature screening is necessary in order to acquire a complement of satisfactory devices for detector array applications.

The goal of this program is to design, produce and test cryogenic MOSFETs, here-after designated CRYOFETs, which are specifically designed to be used at cryogenic temperatures with extrinsic detectors. To prove the merit of the CRYOFETs with respect to the conventional p-channel MOSFETs, which have been widely used in this role, the program has been oriented to produce CRYOFETs along with conventional p-channel MOSFETs for test and comparison at low temperatures.

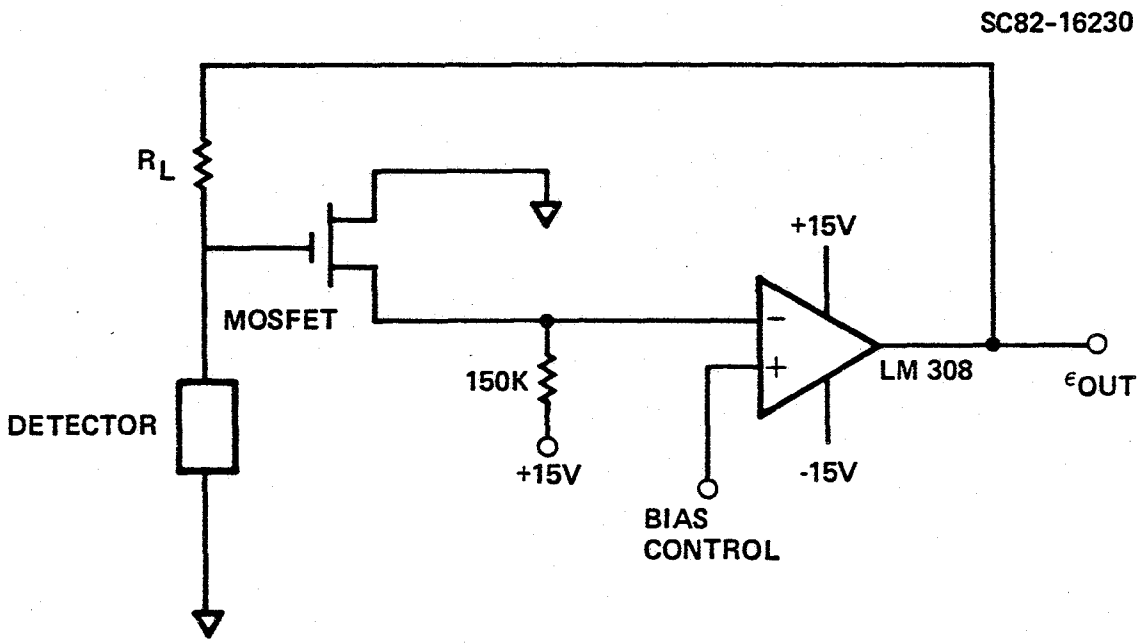



Fig. 1.2 Detector signal processor using constant current mode.

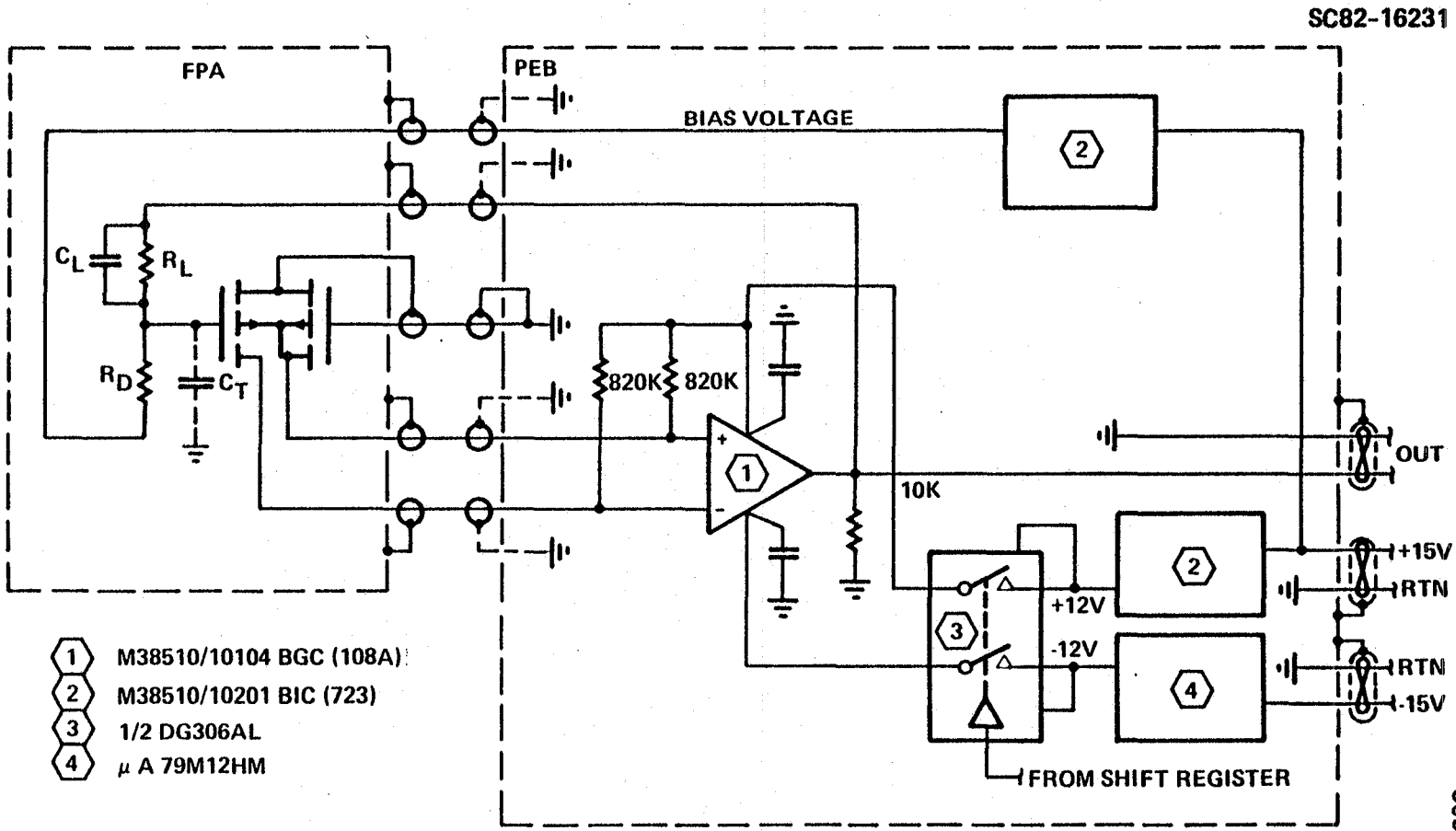



Fig. 1.3 Detector signal processor using balanced MOSFET mode.

## 1.1 Program Summary

CRYOFETs have been designed and produced along with conventional p-channel MOSFETs and the devices have been comparatively tested as source-follower amplifiers as a function of device geometry, substrate resistivity and temperature. The measurements made include gate-source capacitance, I vs V characteristic curves, voltage threshold, source-drain leakage and breakdown, bias requirements (gate and drain) to achieve gains of 0.98 and the noise as a function of frequency under this bias condition. A figure-of-merit for source-follower amplifiers is established. Calculated values, based on measurements, include parasitic and source-gate capacitance values, source-follower figure-of-merits and device power dissipation.

It is found that the CRYOFETs and the MOSFETs follow a similar dependence on device geometry. The performance of CRYOFETs is found to improve with lower substrate resistivity (higher impurity doping concentrations) while that of the MOSFETs degrade. An optimum doping choice is established for the CRYOFETs. The CRYOFETs operate effectively from the lowest temperature investigated, 2.4 K to about 20 K when leakage current between the source and drain limits performance. The low temperature performance of the MOSFETs is impaired by I vs V hysteresis and balky conduction turn-on effects. The CRYOFETs are free of these defects.

Source-follower measurements were made on devices biased up to give gain of 0.98. Noise in CRYOFETs were lower than in MOSFETs by a factor of 2-4. The figure-of-merit, which it is desirable to minimize, was also correspondingly lower. The CRYOFETs exhibit lower threshold values and require lower voltage bias to achieve gains of 0.98. This results in lower source voltages and in device power dissipation which is a hundred or more times lower than in conventional p-channel MOSFETs. With an optimum geometry and substrate resistivity, CRYOFET high gain source-follower operation is demonstrated at dissipation powers below 10 μ watts.

These results indicate that CRYOFETs are superior to MOSFETs for low temperature service with extrinsic detectors. The low power performance will

assist the achievement of extended mission times for detector/detector arrays when cryogenic cooling is limited. In addition, the devices have significant applications for on focal plane signal processing at low temperatures which heretofore were excluded because of performance deficiencies and/or excessive power dissipation.

# 2.0 CRYOFET DESIGN CONSIDERATIONS

MOSFETs may operate in the depletion or enhancement mode at ambient temperatures. The choice is determined by the polarity of the gate and drain voltages that are selected. At cryogenic temperatures, charge carrier freeze-out restricts the MOSFET modes of operation. The freeze-out condition represents a temperature induced depletion and therefore gate control of the depletion condition is lost. The enhancement mode, however, is still operative and conventional p-channel MOSFETs operating in this mode have seen service as low temperature detector preamplifiers. A cross-sectional view of such a device is shown in Fig. 2.1. In the presence of negative potentials applied to the gate and drain, holes injected at the source, traverse the MOSFET channel where they are subject to modulation by the gate potential and are collected at the drain. Difficulties encountered with this device at low temperature include balky turn-on problems, additional noise because of erratic hole injection at low temperature, various nonlinearities and hysteresis effects in the I vs V characteristics.

The CRYOFET makes specific use of the charge carrier freeze-out effect which tends to convert the silicon to an insulator. This makes possible the use of an accumulation-enhancement mode of operation. Referring to Fig. 2.1, the p-diffused source and drains are replaced by n-diffused or ion-implanted source and drains. The gate and drain are now operated with positive voltage bias. Electrons are injected at the source, accumulated under the gate where they are subject to modulation, and are collected at the drain. By avoiding p/n injection which is erratic at low temperature, a possible additional noise source is avoided.

## 2.1 Preamplifier Design Goals

In support of its role to act as an impedance converter at low temperature to change the high impedance of the signal input to a low impedance output signal, there exist a number of desirable device properties.

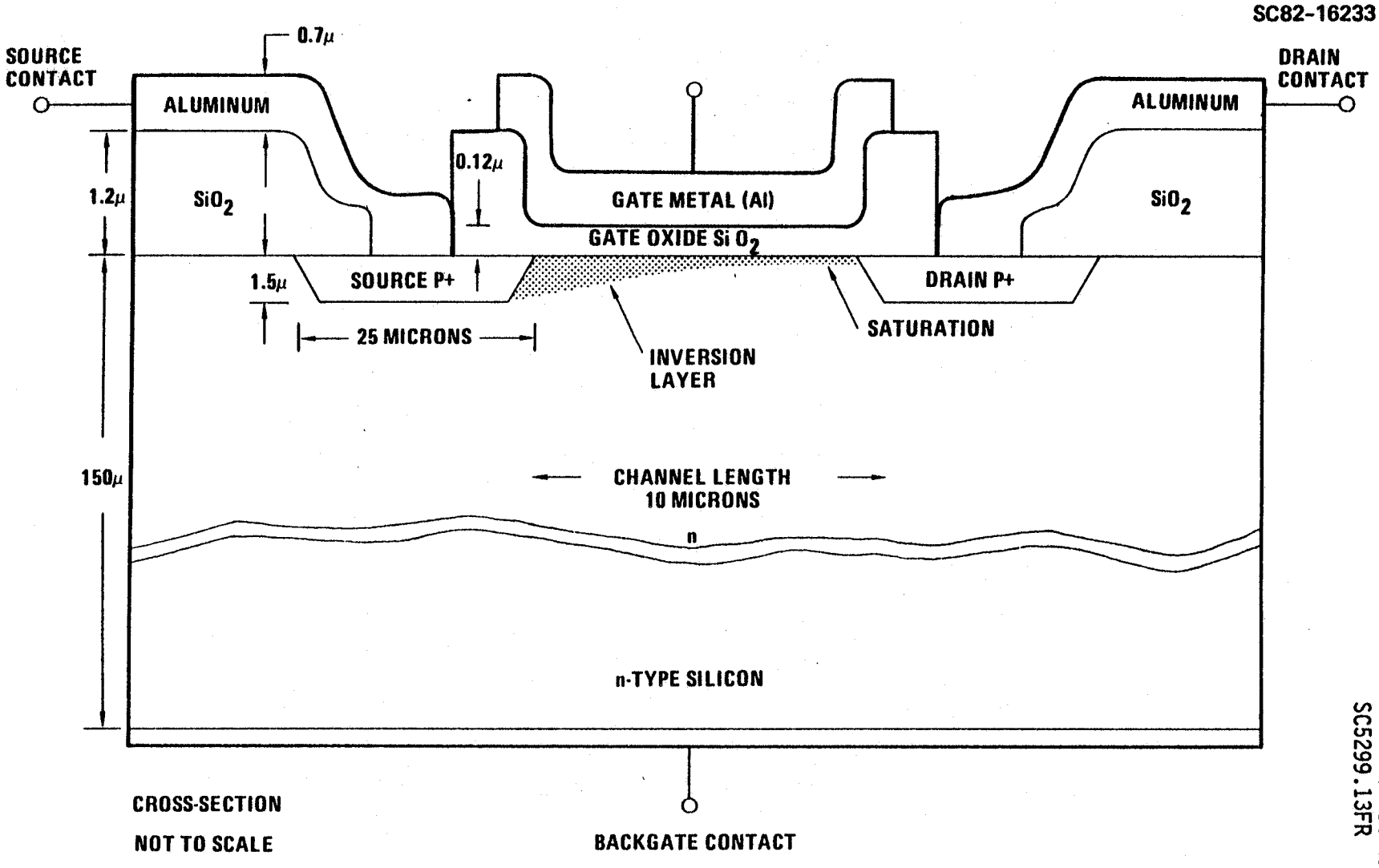



Fig. 2.1 Cross-sectional view of p-channel MOSFET device.

These are that it present a high impedance to the signal input to avoid loading the input circuit, to operate with near unity gain, G, in the source-follower mode using a minimum of device power dissipation, P, and to contribute minimum additional noise voltage, N, to the input signal. The oxide or other dielectric insulated gate provides very high dc input impedance for both the MOSFET and CRYOFET. The input capacitance of the device, C, as measured between the source and gate can control the ac input impedance. It plays a significant role in spite of the fact that it is possible to remove the effect of input capacitance on the signal by the use of feedback (Fig. 1.2). The compensation of capacitance achieved by this method is accompanied by an equivalent increase of bandpass which increases the noise as the capacitance decreases so that the signal to noise ratio remains invariant.

It is possible to establish a simple figure-of-merit for the source-follower amplifier in its usual low temperature operational mode where the condition $\omega R_L C > 1$ applies. Here $\omega = 2\pi f$ is the radial frequency with f the electrical frequency and $R_L$ the load resistor used with the detector across which the detector signal, $S_D$, is developed. The signal and the noise, $N_{D,R_L}$, developed in the detector circuit are given by

$$S_D = G\, S_o/\omega C \qquad V$$

$$N_{D,R_L} = (G/\omega C\ I_{D,R_L})(\Delta f)^{1/2} \qquad V \tag{1}$$

where $S_o$ is the product of the current responsivity of the detector and the incident IR signal power and $I_{D,R_L}$ is the noise current per root hertz provided either by the detector or its load resistor. Adding the MOSFET or CRYOFET noise in quadrature to $N_{D,R_L}$ and forming the signal to noise ratio, we obtain

$$(S/N)_{D,R_L} = \left[ \frac{S_o}{\left( I^2_{D,R_L} + \left(\frac{\omega CN}{G}\right)^2 \right) \Delta f} \right]^{1/2} \quad . \qquad (2)$$

The best signal to noise condition is obtained when the product $\frac{\omega CN}{G}$, which is a property of the source follower, achieves a minimum value. This establishes the figure-of-merit for the source-follower. If this figure-of-merit is calculated at f = 10 Hz, we obtain $62.8 \times 10^{-18} \frac{CN}{G}$ amp/$\sqrt{Hz}$ when C is expressed in units of pfd and N in units of $\mu V/\sqrt{Hz}$. This multiplicative factor will be used to normalize the figure-of-merit values reported. At low frequencies, such that $\left(\frac{\omega CN}{G}\right)^2$ falls below $I^2_{D,R_L}$, the noise will be limited by the detector noise or by the Johnson noise of the load resistor and this figure-of-merit will no longer apply. In this low frequency range, the preamplifier will no longer limit the performance of the detector/detector array. Detectors with high responsivities, which also have higher noise, and large $R_L$ values shift, the frequency at which this occurs, to higher values. For high quality detectors, this is already the case at 10 Hz. In any case, for $R_L = 2 \times 10^{10}$ ohms, this frequency will occur at about 1-2 Hz.

The dissipation power of the MOSFET or CRYOFET at cryogenic temperatures is significant because it limits the number of source-followers or other signal processing devices that can be used without raising the detector array temperature. For a given cryogenic supply, this may limit the time of operation of the system using the detector/detector array. The total power dissipated by the preamplifier includes that dissipated in the conducting channel and that across the source resistor, $R_S$, used with the source-follower.

It is given by

$$P = (V_{D,G})(V_S/R_S) \qquad W \qquad (3)$$

where $V_{D,G}$ is the common voltage applied to the gate and drain and $V_S$ is the source voltage. Gains close to unity at cryogenic temperatures achieved with minimum P are desirable.

Other desirable operational properties at low temperatures are reliable turn-on of conduction of the source-follower, signal linearity, and the freedom of anomalous behavior including hysteresis or memory effects.

## 3.0 MASK SET FOR MICROELECTRONIC PROCESSING AND PACKAGING

The processing mask set selected for processing the MOSFETs and CRYOFETs dates back to an earlier program of some 10 years ago. It permits a wide range of channel lengths, L, and channel widths, W, to be prepared for both conventional MOSFET as well as CRYOFET devices. The geometry range available , along with the calculated W/L ratios and W•L gate areas, is tabulated in Table I.

Table I
CRYOFET and MOSFET Geometries

| W (mils) | L (μm) | W/L | W•L ($10^{-5}$ $cm^2$) |
|---|---|---|---|
| 10 | 6 | 42.3 | 1.52 |
| 10 | 15 | 16.9 | 3.81 |
| 10 | 37.5 | 6.77 | 9.53 |
| 10 | 93.8 | 2.71 | 23.8 |
| 25 | 6 | 106 | 3.81 |
| 25 | 15 | 42.3 | 9.53 |
| 25 | 37.5 | 16.9 | 23.8 |
| 25 | 93.8 | 6.77 | 59.6 |
| 62.5 | 6 | 265 | 9.53 |
| 62.5 | 15 | 106 | 23.8 |
| 62.5 | 37.5 | 42.3 | 59.5 |
| 62.5 | 93.8 | 16.9 | 149 |
| 156 | 6 | 660 | 23.8 |
| 156 | 15 | 264 | 59.4 |
| 156 | 37.5 | 106 | 149 |
| 156 | 93.8 | 42.2 | 372 |

For comparison, the Siliconix G118 p-channel MOSFET which has been widely used as a detector preamplifier at low temperature has approximate dimensions of W = 70 mils, L = 10 μm and calculated values of W/L = 178; W•L = $17.8 \times 10^{-5}$ $cm^2$.

The mask set, as employed on the program, consisted of five layers as tabulated in Table II which includes the identification of the layers and their use.

Table II
Mask Layers in Processing Mask Set

| Mask Layer | Use |
|---|---|
| TC 1P | "P" Diffusion Definition |
| TC 2N | "N" Diffusion Definition |
| TC 3G | Gate Definition |
| TC 4C | Contact Definition |
| TC 5M | Metal Definition |

Exercise of the mask set during processing results in an arrangement of devices which are so organized that the configuration may be diced roughly in one half to realize two chips, A and B. These chips are separately mounted and bonded in 42 pin ceramic packages. The configuration of devices in Chip A with 62.5 and 156 mil gate widths is shown in Fig. 3.1. In Table III, the numbered contact bonding patterns for these devices designating the sources, gate and drains of the individual devices as well as their type are given. Although the sources and drains of the devices are symmetrical and may usually be interchanged, because of the common use of contact 25 for both p and n line elements, it is necessary to designate contact 25 as the source for both the P-P and N-N devices which may then be connected to the substrate. The configuration of devices in Chip B which contains the 10 and 25 mil gate widths

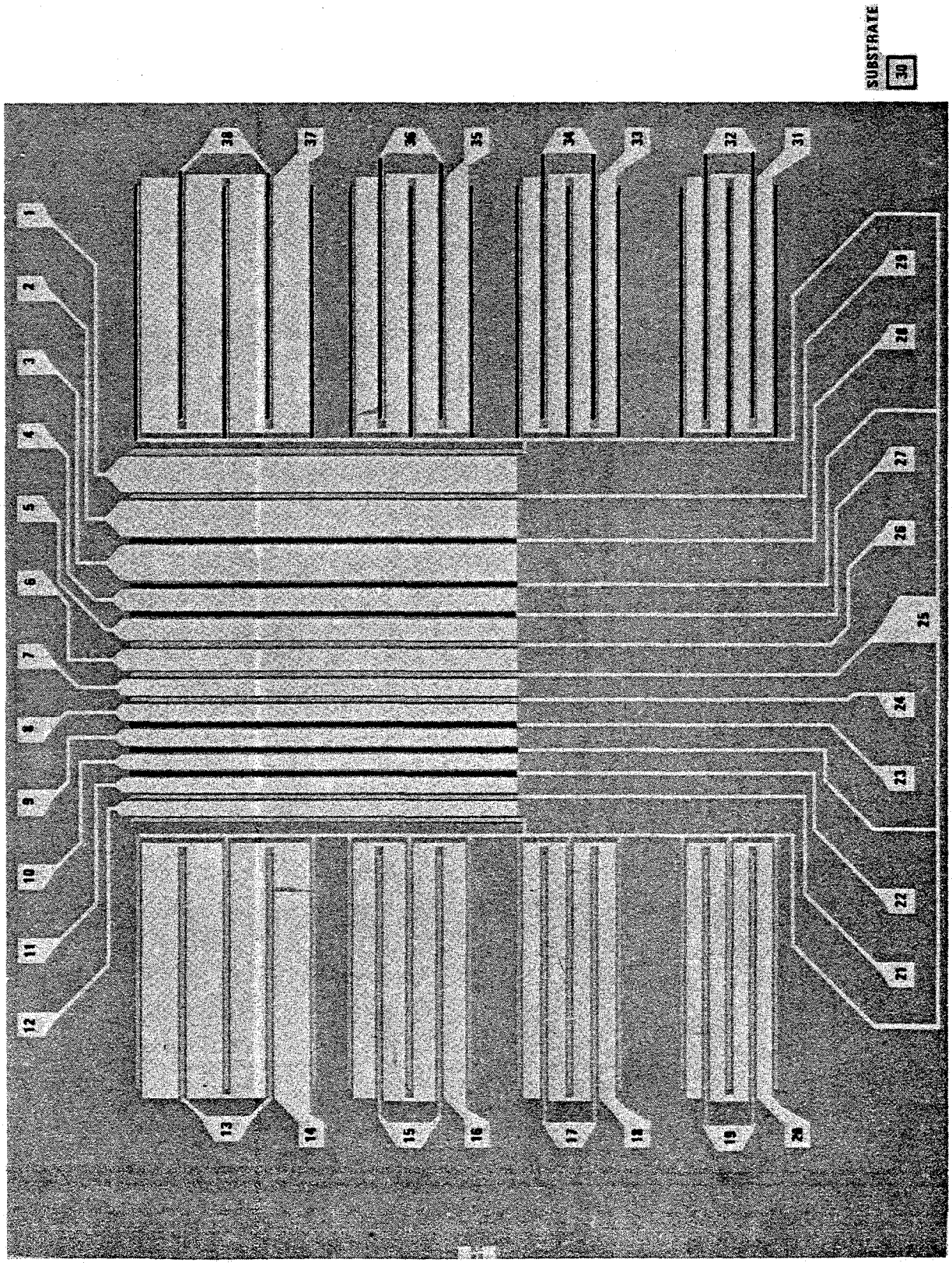



Fig. 3.1 Mask photograph showing layout of chip A.

is shown in Fig. 3.2. In Table IV, the numbered contact bonding pattern for these devices designating the sources, gates and drains of these individual devices as well as their type are given. For this chip, the common contact 29 serves as source for the P-P and N-N devices. The set of devices includes P-P (p-channel), N-N (CRYOFET) and mixed P-N types.

Table III
Bonding Pattern of CRYOFET and MOSFET Devices
(Chip A)

| L ( μm) | W (mils) | Device | D | G | S | D-S Type |
|---|---|---|---|---|---|---|
| 6 | 62.5 | I-6-62 | 22 | 10 | 25 | P-P |
| 15 | 62.5 | I-15-62 | 23 | 9 | 25 | P-P |
| 37.5 | 62.5 | I-37-62 | 27 | 4 | 25 | P-P |
| 93.8 | 62.5 | I-93-62 | 28 | 3 | 25 | P-P |
| 6 | 156 | I-6-156 | 32 | 31 | 25 | P-P |
| 15 | 156 | I-15-156 | 34 | 33 | 25 | P-P |
| 37.5 | 156 | I-37-156 | 36 | 35 | 25 | P-P |
| 93.8 | 156 | I-93-156 | 38 | 37 | 25 | P-P |
| 6 | 62.5 | II-6-62 | 21 | 12 | 25 | N-N |
| 15 | 62.5 | II-15-62 | 24 | 7 | 25 | N-N |
| 37.5 | 62.5 | II-37-62 | 26 | 6 | 25 | N-N |
| 93.8 | 62.5 | II-93-62 | 29 | 1 | 25 | N-N |
| 6 | 156 | II-6-156 | 19 | 20 | 25 | N-N |
| 15 | 156 | II-15-156 | 17 | 18 | 25 | N-N |
| 37.5 | 156 | II-37-156 | 15 | 16 | 25 | N-N |
| 93.8 | 156 | II-93-156 | 13 | 14 | 25 | N-N |
| 6 | 62.5 | III-6-62 | 22 | 11 | 21 | P-N |
| 15 | 62.5 | III-15-62 | 23 | 8 | 24 | P-N |
| 37.5 | 62.5 | III-37-62 | 27 | 5 | 26 | P-N |
| 93.8 | 62.5 | III-93-62 | 28 | 2 | 29 | P-N |

Contact 30 is connected to the chip substrate

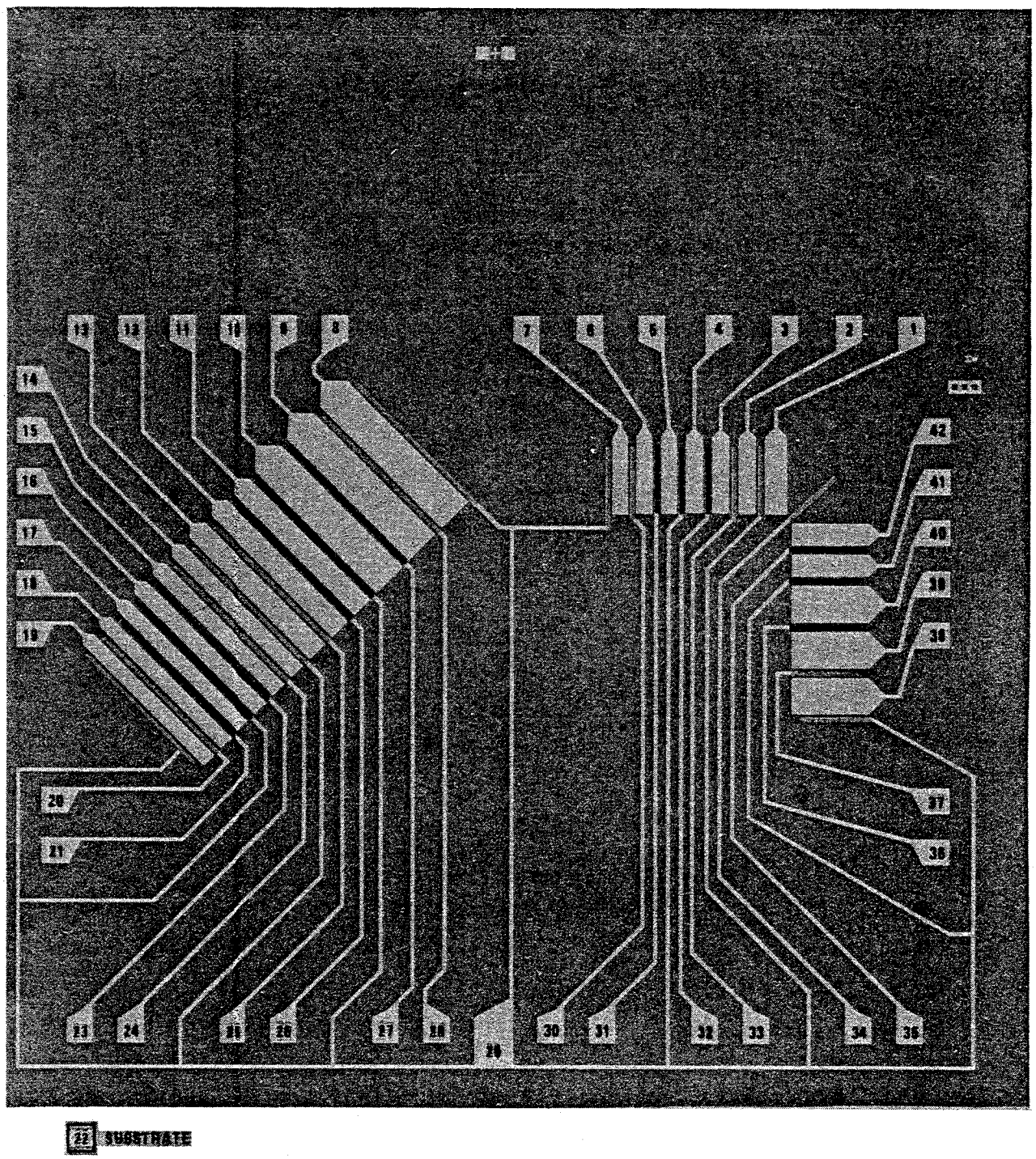



Fig. 3.2 Mask photograph showing layout of chip B.

Table IV

Bonding Pattern of CRYOFET and MOSFET Devices
(Chip B)

| L ( μm) | W (mils) | Device | D | G | S | D-S Type |
|---|---|---|---|---|---|---|
| 6 | 10 | I-6-10 | 31 | 5 | 29 | P-P |
| 15 | 10 | I-15-10 | 32 | 4 | 29 | P-P |
| 37.5 | 10 | I-37-10 | 35 | 41 | 29 | P-P |
| 93.8 | 10 | I-93-10 | 36 | 40 | 29 | P-P |
| 6 | 25 | I-6-25 | 21 | 17 | 29 | P-P |
| 15 | 25 | I-15-25 | 23 | 16 | 29 | P-P |
| 37.5 | 25 | I-37-25 | 26 | 11 | 29 | P-P |
| 93.8 | 25 | I-93-25 | 27 | 10 | 29 | P-P |
| 6 | 10 | II-6-10 | 30 | 7 | 29 | N-N |
| 15 | 10 | II-15-10 | 33 | 2 | 29 | N-N |
| 37.5 | 10 | II-37-10 | 34* | 1 | 29 | N-N |
| 93.8 | 10 | II-93-10 | 37 | 38 | 29 | N-N |
| 6 | 25 | II-6-25 | 20 | 19 | 29 | N-N |
| 15 | 25 | II-15-25 | 24 | 14 | 29 | N-N |
| 37.5 | 25 | II-37-25 | 25 | 13 | 29 | N-N |
| 93.8 | 25 | II-93-25 | 28 | 8 | 29 | N-N |
| 6 | 10 | III-6-10 | 31 | 6 | 30 | P-N |
| 15 | 10 | III-15-10 | 32 | 3 | 33 | P-N |
| 37.5 | 10 | III-37-10 | 35 | 42 | 34* | P-N |
| 93.8 | 10 | III-93-10 | 36 | 39 | 37 | P-N |
| 6 | 25 | III-6-25 | 21 | 18 | 20 | P-N |
| 15 | 25 | III-15-25 | 23 | 15 | 24 | P-N |
| 37.5 | 25 | III-37-25 | 26 | 12 | 25 | P-N |
| 93.8 | 25 | III-93-25 | 27 | 9 | 28 | P-N |

*Element 34 is Mispositioned on Mask
Contact 22 is connected to the chip substrate

These chips are separately mounted in 42 pin packages. The numbered contacts are referenced to the pin connections of the package as shown in Fig. 3.3. When mounting the packages in a dewar for test, it is necessary that the metallic base of the package be electrically insulated from the metallic heat sink of the dewar. This is conveniently accomplished by interposing a thin alumina plate between the package and the heat sink which provides electrical isolation as well as good thermal contact.

Some forty MOSFET and CRYOFET chips were scribed from the processed wafers and packaged. In Table V, the identification of these packages is given. Since the wafers in lot No. 1 proved to be shorted, no devices were packaged from this lot. The tabulated packages resulted from lot No. 2 which, as described in Section 3.0, received two different processing treatments. Also shown in Table V are those packages from which test data was obtained on this program. The three MOSFET packages delivered to NASA-Ames, in accordance with contract requirements, are also indicated.

Table V

CRYOFET and MOSFET Packages

| Substrate Resistivity (ohm•cm) | Wafer Nos. | Package Nos. (Field Oxide 3000-6000 Å) | Wafer No. | Package Nos. (Added 6000 Å Oxide; P Gettering) |
|---|---|---|---|---|
| 3.0 (N) | 69 | A-2-1*; A-2-2*; B-2-1*; B-2-2 | 68 | A-3-1; A-3-2*; (B-3-1) *; B-3-2* |
| 0.90 (N) | 127 | A-2-1*; A-S*; B-2-1*; B-S* | 126 | A-3-1; A-3-2; B-3-1; B-3-2; B-4-1*; B-4-2; |
| 0.22 (N) | 28 | A-2-1*; A-2-2; B-2-1*; B-2-2 | 27 | A-3-1; A-3-2; B-3-1; (B-3-2)* |
| 0.13 (N) | 137 | A-2-1*; A-2-2; B-2-1*; B-2-2 | 135 | A-3-1; A-3-2; B-3-1; B-3-2; B-4-1; (B-4-2)* |
| 1.9 (P) | "P" | A-2-1; A-2-2; B-2-1*; B-2-2 | | |

*Data obtained on this program
( ) MOSFET packages delivered to NASA-Ames.

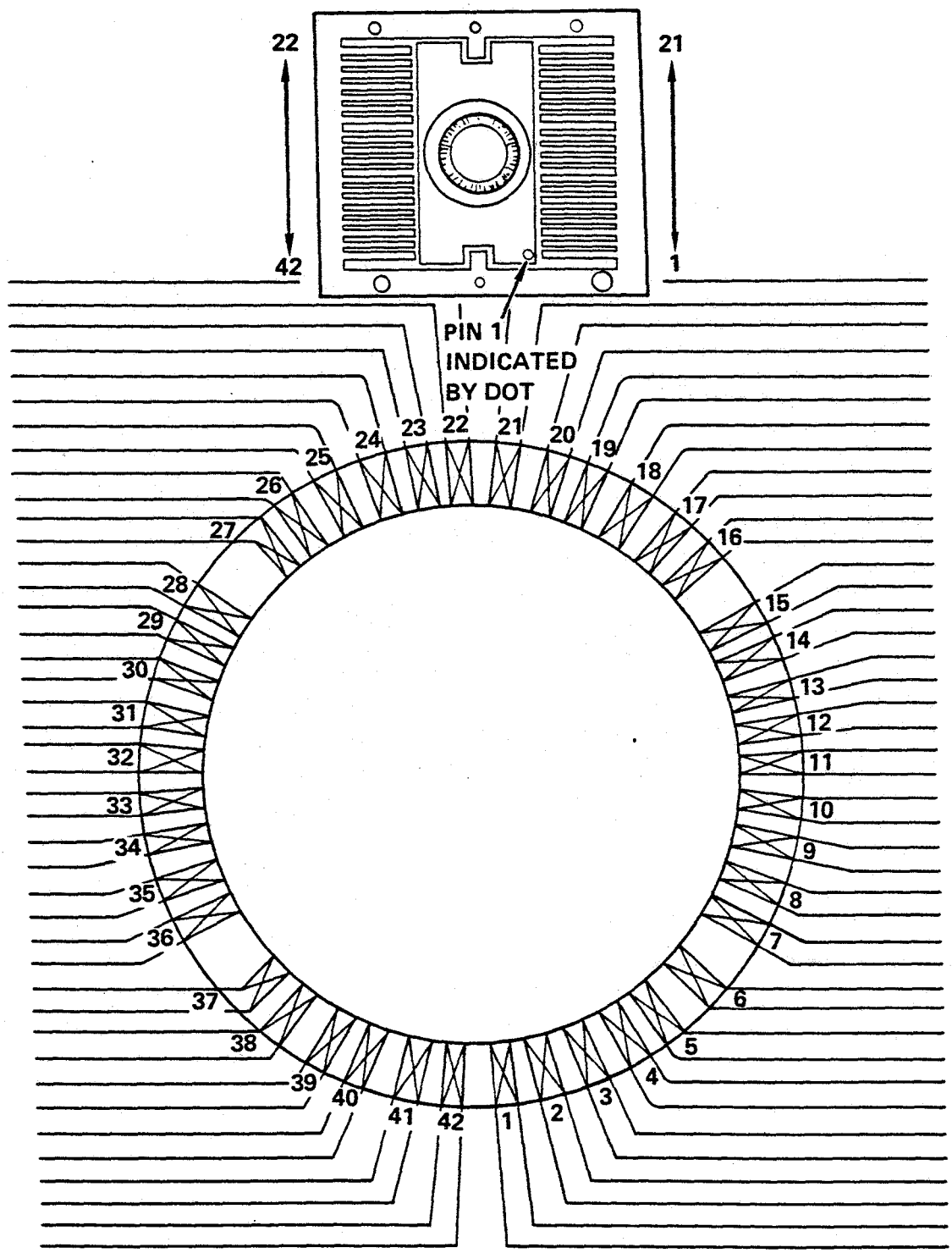



Fig. 3.3 Pin connections on package used with chip A and B.

## 4.0 CRYOFET AND MOSFET PROCESSING

CRYOFET and MOSFET processing was carried out using the 5 layer mask set described in Section 3.0. A selection of two inch diameter n type, arsenic doped silicon wafers oriented in the <100> crystal direction with varying doping concentrations were utilized. In addition, a p-type boron doped silicon wafer control was included. The selection used is shown in Table VI.

Table VI

N- and P-Type Wafers Used in Processing

| Wafer Nos. | ρ (300K) (ohm•cm | Type-Dopant | Doping Conc. ($cm^{-3}$) |
|---|---|---|---|
| 64-69 | 3.0 | N-Si:As | $1.6 \times 10^{15}$ |
| 122-127 | 0.90 | N-Si:As | $5.8 \times 10^{15}$ |
| 23-28 | 0.22 | N-Si:As | $3.1 \times 10^{16}$ |
| 132-137 | 0.13 | N-Si:As | $6.0 \times 10^{16}$ |
| "p" | 1.9 | P-Si:B | $7.0 \times 10^{15}$ |

Standard microelectronic processing with some modifications was used. This involves the growth of oxide, the application of photoresist, the exposure of the photoresist through a selected mask, the development of the photoresist and then the selective etching of the underlying oxide to provide window patterns for the diffusions and for the gate and contact definitions. To define the metal pattern, the photoresist is deposited over a layer of aluminum which is then selectively etched after the exposure and development of the photoresist. The sequence of the major processing steps is shown in Table VII.

Table VII

Sequence of Major Processing Steps

| | |
|---|---|
| 1 | Grow oxide |
| 2 | Apply photoresist |
| 3 | Expose photoresist (TC 2N mask) and develop |
| 4 | Etch N diffusion patterns in oxide |
| 5 | Predeposit/diffuse/predeposit phosphorus |
| 6 | Grow oxide |
| 7 | Apply photoresist |
| 8 | Expose photoresist (TC 1P mask) and develop |
| 9 | Etch P diffusion patterns in oxide |
| 10 | Predeposit/diffuse/predeposit boron |
| 11 | Grow oxide |
| 12 | Expose photoresist (TC 3G mask) and develop |
| 13 | Etch gate patterns in oxide |
| 14 | Grow gate oxide (1000 Å) |
| 15 | Apply photoresist |
| 16 | Expose photoresist (TC 4C mask) and develop |
| 17 | Etch contact patterns in oxide |
| 18 | Deposit aluminum layer (10,000 Å) |
| 19 | Apply photoresist |
| 20 | Expose photoresist (TC 5M mask) and develop |
| 21 | Etch aluminum |
| 22 | Sinter aluminum |

The principal modifications introduced in this processing, designed to accommodate to the low temperature application of these devices, were the addition of a pre-deposition step for the phosphorus and boron impurity treatment after the usual predeposition and drive sequence. This step was instigated guarantee degenerate impurity doping concentrations for the source and drains in order to avoid charge freeze out effects in these elements at low temperatures.

Two processing lots were completed. Processing difficulties were encountered in the first lot. Room temperature wafer probing revealed no evidence of diode action between the p-type sources and drains and the n-type substrate. The gates were found to be satisfactorily insulated from the substrate but the surface below the gates could not be inverted as required for MOSFET action. This suggested that either the gate oxide thickness or the conductivity of the silicon under the gate was excessive. Separate measurement on a control wafer indicated that the gate oxide was approximately 1000 Å in agreement with design goals. One of the processed wafers was then sectioned, stained and observed in cross-section. The p-type source and drains resulting from the boron diffusion were found to be 2.1-2.4 μm deep in agreement with design goals, but a 1.2-1.5 μm heavily doped p-type layer was found to extend over the surface of wafer. This layer prevented surface inversion and surface leakage prevented the observation of diode characteristics. The occurrence of this layer was identified to be the result of excessive oxide etching during the sequence to define the boron diffusion. This permitted the boron dopant intended for the source and drain areas to spread laterally to the rest of the wafer surface.

The second lot was processed in two groups. Probing results on p channel devices, performed at room temperature, yielded MOSFET characteristic curves but the voltage thresholds of the MOSFETs was noted to be abnormally high. Further, the breakdown voltage of the devices on the substrates with lightest doping, was limited by current leakage associated with charge inversion in the silicon under the aluminum leads passing from the pads to the source and drains. These leads are separated from the silicon by some 3000-6000 Å of field oxide.

It was not clear whether these observed room temperature probing limitations would limit performance at low temperature. To guard against this possibility, the lot was divided into two groups and additional processing was performed on one of these groups. This processing increased the thickness of the field oxide to about 12000 Å in order to minimize charge inversion.

Further, a phosphorus oxide gettering step designed to reduce threshold voltages was also implemented. Devices from both of these groups in lot 2 were packaged and compared at low temperatures. As reported in Section 5.0, leakage currents between the source and drain (in the absence of gate bias) were observed for the CRYOFET devices prepared without this additional processing. For the devices in the subgroup which received this additional treatment, this leakage was eliminated. Further, these devices also provided lower threshold voltages for both the conventional P-P as well as the N-N CRYOFETs. Accordingly, this additional processing is to be preferred and the bulk of the measurements reported in Section 5.0 deals with measurements on devices in this subgroup.

# 5.0 CRYOFET AND MOSFET MEASUREMENTS

Evaluation of the CRYOFET requires controlled comparative measurements of the properties of the device and conventional MOSFET versions under identical operational conditions. While some data already exists for conventional MOSFETs at low temperature, the performance characteristics and optimization criteria of the CRYOFETs are essentially unexplored. The processing mask, described in Section 3.0, permits a wide range of device geometries to be studied. The range of substrate resistivities used in the processing, described in Section 3.0, permits the effect of impurity concentration to be studied. The measurement plan evolved on this program was designed to facilitate these studies and to provide the required comparative measurements based on the intended use of these devices as high impedance detector preamplifiers. This requires operation in the source-follower mode with bias selected to promote a gain near unity.

## 5.1 Measurement Plan

### 5.1.1 Room Temperature Measurements

The processed wafers were initially probed at room temperature. Only the conventional MOSFET type are expected to exhibit MOSFET characteristics, i.e., the P type source/drains on n-type substrates and the N type source/drains on p-type substrates. These devices were checked for gate-controlled channel turn-on and for shorts and opens. The CRYOFETs with their N type source/drains on n type substrates exhibited source-drain shorts while the mixed types with source and drains of different conduction type exhibited diode action between the source and drain. All gates are required to be electrically isolated from the substrate. The probe results were used to verify satisfactory processing and to select wafers and die for packaging, in preparation for the cryogenic measurements. When packaging was completed, selected conventional devices were measured at room temperature for MOSFET characteristics. These measurements, which were repeated at cryogenic

temperatures consisted of characteristic MOSFET curves ($I_{DS}$ vs $V_{DS}$ for various $V_{GS}$), $V_T$, threshold voltage at which channel conduction initiates, leakage and junction breakdown voltage, $V_{BVD}$, at which the gate voltage loses control of the current and gate breakdown voltage, $V_{BVG}$. The schematic circuit approaches to these measurements are shown in Fig. 5.1. Since gate breakdown results in gate destruction, this test was limited to exploratory trials and was omitted from the standard test sequence. Capacitance measurements (described in 5.1.2) were also performed at room temperature.

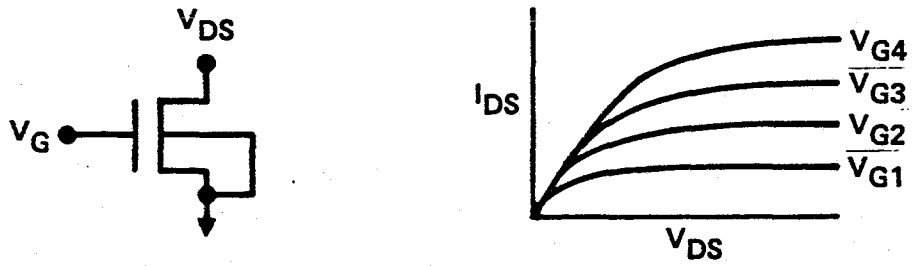
### 5.1.2 Cryogenic Measurements

The die packaged in 42-pin packs were installed in a helium dewar for the cryogenic tests. A fixture to accommodate the packs was mounted on the dewar heat sink and included a heater to raise the temperature of the devices and a thermometer to sense the temperature. In the early measurements, an Allen Bradley 5.1 K ohm resistor was used as the thermometer. A previously calibrated resistance curve covering the range of 4.2-45 K was utilized. For temperatures below 4.2 K, the forward voltage drop across a silicon diode passing 1 μamp current was utilized. An existing calibration curve to 4.2 K was linearly extrapolated for the lower temperatures. These lower temperatures were obtained by reducing the vapor pressure above the liquid helium reservoir. The lowest temperature achieved was approximately 2.4 K.

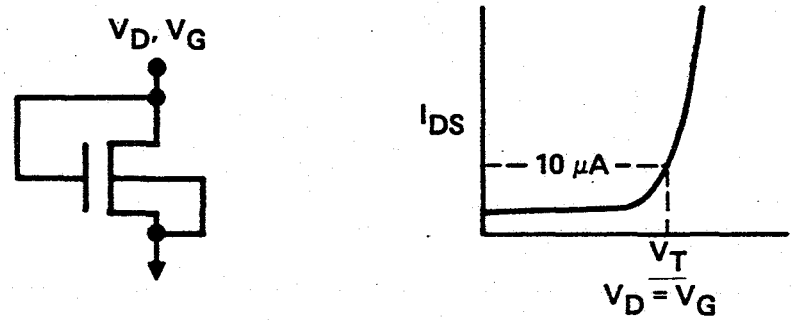
Similar MOSFET characterization screening tests as were carried out at room temperature were performed at the cryogenic temperatures. At these temperatures, the MOSFET measurements were supplemented by measurements on the CRYOFETs (cryogenic MOSFETs). For the CRYOFETs, the opposite polarity voltage is used on the gate and drain.

Following the preliminary curve-tracer screening, representative samples of those device types and geometries which exhibited acceptable characteristics were chosen for detailed evaluation of preamplifier performance parameters. These included the gate-to-source capacitance, the source-follower gain and the noise as a function of frequency and temperature.

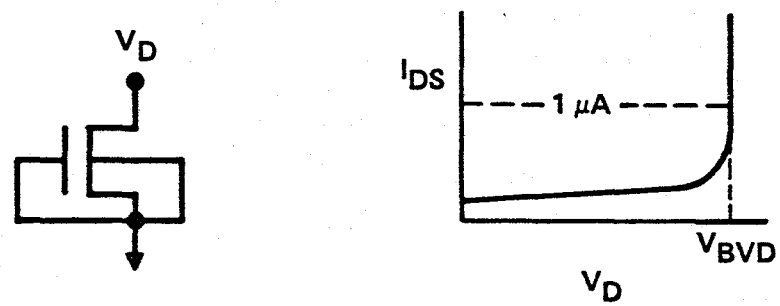
(a) CHARACTERISTIC CURVES




(b) THRESHOLD VOLTAGE




(c) LEAKAGE AND JUNCTION BREAKDOWN




(d) GATE BREAKDOWN

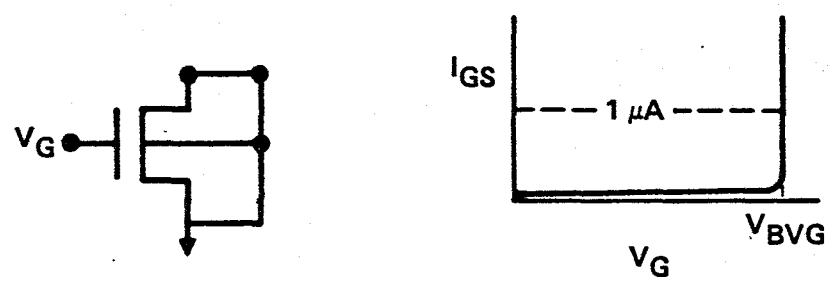



Fig. 5.1 Curve-tracer measurements.

5.1.2.1 Capacitance

The gate-source capacitance measurements were performed using the test set-up depicted in Fig. 5-2. Coaxial leads from the dewar gate and source terminals were fed to the PAR C-V plotter. The C-V plotter measures the capacitance as a function of dc bias applied to the gate. This capacitance is determined by the application of a 1 MHz small signal to the gate and the measurement of the current at 90° phase shift by the use of a phase sensitive lock-in amplifier. The system is calibrated by use of known standard capacitors. This procedure subtracts out the capacitance to ground contributions of the cables. To account for the parasitic capacitance associated with the chip and the package in which the chip is mounted, a fixed capacitance value was subtracted from the measured capacitance values of the devices. This fixed value was deduced by scaling the reduced capacitance values so that they became proportional to the gate areas of the MOSFETs or CRYOFETs for each width set.

5.1.2.2 Source-Follower Gain

The source-follower gain measurements were performed using the test set-up shown schematically in Fig. 5.3. A 10 mV sine wave reference signal derived from the Quantek Wave Analyzer was impressed on the MOSFET or CRYOFET gate and the source-follower output of the device using a $10^5$ ohm source load resistor was fed to the input of the wave analyzer. The gate and drain of the MOSFET or CRYOFET were biased up in common with the voltage adjusted to provide a gain of 0.98 where this value could be achieved. The polarity of the bias shown applies to the CRYOFET. The polarity of this voltage is reversible to accommodate the conventional MOSFETs. The wave analyzer follows the reference signal in frequency and can be automatically swept across a frequency range. The system was calibrated to a gain of one by feeding the reference signal directly back to the input of the wave analyzer.

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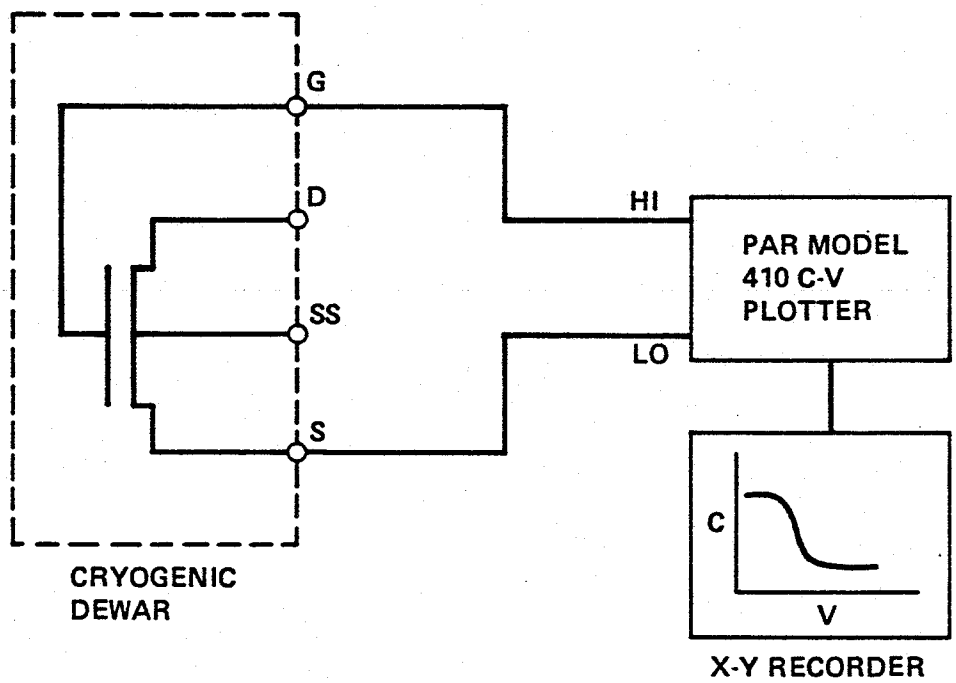


Fig. 5.2 Gate-to-source capacitance test setup.

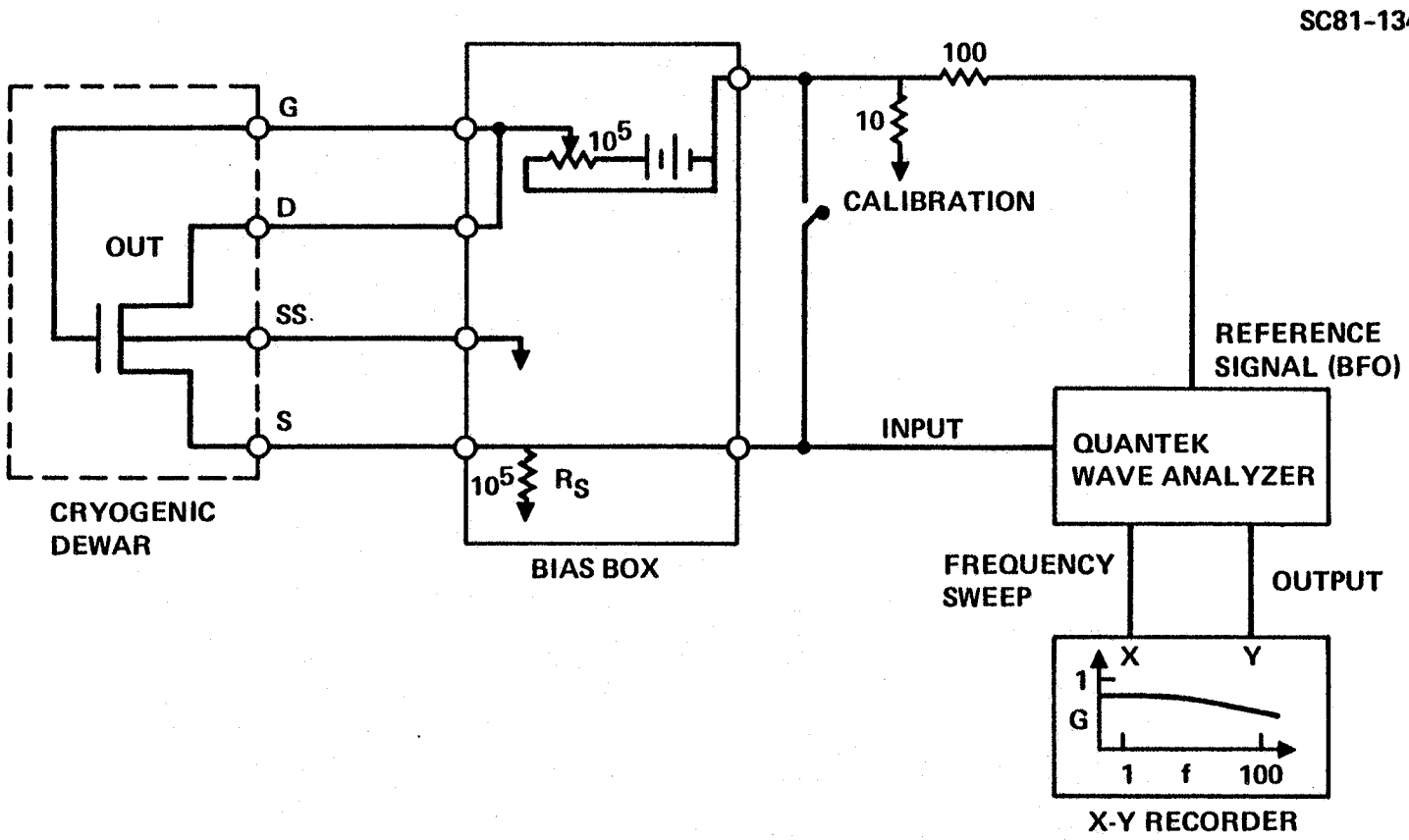


Fig. 5.3 Source-follower gain test setup.

5.1.2.3 Noise

The noise measurements were performed using the test set-up shown schematically in Fig. 5.4. These measurements followed those of the gain measurements and were made under the same bias conditions. This allowed the noise measurements to be compared under identical MOSFET or CRYOFET gains which were adjusted to be equal to 0.98 where this value could be achieved. The noise spectrum was measured over the 1-100 Hz frequency range using the Hewlett Packard 3582 Spectrum Analyzer. The PAR 113 amplifier was operated in the ac mode because this is easier to experimentally perform. As is demonstrated, the noise spectrum measured was found to be identical with that obtained with operation in the dc mode after the dc source offset voltage was compensated.

## 5.2 Measurement Results

In this section, measurement results and analyses of these results, where appropriate, are presented. It is convenient to initiate the presentation with the gate to source capacitance measurements.

### 5.2.1 Gate to Source Capacitance

The gate to source capacitance of the MOSFET or CRYOFET, when operated as a source-follower detector preamplifier, can influence signal/noise optimization dependent on the choice of load resistor and operating frequency. The capacitance consists of the in-series sum of the capacitance of the gate oxide and of a capacitance associated with a possible space charge region in the silicon under the gate. In general, for high quality oxide, the capacitance is essentially independent of voltage and temperature. For the silicon, the voltage dependence depends on the voltage polarity. Negative polarity in n-type silicon depletes the silicon surface under the oxide and yields a voltage dependent capacitance. Positive polarity accumulates negative charge and has the effect of extending the source/drain contacts. The voltage dependence in this case is minor. Since the CRYOFETs operate with this polarity in the accumulated mode, the capacitance measured under this

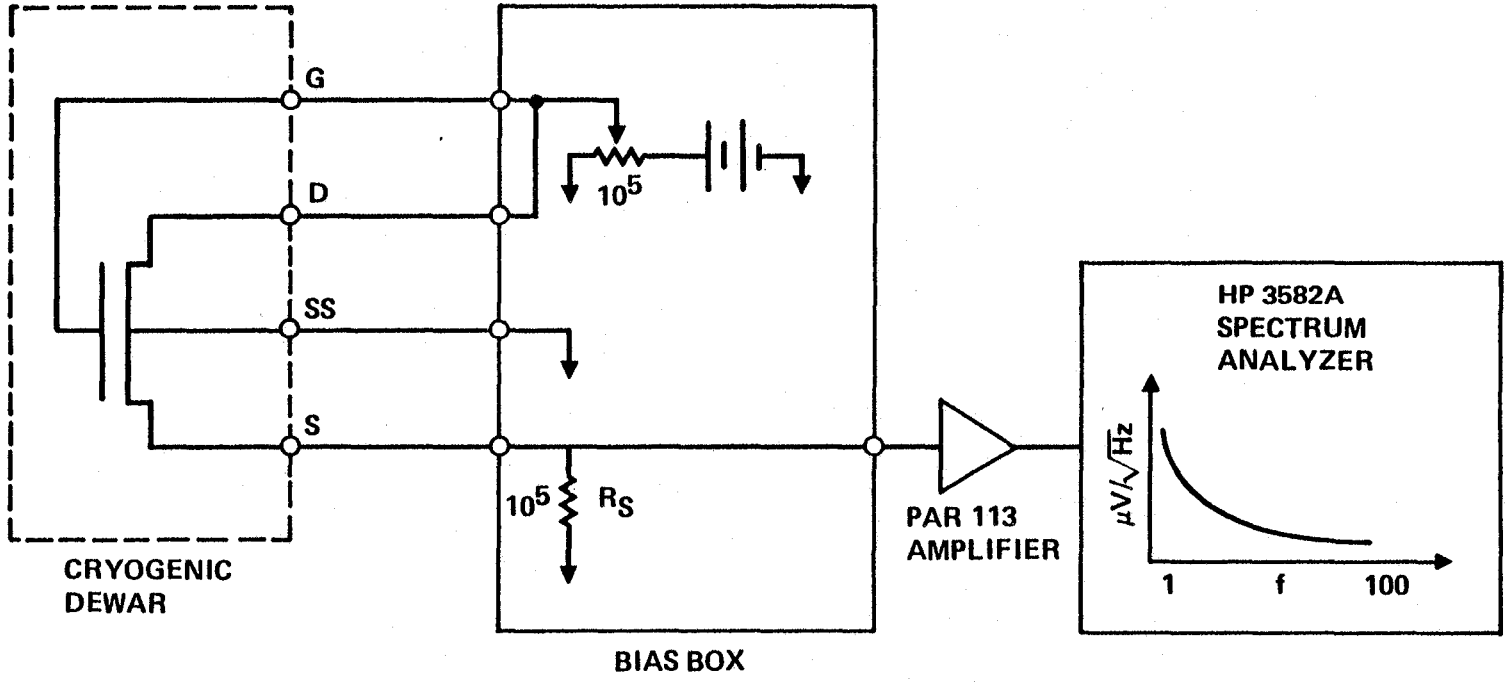


Fig. 5.4 Noise test setup.

condition is appropriate. This capacitance is expected to be essentially that of the gate oxide with the substrate playing a minor role. Experimental mesurements are presented which are consistent with these considerations.

Gate to source capacitance measurements have been performed at ambient and cryogenic temperatures as a function of gate voltage for both polarities. As expected, surface depletion leading to a reduced capacitance was observed for the negative polarity but the capacitance with positive polarity was essentially independent of voltage. In some cases, at low temperatures, a minor shallow maximum of less than 10 percent was observed.

In Table VIII, the results of the measured values of gate to source capacitance obtained for this positive polarity are tabulated for the N-N CRYOFETs and P-P MOSFETs (columns 2 and 3) in package No. 127-B-2-1 at room temperature.

Table VIII

Measured, Reduced and Calculated Values of Gate-Source Capacitance, Package No. 127-B-2-1 at 300 K

| Device | N-N Type Measured Values, (pfd) | P-P Type Measured Values, (pfd) | Reduced Values, (pfd) | Calculated Values, (Pfd) |
|---|---|---|---|---|
| 6-10 | 3.2 | 3.4 | 0.3 | 0.48 |
| 15-10 | 4.4 | 4.0 | 1.2 | 1.2 |
| 37-10 | 5.6 | 6.6 | 3.1 | 3.0 |
| 93-10 | 10.3 | 10.2 | 7.3 | 7.5 |
| 6-25 | 6.0 | 6.0 | 1.0 | 1.2 |
| 15-25 | 7.0 | 7.6 | 2.3 | 3.0 |
| 37-25 | 10.1 | 10.4 | 5.3 | 7.5 |
| 93-25 | 18.7 | 19.0 | 13.8 | 18.7 |

The measured values include parasitic contributions from the chips and the flat pack. Near identical values are obtained for the N-N CRYOFETs and P-P MOSFETs of similar geometry. The reduced values were obtained by deducing a common capacitance, $C_o$, value for each MOSFET or CRYOFET width which was subtracted from the measured values. This capacitance was obtained by requiring the reduced values to scale with the MOSFET or CRYOFET gate areas. A sample calculation applicable to the 25 mil width device to obtain this value is shown below. Three ratios are formed of the 93.8/37.5, 37.5/15 and 15/6 micron MOSFET or CRYOFET channel lengths and the indicated equations were solved for $C_o$. The measured capacitance values used were the average of the values tabulated in column 2 and 3. The average of the $C_o$ was then used to reduce the measured values to those tabulated in column 4. The $C_o$ values obtained by this procedure are $C_o$ = 3.0, 5.0 and 11.2 for the respective 10, 25 and 62.5 mil MOSFET or CRYOFET gate widths.

$$\frac{93-25}{37-25}: \quad \frac{18.8_5 - C_o}{10.2_5 - C_o} = \frac{93.8}{37.5} = 2.5 \; ; \; C_o = 4.5 \text{ pfd}$$

$$\frac{37-25}{15-25}: \quad \frac{10.2_5 - C_o}{7.3 - C_o} = \frac{37.5}{15} = 2.5 \; ; \; C_o = 5.3 \text{ pfd}$$

$$\frac{15-25}{6-25}: \quad \frac{7.3 - C_o}{6.0 - C_o} = \frac{15}{6} = 2.5 \; ; \; C_o = 5.1 \text{ pfd}$$

$$\langle C_o \rangle = 5.0 \text{ pfd} \; .$$

The reduced values are compared with calculated oxide capacitance values using $K_{ox} = 3.9$, the measured oxide thickness of 1100 Å and the tabulated area values of Table I. The calculation is based on the parallel plate capacitance formula

$$C_{ox} = \frac{K_{ox}\ \varepsilon_o\ A}{d}\ \text{pfd} \qquad (4)$$

where $K_{ox}$ is the dielectric constant of the oxide,
$A$ is the area of the oxide,
$d$ is its thickness,
and $\varepsilon_o$ is the permittivity of free space = $8.85 \times 10^{-2}$ pfd/cm.

Approximate agreement within about 25% between the calculated values and the reduced values is obtained. In Table IX, the results for the T = 5 K measurements are tabulated for the N-N devices in package No. 127-B-2-1.

Table IX

Measured, Reduced and Calculated Values of Gate-Source Capacitance No. 127-B-2-1 (5 K)

| Device | N-N Type Measured, (pfd) | Reduced Values, (pfd) | Calculated Values, (pfd) |
|---|---|---|---|
| 6-10 | 3.5 | 0.5 | 0.48 |
| 15-10 | 4.3 | 1.3 | 1.2 |
| 37-10 | 5.5 | 2.5 | 3.0 |
| 93-10 | 10.0 | 7.0 | 7.5 |
| 6-25 | 5.8 | 1.1 | 1.2 |
| 15-25 | 6.8 | 2.1 | 3.0 |
| 37-25 | 10.0 | 5.3 | 7.5 |
| 93-25 | 18.4 | 13.7 | 18.7 |

These measurements give results that are virtually unchanged from the 300 K results of Table VIII and agree equally well with the calculated values.

The lack of a temperature dependence and the general agreement with calculations based on the oxide capacitance, indicates that the gate-source capacitance of the CRYOFETs is essentially that of the gate oxide capacitance when parasitic capacitance values are subtracted out, in agreement with theoretical expectations.

Incomplete capacitance measurements were performed on the devices of package No. 127-A-2-1 of 62.5 and 156 mil widths at room temperature. Spot checks indicated that the reduced values gave comparable good agreement with calculated oxide capacitance values. Accordingly, the calculated values for the devices in No. 127-A-2-1 are tabulated for reference in Table X.

Table X

Calculated Gate-Source Capacitance
(No. 127-A-2-1 at 300K)

| MOSFET Device | Calculated Values, (pfd) |
|---|---|
| 6-62 | 3.0 |
| 15-62 | 7.5 |
| 37-62 | 18.7 |
| 93-62 | 46.8 |
| 6-156 | 7.5 |
| 15-156 | 18.7 |
| 37-156 | 46.8 |
| 93-156 | 117 |

The reduced and calculated gate-source capacitance values in Tables VIII, IX, and X apply to the indicated MOSFET or CRYOFET devices. When they are packaged, some parasitic capacitance must be accepted. In well designed packages appropriate for individual devices, this may aggregate an additional 0.5 to 1.0 pfd.

### 5.2.2 CRYOFET and MOSFET Characteristic Curves

The characteristic curves, the voltage threshold and the source-drain leakage are important parameters that control the MOSFET or CRYOFET performance. In this section, we first present data obtained from the first group in lot 2. this group exhibited threshold and leakage problems which were corrected in the second group of lot No. 2.

As discussed in Section 3, the set of devices consists of 4 widths, W, and 4 channel lengths, L, and each set includes two chips, A and B. The photographed I vs V characteristics at T = 300 for a set of conventional MOSFETs (P-P) fabricated in wafer No. 127 ($\rho$ = 0.9 W cm) are shown in Figs. 5-5, 5-6, and 5-7. Measured values of $V_T$ and $V_{BVD}$ are tabulated in Fig. 5-7. The expected geometry trend for MOSFET device transconductance $(\frac{\Delta I}{\Delta V_G})$ to be proportional to W/L appears to be realized. The measured $V_T$ value based on the customary arbitrary criteria (I = 10 μamps), shows an unexpected approximate correlation with MOSFET channel length. This criteria is based on the assumed linear current dependence of the MOSFET on voltage at low drain voltages. The threshold may also be obtained from the saturation range of the MOSFET where $I_{D,S} \alpha (V_{GS}-V_T)^2$. For this determination the square root of the measured $I_{D,S}$, in the saturated range, is plotted against $V_{GS}$ and extrapolated to $I_{DS}$ = 0 where $V_T = V_{GS}$. An example of this procedure is shown in Fig. 5-8 for MOSFET I-37-10. These $V_T$ values also appear in the tabulation. While the values tend to be somewhat lower, they do not differ significantly. Both sets indicate a higher than expected threshold voltage which suggests that the concentration of surface states at the silicon-oxide interface may be excessive.

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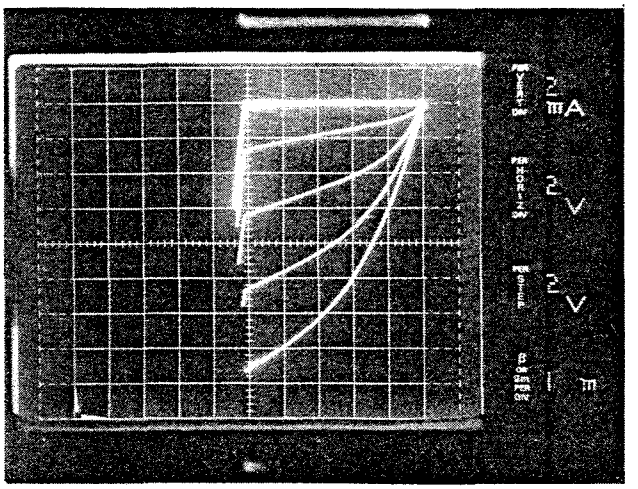
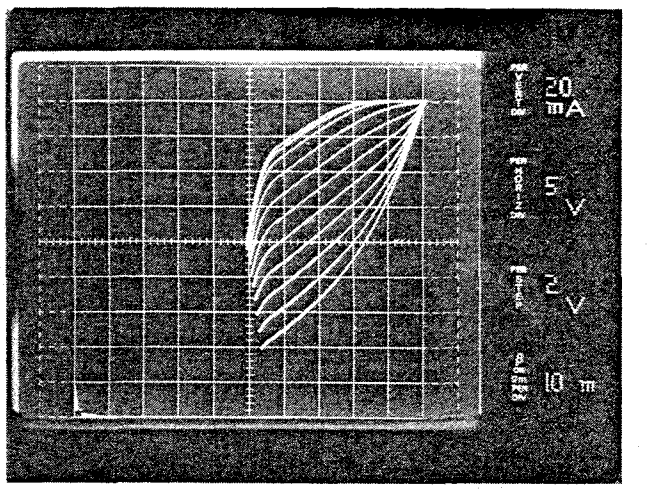
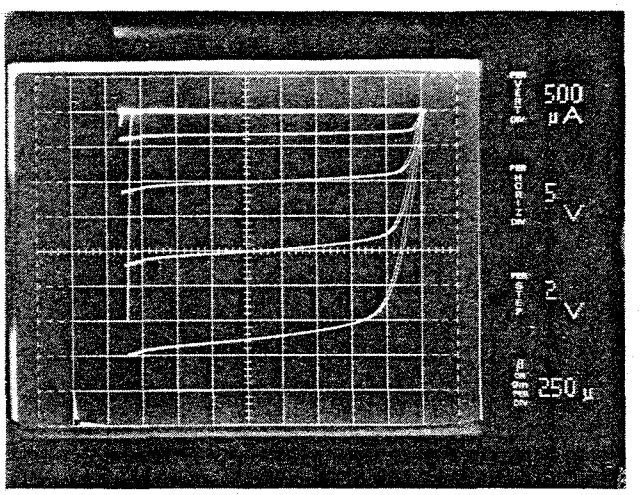


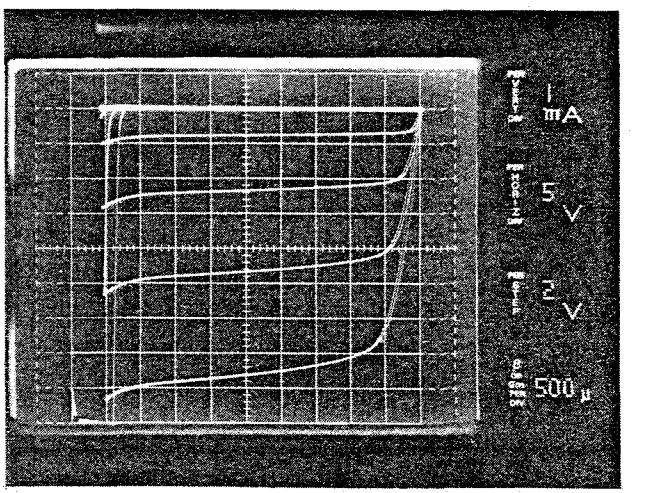

# 1 – 127-B-S; I-6-10 (P-P); 300 K



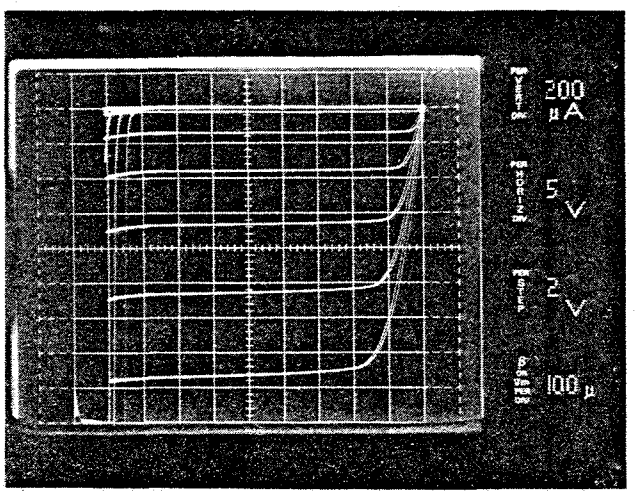

# 2 – 127-B-S; I-6-25 (P-P); 300 K



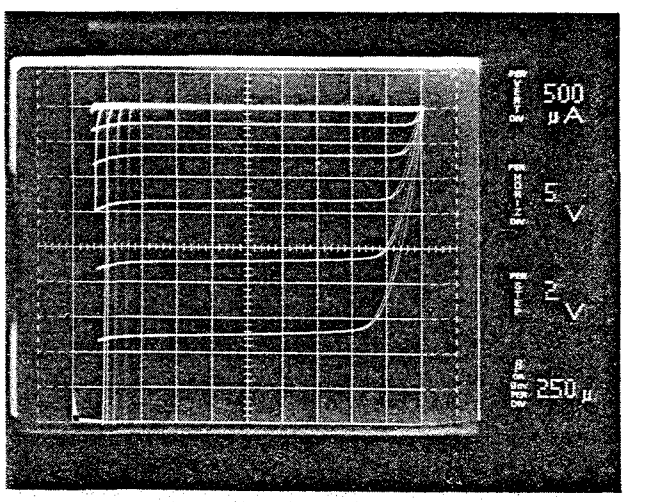

# 3 – 127-B-S; I-15-10 (P-P); 300 K




# 4 – 127-B-S; I-15-25 (P-P); 300 K




# 5 – 127-B-S; I-37-10 (P-P); 300 K




# 6 – 127-B-S; I-37-25 (P-P); 300 K

Fig. 5.5 I vs V characteristics showing MOSFET geometry effects (I) (T = 300K).

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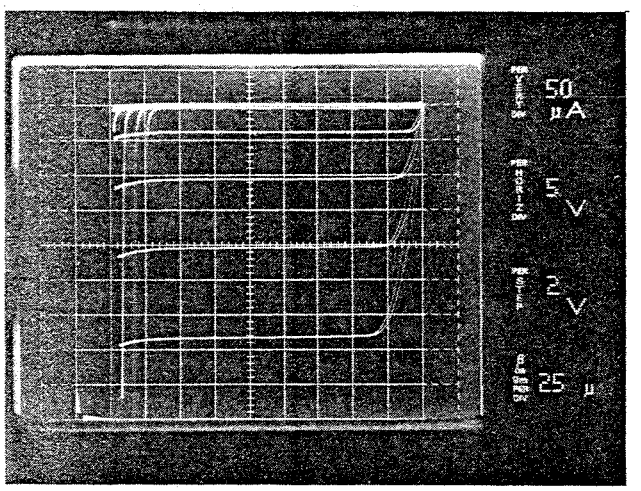
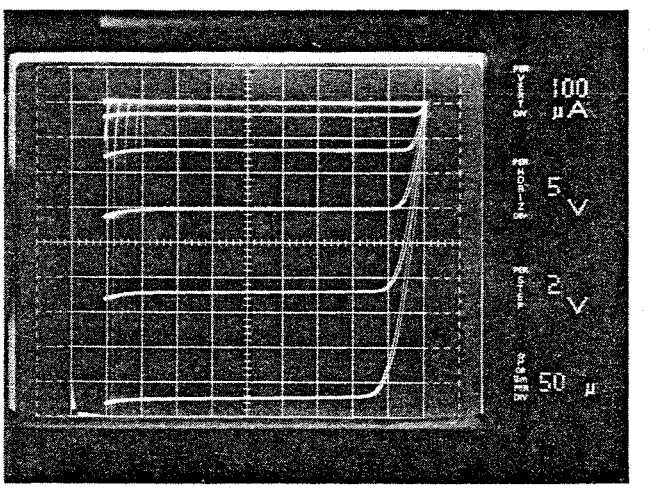
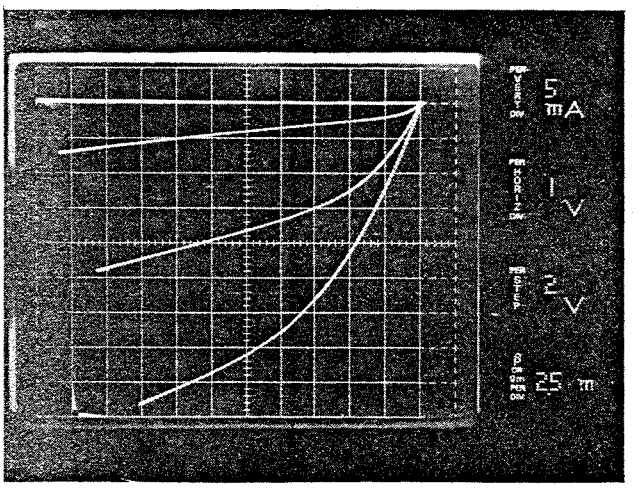


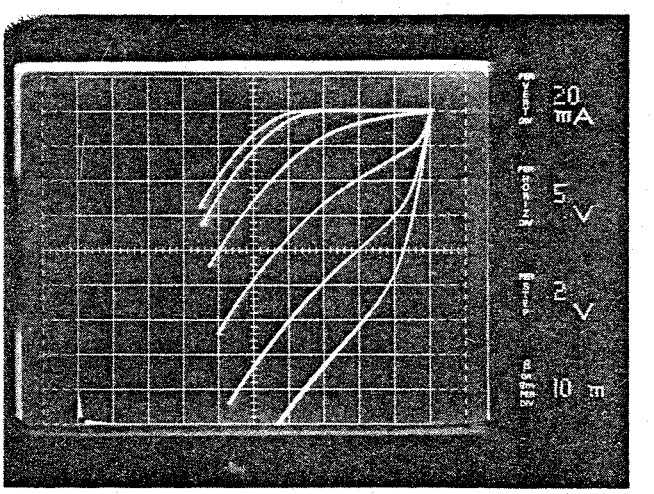

#1 – 127-B-S; I-93-10 (P-P);300 K



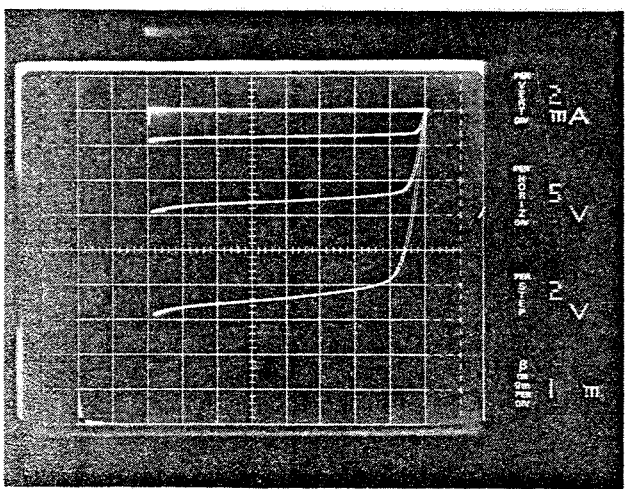

#2 – 127-B-S; I-93-25 (P-P); 300 K



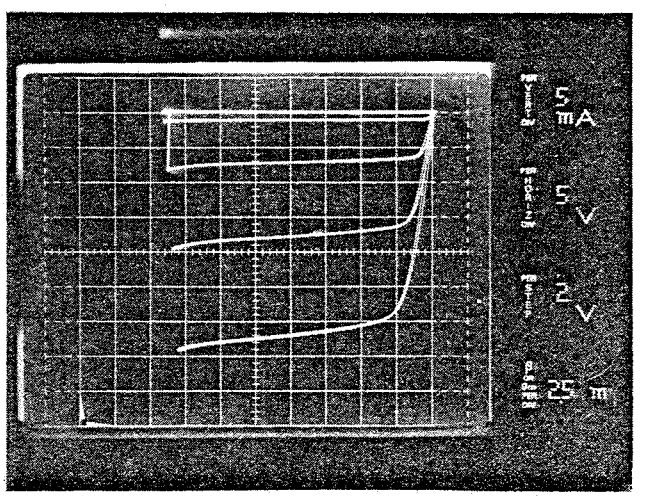

#3 – 127-A-S; I-6-62 (P-P); 300 K




#4 – 127-A-S; I-6-156 (P-P); 300 K




#5 – 127-A-S; I-15-62 (P-P); 300 K




#6 – 127-A-S; I-15-156 (P-P); 300 K

Fig. 5.6 I vs V characteristics showing MOSFET geometry effects (II) (T = 300K).

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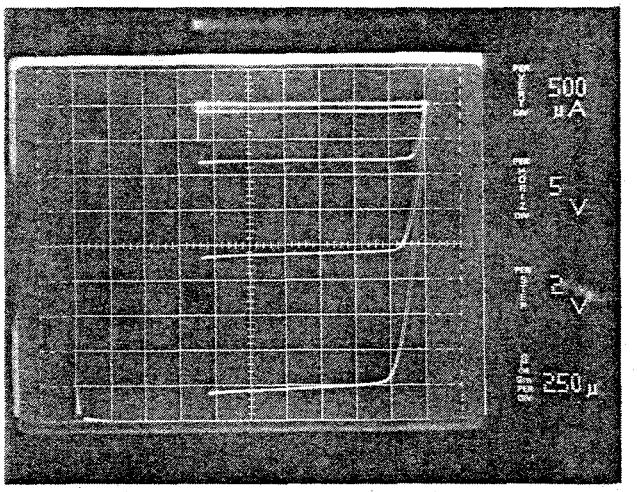
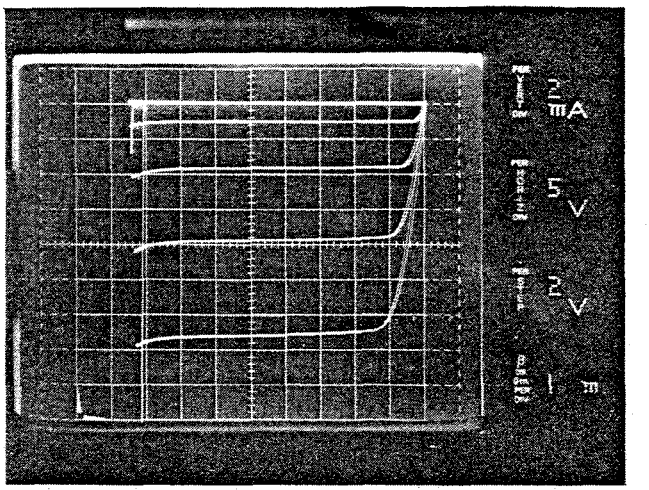
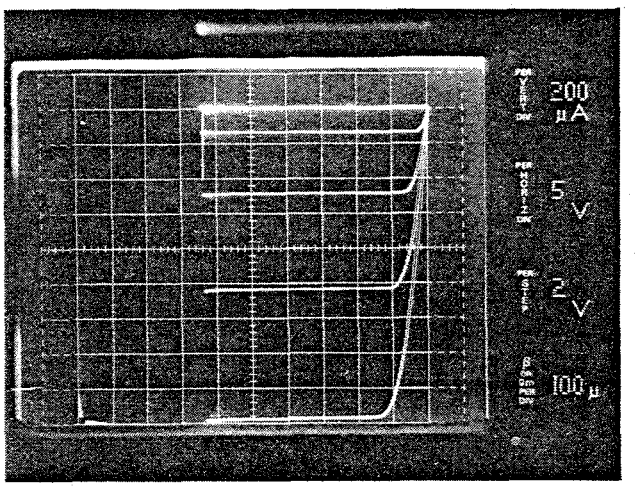


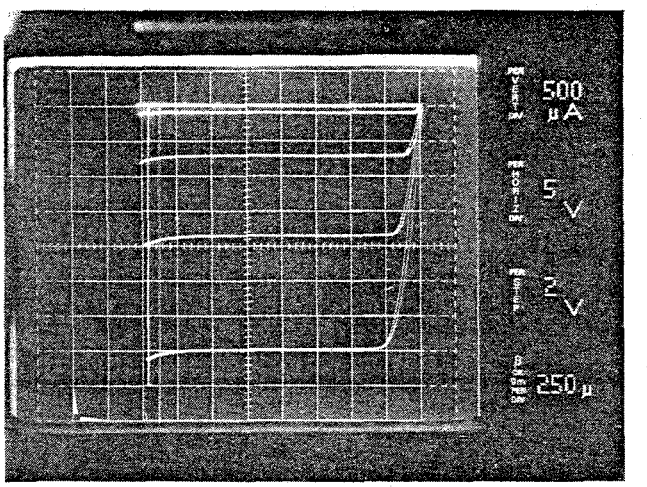

#1 — 127-A-S; I-37-62 (P-P); 300 K




#2 — 127-A-S; I-37-156 (P-P) 300 K




#3 — 127-A-S; I-93-62 (P-P); 300 K




#4 — 127-A-S; I-93-156 (P-P) 300 K

| | 127-B-S | | | | 127-A-S | | |
|---|---|---|---|---|---|---|---|
| DEVICE | $V_T$ @ 10 μa (MEASURED) | $V_T$ (I vs V) | $V_{BVD}$ @ 1 μa | DEVICE | $V_T$ @ 10 μa (MEASURED) | $V_T$ (I vs V) | $V_{VBD}$ @ 1μa |
| I-6-10 | 5.6 V | — | 10 V | I-6-62 | 4.4 V | — | 18 V |
| I-15-10 | 7.8 | 6.8 | >30 | I-15-62 | 5.8 | 5.9 | >35 |
| I-37-10 | 9.4 | 8.4 | >30 | I-37-62 | 7.2 | 6.6 | >30 |
| I-93-10 | 10.2 | 8.7 | >30 | I-93-62 | 8.3 | 7.5 | >30 |
| I-6-25 | 3.4 | — | 4 | I-6-156 | 3.4 | — | 14 |
| I-15-25 | 7.6 | 7.4 | >35 | I-15-156 | 4.8 | 4.2 | >35 |
| I-37-25 | 9.5 | 8.8 | >35 | I-37-156 | 5.8 | 5.6 | >35 |
| I-93-25 | 11.0 | 9.7 | >35 | I-37-156 | 7.1 | 6.6 | >35 |

Fig. 5.7 I vs V characteristics showing MOSFET geometry effects (III) (T = 300 K).

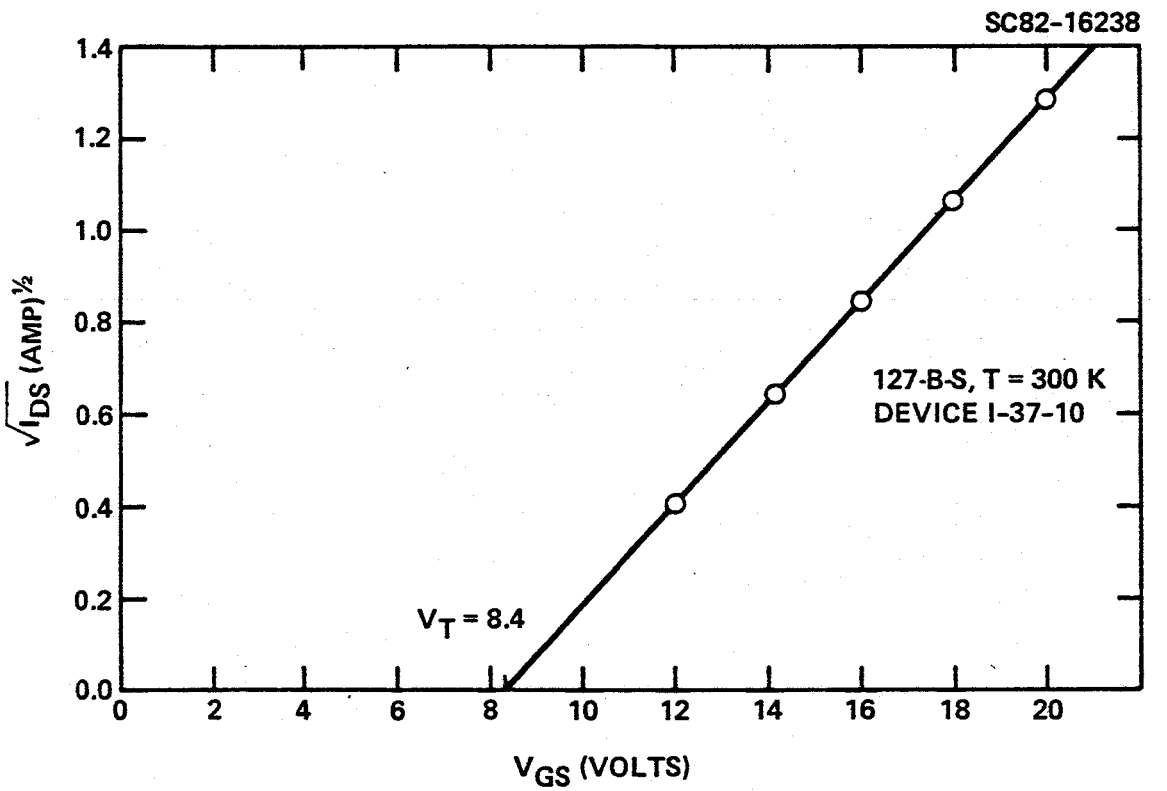



Fig. 5.8 MOSFET threshold determination from I vs V characteristic.

The low temperature characteristics of selected conventional MOSFETs formed in wafer No. 127 are shown in Fig. 5-9. These data were taken nominally at 4.2 K but the power dissipated in the devices under test, raised the devices to the indicated temperature. At the lowest power at which characteristics can be obtained on the curve tracer, the conventional P-P (p-channel) devices show marked hysteresis effects. As the power is increased (and temperature raised), the characteristics clean up and the hysteresis vanishes. The characteristic for I-37-25 at different current (and power) levels, photos No. 2 and No. 4, shows this effect.

The characteristics of selected N-N CRYOFETs devices on this chip are shown in Fig. 5.10. These devices all show families of I vs V curves that are free of hysteresis effects. There is, however, evidence of current leakage between the source and drains without any applied gate voltage. The characteristics on the left side of the page, photos No. 1, No. 3, and No. 5, were obtained without any gate offset voltage. Those on the right side were obtained with selected opposed offset voltages in an attempt to minimize this leakage. The source-drain channel resistance associated with this leakage scales up approximately with the device channel length aggregating approximately 60, 125, 350, and 800 ohms for the respective 6, 15, 37.5 (not shown) and 93.8 micron channel lengths. The effect of the opposed offset gate voltage increases this resistance (decreases leakage current) to about 5000 ohms. The presence of leakage does not rule out the use of the CRYOFETs but it does limit its range of applicability. Fortunately, as will be shown, it was eliminated by the additional processing carried out with the subgroup of lot No, 2.

The low temperature tests on MOSFETs and CRYOFETs formed on wafer 69 (3.0 ohm cm) of this series showed qualitatively similar characteristics. This includes the hysteresis effects in the P-P devices and the leakage currents in the N-N devices. In Fig. 5.11, one characteristic of a P-P device is shown, photo No. 1, and several N-N CRYOFETs. Leakage current is reduced with gate offset voltage to increase source to drain resistance to about 30 K ohm. In the presence of this leakage it is possible to operate the CRYOFETs in the depletion mode. This is shown in the bottom characteristic of photo No. 5.

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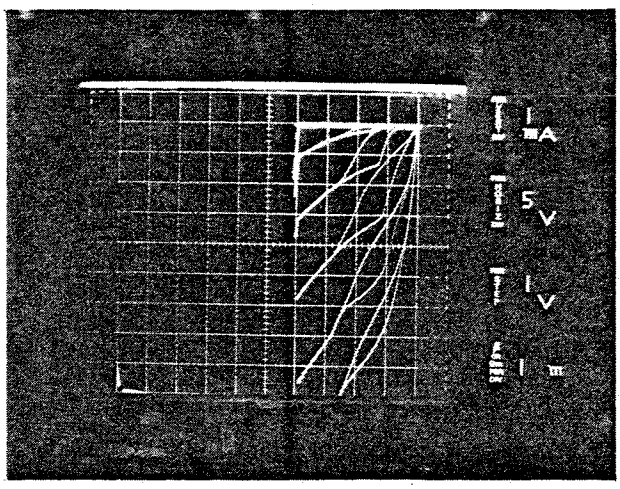
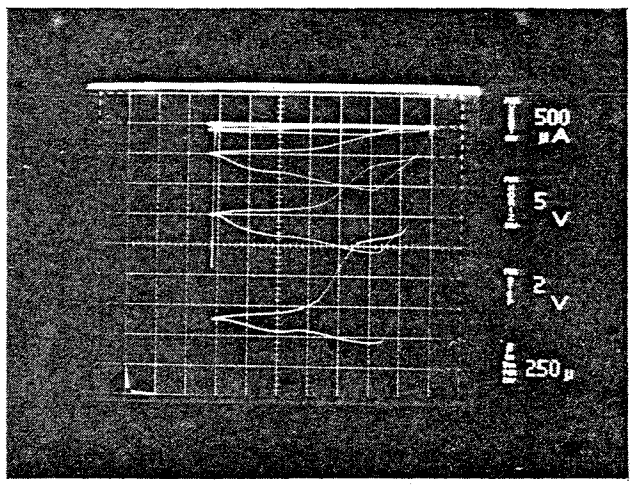
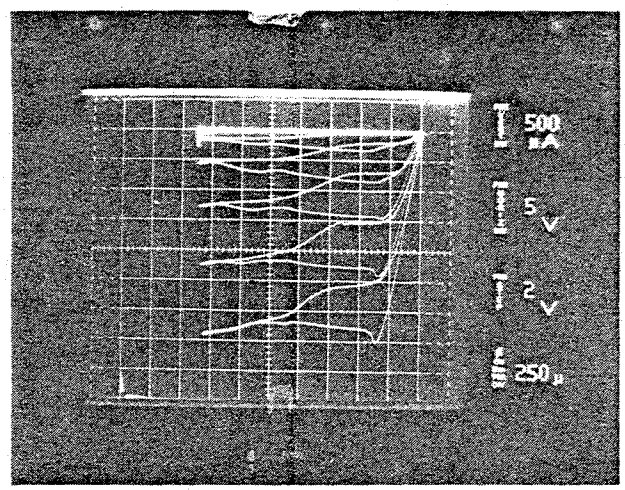


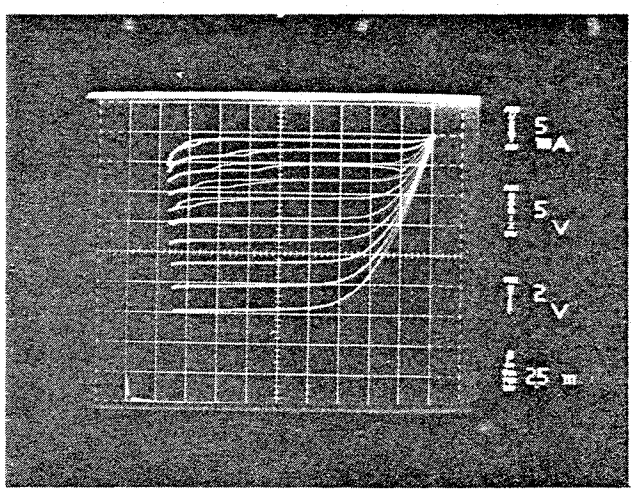

#1 — 127-B-2-1; I-6-10 (P-P); T = 8 K



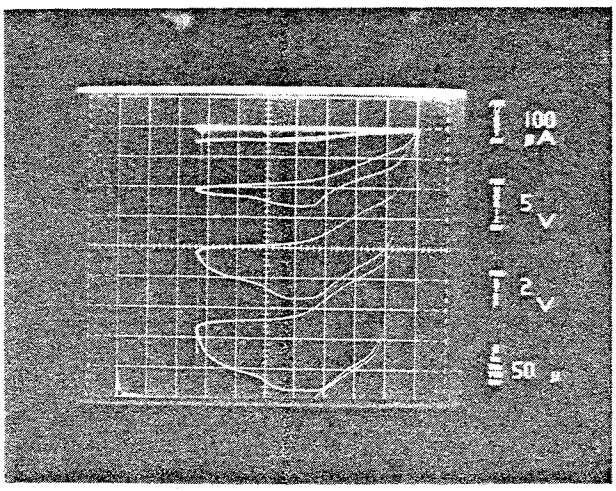

#2 — 127-B-2-1; I-37-25 (P-P); T = 6 K



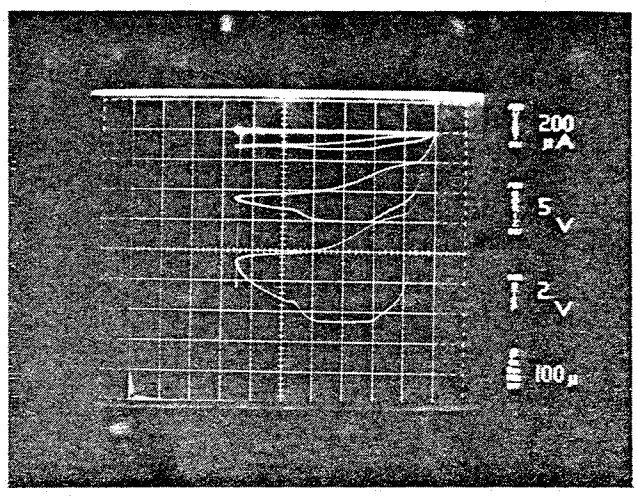

#3 — 127-B-2-1; I-37-10 (P-P); T = 6 K




#4 — 127-B-2-1; I-37-25 (P-P); T = 16 K




#5 — 127-B-2-1; I-93-10 (P-P); T = 5 K




#6 — 127-B-2-1; I-93-25 (P-P) T = 4.5 K

Fig. 5.9 I vs V characteristics showing MOSFET geometry effects at low temperatures.

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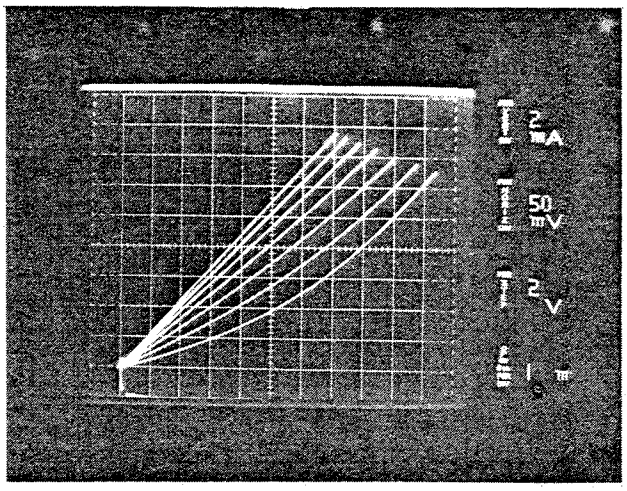
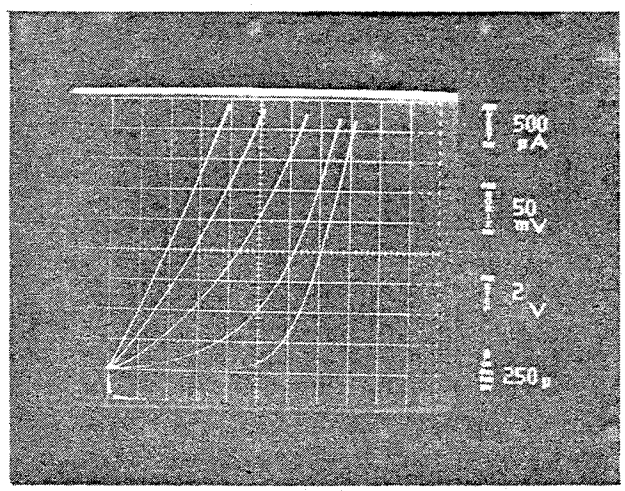
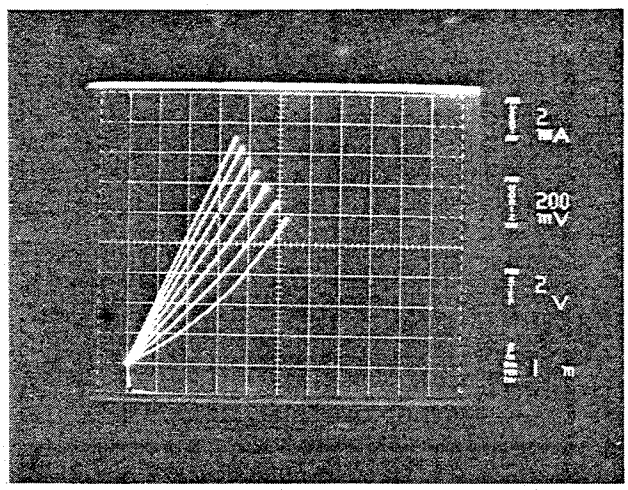


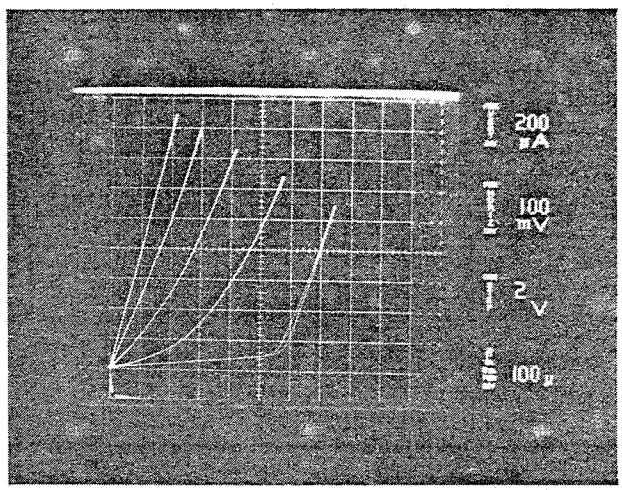

#1 — 127-B-2-1; II-6-25 (N-N); NO OFFSET; T = 4.2 K



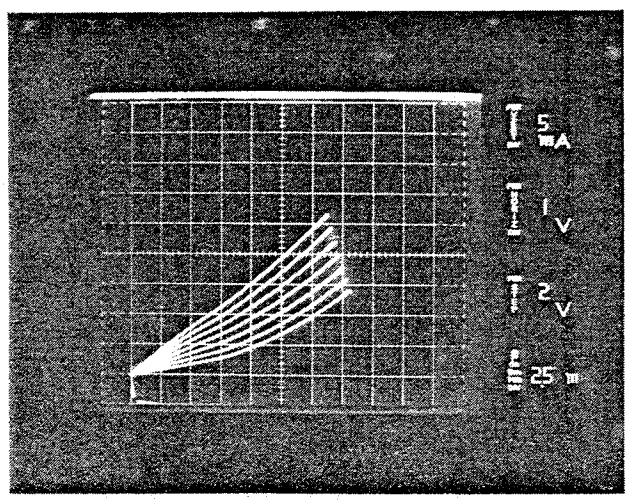

#2 — 127-B-2-1; II-6-25 (N-N); WITH OFFSET; T = 4.2 K



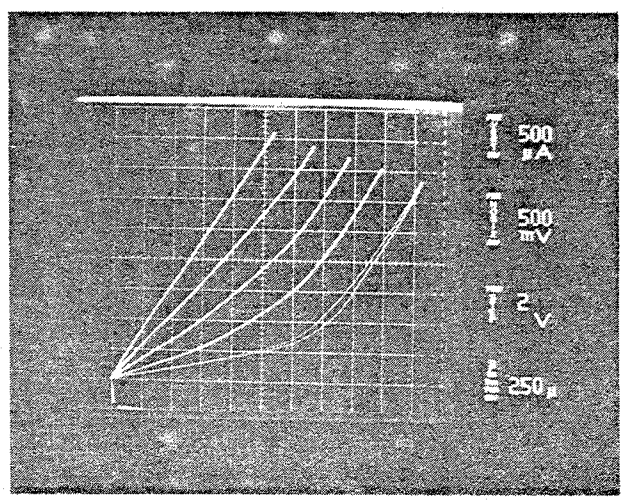

#3 — 127-B-2-1; II-15-25 (N-N); NO OFFSET; T = 4.2 K




#4 — 127-B-2-1; II-15-25 (N-N); WITH OFFSET; T = 4.2 K

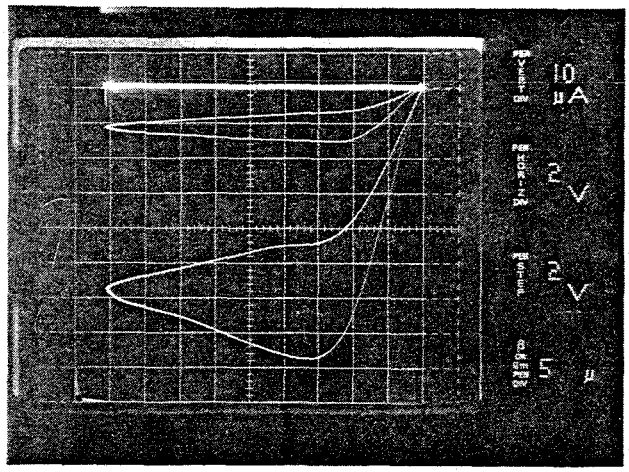



#5 — 127-B-2-1; II-93-25 (N-N); NO OFFSET; T = 4.24 K

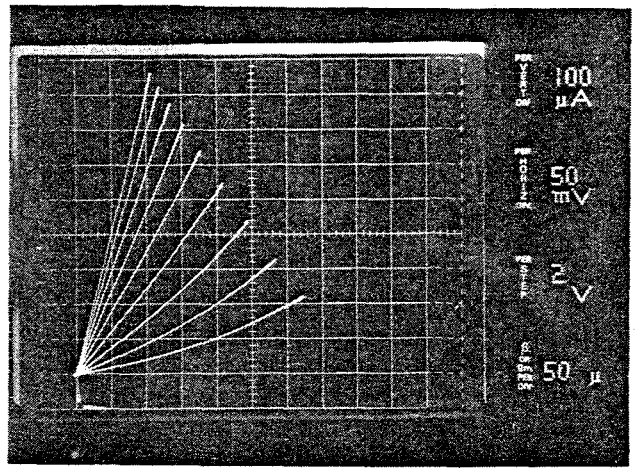



#6 — 127-B-2-1; II-93-25 (N-N); WITH OFFSET, T = 4.2 K

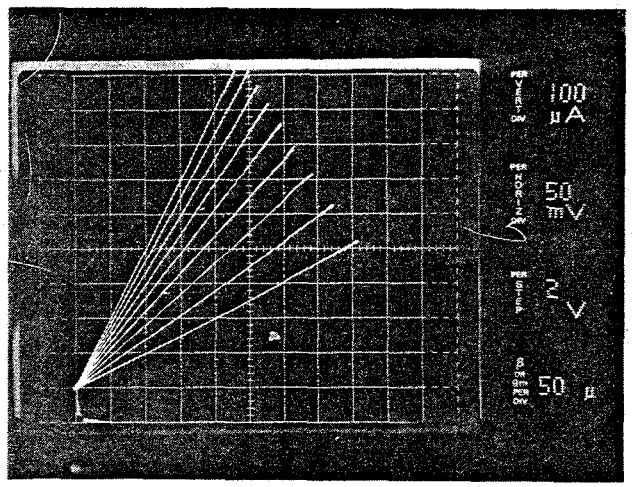
Fig. 5.10 I vs V characteristics showing CRYOFET geometry effects at low temperatures and source-drain leakage.



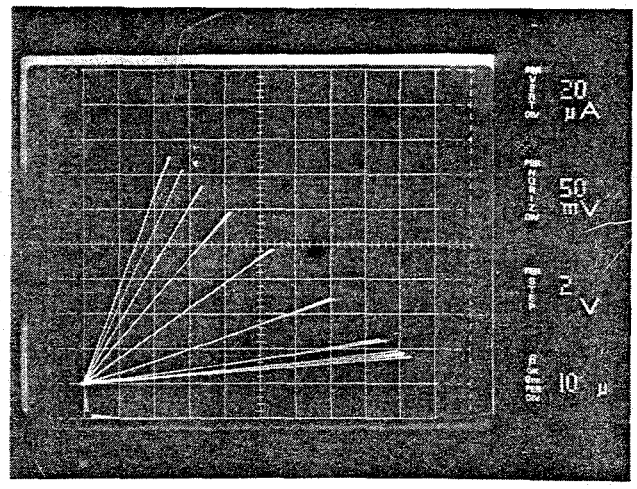

#1 – 69-B-2-1; I-37-10 (P-P); T = 4.3 K



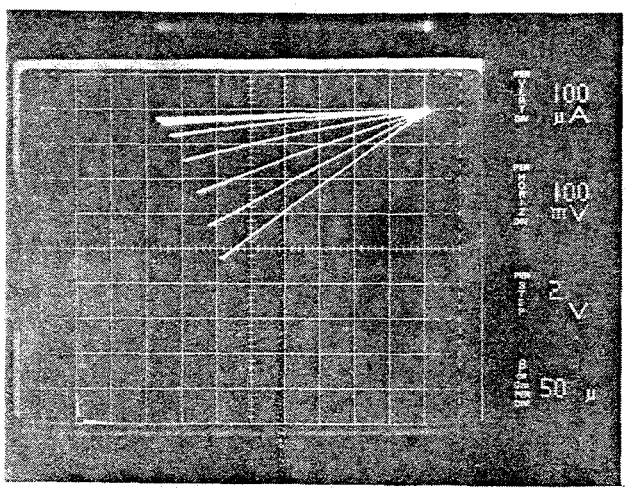

# 2 – 69-B-2-1; II-15-10 (N-N) WITH OFFSET; T = 4.3 K




#3 – 69-B-2-1; II-37-10 (N-N); WITH OFFSET; T = 4.3 K




# 4 – 69-B-2-1; II-93-10 (N-N) WITH OFFSET; T = 4.3 K




# 5 – 69-B-2-1; II-93-10 (N-N); DEPLETION MODE; T = 4.3 K

Fig. 5.11 I vs V characteristics of CRYOFETs and offset gate voltage to reduce leakage; operation in depletion mode.

The low temperature survey of devices obtained from the first group of lot No. 2 is concluded with the set of I vs V characteristics shown in Fig. 5.12. These include mixed devices in which a P diffusion and an N diffusion are utilized as source and drains of a MOSFET. In photo No. 3 an N-P device and in photo No. 2 a P-N device is shown. These devices exhibit a source-drain offset voltage of about 1 volt before channel modulation by gate voltage becomes effective. Such devices have no obvious advantages.

Included on Fig. 5.12, are the characteristics of MOSFETs and CRYOFETs fabricated on the "P" substrate which is p-type. On this substrate the P-P devices represent the CRYOFET accumulation mode of operation. The I vs V characteristics of four of these devices are shown in photos No. 1-4. These accumulation mode devices exhibit hyteresis effects. Also shown is a concentional N-N MOSFET on the P substrate. This device shows no hysteresis effects but exhibits leakage between source and drain (photo No. 5).

The second group of lot No. 2 received additional processing which included growth of an additional thickness of field oxide and a phosphorus gettering treatment. This processing was designed to lower the voltage threshold of the CRYOFETs and to reduce the leakage current between the source and drains which were found in the CRYOFETs produced in the first group of lot No. 2. Data presented here will show that this treatment was highly effective.

In Fig. 5.13, the 4.2 K I vs V characteristics of selected N-N CRYOFETs processed on wafer 68 (3.0 ohm cm) in the second group of lot No. 2 are presented. No evidence of leakage is shown on any of these traces. Separate measurements have indicated that the leakage current at 4.2 K falls below the $10^{-9}$ ampere range. As will be shown, leakage current at higher temperatures, limits the operation of the CRYOFETs. The upper temperature limit is approximately 20 K. Also tabulated are the measured voltage thresholds at 300 K and 4.2 K for the MOSFETs and for the N-N CRYOFETs at 4.2 K. These measurements confirm that the additional treatment has reduced thresholds. The CRYOFETs show low thresholds which contributes to their advantages.

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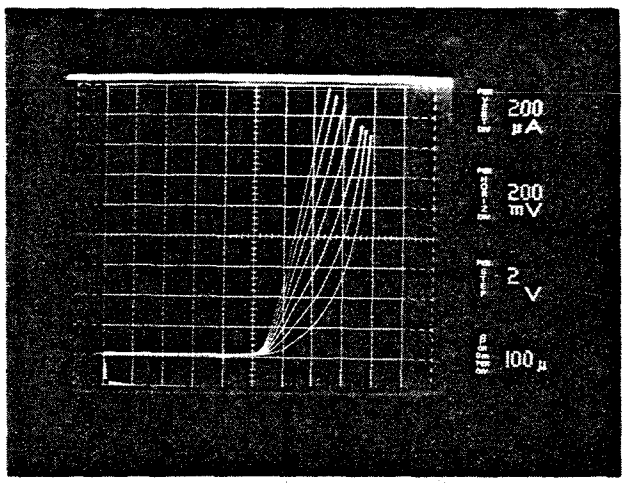
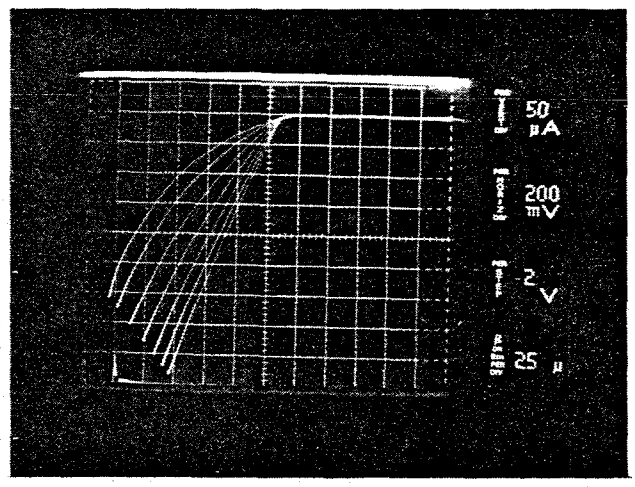
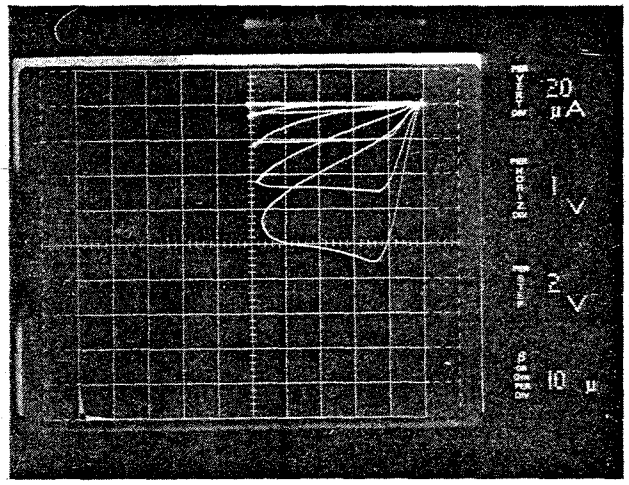


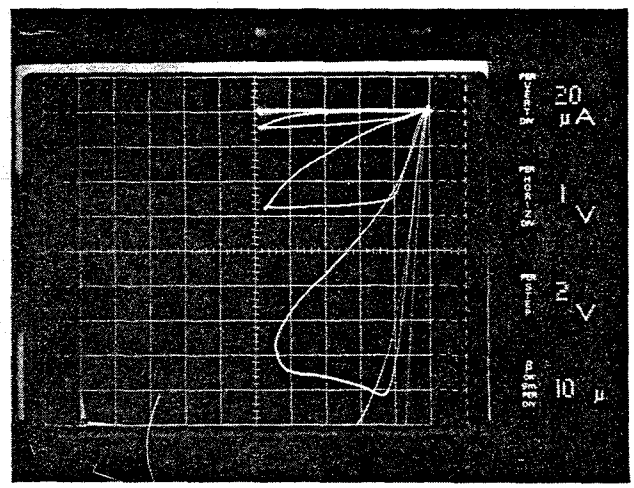

#1 – 127-B-2-1; III-37-10; (N-P); T = 4.3 K



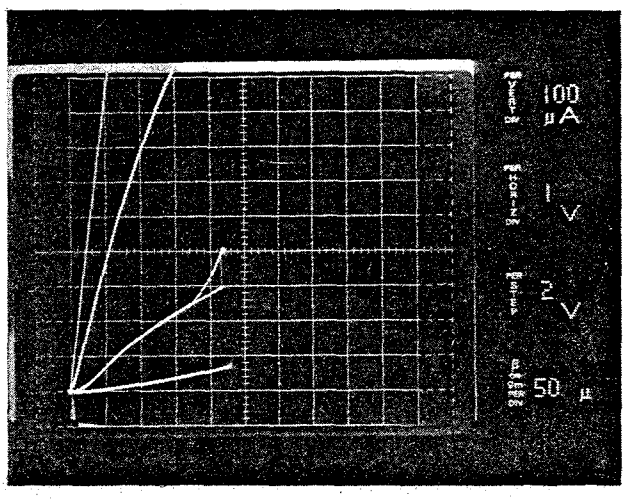

# 2 – 127-B-2-1; III-93-10 (P-N); T = 4.3 K




# 3 – P-B-2-1; I-37-10 )P-P); P SUBSTRATE; T = 4.3 K




# 4 – P-B-2-1; I-37-25 (P-P); P SUBSTRATE; T = 4.3 K




# 5 – P-B-2-1; II-37-10 (N-N); P SUBSTRATE; T = 4.3 K

Fig. 5.12 I vs V characteristics of CRYOFETs with mixed conductivity types for source and drains and on p-type substrate.

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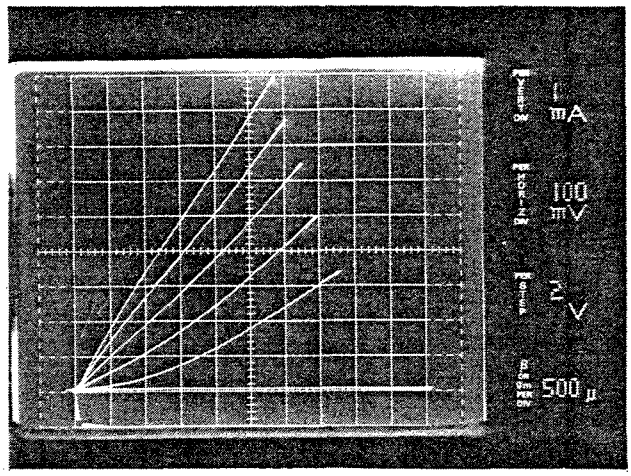
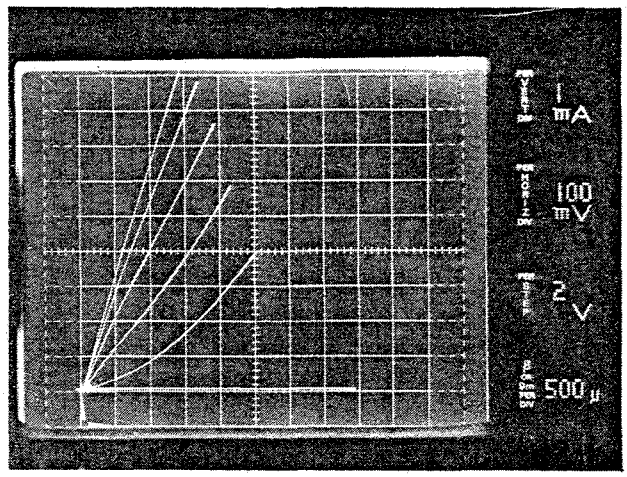
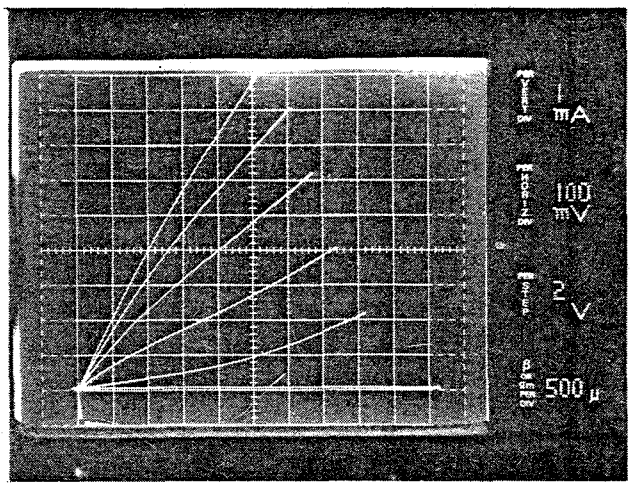


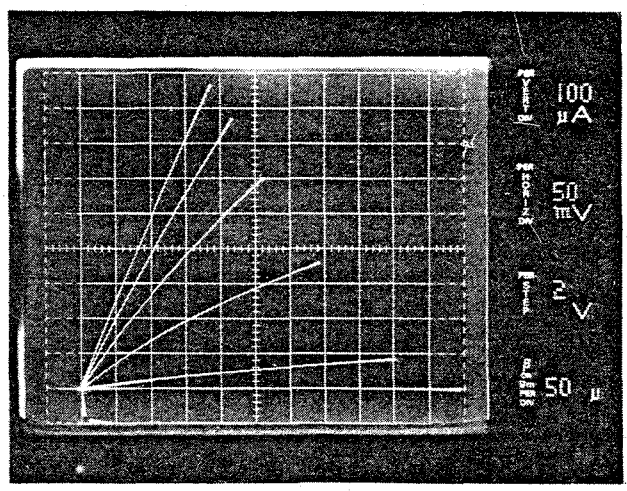

#1 – 68-B-3-2; II-15-10 (N-N); 4.3 K




#2 – 68-B-3-2; II-15-25 (N-N); 4.3 K




#3 – 68-B-3-2; II-37-25 (N-N); 4.3 K




#4 – 68-B-3-2; II-93-10 (N-N); 4.3 K

68-B-3-2

| DEVICE | (300 K) $V_T$ @ 10 µa | (4.3 K) $V_T$ @ 10 µa | DEVICE | (4.3 K) $V_T$ @ 10 µa |
|---|---|---|---|---|
| I-6-10 | 1.5 V | 2.0 V | II-6-10 | – |
| I-15-10 | – | – | II-15-10 | 0.33 V |
| I-37-10 | 2.5 | 2.3 | II-37-10 | 0.44 |
| I-93-10 | 2.9 | 2.4 | II-93-10 | 0.80 |
| I-6-25 | – | 1.8 | II-6-25 | 0.03 |
| I-15-25 | 2.0 | 2.0 | II-15-25 | 0.155 |
| I-37-25 | 2.2 | 2.2 | II-37-25 | 0.46 |
| I-93-25 | 2.5 | 2.2 | II-93-25 | – |

Fig. 5.13 I vs V characteristics of CRYOFETs from 2nd group of lot No. 2 with leakage between source and drain eliminated.

### 5.2.3 Source-Follower Gain

For use with high impedance detectors, the major role of the MOSFET or CRYOFET device is to act as an impedance convertor. It accepts the high impedance signal from the load resistor used with the detector and converts it to a low impedance signal which can then be signal processed without difficulty. The device is used in the source-follower mode with a maximum possible gain of one. Obviously, it is desirable to come as close to one as is practical.

The parameters that control the gain when operating as a source-follower are the gate voltage, the drain voltage and the choice of source resistance across which the output signal is developed. Since these parameters may also affect the power dissipated and the noise developed in the device, it is obvious that a consistent criteria be developed if meaningful comparative measurements of gain and noise are to be made.

The applied voltage needed to obtain a given gain was found to depend on the choice of source resistor. A limited study using $10^3$, $10^5$, and $10^7$ ohm resistors indicated that the choice of $10^5$ permitted the use of the lowest voltage. This value was accordingly adopted.

The measured noise showed, for the devices surveyed, a variable dependence on gain. In some devices, noise was highest at low gains while in others, the reverse was true. In Fig. 5.14, the measured noise as a function of gain, is shown for a N-N and P-P device at 4.2 K. In these devices, there is a near linear dependence of noise on gain at the lower gains followed by a variable behavior at higher gains. Misleading inferences on noise may be drawn unless a suitable reference gain is established.

The power dissipated in the MOSFETs or CRYOFETs also strongly depends on gain. In Fig. 5.15, this power is plotted against gain for these same devices. The conventional P-P MOSFET device is seen to require substantially higher powers to realize a given gain. At a gain of 0.98, the conventional

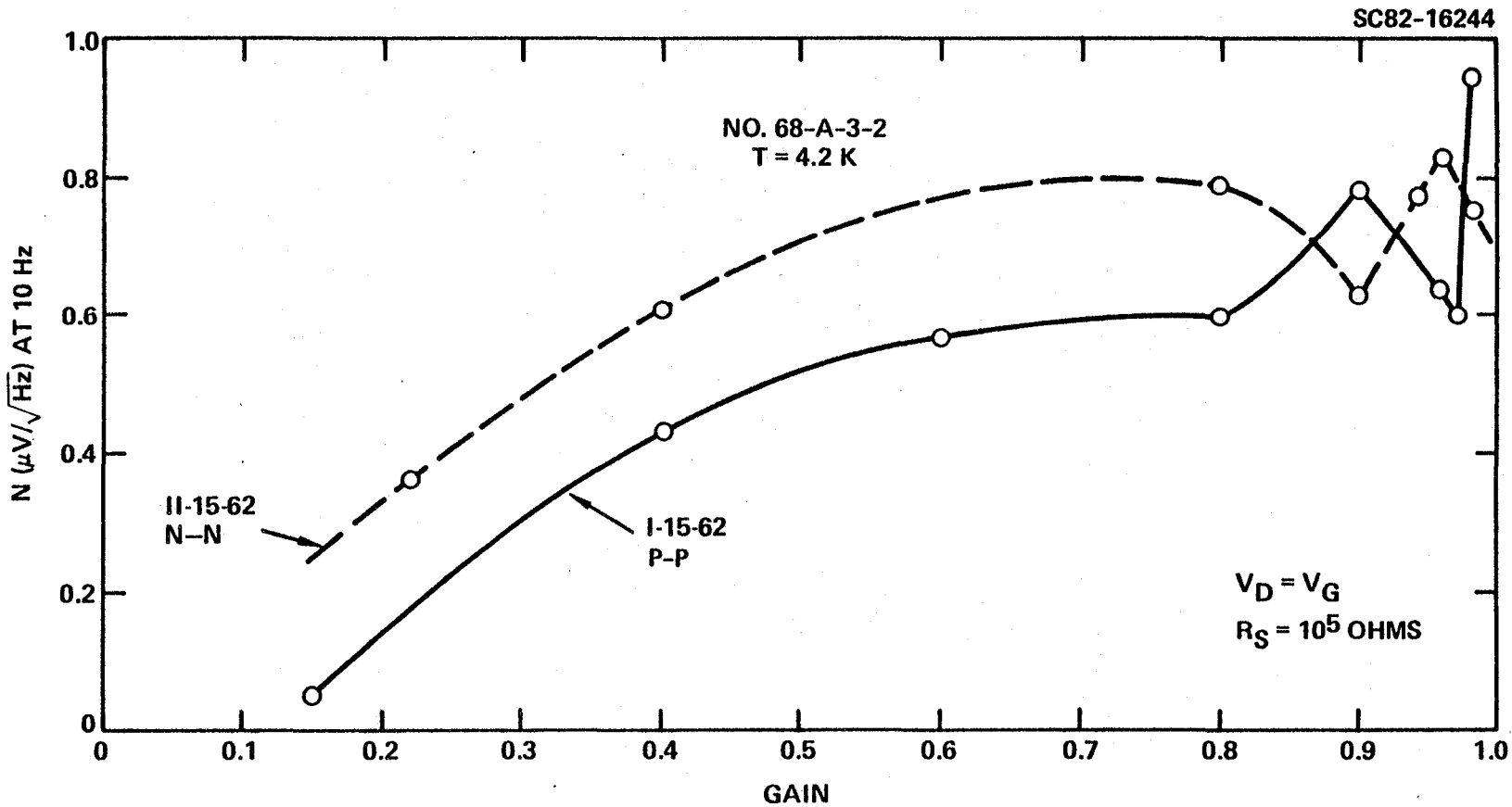



Fig. 5.14 Dependence of noise vs gain at 4.2 K.

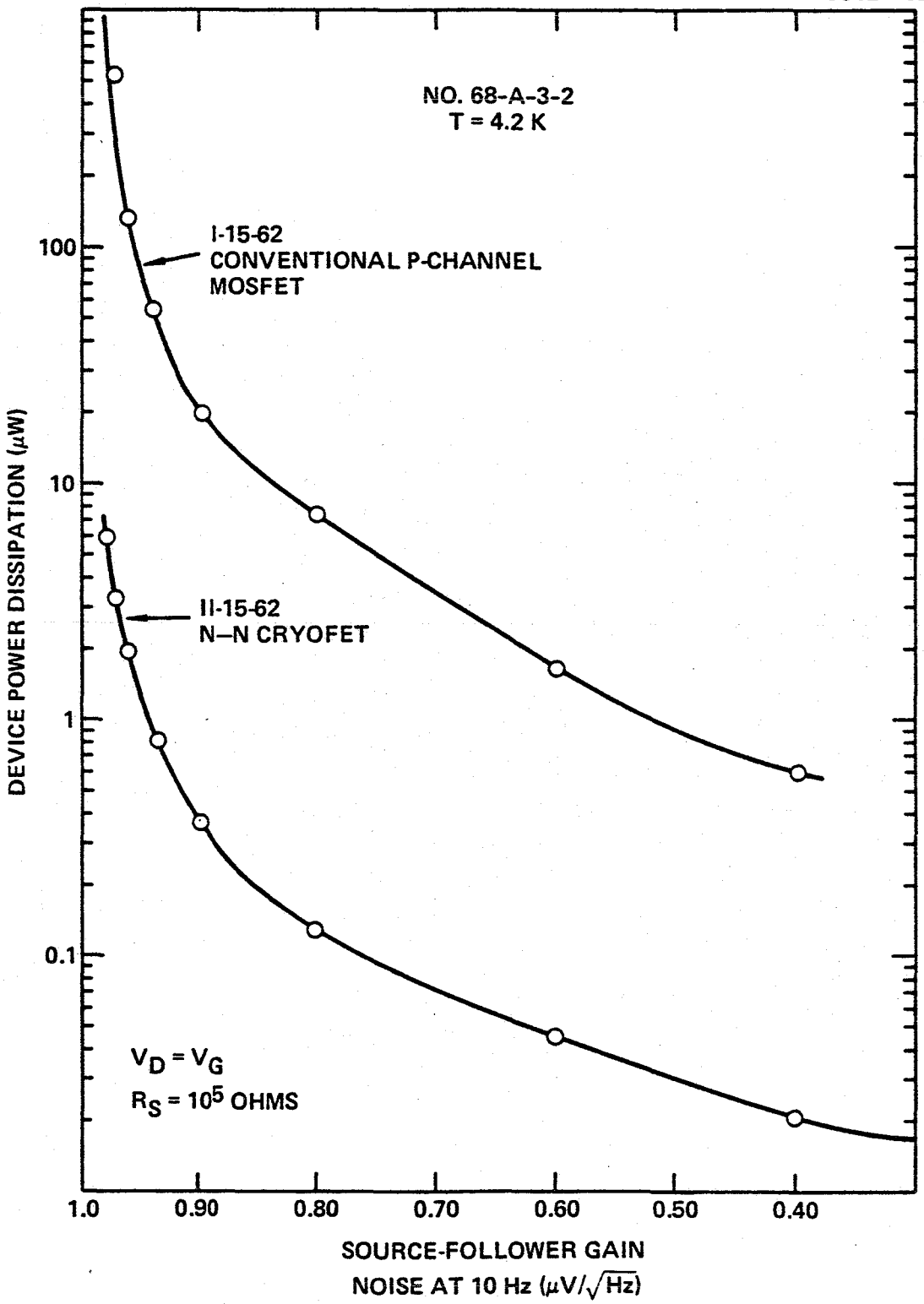



Fig. 5.15 Dependence of device power dissipation vs gain.

MOSFET requires a power more than two orders of magnitude higher than that required for the CRYOFET.

The frequency dependence of the source-follower gain was investigated using $R_S = 10^5$ ohms. It was found to be independent of frequency in the 1-100 Hz frequency range studied. This result was expected. A frequency dependence can be anticipated when the $R_S C_S$ product of the source limits response. This would require a frequency greater than $f = \frac{1}{2\pi R_S C_S}$ which for $R_S = 10^5$ ohms; $C \simeq 10$ pfd is $f = 1.6 \times 10^5$ Hz.

Based on these experimental observations and taking into account, that for source-follower operation, a gain near unity is desirable, the following criteria were adopted on gain for MOSFET, CRYOFET comparison:

1. Use a common voltage for the gate and drain; $V_G = V_D$ with $R_S = 10^5$ ohms.

2. Increase this voltage until the measured gain reaches 0.98 or the maximum voltage of the power supply (V = 24V) is reached.

3. Measure the source voltage and noise.

These criteria were used to develop the source-follower amplifier performance comparisons for these devices.

### 5.2.4 Noise

The noise of the MOSFET or CRYOFET is of fundamental interest in defining its role as a detector preamplifier at low temperature. It has long been known that the presence of the silicon-oxide interface over the conducting channel provides the major source of the 1/f noise associated with this type of device. This circumstance is explained theoretically by the generation-recombination process at this interface which causes the population of free charge carriers in the conducting channel to fluctuate. At low

temperature, this noise may be augmented by a contribution from the injection or collection process at the source and drain respectively.

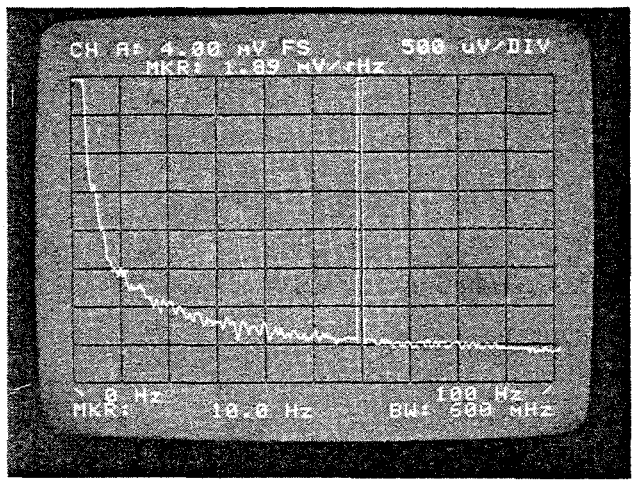
These considerations suggest that the CRYOFETs may have a noise advantage over conventional MOSFETs at low temperature but that the major noise would continue to be dominated by the 1/f noise contributions afforded by the silicon-oxide interface under the gate contact. The measurements to be reported, in which lower noise is obtained with the CRYOFETs, but the noise is still of a 1/f character is consistent with these expectations.

5.2.4.1 Ac Coupling vs dc Coupling

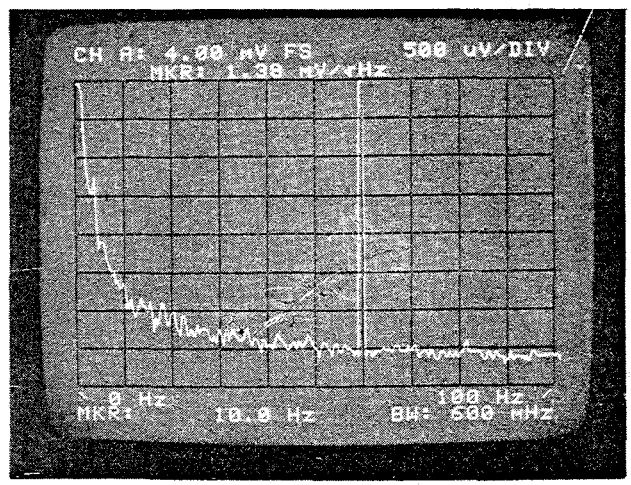
The MOSFET and CRYOFET when operated as source-followers exhibit voltage drops across their source resistor. In the usual ac coupled signal processing approach, this voltage drop has no significance. For signal processing applicable to low frequencies, the ac coupling capacitor is omitted and the dc offset is compensated. This raises the question as to whether a measurement using dc compensation provides a different noise level than does a measurement using ac coupling. To provide an answer to this question, a selected CRYOFET was measured in both modes at various temperatures. The noise spectra obtained from these measurements, in photos, is shown in Figs. 5.16 and 5.17.

The narrow peak shown at 60 hz is a pickup contribution from the ac power mains. These results demonstrate that, within the experimental variability of a noise measurement, the results are identical. Similar measurements carried out with conventional MOSFETs give the same result. The noise scale printed out on the photos must be reduced by 1000 to reflect the gain of 1000 supplied by the PAR 113 amplifier used with these measurements.

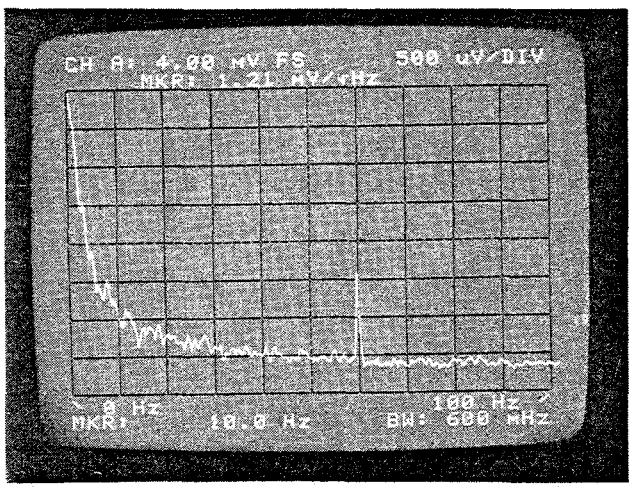
The data also show that noise in these devices apparently peaks at about T = 15 K before declining to the level it had at lower temperatures. This peak response may be associated with a selective trap activation energy,



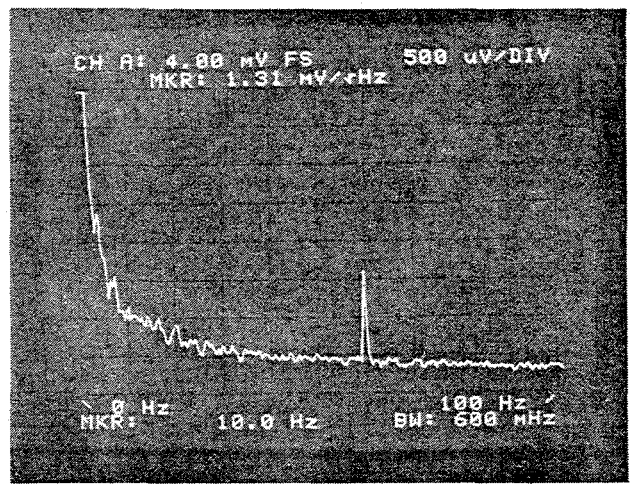

# 1 – 128-B-4-1; 11-37-10 (N-N); DC/C; T = 2.4 K



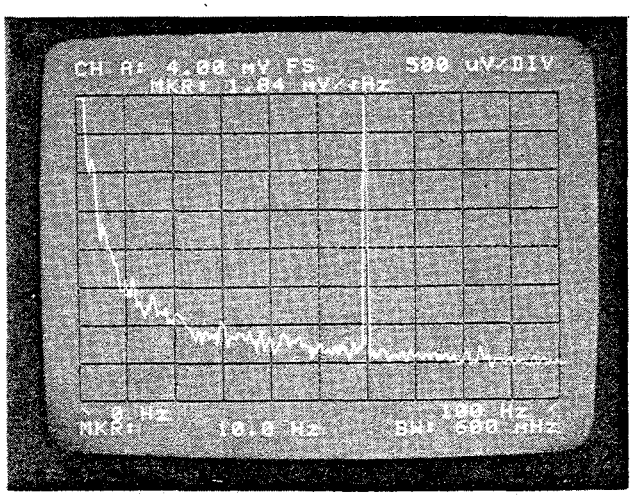

#2 – 126-B-4-1; II-37-10 (N-N); AC/C; T = 2.4 K



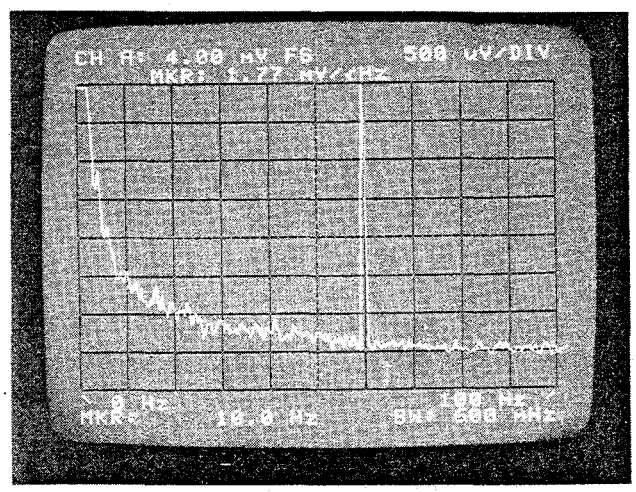

#3 – 126-B-4-1; II-37-10 (N-N); DC/C; T = 4.2 K




#4 – 126-B-4-1; II-37-10 (N-N); AC/C; T = 4.2 K



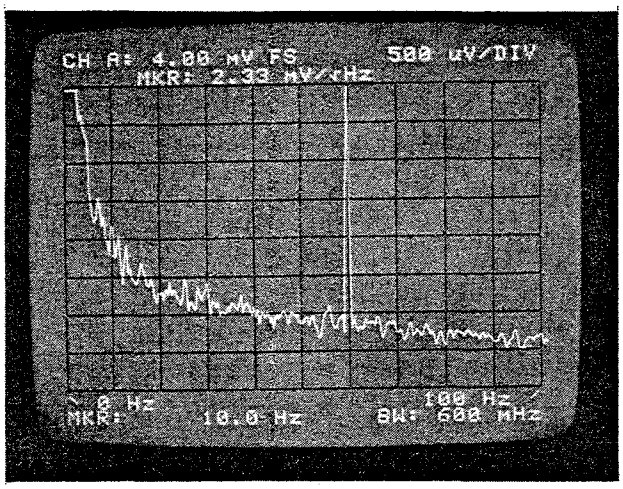

#5 – 126-B-4-1; II-37-10 (N-N); DC/C; T = 10 K



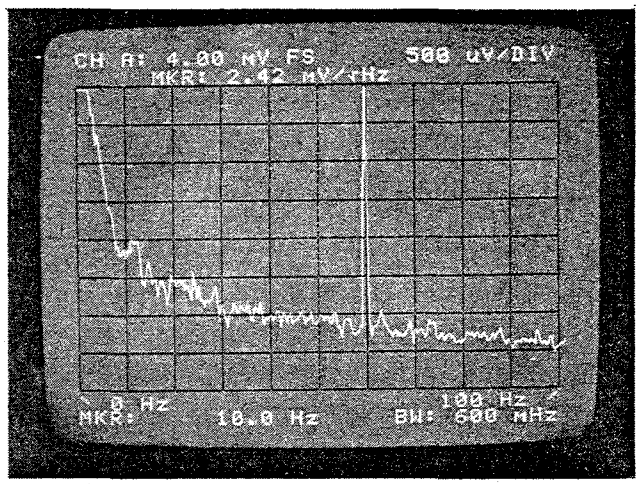

#6 – 126-B-4-1; II-37-10 (N-N); AC/C; T = 10 K

Fig. 5.16 AC coupled and dc coupled noise spectrums (T = 2.4; 4.2; 10K).
(Printed scale should be reduced by 1000.)

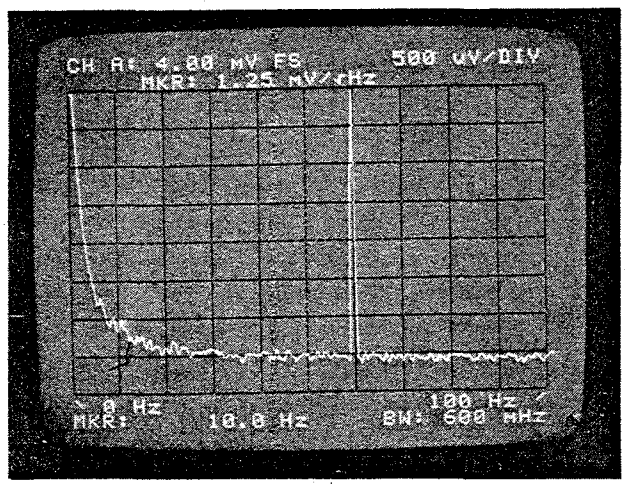
SC82-16247



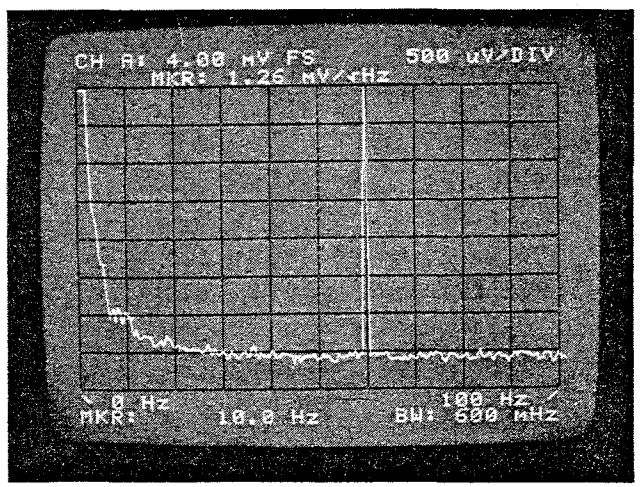

#1 – 126-B-4-1; II-37-10 (N-N); DC/C; T = 15.2 K




#2 – 126-B-4-1; II-37-10 (N-N); AC/C; T = 15.2 K




#3 – 126-B-4-1; II-37-10 (N-N); DC/C; T = 20 K




#4 – 126-B-4-1; II-37-10 (N-N); AC/C; T = 20 K

Fig. 5.17 AC coupled and dc coupled noise spectrums (T = 15.2; 20K).
(Printed scale should be reduced by 1000.)

activated at ~ 15 K by the displacement of the Fermi level, which influences the generation-recombination process.

5.2.4.2 Source-Follower Noise Measurements

Taking note of the experimentally demonstrated fact that ac coupled noise measurements give the same results as the dc coupled measurements, further noise measurements were limited to ac coupled measurements. This was done because this measurement is easier and faster to implement. Noise measurements were carried out as a function of frequency for all operating P-P and N-N devices on chips of the four substrate resistivities at 4.2 K. Selected temperature measurements in the range 2.4-27 K were also made. In general, the character of the curves indicated a 1/f power spectrum and were all similar to those appearing in Figures 5.16, 5.17. Graphical plots on log-log paper of some of the noise data vs frequency (not shown) indicated that the noise voltage accurately declines as $f^{1/2}$ in the 1-100 Hz range which is consistent with the postulated 1/f power spectrum. To make possible a simple noise comparison, the noise obtained at one frequency, 10 Hz, was accordingly tabulated.

5.2.5 Source-Follower Amplifier Performance

A systematic comparative study was made of the source-follower amplifier performance of the conventional MOSFETs and the CRYOFETs prepared from the second group of lot No. 2. The study included device geometry, substrate resistivity, temperature, and for the noise, frequency. This study follows the criteria adopted in sections 5.2.3 and 5.2.4. Thus, comparison was made with the devices biased up ($V_D = V_G$) as source-followers to give a gain of 0.98 using a load resistance of $10^5$ ohms. Tabulated data includes the parameters, $V_T$, $V_{BVD}$, $V_{D,G}$, $V_S$, G, N @ 10 Hz, P and $(\frac{\omega CN}{G})_N$ (10 Hz) and is compiled for the four n-type resistivity substrates processed, i.e.; 3.0; 0.90; 0.22 and 0.13 ohm cm. Data at 4.2 K is tabulated for No. 68-B-3-1 (3.0 ohm cm) in Table XI, for No. 126-B-4-1 (0.90 ohm cm) in Table XII, for No. 27-B-3-

2 (0.22 ohm cm) in Table XIII and for No. 135-B-4-2 (0.13 ohm cm) in Table XIV. In Tables XV, XVI and XVII, data covering the temperature range of 2.4-27 K is given respectively for No. 126-B-4-1, No. 27-B-3-2 and for No. 135-B-4-2.

These data have been examined at 4.2 K for correlation with device geometry, substrate resistivity and MOSFET or CRYOFET device type. Correlation trends discussed for noise are based on a relatively small number of noise samples and this circumstance must weight the firmness of the conclusions.

Table XI

Source-Follower Properties of No. 68-B-3-1 at 4.2 K
(3.0 ohm cm)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz (μV/√Hz) | P(DIS) (μW) | $(\frac{\omega CN}{G})_N$ | |
|---|---|---|---|---|---|---|---|---|---|
| I-6-10 | 2.1 | 13.0 | -17.69 | -14.96 | 0.98 | 4.33 | 2646 | 2.1 | |
| I-15-10 | - | - | - | - | - | - | - | - | (1) |
| I-37-10 | 2.2 | >18 | -24.06 | -19.76 | 0.96* | 0.897 | 4754 | 2.7 | |
| I-93-10 | 2.4 | >18 | -24.13 | -19.28 | 0.96* | 0.498 | 4652 | 3.8 | |
| I-6-25 | 2.0 | 6.5 | -11.53 | -9.38 | 0.98 | 2.63 | 1082 | 3.2 | |
| I-15-25 | 2.0 | >18 | -17.84 | -14.9 | 0.98 | 4.23 | 2658 | 13 | (4) |
| I-37-25 | 3.5 | >18 | -24.14 | -17.89 | 0.95* | 8.31 | 4319 | 64 | (4) |
| I-93-25 | 3.6 | >18 | -24.14 | -17.73 | 0.94* | 8.35 | 4280 | 163 | (4) |
| | | | | | | | | | |
| II-6-10 | 0.17 | 0.19 | 1.74 | 1.59 | 0.98 | 1.58 | 27.7 | 0.76 | |
| II-15-10 | - | - | - | - | - | - | - | - | (1) |
| II-37-10 | 0.46 | 3.0 | 2.84 | 2.36 | 0.98 | 1.12 | 67.0 | 3.4 | |
| II-93-10 | 0.80 | 9.0 | | | | | | | (2) |
| II-6-25 | 0.07 | 0.075 | 1.71 | 1.64 | 0.98 | 0.985 | 28.0 | 1.2 | (3) |
| II-15-25 | 0.33 | 1.0 | 1.37 | 1.04 | 0.98 | 1.44 | 14.2 | 4.3 | |
| II-37-25 | 0.47 | 3.0 | 2.15 | 1.65 | 0.98 | 0.871 | 36.1 | 6.5 | |
| II-93-25 | 0.74 | >18 | - | - | - | - | - | - | (1) |

(1) Gate open
(2) Drain to gate short
(3) 0.2 gain with $V_{D,G}$ = 0 (source-drain leakage)
(4) Dissipated power raised temperature
* Highest gain achievable with existing power supply

Table XII

Source-Follower Properties of No. 126-B-4-1* at 4.2 K
(0.90 ohm cm)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz (μV/√Hz) | P(DIS) (μW) | $(\frac{\omega CN}{G})_N$ | |
|---|---|---|---|---|---|---|---|---|---|
| I-6-10 | 2.0 | 3.0 | -2.80 | -0.735 | 0.96 | 3.6 | 20.6 | 1.8 | |
| I-15-10 | 0.6 | 0.6 | -1.12 | -0.511 | 0.98 | 12.0 | 5.7 | 14 | |
| I-37-10 | 2.2 | >20 | -3.717 | -1.155 | 0.94 | 4.19 | 42.9 | 13 | |
| I-93-10 | 2.0 | >20 | -2.875 | -0.917 | 0.89 | 6.22 | 26.4 | 51 | |
| I-6-25 | - | - | - | - | - | - | | | (1) |
| I-15-25 | - | - | - | - | - | - | | | (1) |
| I-37-25 | 1.6 | 1.0 | -9.787 | -7.41 | 0.98 | 11.1 | 725 | 83 | |
| I-93-25 | - | - | - | - | - | - | | | (1) |
| | | | | | | | | | |
| II-6-10 | 0.19 | 0.18 | 0.570 | 0.396 | 0.97 | 0.819 | 2.3 | 0.40 | |
| II-15-10 | 0.35 | 0.52 | 0.621 | 0.273 | 0.97 | 1.37 | 1.7 | 1.7 | |
| II-37-10 | 0.54 | 1.5 | 1.546 | 0.978 | 0.95 | 1.03 | 15.1 | 3.2 | |
| II-93-10 | 0.86 | 5.5 | 2.00 | 1.135 | 0.89 | 0.650 | 22.7 | 5.6 | |
| II-6-25 | 0.04 | 0.03 | 0.525 | 0.493 | 0.97 | 0.561 | 2.6 | 0.68 | (1) |
| II-15-25 | 0.33 | 0.60 | 0.809 | 0.464 | 0.98 | 0.685 | 3.8 | 2.1 | |
| II-37-25 | - | - | - | - | - | - | | | (1) |
| II-93-25 | 0.70 | 3.0 | 2.07 | 1.175 | 0.86 | 1.52 | 24.3 | 32 | |

(1) Drain-source leakage
* Data taken before criteria of G = 0.98 was adopted.

Table XIII

Source-Follower Properties of No. 27-B-3-2 at 4.2 K
(0.22 ohm cm)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz (μV/√Hz) | Power (μW) | $(\frac{\omega CN}{G})_N$ |
|---|---|---|---|---|---|---|---|---|
| I-6-10 | 3.0 | >18 | -7.47 | -3.38 | 0.98 | 3.86 | 252 | 1.9 |
| I-37-10 | 3.0 | >18 | -24.1 | -17.8 | 0.98 | 6.30 | 4272 | 19 |
| I-6-25 | 3.2 | >18 | -5.60 | -2.10 | 0.98 | 4.36 | 118 | 5.2 |
| I-37-25 | 3.0 | >18 | -7.60 | -3.60 | 0.98 | 1.06 | 274 | 8.0 |
| II-6-10 | 0.22 | 0.20 | 0.85 | 0.65 | 0.98 | 0.660 | 5.5 | 0.32 |
| II-15-10 | 0.38 | 0.52 | 1.20 | 0.83 | 0.98 | 1.26 | 9.9 | 1.5 |
| II-15-25 | 0.37 | 0.50 | 0.86 | 0.50 | 0.98 | 1.12 | 4.3 | 3.4 |
| II-37-25 | 0.60 | 1.0 | 1.74 | 1.14 | 0.98 | 1.12 | 19.8 | 8.4 |
| II-93-25 | 0.82 | 2.5 | 7.65 | 6.60 | 0.98 | 0.760 | 505 | 14 |

Table XIV

Source-Follower Properties of No. 135-B-4-2 at 4.2 K
(0.13 ohm cm)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz (μV/√Hz) | Power (μW) | $(\frac{\omega CN}{G})_N$ | |
|---|---|---|---|---|---|---|---|---|---|
| I-6-10 | 4.0 | >18 | -24.1 | -19.4 | 0.98 | 23.7 | 4675 | 11.6 | |
| I-15-10 | - | - | - | - | - | - | - | - | (1) |
| I-37-10 | 5.9 | >18 | -24.1 | -18.4 | 0.96* | 60.0 | 4434 | 187 | |
| I-93-10 | 7.2 | 19 | -24.1 | -18.0 | 0.95* | 26.0 | 4338 | 205 | |
| I-6-25 | 4.6 | 19 | -15.6 | -11.3 | 0.98 | 13.0 | 1763 | 15.9 | |
| I-15-25 | 4.2 | 19 | -24.0 | -19.1 | 0.98 | 20.1 | 4584 | 61.5 | |
| I-37-25 | 3.5 | 19 | -24.1 | -15.9 | 0.96* | 207 | 3832 | 1617 | |
| I-93-25 | 4.6 | 19 | -24.1 | -13.6 | 0.96* | 112 | 3278 | 2182 | |
| | | | | | | | | | |
| II-6-10 | 0.21 | 0.46 | 1.19 | 0.98 | 0.98 | 0.573 | 11.7 | 0.27 | |
| II-15-10 | 0.46 | 0.54 | 1.35 | 0.98 | 0.98 | 1.41 | 13.2 | 1.7 | |
| II-37-10 | - | - | - | - | - | - | - | - | (1) |
| II-93-10 | 1.1 | 3.0 | 11.0 | 9.56 | 0.98 | | 1052 | | |
| II-6-25 | - | - | - | - | - | - | | | (1) |
| II-15-25 | 0.36 | 0.50 | 1.13 | 0.78 | 0.98 | 0.947 | 8.8 | 2.90 | |
| II-37-25 | - | - | - | - | - | - | | | (2) |
| II-93-25 | - | - | - | - | - | - | - | - | (2) |

(1) Gate open
(2) Drain to gate short.

Table XV

Source-Follower Properties of No. 126-B-4-1
(0.90 ohm-cm)
(Various Temperatures)

| Device | T (K) | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz ($\mu V/\sqrt{Hz}$) | Power (μW) | $(\frac{\omega CN}{G})_N$ |
|---|---|---|---|---|---|---|---|---|---|
| I-37-25 | 2.5 | 1.45 | 1.45 | -24.0 | -20.9 | 0.98 | 32.3 | 5020 | 242 |
| II-37-10 | 2.4 | 0.54 | 1.5 | 3.73 | 3.23 | 0.98 | 1.38 | 120 | 4.1 |
| II-37-10 | 4.2 | 0.54 | 1.5 | 2.58 | 1.99 | 0.98 | 1.31 | 51.3 | 3.9 |
| II-37-10 | 10 | 0.47 | 1.4 | 4.58 | 3.99 | 0.98 | 1.77 | 183 | 5.3 |
| II-37-10 | 15.2 | 0.42 | 1.2 | 5.16 | 4.61 | 0.98 | 2.33 | 238 | 7.0 |
| II-37-10 | 20 | 0.34 | 0.90 | 6.38 | 5.84 | 0.98 | 1.26 | 373 | 3.8 |
| II-37-10 | 27 | 0.125 | 0.125 | | | | | | |

Table XVI

Source-Follower Properties of No. 27-B-3-2
(0.22 ohm cm)
(Various Temperatures)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz ($\mu V/\sqrt{Hz}$) | Power (μW) | $(\frac{\omega CN}{G})_N$ |
|---|---|---|---|---|---|---|---|---|
| | | | T = 2.4 K | | | | | |
| II-6-10 | 0.22 | 0.24 | 1.14 | 0.922 | 0.98 | 0.827 | 10.5 | 0.40 |
| II-15-10 | 0.40 | 0.60 | 1.58 | 1.19 | 0.98 | 1.18 | 18.8 | 1.4 |
| II-15-25 | 0.39 | 0.60 | 1.08 | 0.698 | 0.98 | 1.26 | 7.5 | 3.8 |
| II-37-25 | 0.64 | 1.50 | 1.96 | 1.322 | 0.98 | 1.14 | 25.9 | 8.6 |
| | | | T = 10 K | | | | | |
| II-6-10 | 0.18 | 0.19 | 1.82 | 1.64 | 0.98 | 0.685 | 29.8 | 0.33 |
| II-15-10 | | | | | | | | (1) |
| II-15-25 | 0.325 | 0.38 | 1.99 | 1.65 | 0.98 | 1.31 | 32.8 | 3.9 |
| II-37-25 | 0.47 | 0.90 | 4.85 | 4.28 | 0.98 | 1.10 | 207 | 8.2 |
| | | | T = 18 K | | | | | |
| II-6-10 | 0.09 | 0.10 | 1.46 | 1.35 | 0.98 | 0.698 | 19.7 | 0.33 |
| II-15-10 | 0.25 | 0.32 | 2.04 | 1.74 | 0.98 | 0.985 | 35.5 | 1.2 |
| II-35-25 | 0.22 | 0.29 | 2.00 | 1.73 | 0.98 | 1.06 | 35.6 | 3.2 |
| II-37-25 | 0.36 | 0.74 | 4.36 | 3.92 | 0.98 | 0.735 | 171 | 5.5 |

(1) Gate open

Table XVII

Source-Follower Properties of No.135-B-4-2
(0.13 ohm cm)
(Various Temperatures)

| Device | $V_T$@10 μa (V) | $V_{BVD}$@1 μa (V) | $V_{D,G}$ (V) | $V_S$ (V) | Gain | N@10Hz (μV/√Hz) | Power (μW) | $(\frac{\omega CN}{G})_N$ |
|---|---|---|---|---|---|---|---|---|
| | | | | T = 2.4 K | | | | |
| I-6-10 | 4.0 | >18V | -24.1 | -19.4 | 0.98 | 29.1 | 4675 | 14 |
| I-6-25 | 4.6 | 19 | -14.8 | -10.6 | 0.98 | 11.2 | 1569 | 13 |
| II-6-10 | 0.21 | 0.46 | 1.28 | 1.06 | 0.98 | 0.630 | 13.6 | 0.30 |
| II-15-10 | 0.46 | 0.54 | 1.59 | 1.21 | 0.98 | 1.14 | 19.2 | 1.4 |
| II-93-10 | 1.1 | 3.0 | 15.2 | 14.6 | 0.98 | 2.64 | 2365 | 19.9 |
| II-15-25 | 0.36 | 0.50 | 1.26 | 0.89 | 0.98 | 0.945 | 12.3 | 28 |
| | | | | T = 10 K | | | | |
| I-6-10 | | | -24.1 | -19.3 | 0.98 | 39.5 | 4651 | 19 |
| I-6-25 | | | -24.1 | -19.3 | 0.98 | 28.2 | 4651 | 34 |
| II-6-10 | | | 1.90 | 1.70 | 0.98 | 0.822 | 32.3 | 0.39 |
| II-15-10 | | | 2.80 | 2.40 | 0.98 | 2.35 | 67.2 | 2.8 |
| II-15-25 | | | 2.10 | 1.80 | 0.98 | 1.48 | 37.8 | 4.4 |
| | | | | T = 18 K | | | | |
| I-6-10 | 4.0 | 19 | -24.1 | -17.1 | 0.98 | 11.0 | 4121 | 5.3 |
| I-6-25 | 4.0 | 19 | -24.1 | -17.4 | 0.98 | 9.84 | 4193 | 12 |
| II-6-10 | 0.12 | 0.12 | 2.08 | 1.95 | 0.98 | 0.949 | 40.6 | 0.46 |
| II-15-10 | 0.25 | 0.32 | 2.63 | 2.35 | 0.98 | 0.860 | 61.8 | 1.0 |
| II-93-10 | - | - | - | - | - | - | - | - |
| II-15-15 | 0.22 | 0.28 | 2.61 | 2.37 | 0.98 | 1.08 | 61.9 | 3.2 |

5.2.5.1 Device Geometry

Noise measurements exhibit an unavoidable variability since they involve an integration of a multiplicity of random events. Careful examination of the noise data obtained for the different geometry devices at 4.2 K on the B chips indicates that no obvious correlation can be drawn between the measured noise and device geometry. (The larger geometries on the A chips were not surveyed since the higher capacitances are unfavorable for source-follower application). This applies to both the MOSFETs as well as the CRYOFETs. On the other hand, the voltage required to achieve a gain of 0.98 is definitely related to device geometry. This voltage scales up as the L/W device ratio which is consistent with the expected W/L dependence of device transconductance. The dissipated power which is proportional to this voltage appears to follow the same L/W law. The normalized figure-of-merit $(\frac{\omega CN}{G})_N$, which it is desirable to minimize, increases with both channel length and gate width. These trends suggest that the smallest device tested with L = 6 μm, W = 10 mils which provides comparable noise, adequate gain and both lower power dissipation and lower figure-of-merit is the geometry choice for the CRYOFET. The tabulated figure-of-merit for the MOSFETs use the same capacitance values as for the CRYOFETs. Because of the opposite gate polarity of the MOSFETs, this may not be true at low temperatures.

5.2.5.2 Substrate Resistivity

The substrate resistivity is known to influence the voltage threshold of conventional MOSFETs at room temperature. The tabulated data suggests that this trend continues at 4.2 K. For the 3.0 ($1.6 \times 10^{15}$ $cm^{-3}$) and 0.90 ($5.8 \times 10^{15}$ $cm^{-3}$) ohm cm substrate, the measured threshold is stabilized at the 2 volt range. For the 0.22 ohm cm ($3.1 \times 10^{16}$ $cm^{-3}$) substrate, it rises to about 3 V and for the 0.13 ohm cm ($6.0 \times 10^{16}$ $cm^{-3}$) substrate, it is still higher at the 4 V level. The noise obtained on these substrates for conventional devices appears to show some correlation with increase of doping concentration. MOSFET devices on the 0.13 ohm cm substrate, for example, show

substantially higher noise levels than on the other substrates. Finally the power dissipation of the MOSFET at a gain of 0.98 shows a dependence on substrate. These parameters are plotted against substrate doping concentration for MOSFET I-6-10 at 4.2 K in Fig. 5.18. The definition of these curves is limited by the small numbers of data points. In the case of the power the data point at $5.6 \times 10^{15}$ was taken at a gain of 0.96. It was scaled to a power equivalent to a G = 0.98 using guidance obtained from the P-P curve in Fig. 5.15. The data indicates a minimum at an uncertain concentration which is sketched in.

For the CRYOFETs, the voltage threshold aggregates a fraction of a volt and while there is some suggestion that it depends on channel lengths, there appears to be no significant dependence on substrate resistivity. The noise of the CRYOFET, which is a factor of 2-4 times lower than the conventional MOSFETs, shows a moderate decline with increase of doping concentration in the substrate. The figure-of-merit, moreover, follows the same trend. The power dissipated by the CRYOFET, also shows an apparent dependence on substrate resistivity. In Fig. 5.19, the dependence of noise, figure-of-merit and dissipation power are plotted for CRYOFET device II-6-10. In the case of power dissipation, the indicated value of 2.3 μ watts obtained for a CRYOFET gain of 0.97 (No. 126-B-4-1) was scaled up to 4.6 μW, following the guidance provided by the N-N curve in Fig. 5.15. The data point of the No. 68-B-3-1 of 27.7 μW lies off the graph but its relative position was used to define the curve. As with the power curve of Fig. 5.18, the small number of experimental points and the experimental uncertainity introduced by the scaling of the point at $5.6 \times 10^{15}$ $cm^{-3}$ makes the actually definition of the curve somewhat speculative. Nevertheless, the data indicates that some optimum doping concentration for minimum power exists for the CRYOFET. In comparing the curves of Figs. 5.18 and 5.19, the reduced scale of Fig. 5.19 should be noted. Taking account of the dependence of noise, figure-of-merit and power dissipation, a near optimum doping concentration is provided by the 0.22 ohm cm substrate at $3.1 \times 10^{16}$ $cm^{-3}$. The properties of this CRYOFET

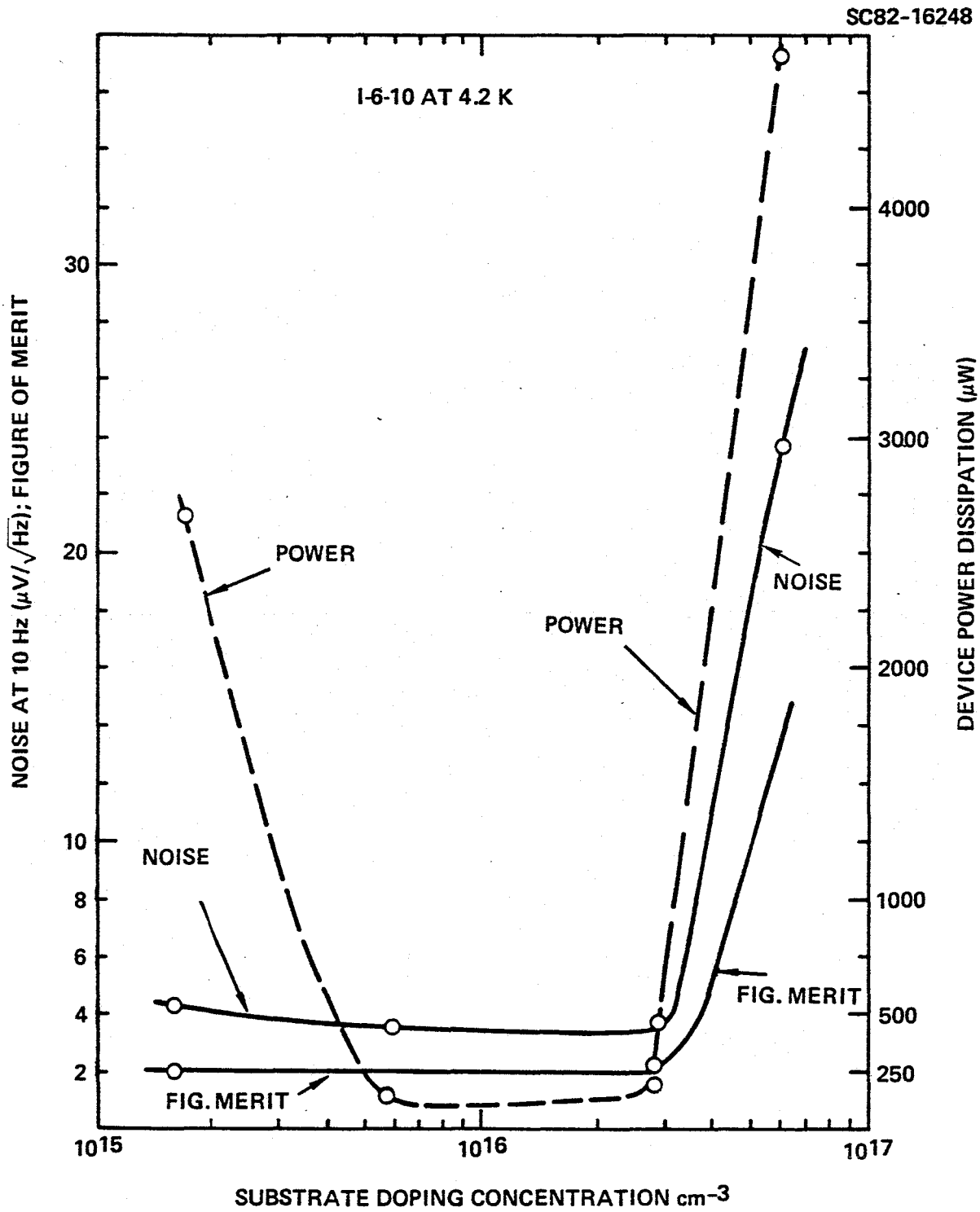



Fig. 5.18 MOSFET source-follower dependence on substrate (T = 4.2 K).

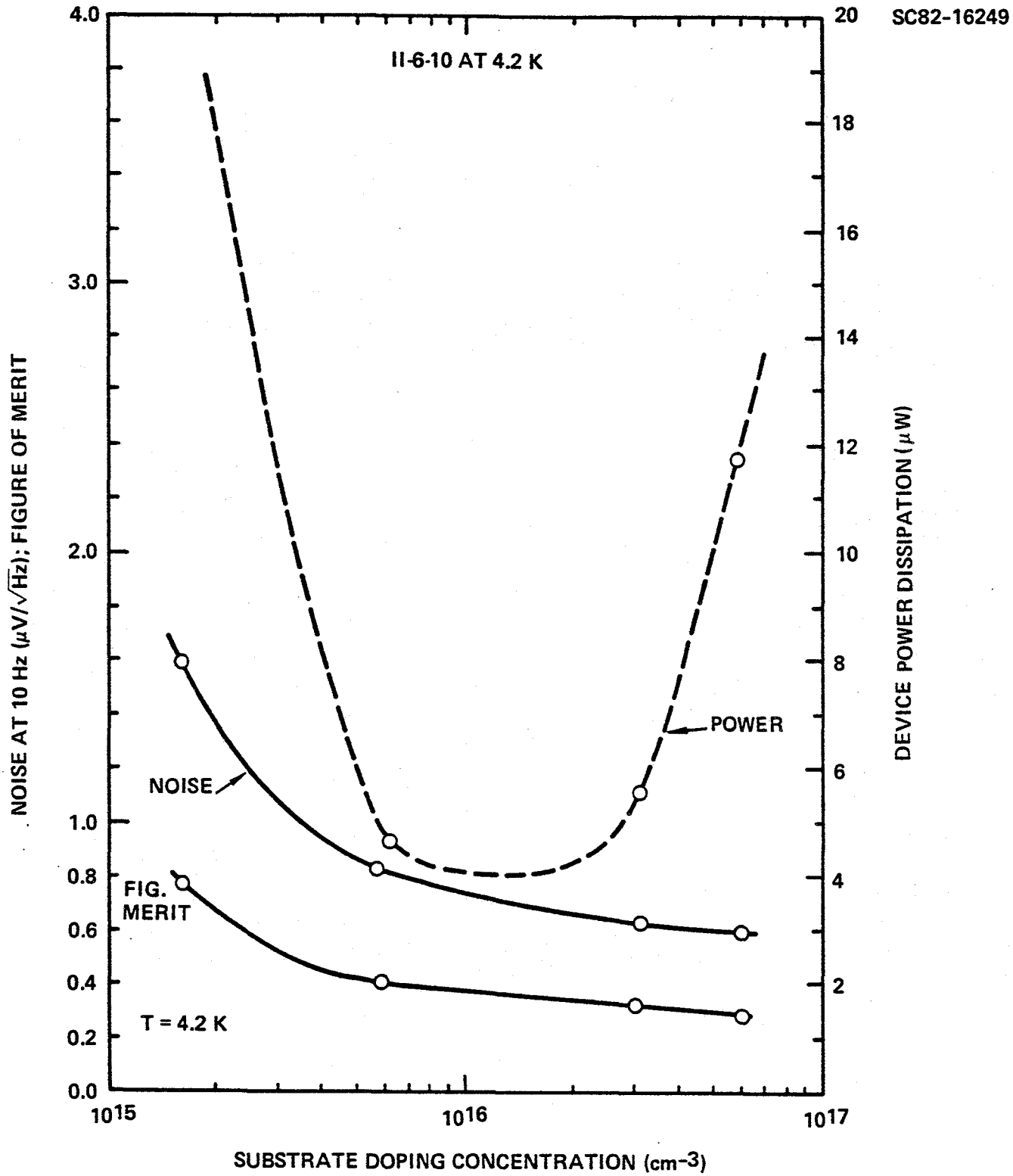



Fig. 5.19 CRYOFET source-follower dependence on substrate (T = 4.2 K).

(L = 6 μm , W = 10 mils) at 4.2 K, are for a G = 0.98, P = 5.5 μW, N (10 Hz) = 0.66 $\mu V/\sqrt{Hz}$ with figure-of-merit = 0.32.

5.2.5.3 Temperature Dependence

The tabulated data of Tables XV, XVI and XVII, in conjunction with the 4.2 K data, is used to elucidate the influence of temperature on the performance in the 2.4-20 K range for the CRYOFET II-6-10. In Fig. 5.20, the noise and calculated normalized figure-of-merits are plotted against temperature. Only for the case of No. 126-B-4-1, did we make a noise measurement at 15.2 K (spectrum appears in Fig. 5.17) which gave a peak value. The other noise curves were accordingly arbitrarily peaked in this temperature range to allow for a dependence which is expected but was not measured. At 4.2 K, noise data for device II-6-10 on No. 126-B-4-1 was obtained as tabulated. Unfortunately, this device was accidentally deactivated before the temperature run could be completed. Accordingly, temperature data obtained on II-37-10 on No. 126-B-4-1 was scaled to the 4.2 K noise value and the temperature data, which was multiplied by this scaling factor, is plotted on Fig. 5.20 for this substrate.

The CRYOFET calculated figures-of-merits are also plotted on Fig. 5.20. These curves are relatively independent of temperature. We draw the curves dashed in the 10-18 K range to allow for a possible peaking if the noise on these device also peaks at ~ 15 K.

The CRYOFET calculated dissipation power is plotted vs temperature in Fig. 5.21. In general, the power increases as the temperature is increased. This occurs because higher voltage is required to obtain the standard G = 0.98 condition. In the case of No. 126-B-4-1, the plotted data is obtained from device II-37-10 which is multiplied by a scaling factor derived by comparing it to device II-6-10 at 4.2 K.

At some elevated temperature, the CRYOFET loses its ability to function as an effective amplifier. This occurs at a temperature where the thermal ionization of charge carriers provides unacceptable leakage between

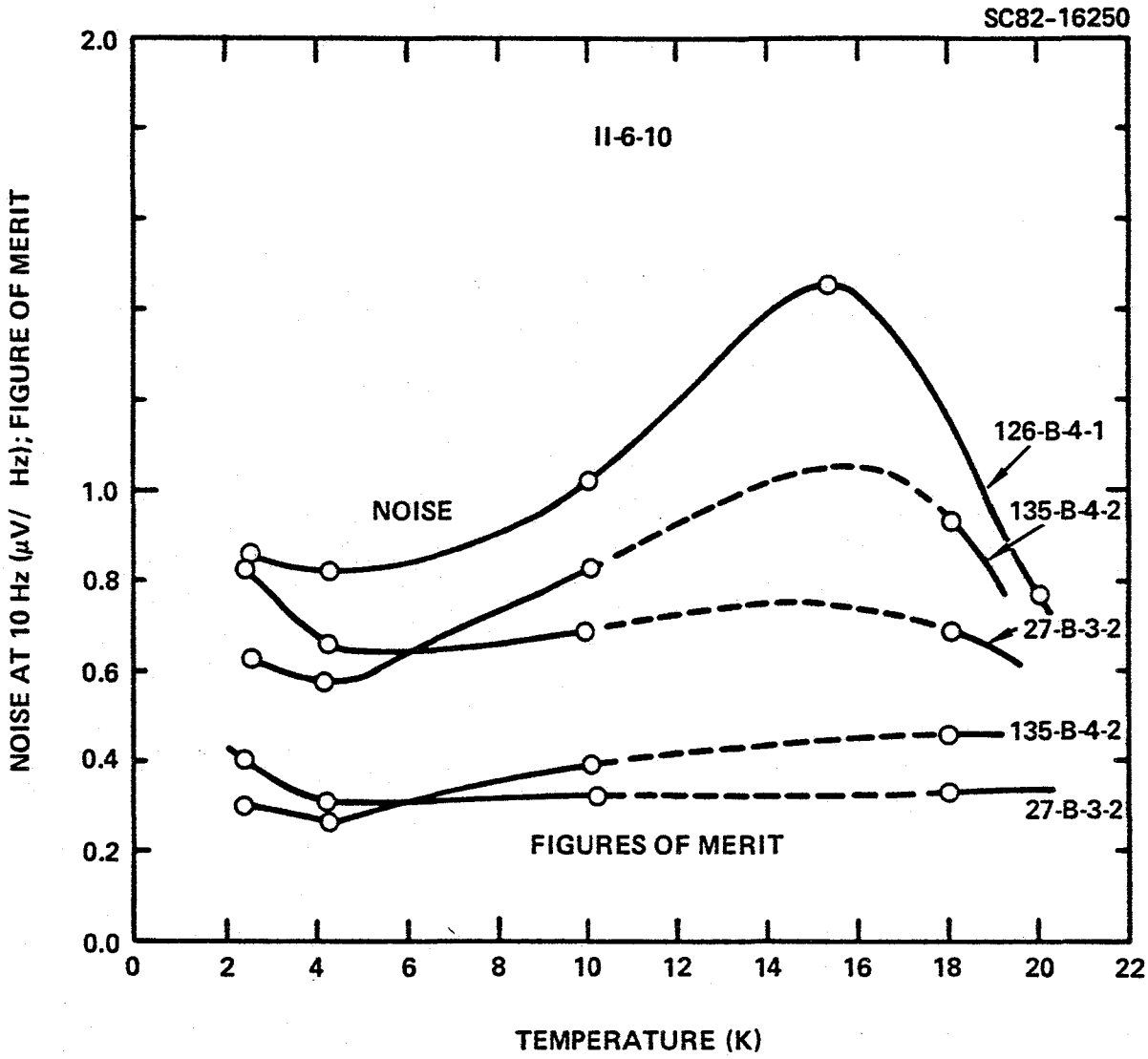



Fig. 5.20 CRYOFET noise and figure-of-merit dependence on temperature.

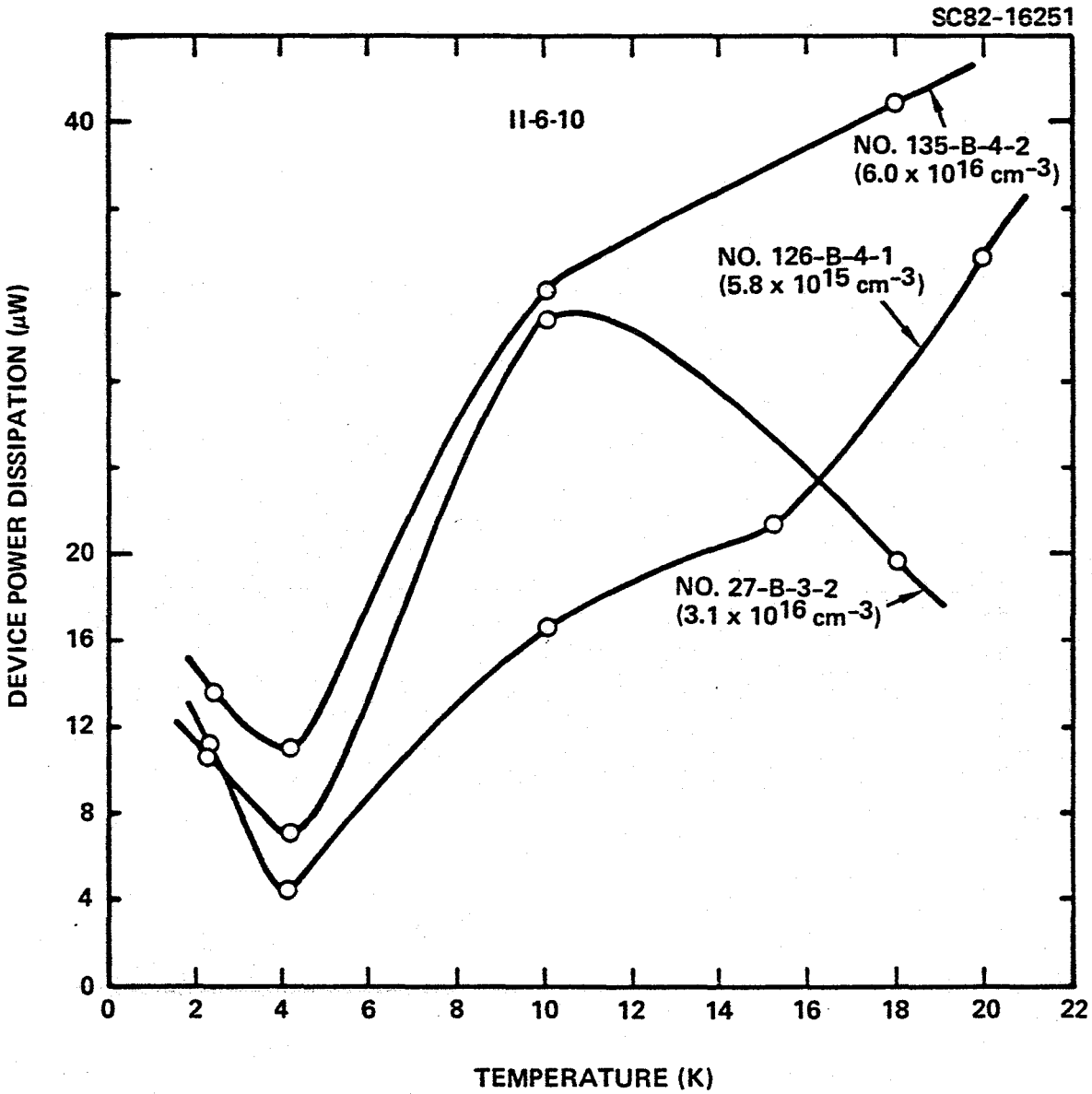



Fig. 5.21 CRYOFET power dissipation dependence on temperature.

the source and drain. The temperature depends on the activation energy of the impurity in the substrate, on the choice of source resistance compared to the leakage resistance and on the degree of leakage which may be tolerated in a given circuit application. For the arsenic doped silicon substrates employed in this study ($\Delta E$ = 0.054 eV), this leakage sets in at about 20 K (see Fig. 5.16) and limits performance. At 27 K, effective operation is no longer possible. The choice of an impurity with deeper activation energy in the substrate (Si:Bi with $\Delta E$ = 0.71 eV, for example) will allow CRYOFET operation to higher temperatures of about 30 K.

No long term device stability tests were carried out on this program. The absence of hysteresis effects in the I vs V characteristics of the CRYOFETs suggests that they are time stable. This inference is supported by experimental observations during measurements of no observable time drift and by our ability to repeat measurements on the same device on different days after warm up and cool down cycles.

## 6.0 CONCLUSIONS

The goal of this program was to design, produce, test and compare CRYOFETs (cryogenic MOSFETs) and conventional p-channel MOSFETs at low temperatures. The orientation in the testing was directed towards the intended applications of these devices which were to serve as source-follower preamplifiers for extrinsic detectors at low temperatures.

The design of the p-channel MOSFETs was conventional and utilized p diffusions for the source and drain on n type Si:As substrates. The CRYOFETs, which take advantage of low temperature charge carrier freezeout, utilized the same geometry but employed n diffusions for the source and drain on the same n type Si:As substrates. To elucidate a possible optimum geometry for low temperature operation, 16 different combinations of device gate width and length were designed for each CRYOFET and MOSFET. To elucidate a possible optimum substrate resistivity for low temperature operation, 4 different n-type substrate resistivities were employed.

Two lots were processed on the program to provide devices for test. In the first lot, a processing error resulted in no useful devices. The second lot was processed in two groups. The first group resulted in devices with high thresholds and source-drain leakage at low temperature. The second group, which employed thicker field oxide and a phosphorus gettering treatment, reduced the thresholds and eliminated the source-drain leakage.

Extensive measurements were made on the program, designed to elucidate the operational characteristics of the CRYOFETs and to compare their performance with that of the p-channel MOSFETs. These studies included device geometry, substrate resistivity and temperature covering the range from 2.4-27 K. These included gate-source capacitance, I vs V characteristic curves and measurements of the gain and noise as a function of frequency when the devices were used as source-followers and biased up to give gains of 0.98.

The measured data is presented as photographs of I vs V curve tracings and noise vs frequency curve tracings and tabulated data compiled in 12

tables. The data from the tables are then plotted to permit ready comparison of the salient performance features of the CRYOFET and the p-channel MOSFET. The plotted features selected are the noise, source-follower figure-of-merit and the device power dissipation. This comparison is made with the device operating with a gain of 0.98. These features are plotted as a function of substrate resistivity at 4.2 K and as a function of temperature covering the range from 2.4-20 K. Optimum performance is enhanced when these features attain minimum values.

The data and plots show the CRYOFET to be clearly superior to the p-channel MOSFET in each of these features. It exhibits noise some 2-4 times lower than the MOSFET over the temperature range and a correspondingly lower figure-of-merit. CRYOFET power dissipation at 4.2 K, at gain of 0.98, is some hundreds of times lower than that of the MOSFET operated at this same gain. The CRYOFET sustains these advantages up to about 20 K when device leakage limits operation. Other attractive advantages are that the thresholds and source voltage offsets are substantially lower than with MOSFETs so that the dynamic range and signal linearity of the CRYOFET may be superior. In addition, pair balancing of devices to remove source voltage offsets is more easily implemented with the reduced source voltages. The substantially reduced power dissipation of these devices reduces the requirements for the expenditure of cooling cryogens and thus may promote longer space missions. Further, it opens up the possibility for more extensive on focal plane signal processing which previously was ruled out because of excessive power dissipation.

The conclusion of this effort indicates that the goals set for the program have been realized. The design, production and testing of CRYOFETs and p-channel MOSFETs has been successfully carried out and the CRYOFET has been demonstrated to be a useful device for low temperature application with properties superior to existing MOSFET devices.

With the demonstration of the superiority of the CRYOFET over the MOSFET for low temperature application, it is useful to compare its properties

with that of the J-FET (P-N junction FET). This device operates in the depletion mode and provides noise levels which are substantially lower than either the MOSFETs or CRYOFETs. The device, however, becomes temperature depleted and does not operate at low temperatures. Recently, a J-FET development[1] was carried out in which J-FETs were mounted in packages supported by Dacron threads so that they were thermally insulated from the package walls. Equipped with a heater, their temperature was brought above the charge carrier freeze-out range and they could then be operated with detectors at lower temperatures. The dissipation power required is more than one order of magnitude higher than that required by the CRYOFET. Capacitance values of 4 pfd are reported which is almost an order of magnitude higher than that of the 0.48 pfd for our optimum CRYOFET size. This reduces the figure-of-merit advantage of the J-FET. Bulky packages are required with the insulated J-FETs which complicates their use with arrays. Finally, occasional drifts of the thermal equilibrium between the heat supplied and the heat conducted away may deactivate the device.

Although the low noise capabilities of the JFET increases the detector performance at moderate and higher frequencies, it loses this advantage at low frequencies where its low noise becomes irrelevant. This follows because, at low frequencies, the dominant noise for high performance detectors is that of the detector itself or that of the Johnson noise of its load resistor (Eq. (1), (2)). In this circumstance, the CRYOFET with its lower power dissipation, small size, and capacitance, and convenient application is clearly preferable to the J-FET.

## 6.1 Recommendations

The exploratory study on the properties of CRYOFETs was made using a test chip which was designed to study device geometry and permit comparison

[1] F.J. Low, "Application of JFETs to Low Background Focal Planes in Space," Proc. SPIE 280 (1981).

with MOSFET devices. The chip is, accordingly, large, and is mounted in a 42 pin package and individual devices are not readily used in practical applications. Taking into account the requirements of the NASA infrared astronomy programs, a configuration of two matched CRYOFET pairs suitable for use in the circuit of Fig. 1.3 would be expected to find useful application. It is recommended that a funded follow-on program be instituted to produce such pairs. This will require the design and exploitation of a new mask set to process these CRYOFET pairs. This processing would benefit from the experience gained on this program and accordingly optimized high quality devices at high yields could be anticipated. Instrumentation assembled for the measurements on this program could be expeditiously deployed to measure and qualify such devices in quantities sufficient to satisfy NASA requirements. In this way, practical devices uniquely appropriate to the NASA missions, which are currently unavailable, could become available in a timely fashion to support the NASA astronomy programs.

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15. Supplementary Notes

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16. Abstract

CRYOFETs, specifically designed for low temperature preamplifier application with infrared extrinsic detectors have been produced and comparatively tested with p-channel MOSFETs under matched conditions. The CRYOFETs exhibit lower voltage thresholds, high source-follower gains at lower bias voltage and lower DC offset source voltage. The noise of the CRYOFET is found to be 2-4 times lower than the MOSFET with a correspondingly lower figure of merit (which is established for source-follower amplifiers). The device power dissipation at a gain of 0.98 is some two orders of magnitude lower than for the MOSFET. Further, CRYOFETs are free of low temperature I vs V hysteresis and balky conduction turn-on effects and operate effectively in the 2.4-20K temperature range. These devices have promise for use on long duration sensor missions and for on-focal-plane signal processing at low temperatures which were heretofore excluded because of performance deficiencies and/or excessive power.

| 17. Key Words (Suggested by Author(s)) | 18. Distribution Statement |
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