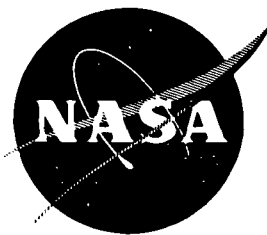


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DEVELOPMENT OF A LARGE AREA SPACE SOLAR CELL ASSEMBLY

by M. B. Spitzer

SPIRE CORPORATION

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16. Abstract This report describes a nine month program to develop a large area high efficiency solar cell assembly. The assembly consists of an ion implanted silicon solar cell and glass cover. The important attributes of fabrication are the use of a back surface field which is compatible with a back surface reflector, and integration of coverglass application and cell fabrications. Cell development experiments concerned optimization of ion implantation processing of 2 ohm-cm boron-doped silicon. Process parameters were selected based on these experiments and cells with area of 34.3 cm ² were fabricated. The average AMO efficiency of the twenty-five best cells was 13.9% and the best cell had an efficiency of 14.4%. An important innovation in cell encapsulation has also been developed. In this new technique, the coverglass is applied before the cell is sawed to final size. The coverglass and cell are then sawed as a unit. In this way, the cost of the coverglass is reduced, since the tolerance on glass size is relaxed, and costly coverglass/cell alignment procedures are eliminated. Adhesives investigated were EVA, FEP-Teflon sheet and DC 93-500. Details of processing and results are reported.					
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FOREWORD

Many individuals at Spire Corporation made contributions to this program. The Program Manager was P.R. Younger and the Principal Investigator was M.B. Spitzer. S.J. Solomon provided technical consultation on cell development and M.J. Nowland conducted the lamination studies.

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TABLE OF CONTENTS

<u>Section</u>		<u>Page</u>
1	INTRODUCTION	1-1
2	CELL DEVELOPMENT	2-1
2.1	Back Surface Field Studies	2-1
2.2	Emitter Development	2-3
2.2.1	Phosphorus Implantation	2-3
2.2.1.1	31P+ Implantation in a Preimplanted Surface	2-3
2.2.1.2	31P+ Implantation Through SiO ₂	2-6
2.2.1.3	Direct Phosphorus Implantation	2-11
2.2.2	Arsenic Implantation	2-11
2.2.2.1	Direct Arsenic Implantation	2-13
2.2.2.2	Arsenic Implanted Through SiO ₂	2-13
2.3	Lifetime Enhancement	2-19
2.4	Back Surface Reflector	2-28
2.5	Summary of Experiments	2-30
3	ENCAPSULATION	3-1
3.1	Assembly Configuration	3-1
3.2	Materials	3-1
3.3	Stress Analysis	3-2
3.4	Lamination	3-3
3.4.1	FEP-Teflon	3-3
3.4.2	Dow Corning 93-500	3-4
3.4.3	EVA	3-6
3.5	Assembly Sawing	3-6
3.6	Testing	3-8

TABLE OF CONTENTS (Concluded)

<u>Section</u>		<u>Page</u>
4	HIGH EFFICIENCY CELLS AND ASSEMBLIES	4-1
	4.1 Cell Fabrication	4-1
	4.2 Assembly Fabrication	4-1
5	COST PROJECTIONS	5-1
6	CONCLUSIONS	6-1
	REFERENCES	R-1
	APPENDIX: AMO CHARACTERISTICS OF 25 BEST SOLAR CELLS	

LIST OF ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
2-1	Furnace Temperature Cycle (a) BSF anneal, (b) Emitter Anneal	2-2
2-2	Spreading Resistance Profiles of Boron, Aluminum and Gallium Implants	2-4
2-3	Comparison of External Quantum Efficiency of $^{27}\text{Al}^+$ BSF Cell and $^{11}\text{B}^+$ BSF Cell	2-5
2-4	External Quantum Efficiency of a Pre-implanted Cell Compared to a Control Cell	2-7
2-5	Dark I-V Characteristics of a Pre-implanted Cell Compared to a Control Cell	2-8
2-6	Spreading Resistance Profiles of Phosphorus Implanted Through 800 Å of SiO ₂ at 75, 80, and 85 keV	2-10
2-7	Sheet Resistivity as a Function of $^{31}\text{P}^+$ Ion Dose	2-12
2-8	Cell Performance as a Function of $^{31}\text{P}^+$ Ion Dose	2-12
2-9	Spreading Resistance Profiles of Arsenic for Various Anneal Periods at 900°C	2-14
2-10	External Quantum Efficiency of Cells with Direct Arsenic Implantation	2-17
2-11	Spreading Resistance Analysis of the Implanted Back surface	2-22
2-12	External Quantum Efficiency of Cells with Back Surface Implantation	2-23
2-13	External Quantum Efficiency of AR-Implanted Cell	2-24
2-14	External Quantum Efficiency of Cell Implanted with Argon Followed by Boron	2-25
2-15	External Quantum Efficiency of a Cell Implanted with Boron	2-26
2-16	External Quantum Efficiency of a Cell without Back Surface Implantation	2-27
2-17	Measured Reflectance as a Function of Wavelength for Two BSR Structures	2-29

LIST OF ILLUSTRATIONS (Concluded)

<u>Figure</u>		<u>Page</u>
3-1	Configuration of the Assembly Consisting of a Wafer Containing the Cell and a Coverglass, Prior to Sawing	3-2
3-2	FEP-Teflon Lay-up Configuration	3-5
3-3	EVA Lay-up Configuration	3-5
3-4	Photograph of the Solar Cell Assembly	3-7
3-5	I-V Characteristics of Laminated Solar Cell	3-10
4-1	Photograph of Completed Assembly Consisting of an Ion Implanted Cell and Coverglass Sawed to Size Simultaneously	4-5

LIST OF TABLES

<u>Table</u>	<u>Page</u>
2-1	Point-Probe V_{OC} and Sheet Resistance Measurements for Three BSF Implants 2-3
2-2	Measured Performance of B, Ga, and Al BSF Solar Cells 2-4
2-3	$^{28}\text{Si}^+$ Implantation Schedule Consisting of Four Separate Implantations 2-6
2-4	Three Step Anneal Process 2-6
2-5	Measured Characteristics of Solar Cells Fabricated From Si Pre-Implanted Emitters 2-7
2-6	Sheet Resistance for Emitter Formed by $^{31}\text{P}^+$ Implantation Through 800 Å of SiO_2 2-9
2-7	Sheet Resistivity of Direct $^{75}\text{As}^+$ Implants 2-15
2-8	Implant and Anneal Parameters Used for Solar Cell Fabrication 2-16
2-9	Average AM0 Solar Cell Performance and Dark I-V Data 2-16
2-10	Sheet Resistance of the Arsenic-Through-Oxide Implantation Matrix 2-18
2-11	Point-Probe V_{OC} Measurements of Arsenic-Through- Oxide Implantation Matrix 2-18
2-12	Average AM0 Performance of $^{75}\text{As}^+$ Implanted Cells 2-19
2-13	Process Groups for Gettering Study 2-20
2-14	Measured Performance of AR-Implant Gettered Solar Cells 2-20
2-15	BOL and EOL Performance of Argon-Implanted Cells 2-21
2-16	Measured Values of Thermal Alpha for Four BSR Processes 2-28
3-1	AM0 Performance of Solar Cell at Each Lamination- and-Saw Process Step 3-9
3-2	AM0 Performance of Assemblies 3-9

LIST OF TABLES (Concluded)

<u>Table</u>		Page
4-1	High Efficiency Silicon Space Cell Process Sequence	4-2
4-2	Average AM0 Performance of Twenty-Five Cells	4-4
5-1	Assumed Starting Material Cost	5-2
5-2	Cost Per Watt of 10 kW Cell Sequence	5-2
5-3	Cost Per Watt for Processing 28.7 kWafers Per Year	5-3
5-4	Cost Per Wafer for Processing Space Solar Cells 28.7 kWafers Per Year	5-4
5-5	Cost for Two Production Levels	5-5

SECTION 1 INTRODUCTION

This is the final report for NASA contract NAS3-22236, a program to develop a large area silicon space solar cell assembly. Significant results were achieved in this effort. Space solar cells of area 34.3 cm^2 that had AM0 efficiency greater than of 14 percent, as measured by NASA-LeRC, were fabricated. In addition, processes were developed that offer substantial cost reduction when employed in large volume production. This report presents the results of the cell and assembly development studies as well as a discussion of cost projections for a space solar cell assembly, assuming kilowatt production lots.

The cell design investigated consisted of a shallow junction n^+pp^+ structure made from 2 ohm-cm boron-doped silicon. The cell thickness was $250 \mu\text{m}$ (10 mils). An important feature of the cell design was the use of a high quality back surface reflector (BSR).

In a recent report,⁽¹⁾ the various low-cost terrestrial cell fabrication technologies were examined and ion implantation was identified as a potential low-cost technology applicable to space cell fabrication. The approach taken in this program focused on this application; cell development was based entirely on ion implantation for p^+ and n^+ doping. In addition, a novel encapsulation technology was investigated and found to be not only feasible, but also low in cost.

The use of ion implantation is particularly advantageous for back surface field (BSF) formation in a space solar cell because implantation leaves the physical appearance of the surface unchanged. Thus, a wafer with a polished back can be used for BSR formation without repolishing after BSF fabrication. This should be contrasted with Al-paste processes, which require extensive repolishing before BSR formation.

In the new encapsulation technique investigated, the coverglass is applied to the wafer before the cell is sawed to final size. The coverglass and cell are then sawed as a unit. In this way, the cost of the coverglass is reduced, since the tolerance on glass size is relaxed, and costly coverglass/cell alignment procedures are eliminated.

This report includes the results of cell development and encapsulation development experiments (Sections 2 and 3), a discussion of the fabrication of deliverable cells (Section 4), and a discussion of cost projections (Section 5). Conclusions are presented in Section 6.

SECTION 2

CELL DEVELOPMENT

This section reviews the experiments that led to the development of the large area high efficiency cell. The structure investigated is the n^+pp^+ BSF solar cell, with the n^+ and p^+ regions formed by ion implantation.

Cell development consisted of an investigation of n^+ and p^+ ion implantation parameters, BSF formation techniques, and ion implantation gettering for lifetime enhancement. All development was based on 2 ohm-cm boron-doped (100) wafers that had polished front surfaces, were 7.6 cm in diameter (3 inch), and were 250 μm thick (10 mils). All large area cells were made from float zone silicon. Some development studies were conducted with Czochralski wafers, as indicated in the subsections that follow.

Solar cell testing was performed under simulated AM0 insolation at 25°C using a Spectrolab X25-MkII solar simulator with a D-550 electronic load. A temperature controlled test block was used for all measurements. Unless otherwise indicated, test cell area was 4 cm^2 .

2.1 BACK SURFACE FIELD STUDIES

The implantation of boron, gallium, and aluminum was investigated for BSF formation. The purpose of this experiment was the identification of the implant species that offers greatest V_{oc} enhancement. To insure maximum activation for each species, a long, high temperature anneal was used. Ordinarily, such an anneal would allow the junction to diffuse to an undesirable depth. To avoid this, the junction was implanted and annealed after BSF formation.

Starting material consisted of Czochralski wafers polished on both sides. The wafers were divided into three groups corresponding to the three implant species. Each group contained wafers of varying thickness to determine whether or not V_{oc} depended on the distance between the BSF and the junction.

Wafers were implanted with either $^{11}\text{B}^+$, $^{70}\text{Ga}^+$, or $^{27}\text{Al}^+$ at 50 keV to a dose of 5×10^{15} ions/ cm^2 at an implant angle of 10 degrees. To insure uniformity, the ion beam was scanned across the implanted surface as the wafers were rotated.⁽²⁾ The wafers were subsequently annealed in flowing N_2 with the temperature cycle indicated in Figure 2-1(a).

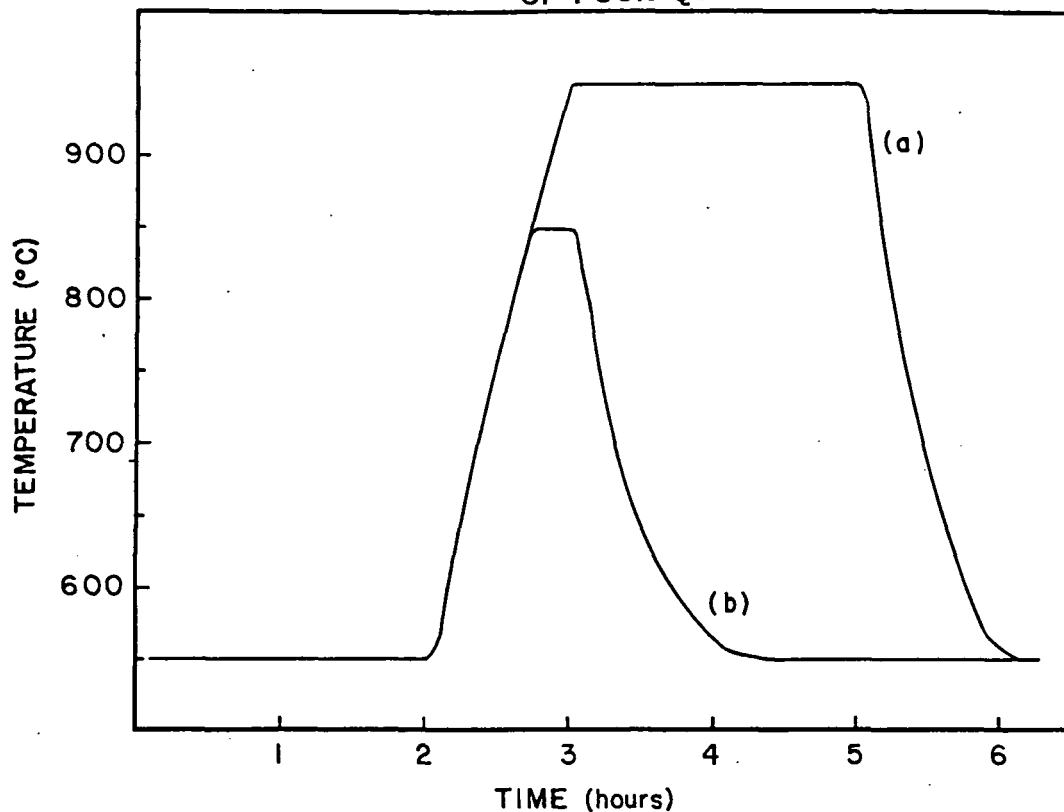


Figure 2-1. Furnace Temperature Cycle: (a) BSF anneal, (b) Emitter Anneal.

To form test cells, the front surfaces were implanted with $^{31}\text{P}^+$ at an energy of 10 keV and a dose of 2.5×10^{15} ions/cm², at an angle of 10 degrees. The wafers were then annealed in flowing N₂ with the temperature cycle indicated in Figure 2-1(b).

Table 2-1 indicates the point-probe V_{oc} and sheet resistance measurements for these wafers. Spreading resistance profiles were measured on samples taken from this group. These profiles are shown in Figure 2-2. They indicate that the greatest utilization fraction is obtained with boron.

Ti-Pd-Ag contacts were applied to the wafers and 2 cm x 2 cm cells were cut from each wafer. No AR coatings were deposited. Table 2-2 lists the result of cell testing. Best results were obtained with $^{11}\text{B}^+$ implantation. No significant dependence on thickness was observed. Figure 2-3 shows a comparison of the external quantum efficiency obtained with boron and aluminum.

2.2 EMITTER DEVELOPMENT

Both phosphorus and arsenic were investigated for front surface emitter fabrication. Various anneals were used to determine the furnace cycle necessary for optimal performance. The desired range of emitter sheet resistance was 50 to 100 ohms per square and the desired range of junction depth was 0.1 to 0.25 μm . Since our object was the investigation of low-cost terrestrial processes, refinements such as oxide passivation and junction tailoring⁽³⁾ were not pursued.

2.2.1 Phosphorus Implantation

The three types of phosphorus implantation examined were (1) phosphorus implanted into a preimplanted surface, (2) phosphorus implanted through SiO_2 , and (3) direct implantation of phosphorus. Best results were obtained with direct implantation.

2.2.1.1 $^{31}\text{P}^+$ Implantation in a Preimplanted Surface.

We have examined phosphorus implantation into surfaces that were first made amorphous by silicon preimplantation. Preimplantation was investigated because, by rendering the surface amorphous, it completely precludes channeling effects. In addition, the amorphous layer yields good epitaxial regrowth during the anneal, since the surface layer has no polycrystalline features.⁽⁴⁾

Table 2-1. Point-Probe V_{oc} and Sheet Resistance Measurements for Three BSF Implants

Ion	Thickness (mils)	R_{sheet} ohms per square	V_{oc} (mV)
BORON	7.2	20	560
	7.8	20	579
	9.9	18	590
	10.1	19	595
	11.4	18	592
	11.6	18	581
ALUMINUM	7.2	79	566
	9.6	61	535
	9.6	60	573
	11.2	55	551
GALLIUM	7.6	75	538
	7.7	70	573
	9.5	65	554
	10.2	57	445

Table 2-2. Measured Performance of B, Ga, and Al BSF Solar Cells

BSF (no. of cells)	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)
Boron (35)	595 (003)	27.0 (0.4)	78.7 (1.4)	9.37 (0.24)
Gallium (11)	584 (005)	26.0 (0.3)	77.4 (4.0)	8.71 (0.59)
Aluminum (24)	584 (003)	26.2 (0.3)	78.8 (0.8)	9.00 (.14)

Notes: Simulated AMO insolation, T = 25°C. No AR coating. Cell area is 4cm². Standard deviation shown in parenthesis.

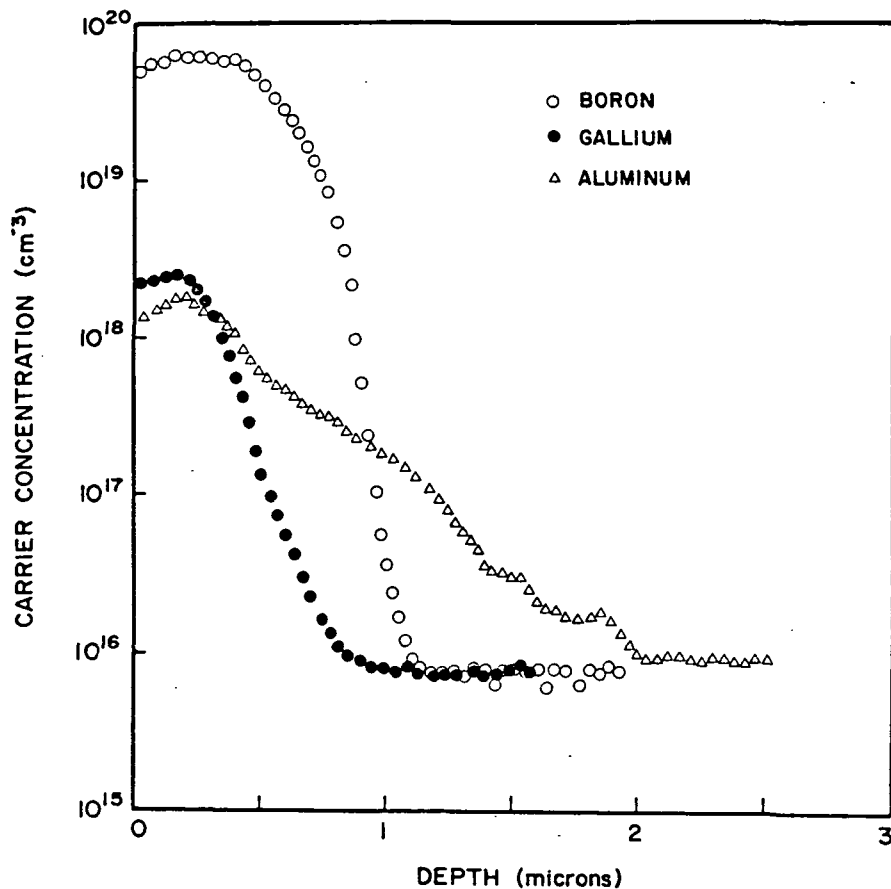


FIGURE 2-2. Spreading Resistance Profiles of Boron, Aluminum and Gallium Implants

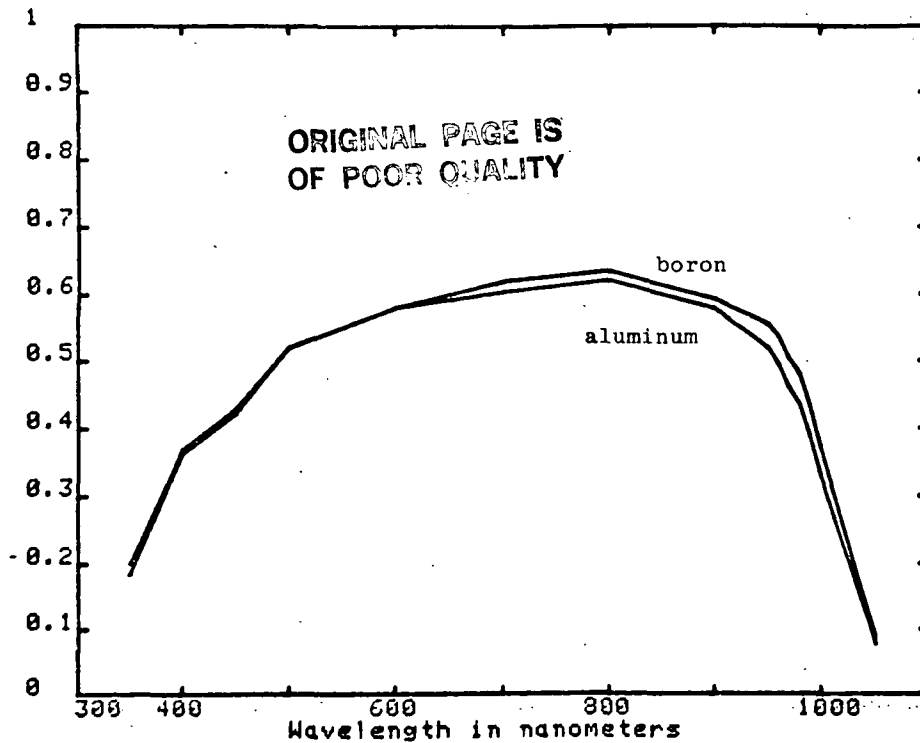


Figure 2-3. Comparison of external quantum efficiency of $^{27}\text{Al}^+$ BSF cell and $^{11}\text{B}^+$ BSF cell

Starting material consisted of $250\ \mu\text{m}$ thick Czochralski (100) wafers, polished on both sides. The backs were implanted with boron at 25 keV to a dose of 5×10^{15} ions/cm² at an angle of 10 degrees. The anneal shown in Figure 2-1(a) was then employed. The group was divided in half. One half received the $^{28}\text{Si}^+$ implantation shown in Table 2-3 while the other half received no $^{28}\text{Si}^+$ implant.

Following Si preimplantation, all wafers were implanted with $^{31}\text{P}^+$ at 10 keV with a dose of 2.5×10^{15} ions/cm². All wafers were annealed in flowing N_2 with the three step process indicated in Table 2-4.

Junction depth was measured by the groove and stain technique and was found to be $0.17\ \mu\text{m}$ in a pre implanted wafer and $0.33\ \mu\text{m}$ in a control. Sheet resistance was measured with a four-point probe. It was found to be 75 ohms per square for a preimplanted wafer and 71 ohms per square for a control.

Wafers were metallized with Ti-Pd-Ag contacts and sawed to 2 cm x 2 cm size. No AR coatings were applied. Thirty experimental cells and 21 controls were produced. Table 2-5 shows the measured AM0 performance for each group. The preimplanted cells have significantly lower V_{oc} .

Although the groove and stain measurements indicate a shallower junction in the preimplanted cells, this is not consistent with the device measurements. Figure 2-4 shows the external quantum efficiency of a preimplanted cell and a control cell. These cells were picked because they each have short circuit current approximately equal to the group average. The difference in quantum efficiency cannot be discerned.

Representative dark log(I)-V characteristics (Figure 2-5) indicate increased saturation current for the preimplanted devices. This is consistent with the decreased V_{oc} shown in Table 2-5. This decrease probably arises from increased emitter current owing to nonannealed defects introduced by the Si preimplantation.

2.2.1.2 $^{31}\text{P}^+$ Implantation Through SiO_2

The implantation of phosphorus through SiO_2 was investigated to determine if in this way better control over the doping profile might be obtained. The advantage of this technique is that the peak of the Gaussian distribution which describes the profile of the implanted ions can be placed at the SiO_2 -Si interface. Subsequent removal of the oxide yields a profile with a peak at the silicon surface. Consequently, no retrograde field exists near the silicon surface. A disadvantage is the introduction of recoil oxygen atoms.⁽⁵⁾

Table 2-3. $^{28}\text{Si}^+$ Implantation Schedule Consisting of Four Separate Implantations

Implant Number	Energy (keV)	Dose (ions/cm ²)	Proj. Range (angstroms)
1	50	1×10^{15}	696
2	30	6×10^{14}	413
3	20	3×10^{14}	279
4	10	1×10^{14}	150

Table 2-4. Three Step Anneal Process

Step	Temperature	Time
1	550°C	2 hours
2	850°C	15 minutes
3	550°C	2 hours

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Table 2-5. Measured Characteristics of Solar Cells Fabricated
From Si Pre Implanted Emitters

Group	No. of Cells	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF (%)	EFF (%)
Pre implanted	30	555 (002)	26.8 (0.1)	77.2 (2.2)	8.5 (0.3)
- Controls	21	582 (001)	26.6 (0.2)	78.1 (1.3)	9.0 (.12)

Notes: Simulated AM0 illumination, T = 25°C, No AR coating. Cell area = 4 cm². Standard deviation shown in parenthesis.

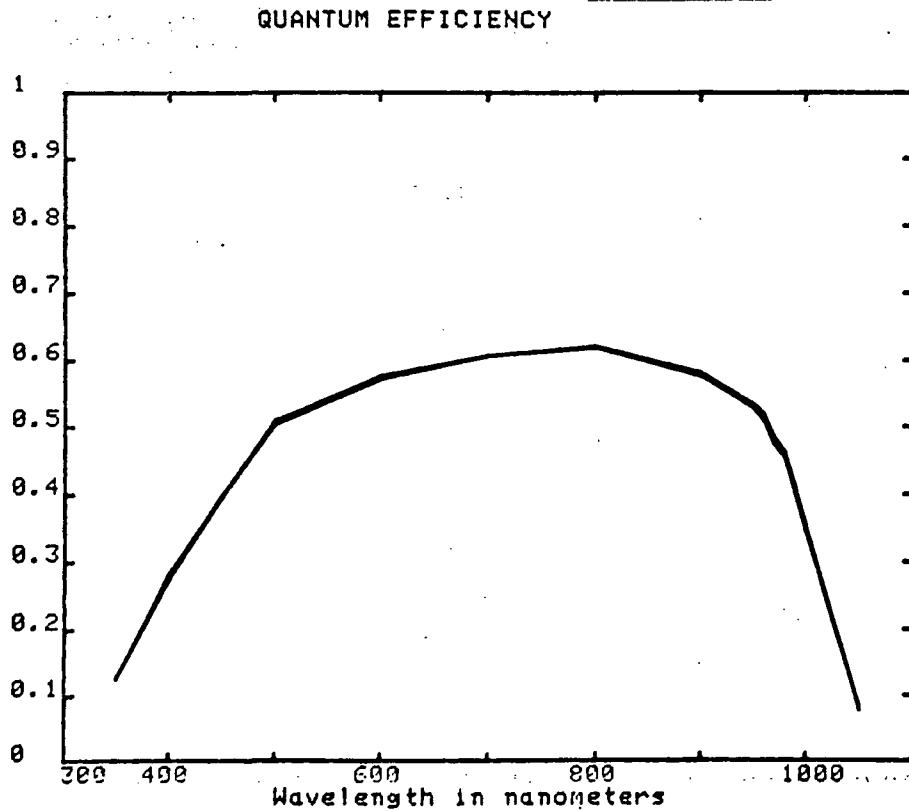


Figure 2-4. External quantum efficiency of a pre-implanted cell compared to a control cell

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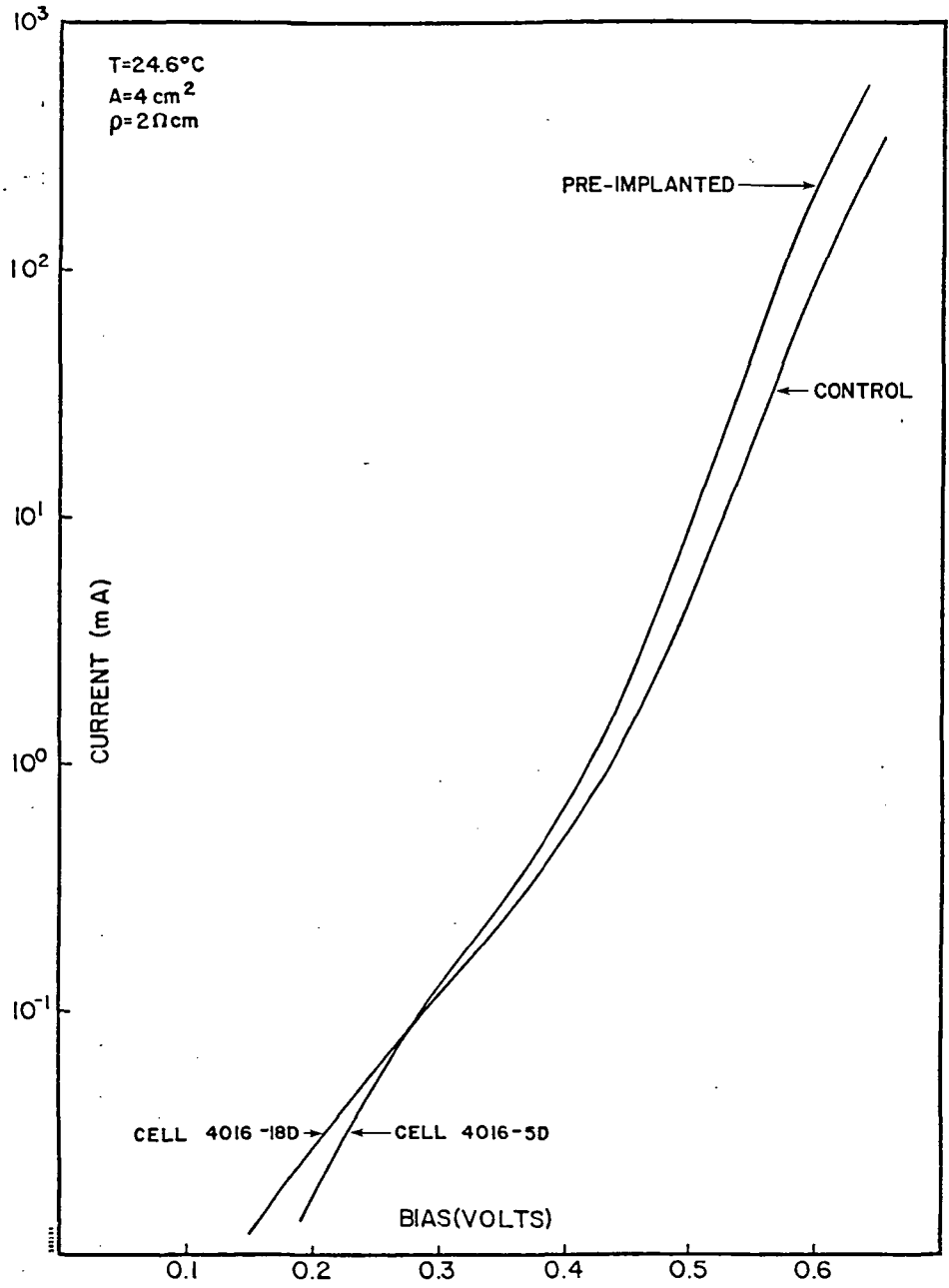


Figure 2-5. Dark I-V characteristics of a pre implanted cell compared to a control cell

Starting material consisted of (100) Czochralski silicon wafers with polished front surfaces. Back surfaces were implanted with boron at 50 keV with a dose of 5×10^{15} ions/cm² at an implant angle of 10 degrees. The wafers were oxidized in dry O₂ at 550°C for two hours followed by 950 degrees C for three hours. The resulting oxide was approximately 800 Å thick.

In order to place the implant profile peak at the Si-SiO₂ interface, the ion range must be selected to match the oxide thickness. The projected range of 80 keV phosphorus ions in SiO₂ is 792 Å. Therefore, implantation was conducted at 75, 80, and 85 keV. Since one half of the implant profile resides in the oxide, the dose was increased to 5×10^{15} ions/cm². The implant angle was 10 degrees.

We examined annealing with and without the oxide present. The temperature cycle used for the anneal of the phosphorus implant is shown in Figure 2-1(b). Table 2-6 indicates the sheet resistance for the emitters produced in this way. Since the phosphorus is not soluble in the oxide, it diffuses into the silicon during the anneal. This explains the lower sheet resistance occurring in samples for which the oxide was not removed until after the anneal.

Figure 2-6 shows the spreading resistance analysis of the wafers processed in this way. In all cases, the junction depth is greater than the desired depth of between 0.1 and 0.25 μm. Because better results were obtained with direct phosphorus implantation, we chose to terminate studies of implantation through SiO₂.

It is interesting to note the change in the profile slope occurring at an impurity concentration of approximately 3×10^{18} cm⁻³. We attribute this profile to concentration dependent diffusion. The mechanisms governing diffusion during the anneal are not well understood and should perhaps be the object of further study.

Table 2-6. Sheet Resistance for Emitter Formed by ³¹P⁺ Implantation Through 800 Å of SiO₂

Energy (keV)	Projected Range (Å)	Sheet Resistance (Ω/□)	
		Oxide Removed Before Anneal	Oxide Removed After Anneal
75	740	69	60
80	792	58	50
85	844	53	48

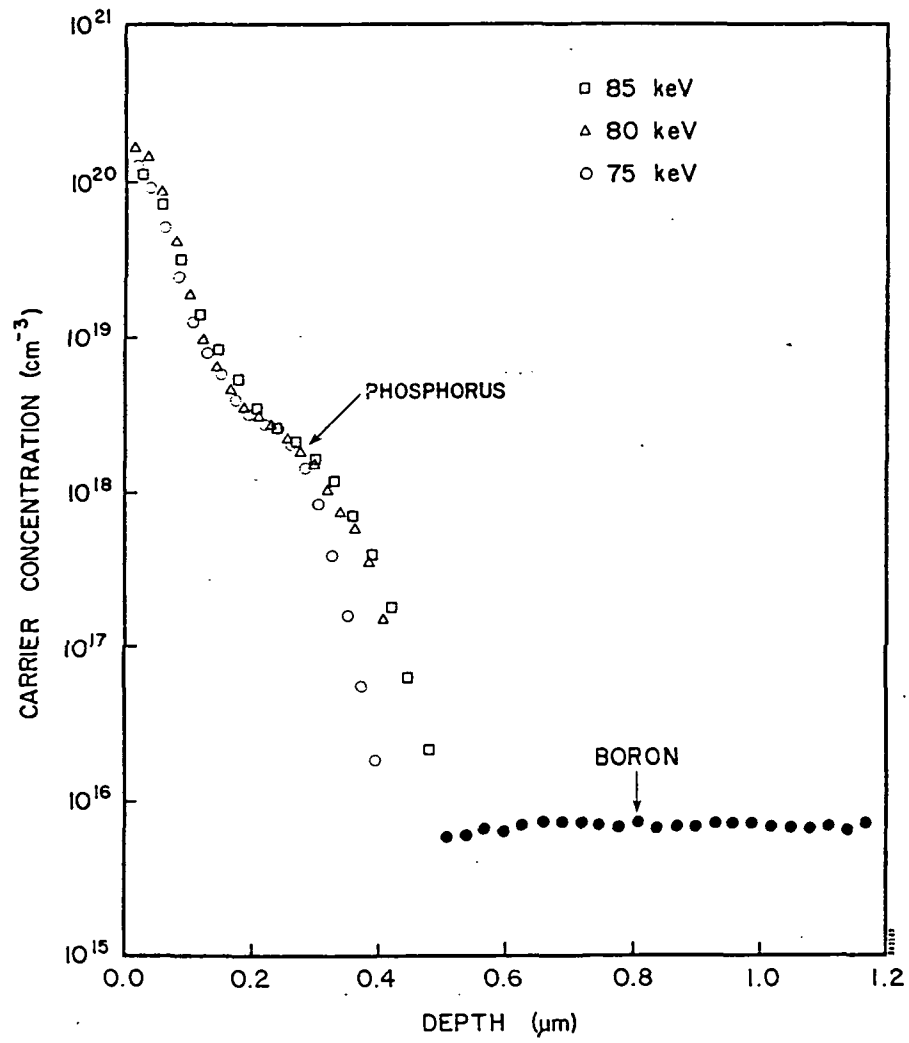


Figure 2-6. Spreading resistance profiles of phosphorus implanted through 800 \AA of SiO_2 at 75, 80, and 85 keV

2.2.1.3 Direct Phosphorus Implantation

Based on the results of the control cells in the preimplantation studies, we examined direct implantation of phosphorus. Since the integral of the spreading resistance profiles consistently indicated that large amounts of the implanted phosphorus were not activated, we considered implantation at reduced dose ($< 2.5 \times 10^{15}$ ions/cm²).

Starting material consisted of (100) float zone silicon wafers which were polished on both sides. The backs were implanted with $^{11}\text{B}^+$ at 50 keV to a dose of 5×10^{15} ions/cm² at 10 degrees. The wafers were then annealed using the cycle shown in Figure 2-1(a).

The wafers were divided into two groups for front implantation at 5 and 10 keV. The dose was varied between 1×10^{15} and 2.5×10^{15} ions/cm² within each group. Figure 2-7 shows the results of a measurement of sheet resistivity for each energy and dose. Note that above 2×10^{15} ions/cm², the sheet resistivity is insensitive to further increase in dose. We infer from this that above 2×10^{15} ions/cm² the dose exceeds the solid solubility.

Solar cells were fabricated from wafers implanted at 5 keV. Cell area was 34.3 cm². Metallization consisted of patterned Ti-Pd-Ag on the front and full area Al-Ti-Pd-Ag on the back. No AR coatings were used.

Cell performance was measured under simulated AM0 insolation. Performance data is graphed in Figure 2-8. The dashed lines indicate a fit to the data by the method of least squares. Note that FF is approximately constant between 1.5×10^{15} and 2.5×10^{15} ions/cm², which is consistent with the sheet resistivity measurements in Figure 2-7. V_{oc} increases in this range, indicating that non activated phosphorus is in some way important to cell performance. This needs to be studied in greater detail.

2.2.2 Arsenic Implantation

We investigated the use of arsenic for shallow junction formation. The projected range of arsenic in silicon is much less than that of phosphorus. Consequently, junction depth should be considerably less than that which is achieved with phosphorus implantation. In these studies, we investigated both direct and indirect arsenic implants, with very shallow junctions obtained in each case.

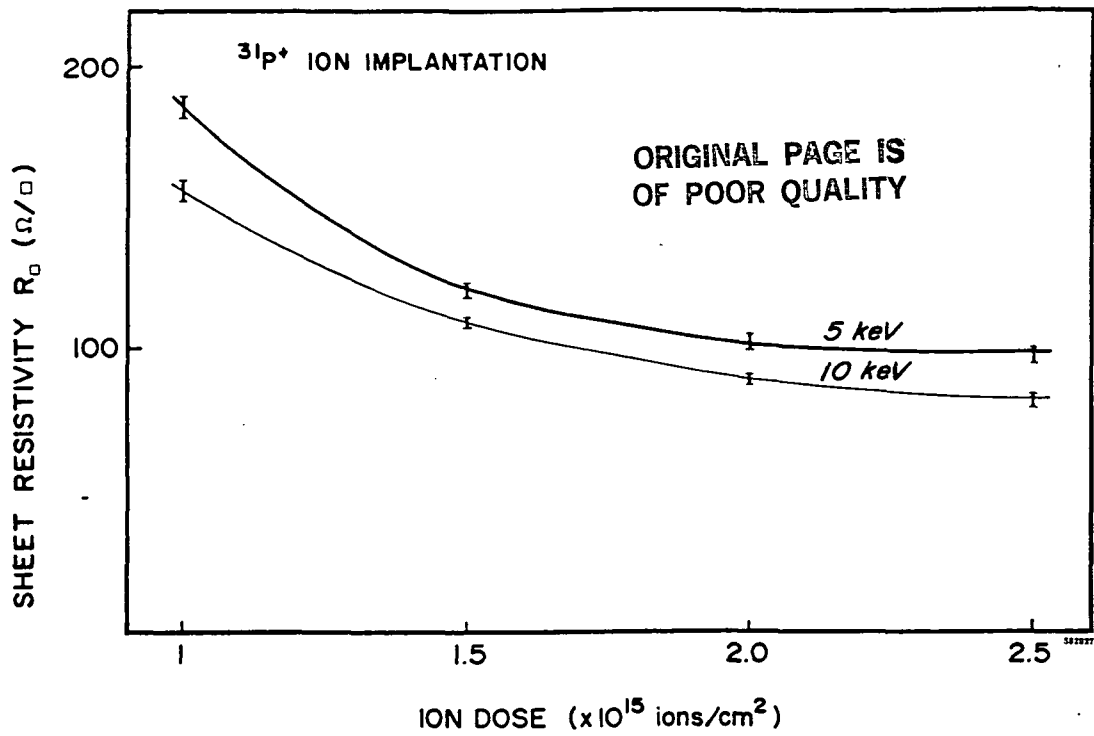


Figure 2-7. Sheet resistivity as a function of $^{31}\text{P}^+$ ion dose

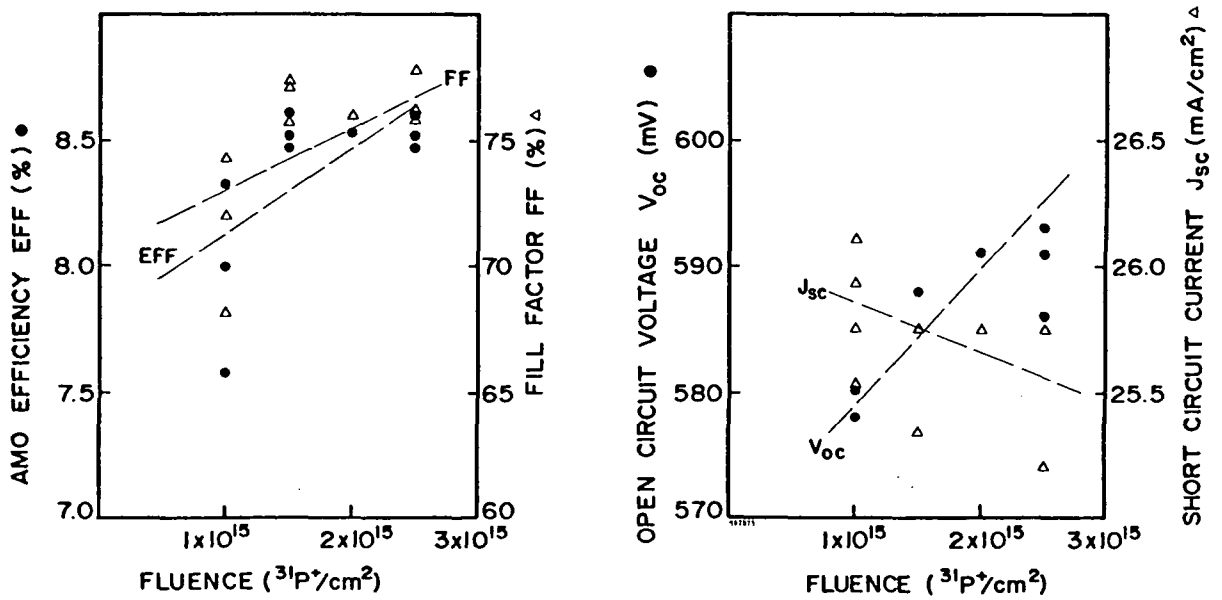


Figure 2-8. Cell performance as a function of $^{31}\text{P}^+$ ion dose

2.2.2.1 Direct Arsenic Implantation

Starting material consisted of (100) Czochralski silicon wafers with thickness of 380 μm (15 mils), and polished fronts. The wafers were implanted with $^{75}\text{As}^+$ and annealed at 900°C in flowing oxygen. A range of implantation energy, dose, and anneal cycles was studied. The resulting sheet resistivity is shown in Table 2-7. All parameters studied yielded acceptable sheet conductivity. Figure 2-9 shows the spreading resistance analysis for emitters annealed at 900°C for various durations. In all cases, the junctions are approximately 0.1 μm .

Solar cells were fabricated using implantation and anneal parameters selected on the basis of the data in Table 2-7. These parameters are indicated in Table 2-8. A back surface field was formed by boron implantation. A single anneal served to regrow front and back surfaces simultaneously. Wafers were metallized using patterned Ti-Pd-Ag contacts, and were sawed to final size (2 cm x 2 cm). No AR coatings were employed.

Dark and light I-V characteristics were obtained for all cells. These are summarized in Table 2-9. Examination of the dark log (I)-V characteristics indicates that the predominant current transport mechanism is diffusion ($n \approx 1$). V_{oc} , however, was lower than that obtained by phosphorus implantation.

The external quantum efficiency for these cells is shown in Figure 2-10. Comparison to the external quantum efficiency of phosphorus cells indicates that these cells have better blue response but poorer red response. We infer from this data that the arsenic junctions are performing well and that cell performance is limited by low bulk lifetime.

2.2.2.2 Arsenic Implanted Through SiO_2

We examined the implantation of arsenic through a thin layer of SiO_2 . The advantage of this technique was described briefly in Section 2.2.1.2.

Starting material for this experiment consisted of polished (100) Czochralski wafers that were 380 μm thick. Each wafer was oxidized in flowing dry O_2 at 900°C for 90 minutes. The resulting oxide was 100 Å thick.

The fronts of the wafers were divided into three groups and implanted with $^{75}\text{As}^+$ at 70, 75, and 80 keV with a dose of 10^{16} ions/cm² at an angle of 10 degrees. The anneals shown in Table 2-10 were carried out in flowing N_2 . Four-point probe measurements of sheet resistance are also shown in the table. Table 2-11 shows the point-probe V_{oc} measurement data.

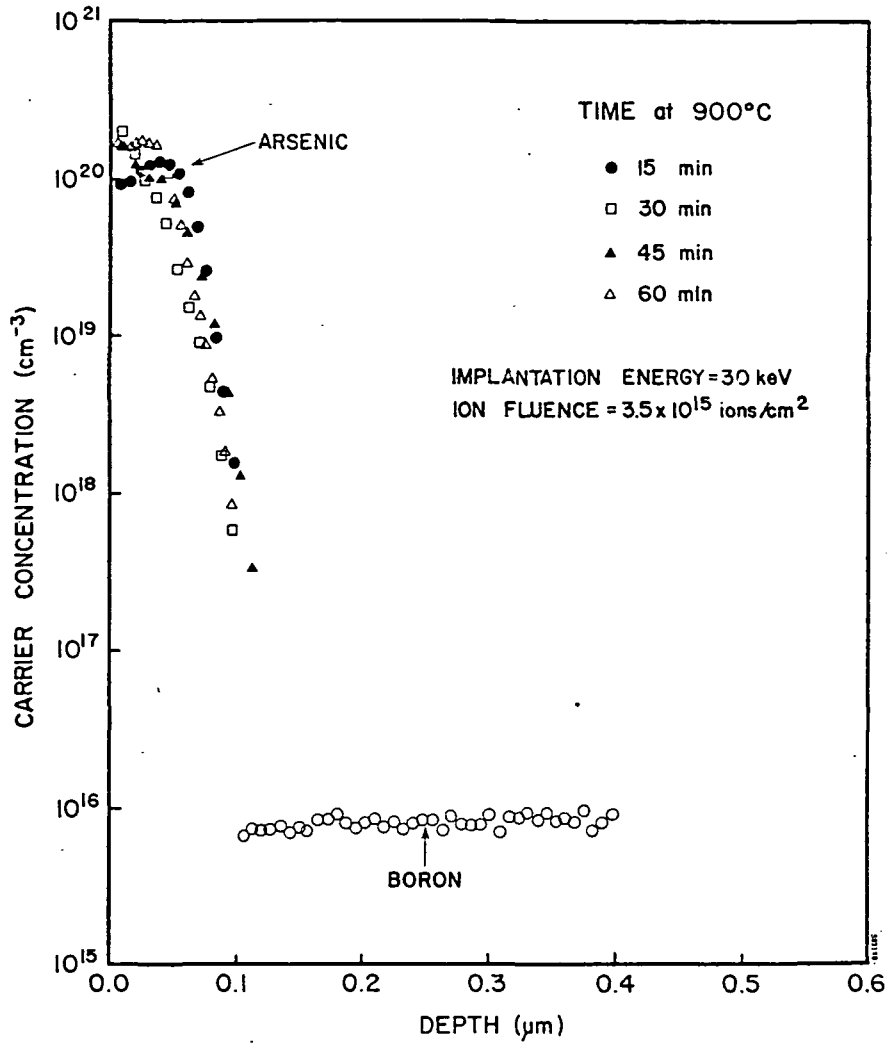


Figure 2-9. Spreading resistance profiles of arsenic for various anneal periods at 900°C.

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Table 2-7. Sheet Resistivity (ohms per square) of Direct $^{75}\text{As}^+$ Implants

Anneal Time (min)	Implant Energy and Dose				
	30 keV $3.5 \times 10^{15} \text{cm}^{-2}$	30 keV $7 \times 10^{15} \text{cm}^{-2}$	30 keV $1.4 \times 10^{16} \text{cm}^{-2}$	40 keV $2 \times 10^{15} \text{cm}^{-2}$	40 keV $1.4 \times 10^{16} \text{cm}^{-2}$
15	105	100	113	91	82
30	95	88	83	79	75
45	89	81	80	74	64
60	89	80	64	69	60

Table 2-8. Implant and Anneal Parameters Used for
Solar Cell Fabrication

Group	Emitter	BSF	Anneal
6	$^{75}\text{As}^+$, 30 keV 7×10^{15} ions/cm ²	$^{11}\text{B}^+$, 25 keV 5×10^{15} ions/cm ²	550°C - 2 hrs, 850°C - 1/2 hr, 550°C - 2 hrs flowing N ₂
3	$^{75}\text{As}^+$, 30 keV 3.5×10^{15} ions/cm ²	$^{11}\text{B}^+$, 50 keV 5×10^{15} ions/cm ²	900°C - 1/2 hr flowing O ₂
7	$^{75}\text{As}^+$, 30 keV 7×10^{15} ions/cm ²	$^{11}\text{B}^+$, 50 keV 5×10^{15} ions/cm ²	900°C - 1/2 hr flowing O ₂

Table 2-9. Average AM0 Solar Cell Performance
And Dark I-V Data

Group	No. of Cells	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF (%)	Eff (%)	J _o (mA/cm ²)	n-factor
6	4	568 (001)	25.4 (1.2)	73.4 (4.2)	7.9 (0.8)	3×10^{-7}	1.24
3	6	567 (001)	24.2 (0.9)	77.3 (0.1)	7.9 (0.4)	7.3×10^{-8}	1.13
7	6	555 (001)	22.5 (0.1)	78.0 (0.3)	7.2 (0.1)	1.2×10^{-7}	1.16

Notes: Cell area is 4 cm². No AR coatings were used. T = 25°C. Standard deviation is shown in parenthesis.

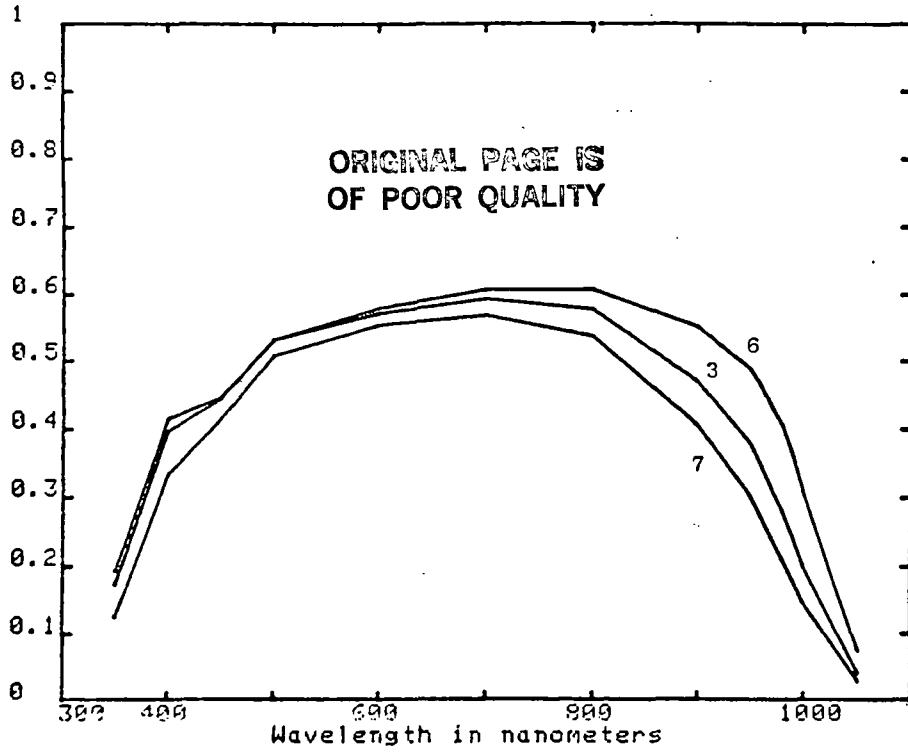


Figure 2-10. External quantum efficiency of cells with direct arsenic implantation

Table 2-10. Sheet Resistance (ohms per square) of the Arsenic-Through-Oxide Implantation Matrix

Implant Energy	Anneal			
	900°C-75 min	950°C-16 min	1000°C-10 min	1000°C-5 min
70 keV	45	37	25	26
75 keV	48	38	27	28
80 keV	44	35	24	26

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Table 2-11. Point-Probe V_{oc} Measurements (mV) of Arsenic-Through-Oxide Implantation Matrix

Implant Energy	Anneal			
	900°C-75 min	950°C-16 min	1000°C-10 min	1000°C-5 min
70 keV	480	472	432	441
75 keV	390	473	460	426
80 keV	514	523	403	368

Table 2-12. Average AM0 Performance of $^{75}\text{As}^+$ Implanted Cells

Implant Energy	No. of Cells	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)
75 keV	12	562 (002)	22.0 (0.1)	78.6 (0.5)	7.2 (0.1)
80 keV	10	561 (006)	21.9 (0.4)	76.7 (3.4)	7.0 (0.4)

Notes: Standard deviation in parenthesis. No AR coating. Cell area is 4 cm². T = 25°C.

Cells were fabricated in two groups using 75 and 80 keV implantation with a fluence of 7×10^{15} ions/cm². Backs were implanted with $^{11}\text{B}^+$ at 50 keV with a fluence of 5×10^{15} ions/cm². The wafers were annealed in dry N₂ for 16 minutes at 950°C followed by 550°C for two hours. Ti-Pd-Ag contacts were applied and 2 cm x 2 cm cells were sawed from each wafer.

AM0 test data for these cells is shown in Table 2-12. Dark log (I)-V curves were also examined; the average n-factor was 1.22 with a standard deviation of 0.09. We infer from this that these devices are essentially the same as the arsenic emitter cells discussed in the previous section. Measurement of external quantum efficiency indicated poor red response which we attribute to low bulk lifetime.

2.3 LIFETIME ENHANCEMENT

An experiment was undertaken to evaluate the effect of implant-gettering using argon back-surface damage. Back surface damage has been reported to getter oxygen in silicon,⁽⁶⁾ and it was thought that lifetime enhancement might be possible using such a process.

The starting material was 250 μm thick Czochralski silicon. The wafers were divided into four groups, as shown in Table 2-13. Argon was implanted on the backs of wafers in groups 1 and 2 at 10 keV to a dose of 10^{16} ions/cm². The boron was implanted at 50 keV to a dose of 5×10^{15} ions/cm². The anneal of the back surface consisted of a ramp from 550°C to 950°C; 950°C for one hour, followed by a ramp to 550°C, all in flowing N₂ (Figure 2-1(a)).

Table 2-13. Process Groups for Gettering Study

Group	Wafers	Back Implant
1	1-4	Argon
2	5-8	Argon followed by boron
3	9-12	Boron
4	12-16	None

Table 2-14. Measured Performance of AR-Implant Gettered Solar Cells

Back Imp.	No. of Cells	V _{oc} (mV)	J _{sc} (mA/cm ²)	FF (%)	EFF (%)
Ar	18	.579 (.003)	26.2 (0.3)	76.6 (1.5)	8.6 (0.2)
Ar + B	24	.592 (.002)	27.3 (0.7)	77.2 (1.7)	9.3 (0.3)
B	20	.592 (.002)	27.7 (0.3)	77.5 (1.7)	9.4 (0.2)
None	24	.582 (.002)	26.3 (0.3)	76.9 (1.9)	8.7 (0.2)

Notes: Cell area = 4 cm². Temperature = 25°C. No AR coating was used. Standard deviation shown in parenthesis.

Junctions were formed by phosphorus implantation (10 keV , $2.5 \times 10^{15} \text{ ions/cm}^2$) and were annealed using a three-step ramped anneal that consisted of 550°C for two hours, ramp to 850°C , 850°C for 15 minutes, ramp to 550°C , 550°C for two hours, as shown in Figure 2-1(b). Figure 2-11 shows the spreading resistance analysis of the back surface. The implantation of Ar does not change the B profile.

Table 2-14 shows the measured AM0 performance of the finished $2 \text{ cm} \times 2 \text{ cm}$ cells. The argon would appear to play no role in solar cell performance, either with or without a boron BSF. External quantum efficiency was also measured (Figure 2-12). It shows no difference between boron and argon-plus-boron cells. It is concluded that the above back surface implantation process does not improve performance.

Since the process could result in oxygen gettering without improved performance, we examined the radiation hardness of one cell from each group by subjecting the cells to $4.2 \times 10^{14} \text{ e/cm}^2$ at 1 MeV . Table 2-15 shows the change in efficiency for these cells, and Figures 2-13 to 2-16 show the changes in external quantum efficiency. These results indicate that no enhanced radiation hardness was achieved. However, a sample of statistically significant size was not tested.

Table 2-15. BOL and EOL Performance of Argon-Implanted Cells

Cell No.	Back Implant	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)
2F	Ar	582	26.6	78.1	8.9
		547	23.0	70.6	6.6
8C	Ar,B	595	27.8	78.5	9.6
		553	23.1	77.3	7.3
9F	B	596	28.2	78.2	9.7
		550	23.2	76.3	7.2
14C	None	582	26.2	79.7	9.0
		547	22.8	77.2	7.1

Notes: Simulated AM0. No antireflection coatings employed. $T = 25^\circ\text{C}$.

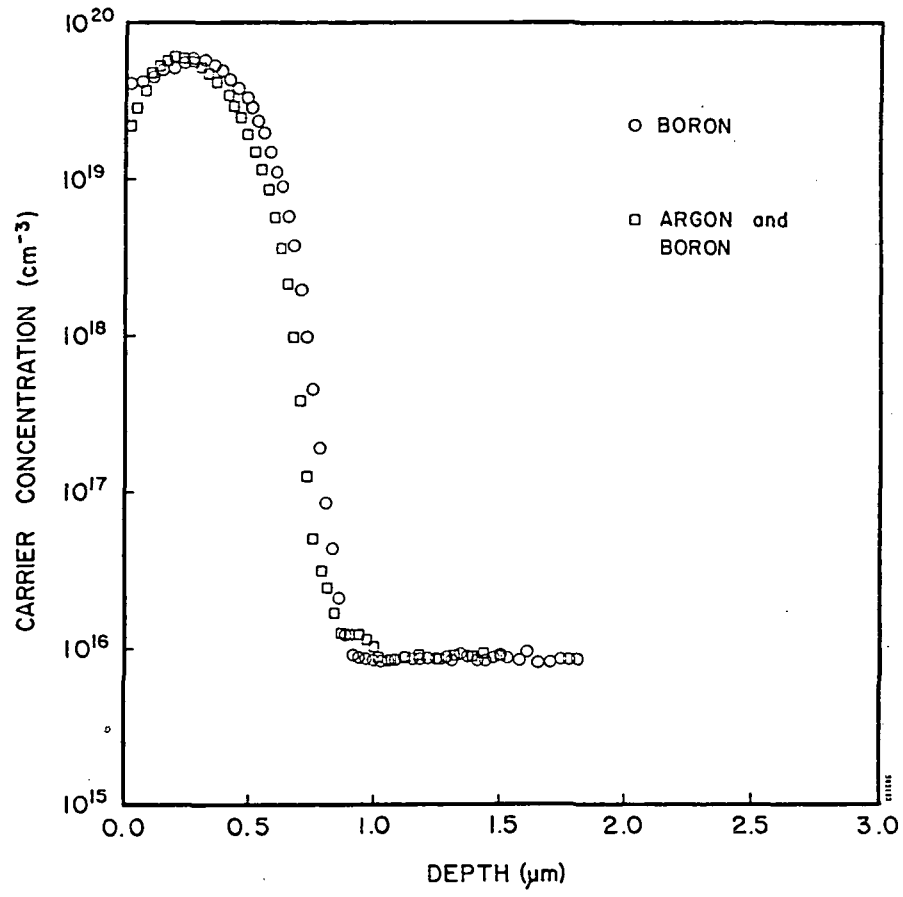


Figure 2-11. Spreading resistance analysis of the implanted back surface

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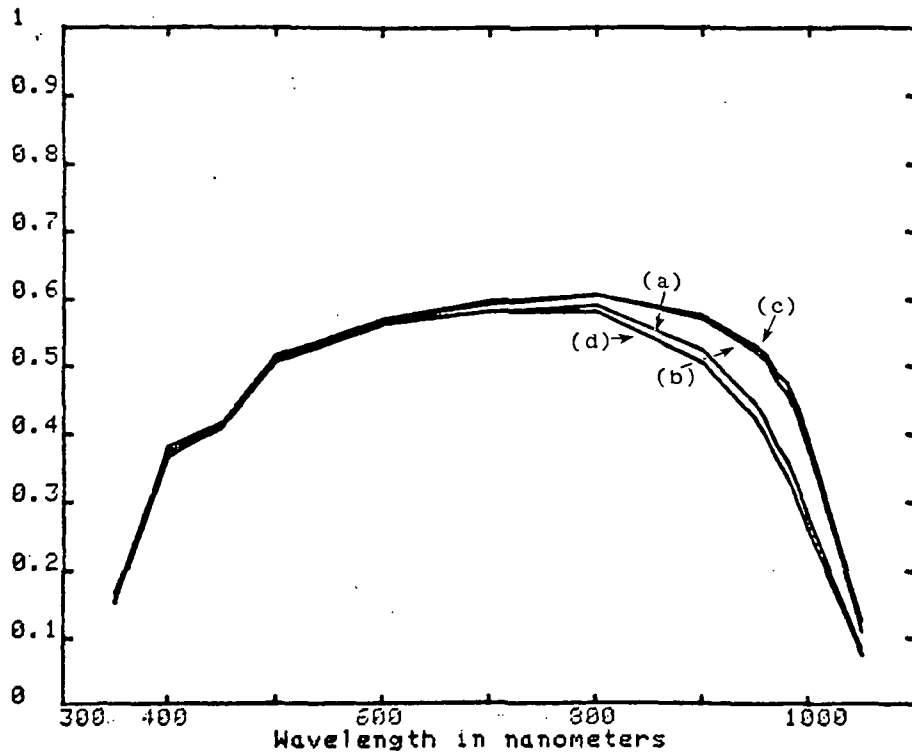


Figure 2-12. External quantum efficiency of cells with back surface implantation: (a) argon cell, (b) argon followed by boron, (c) boron, and (d) none

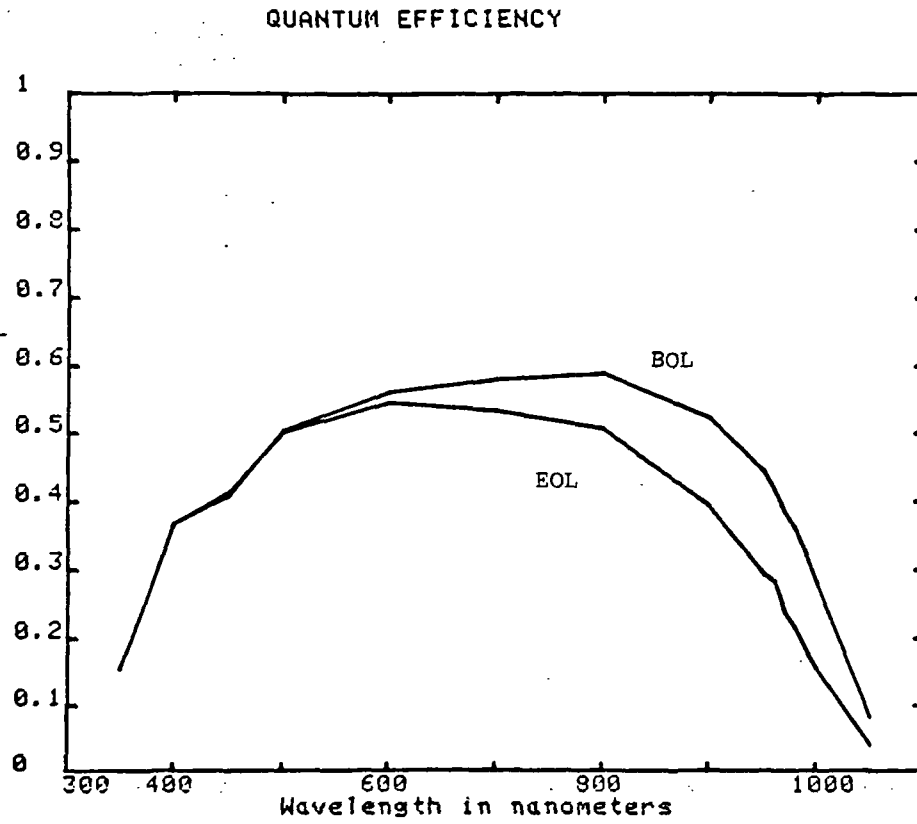


Figure 2-13. External quantum efficiency of AR-implanted cell

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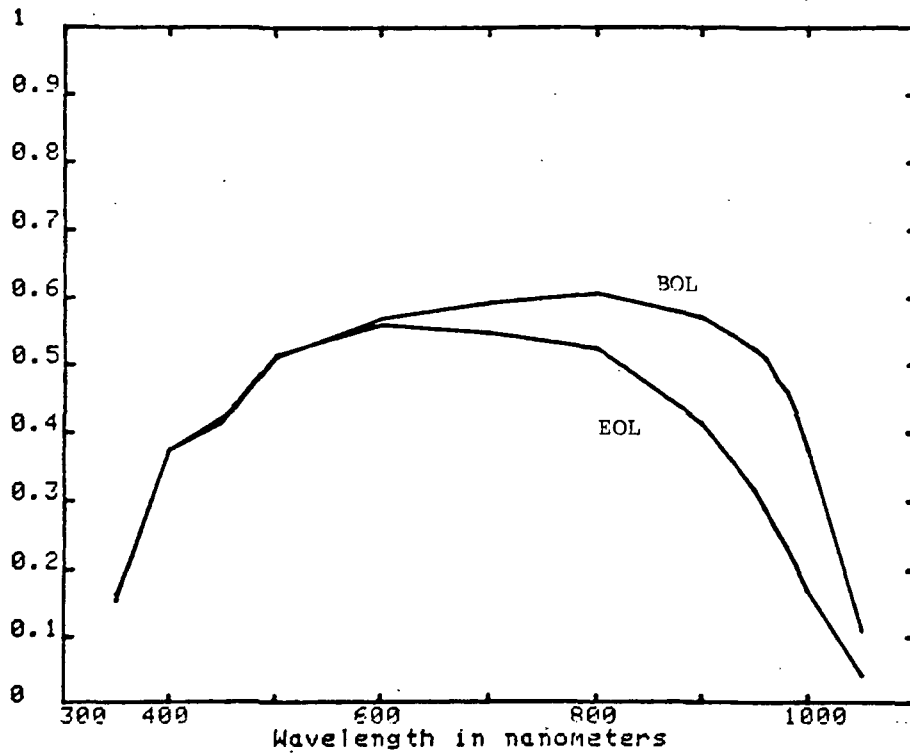


Figure 2-14. External quantum efficiency of cell implanted with argon followed by boron

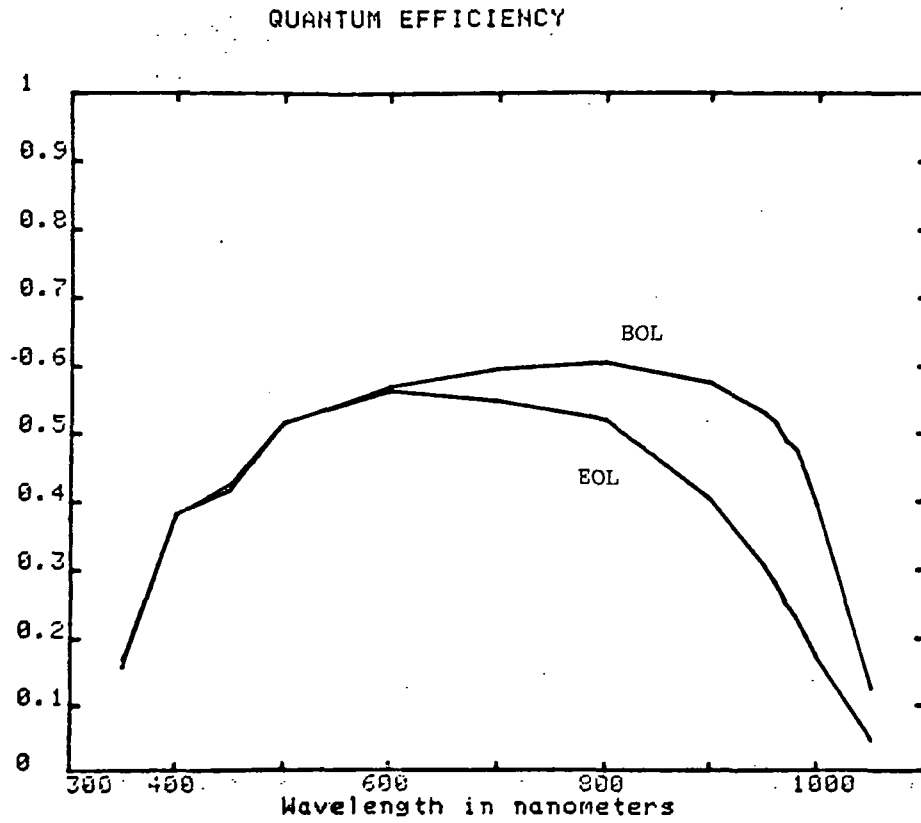


Figure 2-15. External quantum efficiency of a cell implanted with boron

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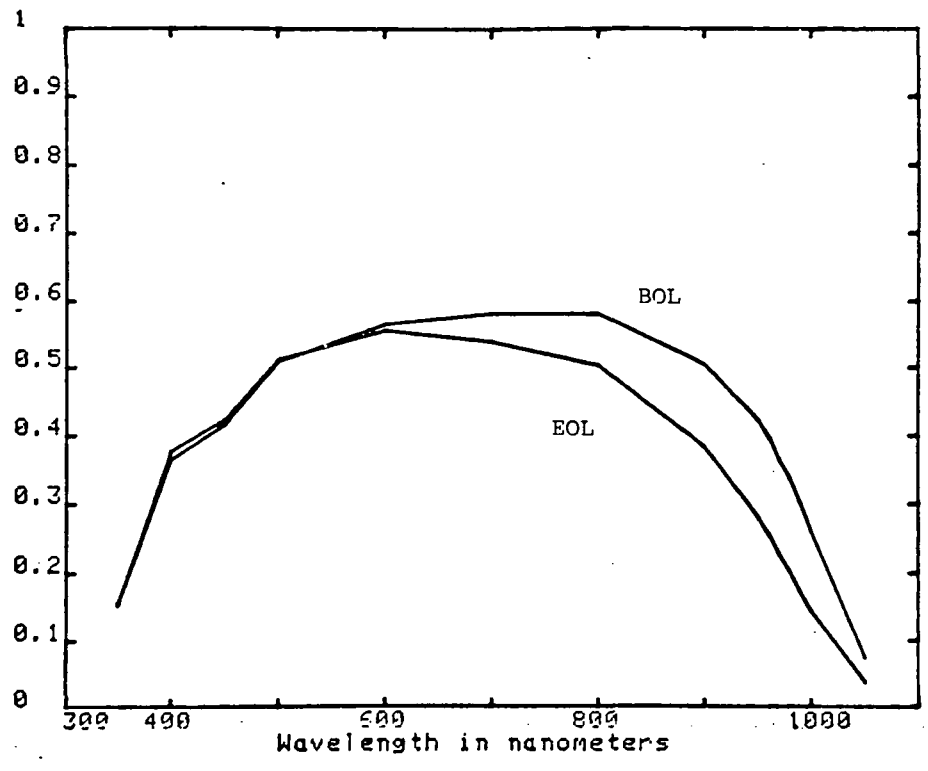


Figure 2-16. External quantum efficiency of a cell without back surface implantation

2.4 BACK SURFACE REFLECTOR

In order to obtain thermal alpha of less than 0.70, we investigated the use of a back surface reflector (BSR).⁽⁷⁾ A particular advantage of the use of ion implantation for BSR formation is that the process leaves the appearance of the back surface unchanged. Thus, BSR formation is quite simple, since no repolishing or other techniques are needed to recover specular reflection.⁽⁸⁾

To evaluate this advantage quantitatively, a BSR was formed on test samples by electron beam evaporation of Al-Ti-Pd-Ag. Starting material consisted of 250 μm Czochralski silicon, polished on both sides. The wafers were divided into four groups, corresponding to the four types of processing shown in Table 2-16. The samples had a TiO_2 AR coating, but no metallization or junction. Table 2-16 also lists the thermal alpha values measured by Henry Curtis of NASA-LeRC. In all cases, this value was less than 0.70. Figure 2-17 shows the reflectance data for two of the samples.

It is important to note that the metallization is deposited over the implanted and annealed surface with no repolishing or other postimplant surface treatment. This results in a significant reduction in process cost.

Table 2-16. Measured Values of Thermal Alpha for Four BSR Processes.

Back Implantation	Metallization	Thermal Alpha
None	Not sintered	0.64 + 0.02
None	Sintered, 400°C	0.66 + 0.02
$^{11}\text{B}^+$	Not sintered	0.67 + 0.02
$^{11}\text{B}^+$	Sintered, 400°C	0.68 + 0.02

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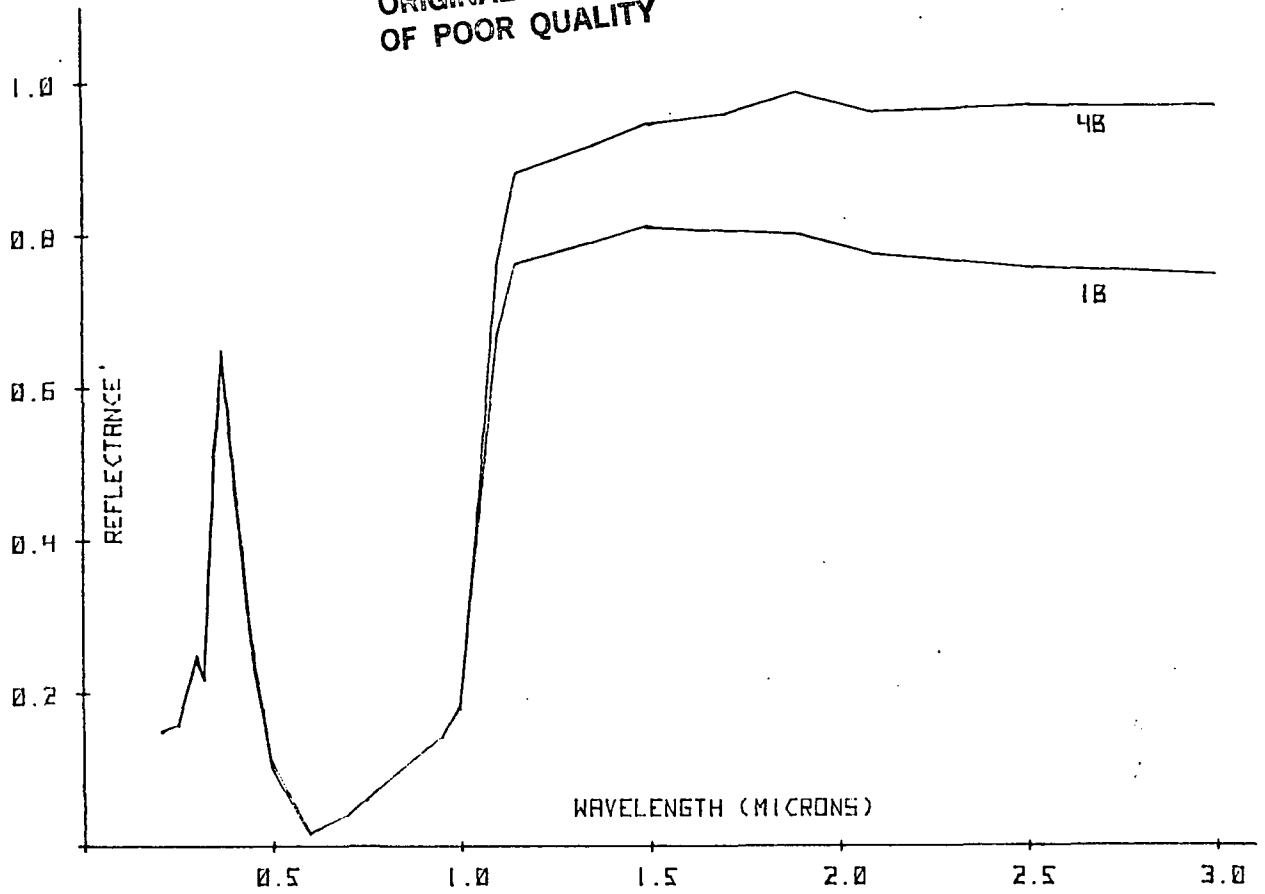


Figure 2-17. Measured reflectance as a function of wavelength for two BSR structures: (1b) boron implantation and sintered BSR contact, (4b) no implantation and no contact sinter of the BSR metallization.

2.5 SUMMARY OF EXPERIMENTS

This section has reviewed the experiments used for solar cell development. For emitter fabrication, best results were obtained with direct phosphorus implantation. Arsenic implantation was found to be promising, but needs further study. For BSF formation, boron implantation was shown to be superior to gallium or aluminum implantation. Separate anneals were used for front and back implants. Although these anneals can probably be combined into a single furnace schedule, this was not investigated explicitly.

Argon implantation was investigated for back surface gettering. No improvement in cell performance or radiation hardness was achieved.

Back metallization consisting of Al-Ti-Pd-Ag was investigated for BSR formation. Excellent results were achieved for evaporated layers on implanted surfaces, without any postimplant polishing.

These results have been combined to form a cell fabrication sequence. This is discussed in Section 4.

SECTION 3 ENCAPSULATION

A major reduction in assembly cost will be achieved by using the new procedure for attaching glass coverslips developed in this program. Standard practice has been to bond a precisely cut coverslip to a finished cell. The demands on cell and glass tolerance and on precision alignment of the coverslip with respect to the cell during assembly add substantially to the assembly cost. To reduce this cost, we have developed a process in which the glass cover is bonded to the wafer before sawing the cell to its final size. In this way, cell and glass are sawed to size as a unit, using a wafer dicing saw. This obviates the need for precision in both coverslip preparation and alignment, without loss of registration, and so results in a major cost saving. We believe that this is the first demonstration of this technology. This section discusses the technique and the results obtained.

3.1 ASSEMBLY CONFIGURATION

The assembly is formed in three process steps. These are (1) weld leads to wafer, (2) laminate wafer and glass, and (3) saw unit to size. In order to saw the unit to size, a contact configuration must be chosen that allows the leads to remain free of the path of the saw.

Figure 3-1 illustrates the contact configuration used in this work. The final cell is square with a connection pad at each corner. Note that the corners of a truly square cell of the size indicated would actually extend beyond the edge of the wafer, since the diagonal of the square is larger than the wafer diameter. The actual corners are therefore rounded and are formed by the edge of the original wafer. This edge is never removed.

If it is desirable to remove all outer edges of the wafer, the rounded corners can be sawed prior to lamination. This might be necessary if the process used for cell fabrication introduces edge shunting. Ion implanted cells, however, do not require edge removal.

3.2 MATERIALS

Two types of glass microsheet were investigated for use as covers: Corning 0211 and Corning 7070. The Corning 0211 glass was nominally 150 μm thick, and the Corning 7070 was nominally 100 μm thick. Best results were obtained with Corning 7070, owing to its coefficient of thermal expansion, which is approximately equal to that of silicon.

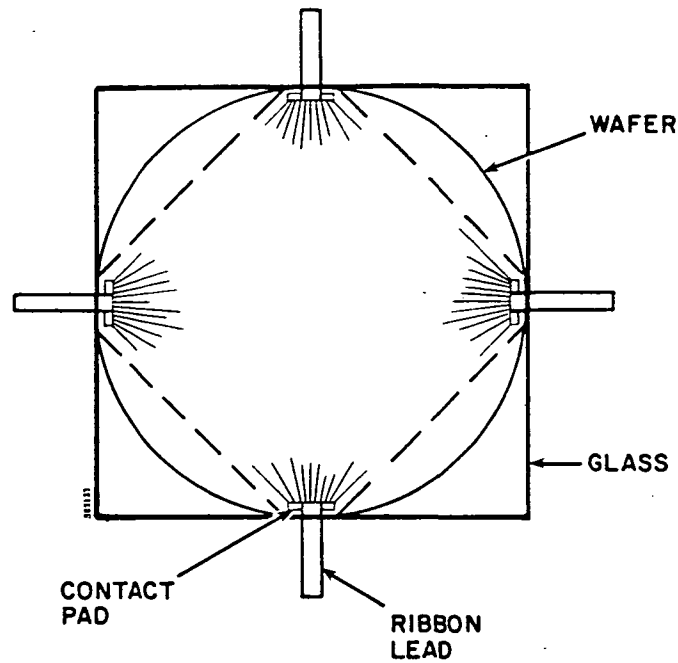


Figure 3-1. Configuration of the assembly consisting of a wafer containing the cell and a coverglass, prior to sawing. The dotted lines indicate the saw cut positions.

Three types of adhesives were investigated: Dow Corning 93-500, ethylene vinyl acetate (EVA), and FEP-Teflon sheet. EVA may be unsuitable for applications in space owing to darkening in ultraviolet radiation environments. The FEP-Teflon was nominally 50 μm thick and the EVA was nominally 250 μm thick.

3.3 STRESS ANALYSIS

The stresses in a three layer laminate composed of glass as the top layer, a relatively soft adhesive as the middle layer, and a silicon solar cell as the bottom layer were calculated. The maximum stress in the top layer of glass is given approximately by the expression

$$\sigma_1 = \frac{E_1 \Delta\alpha \Delta T}{1 + \frac{E_1 t_1}{E_2 t_2}}$$

Here E_1 and E_2 are the effective tensile moduli of the glass and silicon, t_1 and t_2 are the glass and silicon thicknesses, $\Delta\alpha$ is the differential expansion coefficient of the two materials, and ΔT is the total temperature range to which the laminate is exposed.

For the case of Corning 0211 potash soda zinc glass 150 μm thick and a silicon solar cell that is 375 μm thick, the Teflon encapsulation process leads to calculated stresses of

$$\sigma_1 \quad 11,700 \text{ psi tension in the glass,}$$

and $\sigma_2 \quad 4,700 \text{ psi compression in the silicon}$

Since the usual maximum working stress for untempered glass is about 1000 psi, it can be seen that the 0211 glass stress is much too large. The very high stresses occur because 0211 glass has a much larger thermal expansion coefficient than silicon.

Because Corning 7070 glass has an expansion coefficient more closely matched to that of silicon, we chose to use it for large area space cell covers. Calculations were made for 150 μm thick covers of both Corning 7070 and Corning 7740 glass laminated with FEP-Teflon to 250 μm thick silicon solar cells. The results are

- | | | | |
|----------------|------------|---|------------------------------------|
| 1. 7070 covers | σ_1 | = | 564 psi tension in the glass |
| | σ_2 | = | 338 psi compression in the silicon |
| 2. 7740 covers | σ_1 | = | 805 psi tension in the glass |
| | σ_2 | = | 483 psi compression in the silicon |

The cell size and adhesive thickness have a negligible effect on the stresses.

3.4 LAMINATION

Various methods of wafer-to-glass lamination were investigated for each adhesive. The most successful are described below.

3.4.1 FEP-Teflon

The FEP-Teflon lamination sequence consisted of two steps: (1) lay-up of assembly, and (2) temperature/pressure cycle. Figure 3-2 shows the lay-up configuration. The cell, adhesive (FEP-20C), and glass are placed between skived TFE Teflon ($\cong 25 \mu\text{m}$),

adjacent to the cell, and Armalon, adjacent to the glass. This assembly was placed between Kapton (25 μm). The Armalon, Kapton, and skived Teflon serve as release agents.

The assembly was laminated between the parallel graphite platens of Spire's research electrostatic bonder. This bonder allowed us to obtain precise temperature and pressure in a controlled environment. No electrostatic field was used, and precise control of temperature and pressure is not required. The apparatus was used because of the relative ease with which the lamination could be carried out within it.

The temperature/pressure cycle was implemented with the following sequence. The graphite platens were preheated to 290 $^{\circ}\text{C}$. The assembly was then placed on the lower platen. The chamber was pumped out and the platens were pressed so as to apply 45 psi to the assembly. Pressure and temperature were applied for five minutes. The temperature was then reduced to 200 $^{\circ}\text{C}$ while the pressure was maintained. When the temperature reached 200 $^{\circ}\text{C}$, the sample was removed from the apparatus.

It was found that Corning 0211 glass was unsatisfactory for this temperature excursion. The differential thermal expansion created significant residual stress which led to both bowing of the assembly and spontaneous coverglass cracking. This problem was not observed with Corning 7070 covers. Such a result is consistent with the calculations in Section 3.2

3.4.2 Dow Corning 93-500

We achieved excellent results with DC 93-500 adhesive. No lamination equipment was required for this process.

To prepare the wafers for lamination, we first attached blue tape to the cell back. This tape prevented excess adhesive from forming on the back of the cell. Such formations are themselves not a problem, but they degrade the flatness of the back surface and in this way interfere with the vacuum chuck on the wafer dicing saw.

The second step concerns the preparation of the adhesive. The DC 93-500 is mixed and de-aired in a bell jar. The adhesive is then poured onto the wafer surface and de-aired a second time.

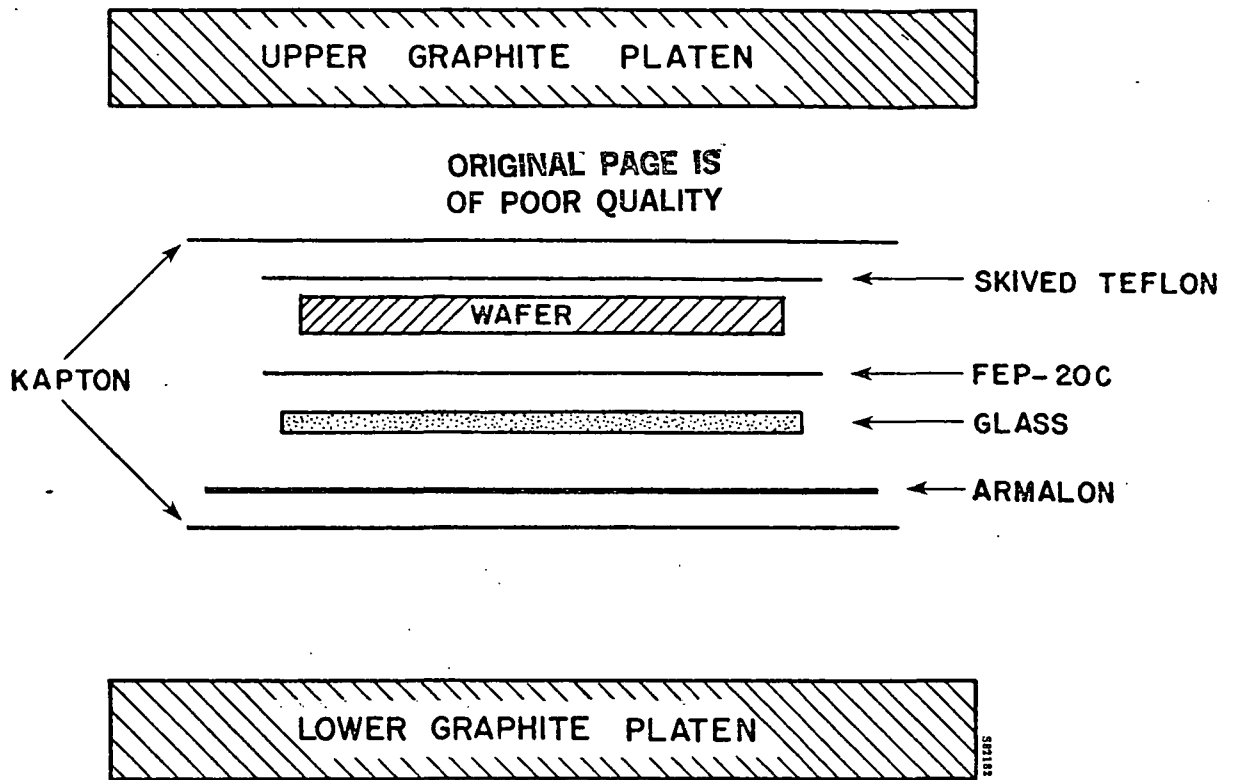


Figure 3-2. FEP-Teflon lay-up configuration

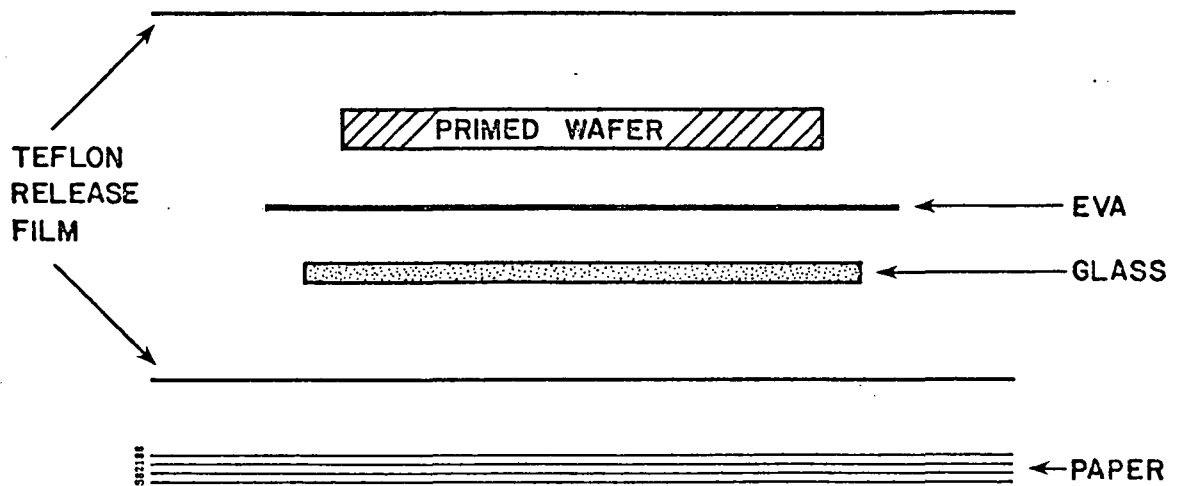


Figure 3-3. EVA lay-up configuration

The coated wafer is placed on a Teflon release film and a cleaned coverglass is applied to the wafer manually. Note that precise alignment procedures are unnecessary. The glass is pressed manually to remove air and to spread the adhesive. The adhesive is then allowed to cure at room temperature for 24 hours.

The fourth and final step is an accelerated cure at 150°C for 15 minutes, after which the DC 93-500 adhesive is fully cured.

3.4.3 EVA

The EVA lamination is straightforward. Both wafer and glass are first coated with GE SS-4179 primer. The EVA sheet is cut into a four inch circle.

FEP Teflon release films are used with the wafer, EVA, and glass, which are assembled as shown in Figure 3-3. The lint free paper was used as a cushion.

The entire assembly is placed in the Spire SPI-LAMINATOR™. The apparatus consists of a vacuum bag and heater assembly for application of pressure and temperature. A pressure of 15 psi and temperature of 140°C are used to form a bond between the cover glass and the wafer.

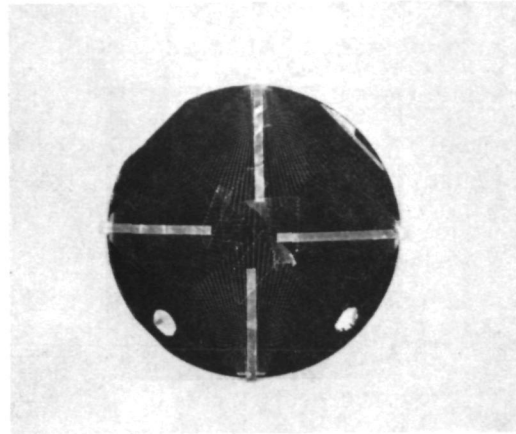
3.5 ASSEMBLY SAWING

After lamination, the assemblies were sawed to size. In order to prevent interconnect destruction, the leads were taped to the front of the assembly. This is shown in Figure 3-4(a). The assembly was then mounted on the vacuum chuck of a Tempres wafer dicing saw and both cell and glass were sawed to size (Figure 3-4(b)).

It was found that wafer bowing interfered with the vacuum chuck on the wafer dicing saw. It is therefore necessary to minimize this bowing. Wafer bowing is absent when DC 93-500 is used with a room temperature curve. Expansion matched glass must be used with processes involving temperature cycling to avoid bowing. If this is not possible, the assembly must be fixed to the saw chuck by some other means. Attaching it to a flat temporary substrate is one possibility. Such variations were not investigated.

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(A)



(B)

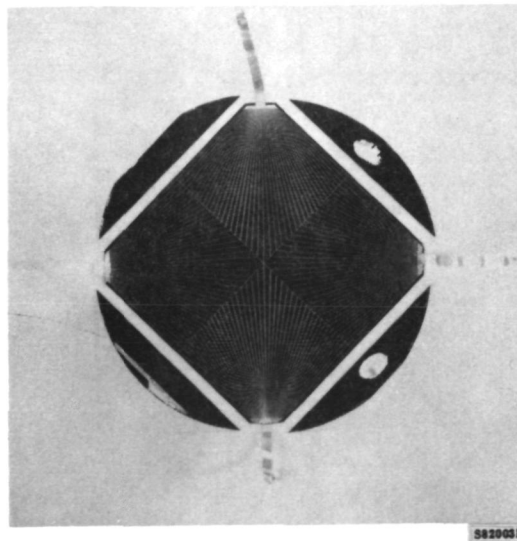


Figure 3-4 Photograph of the solar cell assembly.
(a) Before sawing, with the ribbon leads
folded over the front surface; (b) After
sawing, with the ribbon leads removed from the
front surface.

3.6 TESTING

An experiment was carried out that simulated the lamination sequence developed for DC 93-500. The vehicle for this test was a completed 37.6 cm^2 solar cell. By using a functional pre cut cell, the conversion efficiency could be monitored at each step of the lamination-and-saw sequence. In this way, the effect of each step was determined. To evaluate the actual sawing process, the saw recut the glass and cell as a unit, with a consequent reduction of four percent in cell area.

Table 3-1 lists the cell performance at each step. Figure 3-5 shows the I-V curves from which these data are taken. The data show that there is a small decrease in performance resulting from this type of processing. The DC 93-500 process is conducted at room temperature. Thus, temperature effects, if present in the FEP-Teflon and EVA lamination, would not be detected by this test. It is believed that the small decrease in efficiency results from edge damage caused by the coarse grit saw blade used in this test. Subsequent work with a more suitable blade indicated that this decrease in performance can be avoided.

Laminated nonfunctional assemblies with each type of adhesive were temperature cycled between 77°K and 373°K ten times. No degradation in the lamination was observed.

Functional assemblies were fabricated and the feasibility of each in this application was demonstrated. Table 3-2 lists the best results achieved with each adhesive. Owing to the simplicity of the DC 93-500 lamination, we selected it for deliverable assembly fabrication. It is recommended, however, that future work utilize FEP-Teflon sheet, for it is less costly and its sheet form will be highly desirable for production applications.

Table 3-1. AM0 Performance of Solar Cell at Each Lamination-and-Saw Process Step

Step	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	EFF (%)
1. Bare Cell	584	36.4	77.2	12.1
2. Cell with Ribbon Lead	581	35.6	77.2	11.9
3. Laminated Cell	584	36.4	77.2	12.2
4. Sawcut Cell (Area = 36.0 cm ²)	581	36.4	76.1	11.9

Table 3-2. AM0 Performance of Assemblies

Adhesive	Cover	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	EFF (%)
FEP-Teflon	C7070	591	38.4	77.6	12.8
DC 93-500	C7070	603	39.6	75.1	13.1
EVA	C0211	592	40.1	77.4	13.4

Notes: Area = 34.3 cm², T = 25°C, measured at NASA-LeRC courtesy of R. Hart.

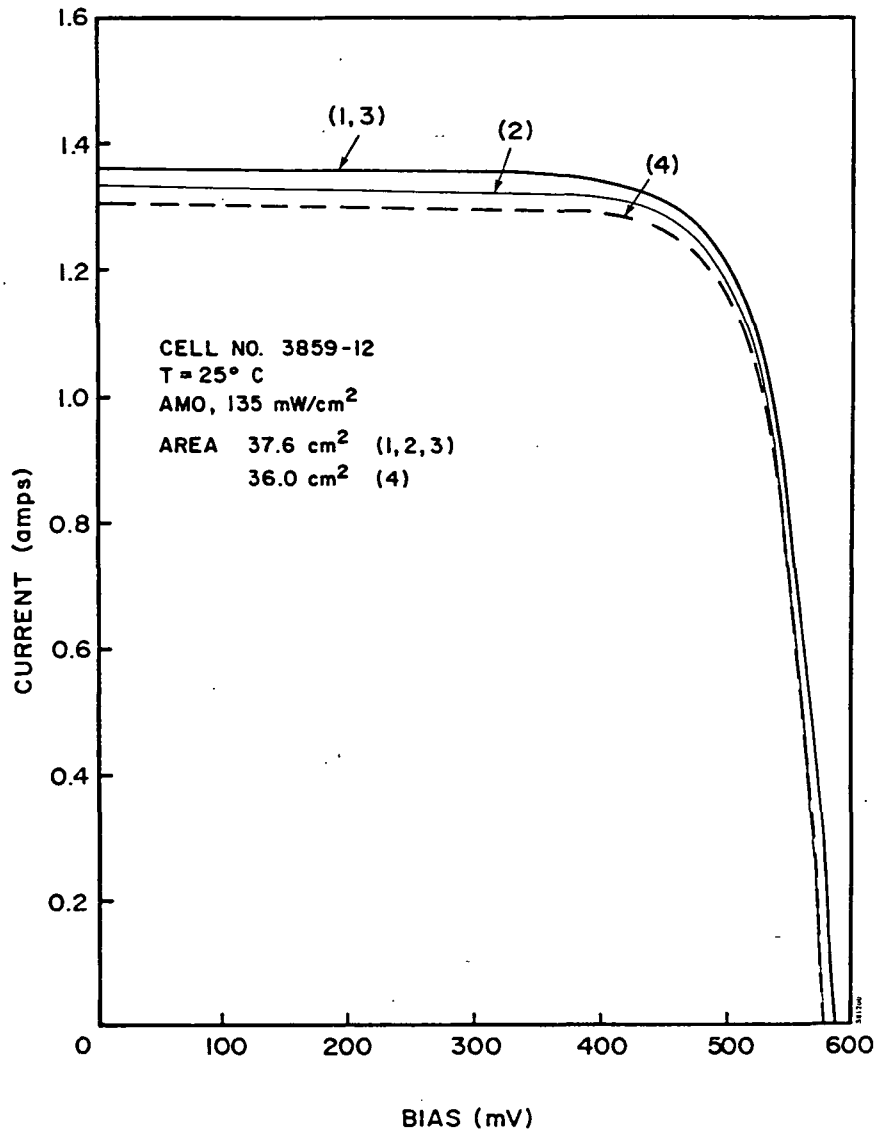


Figure 3-5. I-V characteristics of laminated solar cell.
Curve numbers correspond to process steps shown
in Table 3-1.

SECTION 4 HIGH EFFICIENCY CELLS AND ASSEMBLIES

4.1 CELL FABRICATION

The cell development experiments discussed in Section 2 were used to form a fabrication process sequence. This sequence is outlined in Table 4-1. Starting material consisted of 2 ohm-cm boron-doped float zone (100) silicon obtained from Wacker. The wafers were thinned to 250 μm and chemomechanically polished on both sides.

Implantation consisted of boron for the p^+ BSF and phosphorus for the n^+ junction. A separate anneal was used for the boron to allow it to diffuse to a depth of approximately 1 micron. All anneals were ramped to maintain high minority carrier lifetime. Process parameters are indicated in Table 4-1.

Metallization consisted of full area sintered Al-Ti-Pd-Ag on the back and lift-off patterned sintered Ti-Pd-Ag on the front. The front contacts were plated to a height of approximately ten micrometers. An AR coating of Ta_2O_5 was applied by reactive e-beam evaporation.

The back surfaces of wafers processed in this way exhibited the high degree of specular reflectivity characteristic of polished wafers. Consequently, the thermal alpha of these cells is low. Cell 71-4 has a measured value of $0.66 \pm .02$ (courtesy of Henry Curtis of NASA LeRC).

Twenty-five cells were fabricated and delivered to the NASA Lewis Research Center. These cells were measured under simulated AM0 insolation (courtesy of R. Hart); average performance is given in Table 4-2. Standard deviations are shown in parentheses. The cell area is 34.3 cm^2 . Complete data is listed in Appendix A.

4.2 ASSEMBLY FABRICATION

Experiments on the development of encapsulation procedures indicated that all three adhesives (DC 93-500, FEP-Teflon, and EVA) could be used for the encapsulation process under investigation. Use of FEP-Teflon probably offers the lowest cost. We chose to use DC 93-500 for deliverable assemblies, however, because the process is simple and requires no specialized equipment.

Table 4-1. High Efficiency Silicon Space Cell Process Sequence

1. STARTING MATERIAL
 - Resistivity 2 ohm-cm
 - Growth Float zone
 - Surface (100), polished front and back
 - Thickness 250 micrometer
 - Diameter 3 inches
 2. CLEAN
 3. BACK IMPLANT
 - Ion Species 11B^+
 - Energy 50 keV
 - Dose 5×10^{15} ions/cm²
 4. ANNEAL
 - 550°C - 2 hours
 - Ramp to 950°C, 8°C/minute
 - 950°C - 2 hours
 - Ramp to 500°C 5°C/min
 5. FRONT IMPLANT
 - Ion Species 31P^+
 - Energy 5 keV
 - Dose 2.5×10^{15} ions/cm²
 6. ANNEAL
 - 550°C - 2 hours
 - Ramp to 850°C, 8°C/min
 - 850°C - 15 min.
 - Ramp to 550°C, 5°C/min
 - 550°C - 2 hours
 7. BACK METALLIZATION Electron beam evaporation of Al-Ti-Pd-Ag
 8. SINTER
 9. PHOTOPATTERN FRONT
-

Table 4-1 (Concluded)

10. FRONT METALLIZATION	Electron beam evaporation of Ti-Pd-Ag
11. METAL LIFTOFF	
12. SINTER	
13. PLATE FRONTS	10 micrometers Ag
14. AR COATING	Reactive electron beam evaporation of Ta ₂ O ₅
15. SAW CELL TO FINAL SIZE	
16. TEST	

Table 4-2. Average AM0 Performance of 25 Cells

V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)
608 (002)	40.2 (0.3)	77.6 (1.3)	13.9 (0.3)

Notes: Area = 34.3 cm². T = 25°C, measurement conducted at NASA-LeRC (courtesy of R. Hart).

The performance of the best encapsulated assembly, as measured by R. Hart of NASA-LeRC under AM0 insolation at 25°C is shown below.

V_{oc}	J_{sc}	FF	Eff
603 mV	39.6 mA/cm ²	75.1%	13.1%

The area of this assembly is 34.3 cm². A photograph of a similar assembly is shown in Figure 4-1.

The fabrication process sequence used to fabricate this assembly is shown in Table 4-1, with the simple variation that between steps 13 and 14, welding of the interconnects is inserted, and between steps 14 and 15, lamination is inserted. It can be seen that the encapsulation steps are compatible with the cell fabrication sequence and can be added with a minimal increase in process cost.

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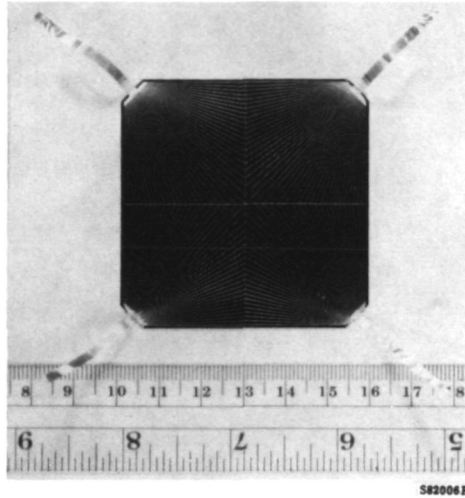


Figure 4-1. Photograph of completed assembly consisting of an ion implanted cell and coverglass sawed to size simultaneously

SECTION 5 COST PROJECTIONS

This section discusses the projected cost of production of the space solar cells developed in this program. This development was based on modifications to Spire's terrestrial cell process sequence. Modifications have been introduced to satisfy the particular requirements of space-quality cells. Low-cost features, however, have been retained. Owing to the general similarity of Spire's space and terrestrial cell processing, cost projections estimated for terrestrial processing, with some modification, can be applied to the projection of cost for space solar cell production.

Under contract to the Jet Propulsion Laboratory⁽⁹⁾ Spire prepared a summary of the Standard Assembly-Line Manufacturing Industry Simulation (SAMIS) estimated price for the Spire Block IV module. This study included the fabrication cost of the ion implanted terrestrial cell. This element of the SAMIS study can be used for a projection of space cell cost. The SAMIS study was based on cost in 1975 dollars. In this report, we use a multiplier (1.5) to convert 1975 dollars to 1981 dollars.

A major assumption in the SAMIS study is that the unused capacity of the production equipment is completely utilized by other types of production. This is justifiable because there is considerable demand for the services of costly machinery (such as an ion implanter). Thus, a profitable service business can insure the complete utilization of the more expensive machines. The cost involved in underutilization of equipment for which there is little demand is neglected. This is believed to introduce little error. For a further discussion of the actual SAMIS study, the reader is referred to Reference 9.

Table 5-1 lists the silicon wafer and wafer polishing cost. This cost is a major driver of the actual cell price. The 1982 costs indicated in the table are the actual prices paid for material used in this program. Conversion to 1975 dollars is made for consistency with the SAMIS study.

Table 5-2 is an excerpt from Table 1 of Reference 9, which lists the cost per watt for each process step in the cell fabrication sequence. These costs have been calculated with SAMIS for 10 kW/year terrestrial production. It is assumed that the resulting module is composed of 152 cells and provides 53 watts. Using this ratio, the cost per watt shown in Table 5-2 can be converted to cost per wafer; this is shown in Table 5-3.

Table 5-1. Assumed Starting Material Cost

	1975 \$	1982 \$
Wafer Cost	2.92	4.38
Thinning and Polishing Cost	4.20	6.30
Total	7.12	10.68

Note: The 1982 cost is Spire's actual direct material cost for cells delivered in this program.

Table 5-2. Cost Per Watt of 10 kW Cell Sequence (1975 dollars)

Process Element	Capital (\$/W)	Labor (Direct)	Mat'l (Direct)	Util (Direct)	Indir*	Value Lost**	Total
Clean	1.37	0.23	0.03	0	2.05	0	3.68
Implant	3.00	1.55	0.46	0.14	3.12	0	8.27
Anneal	0.12	0.14	0	0.04	0.25	0	0.54
Photo	1.53	2.63	0.17	0.01	3.59	0.07	8.00
Evap.	0.95	1.03	0.57	0	1.62	0.25	4.44
Remove	0.56	0.66	0.02	0	1.17	0	2.44
Sinter	0.16	0.19	0	0.07	0.30	0	0.72
Plate	0.58	1.02	0.05	0	1.38	0	3.04
AR	0.21	0.20	0	0	0.30	0	0.71
Saw	0.33	0.58	0	0	0.77	0.72	2.40
Test	0.10	0.14	0	0	0.23	0.76	1.22

* Includes all taxes and miscellaneous.

** Value lost is due to nonunity process yield.

Table 5-3. Cost Per Wafer for Processing 28.7k Wafers Per Year
(1975 dollars)

Process Element	Capital (\$/W)	Labor (Direct)	Mat'l (Direct)	Util (Direct)	Indir*	Value Lost**	Total
Clean	0.48	0.08	0.01	0	.71	0	1.28
Implant	1.05	0.54	0.16	0.05	1.09	0	2.89
Anneal	0.04	0.05	0	.01	0.09	0	0.19
Photo	0.53	0.92	0.06	.01	1.25	.02	2.79
Evap.	0.33	0.36	0.20	0	0.56	.09	1.54
Remove	0.20	0.23	0.01	0	0.41	0	0.85
Sinter	.06	0.07	0	.02	0.10	0	0.25
Plate	.20	0.36	0.02	0	0.48	0	1.06
AR	.07	0.07	0	0	0.10	0	0.24
Saw	.12	0.20	0	0	0.29	0.25	0.86
Test	.03	0.05	0	0	0.08	0.27	0.43

* Includes all taxes and miscellaneous.

** Value lost is due to nonunity process yield.

Table 5-4 lists the costs per wafer for the space cell process sequence developed in this program. Note that the list of process elements has been changed to correspond to the space cell process sequence described in Section 4 of this report.

Implant and Anneal appear twice in Table 5-4 because separate implants and anneals are used for BSF and junction formation in the space cell sequence. In fact, the terrestrial implantation is composed of two sequential implants corresponding to the BSF and junction. These parts are represented in Table 5-2 together as "implant". In Table 5-4, the cost has been split between the two implant elements. The total amount of furnace time used for annealing for the space cell sequence is approximately three times that which is assumed for terrestrial processing. The process cost has therefore been tripled for each anneal process element.

Table 5-4. Cost Per Wafer for Processing Space Solar Cells
28.7k Wafers Per Year (1975 dollars)

Process Element	Capital (\$/W)	Labor (Direct)	Mat'l (Direct)	Util (Direct)	Indir*	Value Lost**	Total
Starting Silicon			7.12				7.12
Clean	0.48	0.08	0.01	0	.71	0	1.28
Implant	0.53	0.27	0.08	0.03	0.55	0	1.46
Anneal	0.12	0.15	0	0.03	0.27	0	0.57
Implant	0.53	0.27	0.08	0.03	0.55	0	1.46
Anneal	0.12	0.15	0	0.03	0.27	0	0.57
Evap.	0.17	0.18	0.10	0	0.28	0.05	0.78
Remove	0.20	0.23	0.01	0	0.41	0	0.85
Sinter	0.06	0.07	0	0.02	0.10	0	0.25
Photo	0.53	0.92	0.06	0.01	1.25	0.02	2.79
Evap	0.17	0.18	0.10	0	0.28	0.05	0.78
Remove	0.20	0.23	0.0	0	0.41	0	0.85
Plate	0.20	0.36	0.02	0	0.48	0	1.06
AR	0.07	0.07	0	0	0.10	0	0.24
Saw	0.12	0.20	0	0	0.29	0.25	0.86
Test	0.03	0.05	0	0	0.08	0.27	0.43
Total	3.53	3.41	7.59	0.15	6.03	0.64	21.41

* Includes all taxes and miscellaneous.

** Value lost is due to nonunity process yield.

The evaporation process element in Table 5-2 consists of front and back evaporations. For the purposes of Table 5-4, the cost is split into two evaporation elements. Note that extra remove and sinter elements have been added to accurately portray the space cell sequence. The remaining process elements are identical.

If one assumes that the final cell has an AM0 efficiency of 14 percent and an area of 34.3 cm², the solar cell cost is projected to be \$32.9 per watt, in 1975 dollars. The production level, which would be 10 kW/year for terrestrial application, is 18.7 kW/year for space application.

In Reference 9, the SAMIS study for 100 kW/year production (287 kwafers/year) is presented. The introduction of automated high throughput equipment is assumed. The cost is consequently lower. Using the method described above, the cost at 187 kW/year can be estimated. In 1982 dollars, this cost is \$30.3 per watt. Table 5-5 summarizes the cost for the two levels of production.

Table 5-5. Cost (dollars per watt) for Two Production Levels.

Level	1975 \$	1982 \$
18.7 kW/year	32.90	49.35
187 kW/year	20.19	30.29

The novel encapsulation process investigated offers a reduction in cost of the completed assembly. The actual amount of this cost reduction cannot be easily estimated. It is clear, however, that the cost must be less than the cost of the conventional approach for the following reasons:

1. The relaxed tolerance on coverglass size reduces the cost of the coverglass material.
2. The relaxed tolerance on cell/cover alignment simplifies the encapsulation process, thereby reducing the amount of labor required.
3. The process introduces no additional costs.

Thus, we conclude that the process offers reduced cost when compared to the conventional encapsulation technique. This reduced cost has not been calculated.

SECTION 6 CONCLUSIONS

This report has described the result of a program to develop a large area space quality solar cell based on low-cost ion implantation processes. The characteristics of the best cell⁽¹⁰⁾ produced in this way are:

Area:	34.3 cm ²
Efficiency:	14.4% AM0
Resistivity:	2 ohm-cm
Thickness:	250 micrometer
Thermal alpha:	0.66

The average AM0 efficiency of the 25 best cells is 13.85 percent; and the standard deviation of this average is less than two percent.

It was found that the best junction was formed by phosphorus implantation and the best BSF was formed by boron implantation. The effect of argon back surface implantation was investigated for lifetime enhancement, but no change in cell performance was observed. It was found that a highly effective BSR could be formed on the boron-implanted back surface without any repolishing or other surface treatment.

A novel encapsulation technique was investigated and found to be feasible. This technique integrates the encapsulation step within the cell formation process, thereby achieving a significant reduction in encapsulation cost. Representative assemblies were fabricated with AM0 efficiency in excess of 13 percent.

Cost projections, based on a SAMIS analysis of terrestrial cell fabrication, were carried out. It was found that 187 kW/year production offers a cost of approximately \$30 per watt.

It is concluded that ion implantation is a process capable of junction and BSF formation in high efficiency silicon space solar cells. Large area cells can be fabricated with this technique, with high cell-to-cell uniformity. As production levels increase, this technology becomes increasingly economical, and therefore, increasingly important.

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10. The best cell was #34-5. The thermal alpha is inferred from a measurement of cell #71-4.

APPENDIX:

AM0 CHARACTERISTICS OF TWENTY-FIVE BEST SOLAR CELLS

REF. CELL A-163 151.9
AREA (CM²) 34.3
TEMP (C) 25
EQ. AIRMASS 0

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CELL	ISC	VOC	IMAX	VMAX	PMAX	FILL	EFF.
34-5							
-1.38443	-0.607	-1.29895	-0.520	675.38	80.3	14.37	
34-6							
-1.39597	-0.609	-1.29461	-0.510	660.46	77.7	14.05	
34-7							
-1.39621	-0.609	-1.28388	-0.511	656.27	77.2	13.97	
34-8							
-1.38841	-0.609	-1.27629	-0.514	656.59	77.7	13.97	
34-14							
-1.38866	-0.607	-1.29084	-0.508	655.67	77.8	13.95	
34-15							
-1.37285	-0.608	-1.28349	-0.508	652.42	78.1	13.88	
34-19							
-1.36986	-0.610	-1.28306	-0.517	663.47	79.5	14.12	
34-21							
-1.36793	-0.609	-1.28373	-0.505	648.71	77.8	13.80	
34-23							
-1.36434	-0.609	-1.26905	-0.512	649.91	78.2	13.83	
34-25							
-1.38091	-0.605	-1.25525	-0.507	636.27	76.1	13.54	
73-1							
-1.36896	-0.604	-1.24499	-0.505	629.21	76.1	13.39	
73-4							
-1.38025	-0.609	-1.27607	-0.507	647.45	77.0	13.78	
73-5							
-1.37608	-0.609	-1.24760	-0.518	646.06	77.1	13.75	
73-8							
-1.37655	-0.609	-1.26736	-0.527	668.43	79.7	14.22	
73-10							
-1.37130	-0.609	-1.25845	-0.510	641.65	76.9	13.65	
73-19							
-1.35835	-0.610	-1.24317	-0.523	650.50	78.5	13.84	
71-4							
-1.38201	-0.612	-1.28421	-0.518	664.60	78.6	14.14	
71-6							
-1.37704	-0.607	-1.28010	-0.510	653.26	78.1	13.90	
71-8							
-1.37068	-0.608	-1.27599	-0.515	657.01	78.8	13.98	
71-10							
-1.38969	-0.608	-1.25751	-0.511	643.07	76.2	13.68	
71-12							
-1.37819	-0.607	-1.26882	-0.508	644.65	77.1	13.72	
71-14							
-1.39357	-0.611	-1.28885	-0.508	655.24	77.0	13.94	
71-18							
-1.38609	-0.608	-1.29368	-0.505	653.18	77.5	13.90	
71-21							
-1.37170	-0.606	-1.22831	-0.502	616.12	74.2	13.11	
71-24							
-1.38475	-0.607	-1.28169	-0.509	652.47	77.6	13.88	

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