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# Optimization of Solar Cells for Air Mass Zero Operation and a Study of Solar Cells at High Temperatures

H. J. Hovel and S. M. Vernon

IBM CORPORATION, Thomas J. Watson Research Center
Yorktown Heights, NY 10598

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# OPTIMIZATION OF SOLAR CELLS FOR AIR MASS ZERO OPERATION

# AND A STUDY OF SOLAR CELLS AT HIGH TEMPERATURES

**Final Report - Phase VI**

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## I. OBJECTIVE

The purpose of this contract is to develop crystal growth procedures, fabrication techniques, and theoretical analyses in order to make GaAlAs-GaAs solar cell structures which exhibit high performance at: 1) Air Mass 0 illumination and 2) high temperature conditions.

## II. INTRODUCTION

The work described in this report is part of an on-going effort over the last six years to optimize the behavior of GaAs solar cells for AMO operation and at high temperatures. The efficiencies of these cells have climbed steadily from the 13-14% value (contact area corrected) reported[1] at the end of Phase I to the 18.5% (uncorrected for contact area) value reported in the middle of the Phase III.[2] The improvement has been brought about by a combination of changes in the liquid phase epitaxial (LPE) growth technique that have resulted in thinner GaAlAs layers, the development of a leaching step to improve the diffusion

length in the starting substrate, and the development of contact metallurgies which obviate the extra Zn diffusion step. In Phase IV, comparisons of contact metallurgies were made, and differences between the etch back epitaxy and saturated melt epitaxy techniques were described. In Phase V the use of metalorganic CVD to produce vapor grown GaAs cells was described along with experiments oriented toward the development of new organic precursors.

For Phase VI of the study, it was decided to explore means of reducing the power to weight ratio of GaAs cells by fabricating devices using low density substrate materials. Substrates such as silicon, glass, or plastics would be desirable, and some work had been done in the laboratory on growing GaAs on Si substrates. These substrates were processed by etching 25 $\mu$m deep grooves with 50 $\mu$m wide spacings into <100> oriented wafers; fine grain polycrystalline GaAs layers 25 - 50 $\mu$m thick were then deposited on these and "recrystallization" was performed - heating the substrates to above GaAs melting point in an $AsH_3$ atmosphere - resulting in large grain regrowth oriented along the groove dimensions. Since this "graphoepitaxy"[3] appeared to be quite promising, it was decided to pursue it further as a technique for producing GaAs solar cells on Si substrates.

## III. GaAs Graphoepitaxy

Silicon was chosen as the substrate material initially because it can be "V-groove" etched by anisotropic etching techniques using an ethylene diamine based process and can then be oxidized thermally to form $SiO_2$, making the growing surface similar to glass. It was conjectured that the GaAs nucleation would begin at the pointed bottom of the groove where all the nuclei have a tendency to be aligned, resulting in as-grown, large grain, oriented films.

When GaAs was deposited on these oxidized, grooved substrates using the MO-CVD process, however, large oriented grains were not obtained under any combination of temperature and growth rate (650-850°C and 0.02 - 1.3 $\mu$m/minute). The films were small grained and unoriented as determined by x-ray analysis. An optical micrograph of such a film is shown in

Figure 1. However, the use of the simple thermal recrystallization step, rapidly heating the film in hydrogen and arsine to above its melting point (1238°C), resulted in GaAs films containing large, flat grains running along the grooves, as is shown in Figure 2. These grains were often as long as 500 $\mu$m. X-ray analysis determined that these recrystallized films were highly oriented in the same direction as the silicon surface with the <100> GaAs x-ray peak being approximately two orders of magnitude larger than that of any other crystal orientation in the film. A problem that arose, however, was that while the grooves were filled with recrystallized GaAs, the flat regions between the grooves most often were left bare. In a few isolated cases, however, the GaAs appeared to form a large crystal which reached from one groove, across the flat, to the adjacent one. It became necessary to make grooved Si substrates with much smaller spacing, to enable the use of smaller GaAs layer thicknesses and to enhance the probability that the recrystallized layer would be continuous across the surface.

To calculate the threshold for continuous GaAs layers over a large groove field, it is necessary to know the groove geometry, the groove depth and spacing, and the initial GaAs layer thickness. Potential continuity of the GaAs layer will be determined by the volume of GaAs available compared to the volume of the grains and the surface tension and wetting properties of molten GaAs relative to the surface it touches. Figure 3 shows a cross section of an as-grown layer of thickness D on a substrate containing a groove field whose grooves are S wide separated by flats F wide. The grooves are H deep and are shown as triangular but in general may have any shape; in particular, plasma etched gooves would have a more rectangular cross section.

The volume of GaAs contained in the unit field is:

$$V_{GaAs} = D(S + F) \qquad (1)$$

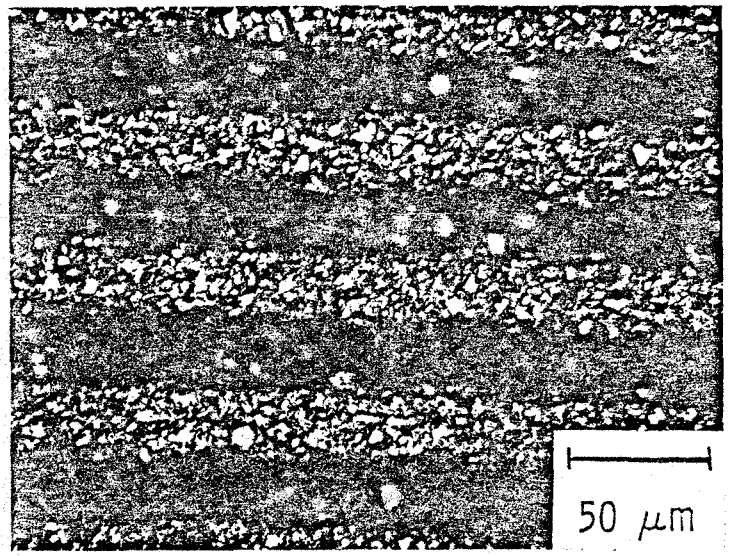
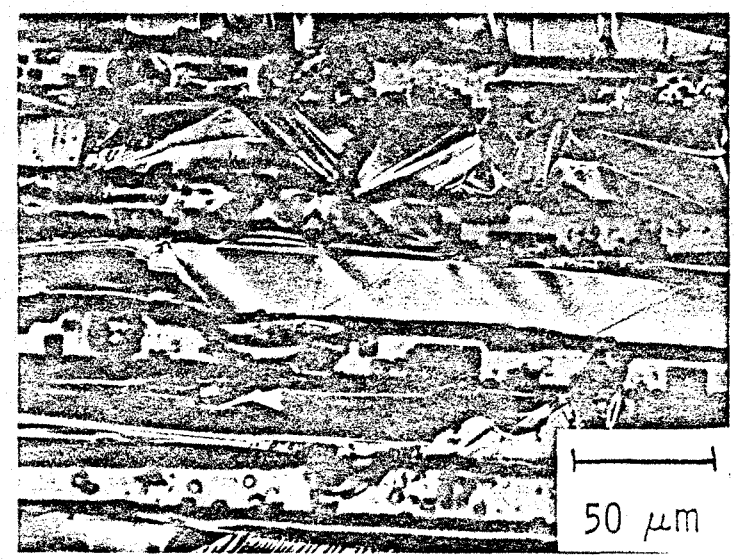



Figure 1. Optical Micrograph of As-Grown GaAs Film.

Figure 2. Optical Micrograph of Recrystallized GaAs Film.



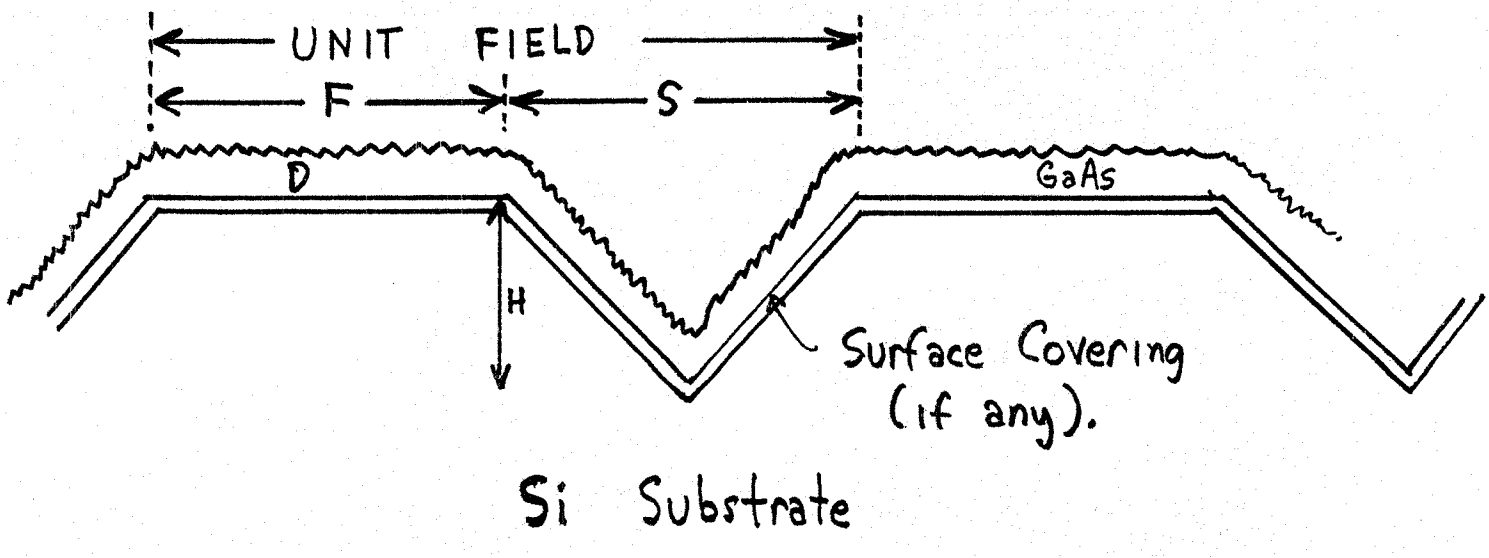



Figure 3. Cross-section of GaAs-covered Si substrate containing groove fields. Initial conditions.

regardless of the shape of the groove, assuming the surface mobility of incoming GaAs atoms is not sufficient to cause preferential growth in the groove, but even if preferential growth does take place, equation (1) correctly describes the deposited volume of GaAs where D is the thickness that would have deposited on a flat substrate. (This would no longer be true if the presence of the grooves alters the basic growth rate.) The threshold for continuity is obtained when this volume of GaAs (normalized for unit length) multiplied by its density $d_1$ just exceeds the volume of the groove multiplied by the GaAs layer density $d_2$ after recrystallization:

$$D(S + F)d_1 > V_{Groove}d_2 \tag{2}$$

resulting in

$$D > \frac{V_{Groove}}{(S+F)} \frac{d_2}{d_1}. \tag{3}$$

For example, if the groove is triangular, its normalized volume is given by

$$V_{Groove}(\text{triangle}) = \frac{1}{2} SH \tag{4}$$

and the threshold becomes

$$D_{(\text{triangle})} > \frac{1}{2} \frac{SH}{(S+F)} \frac{d_2}{d_1}. \tag{5}$$

The preferential etching tends to produce a triangular shaped groove whose depth H is about

half the spacing S. For this special case

$$D_{triangle} > \frac{1}{4} \frac{S^2}{(S+F)} \frac{d_2}{d_1} \tag{6}$$

As an example, if the groove width and spacing are equal, the threshold thickness would be D = (1/8) S x (density ratio). Of course, this would result in all the GaAs located in the groove with, say a monolayer located on the flat, so one would wish to grow the GaAs several times this thickness to ensure a finished layer to usable thickness over the entire field. The densities in the initial and final states could also be significantly different since the initial layer normally consists of random nuclei.

The relationship between the initial and final conditions can be determined from Figures 3 and 4. Again, letting the volume of the groove be $V_{groove}$, the thickness T after recrystallization is given by:

$$D(S + F)d_1 = (V_{groove} + (F + S)T)d_2 \tag{7}$$

$$T = \frac{d_1}{d_2} D - \frac{V_{groove}}{(F+S)}. \tag{8}$$

Using the example once more of a triangular groove whose depth is one half its base, this becomes:

$$T = \frac{d_1}{d_2} D - \frac{1}{4} \frac{S^2}{(F+S)} \text{ (Triangular)} \tag{9}$$

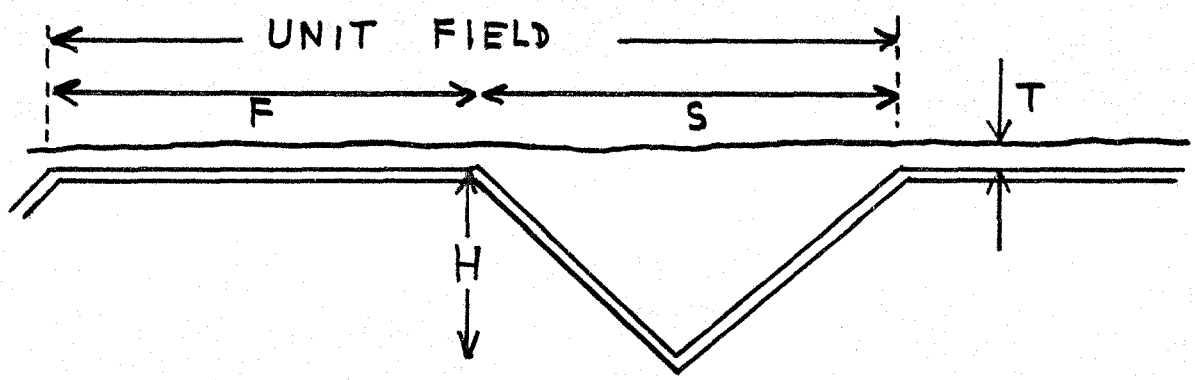



Figure 4. Cross-section of a GaAs/Si structure after recrystallization.

and if the spacing and width are equal,

$$T = \frac{d_1}{d_2}D - \frac{1}{8}S \quad \text{(Triangular, S = F).} \tag{10}$$

This implies that for triangular grooves, the initial layer thickness D can be considerably less than the groove width S and a continuous layer of thickness T might still be obtained.

It is important to remember that these relationships only establish the minimum requirements between layer thickness and groove characteristics. Considerations such as surface tension and wetting between molten GaAs and Si, or GaAs and surface layers such as $SiO_2$ covering the Si, can have a big effect on the tendency of the molten layer to remain continuous across the entire wafer.

In order to work with thin GaAs layers, a photolithographic mask was needed which contained much smaller groove dimensions than the first mask. An ideal mask was found for the growth experiments in that it contained a series of 14 groove spacings and widths in a relatively small area. Using this mask, it would be possible to grow a single GaAs layer and see the effect of the layer thickness/groove dimensions ratio ranging from D (layer thickness) larger than the groove depth and spacing to D smaller than this spacing.

The top view of this groove mask is shown in Figure 5. The mask consists of a number of boxes which are 2 mm x 2.6 mm in size, and each box contains 14 groove fields which are 150 $\mu$m wide by 2.6 mm long. Each groove field is spaced about 30 $\mu$m from the next. Figure 6 is an optical micrograph of a section of one of the boxes showing 4 of the groove fields (the smallest field of grooves, with 3-4 $\mu$m spacings, did not etch properly). Figure 7 shows the 14 groove fields and their dimensions. Figure 8 shows a scanning electron microscope picture of a cross section of a groove pattern with 5 $\mu$m wide grooves on 10 $\mu$m centers. The grooves are made by oxidizing the <100> oriented wafers, producing a photoresist pattern with the

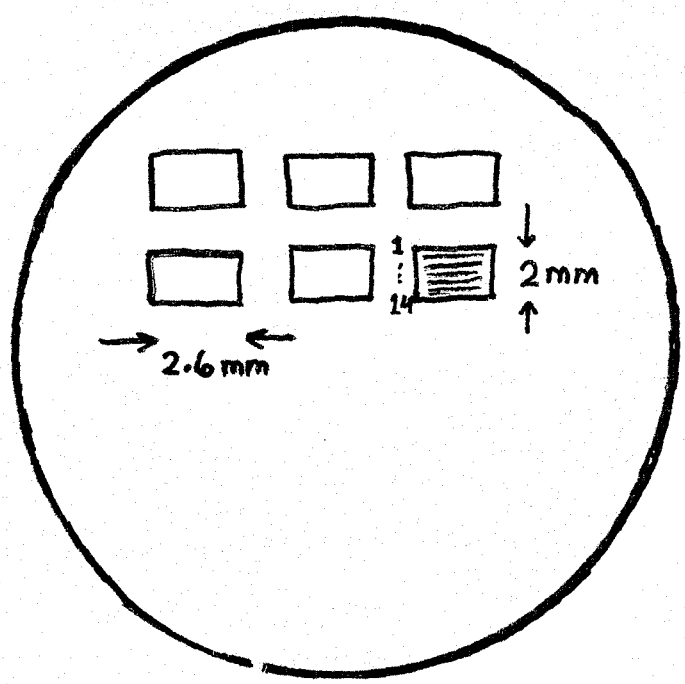



Figure 5. Outline of the new mask showing boxes of groove fields.

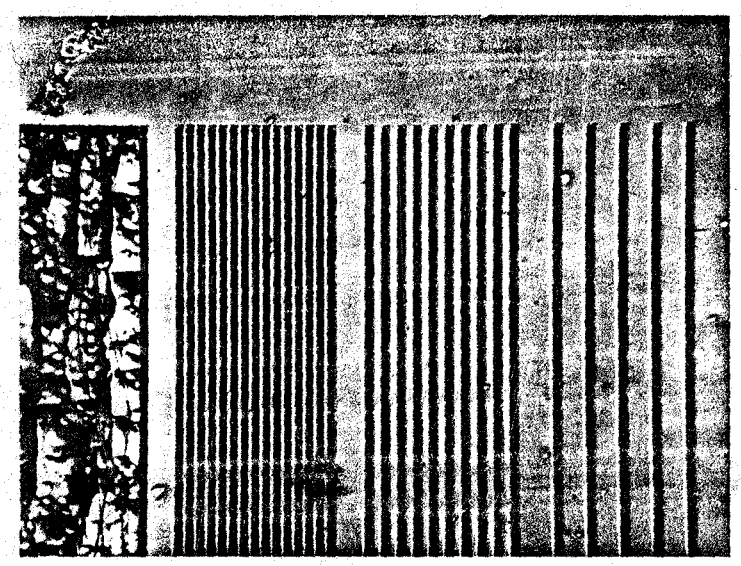


Figure 6. A section of a box showing several groove fields.

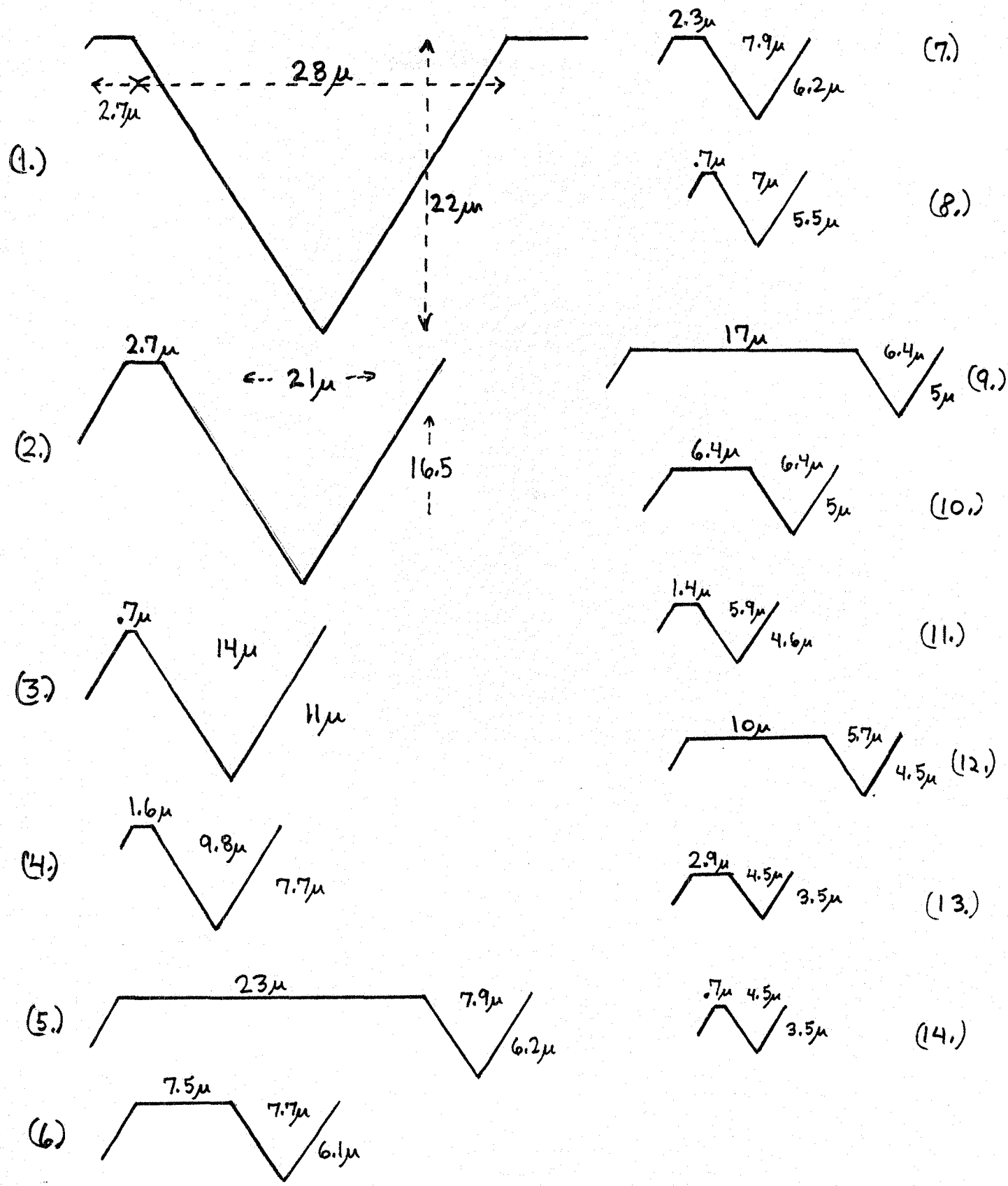



Figure 7. An outline of the groove fields contained in each box.

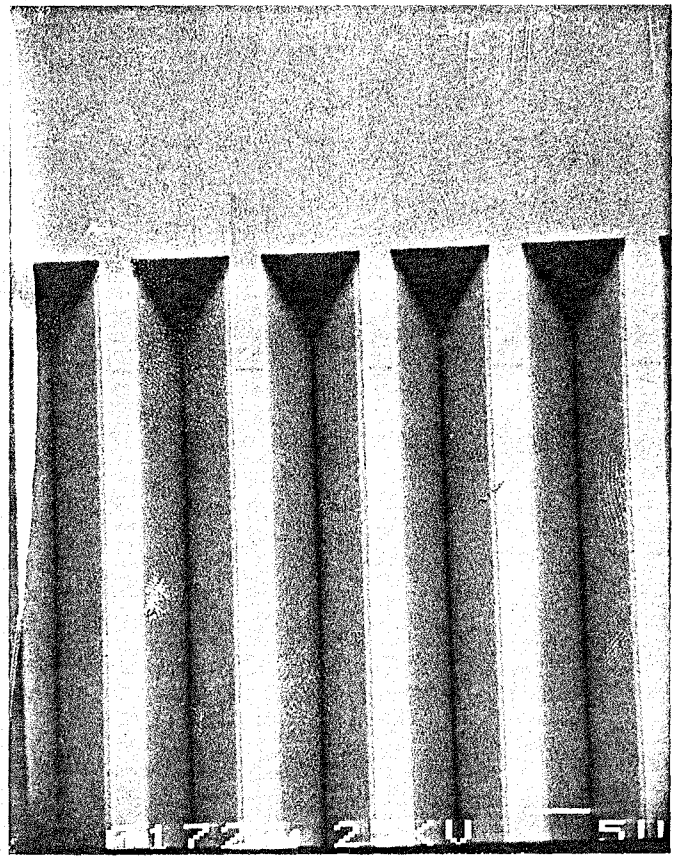


Figure 8 Scanning electron micrograph of a groove field of 5 $\mu$m grooves on 10 $\mu$m centers.

long dimension aligned parallel to the <110> axis, etching grooves in the oxide with HF acid, then etching the Si in ethylene di-amine pyrachatacol. This is a preferential etch which produces triangular grooves whose faces are <111> planes.

Under normal growth conditions which result in single crystal GaAs films on GaAs substrates, only randomly oriented polycrystalline GaAs is formed on the Si surface, as shown in Figure 9. The same GaAs structure is obtained whether the growth is carried out on bare Si, thermally oxidized Si, or $TiO_2$ - covered silicon. (Strangely enough, the GaAs does not nucleate on flat regions of CVD-deposited $SiO_2$ on silicon.) The results are vastly different after recrystallization, however, for the different surface coverings. On bare Si, the GaAs forms an alloy with the Si and usually ends up in isolated patches centered around the grooves, as shown in Figure 10, where the light patches are the GaAs-Si alloy and all the rest is silicon. Figure 11 shows another groove field of 30 $\mu$m spacing where a 10 $\mu$m GaAs film was grown on a wafer with just room-temperature oxide. Here the GaAs has filled in the gooves completely, resulting in an alternate Si-GaAs-Si surface structure. Figure 12 shows the Si k-alpha radiation of this surface; the white dots show where the Si surface is exposed and the dark regions are GaAs.

Regions of thermally oxidized or $TiO_2$-covered Si with groove spacings less than the GaAs layer thickness resulted in continuous large grains covering the entire groove field. Figure 13 shows several groove fields and the resulting recrystallized GaAs layer. The middle pattern consisted of grooves whose depth was approximately equal to the layer thickness but whose spacing was 3 times this depth. GaAs has filled in these grooves but the GaAs is not continuous from one groove to the next. To the right of this is a groove field with smaller groove spacing, resulting in a continuous GaAs grain covering the entire field. The GaAs grain is essentially grown from a molten phase at the end of the recrystallization step and results in a heavily twinned grain which is other wise remarkably free of surface features. Figure 14 shows the k-alpha radiation from this sample. Figure 15 shows a larger view of the water and

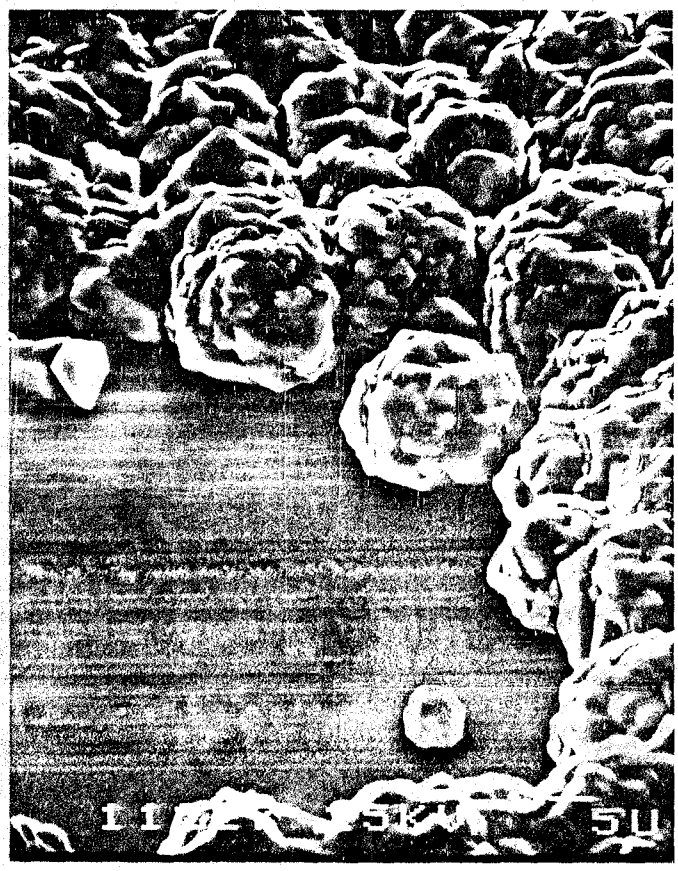


Figure 9. GaAs film grown on $SiO_2$ covered Si wafer.

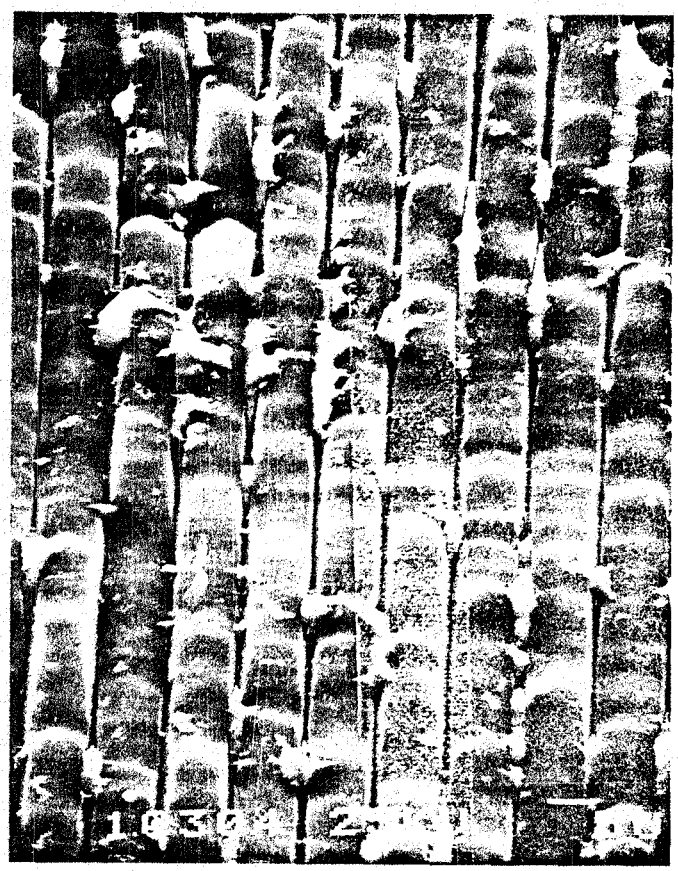


Figure 10. Surface of a recrystallized GaAs layer showing alloy patches between Si flats.

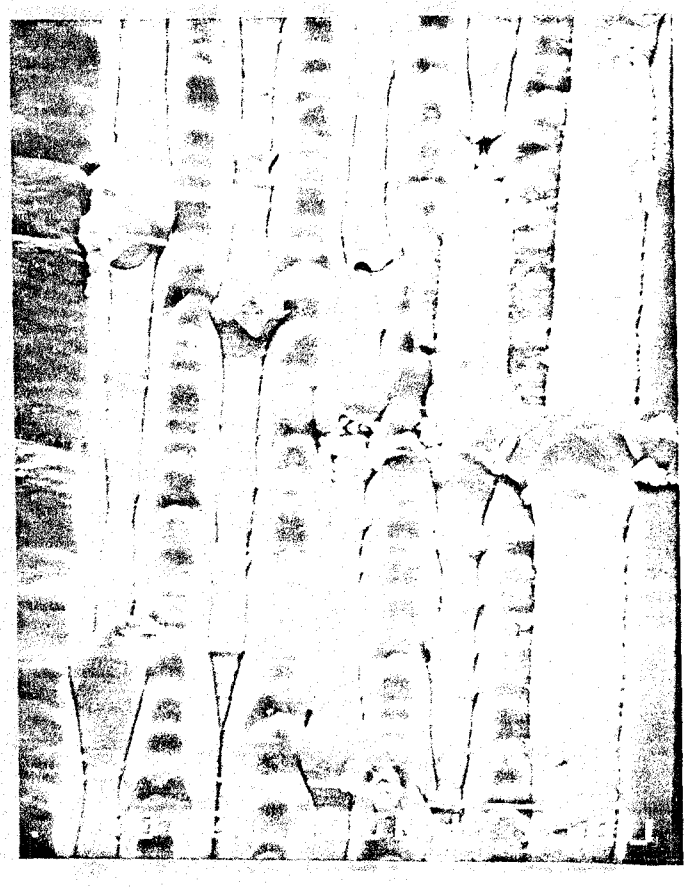


Figure 11. Surface of a recrystallized GaAs layer on Si showing GaAs contained in the grooves separated by Si flats.

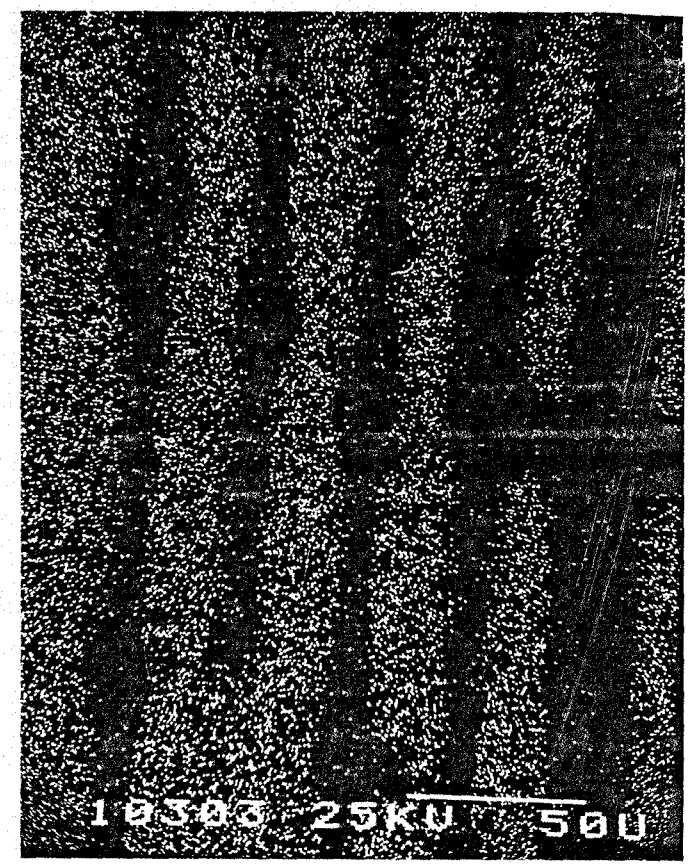



Figure 12. Silicon k-alpha radiation from the sample of Figure 11.

Figure 13. Surface of a recrystallized GaAs film on several groove fields of oxidized silicon

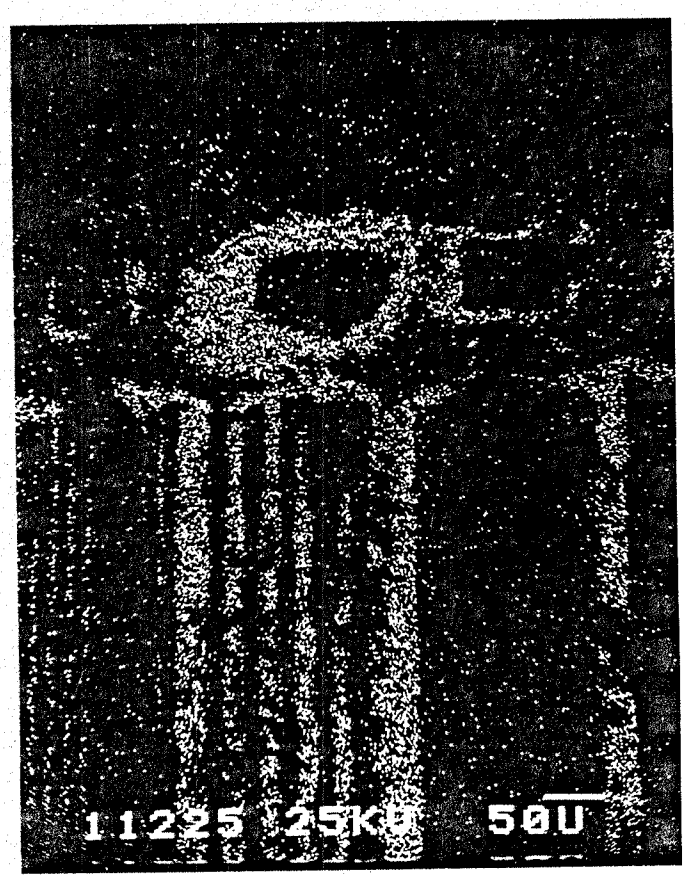


Figure 14. Silicon k-alpha radiation for the sample shown in Figure 13.

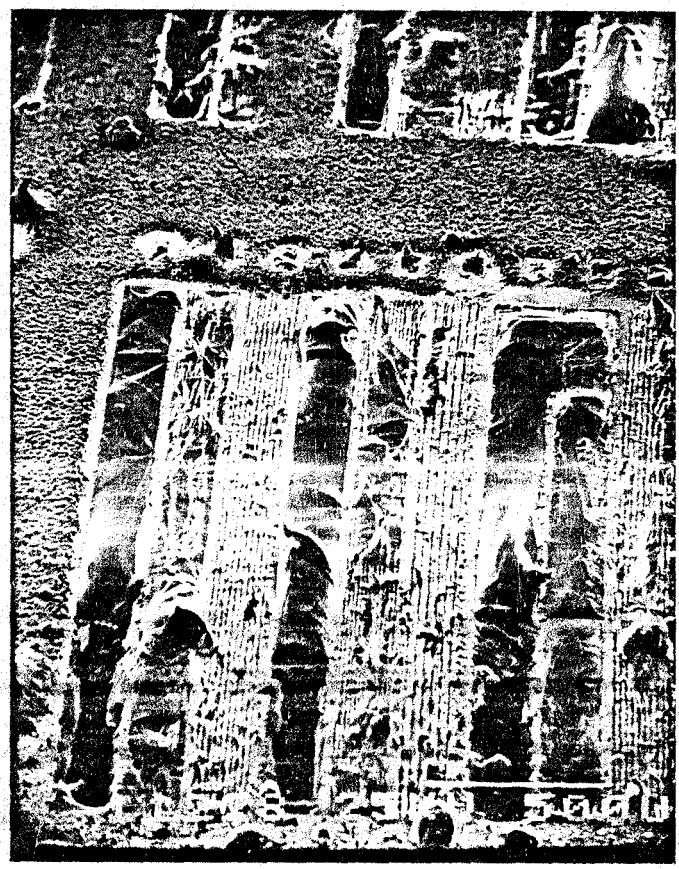


Figure 15. Larger view of the wafer showing several groove fields and continuous GaAs grains.

shows 9 groove fields of various dimensions. In four of these patterns a single grain covers the entire field and in one case the grain has started to carry across two fields.

In order to electrically characterize the recrystallized GaAs graphoepitaxial layers, larger areas were needed than the 50 $\mu$m x 1 mm patters produced by this mask. For this reason, a new large area mask having 5 $\mu$m lines on 10 $\mu$m centers was made for use in 2 1/4 inch diameter Si wafers. The wafers are <100> Si and the mask is aligned on a <110> direction. As a first step, the photolithography was perfected on bare Si until the line width could be reproducibly controlled. However, the anisotropic etch used to make the V-grooves requires $SiO_2$ as an etching mask. When the photolithography was attempted on oxidized Si wafers, problems of adhesion and uniformity resulted. These problem are typical when processing photolithographic structures with dimensions less than 7 or 8 microns. Eventually, wafers were processed to the necessary specifications both by ourselves and by members of the "Silicon Line" at IBM Thomas J. Watson Research Center. The pattern opened in the oxide is shown in Figure 16.

**1. Square Grooves**

The bare Si samples with the large area fine line pattern were plasma etched to obtained square-shaped grooves. This was to check whether or not the groove shape was influential in the GaAs recyrstallization process. Figure 17 shows the cross section of these grooves and 18 shows the rough bottom surface. These samples were tested for usefulness in the graphoepitaxy process by subjecting them to the procedures that had been successful previously on the V-grooved samples. One experiment consisted of growing GaAs on these Si samples which were covered with their natural native oxide formed at room temperature. Attempts at recrystallization resulted in most of the GaAs balling up into a few mounds, while the rest of the surface was left as bare Si with only small isolated spots of GaAs remaining. Also, the GaAs apparently alloyed enough with the Si to cause the square grooves to become quite round (Figure 19). Other samples of this square-grooved Si were coated with $TiO_2$ grown at

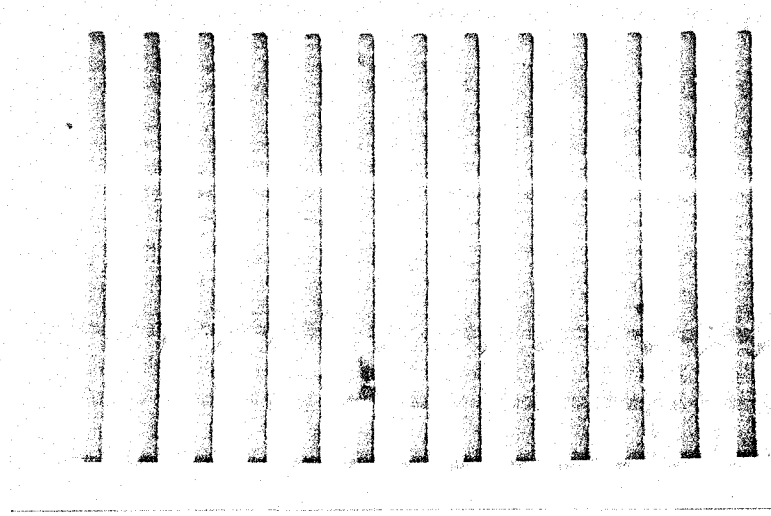


Figure 16. Photolithography pattern in oxide on Si wafer. Darker areas are openings. 700X.

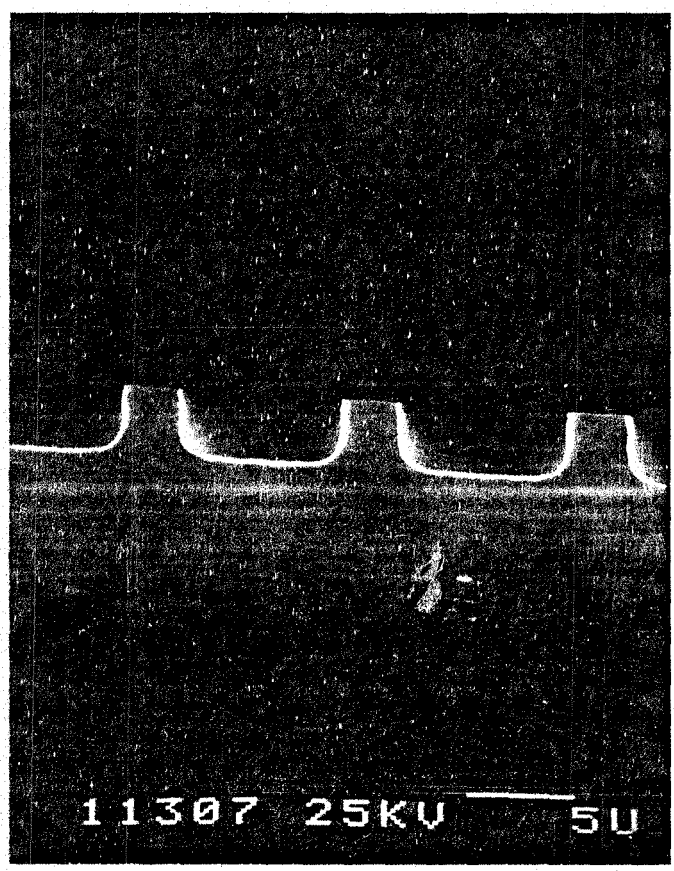



Figure 17. Cross-section of plasma etch grooves.

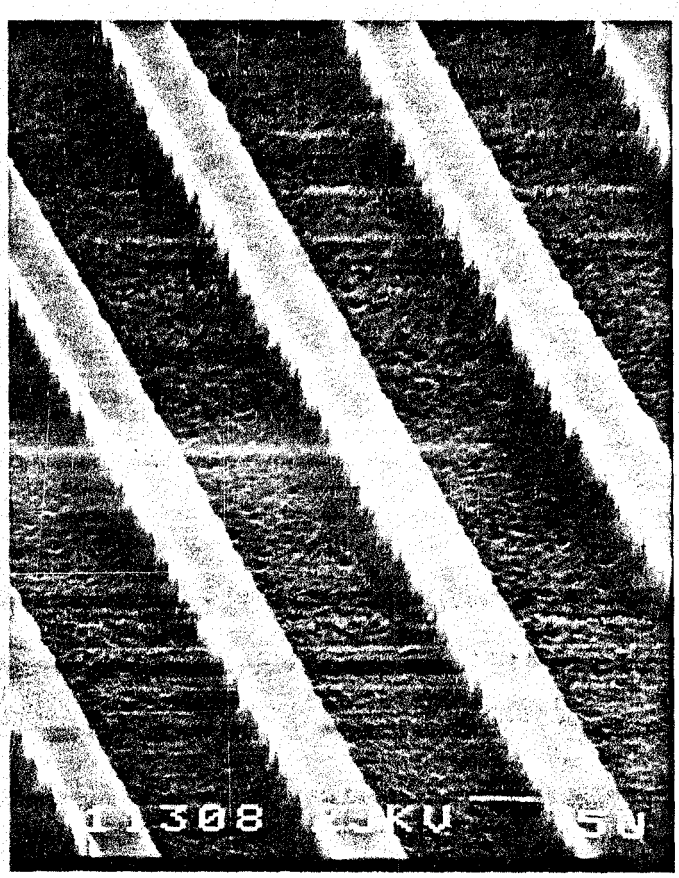



Figure 18. Rough surface of plasma etched grooves.


Figure 19. GaAs clumps in plasma etched grooves which have become rounded.

400°C to a thickness of 1000 Å . GaAs layers were then grown on these substrates. After the recrystallization step, the surface of the samples looked quite rough, with a brownish color; also, most of the GaAs appeared to have balled up into a few large mounds. Analysis in the SEM showed that the brown, rough-looking layer was a Ga-As-Ti compound. This surface is shown in Figure 20. The darker areas are the grooves, which contain less Ti than the lighter stripes between the grooves.

**2. V-Grooves**

The oxidized Si wafers containing the pattern shown in Figure 16 were used to make large area V-grooved substrates by etching with an anisotropic etch rather than plasma etching to produce square grooves. This etch is the normal ethylene diamine pyrocatechol used previously. The etching was done at 115°C, which gives an etch rate of ~ 50 $\mu$m/hr in the <100> direction and ~ 3 $\mu$m/hr in the <111> direction, thus forming grooves with walls that are <111> planes (Figure 21). After the anisotropic etch, the oxide was stripped off, and then the samples were coated with dielectric thin films by three different methods before receiving the GaAs deposition. The samples which received a 1000 Å coating of $TiO_2$ grown at (500-550°C) showed some balling up of the GaAs after recrystallization, but most of the grooves retained enough GaAs to nearly "fill them in". The flat spaces between the grooves were partly covered with GaAs and partly bare; the GaAs does not contain large amounts of Ti in this case, which might be due to the increased temperature at which the $TiO_2$ was deposited. Figure 22 shows one of these samples.

Another sample which had 500 Å of native $SiO_2$ grown at 1000°C in $O_2$ before GaAs deposition was recrystallized also. Most of the surface was left bare with only small GaAs deposits remaining in spots along the groove bottoms (Fig. 23). The GaAs, for the most part, balled up in many small mounds scattered over the surface. However, on one area of the sample the process seemed to work exactly as desired and resulted in a region of GaAs which

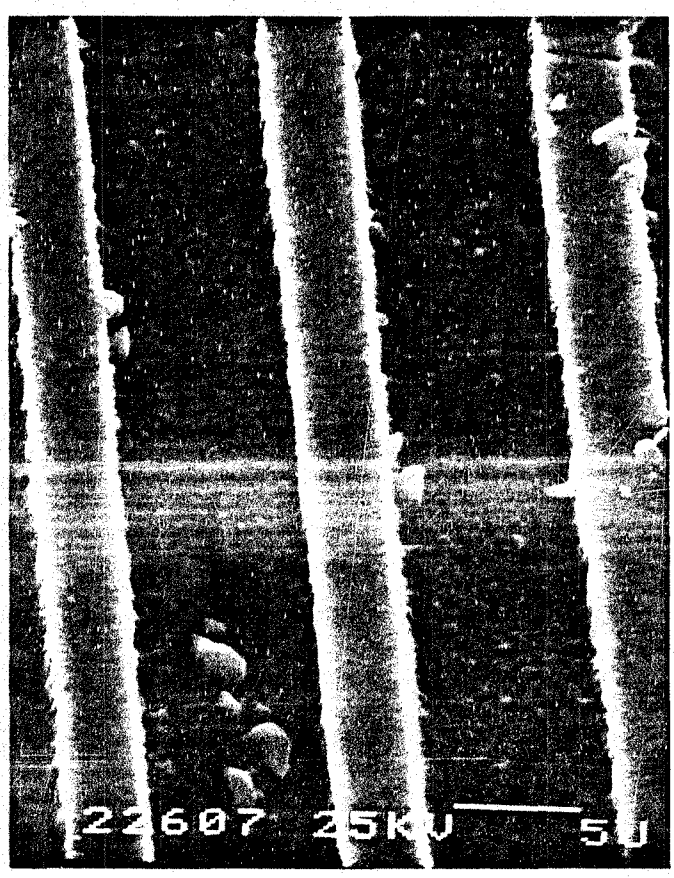



Figure 20. Square grooves with Ga-As-Ti layer.

Figure 21. V-shaped grooves in silicon substrate.

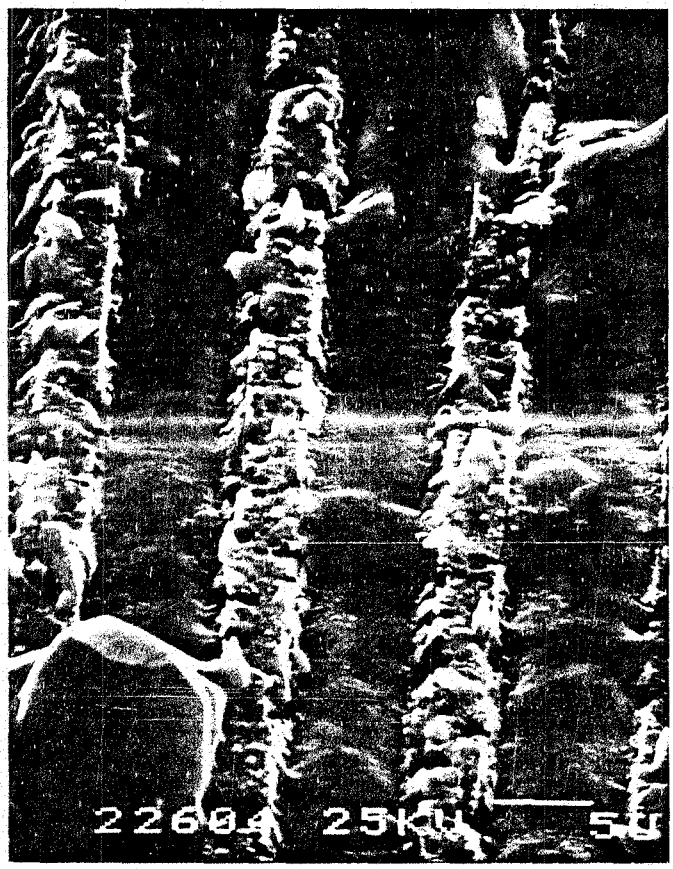



Figure 22. recrystallized GaAs in V-grooves.

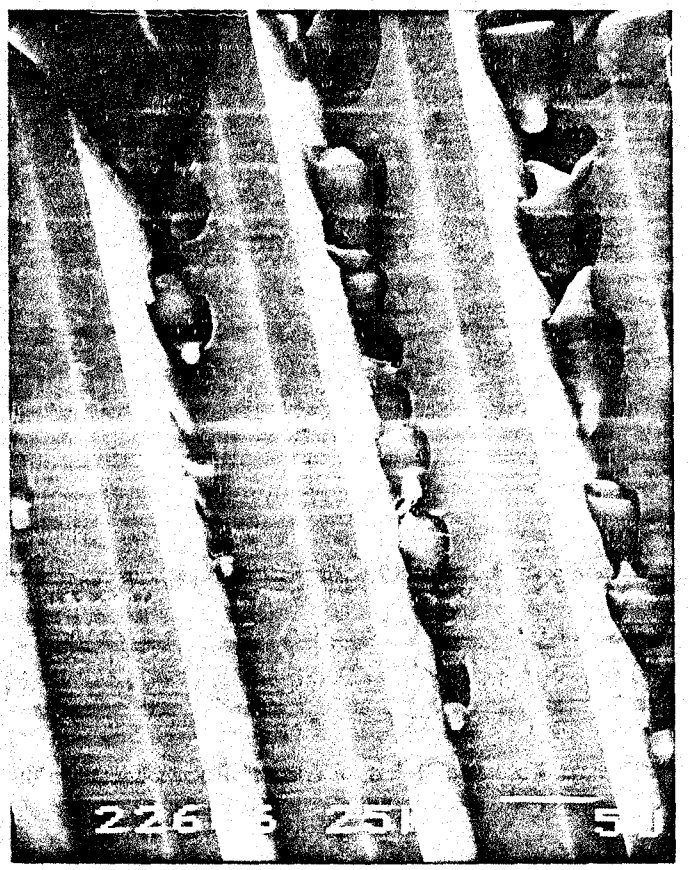


Figure 23. Small clumps of GaAs in bottom of V-grooves.

is continuous, flat, and nearly single crystal. This area is 1 cm long (the length of the sample) and ~ 70 $\mu$m wide. Part of this crystal is shown in Figure 24.

The recrystallization process was not very successful on samples which had only a room temperature oxide separating the GaAs from the Si grooves. Again balling up was a major problem. Most of the sample area was left as bare Si, which had alloyed and lost the V-shaped grooves, with only small spots of GaAs left behind here and there. Sometimes, part of the sample remained covered with GaAs which appears to have remained as small-grained poly which probably did not melt, or, possibly this region could have crystallized in such a way as to have a very rough top surface. Further x-ray analysis is needed to characterize this layer. Figure 25 shows the junction of the almost bare melted grooves with the rough-looking GaAs.

A sample of room temperature oxidized Si with no grooves was also tested. The GaAs recrystallization attempt on this resulted in balling up of the GaAs and melting or alloying of the Si surface.

As a check on our experiments, the conditions which in the past gave very large crystalline GaAs which filled in the grooves and became continuous on the small area, variable spacing pattern were repeated, using the original mask described earlier. The result was exactly the same as before. There is no apparen reason by one mask pattern should work properly while another of almost identical features should not. It might be speculated that the orientation of the grooves parallel to certain crystallographic directions might be critical, and that one pattern set was better oriented than the other. If this were the case, small misorientations could produce large variations in results and non-reproducibility from wafer to wafer in general.

The unknown critical conditions which result in severe nonreproducibility in the recrystallized GaAs layers lead to doubts as to the ease of the GaAs-grooved Si graphoepitaxy process for mass producing GaAs space cells of high power-to-weight ratios. We believe it would be

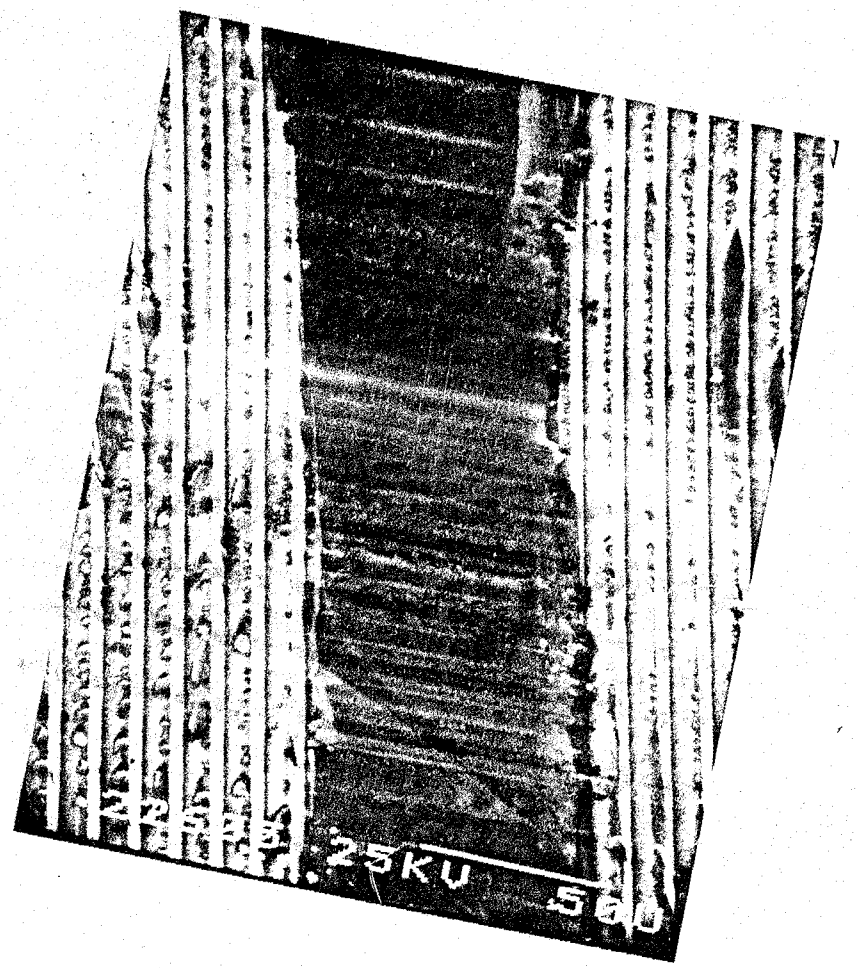



Figure 24. Large, flat GaAs crystal covering several grooves.

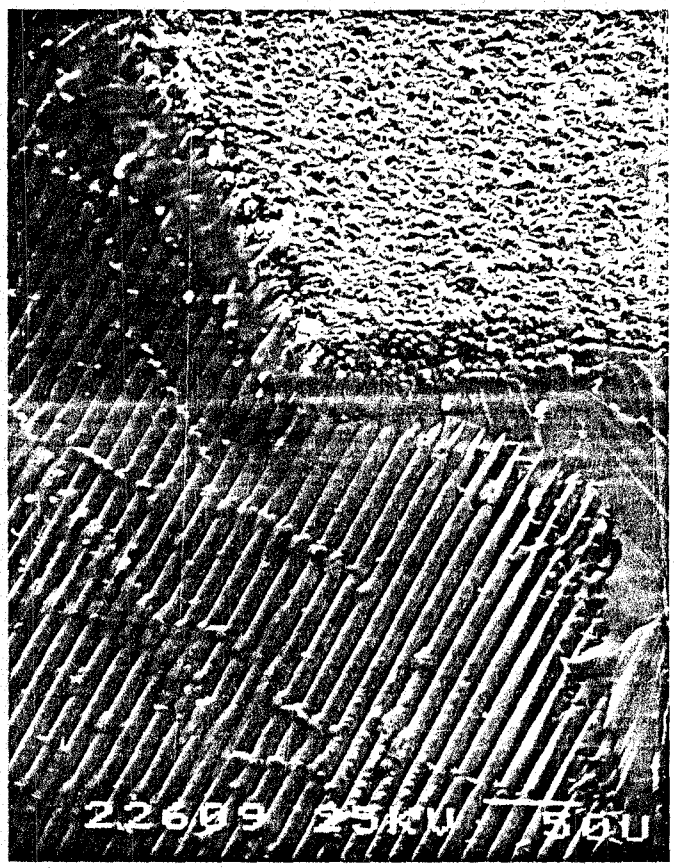


Figure 25. Rough-surfaced GaAs and almost bare Si grooves

possible to produce large grain, oriented, and continuous GaAs films in the laboratory under the right conditions, as shown by Figure 24, but considerably more work would need to be done to discover the reliable and reproducible conditions necessary to do this. In this study, it did not prove possible to obtain continuous film regions large enough for meaningful electrical measurements to be made.

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16. Abstract

The power to weight ratio of GaAs cells can be reduced by fabricating devices using thin GaAs films on low density substrate materials (silicon, glass, plastics). A graphoepitaxy technique has been developed which uses fine geometric patterns in the substrate to affect growth. Initial substrates were processed by etching 25 μm deep grooves into <100> oriented wafers; fine-grained polycrystalline GaAs layers 25-50 μm thick were then deposited on these and recrystallization was performed, heating the substrates to above the GaAs melting point in $AsH_3$ atmosphere, resulting in large grain regrowth oriented along the groove dimensions. Experiments with smaller groove depths and spacings were initially encouraging; single large GaAs grains would totally cover one and often two groove fields of 14 groove each spanning several hundred microns. Dielectric coatings on the grooved substrates were also used to modify the growth.

| 17. Key Words (Suggested by Author(s)) | 18. Distribution Statement |
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