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AND AGC MODIFICATION (Ohio Univ.) 16 p
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RF FRONT END INTERFACE AND AGC MODIFICATION

The Mini-L-82 RF front end has been interfaced to the Ohio University LORAN-C receiver utilizing a modified AGC system.

by

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I. INTRODUCTION

The latest RF front end built by Burhans (Mini-L-82) has been successfully interfaced to the Ohio University LORAN-C receiver (Figure 1). In order for the front end to operate optimally, modifications were made to existing automatic gain control (AGC) circuitry already developed for the Ohio University LORAN-C receiver. This AGC circuit is described in reference 1. This technical memorandum will describe the hardware modifications to the AGC and other interface circuitry, as well as some preliminary results.

II. RF FRONT END DESCRIPTION

The Mini-L-82 RF front end (refer to Figures 2 and 3) is similar in overall design to the previous front end used with the Ohio University receiver but it has a much narrower bandwidth. Also, the Mini-L-82 has a much improved response to lower input signal levels. The output of the front end is a negative-going zero crossing pulse which is 10 microseconds long (Figure 4). In order for the receiver to operate properly, this pulse is inverted using a 7404 TTL inverter. The front end output is also open collector; therefore, an external pull-up resistor is provided. The positive-going 10 microsecond pulse is applied to the existing receiver circuitry which extends the pulse to 70 microseconds using a 74123 monostable. This 70-microsecond pulse is the optimum value for the search and track software routines. Efforts were made to adjust search and track software parameters to use the 10-microsecond pulse. However, it was found that this increased search time substantially and also created difficulties for the tracking loops because of the LORAN-C phase code which causes the zero crossing pulse to shift five microseconds with each phase reversal. Therefore, the interface between the Mini-L-82 and the receiver is essentially the same as that for the old front end.

III. AGC CIRCUIT DESIGN

The AGC circuit is based roughly on the circuit designed for use with the old front end, and it is part of the sensor processor section of the Ohio University LORAN-C receiver (Figures 5, 6, and 7). The envelopes of all the tracked LORAN-C stations are sampled individually with the sampled voltages stored on capacitors. Each tracked station has its own "channel" in the AGC circuit (Figure 8). Channel address control is provided by the microcomputer. Since the magnitude of the sampled voltage often exceeds five volts, all of the AGC circuit components are CMOS integrated circuits with a twelve-volt power supply.

Even though the basic circuit design is similar to the previous AGC circuit, there are important differences to optimize performance with the new front end. The front end is designed to optimize performance at low signal levels. The AGC will "turn down" the gain on the LORAN-C stations until the region of best front end performance is reached. Since the various LORAN-C stations in a given chain are received at various signal amplitudes, it is the function of the AGC to reduce the gain on each

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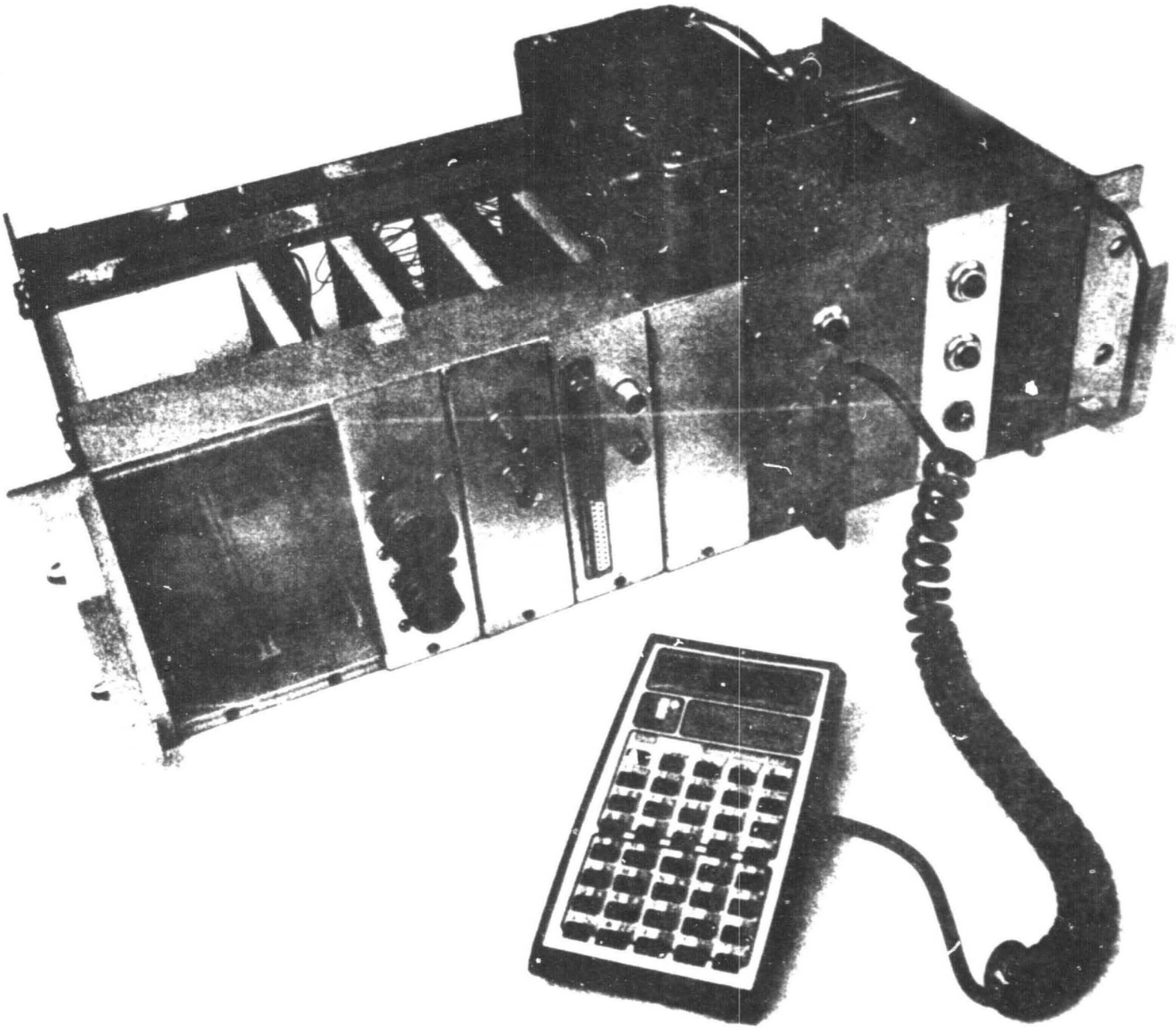


Figure 1. Ohio University Loran-C Receiver.

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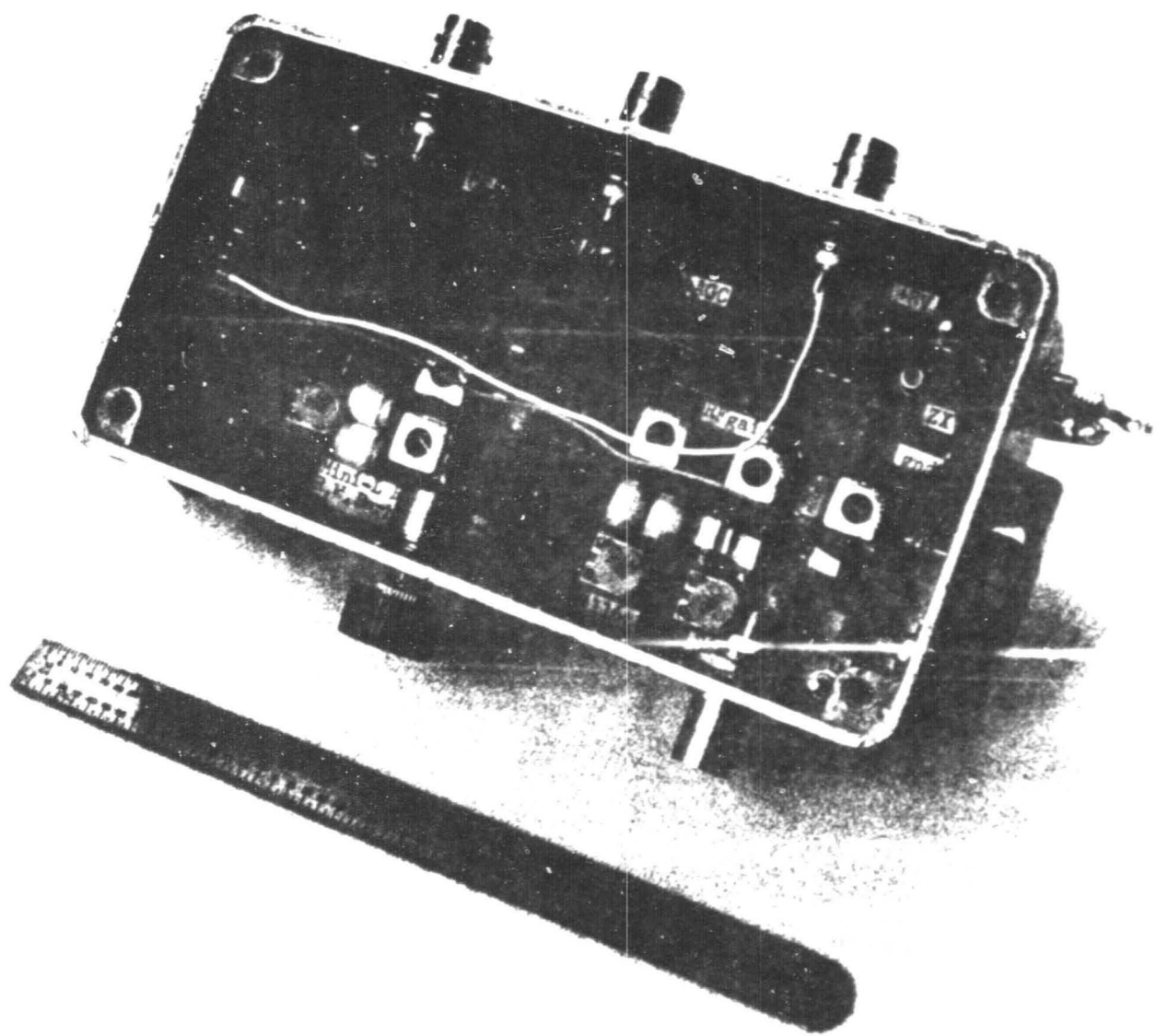


Figure 2. Mini-L-82 RF Front End.

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INPUT from
active preamp
at antenna

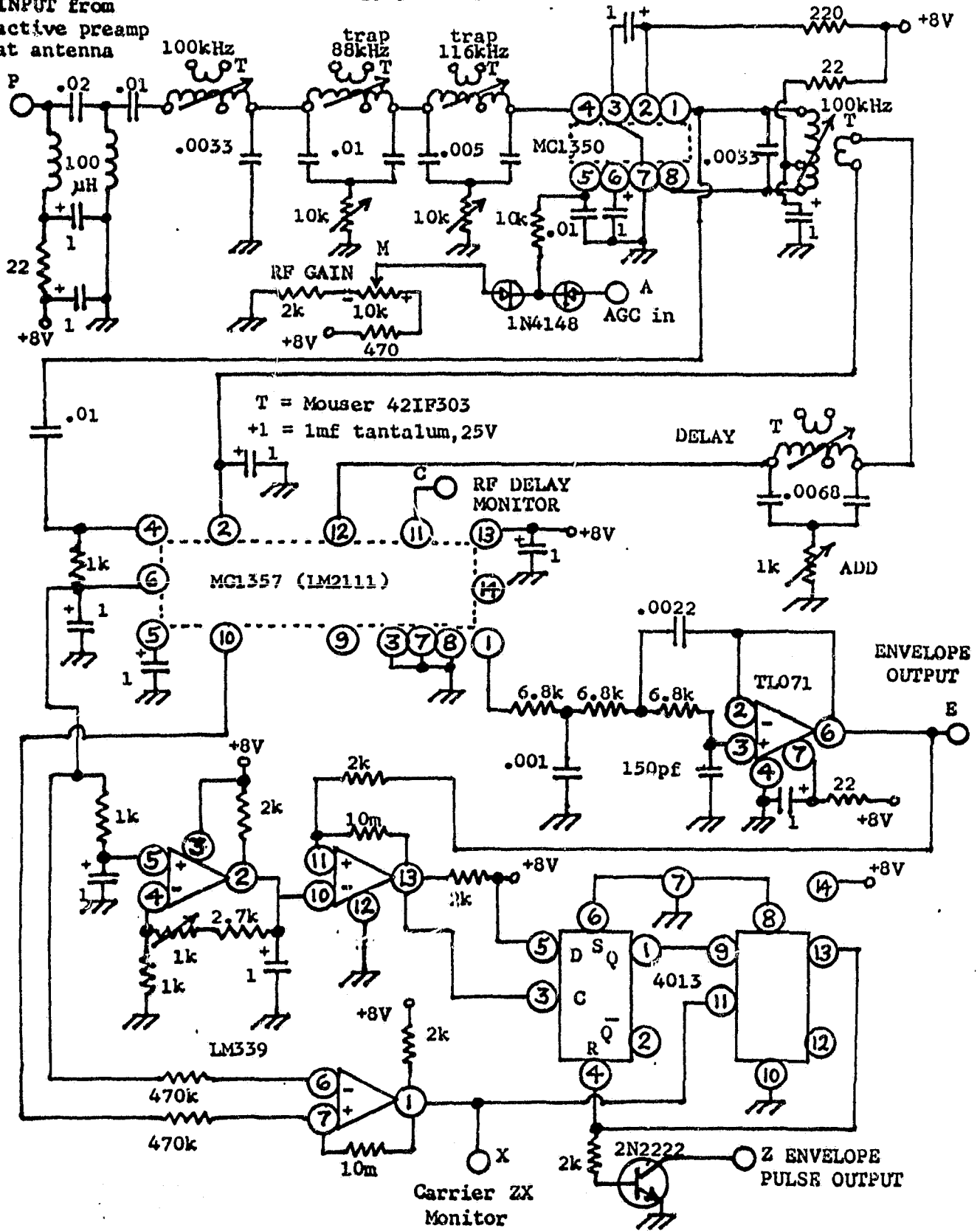


Figure 3. Mini-L-82 Circuit Diagram.

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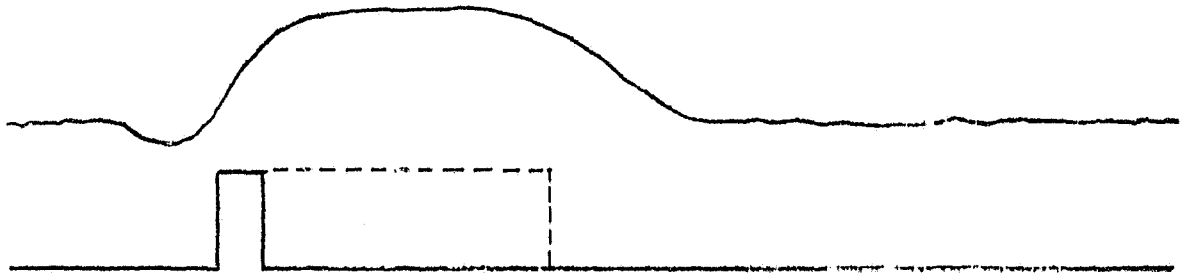
LORAN CHAIN
GRI = 99,600 μ S



LORAN STATION
PULSE SPACING =
1000 μ S



LORAN ENVELOPE
ZERO CROSSING
PULSE = 10 μ S



ZERO CROSSING
PULSE AND
SOFTWARE
EQUALS PULSE
(LENGTH = 1 μ S)

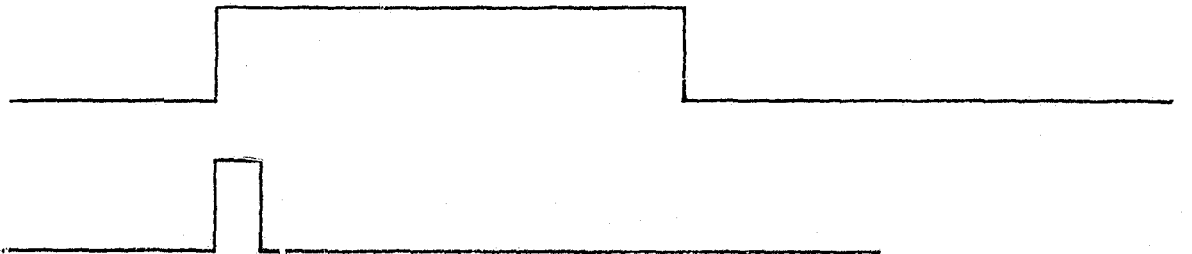


Figure 4. Loran-C Chain Parameters.

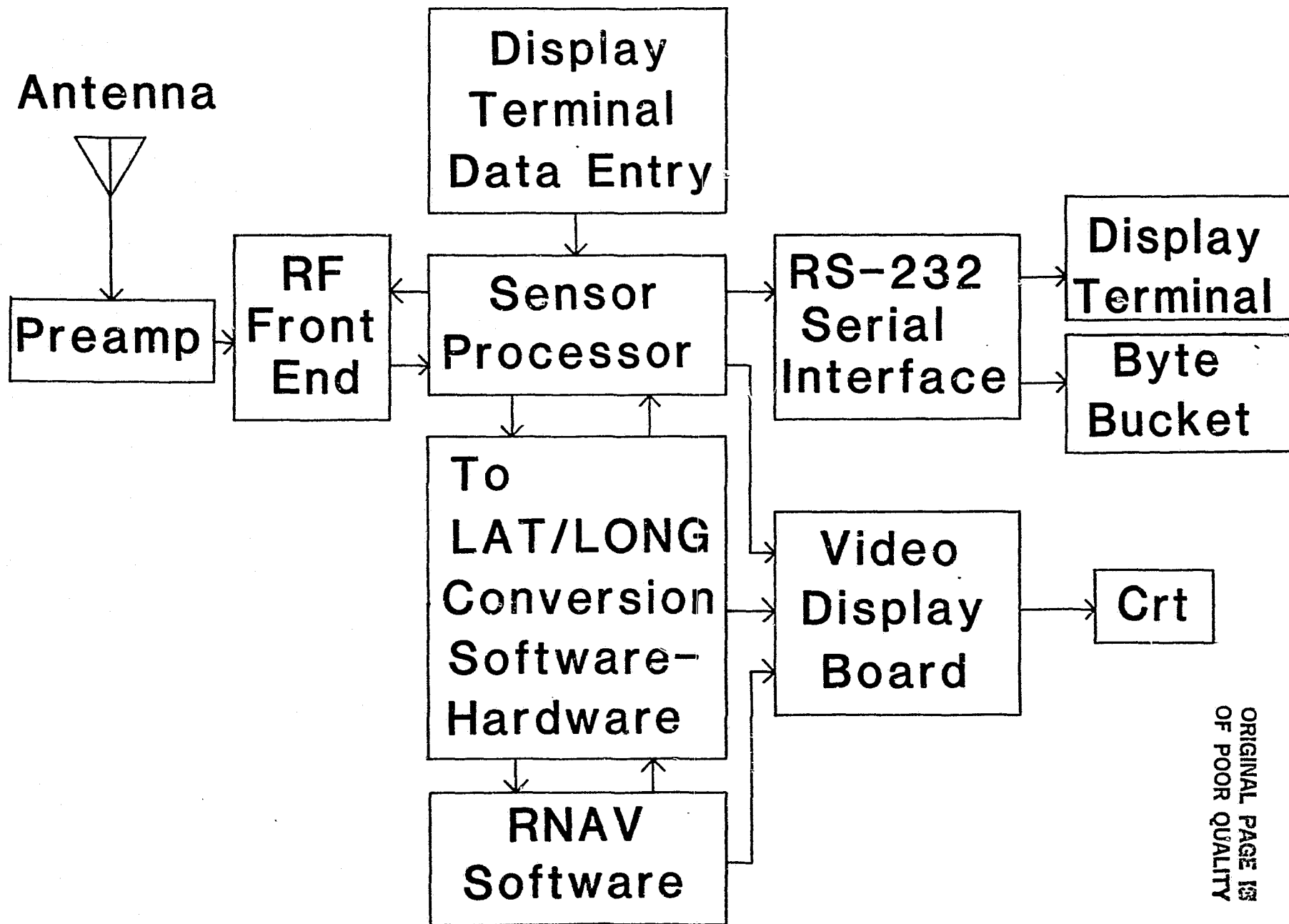


Figure 5. Receiver Block Diagram.

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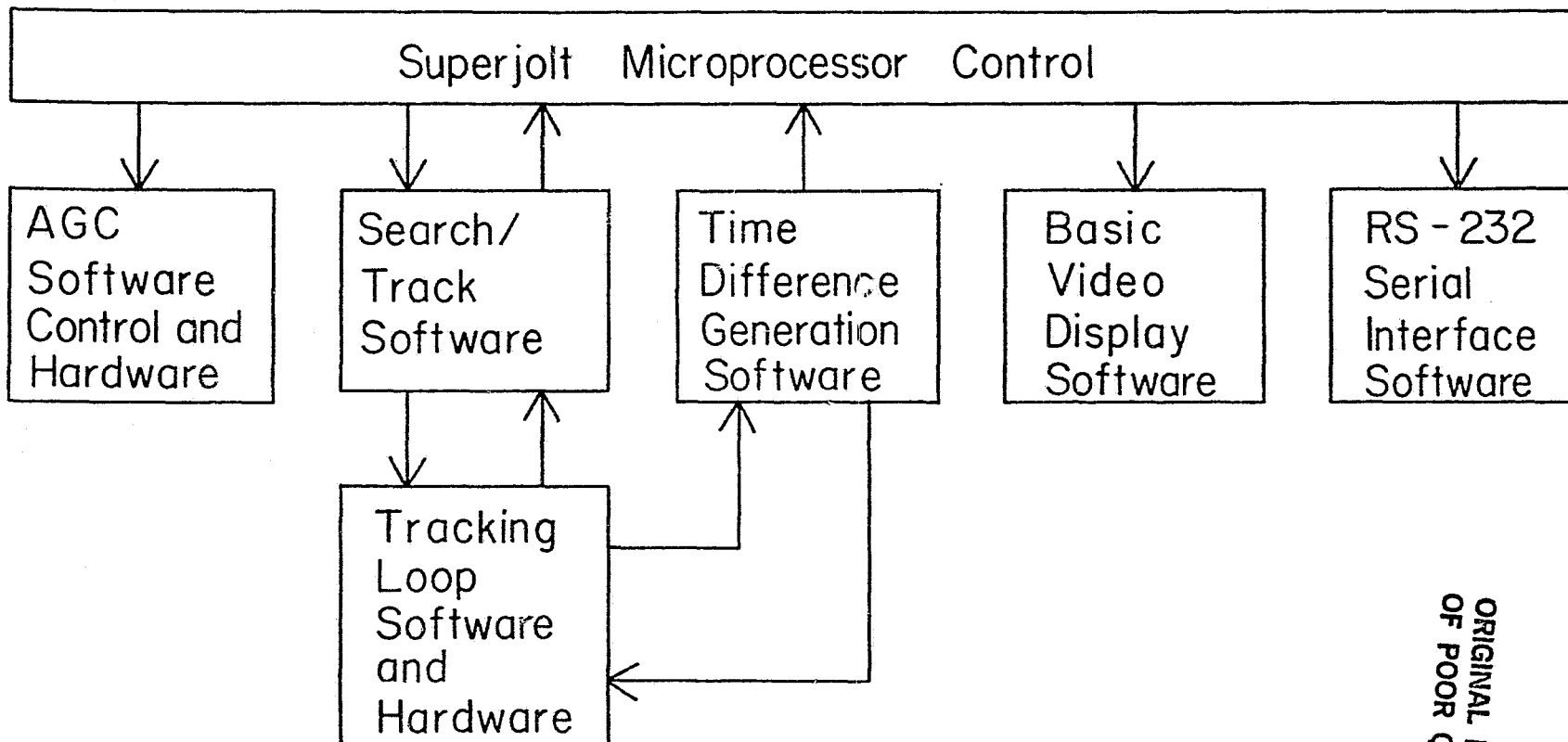


Figure 6. Sensor Processor Block Diagram.

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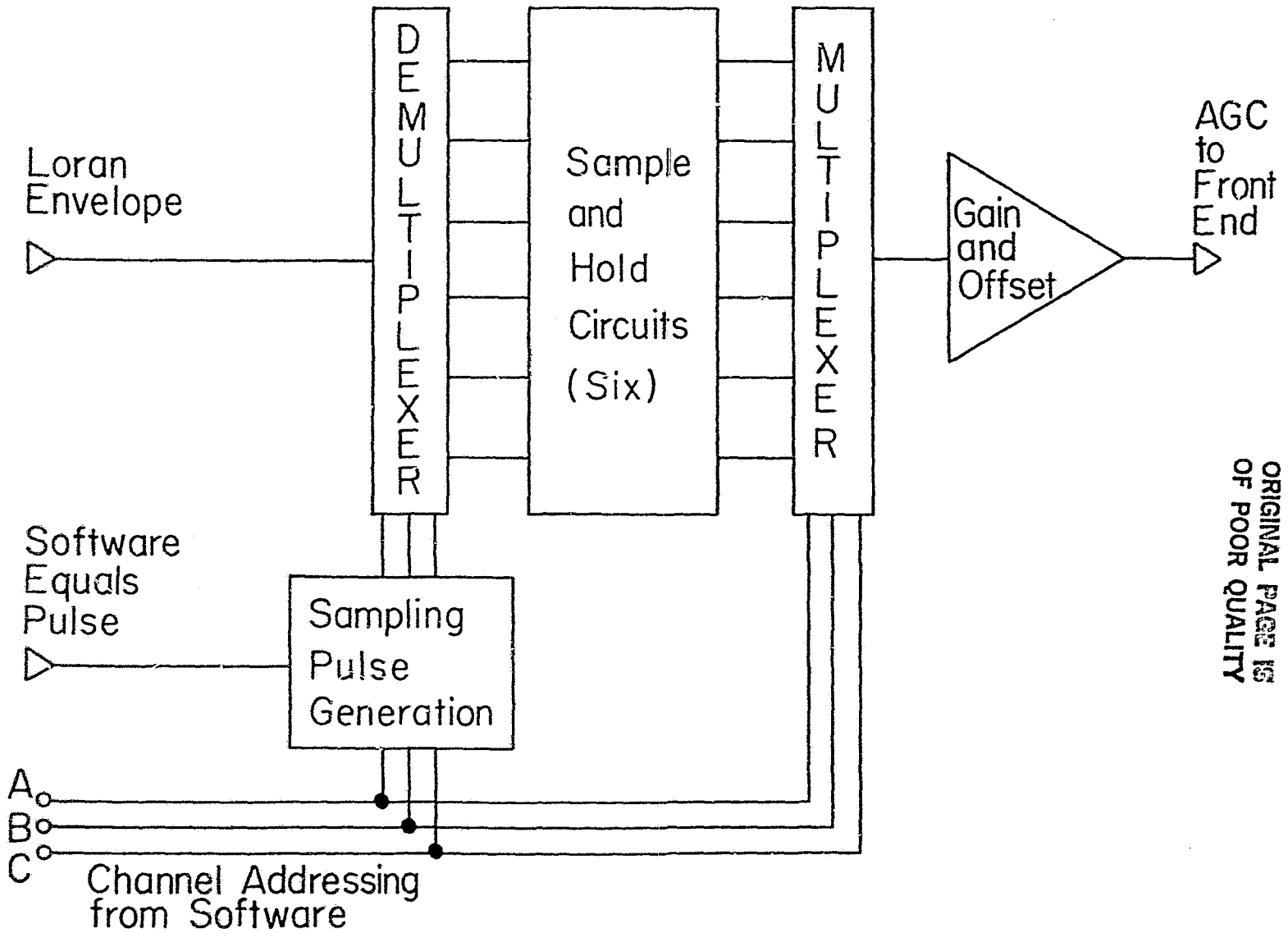
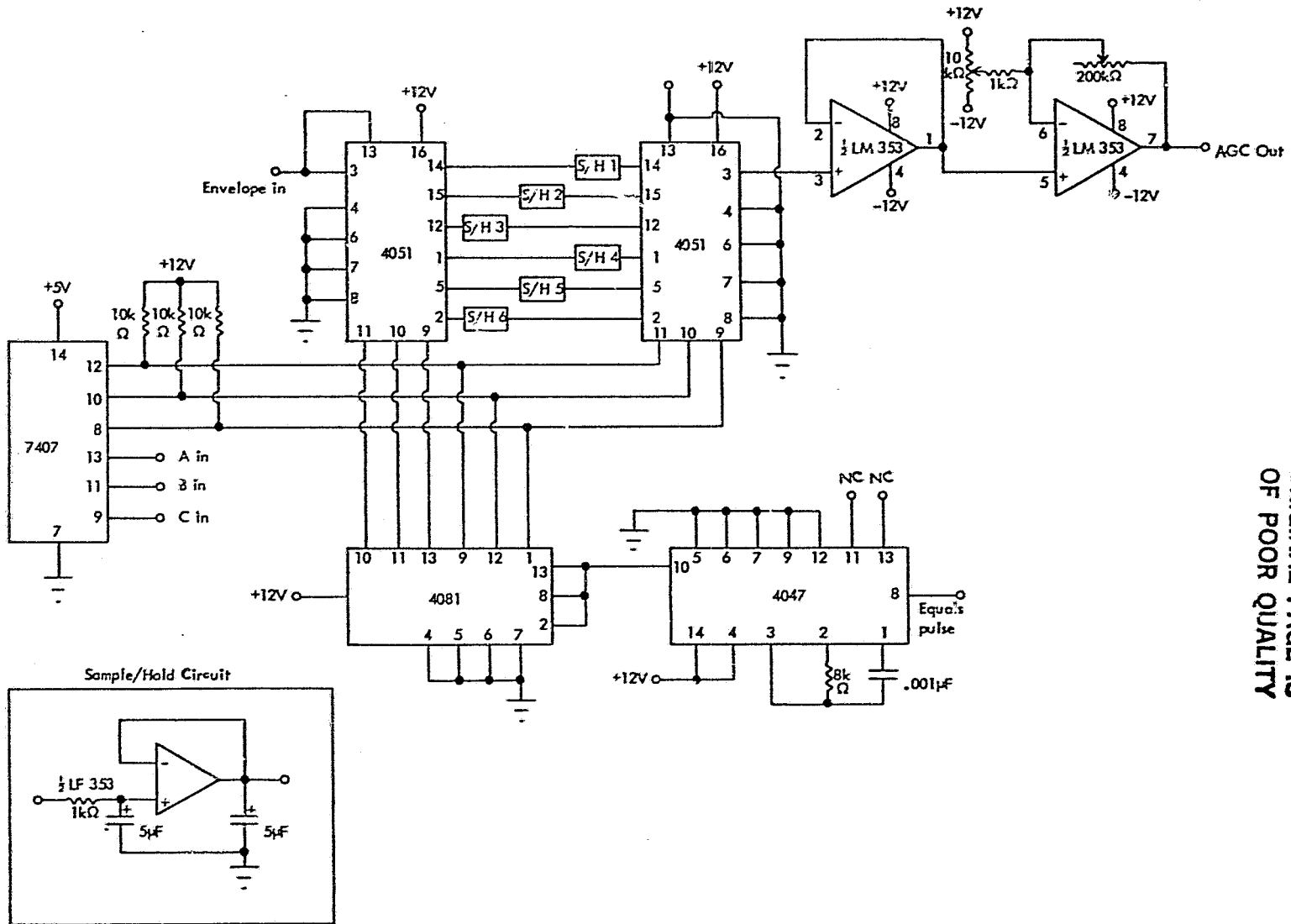


Figure 7. AGC Block Diagram.

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Figure 8. AGC Circuit Diagram.

station proportionate to that station's received signal level. The end result is that all of the LORAN-C stations are processed at a constant signal level. This condition is essential to the proper operation of an envelope-detector front end such as the Mini-L-82.

In the previous AGC circuit, the envelope was sampled during a 20-microsecond sampling window that was delayed 40 microseconds from the zero crossing. It was determined that this sampling area could possibly contain some sky wave contamination. In the current AGC design, the envelope is sampled during a 20-microsecond window starting at the zero crossing. The sampled voltage is dependent on the slope of the envelope at that point. Strong stations have a large slope; hence, a larger sample voltage is stored for that station. The sampled voltages are stored on their respective channels and adjusted for optimum front end performance by the gain and offset adjustment op-amp in the circuit. The AGC amplifier is an integral part of the Mini-L-82 front end design, it provides up to 60 dB of gain.

The AGC circuit was built on a Vector (tm) circuit card in the receiver that also contains 8K bytes of ROM/RAM memory and the serial interface (Figures 9, 10, and 11). Tantalum capacitors were used for the sample and hold circuits because of their low leakage characteristic.

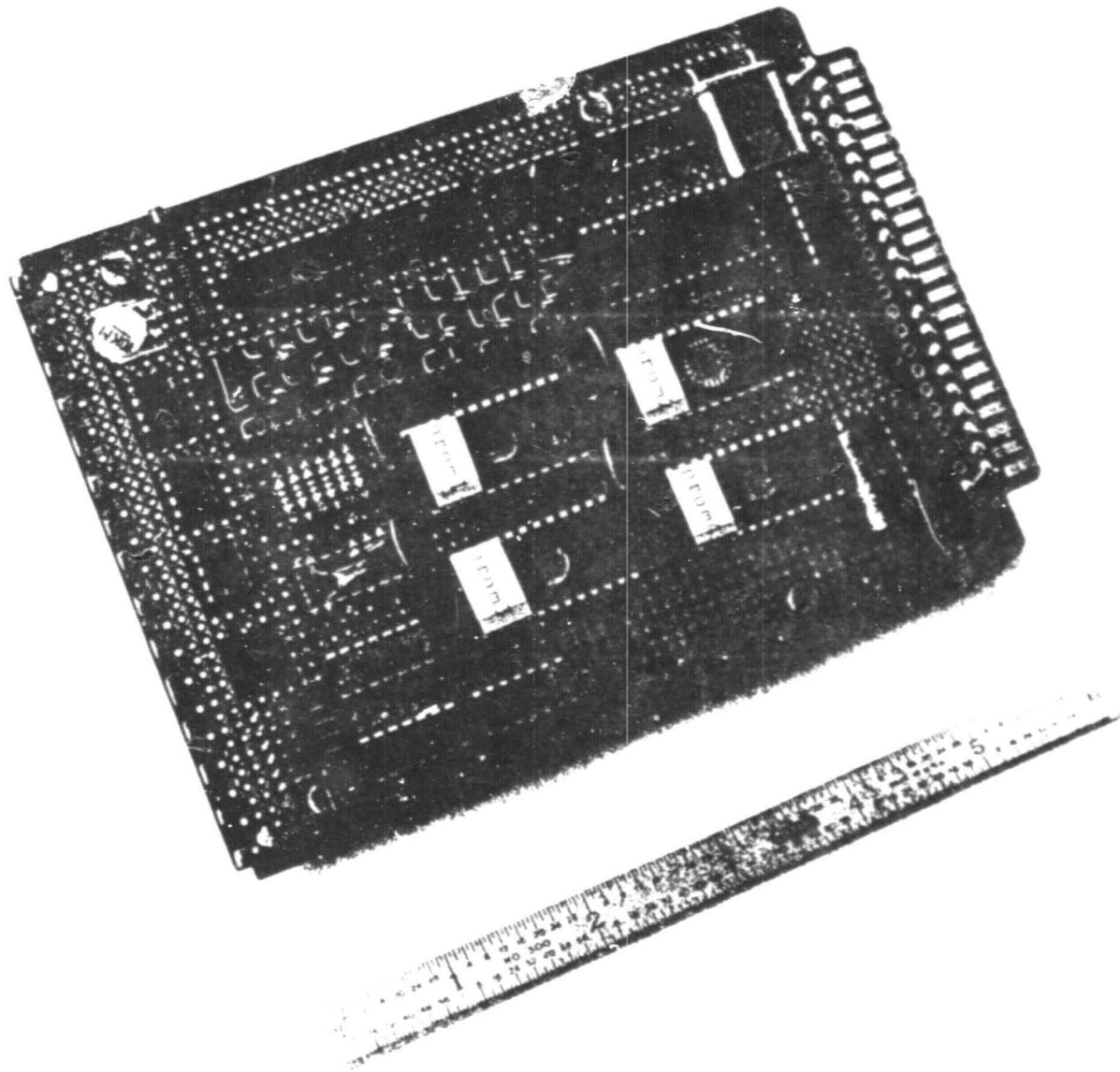
IV. RESULTS AND FURTHER OPTIMIZATION

Preliminary results indicate that the new front end AGC combination perform satisfactorily. Side-by-side bench tests with Trimble 10A and Texas Instruments 9900 LORAN-C receivers have proven that the proper time differences are being obtained. Extensive bench tests and flight tests will follow as time permits.

Further optimization of the AGC circuit will occur as software to track all of the stations in a LORAN-C chain is developed. The AGC circuit was designed to sample up to six separate LORAN-C stations. Along with expanded station tracking software, a more sophisticated search routine is also under development. It is also planned to develop a printed circuit board for the AGC and enclose it with the RF front end in a sealed enclosure to reduce interference from the other digital circuits of the micro-computer.

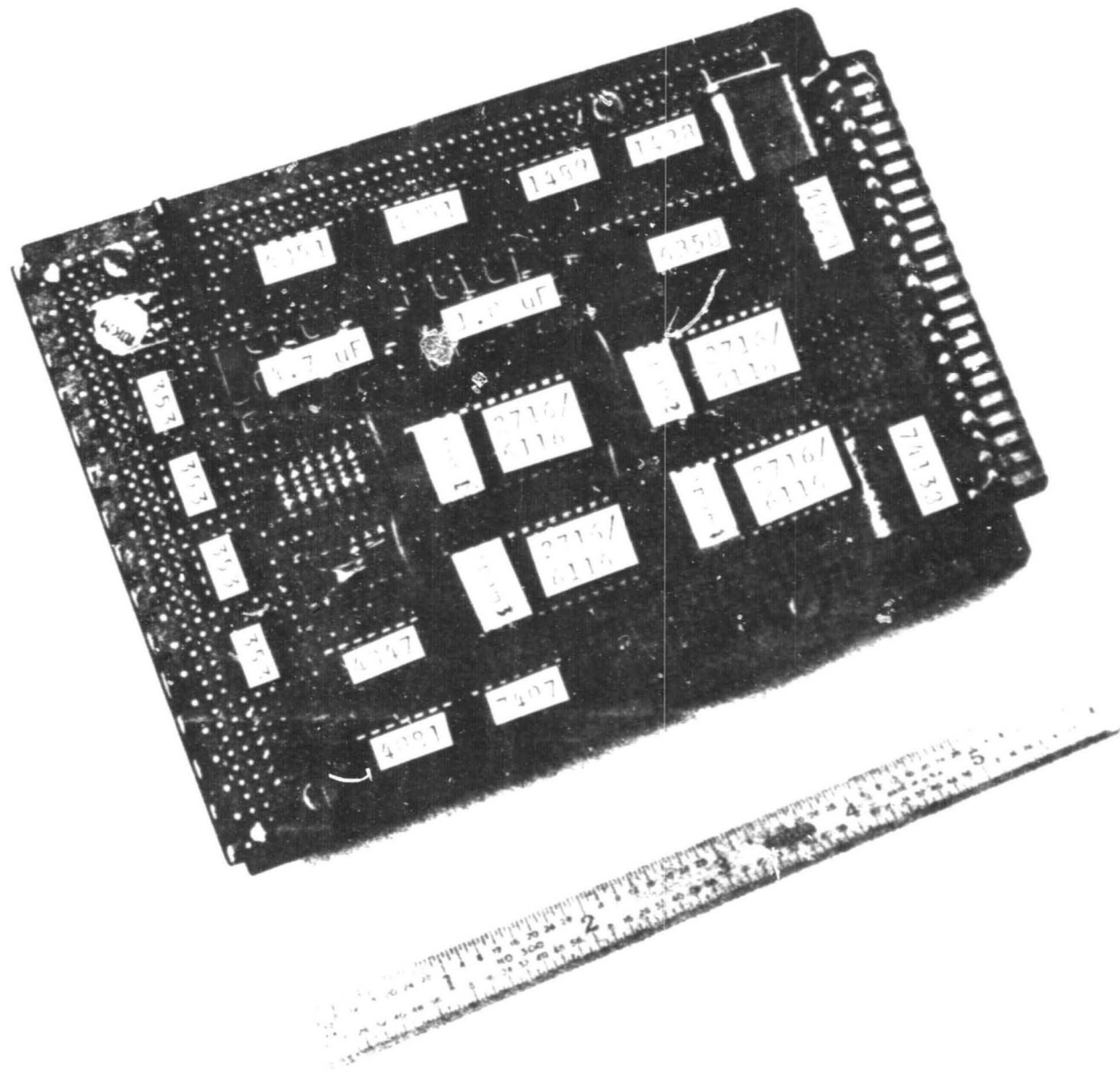
V. ACKNOWLEDGEMENTS

The design, construction, and testing of the Mini-L-82 and the AGC circuitry has been funded by the NASA Joint University Program for air transportation research as a part of the continuing development of Ohio University's LORAN-C receiver. The author would like to thank Mr. Ralph Burhans for continuing his quest for a better front end for the Ohio University LORAN-C receiver. His advise and expertise were of great help in this project. Also providing invaluable assistance were Mr. Jim Nickum, Dr. Robert Lilley, Mr. Daryl McCall, and Ms. Fujiko Oguri. Mr. Nickum took all of the photographs that appear in this report.



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Figure 9. ACC/Memory/Interface Board.



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Figure 10. AGC/Memory/Interface Board Components.

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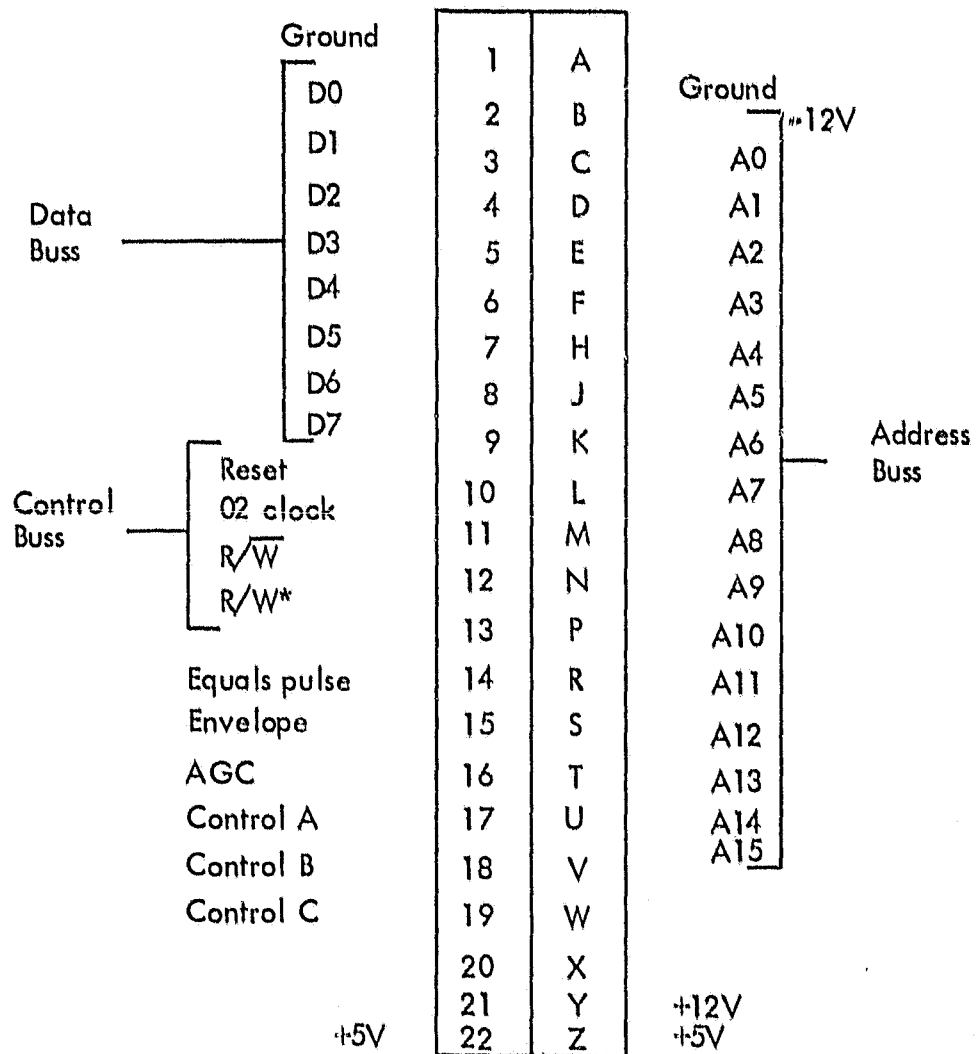


Figure 11. Edge Connector Pin Assignments.

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VI. REFERENCES

1. Yost, Stephen R., "Commutated Automatic Gain Control System", OU NASA TM-81, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, 45701, November 1981.
2. Lilley, Dr. R.W. and Daryl McCall, "A LORAN-C Prototype Navigation Receiver for General Aviation", OU NASA TM-80, Avionics Engineering Center, Department of Electrical Engineering, Ohio University, Athens, Ohio, 45701, August 1981.