IMAGE PROCESSING VIA VLSI

A Concept Paper

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Image Processing via VLSI

Abstract

The general purpose digital computer is not able to handle the data rates and subsequent throughput requirements of data systems in the mid-80's and early 90's. In particular vast quantities of image data will have to be calibrated, geometrically projected, mosaicked and otherwise manipulated and merged at rates that far exceed the capacities of present systems. Even the "super" computers, some of which have been designed explicitly for image processing, promise insufficient throughput capacity. Implementing specific image processing algorithms via Very Large Scale Integrated systems offers a potent solution to this perplexing problem. Two algorithms stand out as being particularly critical -- geometric map transformation and filtering or correlation. These two functions form the basis for data calibration, registration and mosaicking. VLSI presents itself as an inexpensive ancillary function to be added to almost any general purpose computer and if the geometry and filter algorithms are implemented in VLSI, the processing rate bottleneck would be significantly relieved. This work develops the set of image processing functions that limit present systems to deal with future throughput needs, translates these functions to algorithms, implements via VLSI technology and interfaces the hardware to a general purpose digital computer.

Objectives

* Design and fabricate special purpose VLSI chips to perform specific image processing algorithms.
* Integrate such chips into interface systems which are under the control of a central general purpose processor assigned to image processing.

* In particular, design and test filter system and a cubic spline geometric reprojection system.
* Examine and develop VLSI design concepts for other image processing requirements.

Motivation

Bracken (1) has spelled out the need for improving the processing speed of image data collected from an ever increasing array of satellites each with a larger information bandwidth than its predecessor. The processing problem has several dimensions.

* In order to enable the end user to use new information, the data must be restructured to match a previous information base. A common requirement is to reproject and register images taken from an oblique satellite view to a normal projection on the surface. This reprojection along with the need to correct for any systemmatic camera distortions requires that images be stretched like a "rubber sheet" to fit the desired reprojection. This shift which entails many rotations and magnifications within each image requires relocation of interpolated data to locations which may be far distant from some original position.
* In order to determine the precise shift which will bring two images into registration, match points must be determined. Modified cross correlation calculations can be used to maximize the best fit of these match points. Correlation and filtering have similar mathematical structure and both can be implemented with a special purpose VLSI system. The filtering operation is also used to smooth noisy data or enhance fine image detail. Image enhancement has been applied rather infrequently in spite of image improvement because

it is an expensive process. VLSI operation can reduce the cost and time of processing. Filtering also enables certain feature detection and extraction algorithms.

* Another dimension of image processing relates to where in the data stream the processing is to be performed. Our present technology thus far requires transmission of unprocessed images. As high speed compact processing technology evolves, processing can be moved on to the satellite and transmission bandwidth reduced by several orders of magnitude.
* Pipeline processing implies placing simultaneous hardwired algorithms in tandem. Other image processing functions such as sorting maximum values, change detection, developing time dimensions on accumulated data bases become accessible in near real time when thinking in terms of modular hardware.

Background

Digital image processing became a working reality in the early 1960's with the advent of JPL's Ranger, Surveyor and Mariner series. We (Nathan-2) had effectively established the requirements for various processing algorithms from pragmatic pressures. Filtering was performed to remove systematic noises from the camera and geometric corrections also were required to correct camera distortion. Filtering further evolved to enhance fine image detail without stretching low frequency data to cause image saturation. In those early missions it was generally possible to keep up with the data load with the processing power of computers available at the time. No real attempt was made to do more than refine those algorithms using commercially available machines. Since that time the situation has dramatically changed in terms of volume while the algorithms have remained relatively static.

Several attempts at creating special parallel processors have proven expensive and unwieldy. A comparison of several "super" computers was performed by Mitre Corporation (3). They were given several classes of very limited tests against which to measure processing effectiveness. Some of the computers compared were the Cray I, the DAP (English), the PEPE (Army), the Illiac IV, the Cyber 203, the AP-120B, the CLIP 3 and the MPP (Goddard-Goodyear). All but the AP-120B are extremely expensive (several millions of dollars each) whereas the AP-120B is very much slower. Mitre judged the MPP to be the best as determined from the given conditions. But the filter and geometric test problem was much too constrained and just fit the 128x128 area of parallel memory in MPP. Only a kernal of 20x20 can be filtered against a 128x128 image. Only a shift of 8 pixels using linear interpolation is allowed for geometric remapping. These restrictions have been hardwired and only slow software can overcome them. The heart of the MPP is a general purpose VLSI processing unit. The direction of the concept is still in terms of multiple function performance by a particular hardware unit.

VLSI is a general tool which can be viewed as an extension of software in the sense of the next generation of computing power. These concepts have been under development at Caltech under Mead (4). JPL has a very close relationship with the campus. We have recently been working with Mead to aid in the rapid evolution of the software techniques for designing VLSI circuitry and have, in addition, been developing filtering hardware concepts following a data flow algorithm from Cohen (5) which allows successive multiplier-accumulators to be pipelined. A modification in memory handling allows an extension to two dimensions and is being breadboarded to fit the VLSI design. As a seed effort we have started to

design a VLSI chip which will allow us to create a 31x31 element kernal that will compete favorably timewise and dollarwise against the MPP.

Approach

VLSI design is still a rapidly evolving field. Computer languages are under development which will eventually allow high level statements to be made which establish functional criteria and these statements would be converted to n-channel metal oxide semiconductor (n-MOS) or complementary c-MOS wire lists. These lists are in turn converted by computer to drawings of different overlays of metal and metal oxides. The drawings are then photo-reduced and photo-etched onto silicon or sapphire wafers which are then cut and wired to form individual chips.

The amount of logic that can be placed on a single chip is also evolving rapidly. Today many tens of thousands of transistors can be stored on a surface 7x7 mm sq. Within three to five years that number is expected to increase by 2 to 3 orders of magnitude. At JPL we are experimenting with ways to develop languages which will allow variation of parameters, number of multipliers, number of bits/multipliers, serial or parallel additions/multiply and other parameters which will allow us to tailor fit to customer need without massive redesign effort.

As we contemplate the marriage of VLSI technology with image processing requirements, not all the pieces are yet in place. Some of the designing effort is still initiated by manual drawings to meet VLSI design rule requirements. The logic for multiplication is still not finalized as competition for area (on the chip) and speed (minimum clock cycles per multiply) is under study. Conceptual design for the geometry operation is under rapid restructuring as various experts are consulted (Billingsley-6). Projects like these are studied by Caltech students in

Prof. Mead's classes and valuable interchange is derived from those discussions. The whole idea is to be able to upgrade design concepts and create new VLSI chips as though debugging computer software.

In parallel with the actual chip development hardware is being developed to interface the VLSI to existing computer structures. A not too surprising result emerges as this effort progresses. VLSI allows an improvement in throughput over a serial general purpose computer by a factor of 2 to 3 orders of magnitude. We very quickly become I/O bound in terms of magnetic tape or disk. Consideration must be given to grabbing the data once from mass (serial) storage, and performing all processes at once (pipeline serial) before sending the restructured data or extracted information back on to tape or out to the customer.

We have spent some time with the initial development of a VLSI chip which presently has four multipliers each of which stores 20 bits and multiplies an 8-bit pixel by a 12-bit weight. The chip has been submitted for fabrication external to JPL. Turnaround is about two months. JPL's role is not to compete with the commercial fabrication process, but we are more interested in developing more versatile VLSI design tools.

Some effort has gone into the concept of a pipelined geometry remapping chip. An initial concept designed by us (Nathan) was tried successfully by Northrup for the Air Force. But that was only a nearest neighbor design. We have developed many software algorithms over the years, and recently thought is being given to a four point modified cubic spline which should not degrade the image as does nearest neighbor or linear interpolation. The concept is to perform two orthogonal stretches (or contractions) along each axis as serial operations (pipelined in two VLSI functions) while have direct access to several megabytes of random

access memory from the computer main frame. The proposed speed of transformation is many times that presently available.

Expected Results

Two sets of hardwired algorithms are to be produced. One algorithm will perform two dimensional filtering or correlation on an arbitrarily large image using a 31x31 kernal (at present design -- a modifiable parameter). The other algorithm is a pair of one dimensional cubic spline geometry remapping functions which under software control will "rubber sheet" one image to another according to pre-established pass points. It is expected that these systems will be installed for use in JPL's Image Processing Laboratory (IPL) and be used in their image processing production mode.

Progress is anticipated in the development of software which utilizes the filter hardware to establish "pass points" and these in turn will generate the correction grid for the geometry hardware.

Also investigation into class extraction using the filter hardware will be started. Studies of this sort exist as software only. It is desired to explore increased dimension of class search once a fast hardware filter becomes available.

Another product which can be expected is the ability to reproduce other VLSI configurations with minor changes in design parameters. This ability gives us the power to update new hardware without major mechanical redesign as customer needs change.

As concepts develop regarding the utility of other imaging operations, these too shall be pursued.

References

1. Bracken, P.A. (1980) - "Earth Resource Observations Data Systems in the 1980's" in 1980 Annual Meeting of American Astronautical Society and AIAA Paper 80-240.

2. Nathan, R. (1966) - "Digital Video Data-Handling," Technical Report JPL 32-877.

3. MITRE Corp. (1979) - "Parallel Processor Technology Trade-off Study for the NASA End-to-End Data System (NEEDS)."

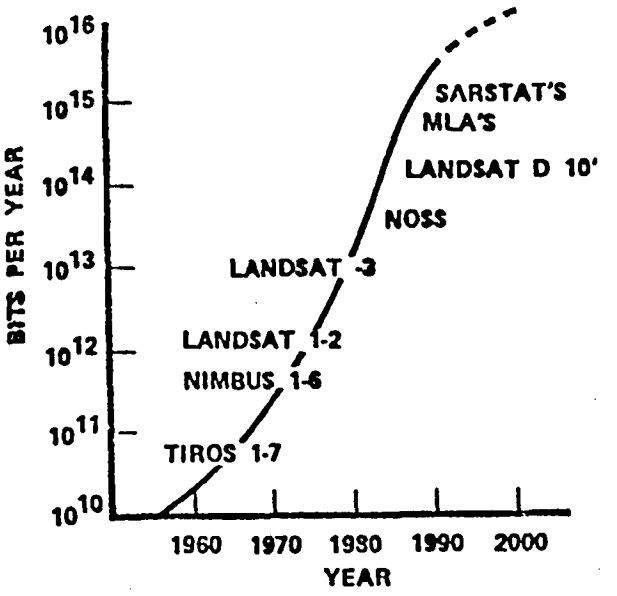
4. Mead, C.A. and Conway, L.A. (1980) - "Introduction to VLSI Systems," Addison-Wesley pub.

5. Cohen, D. (1978) - "Mathematical Approaches to Computational Networks," 151/RR-78-73 Information Sciences Institute/USC.

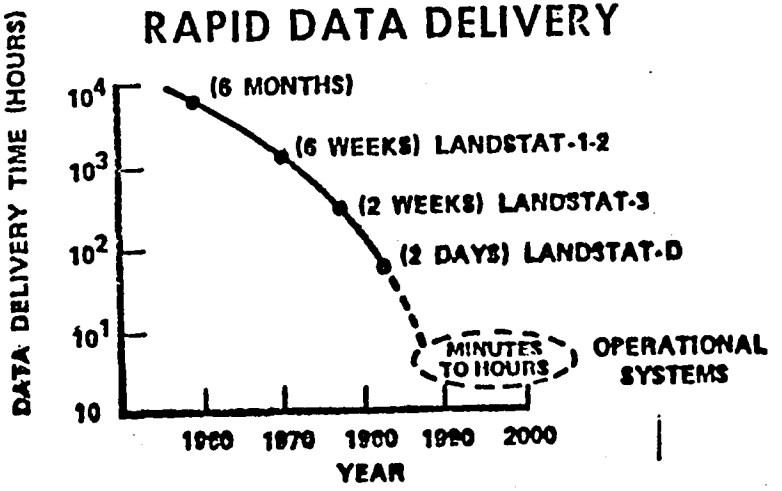
6. Billingsley, F.C. (1981) - "Modelling Misregistration and Related Effects on Multispectral Classification," JPL report in press.

DATA SYSTEM DRIVER

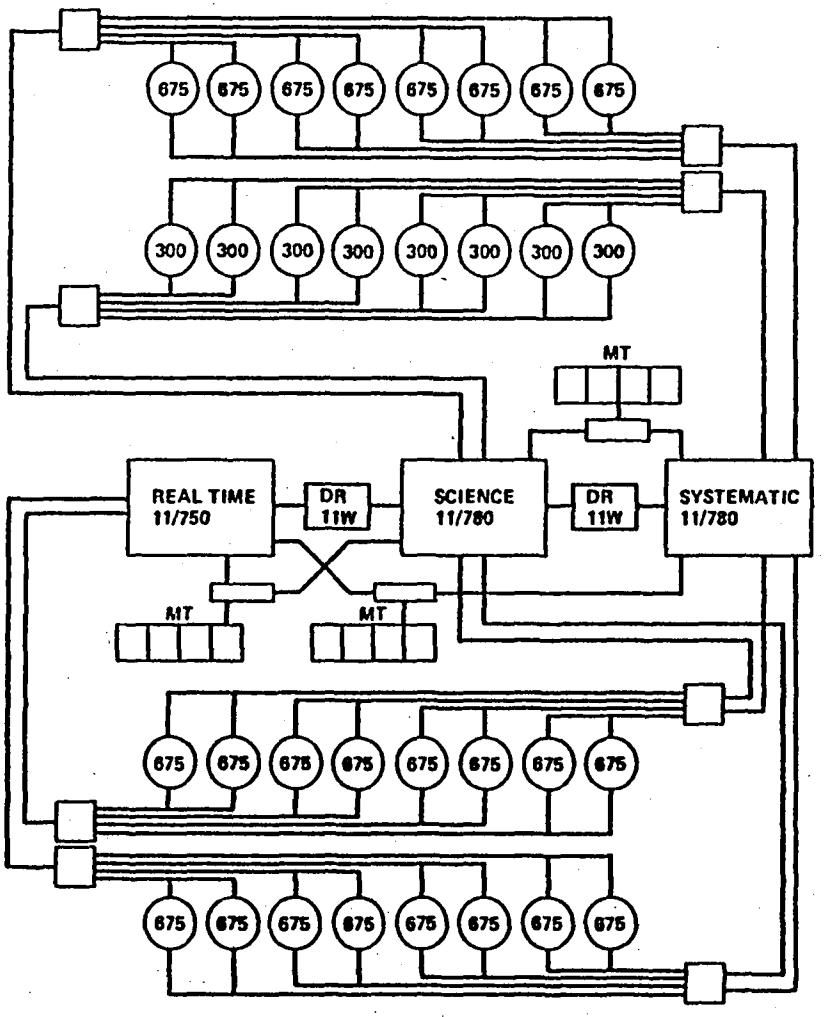
DATA VOLUME

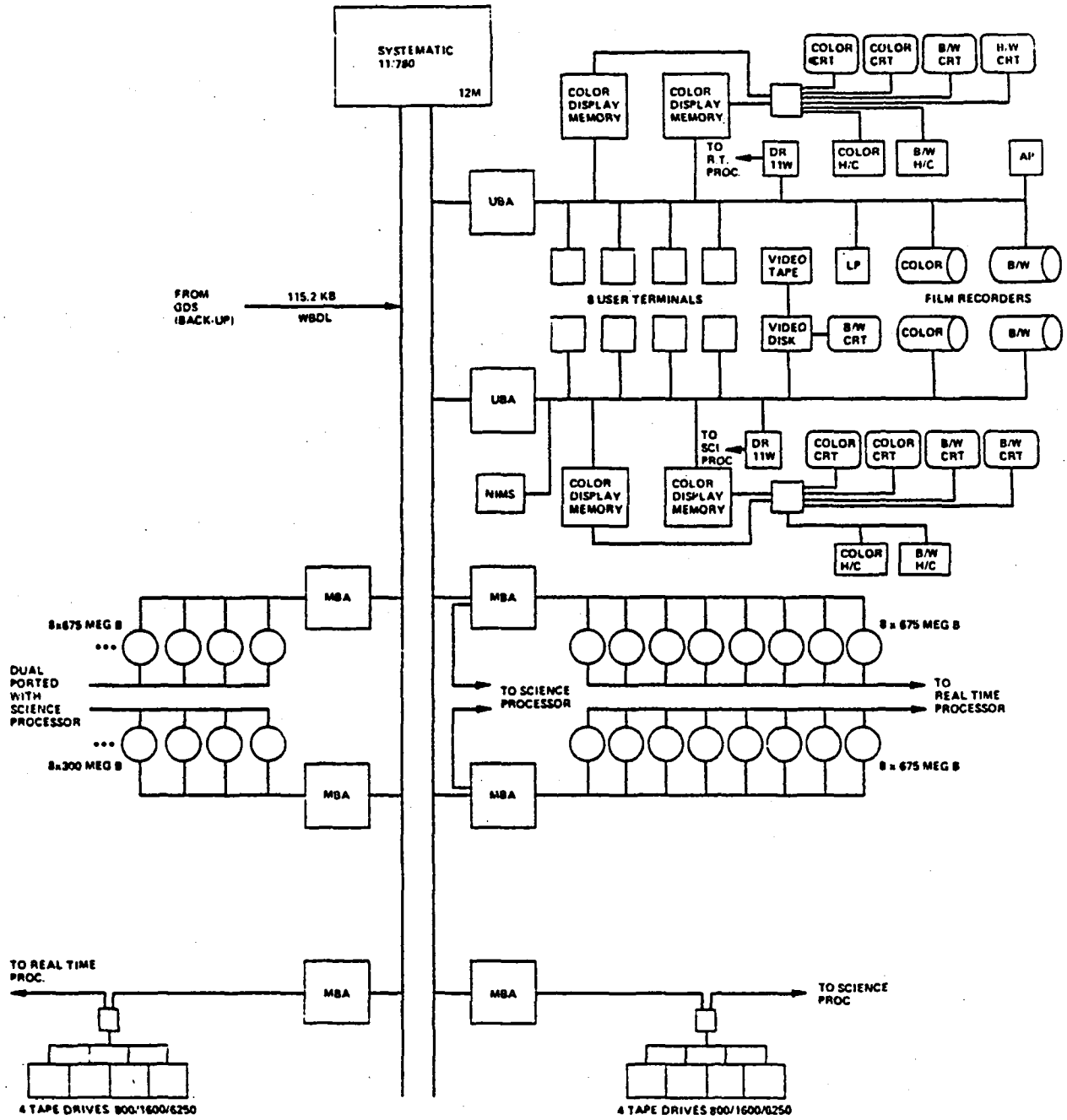


RAPID DATA DELIVERY



MIPL VAX CONFIGURATION




SYSTEMATIC 11/780
12M
COLOR CRT
COLOR CRT
B/W CRT
H.W CRT
COLOR DISPLAY MEMORY
COLOR DISPLAY MEMORY
TO R.T. PROC.
DR 11W
COLOR H/C
B/W H/C
AP
UBA
VIDEO TAPE
LP
COLOR
B/W
8 USER TERMINALS
FILM RECORDERS
FROM GDS (BACK-UP)
115.2 KB
WBDL
VIDEO DISK
B/W CRT
COLOR
B/W
UBA
TO SCI PROC
DR 11W
COLOR CRT
COLOR CRT
B/W CRT
B/W CRT
NIMS
COLOR DISPLAY MEMORY
COLOR DISPLAY MEMORY
COLOR H/C
B/W H/C
MBA
MBA
8x675 MEG B
8 x 675 MEG B
DUAL PORTED WITH SCIENCE PROCESSOR
TO SCIENCE PROCESSOR
TO REAL TIME PROCESSOR
8x300 MEG B
8 x 675 MEG B
MBA
MBA
TO REAL TIME PROC.
MBA
MBA
TO SCIENCE PROC
4 TAPE DRIVES 800/1600/6250
4 TAPE DRIVES 800/1600/6250

	KCPS
NCR V-8560	281
Univac 70/61 (RCA)	287
Univac 70/7 (RCA)	287
Univac 3000E	295
IBM 370/145	300
Univac 70/60 (RCA)	300
Univac 70/3 (RCA)	300
DEC 1056 (2X)	307
CDC Omega 480-I	321
Magnuson M80/3	321
Univac 90/70	329
Burroughs 4700	340
Burroughs 3930	340
Burroughs 6807	340
Univac 9700	344
Honeywell 66/10	350
Nanodata QMX 6333	360
Burroughs 6203	382
NCR V-8570	383
Univac 1100/11	392
Univac 1103	400
Univac 418-III	400
Honeywell 2050 (2X)	405
NCR V-8555M	424
Burroughs 6700	425
IBM 370/148	425
Magnuson M80/31	430
Burroughs 6208	450
Burroughs 6205	459
DEC 2040	462
Honeywell DPS 8/20	473
DEC 1050	486
DEC 1070 KI	497
DEC PDP 11/60	510
CDC 171	520
Honeywell 66/10 (2X)	525
Magnuson M80/4	531
Magnuson M80/32	531
NCR V-8555 MP	531
Honeywell 66/30*	540
Burroughs 6207	544
Univac 1100/80 C1	544
Burroughs 6208	545
IBM 370/155	550
Nanodata QMX 6309	560
CDC Omega 480-II	563
Honeywell 66/20	560
Univac 1100/81 C1	560
IBM 3033/68	568
Univac 1106-II	571
NCR V-8575	576
NAS AS/4	595
DEC PDP 11/70	600
DEC 1095 (2X)	608
Univac 9030-2	630
Univac 1108-II (overlap)	814
Univac 494	850
NCR V-8565	656
Univac 1100/61 C2	672
Univac 1100/60 C2	680

	KCPS
121 Honeywell 66/17*	700
122 IBM 3033/78	700
123 Honeywell DPS 8/44	710
124 Burroughs 4340	718
125 DEC 1077 (2X)	748
126 IBM 4341	750
127 Univac 1108	760
128 Burroughs 6810	765
129 Burroughs 6811	765
130 Burroughs 6812	765
131 NCR V-8585M	770
132 Univac 90/80-3	800
133 Univac 90/80	825
134 DEC 1090 KL	829
135 DEC 1090	829
136 DEC 2060	829
137 IBM 370/158	829
138 NAS AS/5-1	829
139 DEc VAX-11/780	831
140 Magnuson M80/42	834
141 Burroughs 7803	845
142 Burroughs 7750	845
143 Nanodata QMX 6343	880
144 NCR V-8575 MP	884
145 Burroughs 7805	900
146 Honeywell 66/40	900
147 IBM 370/158-3	900
148 NAS AS/5-3	900
149 CDC Omega 480-III	950
150 Magnuson M80/43	985
151 CDC 72	1,000
152 NAS AS/4 MP	1,000
153 Honeywell 66/20 (2X)	1,008
154 Univac 1100/12	1,044
155 IBM 3031	1,045
156 Univac 1100/41	1,092
157 Univac 90/80-4	1,100
158 Honeywell 66/27*	1,120
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160 Univac 1110 (1X1)	1,143
161 Burroughs 6817	1,147
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163 Univac 1100/60 H1	1,153
164 DEC 1099 (2X)	1,160
165 DEC 1088 (2X)	1,180
166 Honeywell DPS 8/52	1,200
167 CDC 172	1,220
168 Burroughs 6821	1,260
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170 Honeywell 66/60	1,296
171 Univac 1108 MP	1,290
172 Burroughs 7755	1,300
173 CDC 73	1,300
174 Honeywell 66/60	1,300
175 NCR V-8535 MP	1,340
176 Univac 1100/61 H2	1,344
177 NAS AS/5-1 MP	1,407
178 Univac 1100/60 H2	1,496
179 Univac 1100/62 E1	1,496
180 Burroughs 7750	1,528

	KCPS
181 NAs AS/5-3 MP	1,530
182 Honeywell 66/40 (2X)	1,6
183 Univac 1100/62	1,70
184 Univac 1100/81	1,800
185 CDC 173	1,870
186 IBM 370/155	1,900
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189 Burroughs 7770	1,960
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193 Univac 1100/82 H1	2,244
194 Honeywell 66/60	2,278
195 IBM 370/168	2,300
196 Honeywell 66/80 (2X)	2,340
197 Burroughs 7765	2,350
198 Amdahl	2,437
199 CDC 74	2,500
200 CDC 6600	2,500
201 IBM 370/168-3	2,500
202 IBM 3032	2,500
203 Burroughs 7780	2,535
204 NCR V-8650	2,650
205 Univac 1100/43	2,759
206 Univac 1100/62	2,000
207 CDC 174	2,005
208 Amdahl 470 V/5-II	2,850
209 Burroughs 7775	3,000
210 NAS AS/6	3,000
211 CDC 76	3,120
212 Univac 1110 (4X4)	3,300
213 Univac 1100/82	3,350
214 Amdahl 470 V/6	3,450
215 Honeywell DPS 8/70	3,570
216 Univac 1100/44	3,615
217 CDC 6700	3,700
218 Amdahl 470V/6-II	3,750
219 Amdahl 470 V/7B	3,825
220 Burroughs 7785	3,900
221 Burroughs 7821	4,000
222 IBM 3033N	4,000
223 Amdahl 470V/7A	4,250
224 NCR V-8670	4,290
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230 IBM 3033U	5,900
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232 Amdahl 470 V/8	6,375
233 Univac 1100/84	6,400
234 Honeywell DPS 8/70 (4X)	6,510
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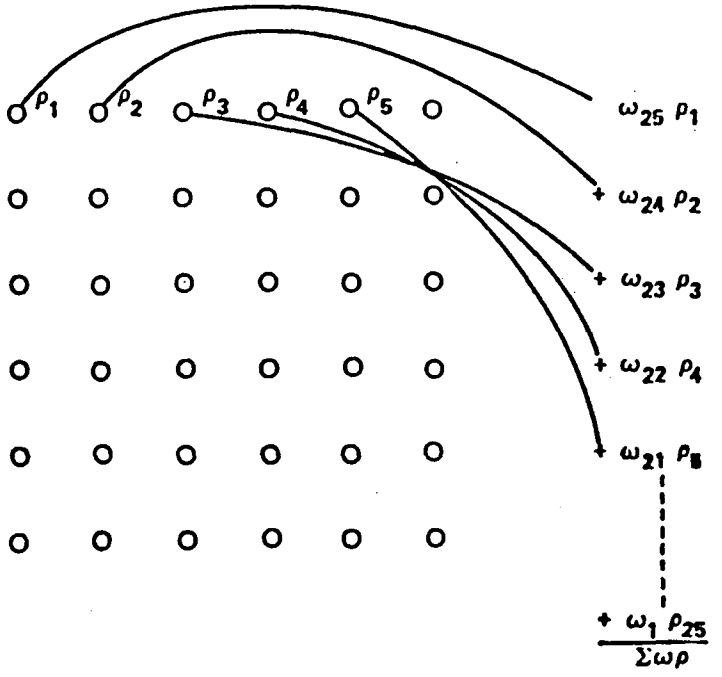
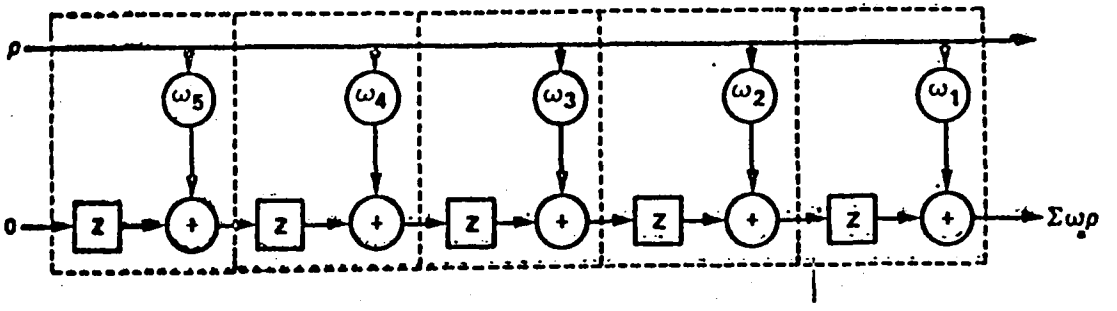
236 CDC 7600	10,000
237 CDC Cyber 205 (vector)	500,000
238 Cray 1 S (vector)	500,000

*Time-shared

SERIAL FILTER



PIPELINE FILTER



VLSI

VERY LARGE SCALE INTEGRATED SYSTEMS

PARALLEL/PIPELINE PROCESSING

CONCURRENT VS. SERIAL

MANY (>10,000 TRANSISTORS) ON A SINGLE CHIP

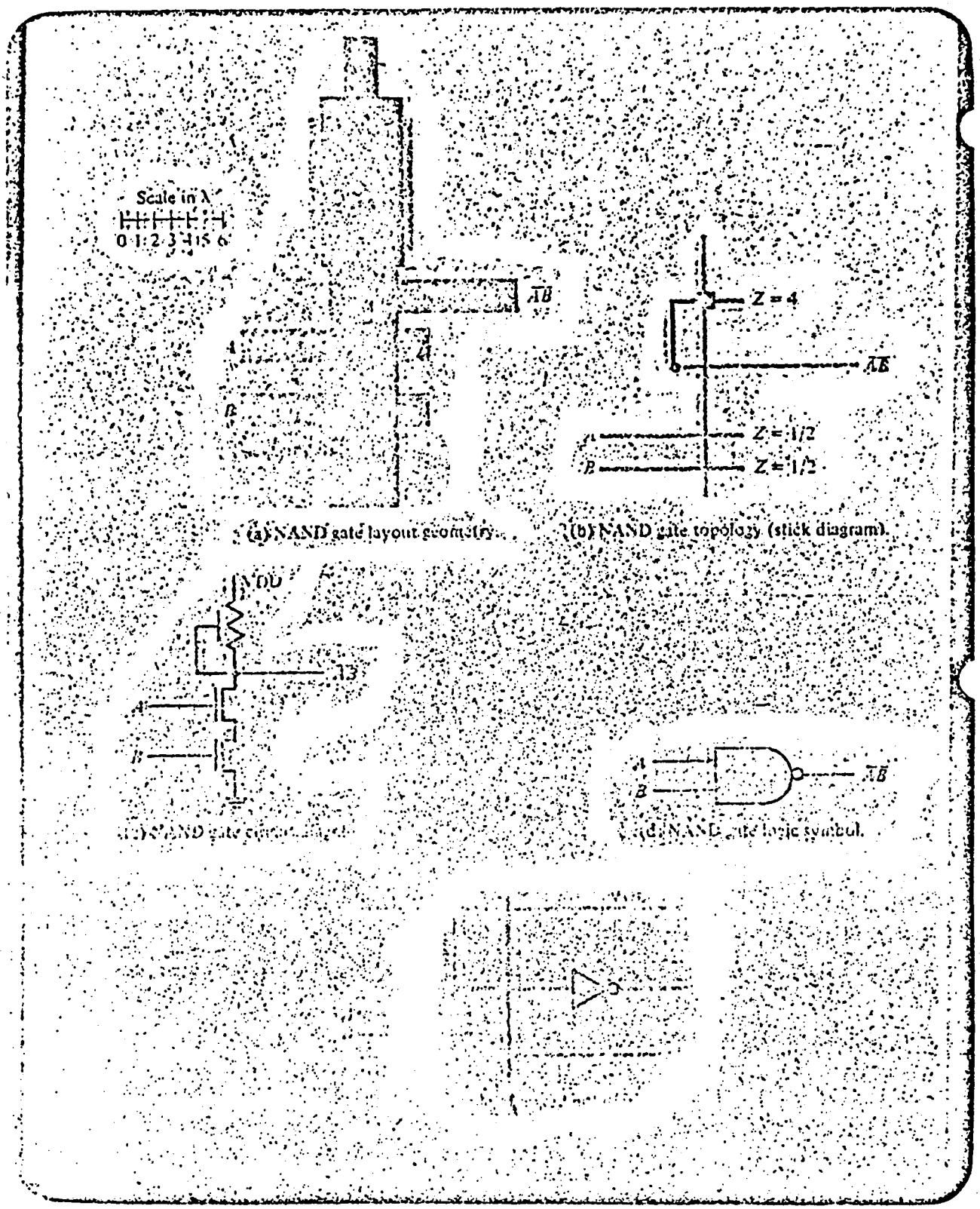
INEXPENSIVE WHEN COMPARED TO DISCRETE LOGIC

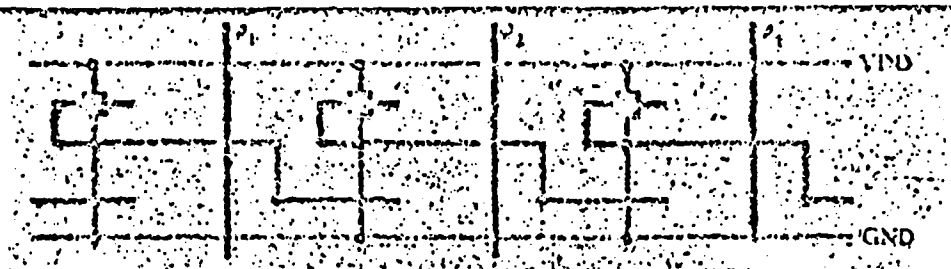
NEXT EVOLUTIONARY STEP BEYOND SOFTWARE

COMPUTERS GENERATING COMPUTERS

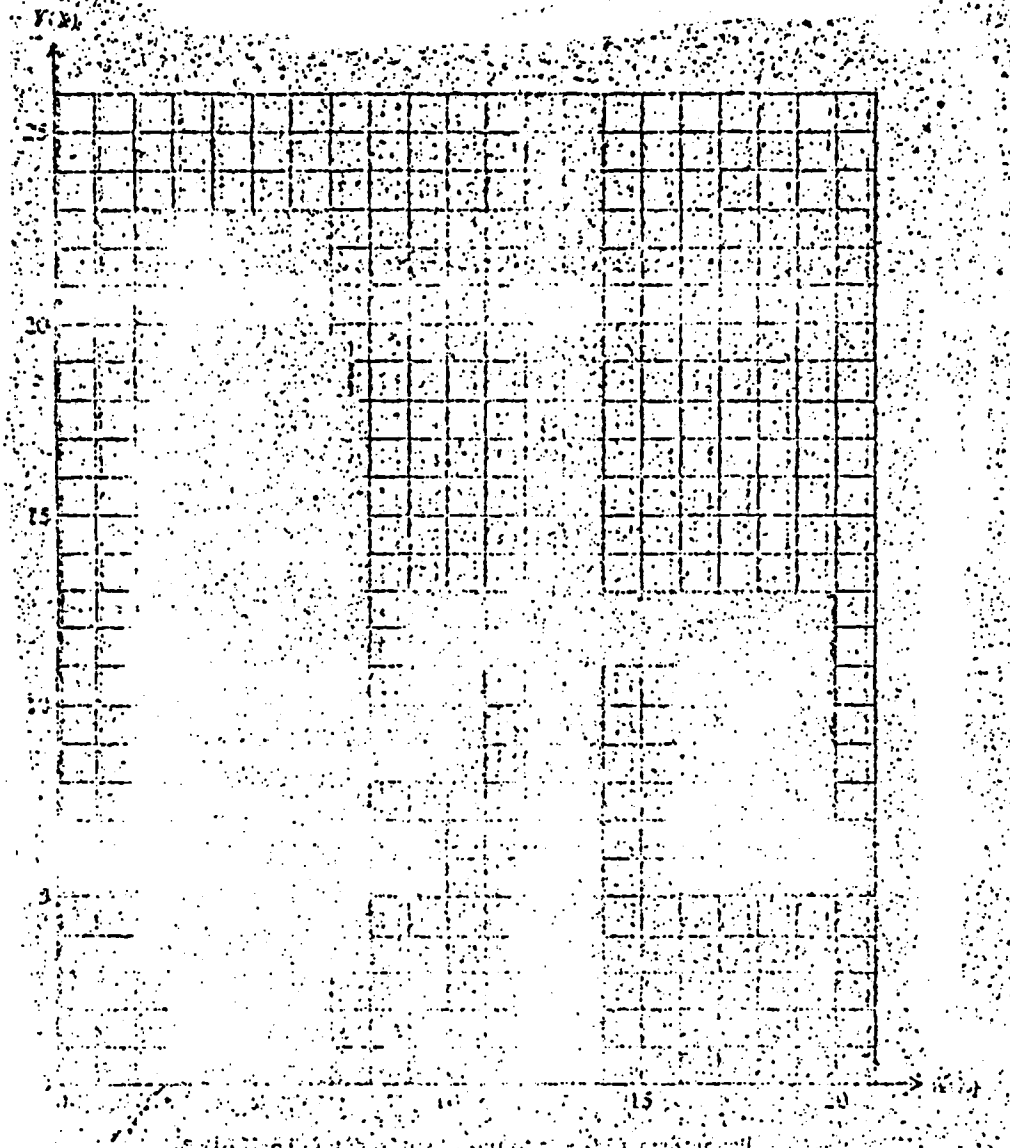
HIGH LEVEL LANGUAGE USED TO CONVERT ALGORITHMS INTO HARDWARE

COST EFFECTIVE COMPARED TO SERIAL PROCESSORS


Scale in λ
0 1 2 3 4 5 6
$\overline{AB}$
A
B
Z = 4
$\overline{AB}$
Z = 1/2
Z = 1/2
B
(a) NAND gate layout geometry.
(b) NAND gate topology (stick diagram).
VDD
A
B
$\overline{AB}$
(d) NAND gate logic symbol.



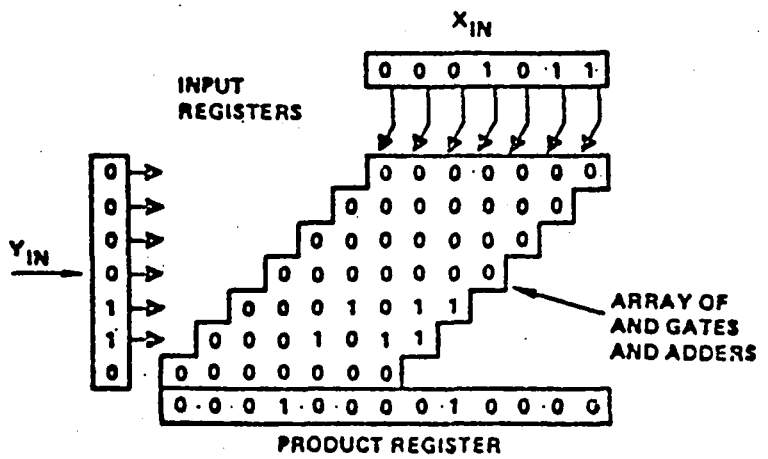
(a) Stick diagram of one row of a shift register array.

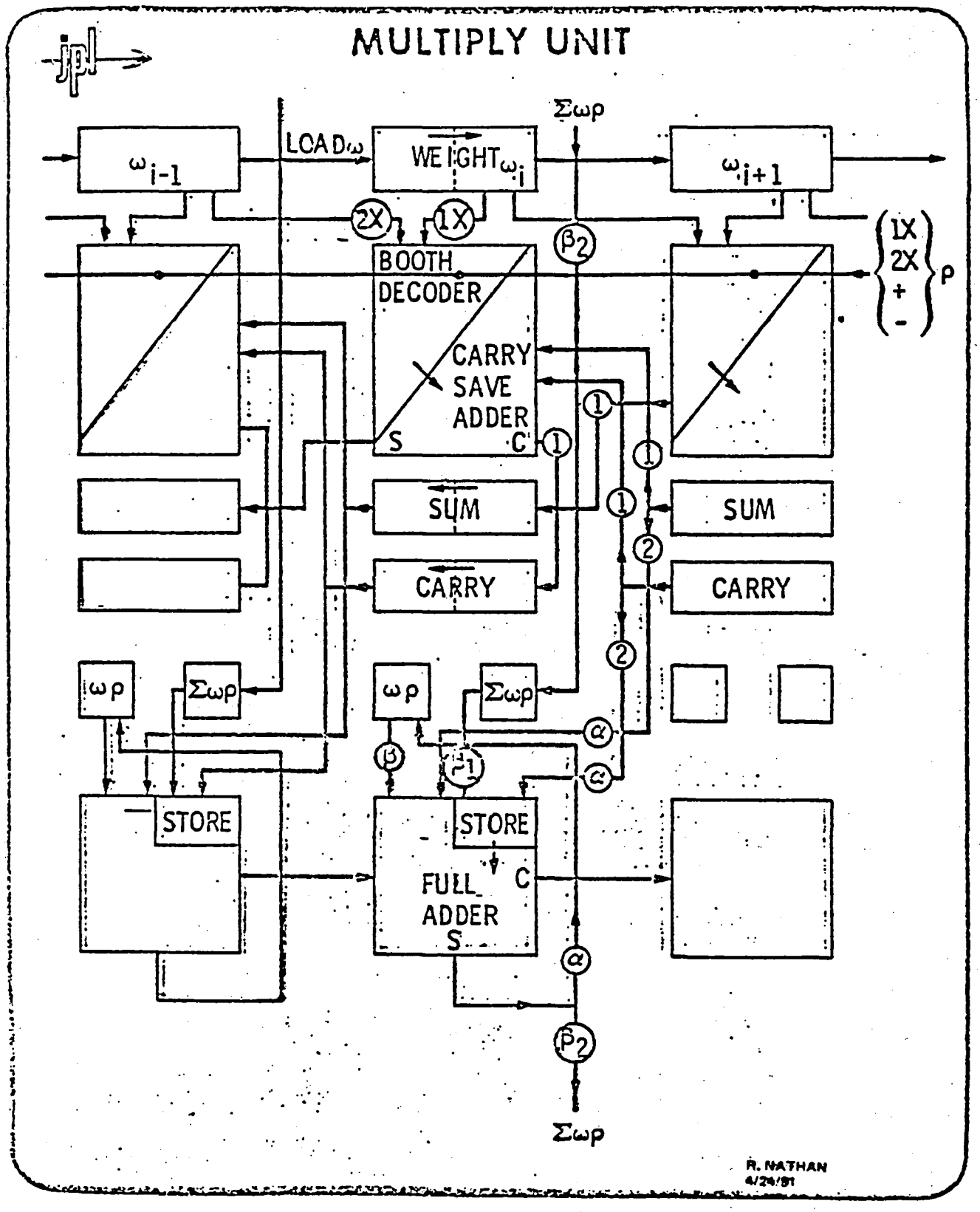


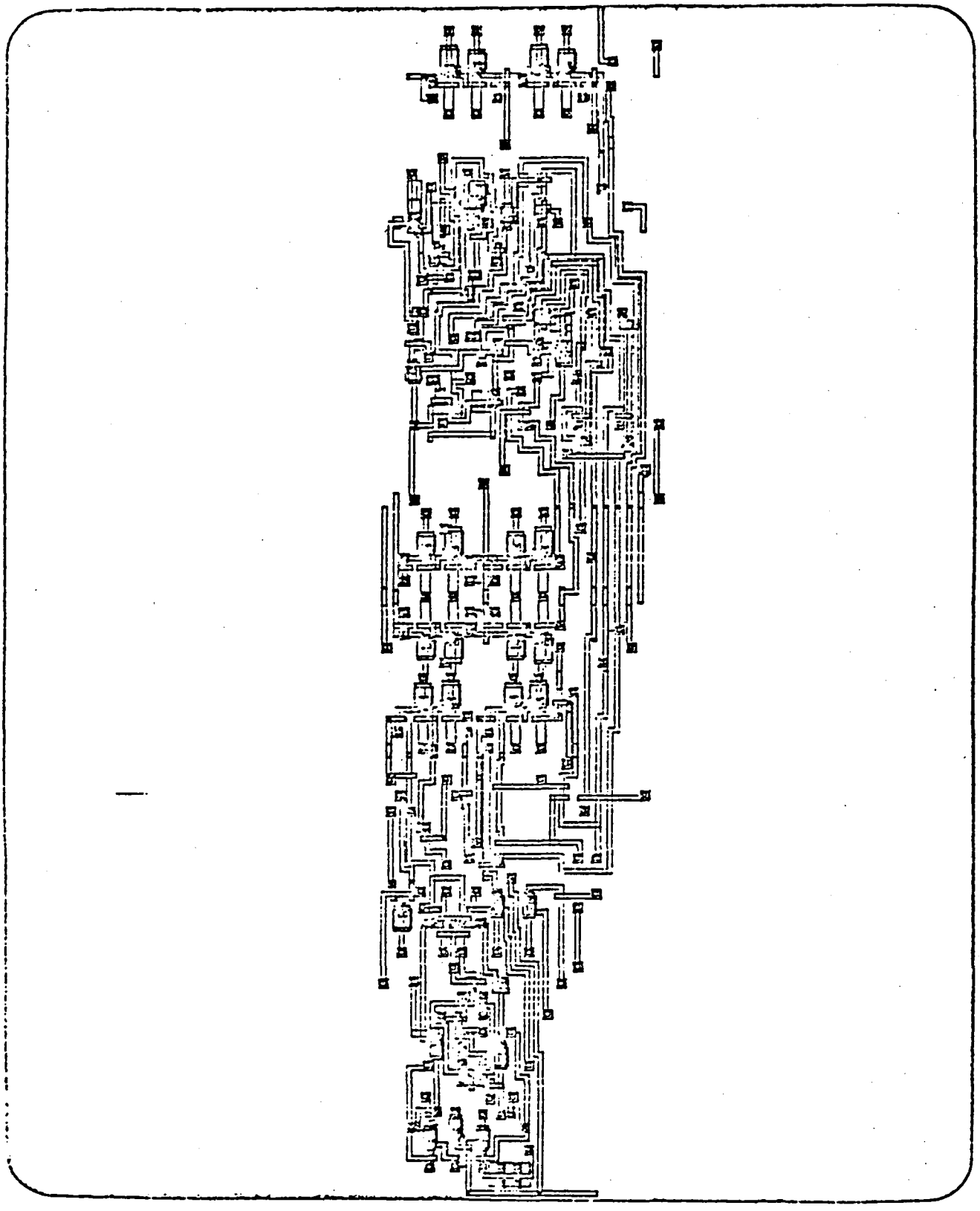
(b) Mask realization of one cell of the shift register cell.

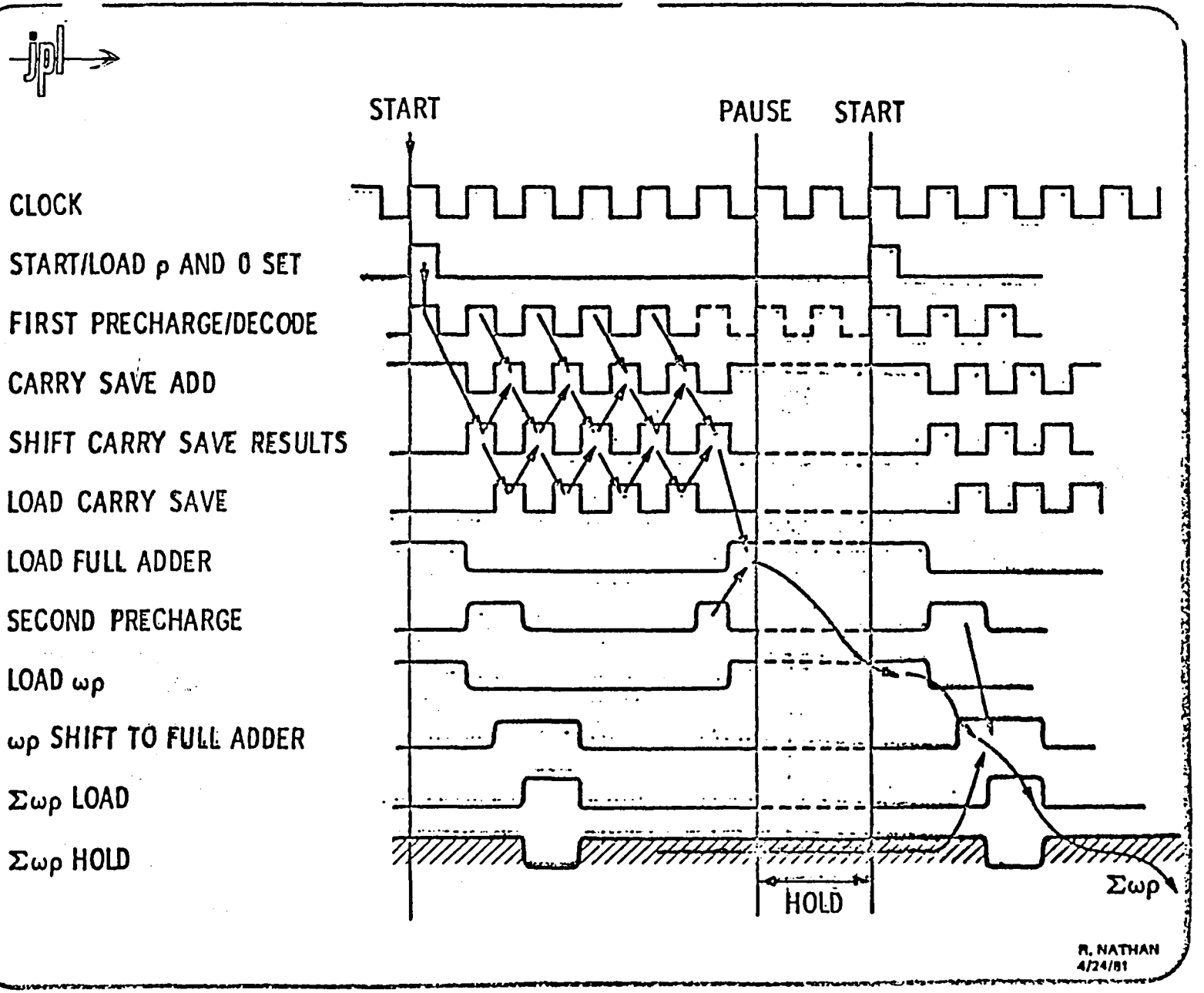
DIGITAL MULTIPLIER

- TYPICAL IC MULTIPLIERS CONTAIN REGISTERS FOR MULTIPLIER AND MULTIPLICAND OPERANDS.
- AN ADDITIONAL REGISTER IS PROVIDED FOR THE PRODUCT.
- MODERN LSI MULTIPLIERS PERFORM ADDITIONS IN A RIPPLE FASHION. THAT IS, EACH SUM IS PASSED ON FROM ONE ADDER TO THE NEXT WITHOUT THE USE OF CLOCKED SEQUENTIAL CIRCUITS. THEREFORE, THE MULTIPLIER IS COMPRISED OF AN ARRAY OF GATES AND ADDERS.



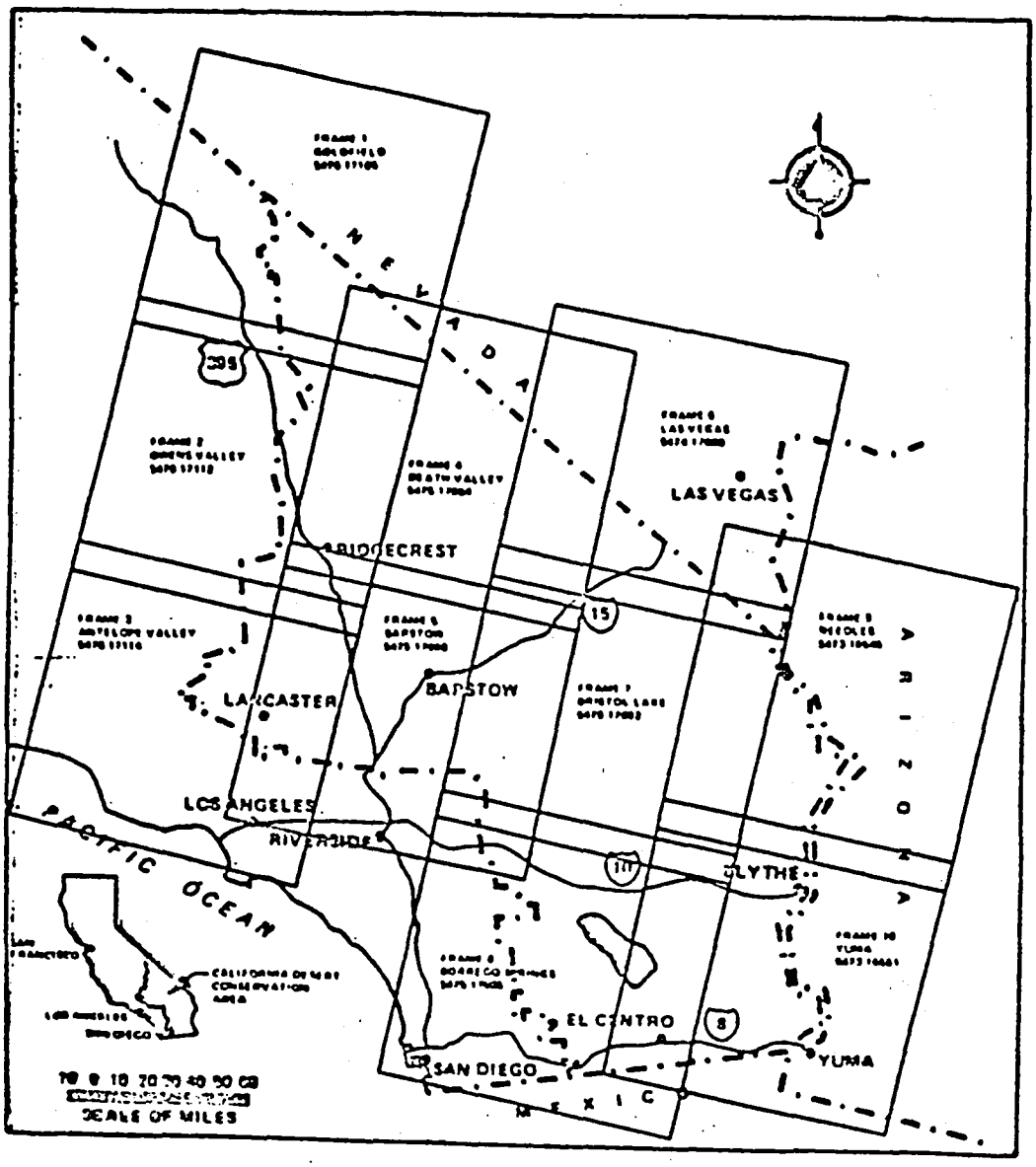

MULTIPLY UNIT
Σωρ
LOAD ω
WEIGHT ω_i
ω_i-1
ω_i+1
2X
1X
β2
BOOTH DECODER
1X
2X
+
-
ρ
CARRY SAVE ADDER
S
C
SUM
CARRY
ωρ
Σωρ
α
β
γ1
STORE
FULL ADDER
C
S
ρ2
R. NATHAN
4/24/81

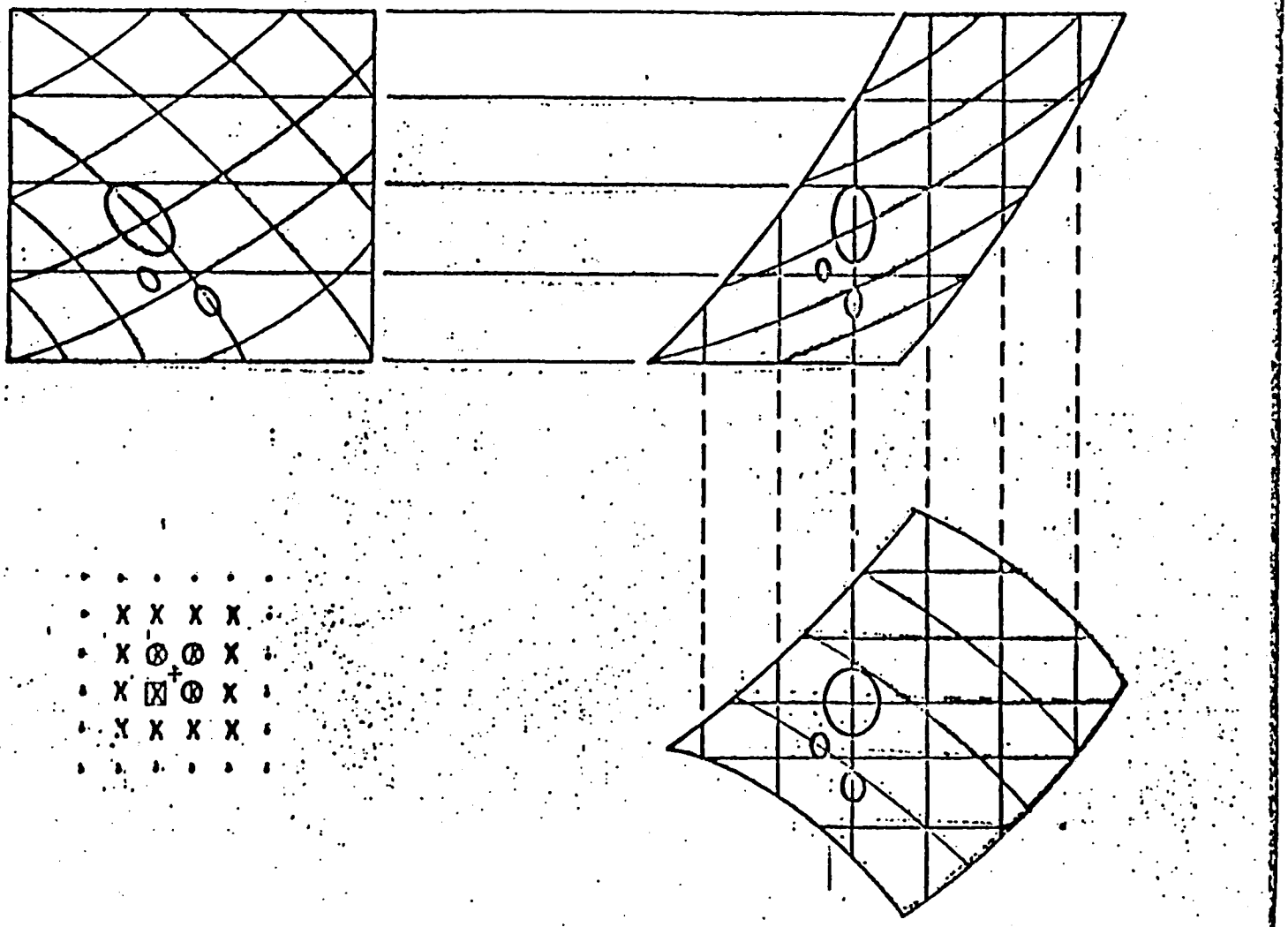



START
PAUSE
START
CLOCK
START/LOAD ρ AND 0 SET
FIRST PRECHARGE/DECODE
CARRY SAVE ADD
SHIFT CARRY SAVE RESULTS
LOAD CARRY SAVE
LOAD FULL ADDER
SECOND PRECHARGE
LOAD ωρ
ωρ SHIFT TO FULL ADDER
Σωρ LOAD
Σωρ HOLD
HOLD
Σωρ
R. NATHAN
4/24/81

BLM

BUREAU OF LAND MANAGEMENT
CALIFORNIA DESERT
CONSERVATION AREA
LOCATION OF LANDSAT SCENES





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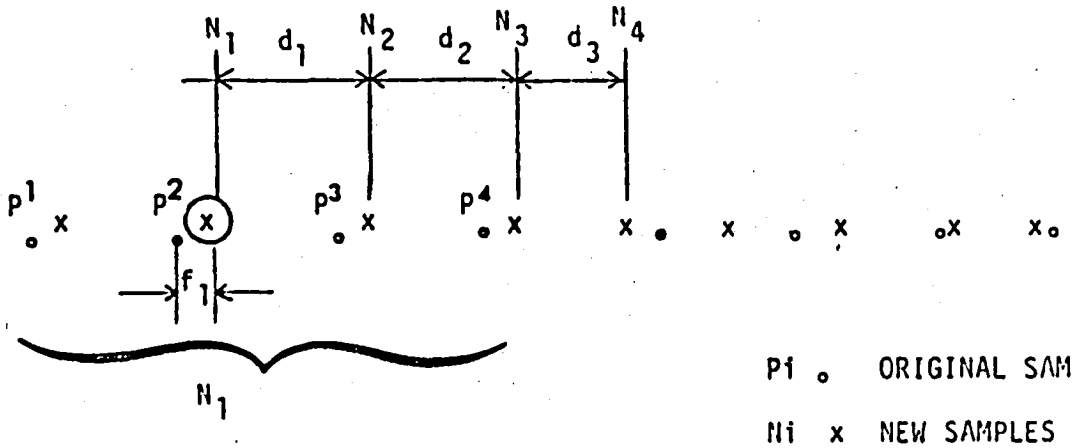
4/24/81

GEOMETRIC REPROJECTION

RESAMPLING



$N = p_1 w_1 + p_2 w_2 + p_3 w_3 + p_4 w_4$

Pi ∘ ORIGINAL SAMPLES

Ni x NEW SAMPLES

f FRACTIONAL DISTANCE BETWEEN POINTS

FOR LINEAR INTERPOLATION OF NEW SAMPLE VALUES

$$W_1 = W_4 = 0$$

$$W_2 = 1 - f$$

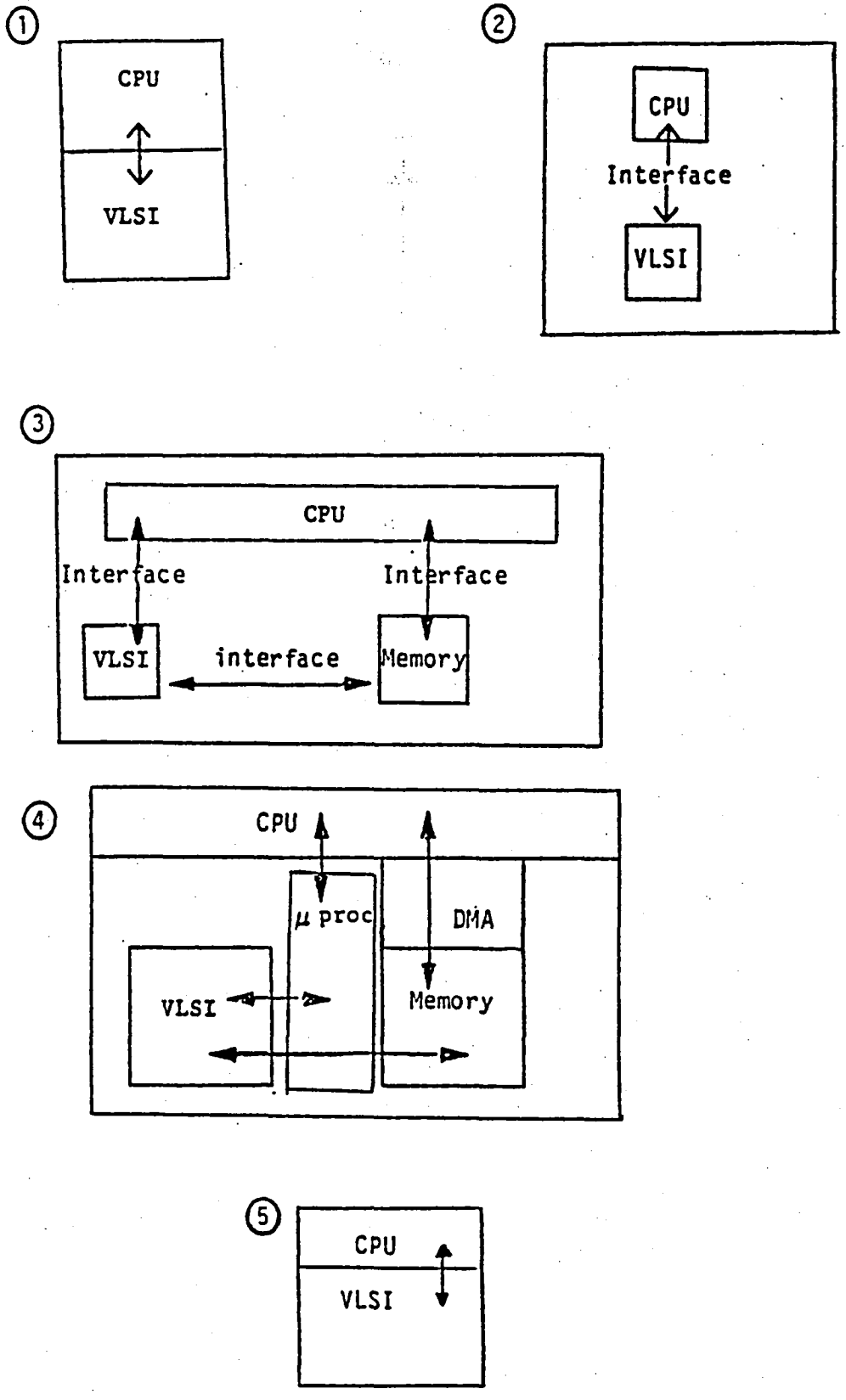
$$W_3 = f$$

THEREFORE $N_1 = P_2 (1-f_1) + P_3 f_1$

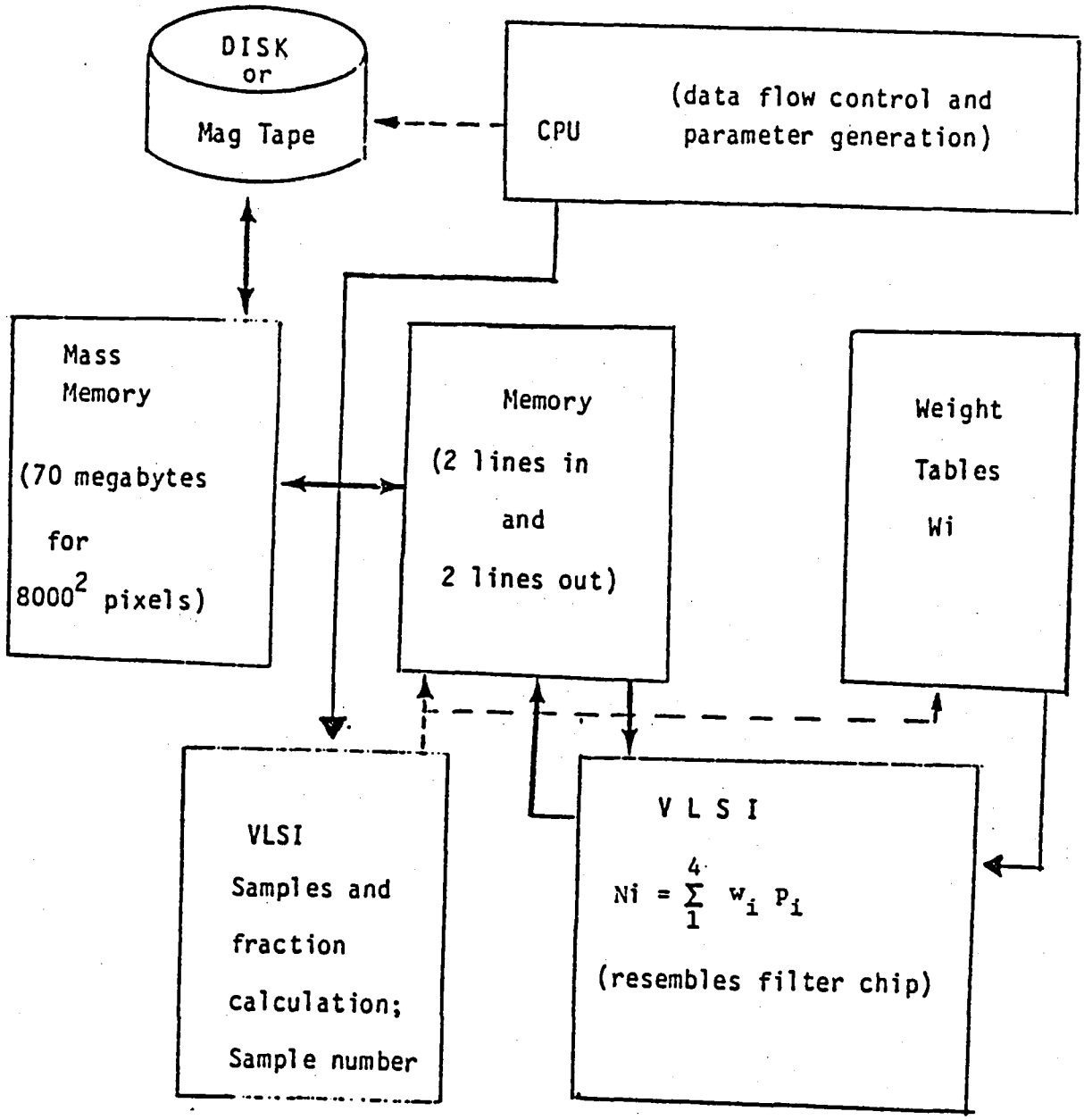
FOR CUBIC INTERPOLATION ALL FOUR Wi ARE A TABLE LOOK UP FUNCTION OF f_i.

THE NEW INTERSAMPLE DISTANCE (d) CAN ALSO BE NONLINEAR. ALLOWANCE IS MADE FOR CUBIC SPLINE ADJUSTMENT FOR NON-LINEAR SAMPLING.

RNATHAN
MARCH 1982

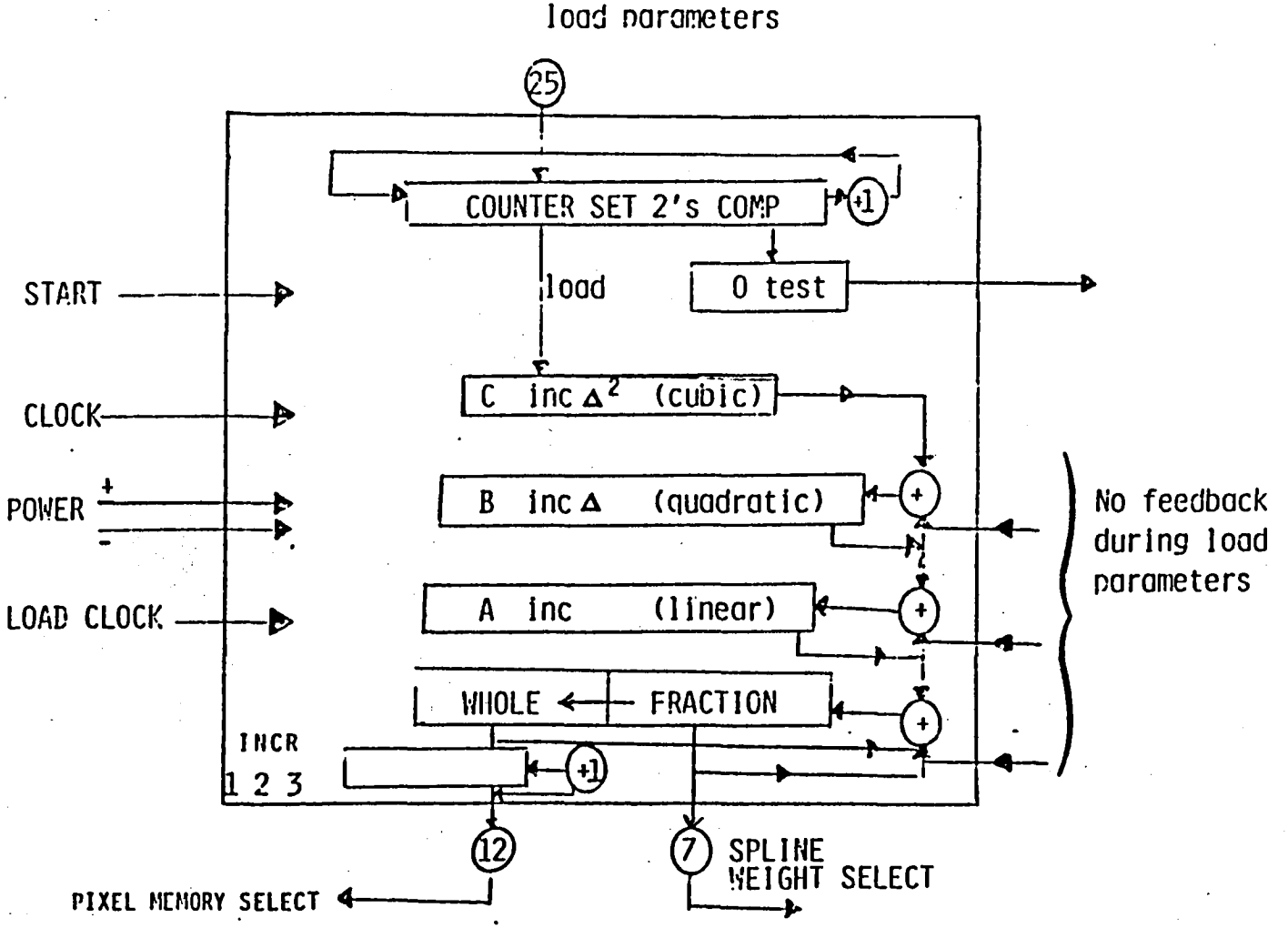


R.NATHAN
March 1982


DISK
or
Mag Tape
CPU
(data flow control and
parameter generation)
Mass
Memory
(70 megabytes
for
8000^2 pixels)
Memory
(2 lines in
and
2 lines out)
Weight
Tables
Wi
VLSI
Samples and
fraction
calculation;
Sample number
V L S I
$Ni = \sum_{1}^{4} w_i P_i$
(resembles filter chip)

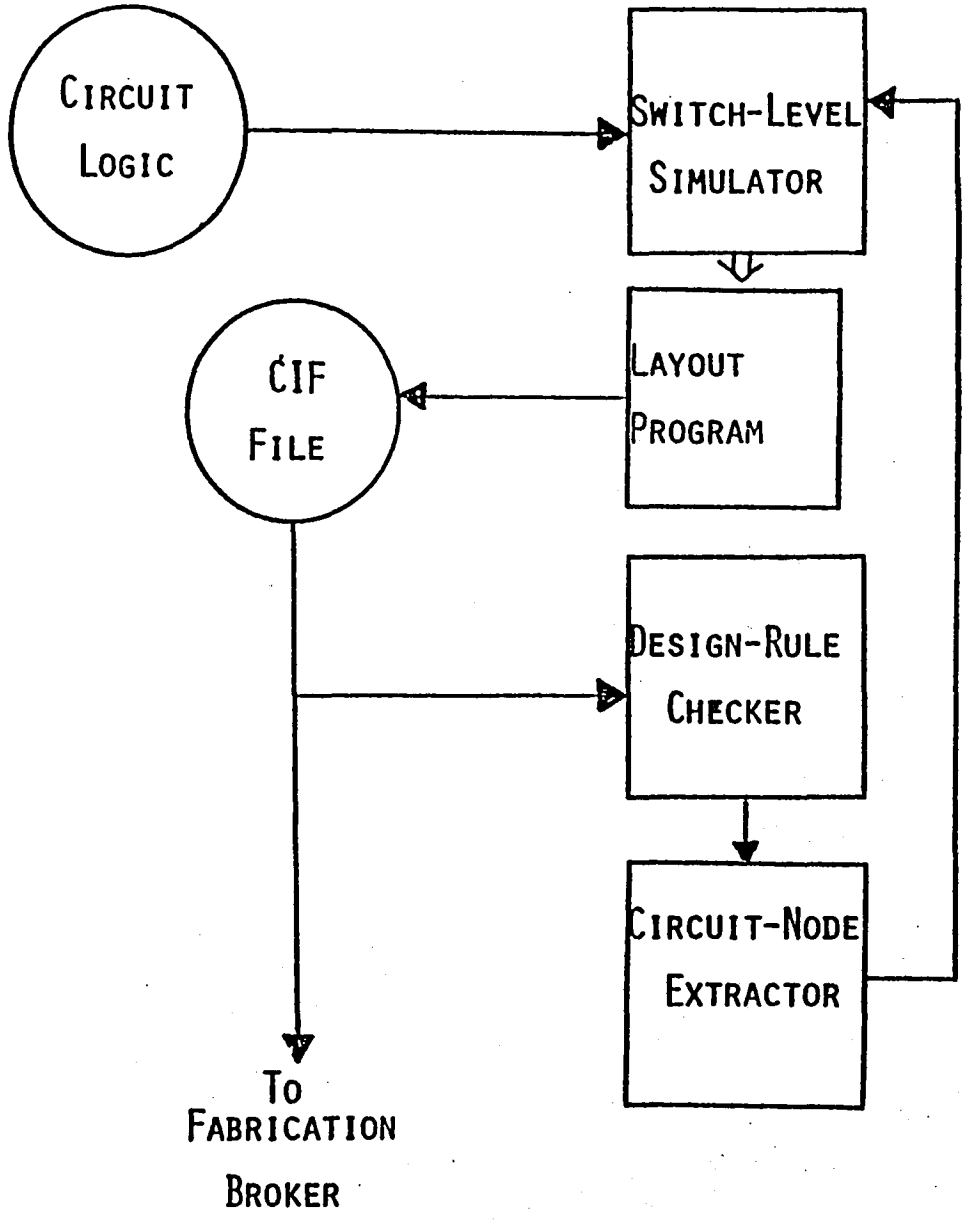
R.NATHAN
3/82

SELECT & COUNT



RNATHAN
MARCH 1982

FUNCTIONAL ELEMENTS OF CAMPUS DESIGN SYSTEM



NOTES:

1. AT JPL, SYSTEM WILL RUN USING MAINSAIL COMPILER ON VAX 11/780 WITH VMS OPERATING SYSTEM
2. SWITCH-LEVEL SIMULATOR IS BASED ON MIT WORK OF BRYANT AND TEMANS.

FUTURE

INDUSTRY DOES NOT WISH TO DEVELOP CUSTOM CHIPS

INTERESTED IN MASS MARKET

JPL AND OTHER USER INSTITUTIONS NEEDED TO

DEVELOP HIGH LEVEL SOFTWARE TO CONVERT

ALGORITHMS TO PARALLEL HARDWARE

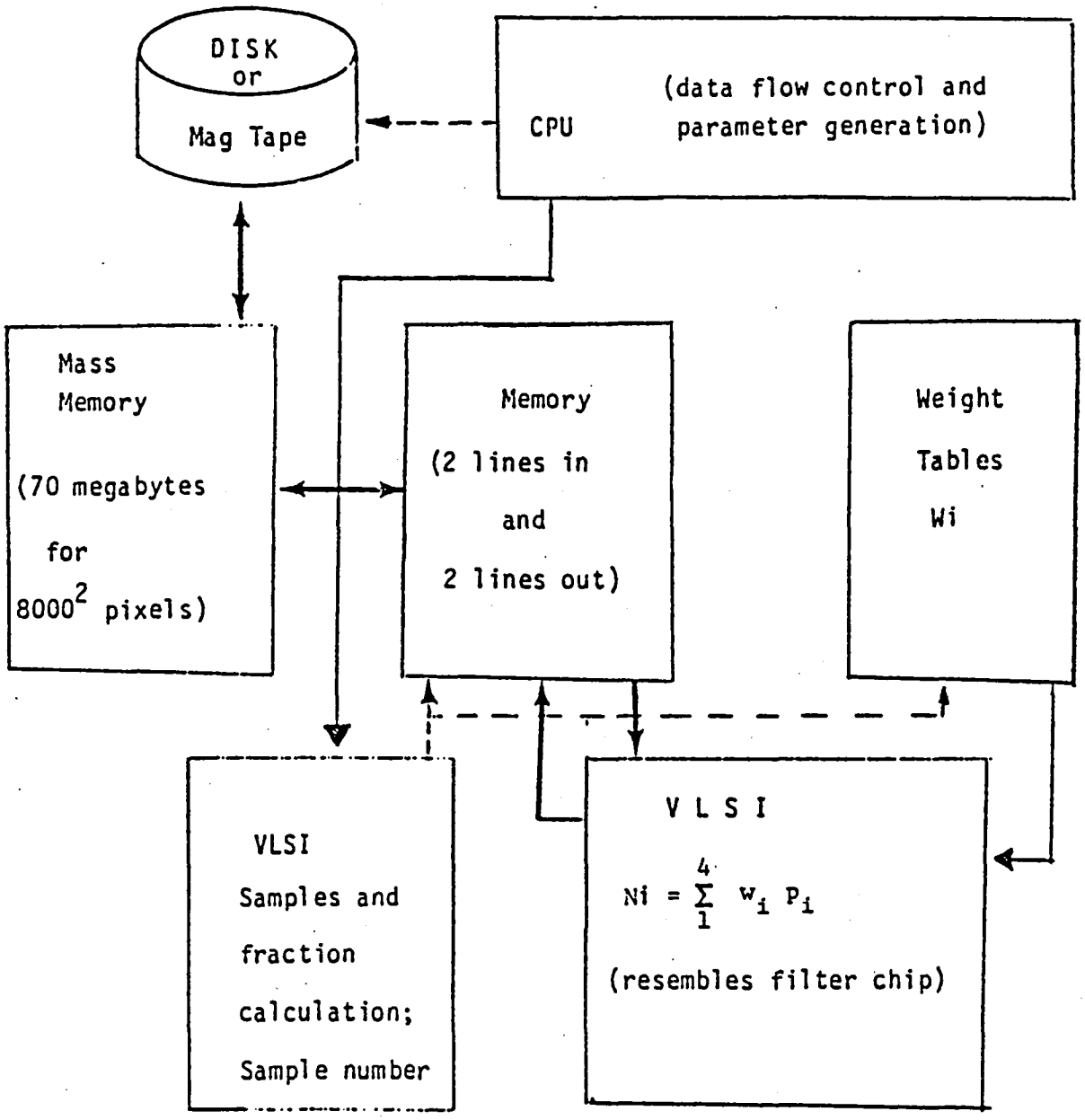
POTENTIAL APPLICATION AREAS

PATTERN EXTRACTION

SAR

I/O PARALLEL DATA FLOW

OTHER DATA BOTTLENECKS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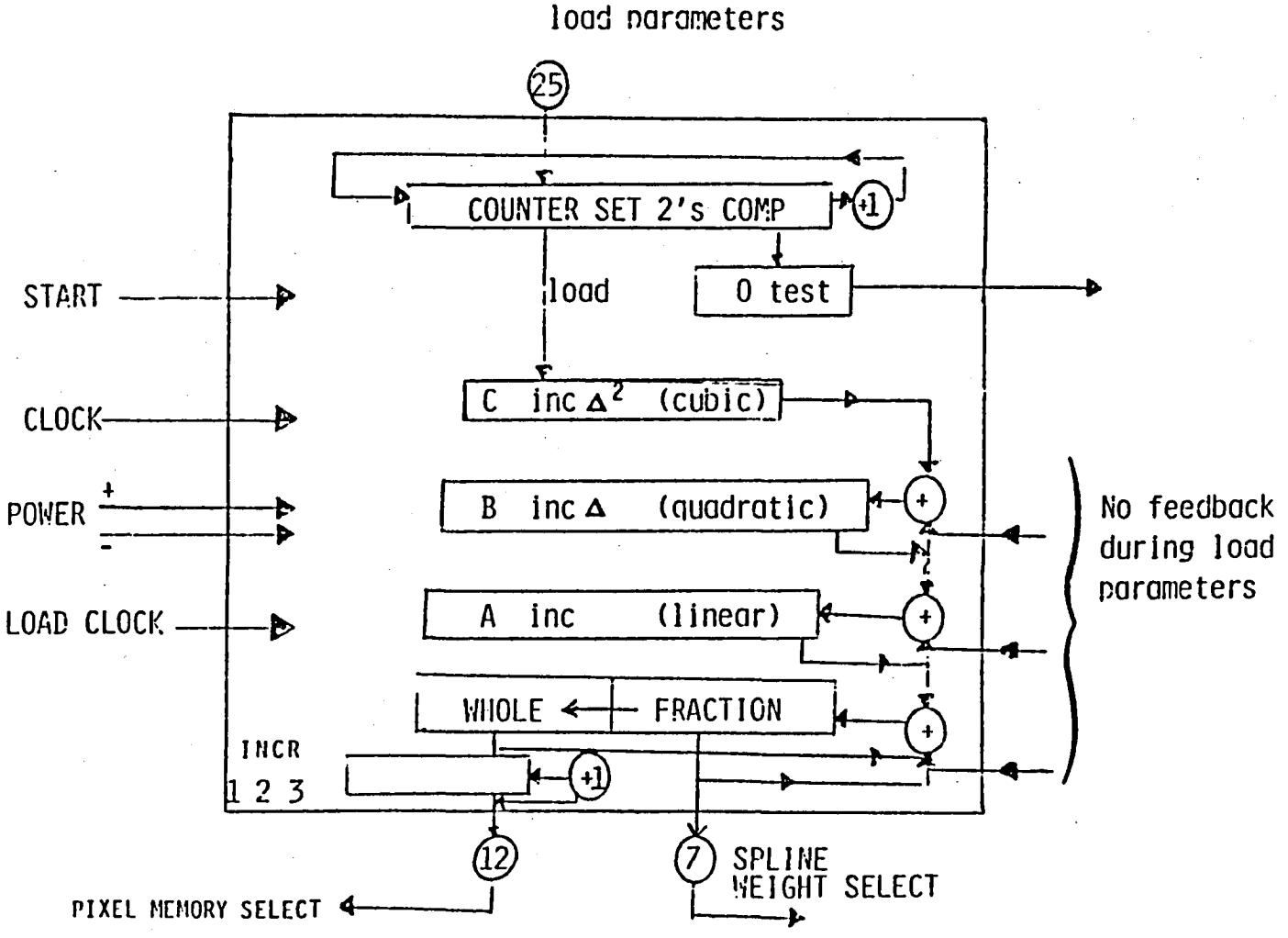
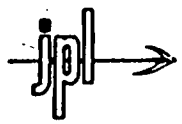


RNATHAN
MARCH 1982



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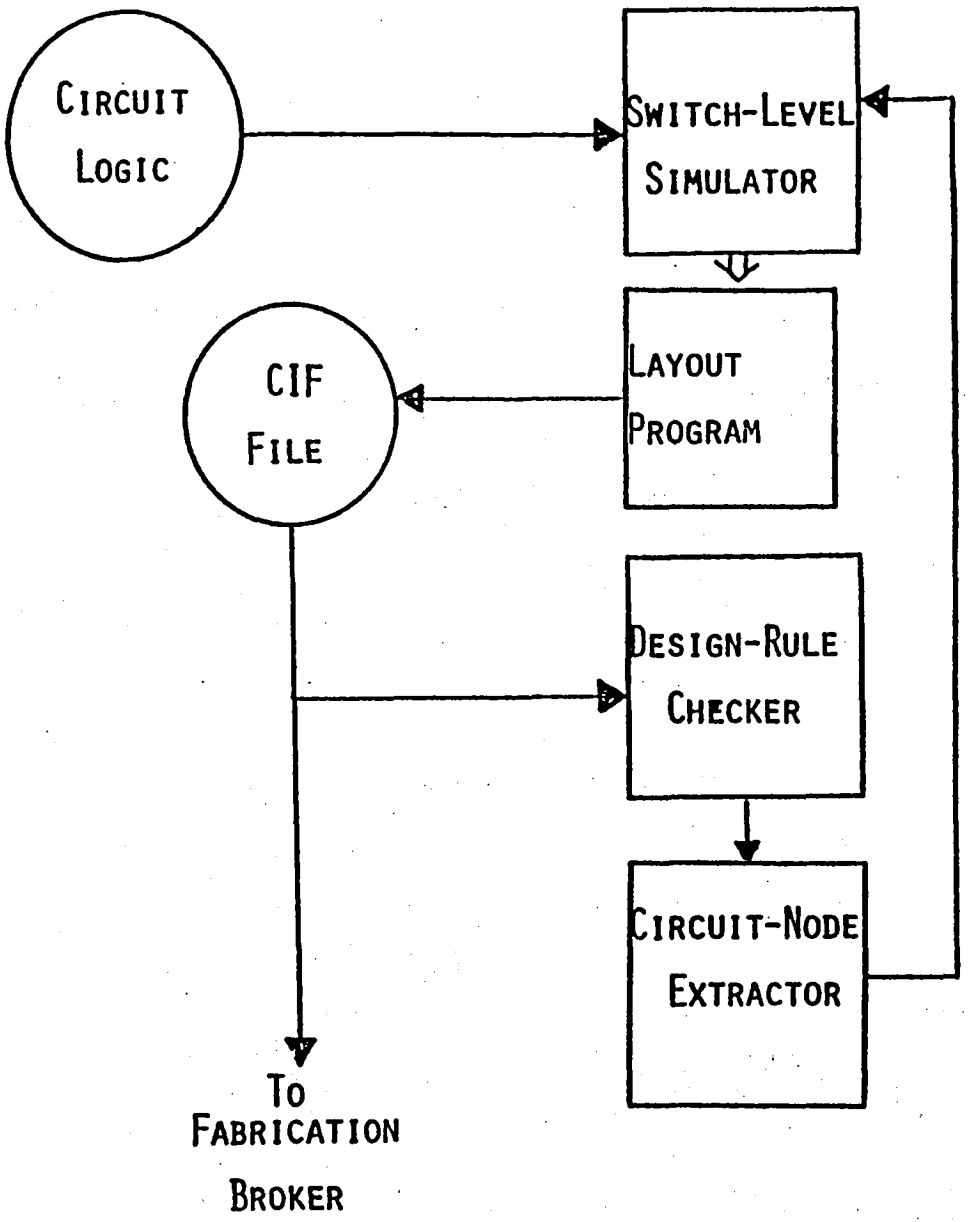

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MIXTURE PIXELS

P. SWAIN

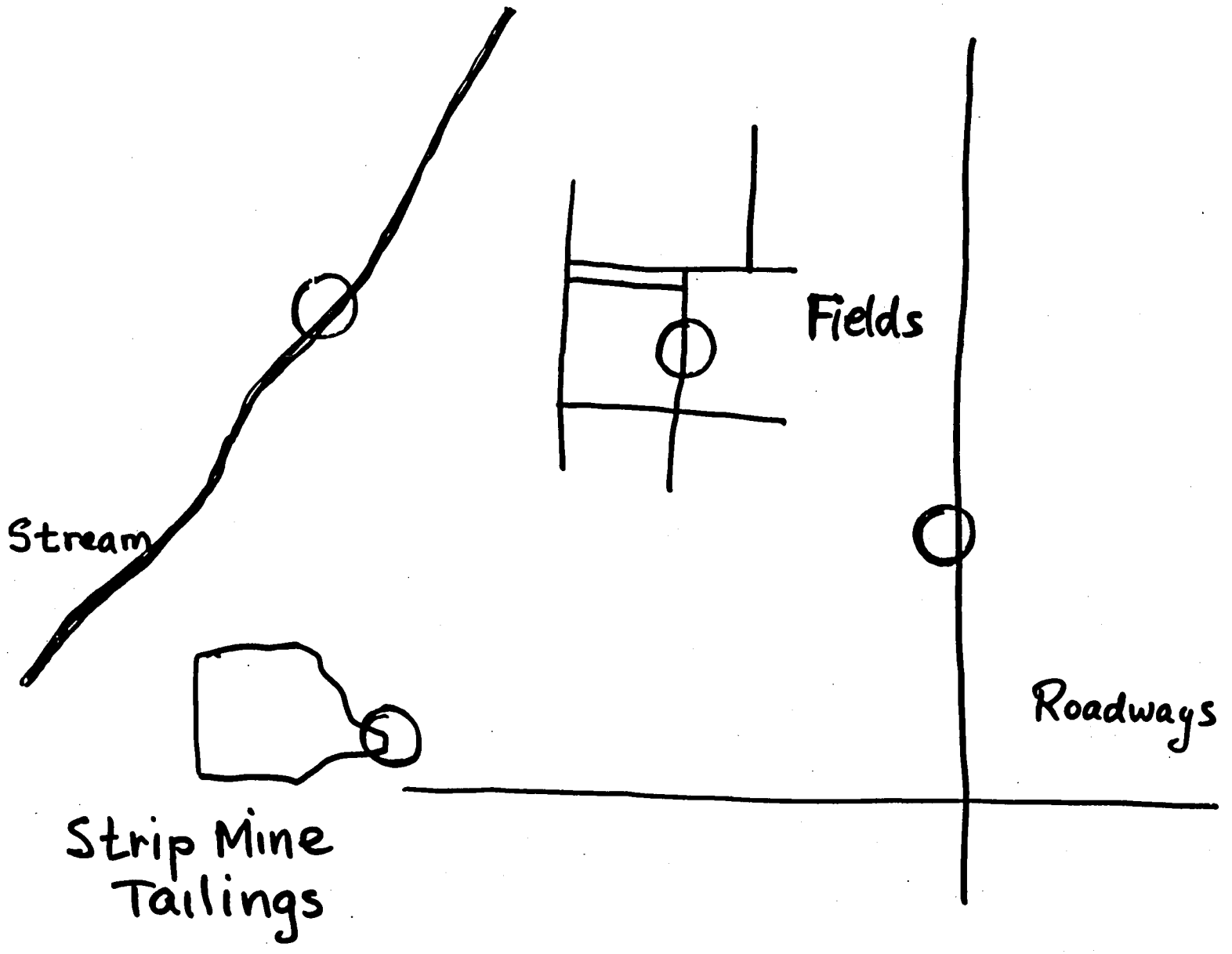
I. HISTORICAL PERSPECTIVE

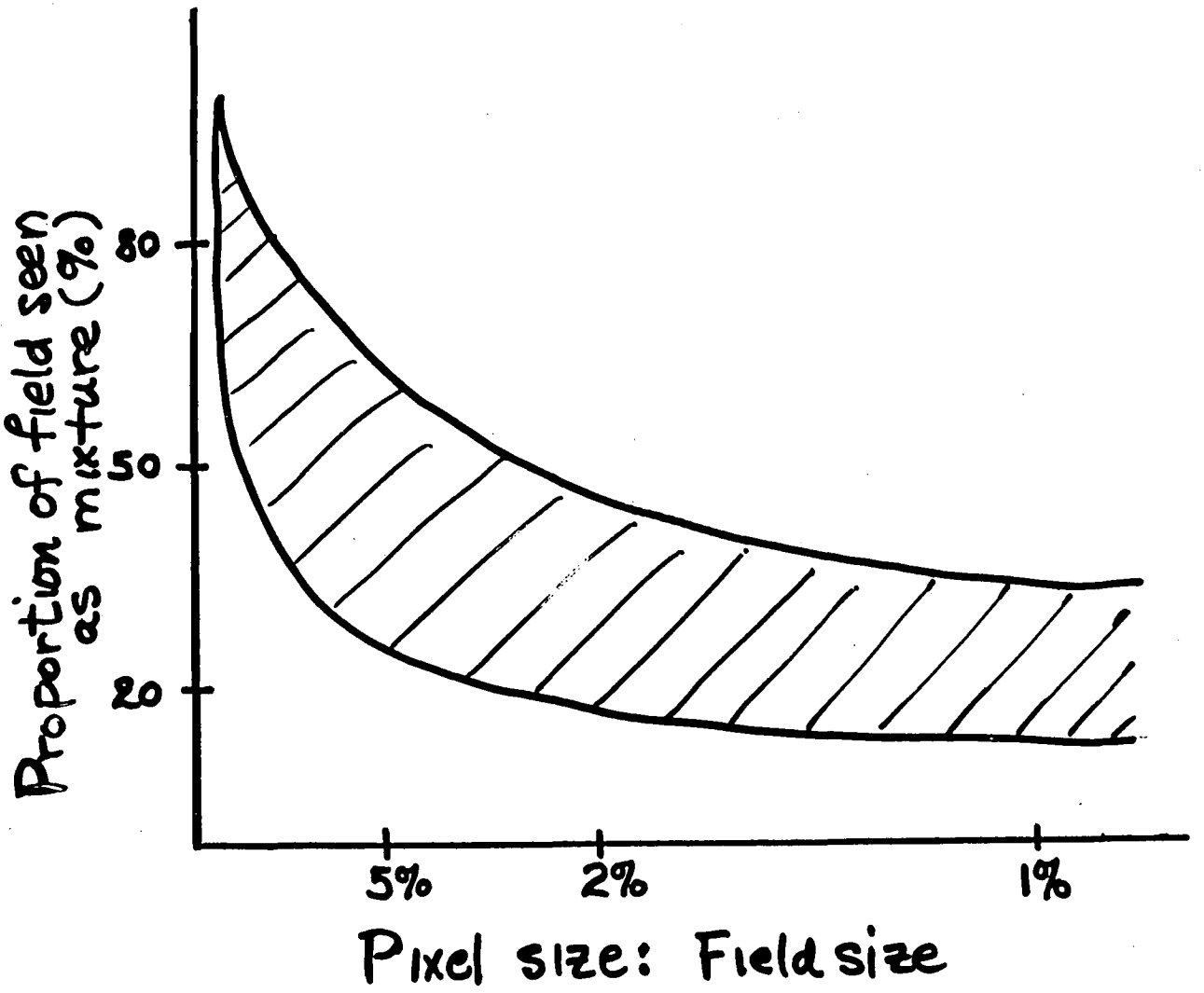
II. ORIGINS OF THE PROBLEM

III. INDUCED PROBLEMS

IV. APPROACHES TO SOLVING THE PROBLEM AND "STATE OF THE ART"

V. DISCUSSION: RELEVANCE IN THE PRESENT CONTEXT


Stream
Fields
Roadways
Strip Mine
Tailings



Adapted from Nalepka & Hyde (ERIM)