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REAL-TIME SIMULATION OF JET ENGINES WITH DIGITAL COMPUTER
1: FABRICATION AND CHARACTERISTICS OF THE SIMULATOR

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16. Abstract

The fabrication and performance of a real-time jet engine simulator using a digital computer are discussed. The use of the simulator in developing the components and control system of a jet engine is described. Comparison of data from jet engine simulation tests with actual engine tests was conducted with good agreement.

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Real-time Simulation of Jet Engines
with Digital Computer (I)
(Fabrication and Characteristics of the Simulator)

1. Preface

When dealing with jet engine control problems, the dynamic characteristics have to be determined as soon as possible. In actual control system tests, closed-loop tests are usually performed using a simulator to approximate the engine's dynamic characteristics before testing the actual engine prototype. This requires a simulator that approximates real conditions and operates in real time.

Faster engine development times are mandatory in today's environment and the design and testing of control systems must take place during the course of development and in parallel with the engine development schedule. This is why high precision simulators have to be used in control system design so that the engine's static and dynamic characteristics can be simulated. Computer simulation uses component characteristics and engine component test data that are knowable in the engine design phase.

After obtaining test results on the JR100 lift engine, we published a report on methods of computing an engine's dynamic characteristics (shown by transfer function) from its static characteristics.[1] The present report examines the second phase of those tests, tests performed in real-time simulation of engine characteristics and devices fabricated for that purpose.

2. Simulating Engine Characteristics

There are numerous reports on simulation of engine characteristics. Some simulation techniques use analog computers while others use digital computer methods. But the simplest use the primary delay shown in Figure 1.

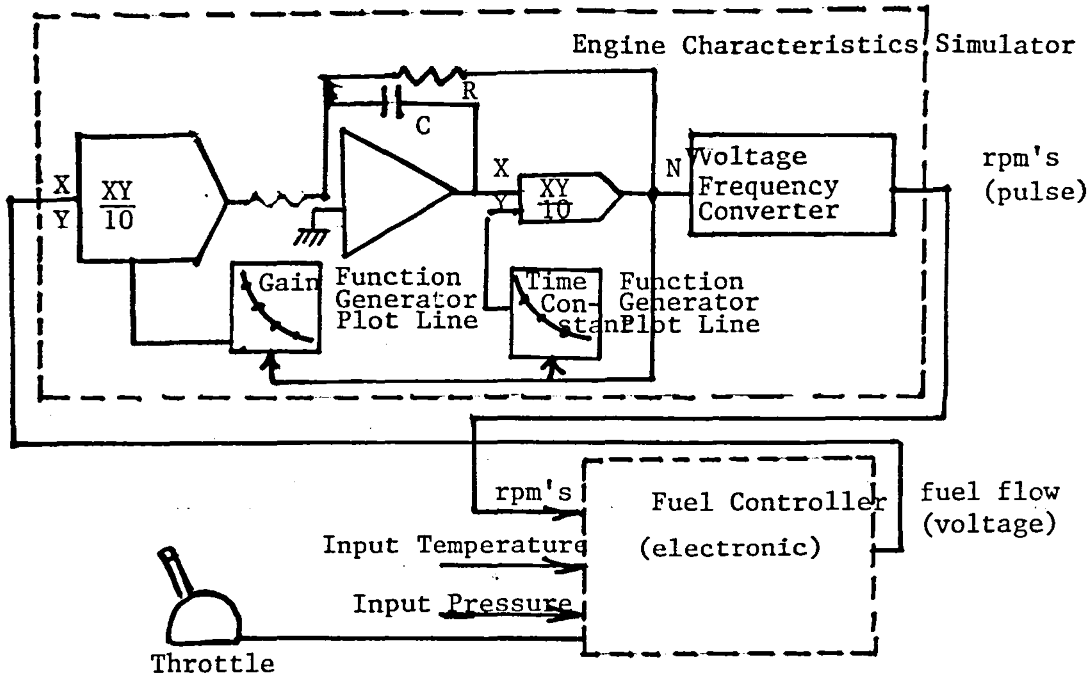


Figure 1 Test by Simulation

The dynamic characteristics of the engine can be expressed in the form:

$$\Delta N_c(S) = \frac{K_E}{1 + T_E S} \cdot \Delta W_{fc}(S)$$

$$\begin{cases} T_E = -I\sqrt{\theta_2} \Big/ \left(\frac{\partial Q_c}{\partial N_c}\right) \cdot J \cdot \delta_2 \\ K_E = -\left(\frac{\partial Q_c}{\partial W_{fc}}\right) \Big/ \frac{\partial Q_c}{\partial N_c} \end{cases}$$

Here

Nc......engine rpm (subscript c is the corrector)

Wfc.....fuel flow

Qc......excess torque

θ_2......ratio of compressor intake temperature to standard temperature

δ_2......ratio of compressor intake pressure to standard pressure

As the JR100 example in Figure 2 shows, the gain and time constant of the transfer function are expressed by the rpm function and thus, they are derived as function generator rpm input and assigned as time constant and gain of the primary delay circuit. This simulation is extremely general, but, even then we have obtained highly practicable data for ground tests of gas turbines or engines

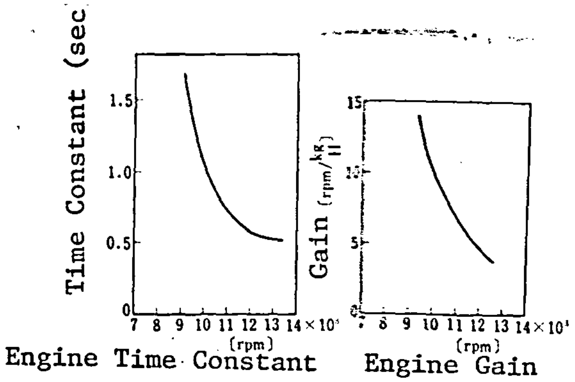


Figure 2 JR100 Transfer Function

which are components of larger systems, such as high performance control VTOLs. In addition, all types of tests are being made both in Japan and abroad, and those test methods can be classified into two major categories, simulation by analog computer and by digital computer.

Most representative of analog computer test simulations are those conducted at the University of Michigan.[2] Figure 3 shows a schematic diagram of a turboshaft engine simulation.

The distinctive feature of this simulation is that logarithms are fed into the arithmetic/logic operation circuits and it avoids the use of a multiplier which would be a source of noise. In addition, devices are being constructed to closely approximate characteristics, such as those of compressors, using 2-input, 1-output function generators and servos. Those devices have large configuration containing, overall, 60 arithmetic/logic operational amplifiers, 10 function generators and four 2-input function generators. Such large-scale devices are not always easy to use due to the need for adjustment, noise processing, and prevention of oscillation. Although the device is good in many respects, it has deficiencies in reproducibility and precision.

The digital method is best for simulation of systems, such as jet engines, assembled from components, the dynamic characteristics of which are indicated by non-linear multi-variable functions. Digital simulation of such systems is conducted primarily in Great Britain. The simulation is used chiefly to clarify dynamic characteristics, but operating time is lengthy and the simulation is not expressed in real time.

Saravanmuttoo, et. al.,[3] have simulated single- and dual-engine performance and examined acceleration-deceleration time characteristics on a compressor map locus. Because this calculation method repeatedly matches pressure and gas flow of an engine in optional state and continues its derivations in minute detail, computer time for single-engine simulation, reportedly, is 50 times real time and 200 times real time for dual-engine simulation and computer memory capacity is more than 10K words.

3. Real-time Simulation of Engine Characteristics

Requirements on control device and engine conformance are becoming stricter as engine performance increases. Satisfying the relationship between engine input (fuel flow) and output (thrust or rpm's) is considered adequate with conventional, simple simulators. However, the conventional simulator will not meet today's stricter specifications. High performance and operations in real time are required of simulators to investigate conformity between control system and engine. We also have to have output on the quantitative status of each component.

The following plans have been made in view of the strong demand for hybrid (analog/digital) simulators which operate in real time and can be used for control system simulation and electronic control system design.

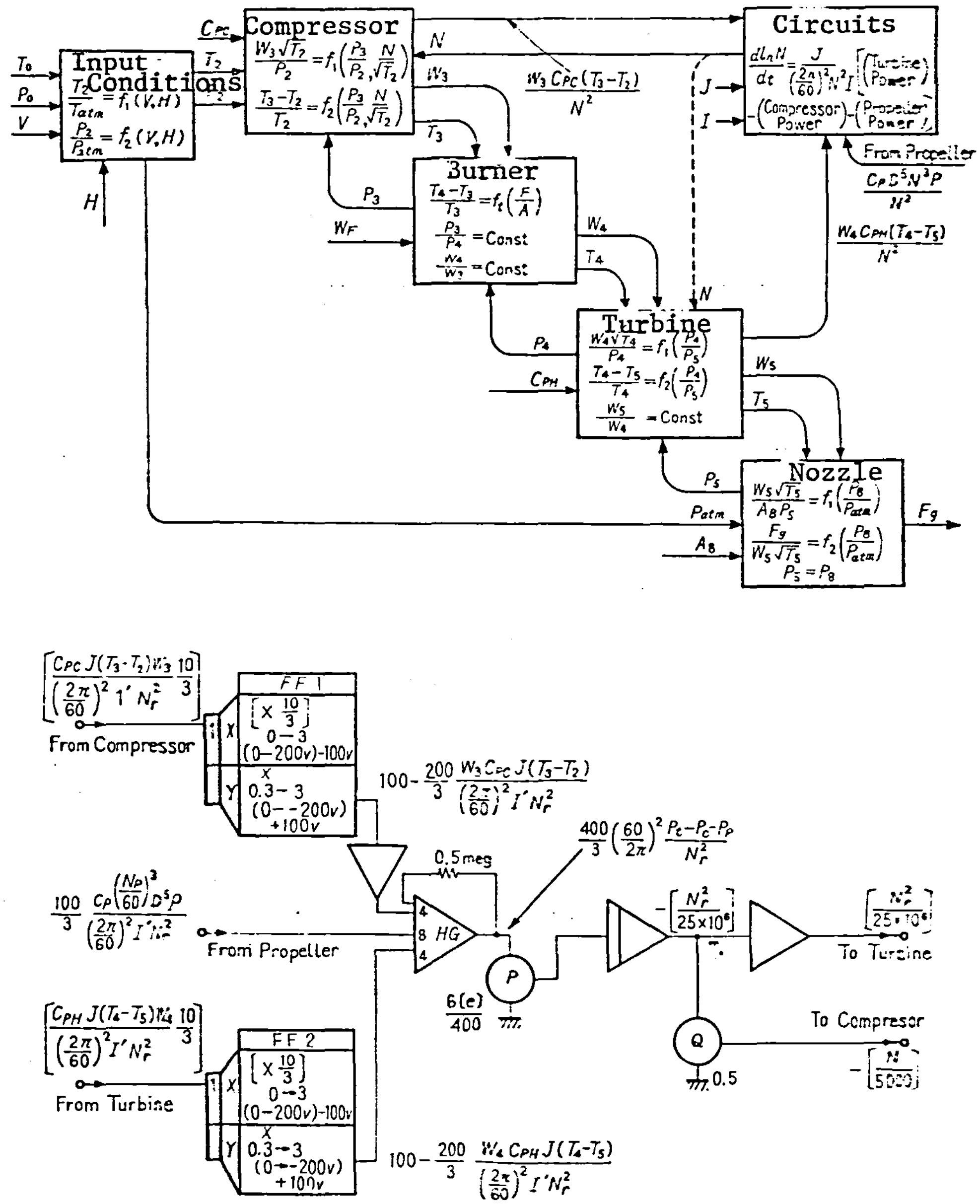


Figure 3 Simulation of Rotor Characteristics

(1) Perform operations in real time.

(2) Specify simulator input such as fuel flow and environmental conditions in analog signals.

(3) Compute simulator output such as thrust, rpm's, pressure on all components, temperature variants and gas temperature in digital and then output in analog.

(4) Make simulation highly reproducible and precise. Have dynamic and static characteristics of the engine conform to actual measurements.

(5) Set a precision target of ±0.1% for each unit of the analog arithmetic/logic operation unit used in the design of engine control systems and add theoretical circuits for theoretical design.

(6) Use a modular mode arithmetic/logic operational amplifier in the analog arithmetic/logic operation unit. Control of arithmetic/logic operations can also be performed by digital computer.

(7) Use a mini-computer for overall control of the digital computer unit.

(8) Be able to display on CRT screen, the characteristics of each component in the engine.

The above is considered to be the general simulator concept. We plan to use a hybrid system that combines analog and digital computation. The distribution is such that the majority of initial simulation computing is performed on a digital computer and only those items of integration in which the time factor enters are performed on analog.

Since the actual results of setting up a program and performing tests showed recognizable inadequacies in simulator stability related to integrator precision, stability/sample and time, we decided to use a digital computer for integration items too. For I/O relations and for engine control system unit we used analog computer.

The simulator consists of the following units:

(1) Digital arithmetic/logic operation unit

(2) Analog arithmetic/logic operation unit

(3) I/O interface

(4) Display

Figure 4.5 shows an external view of the system.

In actually configuring the simulator, we tried, as much as possible, to use existing components effectively. For the digital arithmetic/logic operation unit, we used the NEAC-3200-50 which is usually employed in high temperature turbine measuring instruments. For the arithmetic/logic operational amplifier in the analog arithmetic/logic operation unit, we used a device for engine measurement and high performance jet engine control research. We designed and fabricated a new I/O interface in light of the goals of a real-time simulator and because data I/O should be performed as quickly as possible. We achieved high speed by changing over to an AD converter that has a 20-microsecond conversion time. This hardware will be discussed in further detail in Section 5.

4. Simulator Program

Time required for computing must be known in advance in order to operate a digital simulator in real time. In this simulation, numerical integration is the process (process in which time is an independent variable) relating time. The time range from the start of computing, by data input specification, to output, is the integrating range of numerical integration. When the range of computing time and numerical integration are the same, the simulator is a real-time simulator, in all other instances, the time range is shortened or expanded.

The time required for digital computer calculation varies generally according to data mode even if the same program is used. Since we have no elapsed timer with which to precisely know the time required for normal computation, computer operations must be timed using a fixed time range known in advance. Such timing can be implemented by applying a pulse of fixed period to the computer interrupt line. Figure 6 shows the operations required. If interrupt sampling time is greater than the predicted maximum time from start to end of external input, calculation and external output operations, input will be read in a fixed time range and output obtained.

Figure 7 shows the simulator program configuration. The two chief components of the simulator program are based on actual measured characteristics of each engine component. They are: non-linear simultaneous equation operations to match pressure and flow and first order differential equation operations which use results from the non-linear simultaneous equation operations to derive torque, perform numerical integration and calculate rpm.

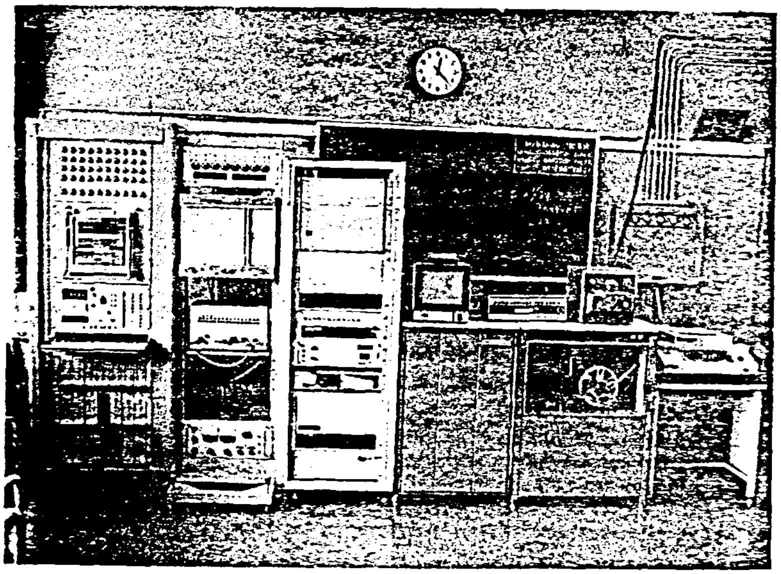


Figure 4 Engine Characteristics Simulator

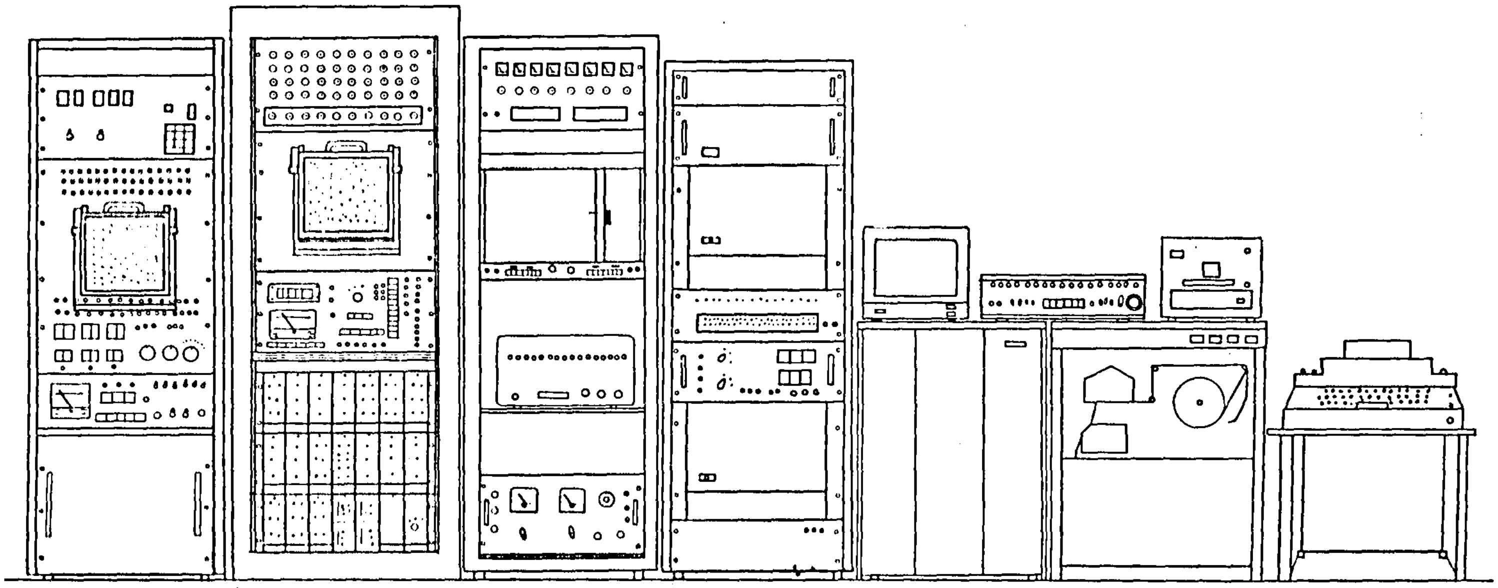


Figure 5 External View of Simulator

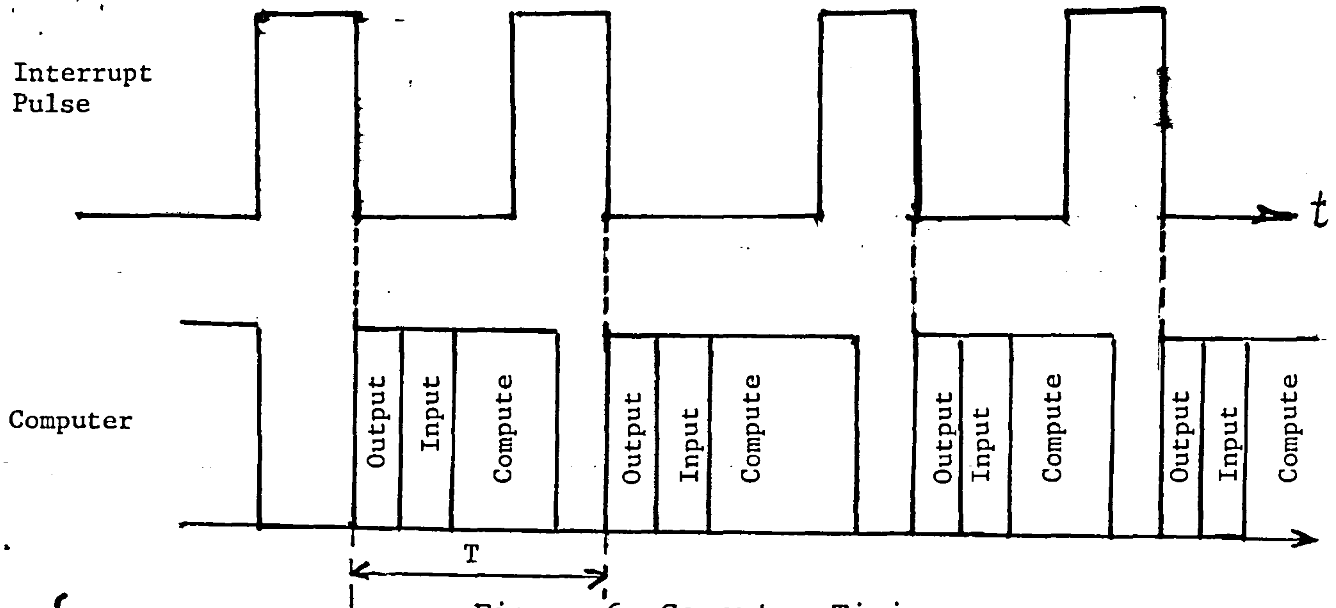


Figure 6 Computer Timing

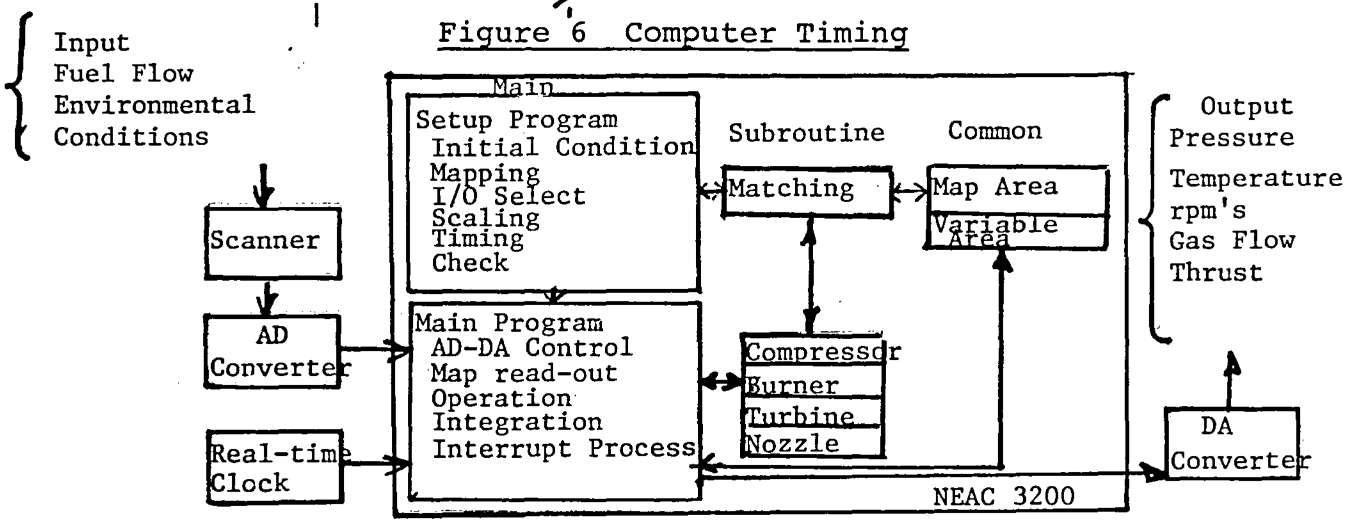


Figure 7 Simulator Program Configuration

The methods of solving non-linear simultaneous equations are numerous. All require many repetitive calculations which mean increased computer time. So, before performing simulation operations, we use a method of matching calculations on corrected fuel flow and corrected rpm combinations. We then store the resulting turbine pressure ratio in memory. The simulator can reference memory for optional input values and initial values and it can compute without repeatedly calculating other status variables.

When operating the computer in real time, computer time determines the step-size of numerical integration. When using high-powered computer methods (Runge-Kutta Method, Adams Method, etc.) to perform extremely precise numerical integration, computer time and computing instability greatly increase. And, if input values in the integration range rapidly change, abnormal values will be produced and when those values are used in the simulator poor conditions will result. Since the engine time constant, even if low, will be on the order of 0.4 seconds, using numerical integration (linear approximation integration) of the oiler for a step-size of several microseconds or several tens of microseconds will give good stability and adequate precision.

We will now show an example of this method where simulation was performed on the JR100H lift jet engine. Figure 8 shows the characteristics of the components in the JR100H that was used. We created two program formats, one in FORTRAN, the other in assembler language. The floating point method was used for arithmetic/logic operations in the former, the fixed point method, in which status variables were normalized, was used in the latter. The ratio of computing time for both was 20:1.

Figure 11 is a flow chart of simulation, and subroutines were created for each component category based on the data on JR100H component characteristics in Figures 8 to 10.

The subroutines are multi-dimensional approximation expressions. Their values are derived by the methods described in item 4 in the bibliography.

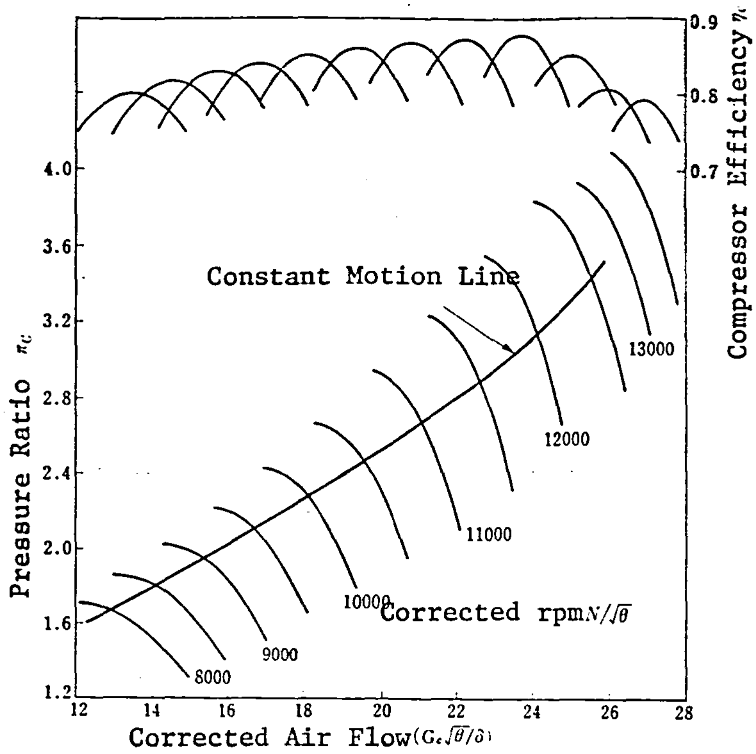


Figure 8 JR100H Compressor Characteristics

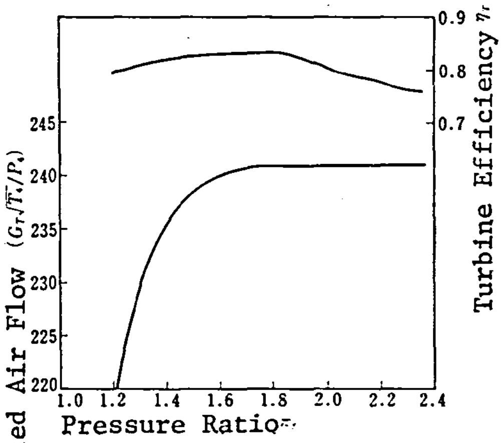


Fig. 9 JR100H Turbine Characteristics

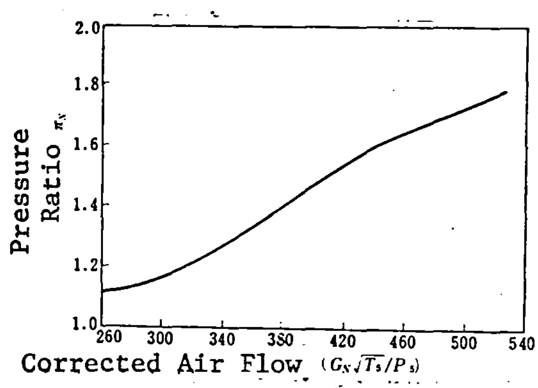


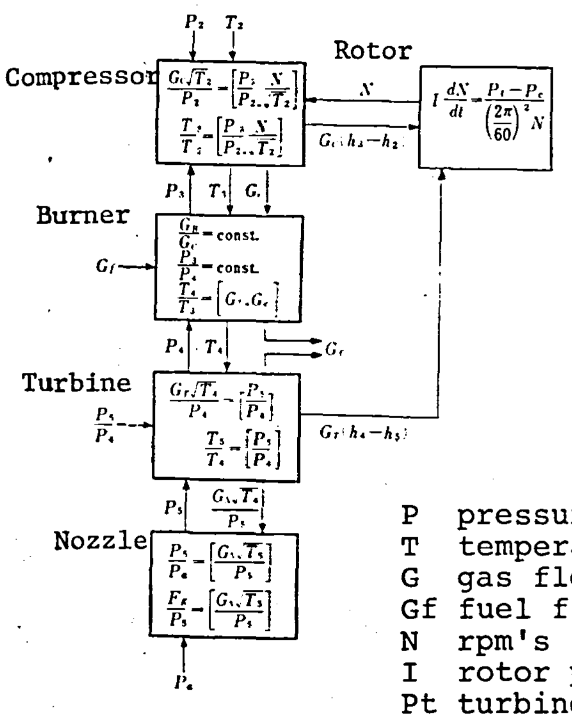
Figure 10 JR100H Nozzle Characteristics

In the method of matching computation, we first postulated the turbine pressurization P_4/P_5, then calculated the status variables for each component to derive turbine gas flow. Because this gas flow is not equivalent to the gas flow derived directly from P_4/P_5, P_4/P_5 was corrected to reduce the difference. This was repeated to derive the matching value.

Table 1 Component Subroutine I/O

Subroutine	Input	Output
Compressor	$N/\sqrt{\theta}$, z_c	$G_c\sqrt{\theta}/\delta$, T_3/T_2, η_c
Turbine	P_4/P_5	$G_T\sqrt{T_4}/F_4$, η_T, T_4/T_5, $G_N\sqrt{T_5}/P_5$
Nozzle	$G_N\sqrt{T_{04}}P_5$	P_a/P_5
Thrust	P_a/P_5	F

θ: ratio of standard temperature to compressor intake temperature
δ: ratio of standard pressure to local pressure
ηc: compressor efficiency
ηt: turbine efficiency
Gc, Gt, Gn: gas flow in each unit
F: thrust
Pa: atmospheric pressure



P pressure
T temperature
G gas flow
Gf fuel flow
N rpm's
I rotor pole moment of inertia
Pt turbine generated torque
Pc compressor intake torque
h enthalpimetric

Figure 11 Simulator Flow

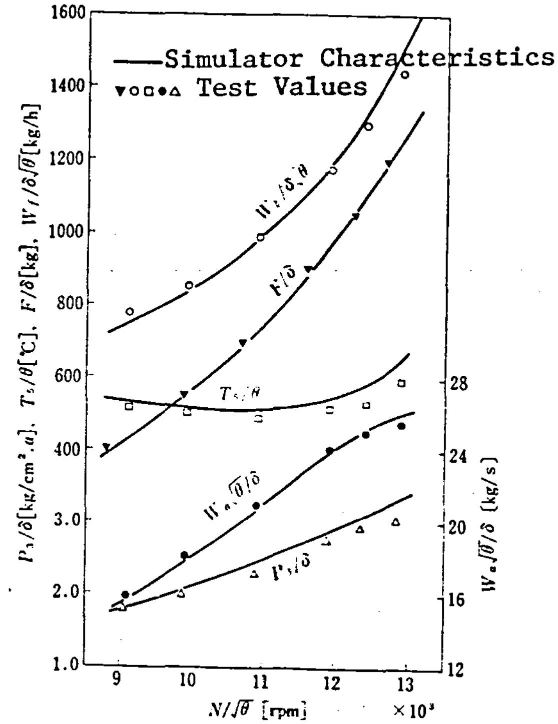
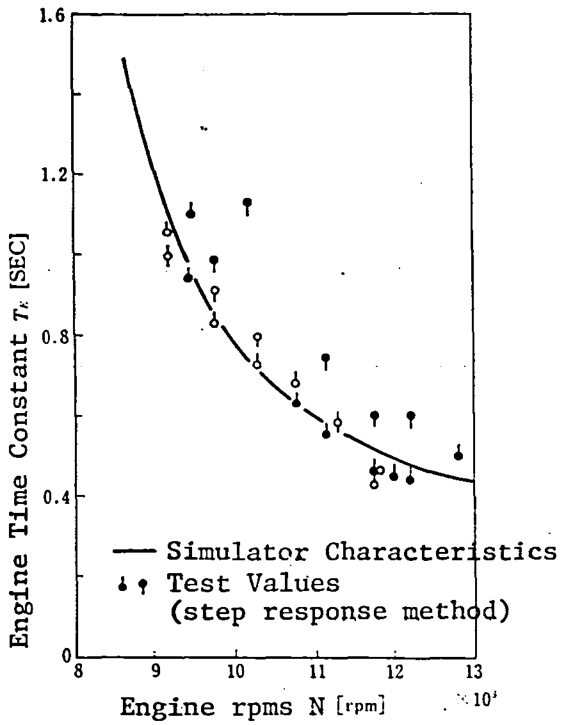


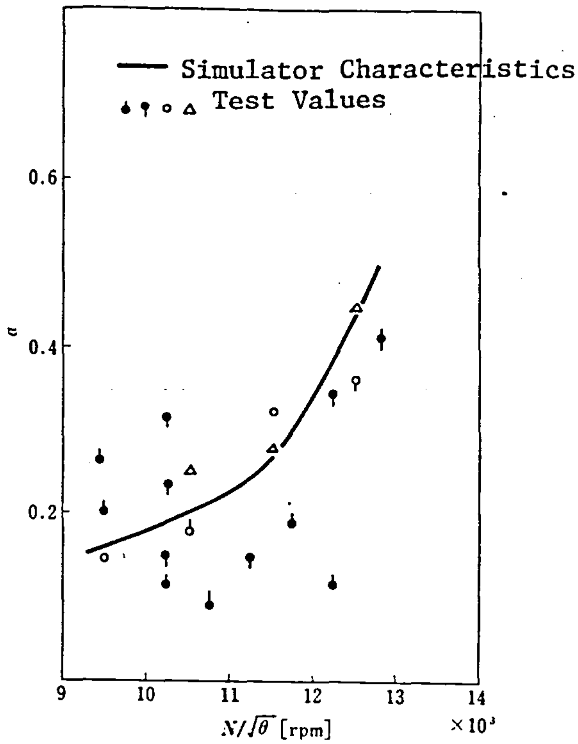
Figure 12 JR100H Static Characteristics

Status variables computed in this way are stored in a common area to which any program can refer and freely perform I/O selection and scaling.

Figure 12 compares test values with static characteristics derived by the simulator. Figures 13 and 14 are engine transfer functions derived by the simulator. They are compared with previously announced measurement data on dynamic characteristics. Figure 15 is a line graph of compressor characteristics when step fuel flow is assigned in combination with electronic fuel control system. Environmental temperature is a parameter. Figure 16 is the data[5] for coupling with a digitally controlled fuel control system. The solid lines are data from the simulator, the broken lines are data from actual engine use. Test conditions are somewhat different, but we can see a good mathc in general trend. Figure 17 shows status changes in each unit of the engine when a change in step fuel flow is assigned. Figure 18 is the data when the program is written in FORTRAN. Sample time is 70 microseconds. We can see the influence of the sample.

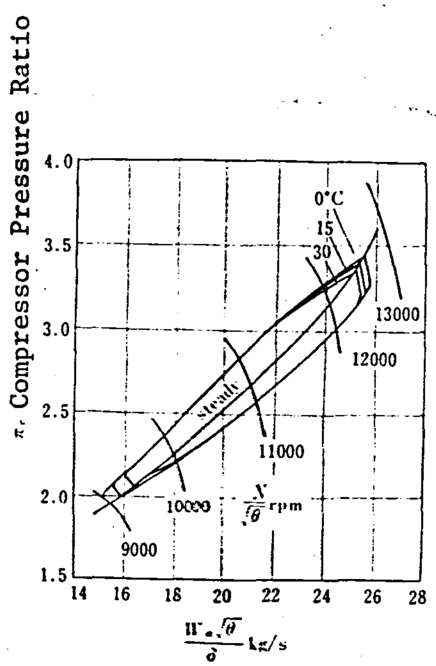


$\frac{N}{W_f} = \frac{1}{1+T_E S}$



$\frac{F}{W_f} = \frac{1+aT_E S}{1+T_E S}$

<u>Figure 13 Engine Transfer Function</u> <u>Figure 14 Engine Transfer Function</u>



<u>Figure 15 Simulation Test Data</u>

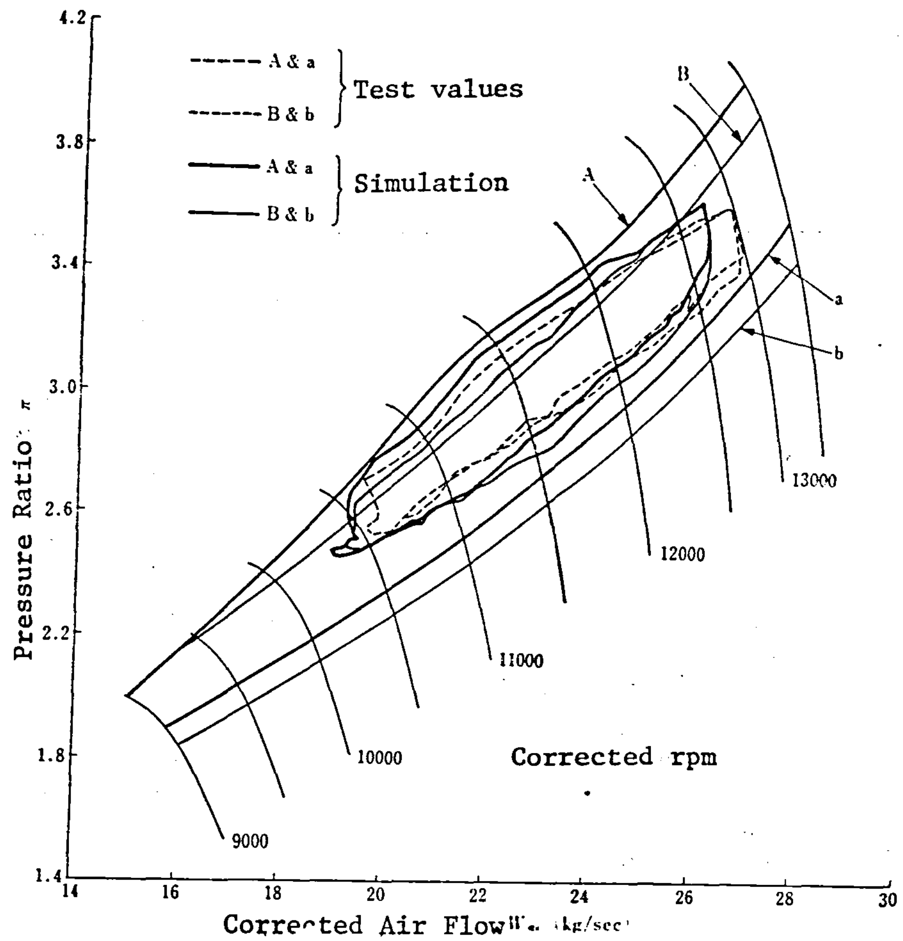


Figure 16 Comparison of Simulation and Tests

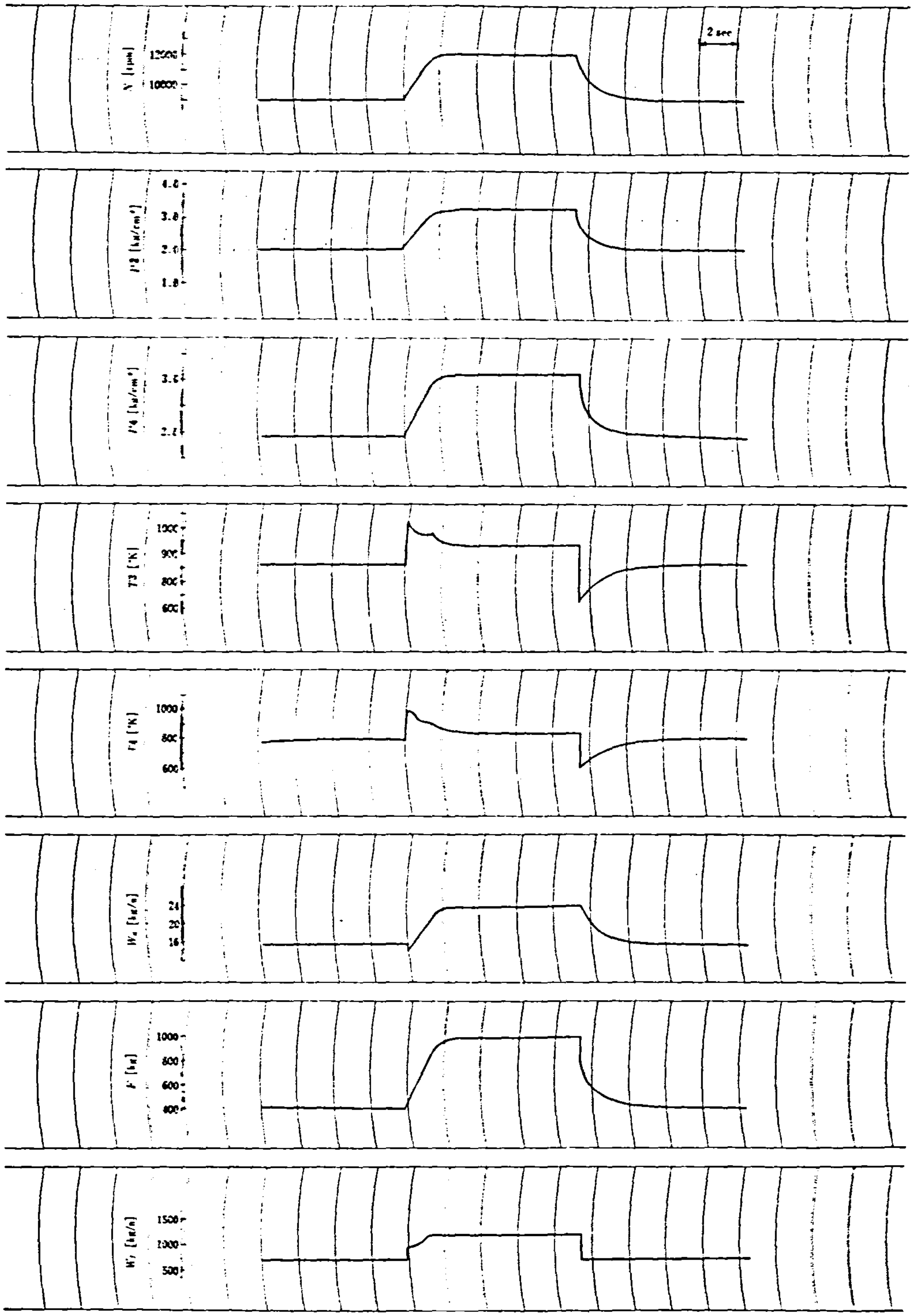


Figure 17 Simulation Data

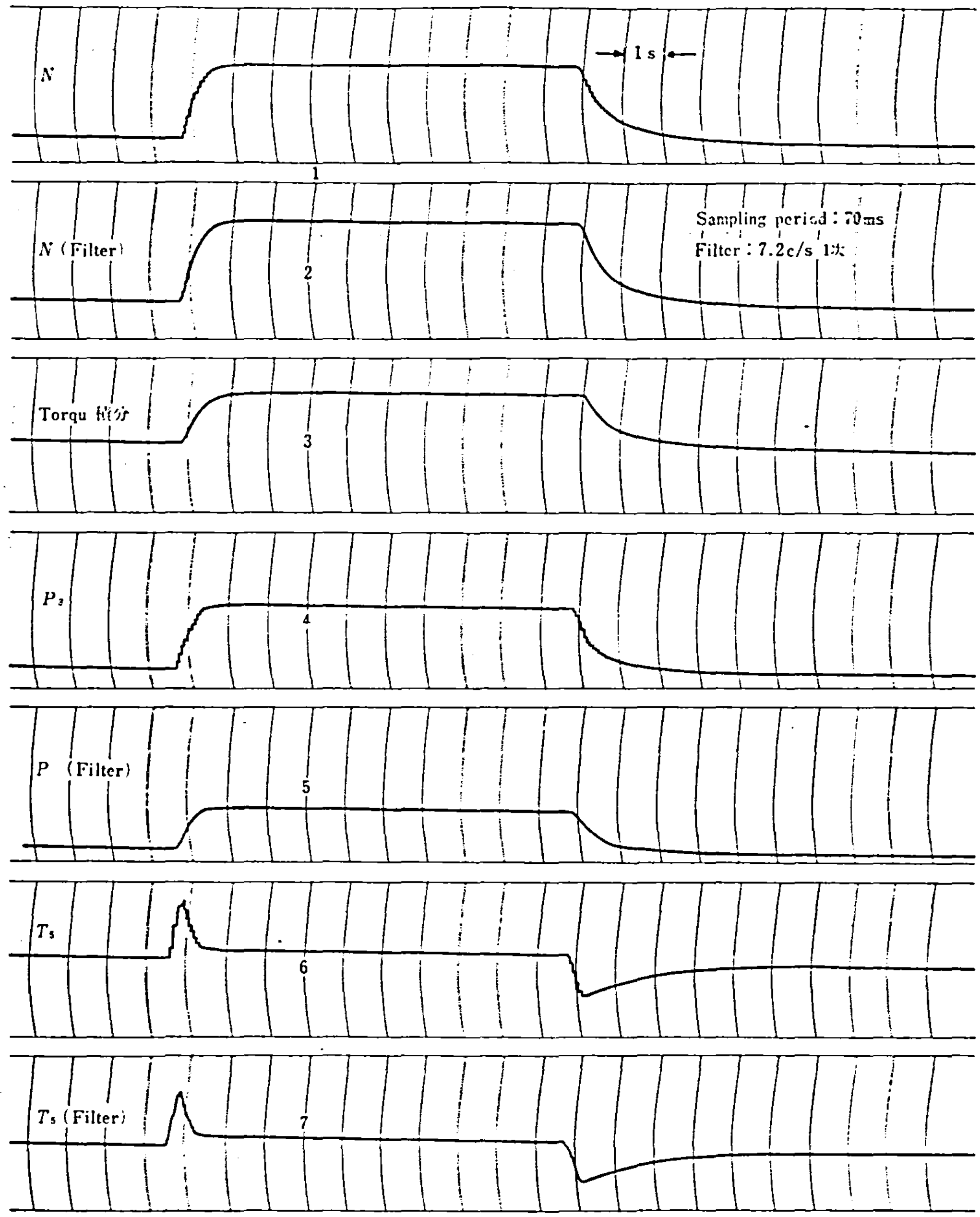


Figure 18 Affect of Sample Time

5. Structure and Characteristics of the Simulator

The simulator can be divided into digital arithmetic/logic operation unit, analog arithmetic/logic unit, I/O interface and display unit. A schematic of the entire configuration is shown in Figure 19. The digital arithmetic/logic operation unit's CPU can perform all simulator controls. Fixed time interval processing can be done by clock. Operation results are recorded by pen-write recorder, X-Y recorder and storage type display. A disk drive is used for temporary data storage to store operating systems and subroutines. Each will be described in the following paragraphs.

5.1 Digital arithmetic/logic operation unit

The digital arithmetic/logic operation unit consists of the following:

(1) Central processing unit
(2) Teletypewriter
(3) Paper tape punch
(4) Paper tape reader
(5) Disk drive storage

5.1.1 Central processing Unit (CPU)

The CPU is a 16-bit control computer in parallel arithmetic format. High speed arithmetic operation circuits have been added to basic commands for the fast multiplication/division required in real-time simulation. Four priority interrupt circuits have been added to the standard interrupt circuits for I/O devices. Each has priority over the standard interrupt circuits. One is used by the clock. Table 2 gives the specifications for the CPU. Figure 20 shows the relationship between internal registers and I/O circuits. The A register is the bus for external output and basic operation. The B register is for double-length operations. The Y register is for specification of memory addresses. The D register is the bus for external input and distribution. The M register is for memory I/O. The X register is the index register. When an interrupt signal is externally input, the priority interrupt moves the program to a specified subroutine. It then returns to the original program after the second program is terminated. A priority interrupt has higher hardware priority than a standard interrupt. A job can be cancelled and a move made to a specified program even when peripherals such as the teletypewriter are in operation. Both the standard interrupt and the priority interrupt are designed so that an interrupt inhibit and interrupt release can be assigned at any time by program-mask-set commands. Figure 21 lists the interrupt mask assignments.

5.1.2 Teletypewriter

The teletypewriter is used for typed output of program creation, measurement data, and computer results. The specifications for the teletypewriter are listed below

1)	Model	ASR-33
2)	Print speed	10 cps
3)	Paper tape read speed	10 cps
4)	Paper tape punch speed	10 cps

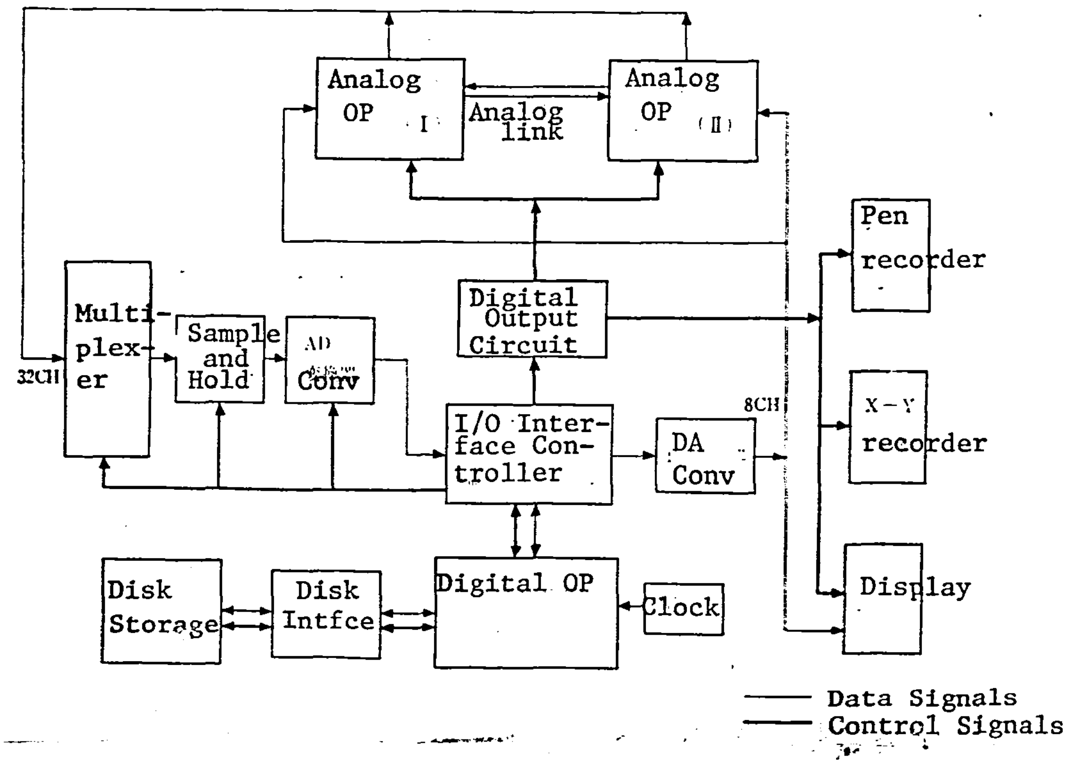


Figure 19 Schematic Diagram of the Simulator

Table 2 CPU Specifications

Name	NEAC 3200-50	
Format	°16-bit parallel binary	
	°Two's complementary operation	
	°Current equalizer mode random access ferrite core memory, 8K words	
	°Single-address mode with multi-level indirect addressing and indexing	
Speed	°Memory cycle time	0.96μsec
	°Addition	1.92 "
	°Subtraction	1.92 "
	°Multiplication	5.28 " *
	°Division	10.56 " *
	°Double precision addition	2.88 " *
	°Single-word I/O transfer	1.92 "
	°Time multiplex I/O transfer	260KHz at DMC* ≥1MHz at DMA*
Power Supply	°115V AC ± 10%, 50/60Hz ± 1.5Hz, 1KW, power supply failure interrupt priority	
Signal Level	°Logical Ø, 0V DC	
	°Logical 1, +6V DC	
Standard I/O Line	°10-bit address pass	
	°16-bit input pass	
	°16-bit output pass	
	°Priority interrupt	
	°External control and sense line	
Weight	113Kg	
Ambient temperatures	0°C-45°C (CPU only)	

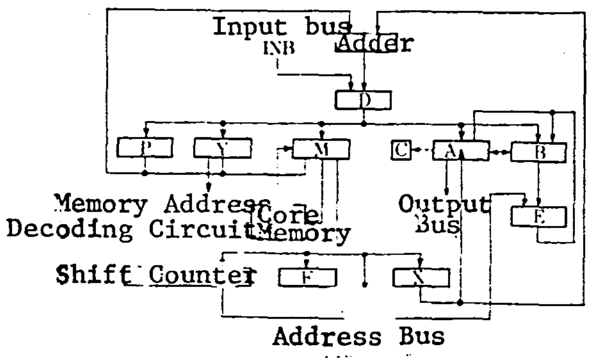


Figure 20 Computer Configuration

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Accumulator

Priority Interrupt (SMK '120)

OTB Bit No.	Device Name
1	Manual Interrupt 1
2	Manual Interrupt 2
3	Manual Interrupt 3
4	Manual Interrupt 4

Priority Interrupt (SMK '20)

OTB Bit No.	Device Name
1	External Storage
2	(Digital Input 1)
3	Communications Controller
4	Indexing Attachment
5	(Digital Input 2)
6	(Digital Input 4)
7	(Digital Input 3)
8	(Disk Storage)
9	(Paper Tape Reader)
10	(Paper Tape Punch)
11	(Teletypewriter)
12	Card Reader [Punch]
13	
14	Line Printer
15	Memory Parity
16	Real-time Clock

Devices in parentheses ( ) are presently in use.

Figure 21 Peripheral Device Mask Assignment

5.1.3 Paper tape punch

The paper tape punch is used for high-speed input and retrieval of measurement data on paper tape. The specifications of the device are given below.

1) Punch paper 8 unit paper tape
2) Punch speed 110 cps
3) Power supply 115V, 50Hz

5.1.4 Paper tape reader

The paper tape reader is used to read programs and store the compiler for program creation. The specifications for the device are given below.

1) Type Optoelectronic

2) Read speed 300 cps

3) Power supply 115V, 50Hz

5.1.5 Disk storage

The usual capacity of the mini-computer memory for control use is 4K to 8K words. When compiling source programs, the object program must be externally output on paper tape. Sub-routines are created in advance on paper tape. The only operation required then is storage of necessary subroutines by relocatable loader. There is little excess area for data storage. To overcome this disadvantage, a disk storage unit is set up for auxiliary memory. The disk storage drive used is in fixed-head mode with a capacity of 132K words. Access time is fast compared to movable head disk drives. Fixed-head drives have excellent MTBF features since there are few movable parts. A single interface links the disk storage drive to the CPU through the I/O-BUS (Figure 22).

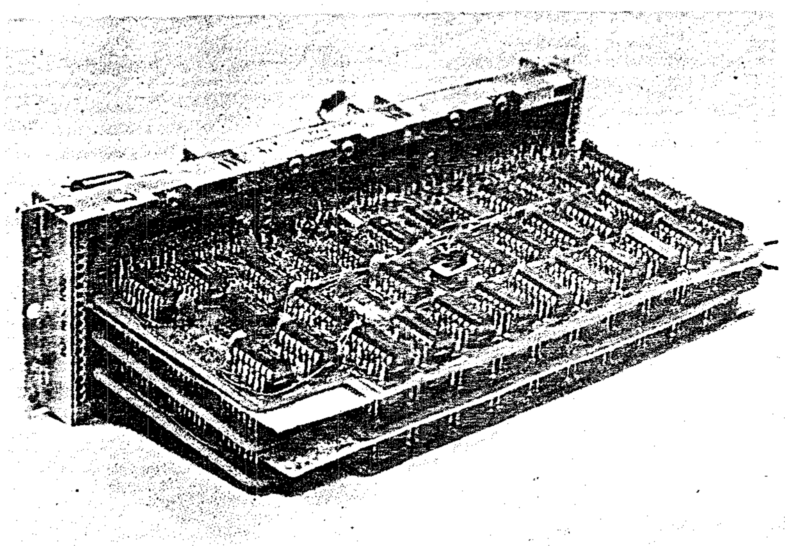


Figure 22 Disk Storage Device Interface

The specifications for the disk storage drive are:

(1) Model DATA DISC Company 1717

(2) Capacity 132KW (1 word is 16 bits + parity)

(3)	Disk rpm's	1800
(4)	Average access time	16.7ms

Table 3 Analo g Operation Unit Configuration

Component Name	No. of Comp. I	No. of Comp. II	Used Operation Device	Specs, etc.
Adder-integrator	9	15	BB1538A(I) BB3072, 3071(II)	Invert
	6	--	CEC 19-407	Non-invert (can invert)
Adder	18	20	BB1516(I) BB3305, 3064	Invert
	6	--	CEC19-301	Non-invert (can invert)
General Operational Amplifier	6	10	BB3072, 3071(I)(II)	
Buffer	12	--	CEC 19-105-2	Non-invert Gain 1
Low-pass Filter	6	--	BB5002	Cross-frequency 5[Hz]
Potentiometer	30	--		Linear ground type
	10	--		3-line
	--	30		Servo-set potentiometer
Multiplier-divider	6	--	CEC 19-302	X_1X_2/X_3
Square-root Operator	3	--	CEC 19-303	$a_0\sqrt{10a_1X}$
Function Generator	6	--	BB 1662	
Comparator	8	8	CEC 19-501(I) Shiquotex NE518G(II)	
White-noise Gen.	1	--	BB4006	
2-input NAND	--	15	Honeywell DI320	
4-input NAND	--	6	Honeywell DN320	
Flip-flop	--	8	Honeywell FA320	
Flip-flop	--	8	Honeywell FA320	
Monostable Multi-vibrator	--	4	Honeywell DM335	
Half-adder	--	8	Honeywell AP320	
Schmitt-trigger	--	4	Honeywell ST335	
UPDOWN Counter	--	3	Honeywell UD335	

Clock Generator	--	1	Honeywell MC335,FA320	1M,100K,10K 1K,100,10, 1[Hz] re-trievable
Chatter Shaper	--	5	ST335	
Pen-write Recorder	8	8		Number of Channels
X-Y Recorder	2	1		
CRT Oscilloscope	4	--		

(Note) I: Low-speed mode
II: High-speed mode

Item \ Part	BB 1538A	BB 307.1	BB 3072	BB 3005	BB 1516	BB 3064
Format	Chopper Stabilizer	Chopper Stabilizer	Chopper Stabilizer	Differentl Amplifier	Diffrntl Amplifier	Diffrntl Amplifier
Input Format	1-sideGND	1-sideGND	1-sideGND	Dffrntl Input	Dffrntl Input	Dffrntl Input
Input Impedance	0.5 [MΩ]	0.5 [MΩ]	0.5 [MΩ]	0.5 [MΩ]	0.2 [MΩ]	0.5 [MΩ]
Input Signal Level	±10 [V]	±10 [V]	±10 [V]	±10 [V]	±10 [V]	±10 [V]
Open-loop Gain	160 [dB]	150 [dB]	150 [dB]	100 [dB]	96 [dB]	86 [dB]
Gain Stability (VS. Temp.)	0.1 [dB/°C]	0.1 [dB/°C]	0.1 [dB/°C]	0.1 [dB/°C]	0.1 [dB/°C]	0.1 [dB/°C]
Frequency Band Refraction (at 0 [dB])	15 [MHz]	15 [MHz]	15 [MHz]	1.5 [MHz]	1.0 [MHz]	5.0 [MHz]
Rated Output	±10 [V] ±20 [mA]	±10 [V] ±20 [mA]	±10 [V] ±20 [mA]	±10 [V] ±20 [mA]	±10 [V] ±10]mA]	±10 [V] ±10 [mA]
Output Impedance	5 [kΩ]	5 [kΩ]	5 [kΩ]	5 [kΩ]	5 [kΩ]	5 [kΩ]
Input Voltage Offset	±15 [μV] (at 25 [°C])	±10 [μV] (at 25 [°C])	±20 [μV] (at 25 [°C])	±0.5 [mV] (at 25 [°C])	±0.5 [mV] (at 25 [°C])	±2 [mV]
Input Voltage Drift (VS. TIME)	±1 [μV/24 h]	±1 [μV/24 h]	±1 [μV/24 h]	±20 [μV/24 h]	±50 [μV/24 h]	—
Input Voltage Drift (VS. TEMP)	±0.5 [μV/°C]	±0.2 [μV/°C]	±0.2 [μV/°C]	±5 [μV/°C]	±10 [μV/°C]	—
Input Conversion Noise	6 [μV] rms (DC~10 [kHz])	1 [μV] rms (6 [Hz]~1 [kHz])	2 [μV] rms (6 [Hz]~1 [kHz])	4 [μV] rms (DC~10 [kHz])	10 [μV] rms DC~10 [kHz]	6 [μV] rms
Temperature Range	−25~85 [°C]	−25~25 [°C]	−25~85 [°C]	−25~85 [°C]	0~60 [°C]	−25~85 [°C]
Power Supply	±15 [V]	±15 [V]	±15 [V]	±15 [V]	±15 [V]	±15 [V]
Remarks	Has Over-flowsignal output	Overflow Signal Output	Overflow Signal Output			

Table 4 Operational Amplifier Characteristics

5.2 Analog Arithmetic/Logic Operation Unit

This unit is composed of two operation units, one high speed, the other low speed for convenience. As far as analog computers are concerned, both operation units are low-speed mode but one is called low- and the other high-speed because the former uses relays for integrator control, and the latter uses electronic switching circuits.

Figures 23 and 24 show external views of the analog arithmetic/logic operation unit. The following discussion is devoted to each component in the configuration.

5.2.1 Adder-integrators

The low speed mode uses relays and the high speed mode uses FET electronic switches to switch to and from the integrators' modes of reset, compute and hold. The circuits are shown in Figures 25 and 26. This switching operation is set so that the computer can perform switching singly or simultaneously or so that manual switching can be performed. A mode for each integrator can be selected in the high speed mode. The circuit in Figure 27 is attached to each integrator to detect integrator overflow. Figure 28 is an external view of the integrator.

5.2.2 Adder

Differential input operational amplifiers are used in the adder's operational amplifier. These are grounded on one side. Table 4 gives the characteristics of those amplifiers. Circuit structure is shown in Figures 29 and 30. Figure 31 shows example data of a circle test performed on a combination of two integrators. The relation between elapsed time and error is shown in Figure 32.

The lack of a chopper stabilizing circuit prevents modulated signals from being used for adder overflow circuits. Instead, a bipolarity comparator was used. That circuit is shown in Figure 33.

5.2.3 Multiplier-divider

The multiplier-divider uses pulse-width modulation format. The schematic diagram of the device is shown in Figure 34. Precision is a full-scale 0.1%. Figure 35 shows the frequency characteristics. Figure 36 gives test data.

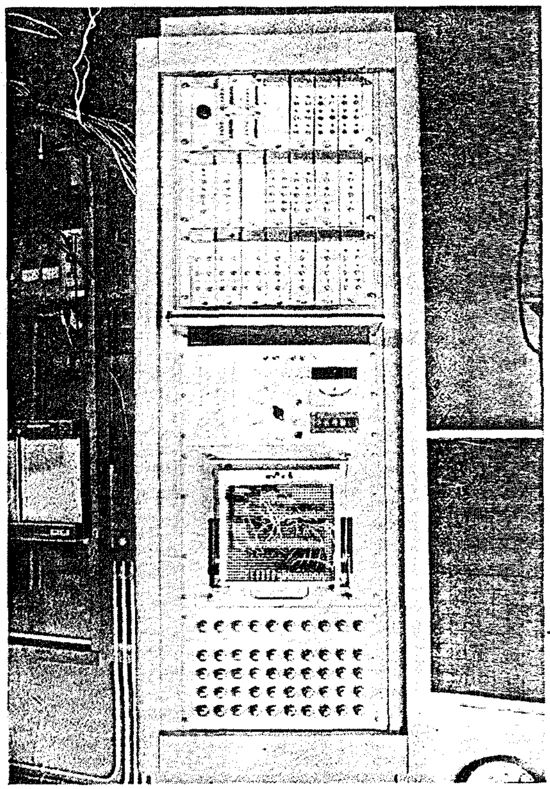


Fig.23 Analog OP Unit (I)

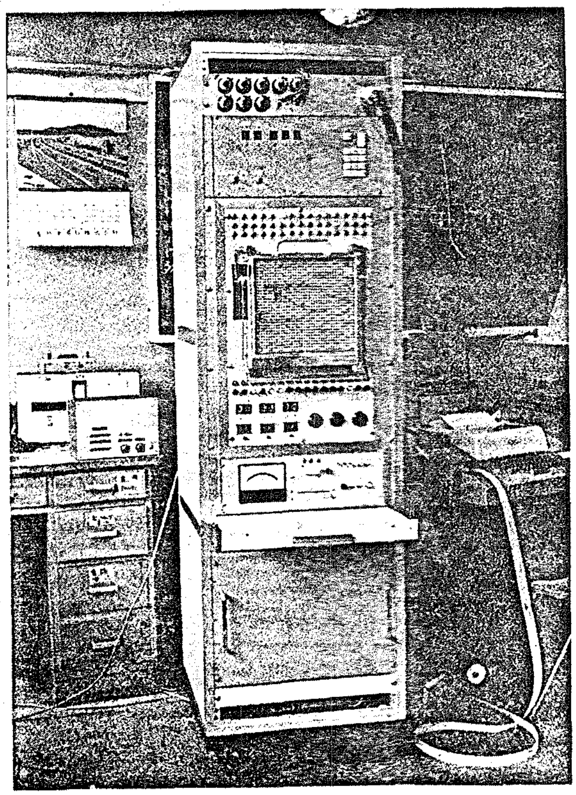


Fig. 24 Analog OP Unit (II)

Mode	contact location	
	A	B
potentioset	2	1
reset	2	1
operate	1	2
halt	2	2

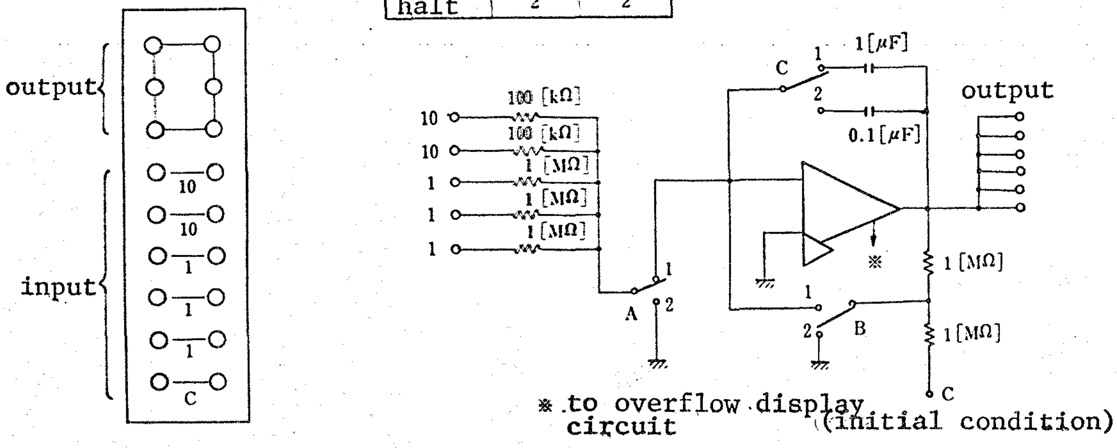


Figure 25 Integrator Circuit (Low-speed)

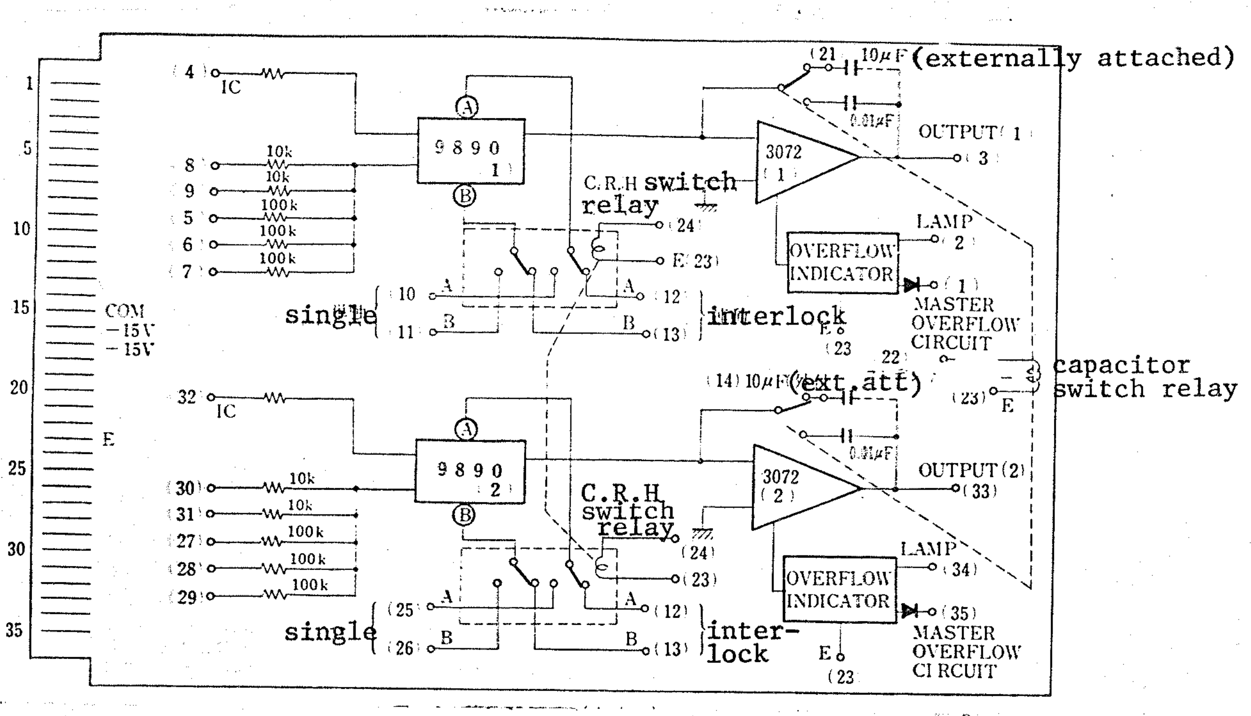


Figure 26 Integrator Circuit (High-speed)

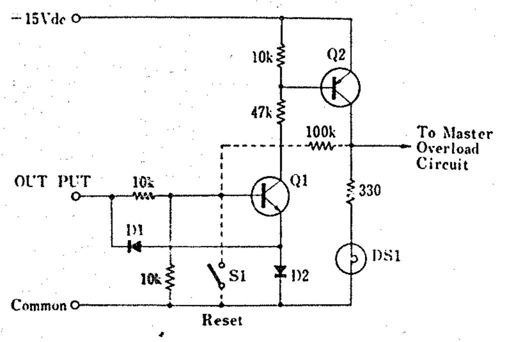


Figure 27 Overflow Detector Circuit

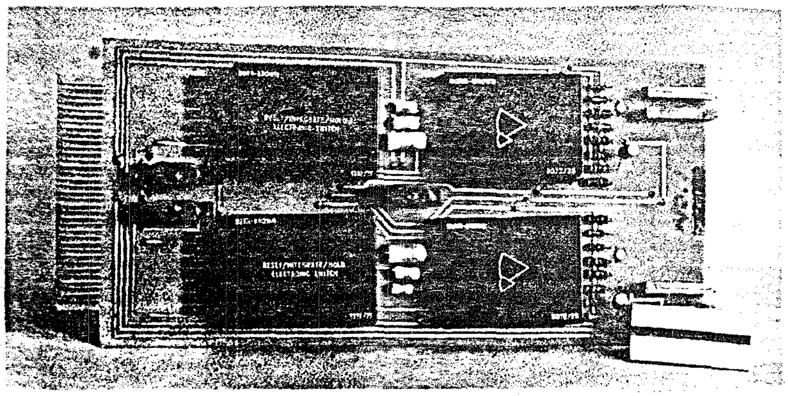


Figure 28 Integrator (High-speed)

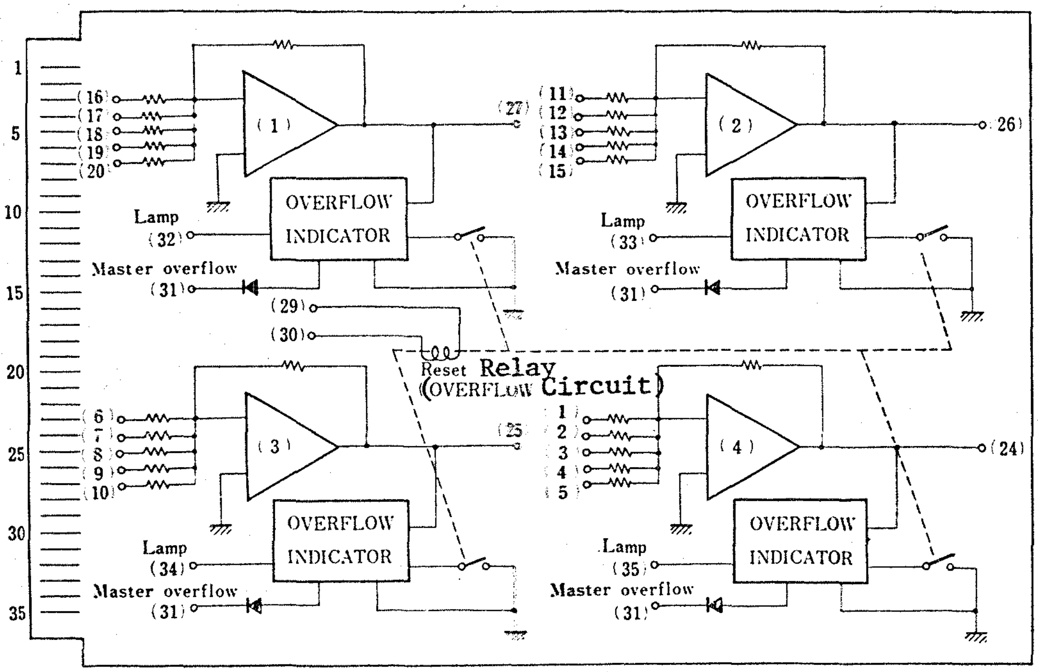


Figure 29 Adder Circuit (High-speed)

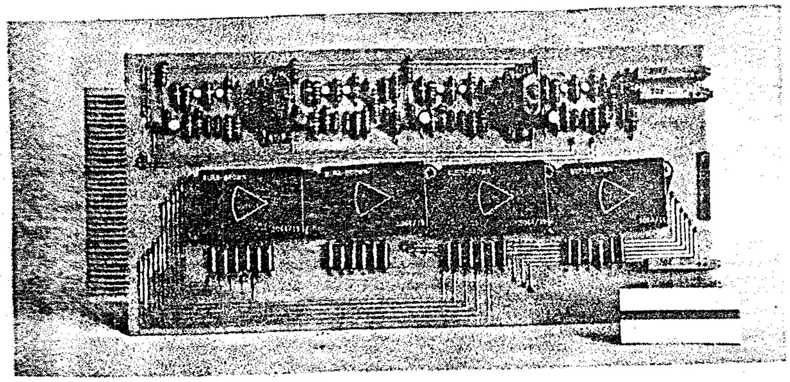


Figure 30 Adder (High-speed)

5.2 Square-root Operator

The square-root operator has the same format as the multiplier-divider. Figure 37 is the schematic diagram, Figure 38 shows the frequency characteristics of the operator. Test data is shown in Figure 39.

5.2.5 Function Generator

The function generator has 11 diode functions. The schematic is shown in Figure 40. An external view of the generator is in Figure 41.

5.2.6 Comparator

Performs 2-input comparison. Output can be extracted by either voltage or relay contacts. Sensitivity is 1mV.

5.2.7 White-noise Generator

Figure 42 is a schematic diagram of the white-noise generator. It is set up so that clock frequency can be changed to three-step and the upper limits of the frequency band can be changed. Table 5 gives the values of the power spectrum.

5.2.8 Digital Element

The circuit of the digital element is shown in Figure 43. The usable integrated circuit is DTL. The operating frequency is 2MHz DC. Logical 1 is +6V, logical Ø is 0V. Connections can be made as required on the patchboard.

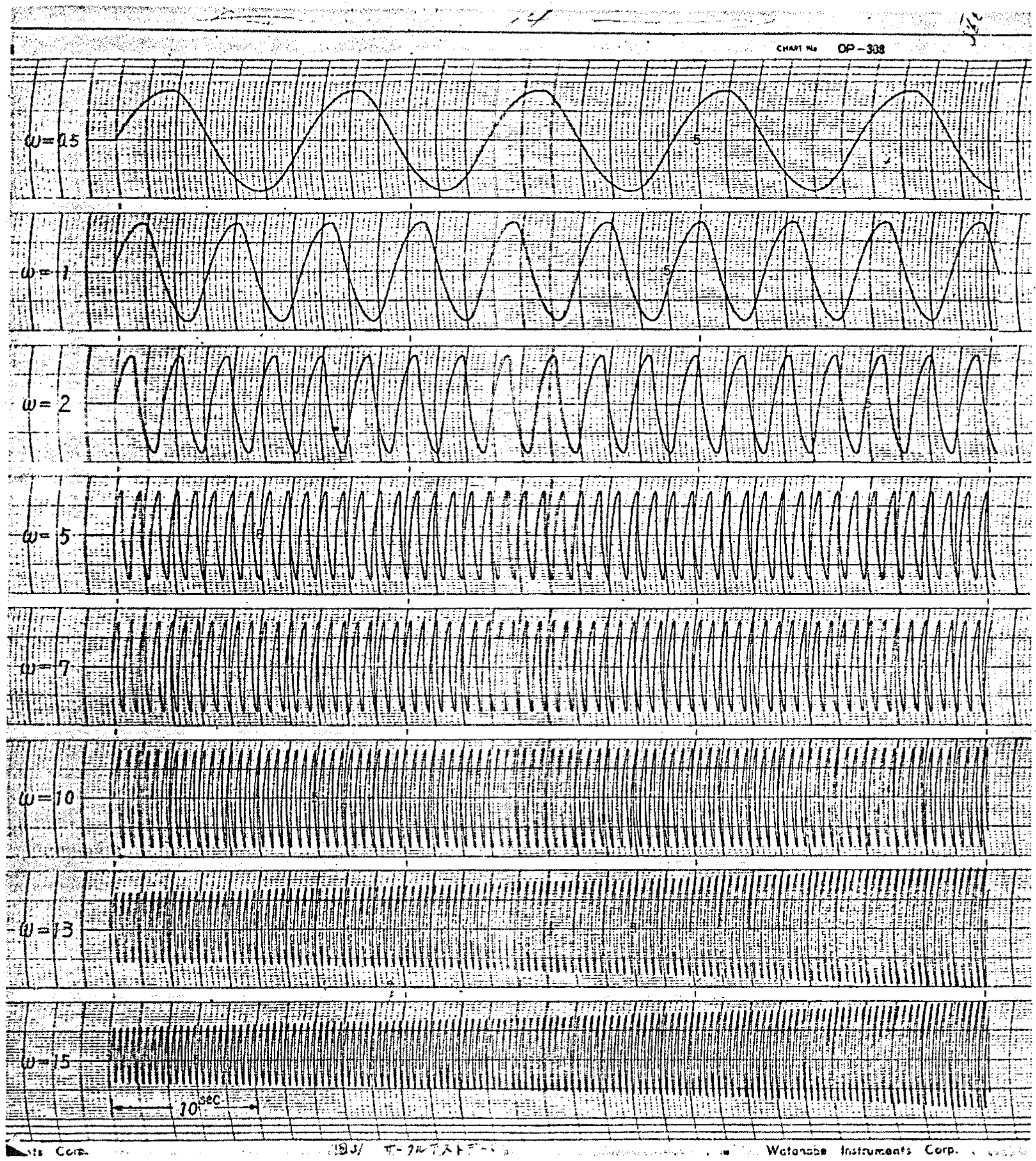


Figure 31 Circle Test Data

5.2.9 Patchboard and Control Board

Has two surfaces one for low-speed use, the other for high-speed use. The pattern of these boards is shown in Figures 44 and 45.

The control board is equipped with-low speed and high-speed modes for divided use. The board is set up so that the three modes: single, simultaneous and computer control can be selected. In the high speed mode, the patch board and operational amplifiers are unified. An external view of the device is in Figure 46.

5.3 I/O Interface

The I/O interface converts analog signals to digital and digital signals to analog between the CPU, the analog arithmetic/logic operation unit and the display. It also generates the controls signals for the recorder. The I/O interface consists of the following devices.

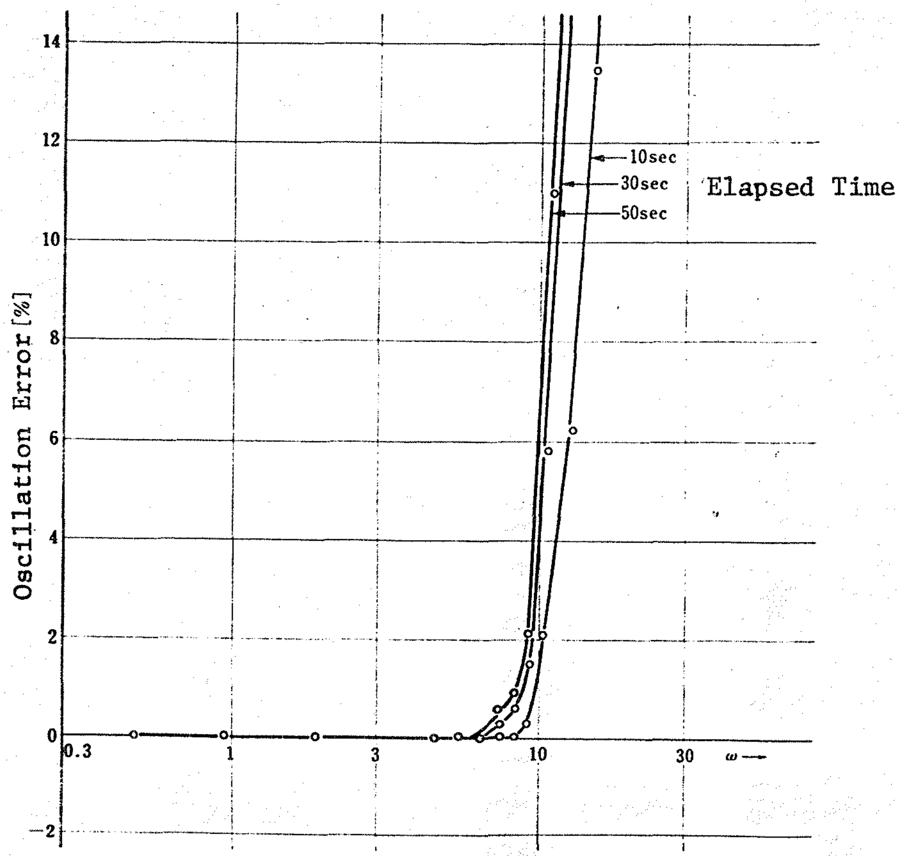


Figure 32 Circle Test Error

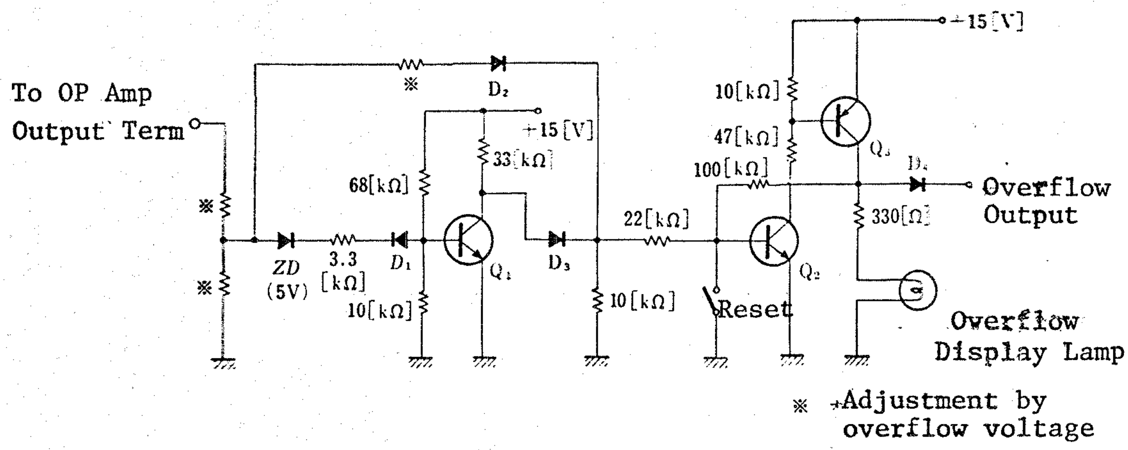


Figure 33 Overflow Voltage Display Circuit

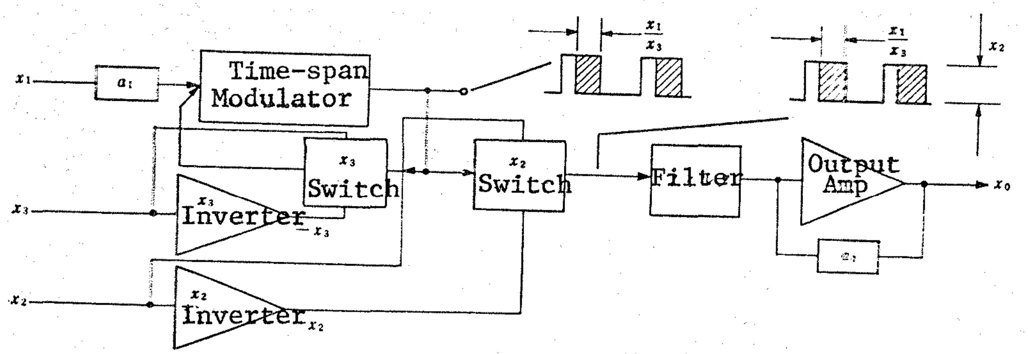


Figure 34 Multiplier-divider Schematic

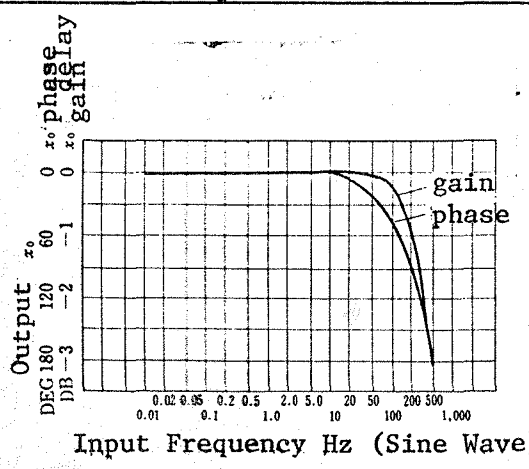


Figure 35 Multiplier-divider Frequency Characteristics

Multiplier $X_0=\frac{X_1 X_2}{X_3}$ Assign X_3 to 10[V]

X_2 \ X_1	0.100	1,000	2,000	3,000	5,000	10,000
0.100	0.006	0.015	0.025	0.035	0.053	0.103
1.000	0.012	0.102	0.201	0.301	0.501	1.001
2.000	0.019	0.199	0.399	0.599	0.999	1.998
3.000	0.027	0.297	0.597	0.897	1.497	2.998
5.000	0.450	0.495	0.995	1.496	2.496	4.998
10.000	0.096	0.997	1.997	2.998	4.999	10.004

Divider $X_0=\frac{X_1 X_2}{X_3}$ Assign X_2 to 10[V]

X_3 \ X_1	0.100	1.000	2.000	3.000	5.000	10.000
0.100	10.110					
1.000	0.964	10.033				
2.000	0.488	5.004	10.023			
3.000	0.327	3.333	6.673	10.016		
5.000	0.194	1.996	3.997	6.000	10.007	
10.000	0.095	0.996	1.995	2.996	4.998	10.004

Figure 36 Multiplier-divider Data

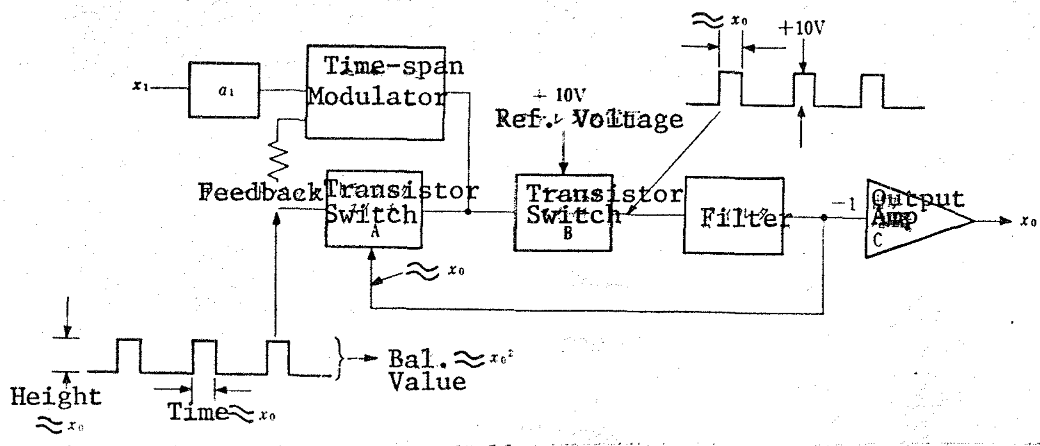


Figure 37 Square-root Operator Schematic

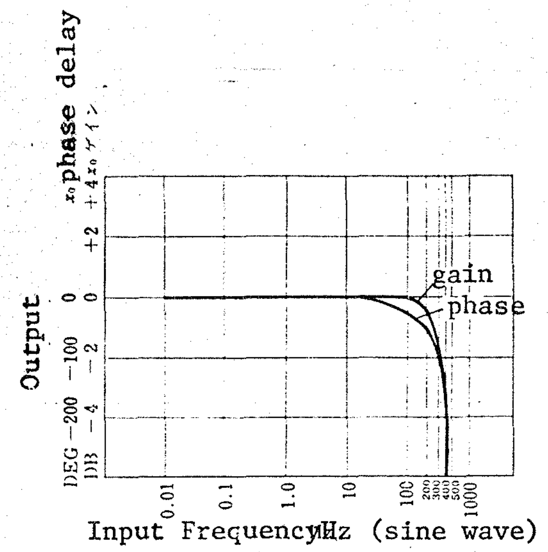


Figure 38 Square-root Operator Frequency Characteristics

XI Input	0.100	1.000	2.000	3.000	5.000	10.000	Noise Output (MAX.)
E_0 Unloaded	1.008	3.172	4.477	5.479	7.070	10.000	8 [mV] P-P
E_0 Loaded	1.007	3.171	4.476	5.482	7.069	9.998	8 [mV] P-P

a_0, a_1 Variable by Externally Attached Resistor

Figure 39 Square-root Operator Data

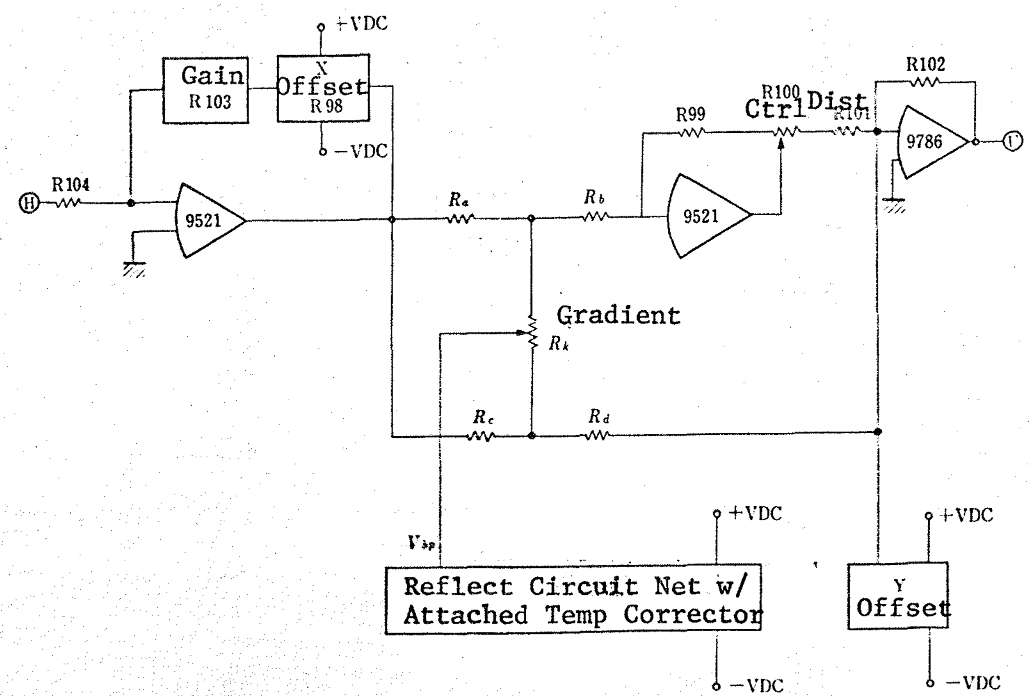


Figure 40 Function Generator Schematic

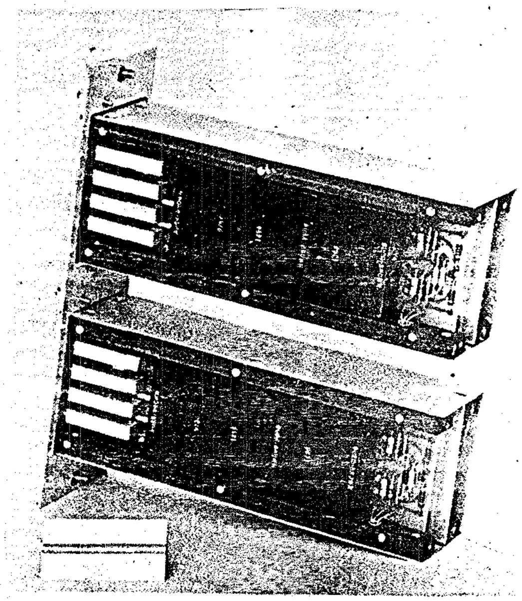


Figure 41 Function Generator

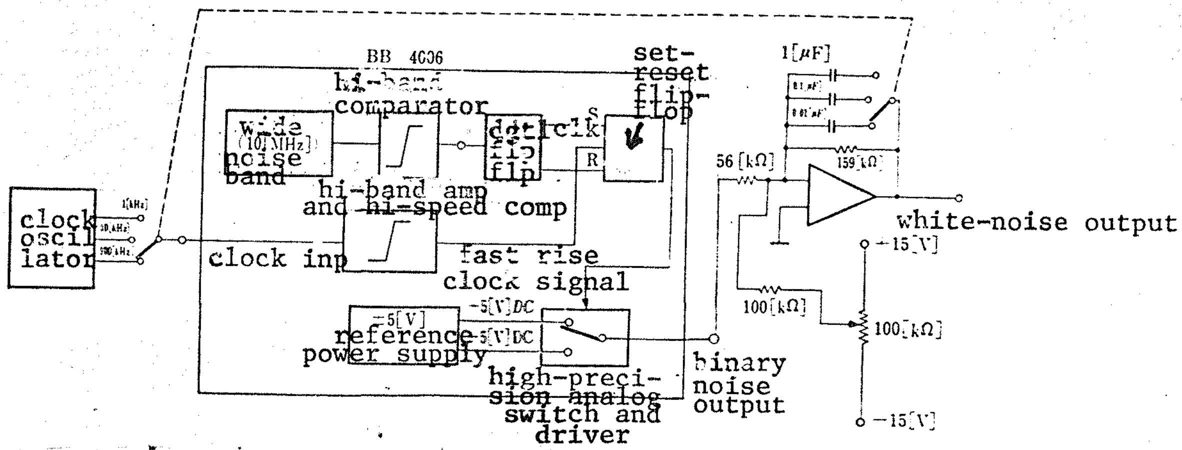


Figure 42 White-noise Generator Schematic

Table 5 Power Spectrum

clock frequency=1/Δ Hz	flat range spectrum V^2/Hz	−0.1 dB frequency Hz	−1 dB frequency Hz
1 kHz	2.5×10^{-2}	80 Hz	250 Hz
10 kHz	2.5×10^{-3}	800 Hz	2.5 kHz
100 kHz	2.5×10^{-4}	8 kHz	25 kHz
1 MHz	2.5×10^{-5}	80 kHz	250 kHz

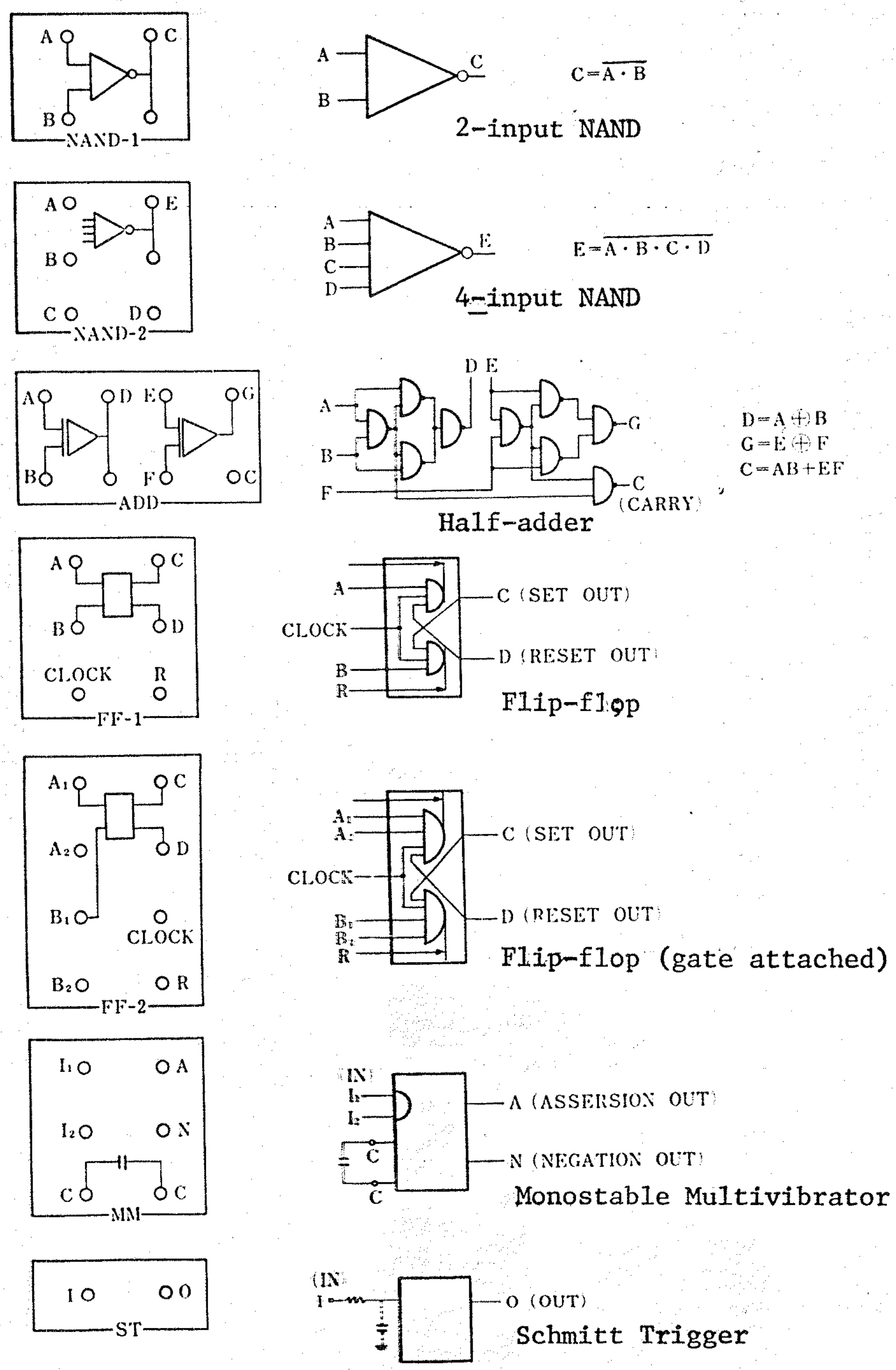

NAND-1
C=A·B
2-input NAND
NAND-2
E=A·B·C·D
4-input NAND
ADD
D=A⊕B
G=E⊕F
C=AB+EF
(CARRY)
Half-adder
FF-1
CLOCK
C (SET OUT)
D (RESET OUT)
Flip-flop
FF-2
Flip-flop (gate attached)
MM
A (ASSERSION OUT)
N (NEGATION OUT)
Monostable Multivibrator
ST
(IN)
O (OUT)
Schmitt Trigger

Figure 43 (a)

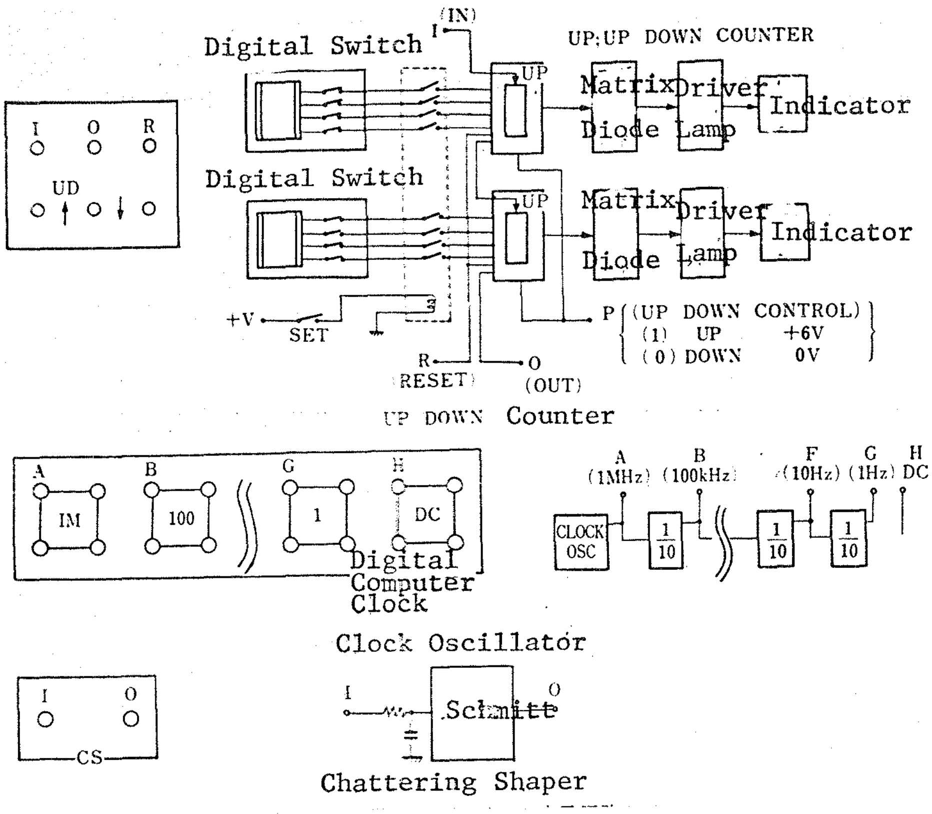


Figure 43 (b) Digital Device Circuit

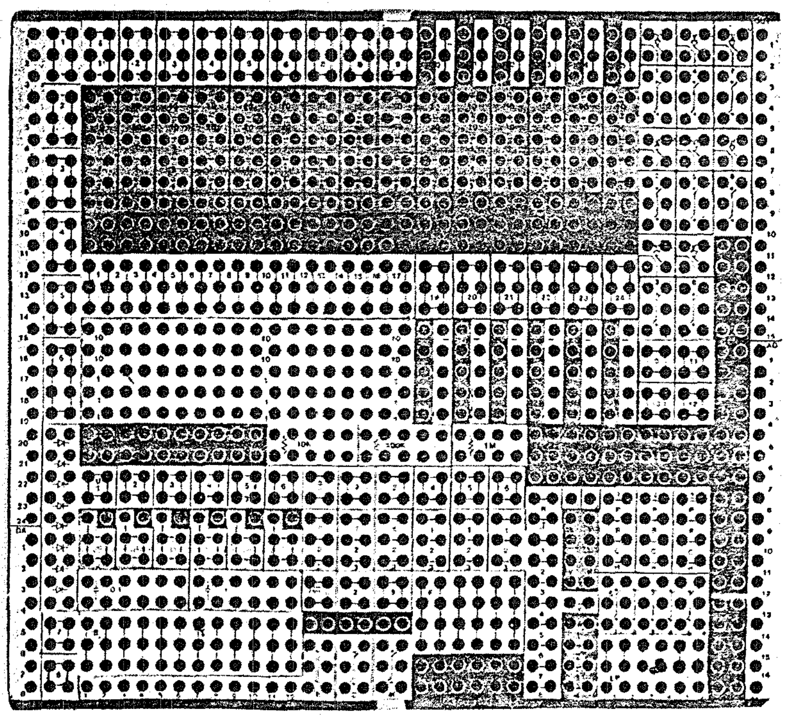


Figure 44 Patchboard (Low-speed Mode)

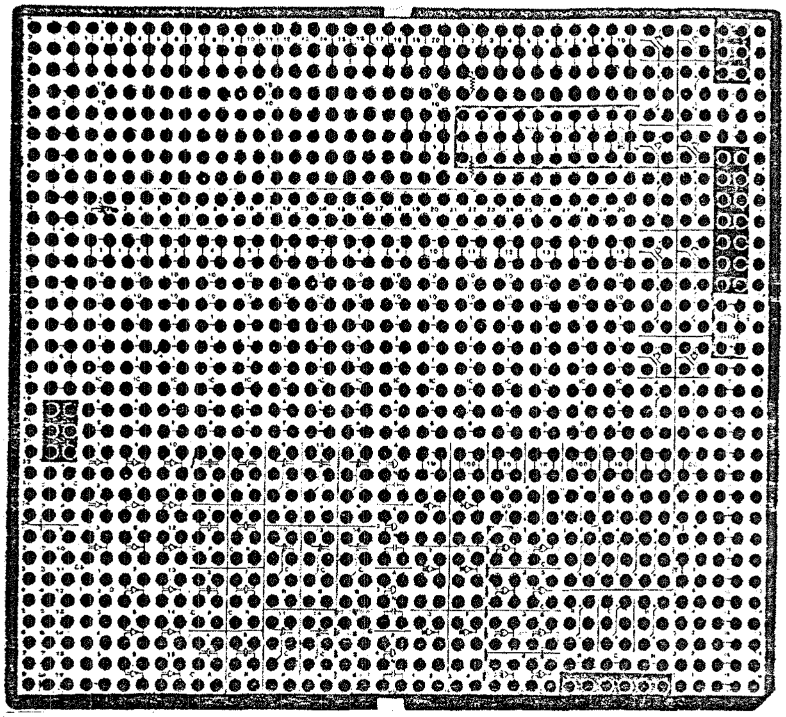


Figure 45 Patchboard (High-speed Mode)

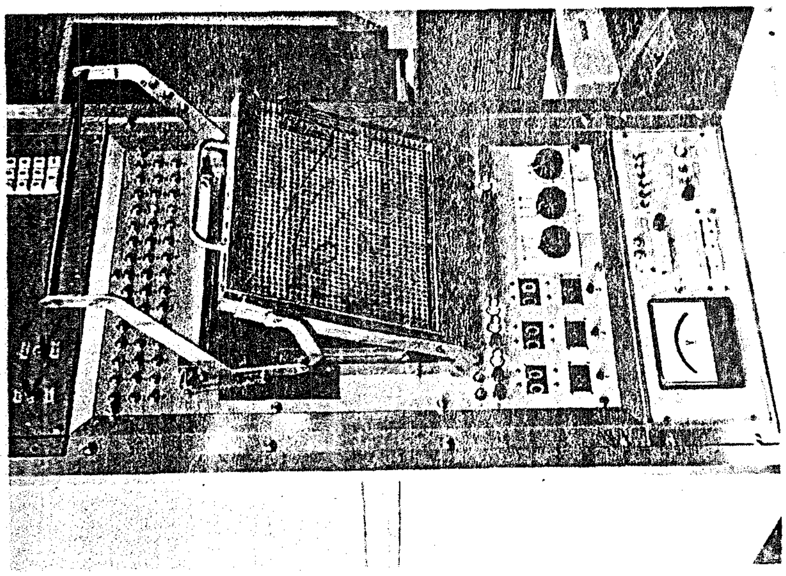


Figure 46 Control Board (High-speed Mode)

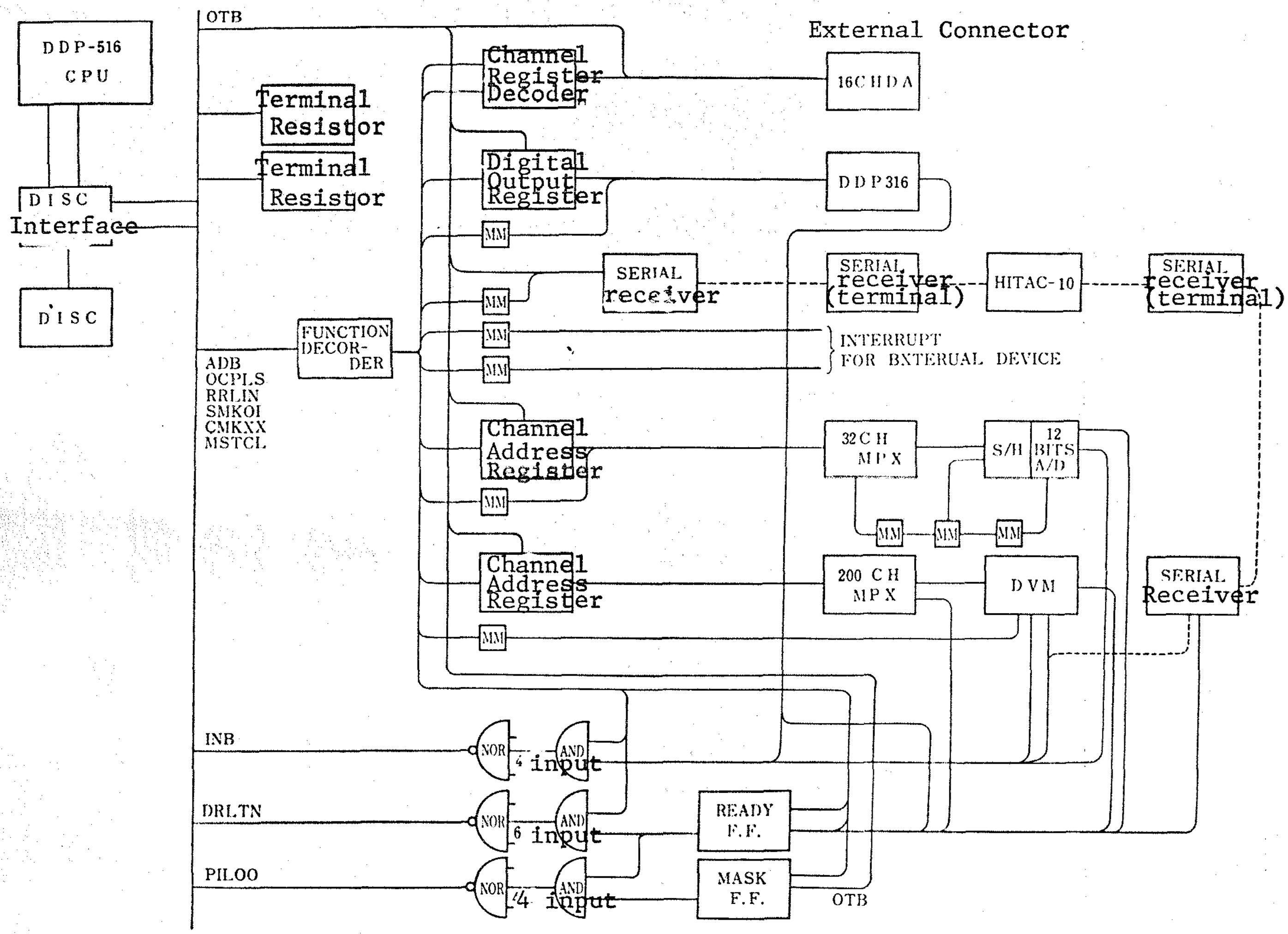


Figure 47 I/O Interface Schematic

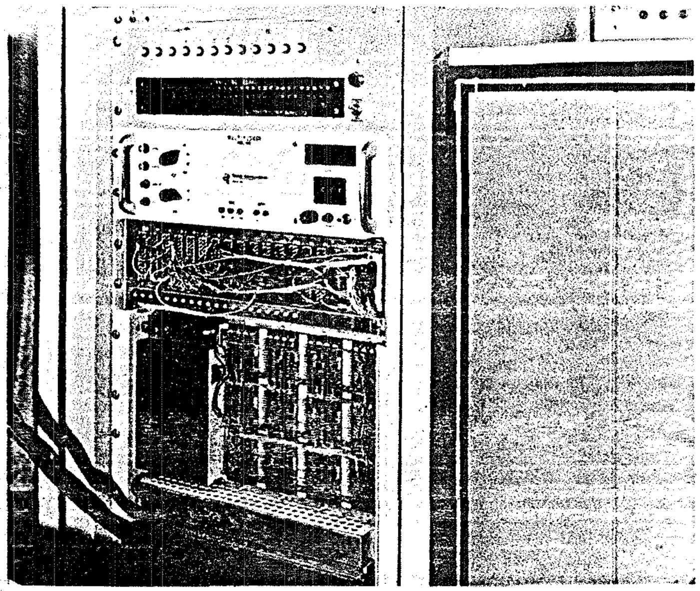


Figure 48 External View of I/O Interface

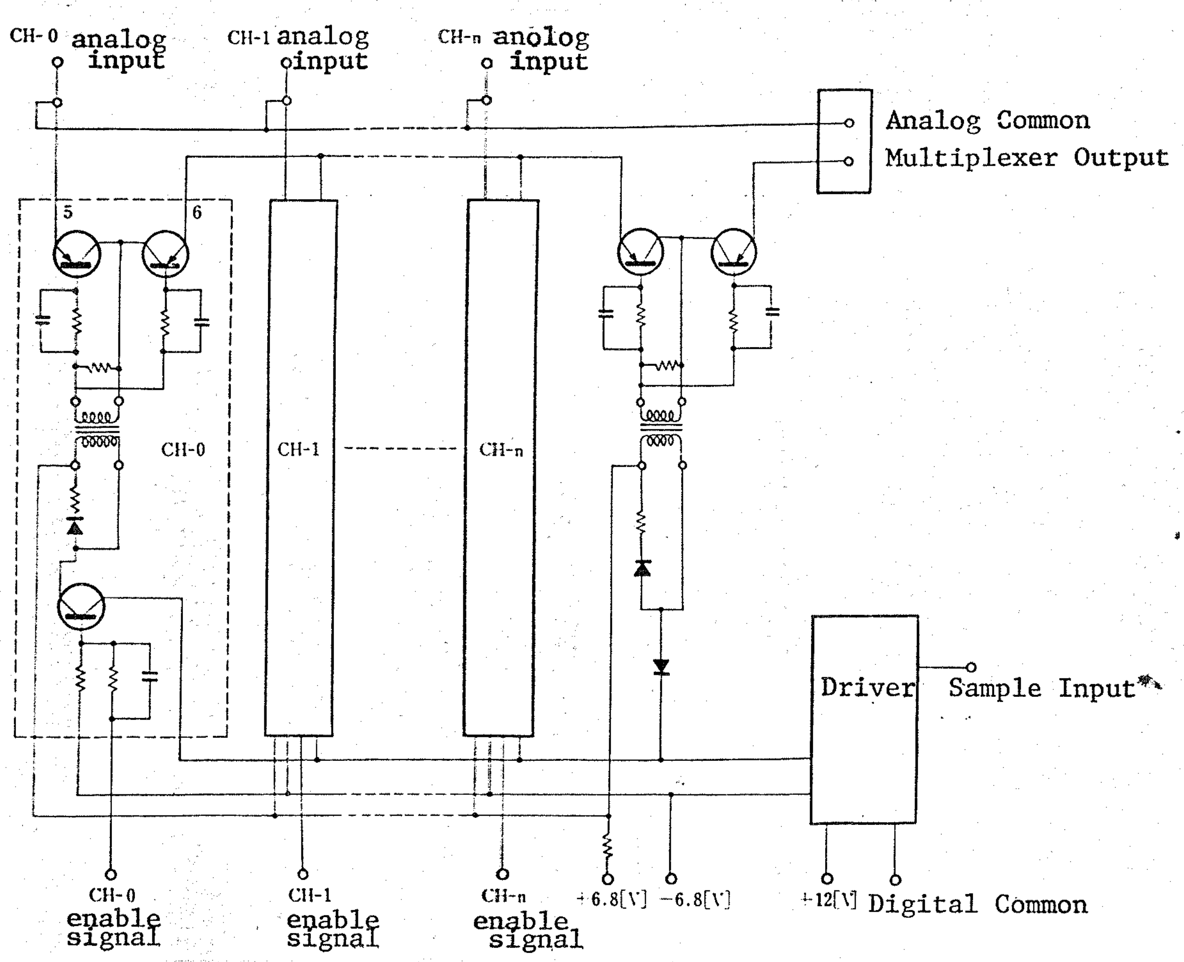


Figure 49 Multiplexer Circuit

(1) Multiplexer

(2) Sample-and-hold

(3) AD Converter

(4) DA Converter

(5) Controller

The schematic diagram is in Figure 47, an external view is shown in Figure 48.

5.3.1 Multiplexer

Analog signals for fuel flow, intake air pressure, atmospheric pressure, etc., are the simulator's input signals. Those analog signals are sampled by the multiplexer and input to the CPU. Modes in the multiplexer are changed by electronic switch and either sequential or random-access mode can be selected. Figure 49 shows the switching circuits. Switching speed can be adjusted to anywhere from 20 to 200 microseconds. Table 6 gives the specifications for the multiplexer.

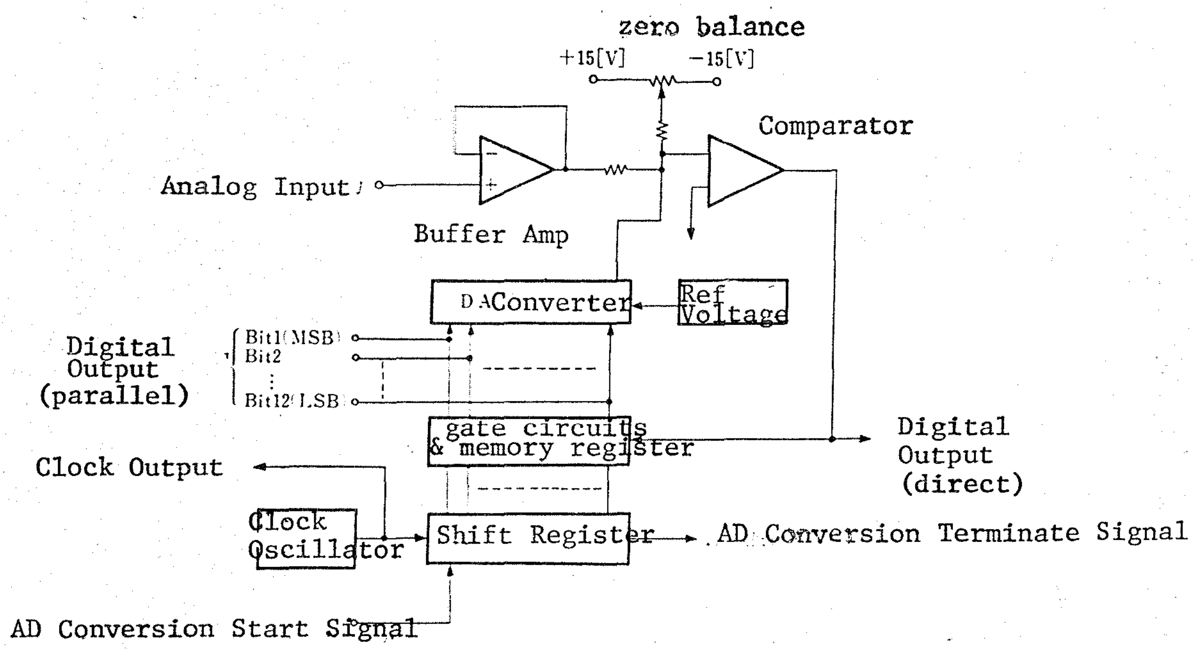


Figure 50 AD Converter Schematic

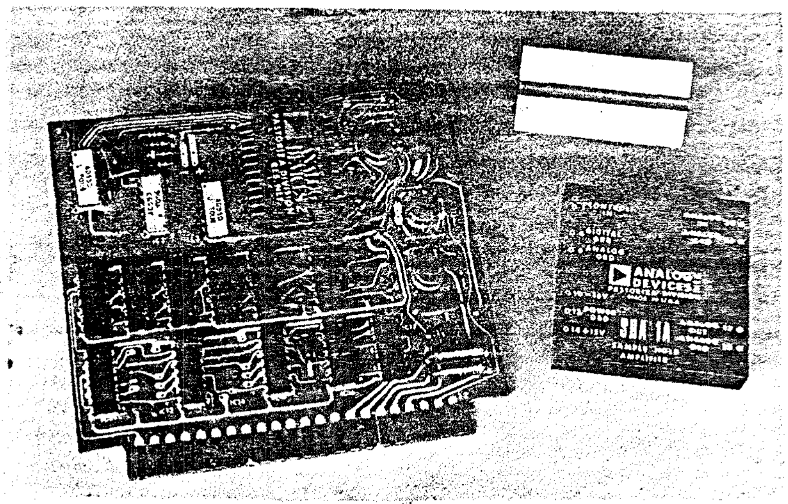


Figure 51 External View of AD Converter and Sample-and-hold

Table 6 Characteristics of the I/O Interface Element

Multiplexer (MODEL 845 E 01 [TI])		Sample-and-hold (MODEL SHAIA (ANALOG DEVICES))		AD Converter (MODE ADC-12Q (ANALOG DEVICES))	
No. of Channel	31	Input	±10 V	Convert Mode	Continual Comparator
Input and Output	±10 [V]	Gain	1	Output Code	12 bit (bipolar, offset binary or two's complementary
Inpt Impedance	1 [kΩ] or more	Gain Accuracy (DC)	+0.0∼−0.05 [%]		
Crosstalk	DC ±0.01 [%] (FS)	Rated Inp Lev	10^{12} [Ω]	Precision	±½ LSB
Sampling Speed	20∼200 [µs/SAMPLE] when address spec. 20∼∞ [µs/SAMPLE]	Rated Output	±10 [V]	Direct Linearity	±½ LSB
		Frequency Resp. (sample mode)	±10 [V] ±20 [mA]	Temp Coefficient	for gain, ±5 ppm for zero point movement ±5 ppm of F.S./°C
Offset	±0.25 [mV] at 25°C±5°C	Swtch Static Time (sample & hold)	500 [kHz] (−3 dB)		
Direct Linearity	±0.01 [%]			Conversion Speed	20 [µs] max.
Switch Impedance	"ON" 50±20 [Ω] "OFF" 2000 [MΩ] 15 [PF] parallel		300 [ns]	Input Voltage Range	±10 [kΩ]
		Hold Characteristic	50 [µV/ms]	Input Impedance	10 [kΩ]
Load Impedance (estimate)	50 [kΩ] or less 500 [PF] or more	Acquire Time (for 20Vstep)	5 [µs] (0.01 [%]) of final value)	Output Level	"0"<0.4 [V] max "1">2.4 [V] min } TTL Connectable
Temperature Range	−10∼+55°C	Mode Control (sample mode)	+2 [V]∼5.5 [V]	Temperature Range	0 [°C]∼70 [°C]
Power Supply	AC 105∼125 [V] 42∼62 [Hz]	(hold mode)	−0.5 [V]∼+0.8 [V]	Power Supply	±15 [V] + 5 [V]
		Temp. Range	0°C∼70°C		
		Power Supply	±15 [V]		

5.3.2 Sample-and-hold

The sample-and-hold circuit is used to precisely convert changeable analog signals to digital signals. We have used a circuit which makes the reception of alternating signals difficult by making all ground circuits independent for analog input and output circuits and for digital control circuits. The specifications of the circuit are described in Table 6.

Table 7 12-bit AD Converter Characteristics

Input Voltage (V)	Output Voltage (V)
0.000	-0.005
0.100	0.093
0.200	0.190
0.300	0.293
0.500	0.488
0.700	0.693
1.000	0.991
2.000	1.987
3.000	2.983
5.000	4.976
7.000	6.973
10.000	9.966

5.3.3 AD Converter

Reducing time to the minimum is highly desirable in real-time simulation so that time relations, particularly time required for AD conversion, can be precise. We have used a modular-form 12-bit serial-comparator AD converter with 20 microsecond conversion time for precise conversion and ease of handling. The converter schematic is in Figure 50, the specifications are given in Table 6 and Figure 51 is an external view of the converter. Table 7 lists the actual measured values.

5.3.4 DA Converter

An 8-channel DA converter has been added to the simulator so that simulator output can be applied to the external operator, recorder and display. Input for the DA converter is binary 10-bit, output is a maximum of 10V, single polarity. Figure 52 is an external view of the DA converter.

Table 8 shows the actual measured values for the DA converter.

5.3.5 Controller

In planning the controller we considered the possibilities of multi-operation of two computers for real-time simulation and generalization, We decided on the following number of I/O channels.

(a) Digital input 4 channels

(b) Digital output 16 channels

Of these, the AD converter circuit uses one digital input circuit channel and the DA converter circuit, digital display and output control circuit use 12 digital output channels. Figure 47 is a schematic diagram of the circuits. Figure 53 is an external view of the controller. The commands in Table 9 were devised for computer control. Corresponding hardware was designed and fabricated.

In the following paragraphs we will discuss the AD converter circuits and the DA converter circuits in the controllers used by the simulator.

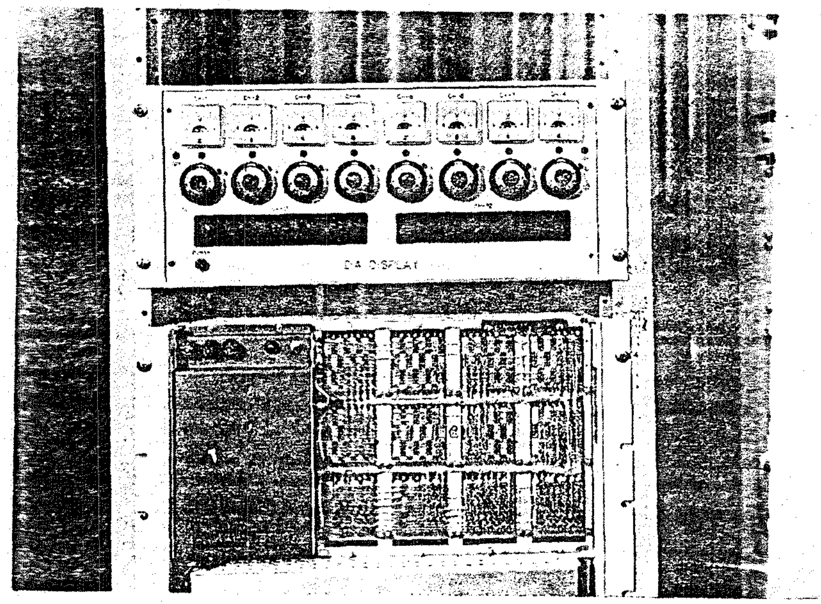


Figure 52 DA Converter

Table 8 DA Converter Characteristics

Digital Input	DA Converter Output							
DATA	CH-1	2	3	4	5	6	7	8
0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
1	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
2	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
4	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
8	0.08	0.08	0.08	0.08	0.08	0.08	0.08	0.08
16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16
32	0.32	0.32	0.31	0.32	0.32	0.31	0.31	0.32
64	0.63	0.63	0.63	0.63	0.63	0.63	0.63	0.67
128	1.26	1.26	1.26	1.26	1.26	1.26	1.26	1.26
256	2.53	2.53	2.53	2.53	2.53	2.53	2.53	2.53
512	5.05	5.06	5.05	5.06	5.06	5.05	5.05	5.06
1023	10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00

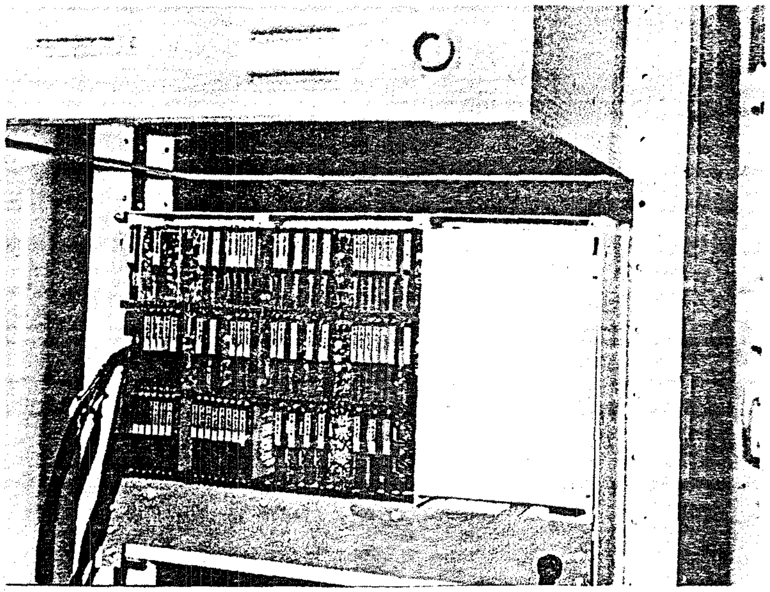


Figure 53 I/O Interface Controller

Table 9 Interface Commands

Device Name	Function	Symbols	Memory Content	Remarks
DA Converter and Line Printer	Outputs data if DA channel assignment is complete	OTA'041	170041	
	Assigns DA channel	OTA'241	170241	
	Skips next command if OTA'041 is executed	SKS'041	070041	
	Skips next command if line printer preparations are complete	SKS'141	070141	
	Directs print by line printer	OCP'041	030041	
	Outputs data to line printer	OCP'141	030141	
Digital Input No. 1	Starts direct transfer if No.1 flag is OFF	OTA'142	170142	HITAC-10 and Digital Volt-meter
	Inputs data if No.1 flag is ON	INA'1042	131042	
	Skips next command if No.1 flag is ON	SKS'042	070042	
	Skips next command if No.1 flag is ON	SKS'142	070142	
Digital Input No. 2	Inputs data if No.2 flag is ON	INA'1043	131043	Digital Voltmeter
	Skips next command if No.2 flag is ON	SKS'043	070043	
	Skips next command if No.2 flag is ON	SKS'143	070143	
	Assigns 200CH scanner channel	OTA'243	170243	
	Skips next command if 200CH scanner flag is ON	SKS'343	070343	
	Clears 200CH scanner flag	OCP'243	030243	
	Starts digital voltmeter measurement	OCP'043	030043	

Digital Input No.3	Inputs data if No.3 flag is ON	INA'1044	131044	Y-316
	Skips next command if No.3 flag is ON	SKS'044	070044	
	Skips next command if No.3 flag is ON	SKS'144	070144	
Digital Input No.4	Inputs data if No.4 flag is ON	INA'1040	131044	AD Con-verter
	Skips next command if No.4 flag is ON	SKS'040	070040	
	Skips next command if No.4 flag is ON	SKS'140	070140	
	Starts AD converter after assignment of 32CH multi-plexer	OTA'240	170240	
Interrupt	Places interrupt on exter-nal device (No.1)	OCP'046	030046	
	Places interrupt on exter-nal device	OCP'146	030146	

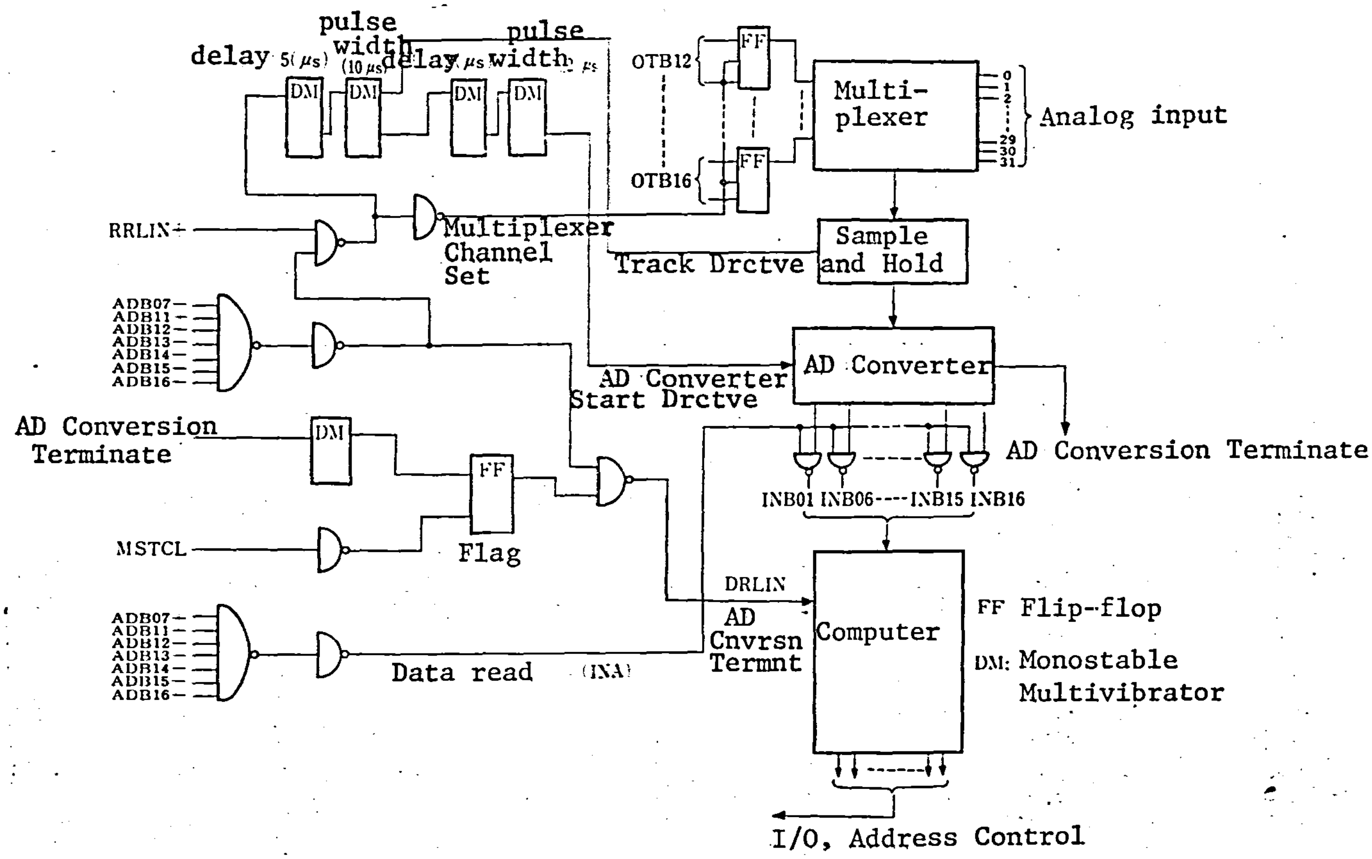


Figure 54 AD Converter Circuit

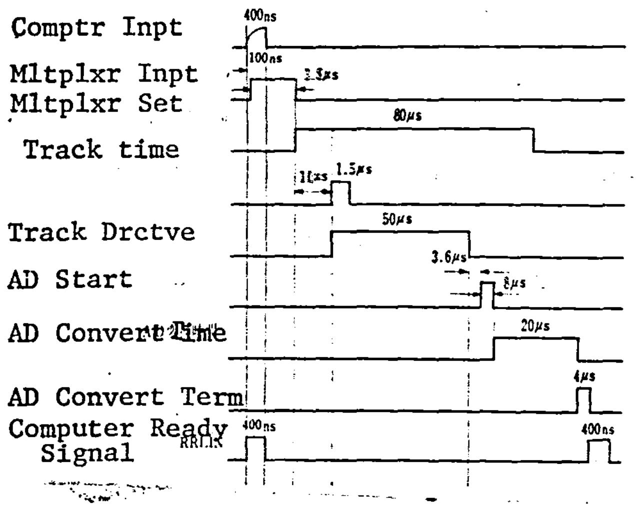


Figure 55 AD Converter Timing

(1) AD Converter Circuit

This circuit has functions such as multiplexer channel selection, issuing of hold directives for the sample-and-hold circuit and input to the computer of generated and converted digital AD converter start signals. Figure 54 is the schematic diagram of this circuit, and Figure 54 is the circuit's timing chart.

The multiplexer channel directives use the lower order 5 bits of the computer register enabling the selection of 32 channels. Of the AD converter's 11 output bits, computer input command enters the signed bit into the computer register's highest order bit and the 10 other bits into the register's 10 lower order bits. The circuit is set up so that the computer can be interrupted by a conversion end signal from the AD converter. The computer can execute other jobs during conversion time. Table 10 gives an example of an AD converter program.

Table 10 AD, DA Converter Program

```
                                  REL
                                  SUBR   ATOD,A
00000    0 000000     A           DAC    **
00001    74 0240                  OTA    '240
00002    000000                   HLT
00003    34 0040                  SKS    '40
00004    0 01 00003               JMP    *-1
00005    54 1040                  INA    '1040
00006    0 01 00005               JMP    *-1
00007    100400                   SPL
00010    100000                   SKP
00011    0 03 00013               ANA    ='3777
00012   -0 01 00000               JMP*   A
00013    003777                   END
```

```
                                  SUBR   DTOA,D
                                  REL
00000    0 000000     D           DAC    **
00001    74 0241                  OTA    '241
00002    000000                   HLT
00003   -0 02 00000               LDA*   D
00004    0 04 00012               STA    JMP
00005   -0 02 00012               LDA*   JMP
00006    74 0041                  OTA    '41
00007    0 01 00006               JMP    *-1
00010    0 12 00000               IRS    D
00011   -0 01 00000               JMP*   D
00012                 JMP         BSS    1
                                  END
```

(2) DA Converter Circuit

The DA converter circuit uses 8 channels in the digital output circuit. Figure 56 is a schematic diagram of the circuit. The display unit's X,Y-axis signals use two channels of the DA converter.

5.4 Display Unit

When testing combinations of engine control systems with the simulator, the display unit displays engine acceleration path, etc., on a compressor characteristics chart.

A storage-type CRT oscilloscope is used in the display unit and AD converter output is added to the X,Y axes. JR100H compressor characteristics are shown, as an example, in Figure 57. The specifications for the display unit are given here.

(1) Model	Techtronics 611
(2) CRT	11 inch
(3) Display	1024 bits x 1024 bits

For display software, we created subroutines which use the same procedures as the software in the laboratory computer center's HITAC 5020 X-Y plotter. Figure 58 and Table 11 show the interrelations and functions of these subroutines.

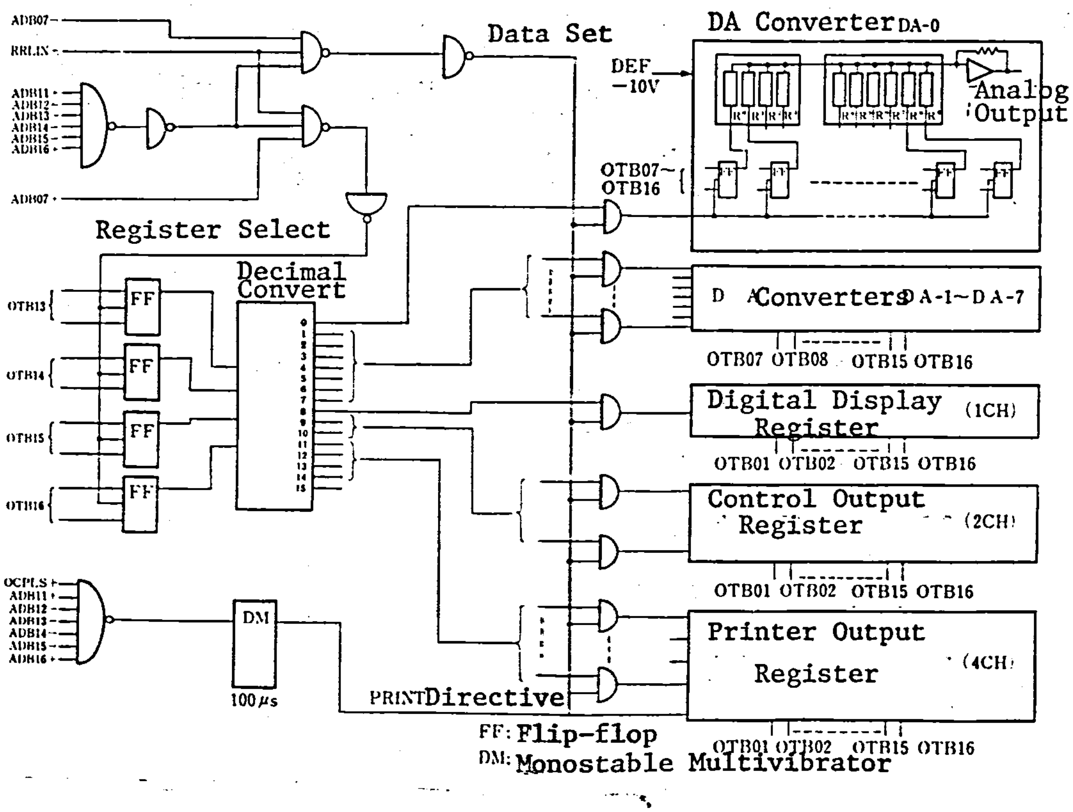


Figure 56 Digital Output Circuit

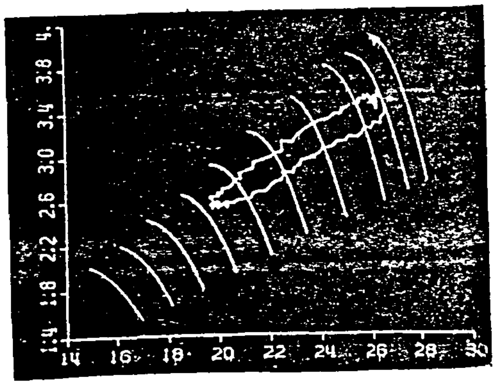


Figure 57 Display of Engine Test Data on Compressor Characteristics: Horizontal-axis Air Flow, Vertical-axis Pressure Ratio

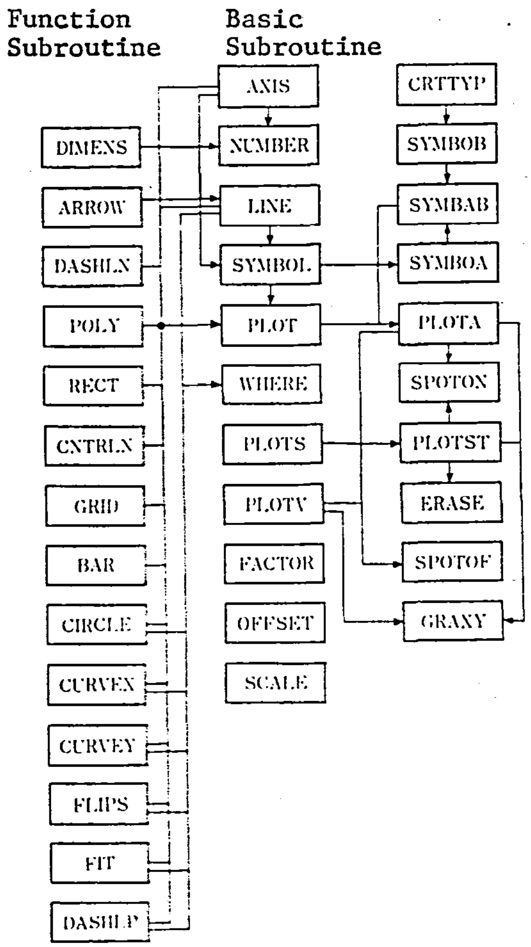


Figure 58 Subroutine Interrelations

Table 11 Display Subroutines

Name	Function
DIMENS	Draws dimension lines
ARROW	Draws curved lines and places arrows at the ends
DASHLN	Draws dotted or solid lines between two points
POLY	Draws positive polygons of n angles
RECT	Draws rectangles
CNTRLN	Draws grids
BAR	Draws bars
CIRCLE	Draws circles, arcs and and helixes
CURVEX	Draws x polynomials
CURVEY	Draws y polynomials
ELIPS	Draws ellipses
FIT	Draws 3 coordinate points by parabolic approximation
DASHLP	Draws curved broken lines
AXIS	Draws coordinate axes
NUMBER	Draws floating point data in decimal
LINE	Draws curved lines
SYMBOL	Draws alphamerics, numerics and symbols
PLOT	Moves spot from present point to specified point
WHERE	Derives present point of spot
PLOTS	Initializes
PLOTV	Performs close processing
FACTOR	Assigns scale factor
OFFSET	Assigns scale factor
SCALE	Performs scaling
CRTTYP	Draws ASCII characters
SYMBOB	Entry only when drawing ASCII characters
SYMBAB	Draws ASCII characters and special characters
SYMBOA	Entry when drawing ASCII characters and special characters
PLOTA	Draws spot on straight line from present location to specified location
SPOTON	Spot ON
PLOTST	Initializes
ERASE	Erases display
SPOTOF	Spot OFF
GRAXY	Moves spot to specified location

6. Conclusion

We found excellent conformity between test data on both static and dynamic characteristics with the real-time simulator for engine characteristics described here. Simulation is very faithful compared to that in the analog format and operability is simple. Using assembler language we achieved a sample time of 4ms and in that range no practical problem was presented with software for real-time simulation. There is still room for improvement by speeding up the multiplexer and sample-and-hold and for faster use of the interrupt function. A method, as stated in Section 3, which performs matching computations in advance, stores the results in memory and references that memory for the status of an engine at any time has deficiencies for simulation programming. In generalizations where the number of independent variables is large, as with dual- and triple-engines, would require very large memory. At the present time, development has been completed on a simulation program which includes matching computations. An announcement of that development is scheduled for the second phase of this report.

With devices, too, the 0.1% element precision considered necessary for tests of engine control systems, has been satisfied. Frequency characteristics, along with other important factors, were excellent. The I/O interface was designed for generalization, and it is possible to perform multi-processing with other computers. Using the simulator, we anticipate further progress in real-time simulation of multi-engines.

Reference Bibliography

1) Nishio, Endo, Sugiyama, et.al., "On the Dynamic Characteristics of the JR100H Lift Jet Engine," NAL TR-238, 1971.

2) Larrowe, V. L., "A Dynamic Performance Computer for Gas Turbine Engines," WADC TR-54-577 Part 2, 1955.

3) Fawke, A. J. and H. I. H. Saravanmuttoo, "Digital Computer Methods for Prediction of Gas Turbine Dynamic Response," SAE 710550, 1971.

4) Oyama; "Methods of Computing the Dynamic Characteristics of Aircraft Gas Turbine Engines," Collected Speeches of the Kikai Gakkai, No. 211-505

5) Nishio, Endo, Sugiyama, et.al., "Jet Engine Digital Control (I)," NAL TR-281, 1972.

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