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PROCESS RESEARCH ON POLYCRYSTALLINE SILICON MATERIAL

(PROPSM)

QUARTERLY REPORT NO. 6

MARCH 1, 1982 - JUNE 30, 1982

CONTRACT NO. 955902

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The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initial a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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QUARTERLY REPORT

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1.0 INTRODUCTION

The emphasis of this program has been changed from the design, development, and fabrication of an automated production process to the investigation of polycrystalline silicon to determine the mechanisms affecting conversion efficiency and to the development of processes that take full advantage of its potential as a photovoltaic material. In light of this change of emphasis the name of the program has been changed from Module Experimental Process Development Unit (MEPSDU) to Process Research of Polycrystalline Silicon Material (PROPSM).

During this quarter a revised program plan was prepared describing the program effort for the PROPSM contract. A description of the technical program plan appears in Section 2.2. The first task is to determine the mechanisms limiting performance in polycrystalline silicon. The initial set of experiments in this task entails the fabrication of cells of various thicknesses for four different bulk resistivities between 0.1 and 10 Ω-cm. The results for the first two lots are presented in Section 2.3.

2.0 TECHNICAL PROGRESS

2.1 Documentation

The following reports were submitted during this quarter:

26 Technical Progress Report No. 16

27 Quarterly Report No. 5

28 Program Plan for PROPSM

29 Technical Progress Report No. 17

30 Technical Progress Report No. 18

31 Technical Progress Report No. 19

2.2 Revised Program Plan

The emphasis of the program is now on the investigation of polycrystalline silicon to determine the mechanisms affecting conversion efficiency and on developing processes that take full advantage of its potential as a photovoltaic material. The initial effort under Task #1 will be to determine the Mechanisms Limiting Performance in polycrystalline material. Task #2 efforts will thus be the Development of Processes to Improve Performance of polycrystalline solar cells. The efforts to be performed are described in the following sections.

TASK 1 - Mechanisms Limiting Performance

EXPERIMENT 1 - Bulk Resistivity Experiments

Cells will be fabricated using a minimum of four different bulk resistivity values in the range 0.1 to 10 Ω-cm. For each bulk resistivity, wafers of thickness 300, 250, 200, 150, 100, 50 microns will be processed into solar cells using a well known high efficiency cell process with a back surface field (BSF). The results of short-circuit current as a function of bulk resistivity should provide a measure of the effective minority carrier diffusion length as compared to that of single crystal silicon. The dependence of open-circuit voltage on wafer thickness will also provide information on the minority carrier diffusion length for the various bulk resistivities. The dependence of open-circuit voltage on bulk resistivity will help to identify the voltage limiting mechanisms as compared to single crystal silicon where the voltage limiting mechanism shifts from the bulk to the emitter as the bulk resistivity drops from 10 Ω-cm to 0.1 Ω·cm. Comparison of polycrystalline material results with single crystal results should indicate whether the bulk is controlling the open-circuit voltage or whether grain boundary effects dominate.

EXPERIMENT 2 - Silicon Substrate Experiments

A variety of 10cm x 10cm polycrystalline wafers will be processed into samples containing 400 isolated 0.5cm x 0.5cm mini-cells. Electrical performance of each of the mini-cells will be measured. Contour plots of I_{sc}, V_{oc}, P_{max} and diode factor will be made. In regions of interest (such as very high or low performance) localized V_{oc} probing or spot scanning of I_{sc} will be conducted. Attempts will be made to equate performance to macroscopic structure (i.e., placement in the brick) and microscopic structure (i.e., grain boundaries, twins, etc.). Attempts will be made to understand the functional dependence of I_{sc}, V_{oc}, and diode factor on the various structures.

Interpretation of the results of these two experiments will aid in determining the mechanisms limiting cell performance. This will be used to update the theories of polycrystalline cell performance and to select for further investigation those process techniques or process modifications which may lead to the most significant improvements in cell performance.

TASK 2 - Processes To Improve Performance

The measurements and analysis in Task 1 will determine the types of process developments most likely to aid cell

efficiencies. Process areas to be investigated may include, but not be limited to, the following:

1. Hydrogen Passivation of Grain Boundaries - A number of studies have been conducted in the area of hydrogen passivation of grain boundaries. The use of hydrogen to take up dangling bonds is a proven technology, especially for α-Si. The value of this method for a large grain polycrystalline silicon remains to be shown.

2. Enhanced Diffusion Down Grain Boundaries - Light diffusion down grain boundaries enhances current collection near the boundary. The use of selective etching including plasma etching can lead to enhancing the diffusion paths down the grains. It may then be possible to get increased performance near the grain boundary, at least for shorter wavelength light.

3. Gettering - Gettering has been shown to improve cell performance when there are impurities present. The first step would be to determine if gettering improves cell performance and, if it does, to determine whether the improvement is due to changes in the grain bulk or at the grain boundaries.

4. Surface Passivation - The irregularity of polycrystalline silicon surface compared to that of single crystal silicon, may result in higher surface recombination velocities and lower open-circuit voltages. If this hypothesis is confirmed during Task 1, the efforts to passivate the front surface, such as growth of a thin oxide or deposition of a thin window layer of higher band gap material like α-Si or α-SiC, may significantly improve cell open-circuit voltage.

The results of these process developments will be analyzed to include the effects on cell efficiency, process cost, compatibility with other cell processes, and the applicability of the process to particular polycrystalline materials.

2.3 Fabrication of Cells of Various Thicknesses

The process sequence for the solar cells is shown in Figure 1 and is described in detail in Reference 1. This is a standard BSF space-cell process that produces high efficiency cells on all single crystal thicknesses. (It did not include texturing, double layer antireflective coating (AR) or back surface reflection, which are required to produce maximum efficiency from 2 mil cells.) The cells are 2cm x 2cm in size with space type Ti/Pd/Ag metallization and Ta_2O_5 single layer AR coating.

In each experiment a particular bulk resistivity is selected. Polycrystalline wafers (usually supplied by Semix) are coprocessed with single crystal wafers of similar bulk resistivity. A CP-type etch (a mixture of HF-acetic-nitric acids) is utilized to thin the wafers to various thicknesses between 50 and 300 microns. After processing, the cells are measured at AMO, 135.3 mW/cm^2 and 25^oC. In addition the spectral response of the short-circuit current is compared by measuring the "red" current using a #2408 Corning filter and by measuring the "blue" current using a #9788 Corning filter.

The first two lots were completed during this quarter. Lot #1 was fabricated using 1 Ω-cm silicon, while Lot #2 used 3 Ω-cm silicon. The results are summarized in Tables #1-5. The averages in these tables do not include cells from the following two categories.

1. Severe shunting is prevalent on many of the thinner cells both single and polycrystalline. This may be due to penetration of the aluminum paste through the entire wafer. High yields of thin cells with this process require more care with paste application and firing profiles. The use of polycrystalline silicon does not appear to affect the incidence of the shunting.

2. A number of polycrystalline cells in Lot #1 had low current and voltage, but with good fill factors. Such curves have been seen in the past in material with degraded minority-carrier lifetime (see, for example Reference 2). It is likely that some wafers or parts of wafers in this lot had unusually low minority-carrier lifetime.

The results of the single crystal controls for Lots #1 and #2 were similar, with all parameters improving with increasing thickness, because a thicker cell absorbs more light in the bulk and produces more electron-hole pairs. The reduced open-circuit voltage for thinner cells indicates that the BSF may not be the dominant mechanism controlling the voltage for these bulk resistivities. Lot #2 controls had appreciably better performance than Lot #1 controls, i.e., peak power of 75-76 mW versus 73 mW for 250 micron thickness cells. This improvement was entirely due to higher open-circuit voltage, i.e., 605-607 mV versus 597 mV at 250 microns. This of course is not consistent with the expected dependence on bulk resistivity; that is, higher bulk resistivity yields lower cell open-circuit voltage which could be due to a combination of higher minority-carrier lifetime (allowing more influence of the BSF) for the 3 Ω-cm silicon, or it could be the result of improved processing (although the process parameters for the two lots were supposedly identical).

The polycrystalline cells do not show improvement of all parameters with increasing thickness. Indeed the highest open-circuit voltage was obtained for the thinnest cells, indicating that for this polycrystalline silicon the BSF may be able to significantly enhance the voltage. While the dependence of short-circuit current and red current is different in the two lots, the ratio of polycrystalline to single-crystal short circuit current and red current is the highest for the thinnest cells in both lots. This is an indication that the first 50 or 100 microns of the polycrystalline material is reasonably efficient at current collection. However, collection of carriers deeper than 100 microns is not nearly as efficient for the polycrystalline cells as for the single-crystal solar cells.

The blue current shows little dependence on thickness, bulk resistivity or crystal structure. As expected, it is more a function of the process sequence.

3.0 SCHEDULE AND PLANS

During the next quarter the set of experiments to fabricate polycrystalline cells of various thicknesses will continue, including one lot with higher bulk resistivity, approximately 8 Ω-cm, and another with lower bulk resistivity, approximately 0.3-0.6 Ω-cm. Efforts will begin to prepare for the silicon substrate experiments with 400 mini-cells on one wafer. In addition, efforts will continue on the MEPSDU Summary Report.

TABLE #1

I_{sc} (mA) AT AM0 - 25°C

LOT #	CRYSTAL TYPE	BULK RESISTIVITY (Ω-cm)	THICKNESS (MICRONS) 50	100	150	200	250	300
1	SINGLE	1	-	150.5	155	159	159	-
1	POLY	1	-	140	129	132	133	-
2	SINGLE	3	140	151	158	154	158	160
2	POLY	3	128	135	129	127	134	132
1	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	-	.93	.83	.83	.83	-
2	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	.91	.9	.82	.83	.85	.83

TABLE #2

V_{OC} (mV) AT AM0 - 25°C

LOT #	CRYSTAL TYPE	BULK RESISTIVITY (Ω-cm)	THICKNESS (MICRONS) 50	100	150	200	250	300
1	SINGLE	1	-	590.5	593	600	597	-
1	POLY	1	-	576	562	566	571	-
2	SINGLE	3	593	603	607	606	604	607
2	POLY	3	565	-	562	561	559	559
1	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	-	.98	.95	.94	.96	-
2	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	.95	-	.93	.93	.93	.92

TABLE #3

RED (SHORT CIRCUIT CURRENT IN mA) AT AM0 - 25°C

LOT #	CRYSTAL TYPE	BULK RESISTIVITY (Ω-cm)	THICKNESS (MICRONS) 50	100	150	200	250	300
1	SINGLE	1	-	82	84	88	89	-
1	POLY	1	-	74	63	65	66	-
2	SINGLE	3	72	80	86	84	88	86
2	POLY	3	65	71	62	63	68	66
1	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	-	.90	.75	.74	.74	-
2	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	.9	.89	.72	.75	.77	.77

TABLE #4

BLUE (SHORT CIRCUIT CURRENT IN mA) AT AM0 - 25°C

LOT #	CRYSTAL TYPE	BULK RESISTIVITY (Ω-cm)	THICKNESS (MICRONS) 50	100	150	200	250	300
1	SINGLE	1	-	31	34	33	34	-
1	POLY	1	-	30	32	34	32	-
2	SINGLE	3	33	34	33	36	35	37
2	POLY	3	31	31	33	33	34	34
1	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	-	.97	.94	1.03	.94	-
2	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	.94	.91	1.0	.92	.97	.92

TABLE #5

I_{sc} X V_{oc} PRODUCT (IN mW) AT AM0 - 25°C

LOT #	CRYSTAL TYPE	BULK RESISTIVITY (Ω-cm)	THICKNESS (MICRONS) 50	100	150	200	250	300
1	SINGLE	1	-	88.9	91.9	95.4	94.9	-
1	POLY	1	-	80.6	72.5	74.7	75.9	-
2	SINGLE	3	83	91.1	95.9	93.3	95.5	97.2
2	POLY	3	72.3	-	72.5	71.2	74.9	73.8
1	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	-	.91	.79	.78	.80	-
2	RATIO	$\frac{\text{POLY}}{\text{SINGLE}}$	.87	-	.76	.76	.78	.76

CELL PROCESS SEQUENCE

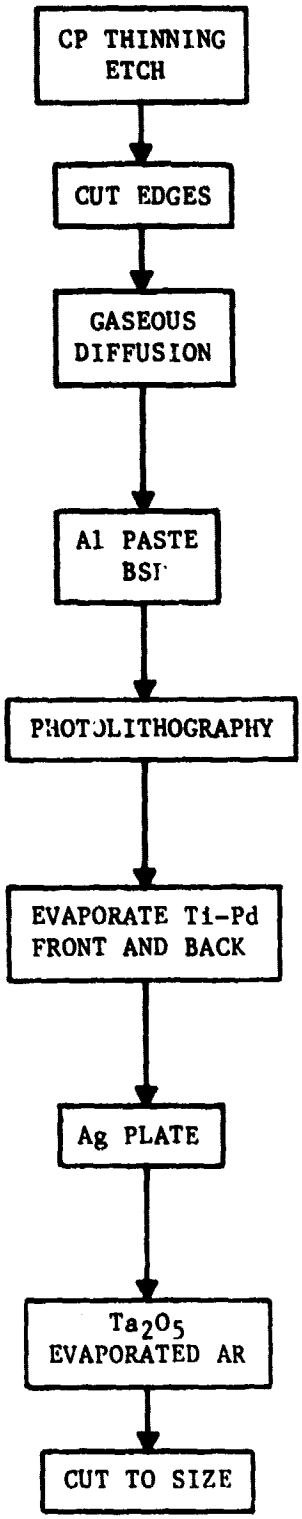

FIGURE 1

REFERENCES

1. G. Storti, J. Culik and C. Wrigley, "Development of a High Efficiency Thin Silicon Solar Cell", Final Report, JPL Contract No. 954883, December 1980.

2. J. H. Wohlgemuth and M. N. Giuliano, "Analysis of the Effects of Impurities in Silicon", Final Report, JPL Contract No. 955307, January 1980.