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June 20, 1983

ANNUAL REPORT
PHOTOVOLTAIC MODULE BYPASS DIODE ENCAPSULATION

Prepared Under JPL Contract 956254

GENERAL ELECTRIC

ADVANCED ENERGY PROGRAMS DEPARTMENT
P.O. Box 527
King of Prussia, PA 19406

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ANNUAL REPORT

Photovoltaic Module Bypass Diode Encapsulation

Prepared Under JPL Contract 956254

N.F. Shepard, Jr., Program Manager

The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of flat-plate solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

GENERAL ELECTRIC

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N.F. Shepard, Jr.	Program Manager and Principal Technical Contributor
R. Landes	Survey of Diode Types
J. Parker	Thermal Analysis of Encapsulated Bypass Diode
A. J. Yerman	Diode Thermal Resistance Measurements
D. M. Mullings	Encapsulated Bypass Diode Costing Analysis
T. S. Chan	Bypass Diode Reliability Assessment

Mr. R. S. Sugimura was the JPL Project Manager. His guidance and helpful suggestions are gratefully acknowledged.

ABSTRACT

The design and processing techniques necessary to incorporate bypass diodes within the module encapsulant are presented in this annual report. A comprehensive survey of available pad-mounted PN junction and Schottky diodes led to the selection of Semicon PN junction diode cells for this application. Diode junction-to-heat spreader thermal resistance measurements, performed on a variety of mounted diode chip types and sizes, have yielded values which are consistently below $1^{o}C$ per watt, but show some instability when thermally cycled over the temperature range from -40 to $150^{o}C$.

Based on the results of a detailed thermal analysis, which covered the range of bypass currents from 2 to 20 amperes, three representative experimental modules, each incorporating integral bypass diode/heat spreader assemblies of various sizes, were designed and fabricated. Thermal testing of these modules has enabled the formulation of a recommended heat spreader plate sizing relationship. The production cost of three encapsulated bypass diode/heat spreader assemblies were compared with similarly rated externally-mounted packaged diodes.

An assessment of bypass diode reliability, which relies heavily on rectifying diode failure rate data, leads to the general conclusion that, when proper designed and installed, these devices will improve the overall reliability of a terrestrial array over a 20 year design lifetime.

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SUMMARY

SECTION 1
SUMMARY

The integration of bypass diodes within photovoltaic modules may be necessary to limit the potential for reverse voltage "hot-spot" heating if the individual modules are evaluated to the requirements of proposed product standards for flat-plate photovoltaic modules and panels. In such cases, where the use of module bypass diodes is indicated, the mechanical and electrical integration of these diodes within the module encapsulation system is a viable design solution which offers many advantages over conventionally packaged diode mounting methods. A diode/heat spreader plate assembly of the configuration shown in Figure 1-1, where the pad-mounted diode chip is soldered to the center of a square copper plate, can be conveniently laminated within the module encapsulation system as shown in Figure 1-2. This arrangement, with the diode/heat spreader plate assembly positioned behind the solar cell circuit, results in a negligible increase in encapsulant volume with no increase in module frontal area. The module encapsulation system also functions to electrically isolate the diode installation.

A comprehensive survey of available pad-mounted PN junction and Schottky diodes resulted in the selection of Semicon PN junction diode cells for this application. The use of Schottky devices in internal module bypass circuits was ruled-out because of higher level array circuit design considerations which are discussed in Section 3.1.

The results of diode junction-to-heat spreader thermal resistance measurements were used in a multi-node thermal model to predict the diode junction temperature as a function of copper heat spreader plate size and diode heat dissipation. A 130^{o}C ethylene vinyl acetate temperature limitation was used to establish the criterion for determining the required plate size for a specified bypass current.

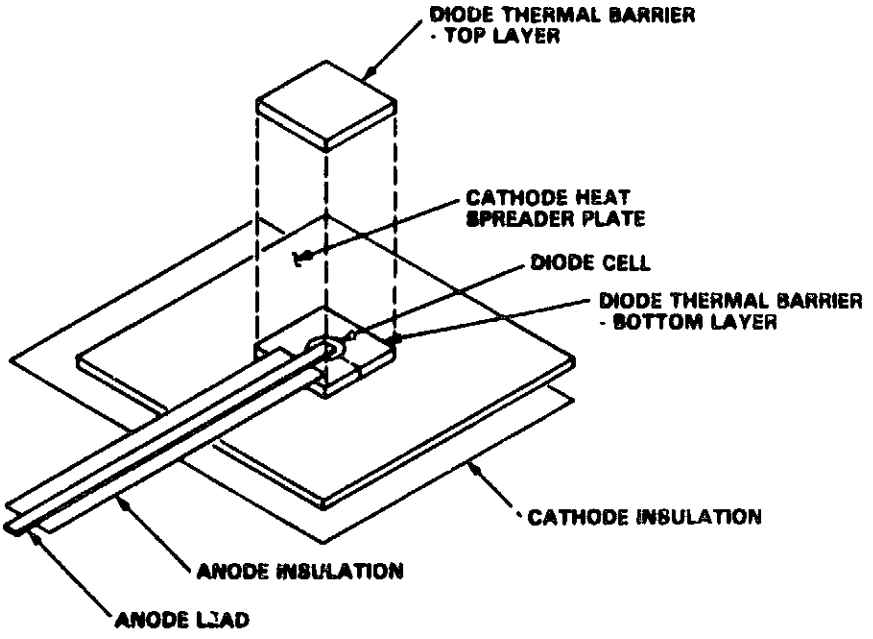

Figure 1-1. Diode/Heat Spreader Configuration

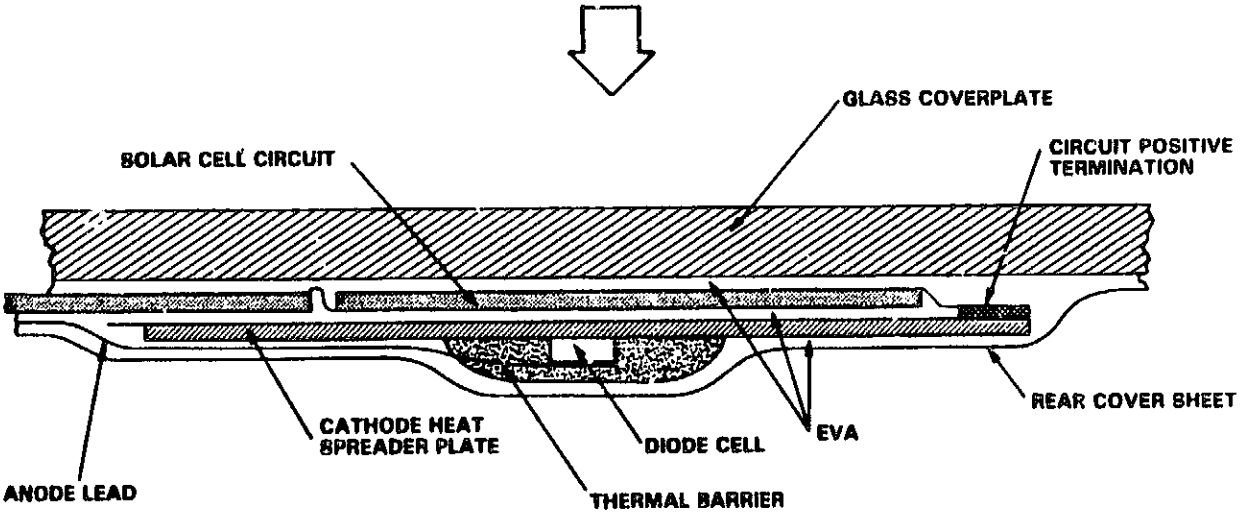

Figure 1-2. Typical Glass Superstrate Lamination Stack-up with Encapsulated Bypass Diode

Three module segments, each consisting of twenty-four square solar cells, 100 mm on a side, arranged in different circuit configurations and with different size heat spreaders, were designed and fabricated to function as test specimens for the experimental determination of the heat spreader temperature rise as a function of diode heat dissipation. The data from these characterization tests were used to develop the relationship shown in Figure 1-3. It is recommended that this curve be used as a design guide in the sizing of copper heat spreader plates for encapsulated bypass diode installations.

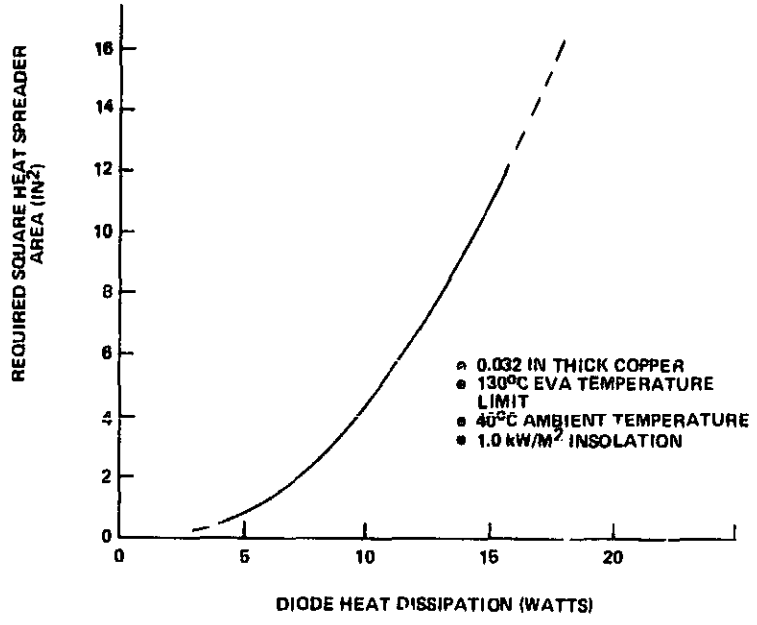

Figure 1-3. Recommended Encapsulated Diode Heat Spreader Plate Size Based on Limited Experimental Data

A detailed manufacturing cost comparison of encapsulated bypass diode cells of several current ratings with comparable externally-mounted packaged diodes has revealed no strong cost-related incentive for one approach over another. The decision to package a bypass diode as an integral part of a photovoltaic module, whether externally or internally-mounted, should be made by the module designer based on requirements related exclusively to the ability of the module to survive the "hot spot" heating conditions. Depending on the module circuit configuration, it may be necessary to employ multiple bypass diodes as part of the module design to insure satisfactory performance during this test exposure. This is particularly true for

residential applications where the requirements for dc system voltage and array and module size tend to dictate a relatively large number of series-connected cells per module. In such cases, where the requirement for multiple bypass diodes would require the repeated penetration of the module encapsulant for connections to externally-mounted diodes, it would seem logical to mount the diodes as an integral part of the encapsulation system so that no intermediate penetrations are required.

The use of a single module-mounted bypass diode must be questioned on the basis of intended function since such an application will not enhance the survivability of the module in the hot-spot heating test environment, as defined by the proposed UL standard, and the inclusion of a single bypass diode at the module level may only complicate the array circuit design by introducing problems of current sharing among these individual module diodes if the array circuit designer wishes to employ a parallel-connected group of modules as a circuit element. Under such circumstances current sharing among parallel-connected diodes can be forced by the inclusion of an appropriately selected series resistance value in each bypass path. The magnitude of the voltage drop in each forward conducting bypass path will be significantly increased by the presence of this additional resistance. This, in turn, may cause a disproportionately large decrease in the power output capability of the affected source circuit at the system output voltage which is determined by the maximum power operating point of the unaffected source circuits. This shortcoming can be avoided by the use of an externally-mounted bypass diode which is selected by the array circuit designer and sized to accommodate the bypass current from all parallel-connected modules in the bypass group. Virtually all bypass current will be through this large external diode if its forward voltage drop, when passing this current, is significantly less than the individual module diodes. Such a situation can exist if the large external diode is a Schottky device and the single module diodes are PN junction devices or if multiple, series-connected PN junction devices are used as module bypass diodes with a single large PN junction diode used as the array bypass diode.

The photovoltaic module bypass application is not particularly demanding relative to the conventional rectifying application for power diodes. The operating environment for a photovoltaic module bypass diode is characterized by a prolonged exposure to a low level reverse voltage (~0 vdc during nighttime periods and typically 15 vdc during daytime periods). Under these reverse voltage conditions the diode temperature varies from near the ambient air temperature during nighttime periods to a temperature approximately equal to the module operating temperature during daytime periods. Occasionally the diode may be required to perform its bypass function by conducting a portion of the circuit current in the forward direction. Under these conditions the diode junction temperature could approach the maximum rated value, but the time spent in this mode of operation is probably several orders of magnitude less than the time spent in the reverse voltage operating mode.

Diode failure rate data is available for a rectifying application where the excitation source is a 60 Hz sinusoidal waveform and where failure is defined as a relatively small change in reverse leakage current. The application of this data to the dc blocking operation of a bypass diode leads to the general conclusion that, with proper design, the bypass diode failure rate will be sufficiently low so that their inclusion can be justified on the basis of an overall array reliability improvement over a 20 year design lifetime.

The thermal resistance between the diode junction and the heat spreader is a critical element in the determination of diode junction temperature (and, hence, reliability) under forward conducting conditions. The stability of this thermal resistance with temperature cycling requires further study in the light of the results from a limited thermal cycling exposure test where twelve specimens were cycled 100 times between the extremes of -40 and 150^{o}C. This temperature cycling exposure, which is unquestionably severe in terms of the magnitude of the temperature extremes, resulted in significant increases in the thermal resistance across the soldered interface between the silicon die and the heat spreader. Such changes in thermal resistance are indicative of the propagation of void areas in the solder joint.

SECTION 2
INTRODUCTION

SECTION 2
INTRODUCTION

This research is an outgrowth of the bypass diode integration activity reported in Reference [1], which led to the conclusion that the direct mounting of diode chips onto copper heat spreader plates for lamination within the module encapsulant offers an attractive installation option with the following advantages:

- the thermal resistance from the diode junction-to-heat sink can be somewhat lower with the chip, since the case, which is associated with the packaged diode, has been eliminated and replaced with a relatively large heat spreader plate,
- the mounted chip is much smaller than the packaged diode and therefore its placement in the module is not limited to locations that are large enough to accommodate the rather bulky diode case, and
- the environmental protection and electrical insulation are provided by the module encapsulant.

The original objective of this contract was to research the design and processing techniques necessary to incorporate a bypass diode/heat spreader assembly within the module encapsulant. This objective was broadened, as a result of a subsequent contract modification, to include the more general application of diodes, used in both bypass and blocking modes, to modules in high voltage and high power systems. The program activity is organized into nine major tasks as listed below.

Task 1 - Requirements Definition
Task 2 - Design Synthesis and Development
Task 3 - Component and Module Mock-up Fabrication
Task 4 - Bypass Diode Cost Comparison
Task 5 - Bypass Diode Reliability Considerations
Task 6 - Parallel Bypass Diode Load Sharing Considerations

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1. "Bypass Diode Integration - Final Report", DOE/JPL 955894-5, December 11, 1981

Task 7 - Thermal Cycling Endurance of Soldered Diode Cells
Task 8 - Bypass Diode/Enclosure Designs
Task 9 - Blocking Diode/Enclosure Designs

As illustrated in Figure 2-1, this annual report covers the results of the first seven task activities which were completed as of this reporting date. Under Task 1 the requirements for incorporating PN junction or Schottky diode chips into the module encapsulant system were developed. Available diode chips of both types, rated for forward currents over the range from 2 to 20 amperes, were investigated. Sources of supply were identified and diodes were characterized by mounting configuration, junction temperature limitation, and by forward current-voltage relationship. Functional requirements related to the integration of bypass diodes into a module laminate, including encapsulant temperature limitations, electrical insulation, anode lead attachment and environmental protection, were investigated.

The Task 2 activity addressed the issues related to the design synthesis of the diode/heat spreader assemblies for the forward current range of 2 to 20 amperes. A thermal analysis was performed to permit the selection of the required square copper plate size as a function of diode heat dissipation. Encapsulation considerations included the selection of appropriate insulating materials, anode lead routing, and the integration of the heat spreader with the internal current collecting buses.

Task 3 included the fabrication and test of various bypass diode/heat spreader assembly mock-ups including the encapsulation of these assemblies within simulated modules. As a final verification of the design concept, diode/heat spreader assemblies of six different sizes were encapsulated in three separate modules, each configured with twenty-four square solar cells, 100 mm on a side, to produce short-circuit currents of 3, 12 and 18 amperes.

A comparative cost assessment of the encapsulated bypass diode packaging approach with the more conventional externally-mounted enclsoure method was performed under Task 4.

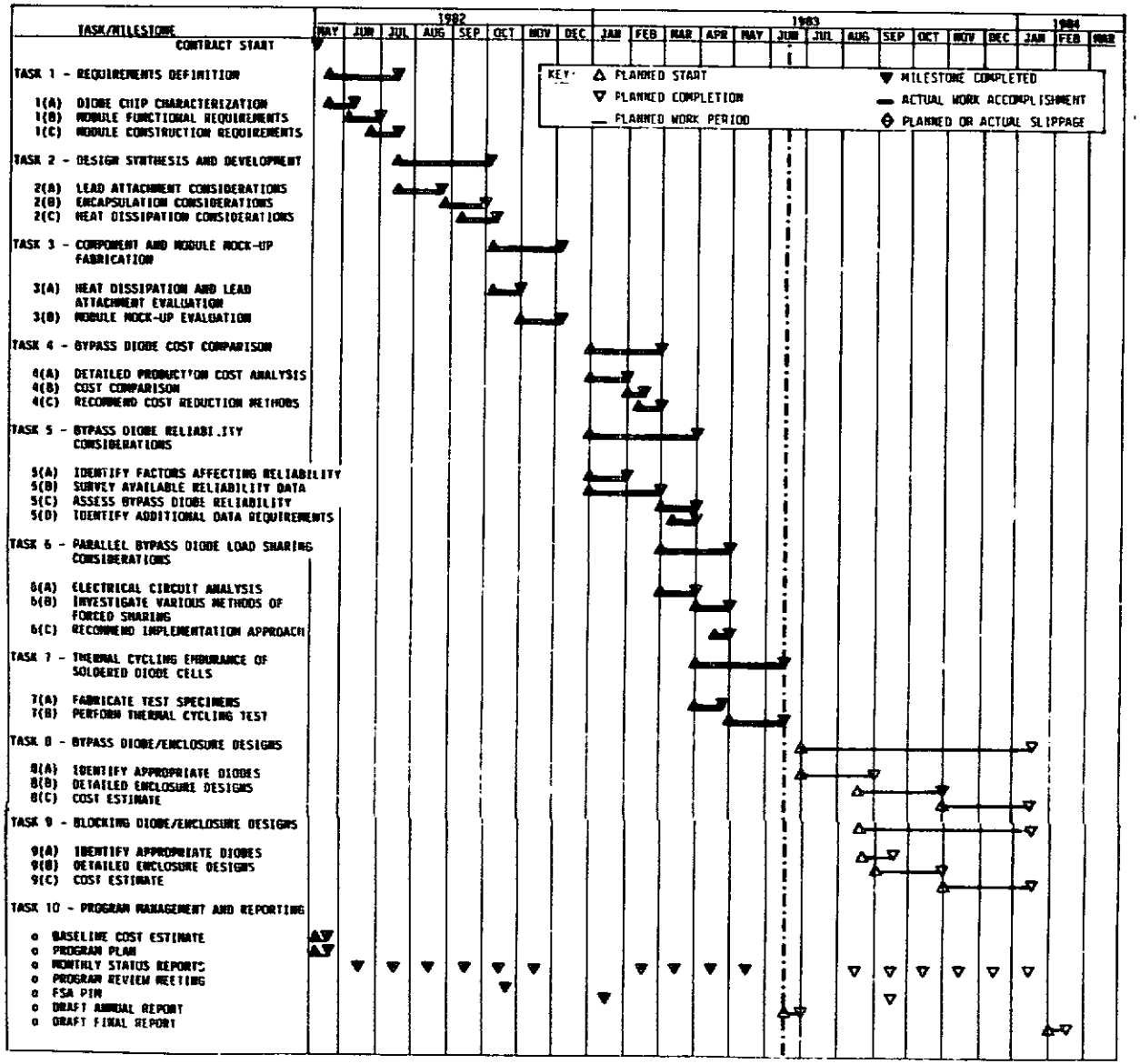


Figure 2-1. Master Program Schedule

The factors affecting the reliability of rectifying diodes used in photovoltaic array bypass applications were addressed as part of Task 5. Available diode failure rate data were assembled and used to estimate the reliability of bypass diodes.

The current sharing in parallel-connected diodes was investigated under Task 6. The circuit analysis performed as part of this activity included the parallel connection of PN junction diodes of the same type as well as a PN junction diode in parallel with a Schottky diode. In all cases the effects of an imposed junction temperature difference and series resistance in the bypass paths were evaluated.

The stability of the solder joint between the diode cell and the heat spreader, which is crucial to the thermal dissipation capability of an encapsulated diode package, was experimental investigated by a limited thermal cycling exposure as defined under Task 7.

SECTION 3

TECHNICAL DISCUSSION

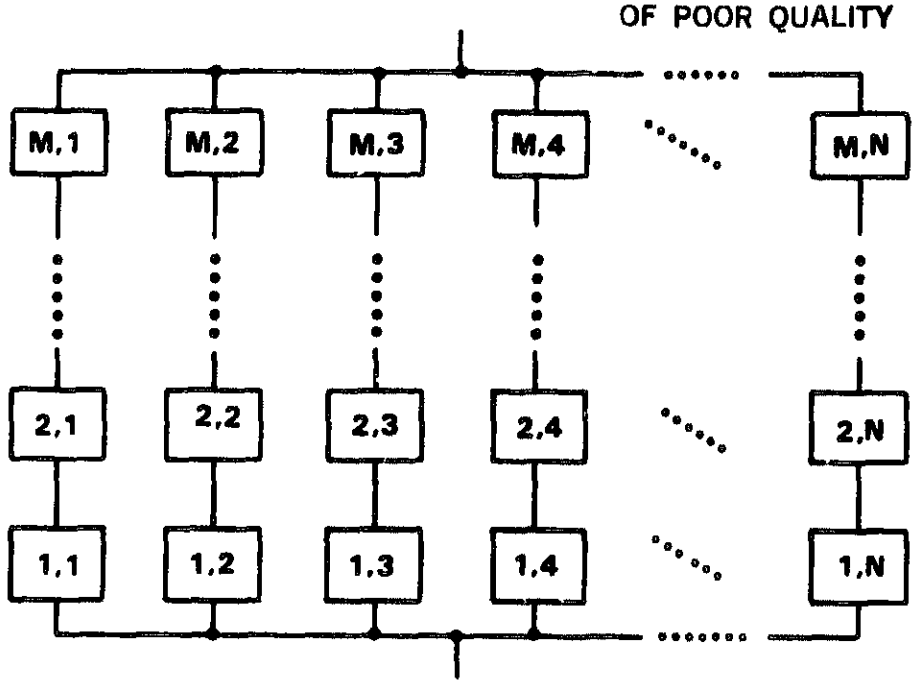
SECTION 3
TECHNICAL DISCUSSION

3.1 BYPASS DIODE FUNCTIONAL REQUIREMENTS

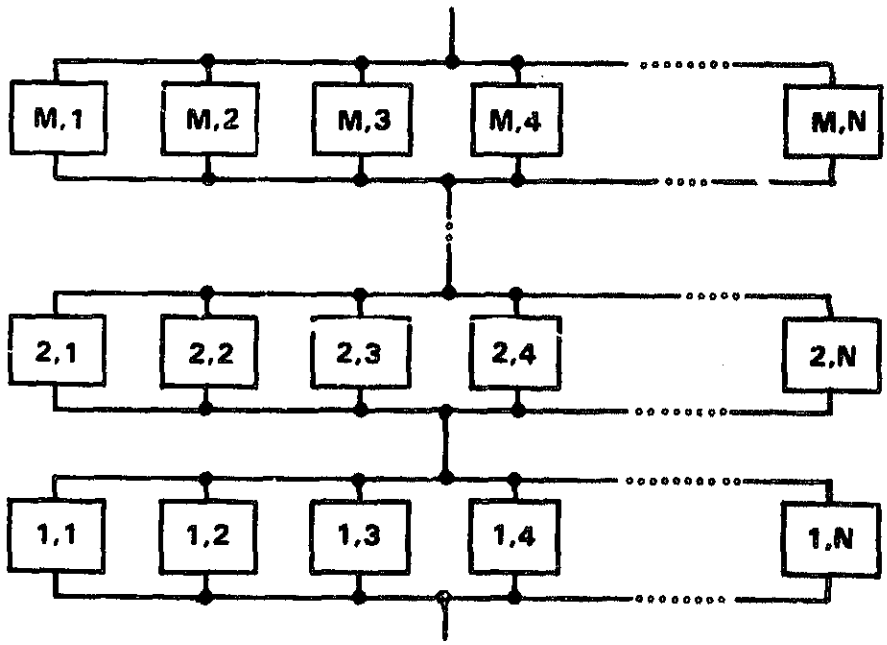
Bypass diodes are often used in photovoltaic array circuits to perform the following functions:

- Provide a parallel path for current around faulty module circuit elements so that the source circuit current capability is not limited by any more than the approximate short-circuit current capability of elements within the bypassed group.
- Limit the reverse voltage that can be developed across the bypassed group to the forward voltage drop of the forward conducting bypass diode. This limits the amount of reverse voltage "hot-spot" heating that can occur within an affected solar cell of the bypassed group.
- Provide a parallel path for current, when connected externally around a module, so that the removal of the module from an illuminated array does not create an arc.

the electrical interconnection of modules to form an array is generally accomplished in one of the two ways diagrammed in Figure 3-1. The first of these methods, called "Parallel-connected Series Strings" in Figure 3-1(a), has been widely used but is characterized by a disproportionately high power loss due to short-circuit current mismatch among the modules within each individual series string. This mismatch loss can be minimized by interconnecting the modules as shown in Figure 3-1(b), referred to as the "Series-connected Parallel Groups" arrangement. With this latter interconnection scheme, where the number of parallel-connected modules is relatively large, the modules can be randomly placed within the array circuit with little impact on the resultant total array short-circuit current capability. However, when bypass diodes are incorporated into a circuit of this configuration it is necessary to carefully evaluate the sizing of these diodes relative to the short-circuit current capability of the entire parallel group. Modules with individual bypass diodes may require the additional protection of a single bypass diode which is connected across each parallel



(a) Parallel-connected Series Strings



(b) Series-Connected Parallel Groups

Figure 3-1. Alternative Module-to-Module Interconnection Approaches

group and sized to carry the total short-circuit current produced by all modules in the parallel group at a voltage drop substantially lower than the individual module bypass diodes.

The driving requirement that forces the module designer to consider the use of bypass diodes is the "hot-spot" endurance test specified in the proposed UL "Standard for Flat Plate Photovoltaic Modules and Panels" [2], which has its origins in a JPL Block V specification [3]. Depending on the module circuit configuration it may be necessary to employ multiple module-mounted bypass diodes to insure satisfactory performance during this test exposure. This is particularly true for residential applications where the requirements for dc system voltage and array and module size tend to dictate a relatively large number of series-connected cells per module. Under such circumstances it is clear that the best solution involves the use of both internal and external diodes in an arrangement of the type illustrated in Figure 3-2. In this case, cross-ties have been used to parallel multiple modules as an element of a source circuit. It is clear that without the external bypass diodes this circuit would be subject to internal diode current overloading in the event of open-circuit failures or shadowing. It is also apparent that the elimination of all internal bypass diodes may compromise the ability of the module to survive the JPL hot-spot endurance test. However, with the arrangement shown, the combined use of both internal and external bypass diodes would seem to resolve all the concerns mentioned above since the forward voltage drop of the external diode, relative to the series-connected drop of the multiple internal diodes will assure that the bypassed current will pass through the external diode which can be sized to accommodate the short-circuit current of the entire source circuit.

When the external diode is used to bypass a relatively large number of series-connected solar cells, as in the case illustrated in Figure 3-2, it is important to assure that the reverse blocking voltage of the external diode is sufficiently high. This consideration would eliminate the Schottky

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2. UL 1703, "Standard for Flat-Plate Photovoltaic Modules and Panels" (Draft Document)
3. "Block V Solar Cell Module Design and Test Specification for Residential Applications - 1981", JPL Document 5101-162.

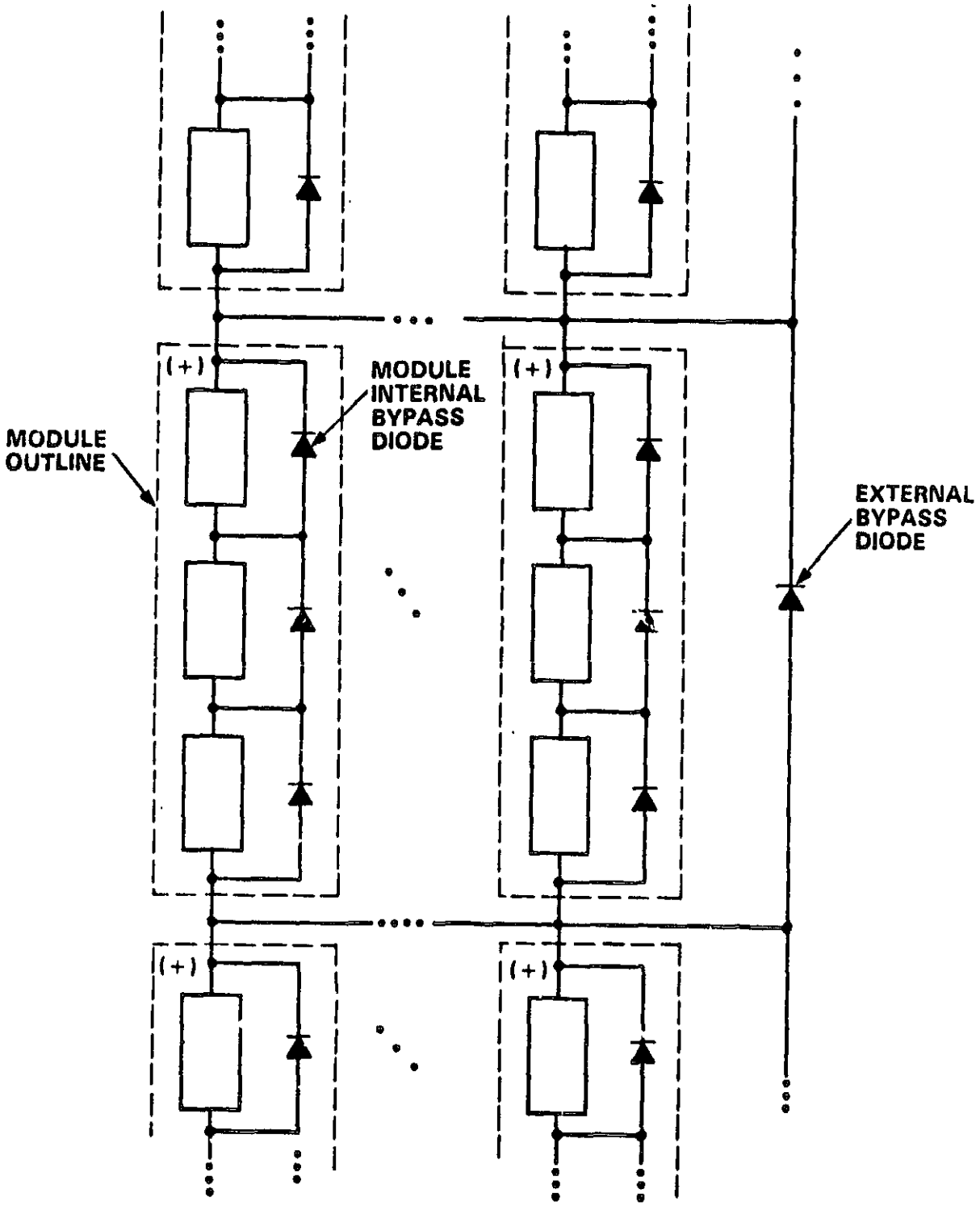


Figure 3-2. Typical Array Source Circuit Diagram with Modules Having Multiple Internal Bypass Diodes

diode for applications where more than 26 series-connected solar cells (at 0.75 volts per cell at -20°C) are bypassed by the external diode. This assumes a 40 volt Schottky reverse blocking voltage which is derated by a factor of two. In these cases, the use of a PN junction device for the external diode is indicated. Thus, in the general case where multiple internally bypassed cell groups are cross-tied and externally bypassed, it will be necessary to use a PN junction device for the external diode as well as PN junction devices for the internal module diodes. This latter conclusion stems from the observation that the forward drop of two series-connected internal Schottky diodes may not be greater than the forward voltage of the single external PN junction diode which is the condition required to assure a current through the external bypass path.

The special case illustrated in Figure 3-3 depicts the cross-strapping of modules which each have a single bypassed cell group. In this case, the number of series-connected solar cells in each group will generally be less than 26 due to hot-spot heating considerations and protection of the internal diodes is assured by using a Schottky device for the external diode and a PN junction device for the internal diodes.

Thus, these arguments lead to the conclusion that integral bypass diodes will generally be required to assure compliance with established JPL hot-spot testing specifications and that, when used, these diodes should be PN junction devices to provide the forward voltage drop necessary to permit external diode protection of cross-tied groups.

3.2 AVAILABLE DIODE CHIP TYPES

Potential suppliers of PN junction and Schottky diodes were contacted to determine their interest in supplying diodes in chip form for use in the photovoltaic module bypass application. The manufacturers listed in Table 3-1 currently produce such devices and indicated an interest in selling diode chips with integral mounting pads (to facilitate handling and assembly). These diode cells are generally of two configurations as depicted in Figure 3-4, depending on the diode type. PN junction devices are supplied in a button or pill configuration as shown in Figure 3-4(a) with the silicon die soldered between metallic disks and protected with a circumferential Silastic seal. A high lead solder composition is generally

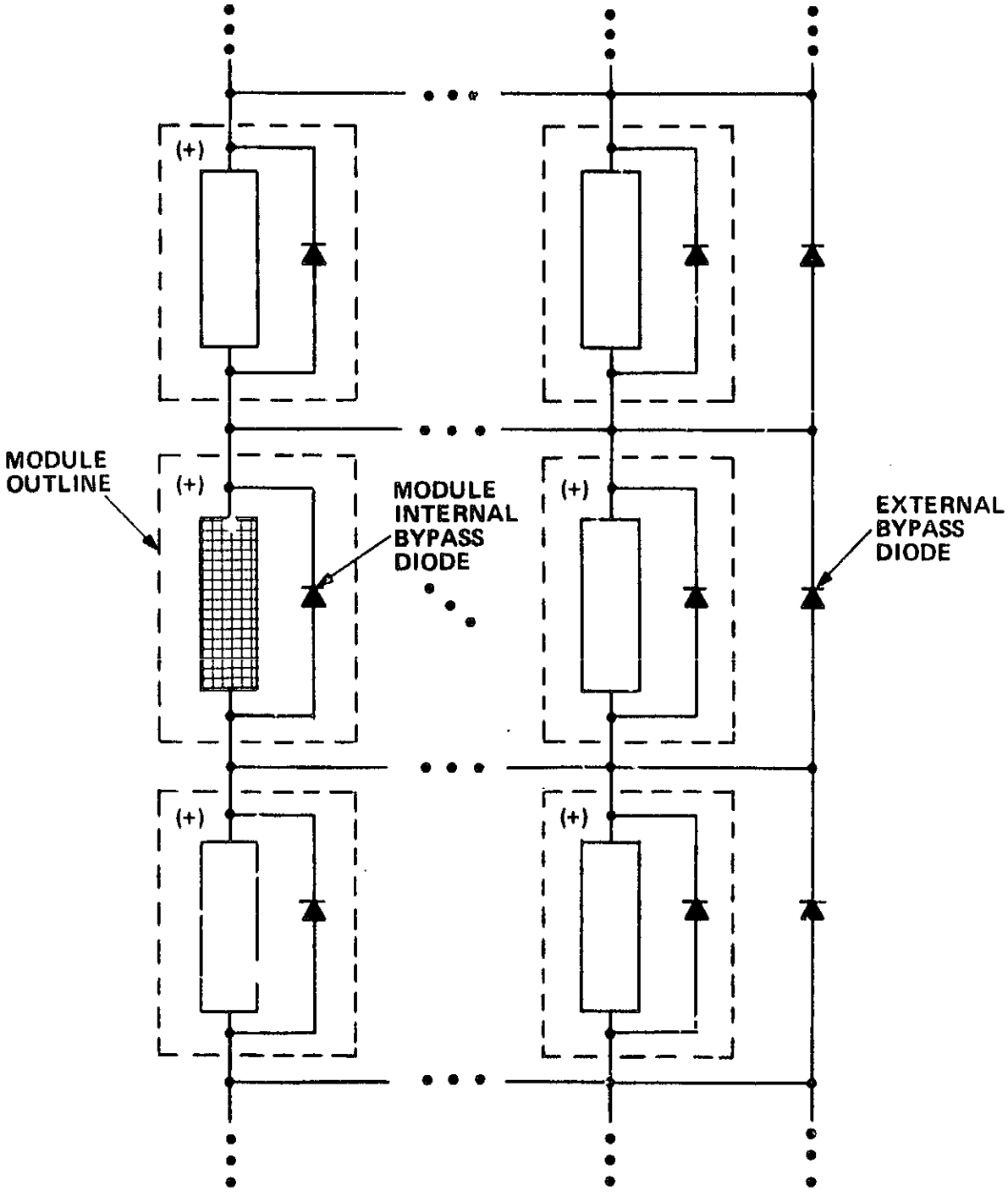
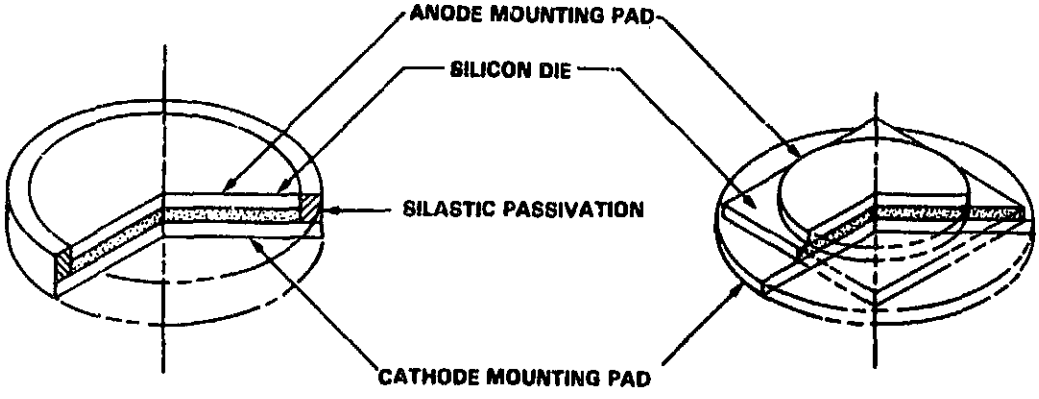


Figure 3-3. Typical Array Source Circuit Diagram With Modules Having a Single Internal Bypass Diode

Table 3-1. Potential Diode Chip Suppliers

MANUFACTURER	DIODE CHIP TYPE	FORWARD CURRENT RATING (AMPERES)
GENERAL INSTRUMENT	PN JUNCTION	8, 25
INTERNATIONAL RECTIFIER	SCHOTTKY	10, 30, 60
M/ACON (FORMERLY MICROWAVE ASSOCIATES)	SCHOTTKY	5, 15, 30, 60
MOTOROLA	SCHOTTKY	15, 30, 60, 75
SEMICON	PN JUNCTION SCHOTTKY	6, 12, 20, 40, 50 15, 30, 75
TRW	SCHOTTKY	30, 60
UNITRODE	SCHOTTKY	8, 30, 60
VARO	SCHOTTKY	15, 30, 60



(a) PN Junction Device

(b) Schottky Device

Figure 3-4. Typical Diode Cell Packaging Configuration

used to join these layers since it provides superior joint-fatigue tolerance. A typical Schottky device package, as shown in Figure 3-4(b), mounts the die on a molybdenum disk to form the cathode terminal. A smaller metal disk, or solder mound is attached to the top of the die to form the anode contact. The edges of the device are unprotected, thus creating the requirement for careful handling and processing to avoid performance degradation during higher level assembly operations.

Tables 3-2 through 3-9 contain a summary of the device offerings from each potential supplier including general physical characteristics and pertinent performance rating parameters. The tabulated values of average forward current rating, which are based on 60 Hz half-wave rectified ac operation, can be conservatively increased by 25 percent for dc operation. Each device is identified with its associated package type (e.g., DO4 or DO5) and a representative value of junction-to-case thermal resistance is listed based on this package design. When soldered directly to a flat-plate heat spreader, the thermal resistance measured between the junction and the heat spreader could be expected to be lower than the tabulated value for the packaged diode configuration.

Mounted PN junction chips are available from Semicon and General Instrument as standard product lines. However, Schottky diode chips are only available if a production run is underway for packaged units using this die. A minimum order of approximately $500 is usually required by most manufacturers to start-up a line for a particular Schottky diode chip not in stock. Based on a survey conducted in June 1982, Motorola provided the shortest response time for the delivery of a variety of mounted Schottky diode chips. This same survey yielded the range of mounted chip prices given in Table 3-10 for an order quantity of 1000 units. These data indicate that mounted Schottky diode chips can be expected to be approximately double the price of comparably rated PN junction devices.

Sample quantities of available diode chips of both types were requested from all potential suppliers. Evaluation samples of the types listed in Table 3-11 were received from four manufacturers. Mounted Schottky diode chips were readily available from Motorola since they are assembled to the mounting pads and tested as an initial operation prior to insertion into

Table 3-2. Characteristics of General Instrument Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
PN Junction	Die Overall Height	.112 dia .158 dia -	- - .086	Nickel plated copper-top and bottom	8 (Button cell PR4-A without attachment to copper heat sink rated at 3 amps)	175	PR 4-A (3 amp)	Button Cell	2.0
PN Junction	Die Overall Height	.160 dia .220 dia -	- - .086	Same as above	25 (Button cell SOZA-A without attachment to copper heat sink rated at 6 amps)	175	502A-A (6 amp)	Button Cell	1.2

Table 3-3. Characteristics of International Rectifier Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
Schottky	Die Top Pad Bottom Pad	.125 sq. .100 dia .180 dia	.010 .010 .010	Nickel plated, molybdenum - top and bottom	10	150*	10TQ030 35 40 45	To 220	5.0
Schottky	Die Top Pad Bottom Pad	.175 sq. .150 dia .280 dia	.010 .010 .010	Same as above	30	150*	21FQ035 (SD41)	D04	2.0
Schottky	Die Top Pad Bottom Pad	.200 sq. .175 dia .250 dia	.010 .010 .010	Same as above	50	150*	S1HQ045 (SD51)	D05	1.0

*175°C Junction Temperature Chips Available (IR Process 830)

Table 3-4. Characteristics of M/ACON* Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
Schottky	Die Top Pad Bottom Pad	.084 sq. Solder Ball .125 dia	.010 .007 .010	Lead/Indium/Silver solder mound-top Lead/Indium/Silver clad molybdenum-bottom	5	150	MA4D520	D01 (Axial)	8.0
Schottky	Die Top Pad Bottom Pad	.112 sq. Solder Ball .169 dia	.010 .007 .010	Same as above	15	150	MA4D1520	D04	4.0
Schottky	Die Top Pad Bottom Pad	.152 sq. .125 dia .220 dia	.010 .007 .010	Lead/Indium/Silver clad molybdenum-top and bottom	30	150	SD 41	D04	2.0
Schottky	Die Top Pad Bottom Pad	.216 sq. .169 dia .310 dia	.010 .007 .010	Same as above	60	150	SD 51	D05	1.0

* Formerly Microwave Associates

Table 3-5. Characteristics of Motorola Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
Schottky	Die Top Pad Bottom Pad	.126 sq. .100 dia .182 dia	.007 .015 .010	Nickel plated, molybednum - top and bottom	15	125	MBR 1520 1530 1540	D04	2.5
Schottky	Die Top Pad Bottom Pad	.160 sq. .136 dia .230 dia	.007 .015 .010	Same as above	30*	125	MBR 3520 35 45 SD 41	D04	2.0
					60**	150	MBR 6020 35 45 SD 37	D05	1.0
Schottky	Die Top Pad Bottom Pad	.200 sq. .176 dia .286 dia	.007 .015 .010	Same as above	75	150	MBR 7520 30 35 40 45	D05	1.0

* Chrome Metal Barrier Material
** Platinum Metal Barrier Material

Table 3-6. Characteristics of Semicon Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
PN Junction	Die Top Pad Bottom Pad	.100 dia .100 dia .120 dia	.012 .021 .021	Silver clad aluminum top and bottom Silastic around periphery of die and pads	6	175	1N1612A 1N2228 1N2147A 1N2229A	004 004 0010 0010	2.5
PN Junction	Die Top Pad Bottom Pad	120 dia .120 dia .140 dia	.012 .021 .021	Same as above	12	175	1N2576 1N2587 1N2246A	0010 0010 004	2.5
PN Junction	Die Top Pad Bottom Pad	.140 dia .140 dia .160 dia	.012 .021 .021	Same as above	20	175	1N3491	0021	1.0
PN Junction	Die Top Pad Bottom Pad	.209 dia .200 dia .220 dia	.012 .021 .021	Same as above	40	175	1N2154 S25A05 1N3659 1N1183A 1N2446 S40A05 1N1434	005 005 0021 005 005 005 005	1.0
PN Junction	Die Top Pad Bottom Pad	.220 dia .240 dia .240 dia	.012 .021 .021	Same as above	50	175	1N2458	00E	1.0
Schottky	Die Top Pad Bottom Pad	.130 sq. .110 dia .220 dia	.007 .017 .017	Silver plated, nickel clad molybdenum top and bottom	15*	150	SSH5A20 30 40 50 60 (5 amp rating in axial package)	Axial	2.5
Schottky	Die Top Pad Bottom Pad	.165 Hex .125 dia .220 dia	.007 .017 .017	Same as above	30*	150	SSH30A20 30 40 50 60	004	1.5
Schottky	Die Top Pad Bottom Pad	.210 sq. .160 dia .315 dia	.007 .017 .017	Same as above	75*	150	SSH75A20 30 40 50 60	005	0.65

* Tungsten Metal Barrier Material

Table 3-7. Characteristics of TRW Power Semiconductors

Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
Schottky	Die Top Pad Bottom Pad	.165 sq .110 dia .240 dia	.010 .014 .014	Lead/Indium/Silver clad molybdenum - top and bottom	30	150	SD41	D04	2
*Schottky	Die Top Pad Bottom Pad	.211 sq .110 dia .310 dia	.010 .014 .014	Gold/Germanium clad molybdenum on top. Lead/Indium Silver clad molybdenum on bottom	60	150	SD51	D05	1

* Being redesigned - new unit available approximately Jan., 1983

Table 3-8. Characteristics of Unitrode Diode Chips

DIODE CHIP TYPE	DIMENSIONS	SIZE (inches)	THICKNESS (inches)	TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (°C)	USED IN PACKAGE TYPE (TYP. EXAMPLE) IDENTIF. NO.	STYLE	THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (°C/WATT)
Schottky	Die Top Pad Bottom Pad	.113 sq. .067 dia .140 dia	.010 .014 .014	Lead/Indium/Silver clad molybdenum - top and bottom	8	150	USD 720 735 745	TO220	2.8
Schottky	Die Top Pad Bottom Pad	.157 sq .120 dia .180 dia	.010 .014 .014	Same as above	30	150	SD 41	D04	2.0
Schottky	Die Top Pad Bottom Pad	.183 sq .140 dia .320 dia	.010 .014 .014	Same as above	60	150	SD 51	D05	1.0

Table 3-9. Characteristics of Varo Diode Chips

DIODE CHIP TYPE	DIMENSIONS			TYPE OF METALLIZED PADS	AVERAGE FORWARD CURRENT RATING (BASED ON 60 HZ-AC) ON HEAT SINK (AMPS)	MAXIMUM ALLOWABLE JUNCTION TEMPERATURE (^{o}C)	USED IN PACKAGE TYPE (TYP. EXAMPLE)		THERMAL RESISTANCE IN PACKAGE (JUNCTION TO HEAT SINK) (^{o}C/WATT)
		SIZE (inches)	THICKNESS (inches)				IDENTIF. NO.	STYLE	
Schottky	Die Top Pad Bottom Pad	.130 sq. .105 dia. .200 dia.	.015 .015 .015	Lead/Tin/Silver clad copper - top Lead/Tin/Silver clad molybdenum - bottom	15	150	VSK1520 1530 1540	D04	2.5
Schottky	Die Top Pad Bottom Pad	.160 sq. .140 dia. .285 dia.	.015 .015 .015	Lead/Tin/Silver clad molybdenum - top and bottom	30	150	VSK3020 3030 3040	D04	2.0
Schottky	Die Top Pad Bottom Pad	.200 sq. .175 dia. .285 dia.	.015 .015 .015	Same as above	60	150	VSK6020	D05	1.0

Table 3-10. Mounted Diode Chip Unit Prices (1982 $/Device)
Based on a Quantity of 1000 Units

Diode Type	Forward Current Rating (Amperes)					
	12	15	20	30	40-60	60-75
PN Junction (V_R = 50V)	0.30-0.50	—	0.60-0.80	—	1.20-1.80	—
Schottky (V_R = 20V)	—	1.00-2.00	—	1.50-2.50	—	2.25-3.50

Table 3-11. Mounted Diode Chips Received
as Samples for Evaluation

Manufacturer	Diode Chip Type	Average Forward Current Rating (Amperes)
General Instrument	PN Junction	8, 25
M/A-CON	Schottky	30
Motorola	Schottky	15, 30, 60, 75
Semicon	PN Junction	6, 12, 20, 40, 50
	Schottky	15, 30, 75

standard package types. Semicon produces a complete line of mounted type PN and Schottky diodes and supplies a market in these special units. General Instruments also produces some mounted PN diodes that are readily available from stock. The Schottky units received from M/A-CON happened to be available from previous orders for packaged units. At the time of the request M/A-CON process lines for these units were not in operation.

Other potential suppliers of mounted chips (i.e., TRW, International Rectifier, Unitrode and Varo) could not provide sample units for one or another of the following reasons: (1) units were not available from stock, (2) no production orders for packaged diodes using the same die were in process at the time of the request, (3) dies were available but the assembly

of the metal pads, which is normally done as part of the packaged diode process run, would require a special set-up costing at least $500.

3.3 DIODE PERFORMANCE CHARACTERISTICS

3.3.1 CURRENT-VOLTAGE CHARACTERISTICS

Reverse and forward characteristics of the sample diodes were evaluated using a Tektronix Curve Tracer, Model 576, and a Pulsed High Current Fixture, Model 176 (100 ampere capacity). All the units met or exceeded their reverse blocking voltage ratings. Schottky chips exhibited blocking voltages from 15 to 50 volts. The PN junction chips, randomly selected from existing stock by the manufacturers, exhibited reverse blocking voltages as high as 1000 volts. The PN junction manufacturing process is usually targeted to yield maximum reverse voltages, with a selection operation used to segregate the units into various voltage levels down to 50 volts. The lower rated reverse voltage units are usually the lowest priced.

Forward current versus forward voltage drop traces were obtained for each unit and recorded using a Polaroid camera attachment to the Tektronix Curve Tracer. All the traces were replotted on a single graph, as presented in Figure 3-5, to permit a comparison of the various manufacturer's offerings. It should be pointed out that the data presented is based on one chip of each type. However, in a few cases, more than one chip of a particular type was tested as a verification that chips from the same manufacturer's lot exhibit closely matched forward characteristics.

Schottky unit forward voltage drops are somewhat less than half that of a PN junction diode in the 2 to 20 ampere range of interest for this program. The data presented in Figure 3-5 was obtained at room temperature with junction temperature rising only slightly during the short duration test current pulse. At the higher operating junction temperatures, the forward voltage drop decreases for both the PN and Schottky diodes.

A comparison of the Semicon and General Instrument PN junction units indicates a close match of forward voltage drops for the range of currents shown. For the Schottky devices, Motorola units exhibit somewhat lower forward voltage drops than the Semicon dies. The 30 ampere M/A-COM Schottky

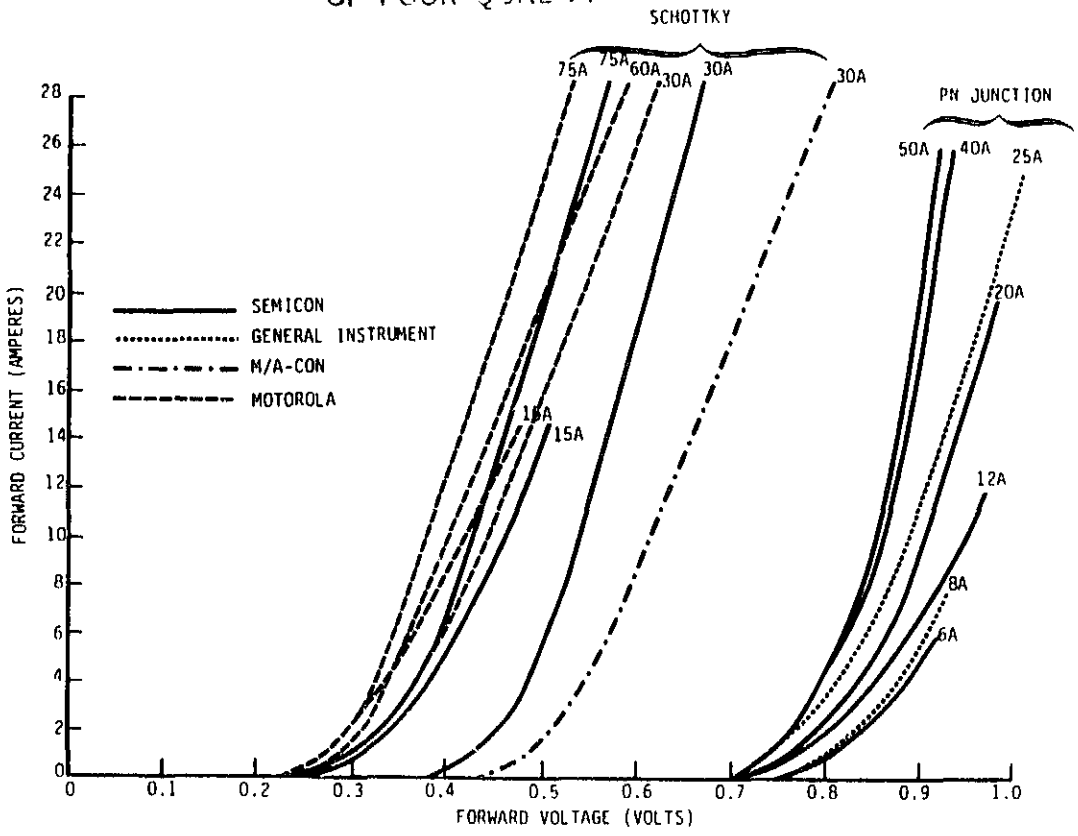


Figure 3-5. Forward Current - Voltage Characteristics of Mounted Diode Chips

device yielded the highest voltage drop of any of the Schottky diodes evaluated.

3.3.2 THERMAL RESISTANCE

Representative diodes of both types from two manufacturers were soldered to simulated cathode heat spreader plates to serve as test specimens for the measurement of junction-to-heat spreader thermal resistance as described in Appendix A. As shown in Figure 3-6 these test articles consisted of the pad-mounted chips of the various types soldered to 0.5x1.5x0.032 inch thick nickel-plated copper cathode heat spreader plates with short anode lead straps to accommodate the test equipment. The test results, as summarized in Table 3-12 reveal that the junction-to-heat sink thermal resistance is generally below 1.0^{o}C/watt for all devices with the higher values being associated with the smaller unit sizes. The PN junction diodes exhibited a somewhat more consistent decrease in thermal resistance with increased chip size than the Schottky devices. This can probably be attributed to the

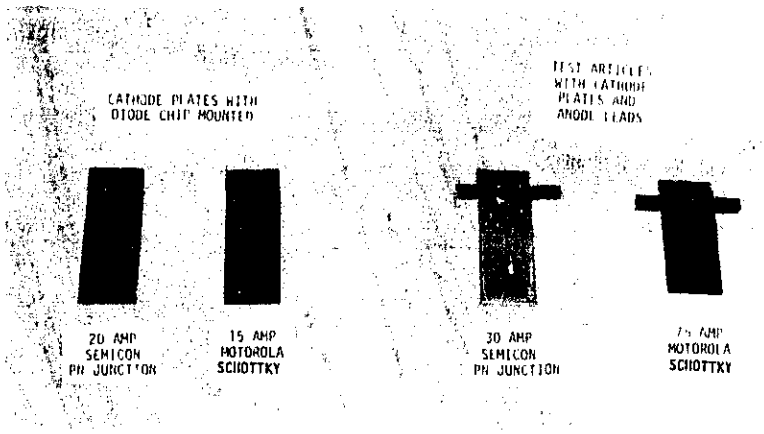


Figure 3-6. Typical Thermal Resistance Test Articles

Table 3-12. Comparison of Diode Chip Thermal Resistance Values

MANUFACTURER	DIODE TYPE AND RATING	THERMAL RESISTANCE JUNCTION-TO-SINK (°C/WATT)	
		STANDARD PACKAGED UNIT (TYP. PACK. TYPE)	PAD MOUNTED CHIP SOLDERED TO CATHODE PLATE *
SEMICON	PN - 12A	2.5 (DO4)	0.97
SEMICON	PN - 20A	1.0 (DO21)	0.95
SEMICON	PN - 40A	1.0 (DO5)	0.61
SEMICON	PN - 50A	1.0 (DO5)	0.50
MOTOROLA	SCHOTTKY - 15A	2.5 (DO4)	0.78
MOTOROLA	SCHOTTKY - 30A	2.0 (DO4)	0.79
MOTOROLA	SCHOTTKY - 60A	1.0 (DO5)	0.79
MOTOROLA	SCHOTTKY - 75A	1.0 (DO5)	0.45
SEMICON	SCHOTTKY - 15A	2.5 (AXIAL)	0.84
SEMICON	SCHOTTKY - 30A	1.5 (DO4)	0.72
SEMICON	SCHOTTKY - 75A	0.65 (DO5)	-

* Includes the thermal resistance of a grease interface between the cathode plate and the heat sink. The calculated thermal resistance of this interface is 0.3°C/watt based on nominal values for contact area and grease film thickness.

better solder connections to the cathode plate for these devices as compared to the Schottky diodes which proved more difficult to solder. As indicated in the table the measured thermal resistance values were considerably lower than the published values for the standard packaged unit, containing the same chip type and rating.

3.3.3 SOLDERABILITY

The solderability of the mounted diode cell to the cathode heat spreader plate and to the anode lead strap was evaluated by the assembly of numerous samples of the type used for the thermal resistance measurements. The fabrication of these test articles proved to be a valuable vehicle for the development of soldering techniques applicable to joining the diode cell terminals to the cathode heat spreader plate and to the anode lead strap.

An inert atmosphere soldering process was selected to prevent any possible oxidation that could effect the thermal integrity of the cathode solder joint by producing voids in this critical interface. The equipment pictured in Figures 3-7 and 3-8 was used to solder all thermal resistance and pull test articles. The specimen to be soldered was placed on a temperature-controller carbon heater plate and held by a spring loaded clamp containing a thermocouple probe. A glass bell jar enclosure was used to contain a forming gas (15 percent hydrogen and 85 percent nitrogen) atmosphere around the components during the automatic soldering operation. Solder foil preforms with a nominal thickness of 0.003 inches were inserted between the diode chips and the cathode and anode mating components. A Sn62 solder composition (62 percent tin, 36 percent lead and 2 percent silver) was used with silver plated mating surfaces since tin tends to scavange silver from the plated surfaces. Low percentage silver bearing solders overcome this problem since the solubility of silver in tin is approximately 3 percent at the required processing temperature. Sn62 preforms were used with both the Semicon PN junction devices (which have silver-clad aluminum pads) and the Semicon Schottky devices (which have silver-flashed nickel clad molybdenum pads) whether or not the cathode and anode mating components were silver plated. A Sn60 solder composition (60 percent tin and 40 percent lead) was used for all joints not involving silver plated surfaces at either interface.

Figure 3-7. Inert Atmosphere Soldering Unit

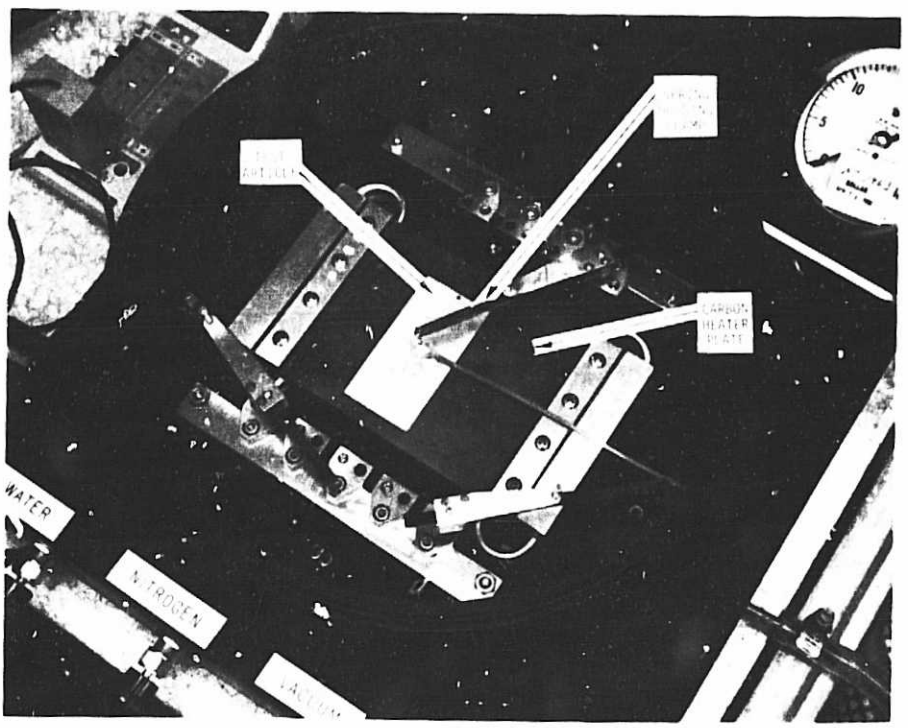


Figure 3-8. Diode/Heat Sink Unit Mounted on Heater Plate of Inert Atmosphere Soldering Unit

Soldering temperatures should be 40°C to 70°C higher than the melting point of compositions used (183°C for Sn60 and 179°C for Sn62) to insure proper melting of the solder. The highest temperatures were found necessary with the Schottky diodes that have molybdenum pads. Consequently tin plated mating components can experience tin reflow at temperatures above 232°C, and expose copper surfaces. Therefore, where tin plating is desired because of its excellent solderability and low cost, care must be exercised during processing to insure soldering temperatures below 230°C. For the Schottky devices used as test articles, nickel proved most applicable because of the temperature limits associated with the tin-plate and the higher costs of silver plating. For nickel-plated components, it was found advantageous to lightly burnish the immediate areas to be soldered (including the diode pads, if nickel-plated) using an ordinary pencil eraser to remove any possible oxide films.

When the diode chip pads already had a solder cladding applied to the exposed surface of the pad (e.g., the M/A-COM Schottky molybdenum pads clad with a 92% lead, 5% indium, 2% silver solder) no additional preforms were used. The clad solder should be reflowed at a temperature somewhat above the melting temperature of the applied solder. A M/A-COM Schottky diode was successfully bonded to nickel-plated cathode/anode mating components at a reflow temperature of approximately 330°C. The potential problem with reflow is that the chip is already bonded to the molybdenum pad with the same solder cladding which also reflows and care must be taken to avoid a shift of the chips and molybdenum pad.

In the initial experiments no flux was used in the soldering process since most fluxes start to polymerize at approximately 250°C, harden and become difficult to remove. If flux is left in the vicinity of a semiconductor, migration of chemicals in the flux can take place and detrimentally react with the device. Manufacturers of the pad mounted type diode chips do not use fluxes since high lead solders that melt above 300°C are used to join the pads to the chip. Moreover, the automatic die bonding machines in the semiconductor industry have vacuum tool holding devices that permit controlled movement of the parts being soldered which provides scrubbing action and consequently good solder wetting without the need for a flux. However, the use of a small amount of non-activated flux (e.g. Alpha 100 or

Kester 115) has been found to enhance the solderability particularly with nickel-plated components. Since soldering temperatures are below 250°C no polymerization of the flux should occur and any flux residue can be readily removed with reagent alcohol in an ultrasonic bath.

3.3.4 JOINT INTEGRITY TESTING

A number of soldered test articles were subjected to an anode pull and cathode/chip shear test to determine joint structural integrity. The Instrom tensile tester pictured in Figure 3-9 was used for the anode lead pull tests while the Anza Tech machine shown in Figure 3-10 was used to apply the horizontal force for the diode shear tests.

Results of these tests are presented in Table 3-13. Two units, a Semicon 30 amp Schottky and a Semicon 20 amp PN junction device, failed at less than 1 lb. force while all other specimens exhibited lead strengths comparable to that achieved with similarly sized solar cell interconnector strips. Examination of fractured surfaces of these two units indicated some small voids which are characteristic of incomplete solder wetting of the surfaces. As anticipated, the larger the anode lead solder contact area, the greater the pull force to effect a failure. Two similar sets of Semicon PN junction diodes (20 amp and 50 amp devices), one set with tin-plated and the other with nickel-plated mating components, indicated somewhat superior anode holding strength for the tin-plated units. This probably can be attributed to the fact that flux was not used with these first nickel-plated units thereby reducing the integrity of the solder bond.

All subsequent nickel plated test articles were soldered using non-activated flux. Tinned flat braid and tinned round copper wire anode lead test articles yielded pull test results comparable to the rectangular copper foils. The 0.040" diameter round wire (AWG18) exhibited excellent pull strength (2.5 lb_f.) for its size due to the build-up of a solder fillet around a major portion of its periphery.

The chip push (or shear) tests resulted in no bond fractures when the maximum machine capacity of 11 lb_f was applied.

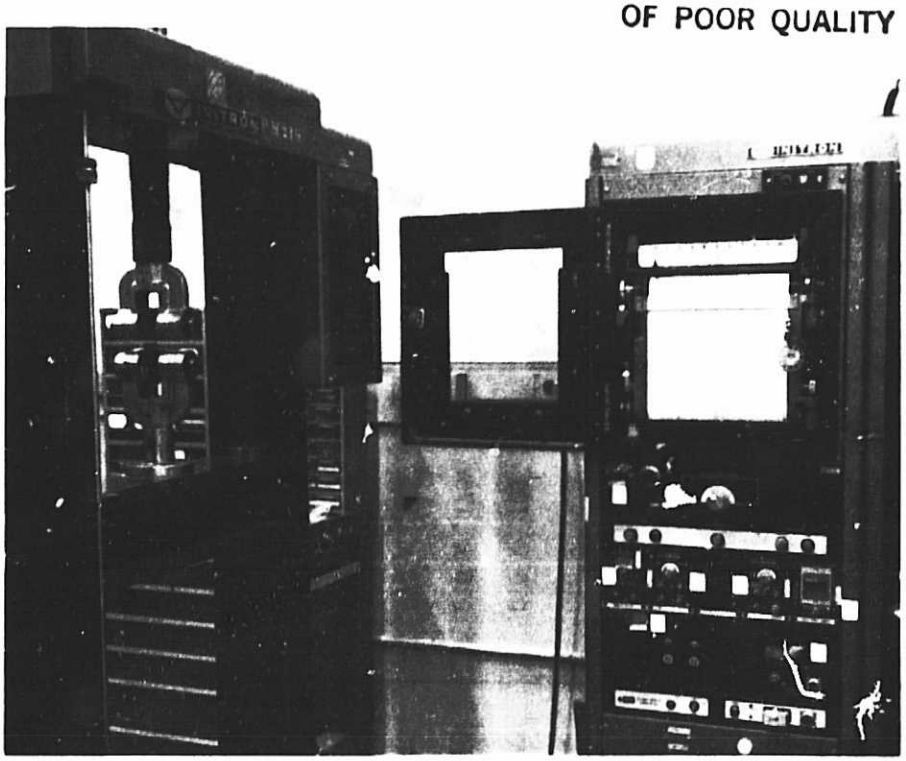


Figure 3-9. Anode Lead Pull Test

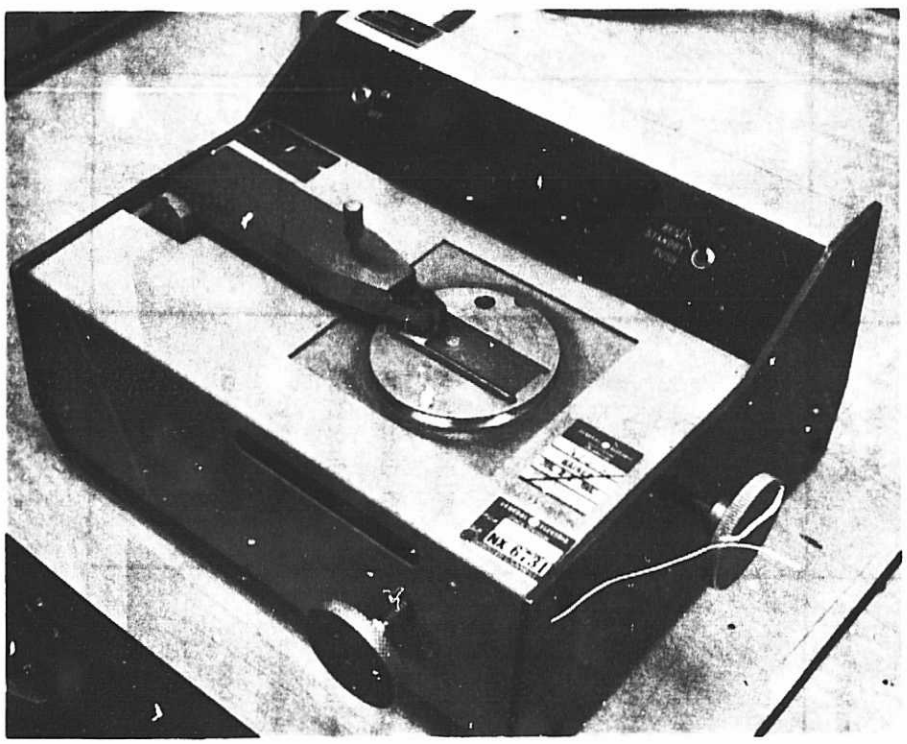


Figure 3-10. Diode Chip/Cathode Plate Shear Test

Table 3-13. Anode Pull Test Results

Manufacturer	Type Of Diode	Avg. Forward Current Rating (Amps)	Copper Anode/ Cathode Plating	Anode Dia. of Mounted Chip (Inches)	Anode Lead Size (Inches)	Vertical Pull Force To Failure Of Anode Lead Solder Joint (lb_f)
Semicon	Schottky	30	Silver	.220	.010 Thk x .170 Width	0.74*
Semicon	Schottky	15	Silver	.140	.010 x .125	2.55
Motorola	Schottky	60	Nickel Cathode	.136	.020 x .187 Tinned Cu Braid	2.20
Motorola	Schottky	75	Nickel	.176	.010 x .170	3.15
Semicon	PN Junction	20	Tin	.140	.010 x .125	1.75
Semicon	PN Junction	50	Tin	.240	.010 x .170	2.55
Semicon	PN Junction	20	Nickel	.140	.010 x .125	0.65*
Semicon	PN Junction	50	Nickel	.240	.010 x .170	1.90
M/A-Con**	Schottky	30	Nickel	.125	.010 x .125	1.70
Semicon	PN Junction	12	Nickel Cathode	.120	.020 x .093 Tinned Cu Braid	1.20
Semicon	PN Junction	12	Silver Cathode	.120	AWG #18 (.040" dia) Tinned Cu Wire	2.50

* Examination Indicated Poor Solder Wetting of Bonded Surfaces

** Reflowed Lead/Indium/Silver Solder Clad to Diode Metallized Pads to Attach to Cathode and Anode Components (330°C Soldering Temp.)

3.4 DIODE PACKAGING CONSIDERATIONS

3.4.1 GENERAL REQUIREMENTS

The dissipation of the heat generated within the small diode chip when conducting the bypass current represents the most difficult design problem involved with the integration of these chips within the module encapsulant. It is also essential that the thickness of the package to be laminated along with the solar cell circuit be kept as small as possible to assure conformance of the rear cover sheet with the minimum use of encapsulant material. These requirements combine to dictate that the diode chip be mounted to a thin heat spreader plate which is fabricated from a material of high thermal conductivity.

In this way it is possible to maintain an acceptably low junction temperature by transferring the heat from this small source through the fin created by the plate and on out into the adjacent solar cell circuit elements where it can be ultimately rejected to the surroundings by radiation and convection. The size of the heat spreader plate required to produce the specified temperature level within the laminate will depend on the diode heat generation as well as on the insolation level, ambient temperature, wind speed and details of the module mounting arrangement. The most logical mounting location for this plate is directly behind the solar cell circuit where the required fin area can be encapsulated without increasing the exposed module area. This mounting arrangement will generally require that the heat spreader plate be electrically insulated from the rear sides of the solar cell circuit, since the plate size and/or mounting location may require the plate to stradle cells of different potentials within the circuit. Similarly it will be necessary to insulate the anode lead from the rear side of the solar cell circuit. The location of the diode/heat spreader plate should consider the ease of making both the anode and cathode connections to the circuit terminations. If positioned properly the heat spreader plate, which is the diode cathode, can also function as the circuit positive termination.

3.4.2 ENCAPSULANT MATERIALS

Existing module design data was reviewed to define typical encapsulant materials, along with the associated construction and processing procedures from the standpoint of identifying the impact on the diode/heat spreader

design. The most commonly used pottants today are silicone rubber (RTV 615 and Sylgard 184), polyvinyl butyral (PVB) and ethylene vinyl acetate (EVA). PVB and EVA are applied as films, while silicone rubber is a casting type material. Silicone rubber syrup is poured into a PV module at room temperature, cured for 6 hours, and then heated to approximately 90°C for an additional hour. Operating temperatures considerably in excess of 150°C are possible with cured silicone rubber without degrading the pottant. EVA film is cured at 150°C for approximately 15 to 20 minutes, but has a lower maximum operating temperature of 130°C, established by the results of a continuous 400 hour test recently completed by Springborn Laboratory [4]. PVB is handled in a similar manner to EVA and is thermoset at approximately the same temperature.

EVA has received the widest acceptance of the pottants described above, and therefore is recommended for use in this program. Since EVA has the lowest maximum operating temperature of the commonly used pottants, successful application of an encapsulated diode/heat spreader with EVA should readily permit its application with the other candidate pottants. Thus, for satisfactory performance in an EVA encapsulated module the diode/heat spreader assembly should not present contact temperatures to the EVA in excess of 130°C. Material selected for insulating the diode/heat spreader must be capable of adherence to the EVA, and in addition, be capable of withstanding the 150°C, 20 minute cure cycle.

3.4.3 DIODE/HEAT SPREADER CONFIGURATION

3.4.3.1 General Description

The diode/heat spreader configuration shown in Figure 3-11 consists of a diode cell soldered to the center of an appropriately-sized cathode heat spreader plate. A narrow copper foil anode lead is soldered to the top of the diode cell and exits to the side with a length as required to reach the point of attachment to the solar cell circuit termination. An insulation tape is attached to the underside of both this foil strip and the heat spreader plate to electrically isolate these elements from the rear side of

4. Telephone conversation with Paul B. Willis, July 28, 1982

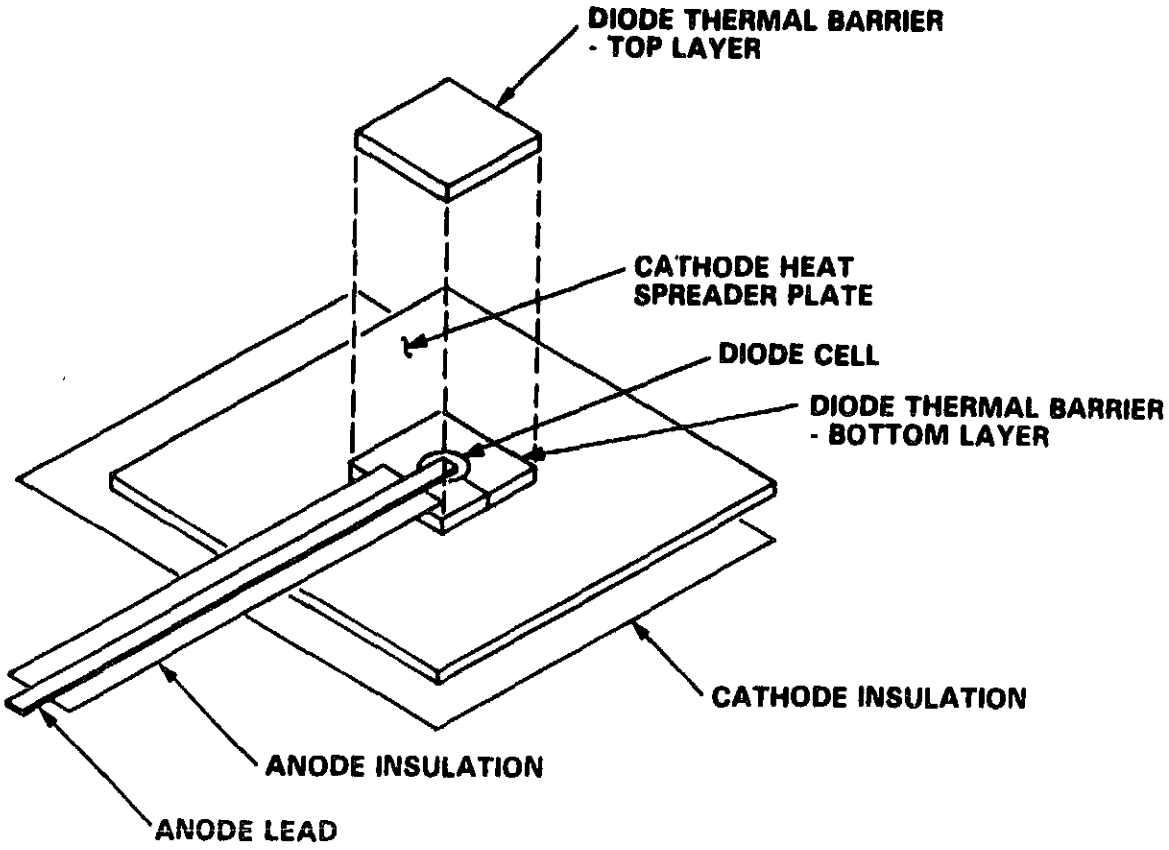


Figure 3-11. Diode/Heat Spreader Configuration

the solar cell circuit. The assembly is completed by the installation of a silicone foam tape thermal barrier layers around the diode cell to prevent the EVA encapsulant from contacting the diode body which will be somewhat hotter than the adjacent heat spreader plate. This foam tape barrier, which is configured in two layers to completely surround the diode cell, also functions to ease the conformance of the rear cover sheet during module lamination in that no abrupt changes in thickness are encountered as the rear cover sheet is forced down by the laminator diaphragm.

3.4.3.2 Cathode Heat Spreader Plate

The size and thickness of the square cathode heat spreader plate is dependent on the diode heat dissipation requirement as discussed in Section 3.5. Candidate materials for this heat spreader include copper and aluminum with pertinent properties as summarized in Table 3-14. When its superior thermal conductivity is coupled with its better solderability, copper is the preferred material for this application. However, the relatively high cost

Table 3-14. Properties of Candidate Heat Spreader Plate Materials

Property	Copper (C10200)	Aluminum (1100-0)
Density (kg/m^3)	8940	2710
Thermal Conductivity at 20°C (W/m K)	391	222
Electrical Resistivity at 20°C (μohm-cm)	1.72	2.9
Modulus of Elasticity (GPa)	117.2	68.9
Tensile Strength (MPa)	248 (Half-hard temper)	90
Average Coefficient of Thermal Expansion ($^oC^{-1}$)	$18x10^{-6}$ (20 to 300°C)	$24x10^{-6}$

of copper clouds this issue and makes the choice between copper and aluminum more difficult. The plating required for each material is an important consideration in this selection process. A tin or nickel plating is required to protect the copper from corrosion and a silver or tin plating is necessary to improve the solderability of the aluminum. The ultimate selection between these two material options is thus a strong function of the plate size and thickness as well as the surface preparation required for corrosion protection or solderability. Copper was used in all experimental work under this contract, but the detailed cost analysis described in

Section 3.7 evaluated the cost impact of both potential heat spreader materials.

3.4.3.3 Anode Lead

Copper foil strips are the obvious choice for the anode conductors, but the selection of conductor cross-sectional area for a given bypass current requirement is not as straightforward. Power dissipation per unit of conductor surface area is perhaps the best choice for a sizing criterion since it can be directly related to the conductor temperature in the encapsulant laminate. As the cross-sectional area is reduced the power dissipation per unit of exposed conductor surface area increases causing the conductor temperature to increase for a constant current. This increase in anode lead resistance also causes an increased forward voltage drop which increases the circuit power loss when the diode is required to function as a bypass path. Available solar cell "hot-spot" heating data [5], which relates the localized temperature rise above ambient to the total power density (insolation plus electrical heating) into the hot-spot region, can be used to estimate the rise in temperature for the embedded flat anode lead. Thus, for an assumed $50^{o}C$ rise above ambient, the solar cell hot-spot temperature data yields an areal power density of 70 mW/cm^2 as the internal electrical heating load. Assuming a $40^{o}C$ worst case ambient temperature with a 0.125 inch (3.2 mm) anode strip width and a 35:1 strip width-to-thickness ratio, the resulting permissible conductor current density is 12,000 amperes per in^2. This value can be used to bound the lower limit of cross-sectional area required to carry a specified bypass current. Lower current densities will reduce the lead power dissipation and voltage drop at the expense of increased copper cost.

3.4.3.4 Insulating Tapes

Candidate materials for the insulation of the side of the cathode heat spreader plate and anode lead strip facing the solar cell circuit include commecially-available electrical insulating pressure-sensitive adhesive tapes

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5. "Flat-Plate Photovoltaic Module and Array Circuit Design Optimization - Workshop Proceedings", JPL, March 31 and April 1, 1980.

of two types. Film carriers of polyester (130°C continuous rating) and Kapton (180°C continuous rating) are available in a 3.5 mil thick (2 mil film plus 1.5 mil adhesive) tape of various widths. In either case, the 2 mil thick carrier film should provide considerably more dielectric strength than required as well as providing adequate mechanical protection against penetration by burrs on the solar cells or copper connector strips. A polyester tape (CHR No. M99) was selected based on its acceptable temperature rating and lower cost compared to the Kapton film.

A flexible, silicone rubber sponge tape material with pressure-sensitive adhesive on one side (CHR Strip-N-Stick) was selected as the thermal barrier material around the diode cell. This sponge tape is available in 0.5 to 2. inch widths and thicknesses ranging from 0.06 to 0.19 inches which can be quickly cut-to-length and taped over the diode. The material readily conforms under the lamination pressure and provides a smooth transition between the diode and the rear cover sheet. Two stacked layers of 1.0 inch square by 0.06 inch thick tape were used as the thermal barrier around each diode.

3.4.4 LAMINATION STACK-UP

A typical lamination stack-up, including the diode/heat spreader assembly, is shown in Figure 3-12. The bypass diode, with its associated heat dissipation and insulation components, is mounted beneath the solar cell circuit. An intermediate layer of EVA film is used to bond the insulated surface of the heat spreader plate to the rear side of the solar cell circuit. The cathode connection is made by soldering the heat spreader plate to the solar cell circuit positive termination as shown on the right hand side of the figure. The insulated anode lead, which is soldered to the opposite end of the diode cell, exits off to the left hand side of the figure where it will be soldered to the appropriate circuit tap point to complete the bypass path. Another EVA film sheet overlays the diode/heat spreader assembly and the completes the encapsulation system by bonding to the rear cover sheet, which is typically a multiple layer laminate of Tedlar, polyester, aluminum foil and Tedlar. The inner layer of Tedlar is pre-coated with Dupont adhesive No. 68040 to improve the adhesion to the EVA.

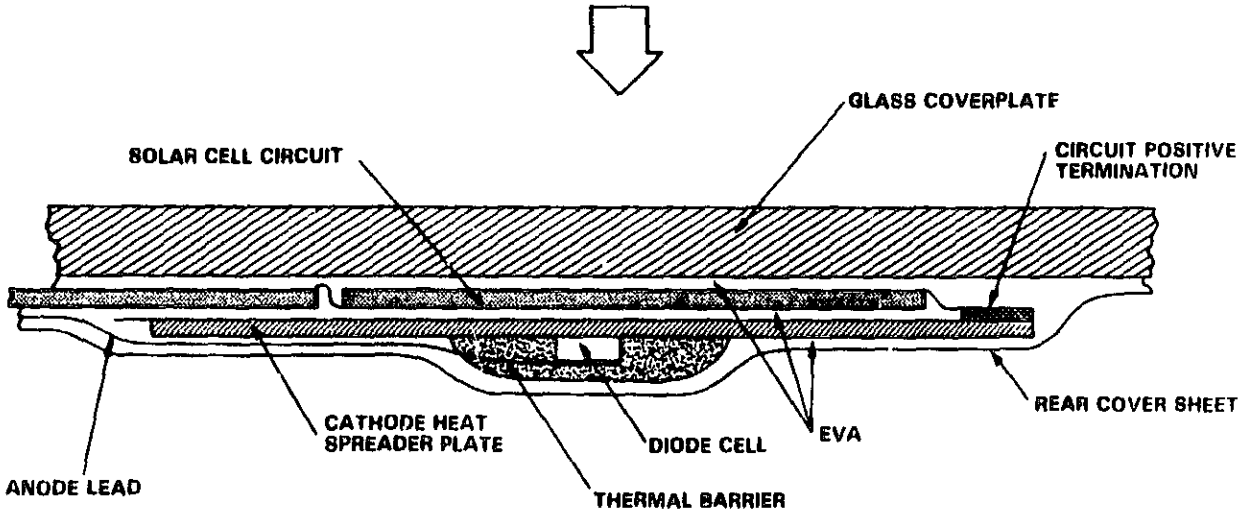


Figure 3-12. Typical Glass Superstrate Lamination Stack-up with Encapsulated Bypass Diode

3.4.5 ENCAPSULATION TEST SPECIMENS

Five encapsulation test specimens, with the characteristics described in Table 3-15, were fabricated as a processing verification of the diode/heat spreader assembly and lamination stack-up design concept described above. In each case the specimen consisted of four square solar cells, 100 mm on a side, arranged on a small glass superstrate as shown in Figure 3-13. The size of the heat spreader plate was selected based the preliminary analysis contained in Reference [1] along with the recently established values of diode-to-heat spreader thermal resistance.

The construction of these specimens is illustrated in Figure 3-14 where the layers of the lamination stack-up are folded-back to reveal the arrangement of components. The only problem experienced during the lamination of these five specimens was the shorting of the diode anode lead to the solar cell

Table 3-15. Design Characteristics of the Encapsulation Test Specimens

IDENTIFICATION LETTER	PAD MOUNTED CHIP TYPE	COPPER CATHODE HEAT SPREADER PLATE DIMENSIONS WxLxT (INCHES)	COPPER ANODE LEAD DIMENSIONS WxLxT (INCHES)
A	SEMICON 12 AMP PN JUNCTION	1.5x3x.032	.100x6x.005
B	SEMICON 20 AMP PN JUNCTION	2x4x.032	.125x6x.005
C	SEMICON 40 AMP PN JUNCTION	4x4x.032	.125x6x.010
D	SEMICON 50 AMP PN JUNCTION	4x4x.032	.125x6x.010
E	MOTOROLA 60 AMP SCHOTTKY	2x4x.032	.125x6x.010

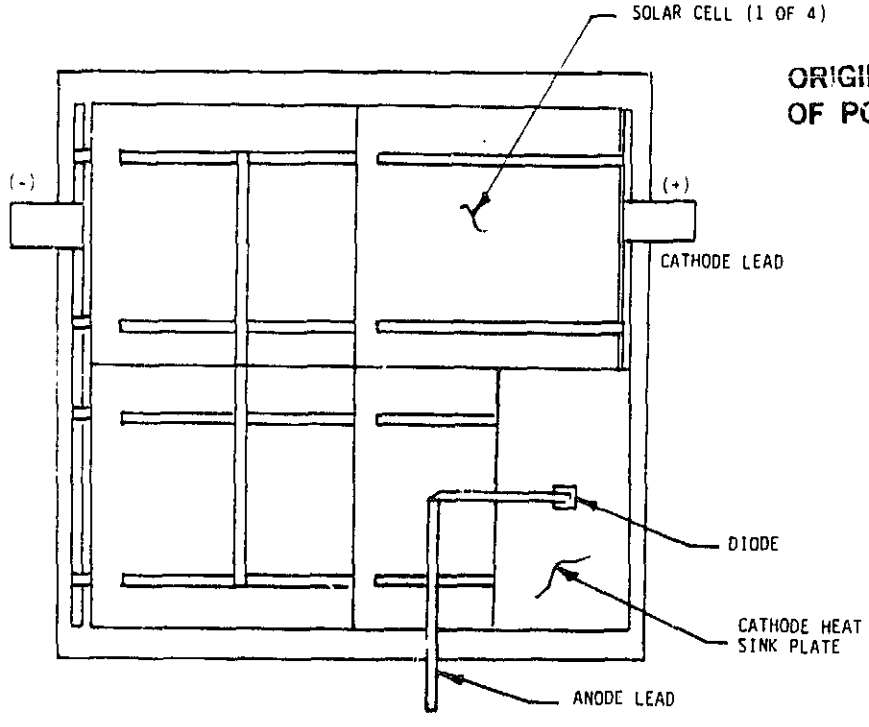


Figure 3-13. Typical Encapsulation Test Specimen (Rear View with Rear Cover Sheet Removed)

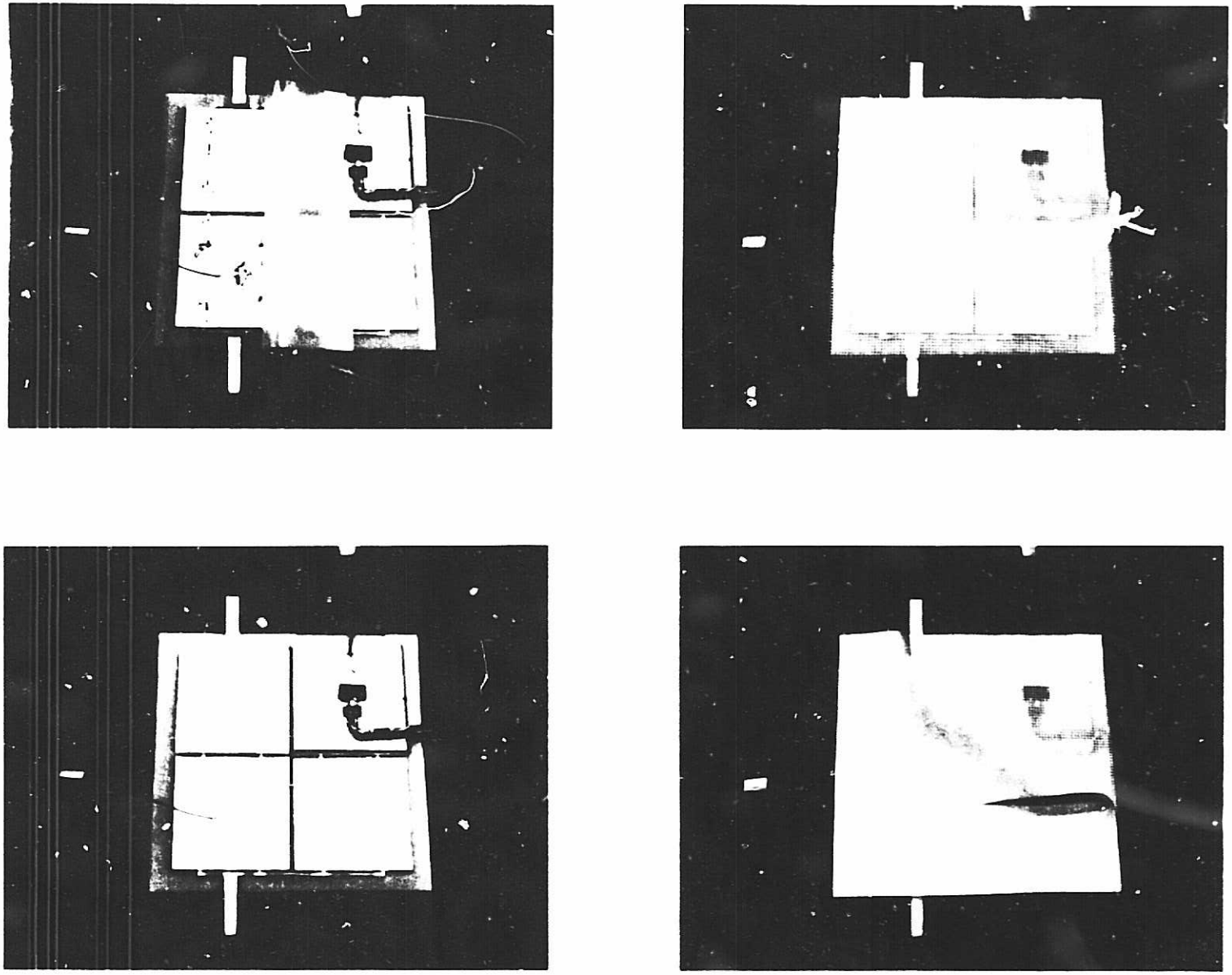


Figure 3-14. Assembly Steps for the Fabrication of the Encapsulation Test Specimens

circuit. This short occurred at point where the anode lead was folded to permit exit at the bottom as shown in Figure 3-13. The extra material thickness at this point was sufficient to force the sheared edge of the copper foil through the insulating tape to make contact with the solar cell metallization. This weak point in the insulation system can be eliminated by using only straight runs of the anode lead with more carefully control of the edge burrs on the copper strip or by the use of multiple insulating layers in the area of a fold in the conductor. In any case the thickness of the insulating tape should be significantly greater than the anticipated height of any burr on the copper strips.

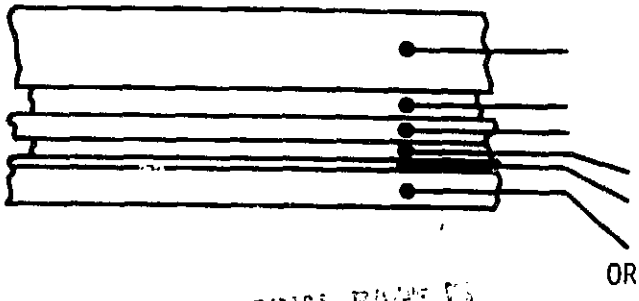
3.5 THERMAL ANALYSIS

A multi-node steady-state thermal analysis was performed using a detailed model of the lamination stack-up with three different heat spreader plate sizes: 1.33, 4, and 12 inches square. The nodal representation for the 4 inches square case is diagrammed in Figure 3-15 where the heat spreader has been divided in nine nodes as identified by numbers 17 through 25. This nodal format is carried through to intervening layer of EVA and into the solar cell circuit layer where four additional larger area nodes are included to more accurately calculate the effects of lateral conduction in this silicon layer.

Boundary conditions and assumptions for this analysis included the following:

1. Adiabatic rear surface to simulate the worst case condition of a module mounted directly to an insulated surface
2. Total insolation level of 0.8 and 1.0 kW/m^2
3. Wind speed < 1 m/s
4. Ambient temperatures of 20 and $40^{o}C$

These constraints were combined with the three heat spreader plate sizes to produce a matrix of simulation cases covering a wide range of operating conditions. In an effort to summarize these results in a convenient form for later use in diode mount sizing and comparison with test results, a temperature difference approach was adopted to normalize and combine these analytical predictions. With no internal diode heat dissipation the embedded diode temperature rise above ambient is given in Figure 3-16 as a function of ambient temperature and insolation. These predicted temperature



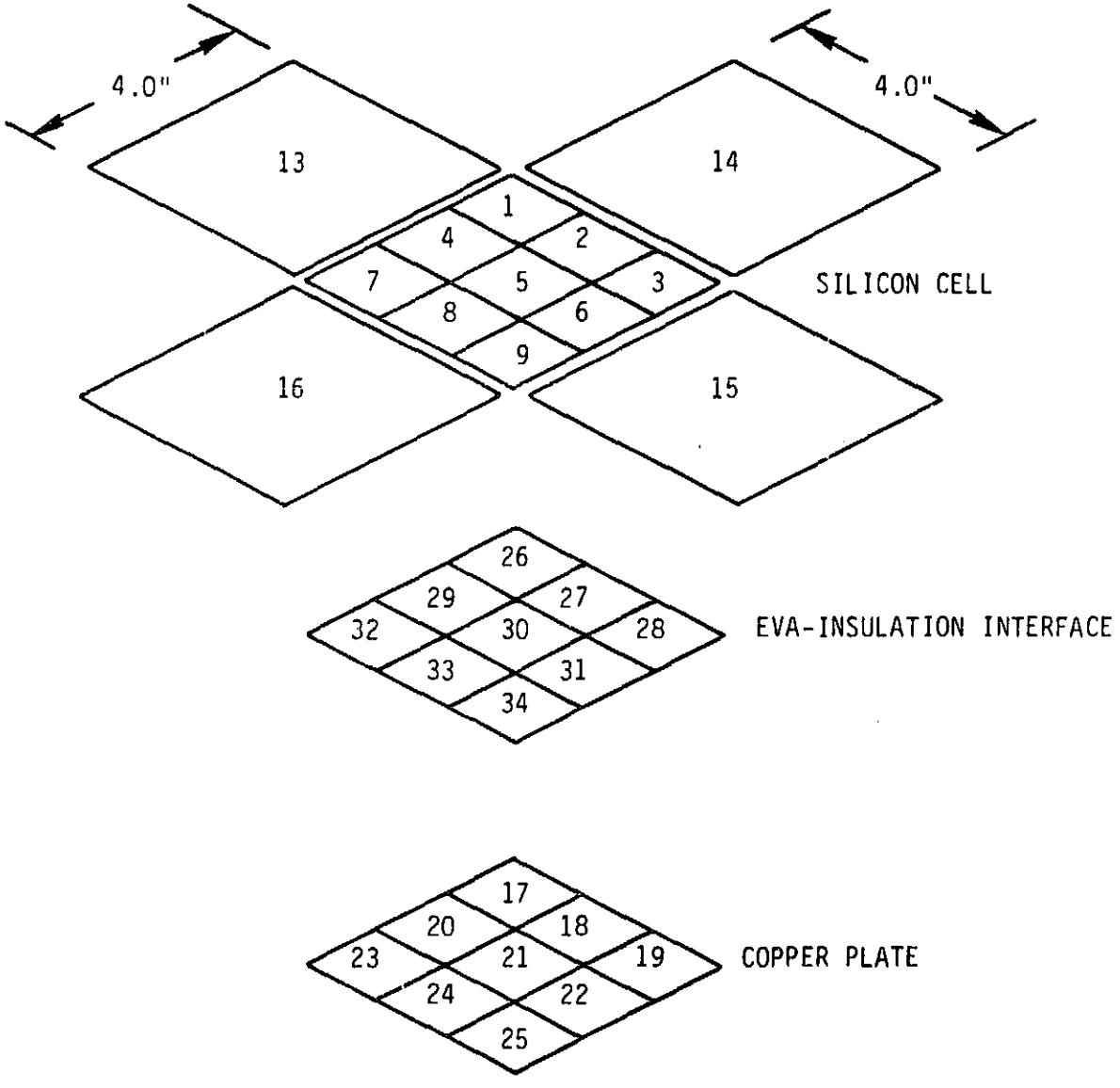


Figure 3-15. Bypass Diode Thermal Model for a 4 Inch Square Heat Spreader Plate

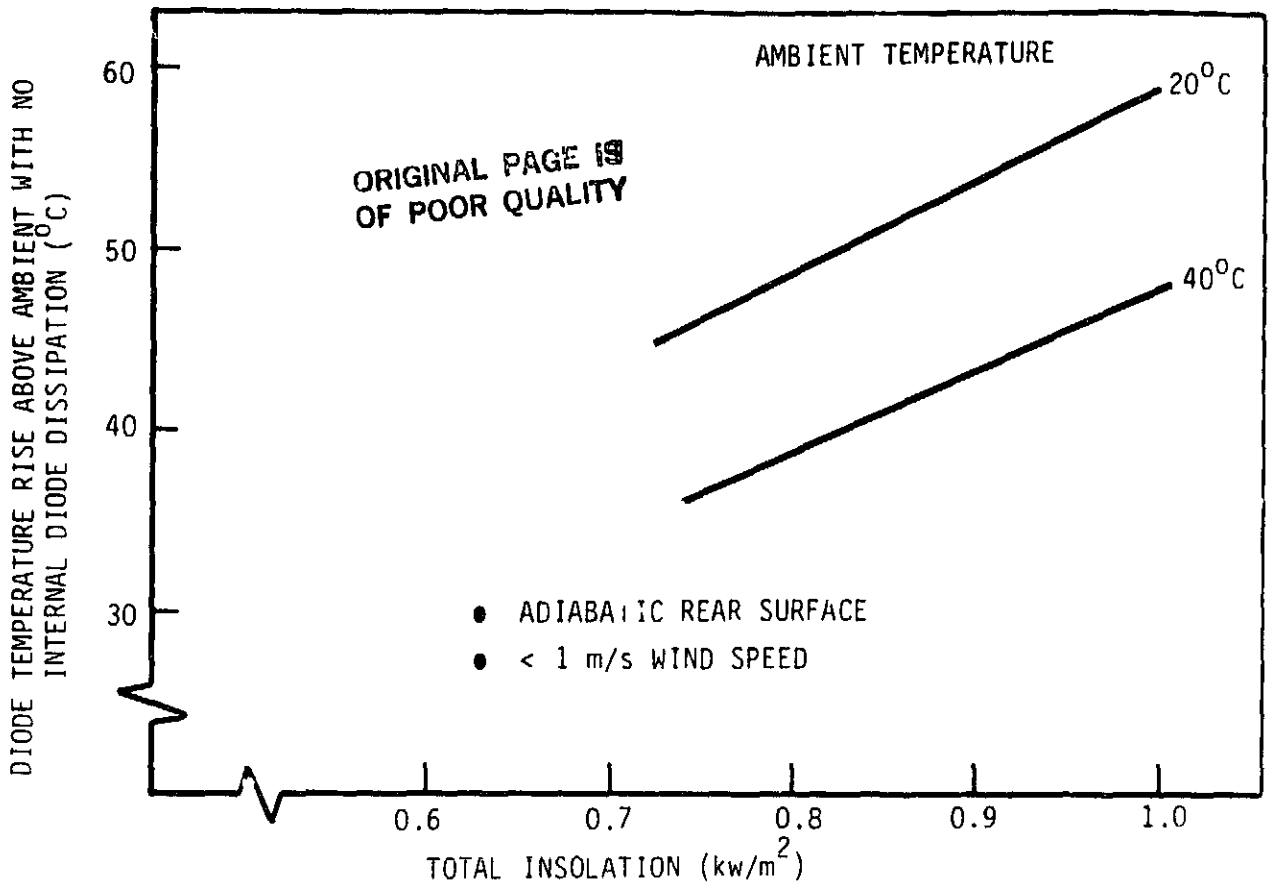


Figure 3-16. Diode Temperature Rise Above Ambient with No Internal Diode Dissipation as a Function of Total Insolation and Ambient Temperature

rises above ambient are somewhat larger than might be predicted for a direct-mounted solar cell module, but this is of little consequence since the temperature difference approach used to present the diode temperature rise will permit the use of any appropriate data relating solar cell temperature to insolation and ambient temperature.

Figure 3-17 establishes the relationship between the diode junction temperature rise above the normal steady-state diode temperature with no internal dissipation (also approximately equal to the operating temperature of the solar cells within the module with only solar heating) to the square copper heat spreader plate area and diode heat dissipation. Implicit in these data is a junction-to-heat spreader thermal resistance of 1°C per watt, representing the maximum value measured on development test specimens as reported in Section 3.3.2. A cross-plot of the data contained in Figure

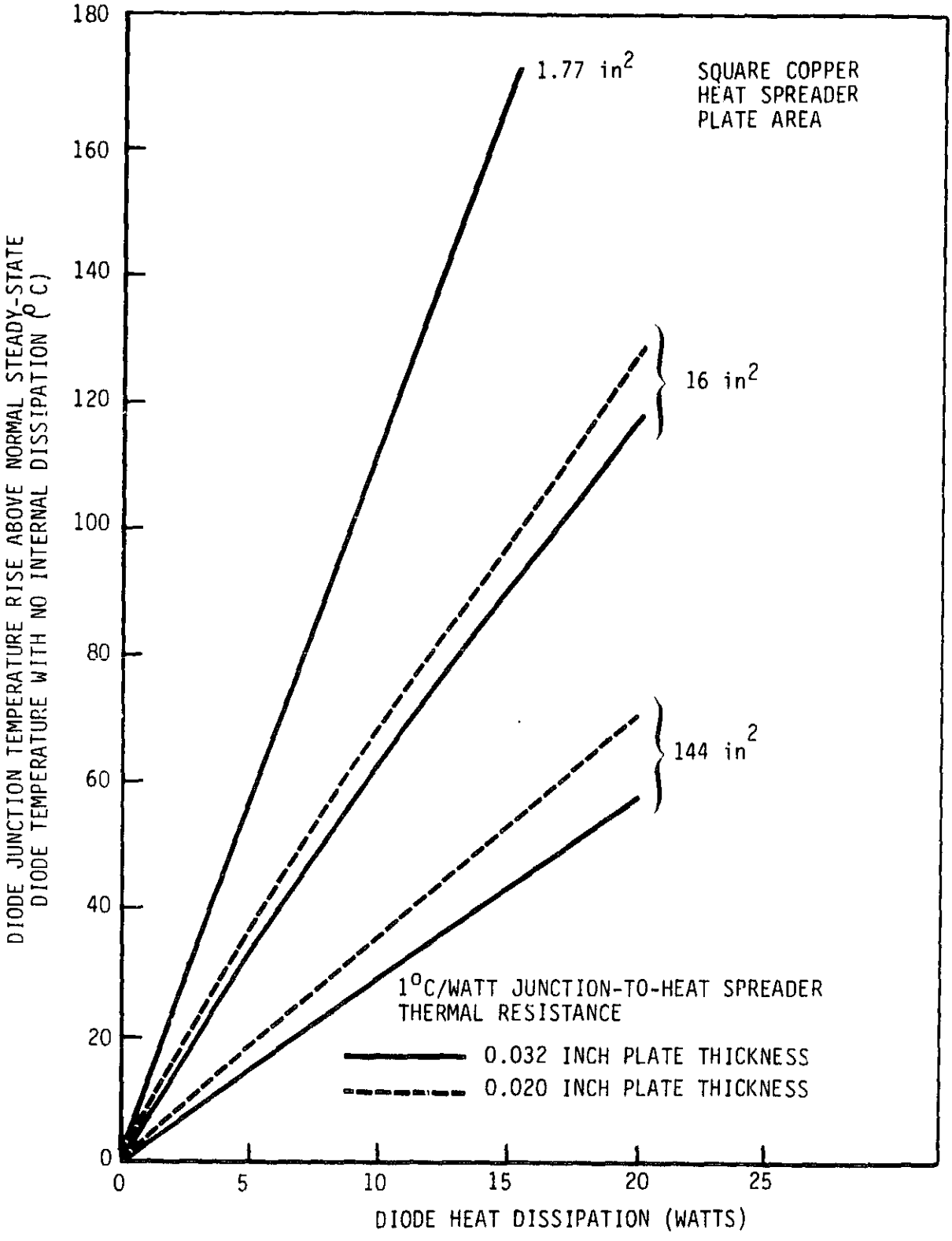


Figure 3-17. Diode Junction Temperature Rise as a Function of Heat Spreader Area and Heat Dissipation

3-17 yields the square heat spreader plate area required to maintain the temperature rise of this plate, near the diode, to a specified value as shown in Figure 3-18. The temperature difference displayed on this plot is identical to that used on Figure 3-17 except that the value has been reduced to account for the temperature drop between the diode junction and the heat spreader plate near the diode mounting location. A thermal resistance of $1.^{o}C$ per watt was used to make this data translation. The following example illustrates how these analytically predicted temperature difference plots can be used to establish the heat-spreader plate area required for a specified diode heat dissipation. Assuming, in the worst-case, that the ambient temperature is $40^{o}C$ with an insolation of 1.0 kW/m^2, Figure 3-16 yields $88^{o}C$ ($48^{o}C$ + $40^{o}C$) as the temperature of the active module components with no internal heat dissipation. Using $130^{o}C$ as the maximum allowable EVA temperature in contact with the heat spreader, $42^{o}C$ of temperature rise in this plate near the diode is permissible due to internal diode heat dissipation. With 5 watts of internal diode heat generation, Figure 3-18 yields 4.4 in^2 as the required square heat spreader area.

Figure 3-19 summarizes the results of similar calculations performed for 20 and $40^{o}C$ ambient temperatures with insolation levels of 0.8 and 1.0 kW/m^2. Thus, this figure defines the 0.032 inch thick square copper heat spreader size required to limit the EVA temperature to the established $130^{o}C$ maximum. If a $40^{o}C$ ambient temperature with a 1.0 kW/m^2 total insolation is considered to represent worst-case design condition, the upper curve of Figure 3-19 can be specified as the heat spreader design curve for sizing purposes. It remains to be seen if these analytical predictions can be experimentally verified. To this end, three modules, containing a total of six different size heat spreaders, were designed, fabricated and tested as described in the following section.

3.6 EXPERIMENTAL MODULE DESIGN

3.6.1 CONFIGURATION

Three active module segments were designed and fabricated as test specimens for the experimental determination of the heat spreader temperature as a function of plate size and diode heat dissipation. As described in Table 3-16 each of these modules, designated as 6A, 12A and 18A corresponding to

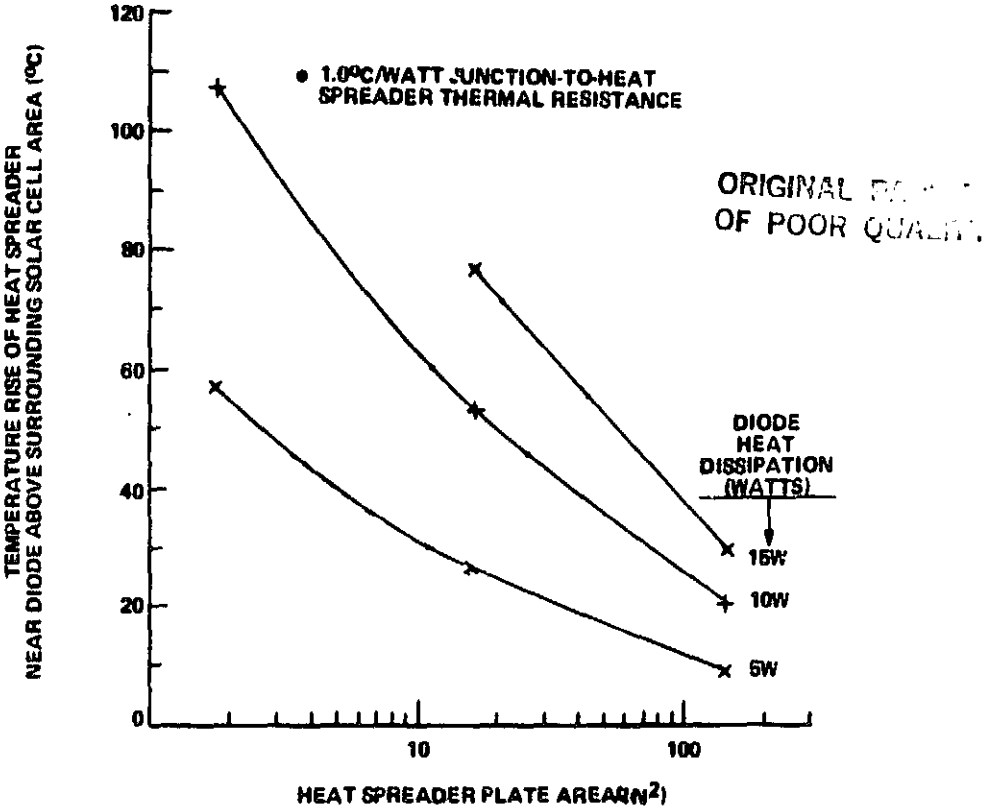


Figure 3-18. Maximum Heat Spreader Plate Temperature Rise Above Solar Cell Temperature

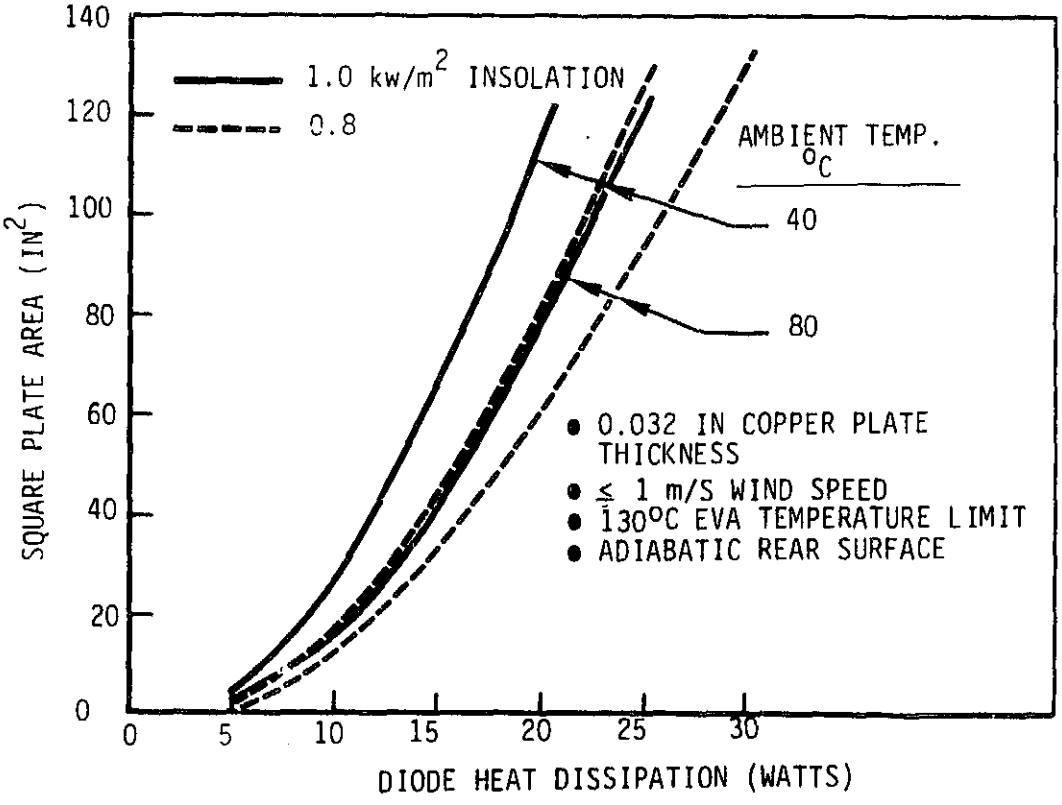


Figure 3-19. Square Plate Area Required to Limit the EVA Temperature to 130°C

Table 3-16. Design Characteristics of Experimental Modules

Module Designation	Module Rated* Short-Circuit Current (Amp)	Diode Type and Rating	Square Copper Heat Spreader Area (in^2)
6A	6	Semicon PN 20 Amp	2.0 4.0
12A	12	Semicon PN 40 Amp	15.2 27.0
18A	18	Semicon PN 50 Amp	39.7 65.6

* At 1.0 kW/m^2 insolation and 25°C cell temperature

the module rated short-circuit current, was constructed with two heat spreader plates of differing sizes. In this way it was possible to cover a wide range of heat spreader areas from 2 to 65.6 in^2 while maintaining representative encapsulation boundary conditions including the influences from surrounding solar cells and circuit termination conductors. As shown in Figure 3-20 the electrical circuit arrangement of each module was configured to supply a representative level of rated short-circuit current corresponding to the number of parallel-connected 100mm square solar cells. The bypass diode circuits were also configured to permit the external introduction of forward current, independent of the solar cell circuit. Thus, these module designs permit the testing of the bypass diodes either as an integral part of the solar cell circuit, where the bypassed current is determined by the short-circuit current capability of the solar cell circuit, or as independent bypass circuit elements where the solar cells function only thermally as a part of the heat rejection path for the diode.

A rear view of each module assembly, showing the details of the diode/heat spreader assembly installation, is pictured in Figures 3-21 through 3-23. It is important to note the location of the five thermocouples which are laminated within the encapsulation system to monitor heat spreader temperature rise. The temperature is measured at two locations on each

copper heat spreader plate by thermocouples bonded at locations which are 0.12 inches from the diode body and 0.17 inches in from the corner on the diagonal. The fifth thermocouple is bonded to the rear contact of a solar cell which is removed from the influence of the localized diode heating.

3.6.2 TEST RESULTS

The three experimental modules described above were subjected to a series of thermal characteristic tests involving the external introduction of bypass circuit current to force a diode heat dissipation which could be varied with the value of the current supplied. These tests were performed under room ambient conditions with the modules mounted face-up on a horizontal work bench surface. An 2 inch thick styrofoam insulation board was placed under the modules to virtually eliminate heat rejection from the rear side. The externally supplied bypass current was varied to produce a range of diode heat dissipations. At each constant current level the module was allowed to reach thermal equilibrium before the thermocouple readings were recorded. The results for the eleven test conditions simulated are summarized in Table 3-17. The difference between the temperature measured on the heat spreader near the diode body and the surrounding solar cell temperature is plotted in Figure 3-24 to permit a direct comparison with the analytical predictions previously presented in Figure 3-18.

The poor agreement between the analytical predictions and the experimental results becomes more apparent when these results are represented in terms of the plate area required for a given diode heat dissipation as shown in Figure 3-25. Using a $40^{o}C$ ambient temperature with a 1.0 kW/m^2 insolation as a design condition, the analytical model would predict the requirement for 65 in^2 of heat spreader plate area for 15 watts of diode dissipation. Under these same design conditions the experimental data indicates that 11 in^2 of plate area would suffice. The source of this large discrepancy is thought to be the lateral conduction of heat through solar cell material which was not adequately accounted for in the model.

3.7 COST COMPARISON OF BYPASS DIODE IMPLEMENTATION APPROACHES

Since cost is of paramount concern in the selection of any bypass diode implementation approach for terrestrial photovoltaic arrays, an assessment of this factor was performed for both candidate packaging options, viz., the

Table 3-17. Experimental Module Thermal Test Results

Run No.	Module Designation	Heat Spreader Designation	Bypass Current (Amp)	Diode Voltage Drop (Volts)	Diode Heat Dissipation (Watts)	Temperature (^{o}C)		
						Heat Spreader Near Diode	Heat Spreader Corner	Solar Cells
1	6A	Small (2.0 in^2)	6.2	0.842	5.2	52.8	50.6	26.1
2	6A	Small (2.0 in^2)	12.4	0.862	10.7	79.4	75.6	26.1
3	6A	Large (4.0 in^2)	6.1	0.868	5.3	50.0	47.2	25.6
4	6A	Large (4.0 in^2)	12.4	0.839	10.4	67.2	61.1	23.9
5	6A	Large (4.0 in^2)	17.7	0.836	14.8	98.9	80.6	23.9
6	12A	Small (15.2 in^2)	12.4	0.884	11.0	52.2	43.9	27.8
7	12A	Small (15.2 in^2)	6.4	0.823	5.2	36.1	32.2	23.3
8	12A	Small (15.2 in^2)	17.8	0.868	15.5	61.1	50.0	25.0
9	12A	Large (27.0 in^2)	12.4	0.955	11.8	48.3	39.4	29.4
10	18A	Small (39.7 in^2)	18.6	0.880	16.4	52.8	41.7	25.0
11	18A	Large (65.6 in^2)	18.5	0.825	15.3	52.2	38.3	28.3

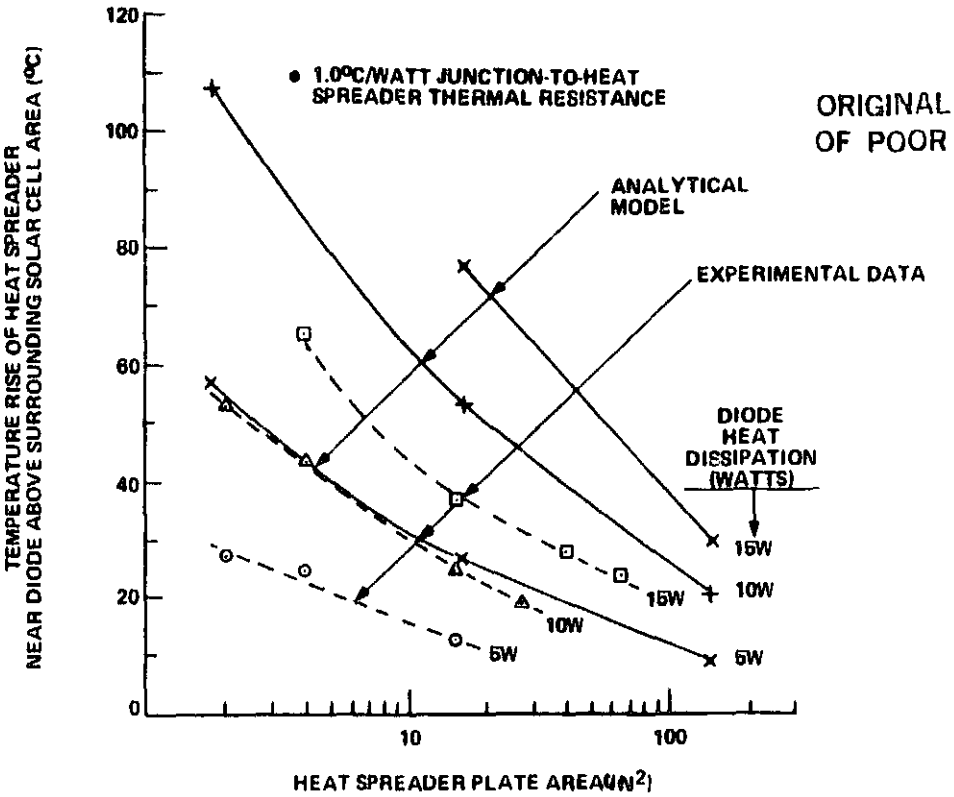


Figure 3-24. Comparison of Analytical and Experimental Results

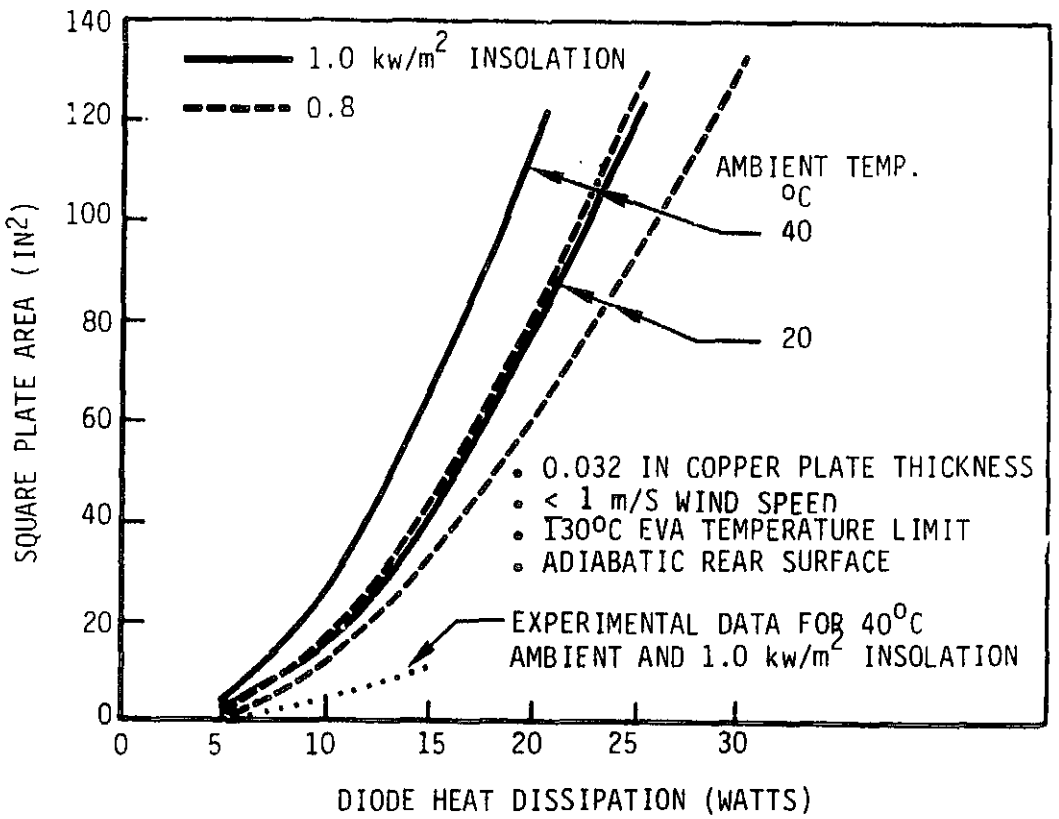


Figure 3-25. Comparison of Heat Spreader Plate Area Requirements Between Analytical and Experimental Results

encapsulated diode/heat spreader and the externally-mounted, conventional diode.

3.7.1 COST ANALYSIS OF ENCAPSULATED BYPASS DIODE/HEAT SPREADER ASSEMBLY

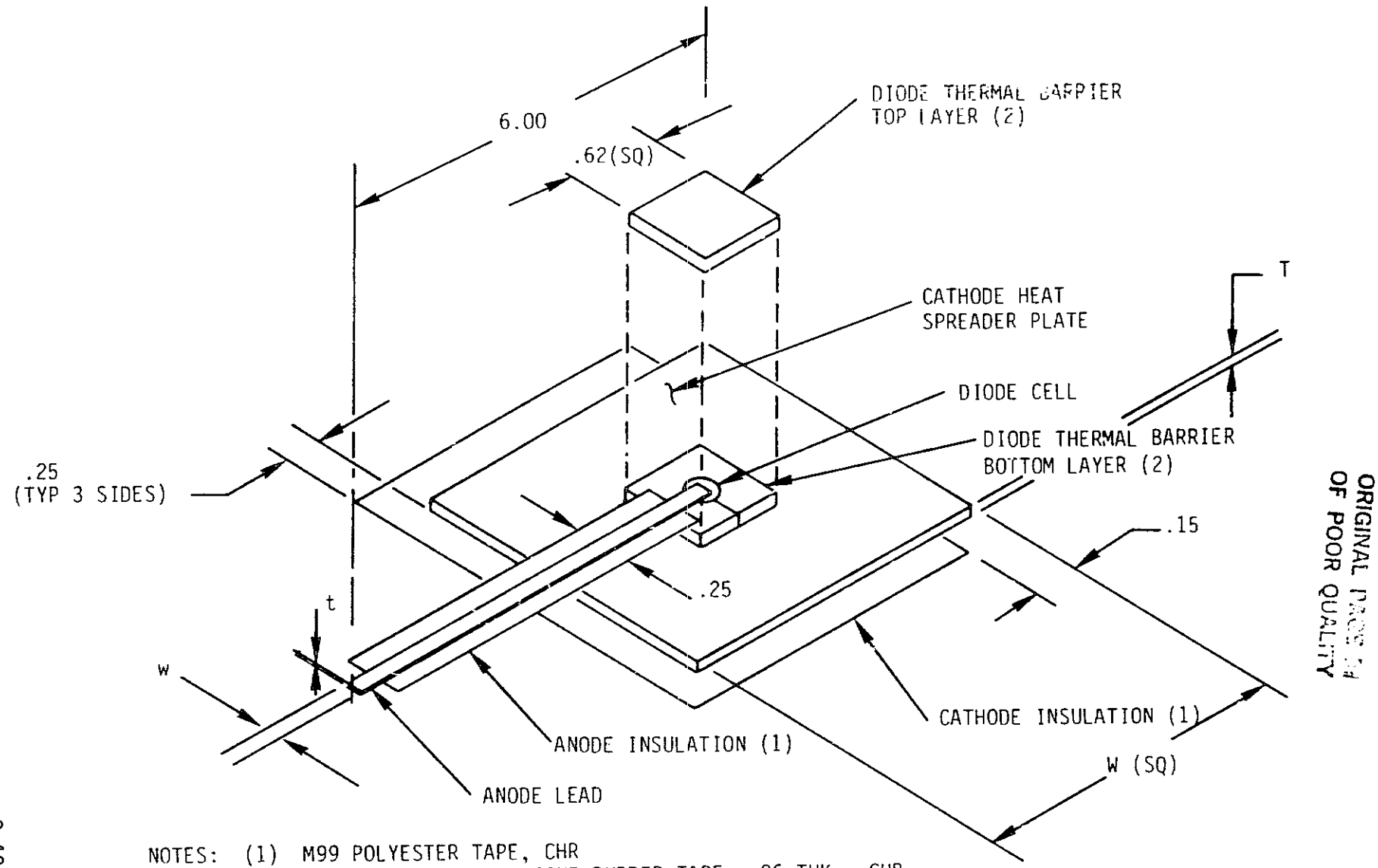
The encapsulated bypass diode/heat spreader configuration shown in Figure 3-26 was sized for three levels of rated bypass current using the experimental results reported in Section 3.6.2. The pertinent physical parameters for these three assembly sizes are as specified in Table 3-18.

At each of these three current levels, the cost analysis is to include the effects of two heat spreader plate materials (i.e., copper and aluminum), assuming that the plate size is unchanged but that the aluminum thickness is increased to compensate for its lower thermal conductivity. The number of bypass diode/heat spreader assemblies required to satisfy the annual production needs of 1000, 10000 and 50000 m^2 of module area will vary with the current rating of the unit. Using 30 mA/cm^2 as the solar cell short-circuit current density at 100 mW/cm^2 insolation and assuming that each bypass group consists of 12 series-connected cell groups, it is possible to calculate the number of bypass diodes required for each of these module production rates with the results as given in Table 3-19.

3.7.1.1 Assumptions and Costing Methodology

The methodology employed for this cost analysis consisted of first preparing a set of detailed drawings defining each subassembly and each individual component of the unit to be fabricated. A complete set of these drawings is contained in Appendix B. Local vendors specializing in the particular fabrication area involved for each of the piece parts were asked to provide price quotations based on the component drawing for the quantities required to cover the production rate range of interest.

These material costs were accumulated for later use in estimating the total FOB factory cost of the assembly. In parallel with the acquisition of this material cost data a process flow sequence was defined and an experienced manufacturing engineer was employed to estimate the direct labor required for each assembly step. The sum of the labor required for each step was then adjusted for work productivity and other handling and equipment



NOTES: (1) M99 POLYESTER TAPE, CHR
(2) "STICK & BOND" SILICONE RUBBER TAPE, .06 THK., CHR

Figure 3-26. Configuration of Diode/Heat Spreader Assembly

Table 3-18. Diode/Heat Spreader Assembly Design Parameters

Rated Bypass Current (Amperes)	Diode Cell Manufacturer/Rating	Cathode Heat Spreader Plate			Anode Lead		
		Material	T (inches)	W (inches)	Material	t (inches)	w (inches)
6	Semicon/20 Amp	Copper	0.032	0.90	Copper	0.005	0.120
6	Semicon/20 Amp	Aluminum	0.056	0.90	Copper	0.005	0.120
12	Semicon/40 Amp	Copper	0.032	2.10	Copper	0.007	0.170
12	Semicon/40 Amp	Aluminum	0.056	2.10	Copper	0.007	0.170
18	Semicon/50 Amp	Copper	0.032	3.30	Copper	0.010	0.180
18	Semicon/50 Amp	Aluminum	0.056	3.30	Copper	0.010	0.180

Table 3-19. Number of Bypass Diodes Required as a Function of Module Area

Bypass Current Rating (Amperes)	Annual Module Production Rate (m^2)		
	1000	10,000	50,000
6	3,750	37,500	187,500
8	2,813	28,125	140,625
12	1,880	18,800	94,000
18	1,250	12,500	62,500
30	750	7,500	37,500

downtime delays to produce the total estimated assembly labor for each unit. The direct labor cost was then obtained by multiplying this total time (in hours) by an average hourly rate of $10.80, which assumes a U.S. assembly plant location.

The direct labor cost, when burdened with a 180 percent overhead rate, are added to the total material costs, which are burdened by a 3 percent material overhead, to obtain the total estimated cost to fabricate the assembly. A 25 percent profit margin was applied to this cost to obtain the estimated FOB factory price of the assembly.

3.7.1.2 Details of Process Flow

The cost of fabricating the three different sizes of bypass diode/heat spreader assemblies was analyzed based on the flow sequence shown in Figure 3-27 for the entire range of annual production rates from 1000 to 200,000 units per year. It was felt that, even at the upper end of this range, the rates are still sufficiently low to permit the use of the same basic process described in the diagram. The assembly of the seven parts which constitute a bypass diode/heat spreader begins at the upper left of the diagram where the pre-fabricated cathode heat spreader plate and anode lead are loaded into a soldering fixture along with the solder preforms and the diode cell. The incoming diode cells are individually checked to verify polarity, forward voltage drop at a specified test current, and leakage current at 50 V reverse voltage.

After passing through the tunnel oven the soldered diode/heat spreader plate subassemblies are unloaded from the fixture and tested again, by the measurement of forward voltage drop at a specified test current and leakage current at a 50V reverse voltage, to verify that the soldering process did not destroy the integrity of the diodes. At this point the subassemblies which have satisfactorily passed the electrical screening test are loaded into vapor degreaser racks and cycled through the degreaser to remove residual solder flux. The cleaned subassemblies are stored to await the subsequent taping and insulation process step. The cathode plate and anode lead insulating tapes are dispensed onto the soldered subassemblies which have been removed from storage and placed in a locating fixture. The assembly is completed by installing the two layer silicone foamed tape

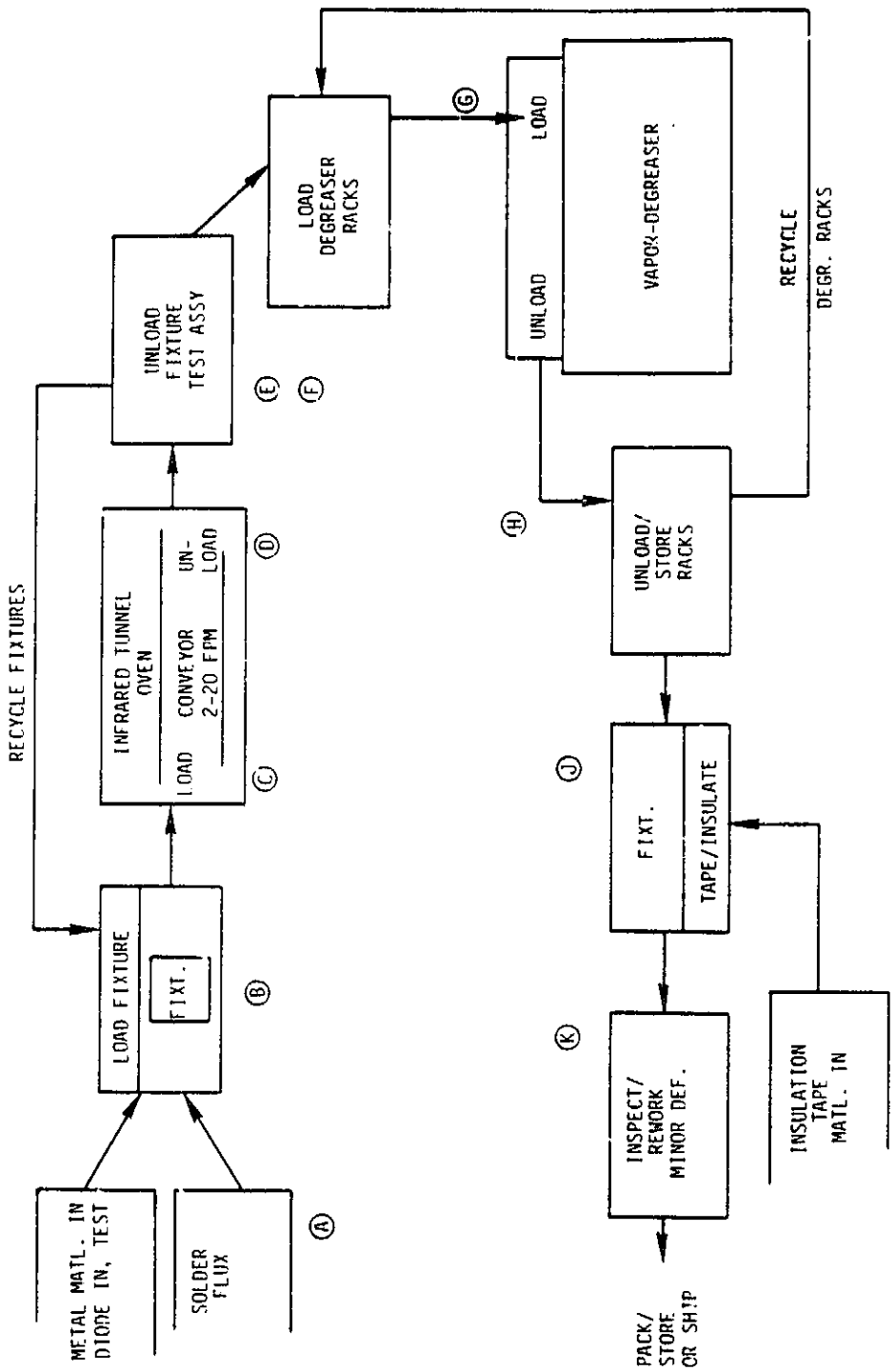


Figure 3-27. Assembly Flow Diagram

thermal barrier. A final inspection is performed and minor rework is accomplished prior to packing in cardboard boxes for storage and subsequent shipment to the module manufacturer.

3.7.1.3 Direct Labor Estimates

The flow sequence described in previous section was used to estimate the direct labor required for each step of the assembly process with the results as summarized in Tables 3-20, 3-21 and 3-22. As the size of the cathode heat spreader plate increases with the current rating of the assembly, the number of parts that can be loaded onto a single soldering fixture, which is sized for the tunnel oven opening, decreases as shown in these tables. For the range of production rates to be considered in this evaluation, it is felt that this estimate of the direct labor hours per unit can be used, with reasonable accuracy, to predict the labor cost over the entire range. Table 3-23 summarizes the labor content for each of the three assembly current ratings and includes several adjustments to this direct labor to reflect productivity factors, including: (1) a 50 minute working time per hour, (2) a 20 percent time loss due to parts handling and equipment downtime, and (3) a 98 percent overall process yield. The resulting adjusted direct labor per unit is converted in a burdened labor cost, as shown in Table 3-24, by first multiplying the hours per unit by the average hourly rate and then applying a 180 percent labor overhead factor.

3.7.1.4 Production Cost Summary

The FOB factory cost of producing the three sizes of the encapsulated bypass diode/heat spreader assembly was estimated by combining the direct labor and overhead costs from the previous section with the material costs as obtained from vendor quotes for each piece part as defined by the detail drawings. These material cost estimates are summarized in Tables 3-25, 3-26 and 3-27 for the 6, 12 and 18 ampere current ratings, respectively. Two materials (viz., copper and aluminum) were considered for use in the fabrication of the cathode heat spreader plate. The cost quotation obtained for these parts indicate that there is no advantage to be gained by using aluminum for this component. The increased difficulty in plating aluminum, relative to copper, is reflected in a differential plating cost which is more than enough to offset the initial cost advantage of the aluminum.

Table 3-20. Direct Labor Estimate for the 6 Ampere Assemblies

Description of Operation		Labor-Seconds per Unit
Operation 10-Solder Diode Assembly*		
.10	Place Cathode Plates in Fixture	1.7
.20	Clean Parts With Alcohol	3.3
.30	Position Diode Template	0.2
.40	Place Preforms/Flux in Fixture	3.3
.50	Place Diodes	1.7
.60	Place Preforms/Flux	1.7
.70	Clean Anode Straps With Alcohol	0.2
.80	Place Anode Straps in Fixture	1.7
.90	Drop Fixture Holding Device and Latch	0.2
.100	Place Fixtured Parts in Oven	0.3
.110	Bake Cycle/Cool Cycle	---
.120	Unload Fixture/Template	3.3
.130	Check Resistance and Etch Part Number	5.0
.140	Load Parts in Vapor-Degreaser Rack	3.3
.150	Vapor-Degrease Cycle	0.3
.160	Store Rack for Oper. 20	0.3
	Sub-Total	26.5
Operation 20-Insulate Soldered Diodes		
.10	Strip Anode Tape	1.8
.20	Place Soldered Assembly in Template	2.9
.30	Apply Anode Tape	7.2
.40	Strip Cathode Tape	1.8
.50	Place/Press Cathode Tape	7.2
.60	Remove Taped Assy From Template and Invert on Table	1.8
.70	Strip Keyhole Insulator	1.8
.80	Apply/Press Insulator Around Diode	14.4
.90	Strip Top Insulation	1.8
.100	Apply/Press Top Insulation	10.8
.110	Place Completed Assembly in Storage Tray	2.9
	Sub-Total	54.4
Operation 30-Diode Preparation		
.10	Measure Diode Resistance/Record	5.8
.20	Mark Cathode Side	4.6
.30	Degrease Cycle	0.4
	Sub-Total	10.8
	Total	91.7 (0.0255 Hrs.)

* Labor estimate is based on 35 assemblies per template load.

Table 3-21. Direct Labor Estimate for the 12 Ampere Assemblies

Description of Operation		Labor-Seconds per Unit
Operation 10-Solder Diode Assembly*		
.10	Place Cathode Plates in Fixture	1.7
.20	Clean Parts With Alcohol	3.4
.30	Position Diode Template	0.4
.40	Place Preforms/Flux in Fixture	3.4
.50	Place Diodes	1.7
.60	Place Preforms/Flux	3.4
.70	Clean Anode Straps With Alcohol	0.4
.80	Place Anode Straps in Fixture	1.7
.90	Drop Fixture Holding Device and Latch	0.4
.100	Place Fixtured Parts in Oven	0.6
.110	Bake Cycle/Cool Cycle	---
.120	Unload Fixture/Template	3.4
.130	Check Resistance and Etch Part Number	6.0
.140	Load Parts in Vapor-Degreaser Rack	3.4
.150	Vapor-Degrease Cycle	0.6
.160	Store Rack for Oper. 20	0.6
	Sub-Total	31.1
Operation 20-Insulate Soldered Diodes		
.10	Strip Anode Tape	1.8
.20	Place Soldered Assembly in Template	2.9
.30	Apply Anode Tape	7.2
.40	Strip Cathode Tape	1.8
.50	Place/Press Cathode Tape	7.2
.60	Remove Taped Assy From Template and Invert on Table	1.8
.70	Strip Keyhole Insulator	1.8
.80	Apply/Press Insulator Around Diode	14.4
.90	Strip Top Insulation	1.8
.100	Apply/Press Top Insulation	10.8
.110	Place Completed Assembly in Storage Tray	2.9
	Sub-Total	54.4
Operation 30-Diode Preparation		
.10	Measure Diode Resistance/Record	5.8
.20	Mark Cathode Side	4.6
.30	Degrease Cycle	0.4
	Sub-Total	10.8
	Total	96.3 (0.0268 Hrs.)

* Labor estimate is based on 17 assemblies per template load.

Table 3-22. Direct Labor Estimate for the 18 Ampere Assemblies

Description of Operation		Labor-Seconds per Unit
Operation 10-Solder Diode Assembly*		
.10	Place Cathode Plates in Fixture	1.6
.20	Clean Parts With Alcohol	3.2
.30	Position Diode Template	0.8
.40	Place Preforms/Flux in Fixture	3.2
.50	Place Diodes	1.6
.60	Place Preforms/Flux	3.2
.70	Clean Anode Straps With Alcohol	0.8
.80	Place Anode Straps in Fixture	1.6
.90	Drop Fixture Holding Device and Latch	0.8
.100	Place Fixtured Parts in Oven	1.2
.110	Bake Cycle/Cool Cycle	---
.120	UnLoad Fixture/Template	6.4
.130	Check Resistance and Etch Part Number	5.6
.140	Load Parts in Vapor-Degreaser Rack	3.2
.150	Vapor-Degrease Cycle	1.2
.160	Store Rack for Oper. 20	1.2
	Sub-Total	35.6
Operation 20-Insulate Soldered Diodes		
.10	Strip Anode Tape	1.8
.20	Place Soldered Assembly in Template	2.9
.30	Apply Anode Tape	7.2
.40	Strip Cathode Tape	2.9
.50	Place/Press Cathode Tape	14.4
.60	Remove Taped Assy From Template and Invert on Table	1.8
.70	Strip Keyhole Insulator	1.8
.80	Apply/Press Insulator Around Diode	14.4
.90	Strip Top Insulation	1.8
.100	Apply/Press Top Insulation	10.8
.110	Place Completed Assembly in Storage Tray	2.9
	Sub-Total	62.7
Operation 30-Diode Preparation		
.10	Measure Diode Resistance/Record	5.8
.20	Mark Cathode Side	4.7
.30	Degrease Cycle	0.7
	Sub-Total	11.2
	Total	109.5 (0.0304 Hrs.)

* Labor estimate is based on 9 assemblies per template load.

Table 3-23. Summary of Direct Labor Requirements

Assembly Current Rating (Amperes)	Direct Labor (Hrs. per Unit)			
	Unadjusted	Adjusted for 50 Minute Hour	Adjusted for Handling and Delays	Adjusted for 98% Yield
6	0.0255	0.0306	0.0368	0.0375
12	0.0268	0.0322	0.0388	0.0396
18	0.0304	0.0365	0.0438	0.0447

Table 3-24. Direct Labor Costs

Assembly Current Rating (Amperes)	Adjusted Labor Hours Per Unit	Direct* Labor Costs (1983 $/Unit)	Overhead at 180% (1983 $/Unit)	Total Burdened Labor Cost (1983 $/Unit)
6	0.0375	0.405	0.729	1.134
12	0.0396	0.428	0.770	1.198
18	0.0447	0.483	0.869	1.352

* Based on an average labor rate of $9.00/hour plus a 20% burden for benefits = $10.80/hour

Figure 3-28 gives the estimated FOB factory price of the three assembly current ratings as a function of annual production rate. It should be noted that this price includes a 25 percent profit mark-up.

In support of this analysis, John-Watt Associates, Inc. prepared an independent estimate of the price of the completed assemblies in the three sizes specified. The agreement between these independently-derived

Table 3-25. Material Cost Summary for the 6 Ampere Assembly (1983 $/Unit)

Component Description	Annual Production Rate (Units/Year) 1,000	10,000	100,000	200,000
Copper Cathode Plate	0.2850	0.1600	0.1530	0.1500
Aluminum Cathode Plate	0.3200	0.1890	0.1840	0.1810
Anode Lead	0.9600	0.8100	0.1080	0.0378
Solder Preforms	0.3450	0.0412	0.0068	0.0046
Diode Cell	0.2400	0.2000	0.1500	0.1350
Anode Insulator Tape	--*	0.0850	0.0085	0.0043
Cathode Insulator Tape	0.2500	0.1350	0.0135	0.0068
Thermal Barrier Tape	0.2168	0.1278	0.1004	0.0652
Totals**				
With Copper Cathode	2.366	1.606	0.556	0.416
With Aluminum Cathode	2.402	1.636	0.588	0.448

* Included in the cost of the anode lead

** Includes an additional 3 percent burden for material overhead.

Table 3-26. Material Cost summary for the 12 Ampere Assembly (1983 $/Unit)

Component Description	Annual Production Rate (Units/Year) 1,000	10,000	100,000	200,000
Copper Cathode Plate	0.5250	0.3670	0.3530	0.3480
Aluminum Cathode Plate	0.5800	0.3880	0.3820	0.3770
Anode Lead	0.9600	0.8100	0.1080	0.0378
Solder Preforms	0.3450	0.0418	0.0074	0.0050
Diode Cell	0.4200	0.3500	0.2650	0.2400
Anode Insulator Tape	--*	0.0850	0.0085	0.0043
Cathode Insulator Tape	0.7500	0.4890	0.0489	0.0245
Thermal Barrier Tape	0.2168	0.1278	0.1004	0.0650
Totals**				
With Copper Cathode	3.314	2.338	0.918	0.746
With Aluminum Cathode	3.370	2.360	0.943	0.776

* Included in the cost of the anode lead.

** Includes an additional 3 percent burden for material overhead.

Table 3-27. Material Cost Summary for the 18 Ampere Assembly (1983 $/Unit)

Component Description	Annual Production Rate (Units/Year) 1,000	10,000	100,000	200,000
Copper Cathode Plate	0.8100	0.6950	0.6850	0.6800
Aluminum Cathode Plate	0.8840	0.7050	0.6800	0.6690
Anode Lead	0.9600	0.8100	0.1080	0.0378
Solder Preforms	0.3450	0.0443	0.0099	0.0075
Diode Cell	0.5900	0.5100	0.3800	0.3352
Anode Insulator Tape	-- *	0.0850	0.0085	0.0043
Cathode Insulator Tape	1.5000	1.0500	0.1050	0.0525
Thermal Barrier Tape	0.2168	0.1278	0.1004	0.0652
Totals**				
With Copper Cathode	4.555	3.422	1.439	1.218
With Aluminum Cathode	4.631	3.432	1.434	1.207

* Included in the cost of the anode lead.

** Includes an additional 3 percent burden for material overhead.

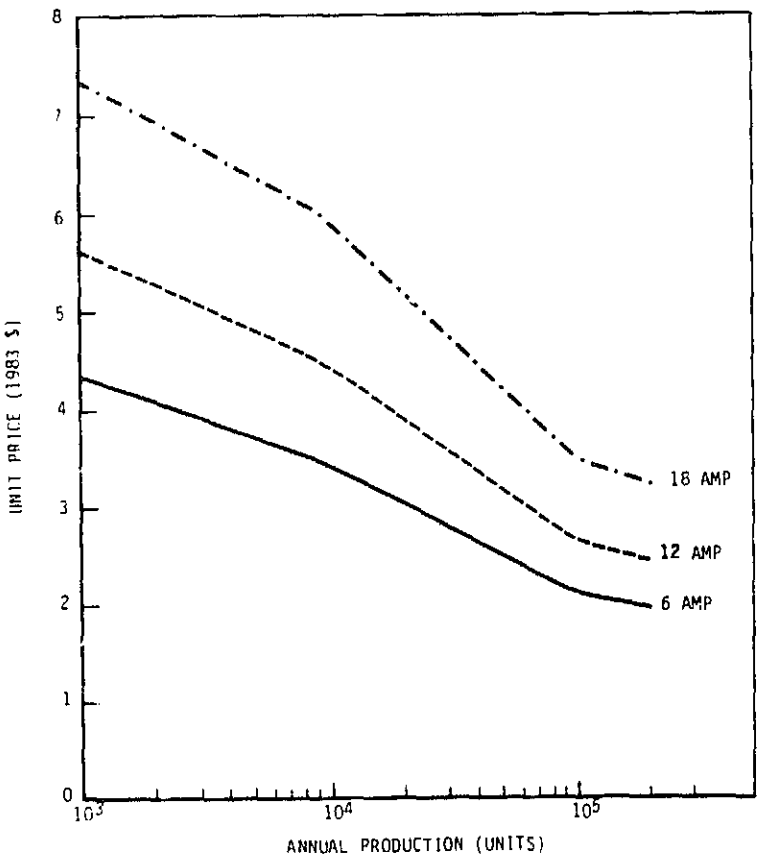


Figure 3-28. Estimated FOB Factory Price of the Encapsulated Bypass/Heat Spreader Assemblies

estimates was remarkably good with only a 40 percent difference at the worst point, which was for the smallest part at the highest production rate.

3.7.2 COST OF CONVENTIONAL DIODES AND DIODE ENCLOSURES

The enclosures shown in Figures 3-29, 3-30 and 3-31 are marketed by AMP Inc. for use with externally-mounted photovoltaic module diodes. These enclosures are designed for mounting to the frame or rear surface of the module, and in the latter two cases, the junction box also contains the mating connectors for module-to-module interconnecting wiring. The first two housings are designed to accept axial lead diodes while the last junction box, which is equipped with an extruded aluminum heat sink cover, can be used to mount a DO5 diode package.

Assuming a 150°C limit on PN diode junction temperature with a 40°C ambient temperature, the AMP thermal performance data indicates that these enclosures are capable of carrying forward diode currents of approximately 6, 8 and 30 amperes for the Figure 3-29, 3-30 and 3-31 enclosures, respectively.

The selling price of these AMP products as a function of the quantity purchased is given in Figure 3-32 [6] along with the price of typical packaged diodes which might be used in these enclosures [7]. If the price of the package diode is added to the price of the enclosure, the upper curve in each case gives the total price of the assembly exclusive of the labor required to mount the diode within the enclosure. It is apparent from these data that the pricing policy for the axial lead diode connector differs considerably from that used on the junction box enclosures. In fact, a reasonable extrapolation of the plastic cover junction box data would show cost parity with the axial lead diode connector enclosure at about 8000 units. These resulting prices are summarized in Table 3-28 for quantities of 1,000, 5,000 and 20,000 units.

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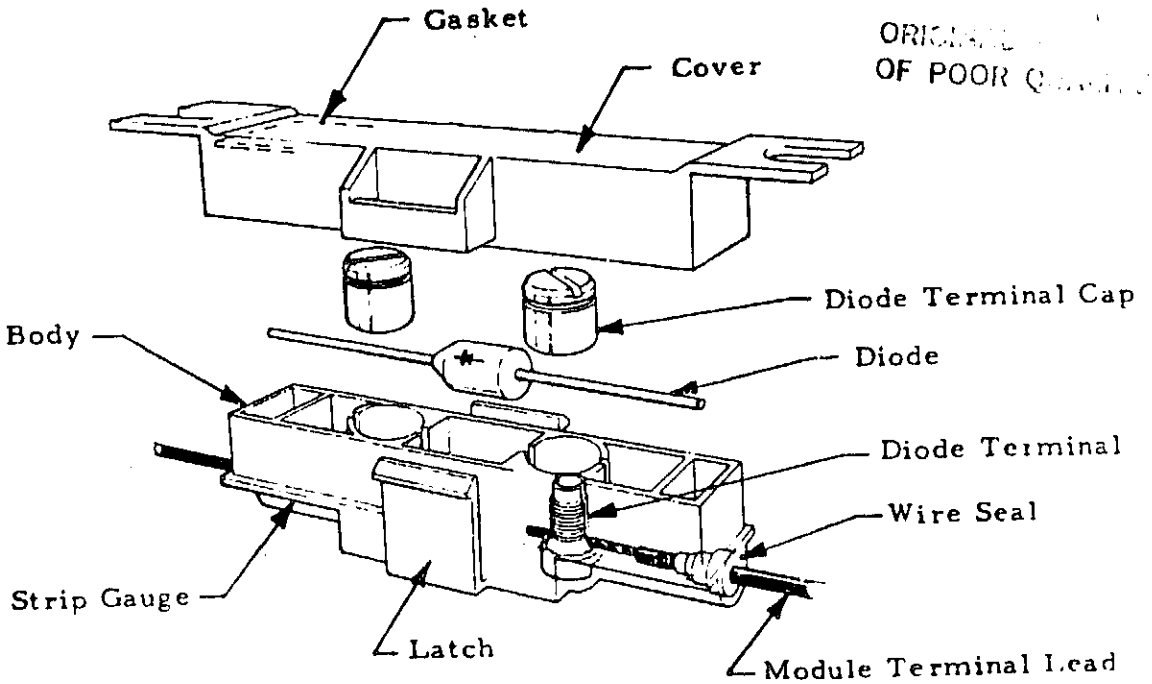
6. Private communication, M. Jones, AMP, Inc. March 3, 1983

7. Private communication, L. LeBow, Semicon, Inc., January 12, 1983.



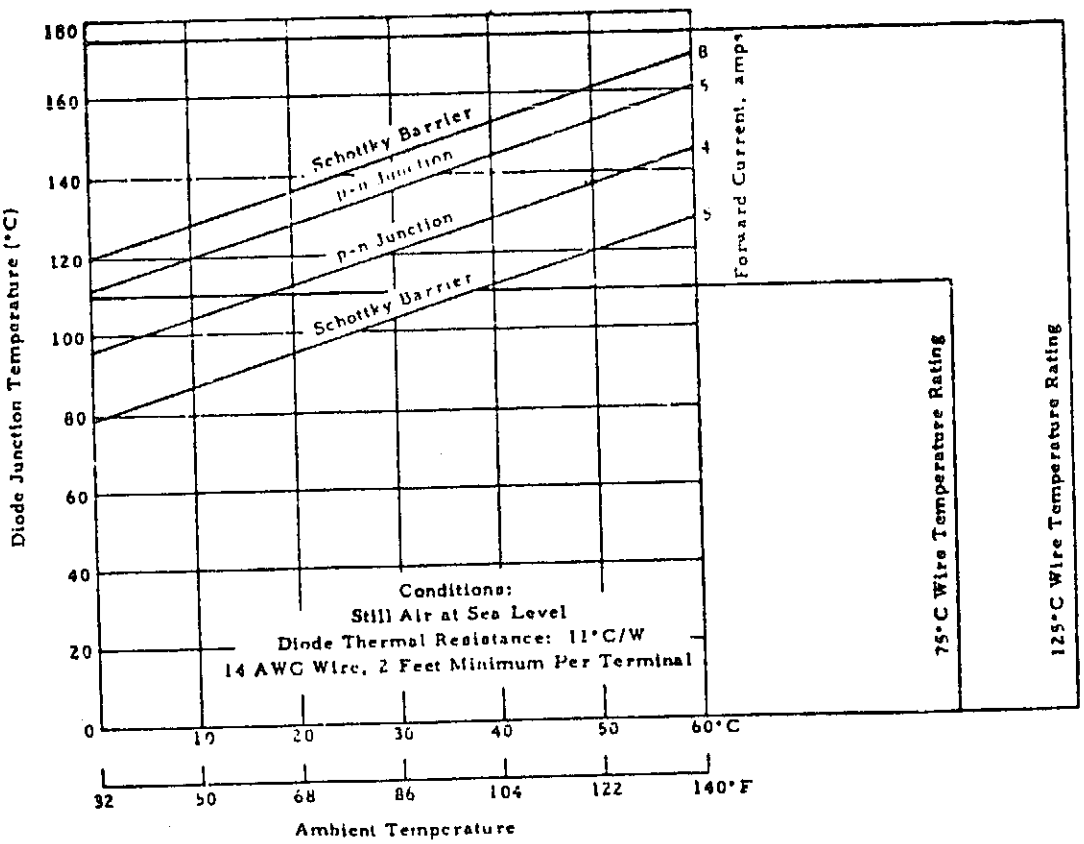
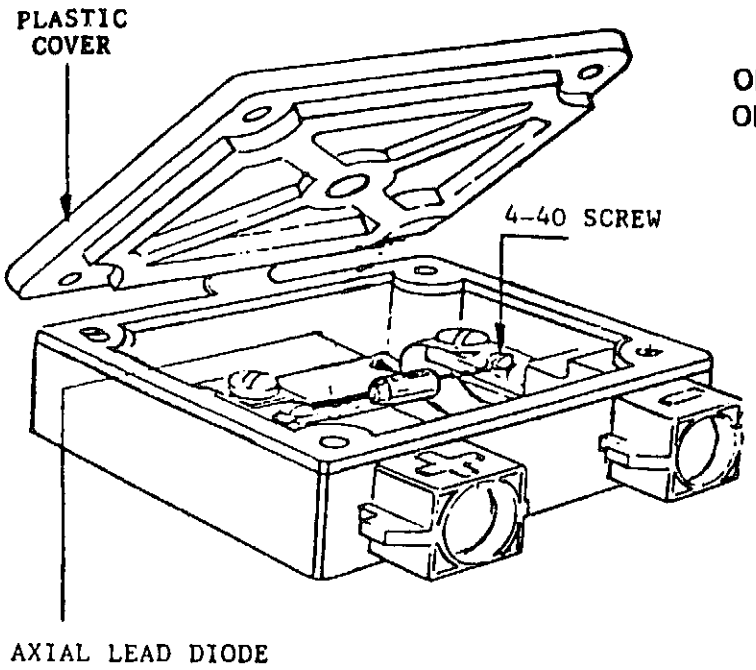


Figure 3-29. AMP, Inc. Axial Lead Diode Connector



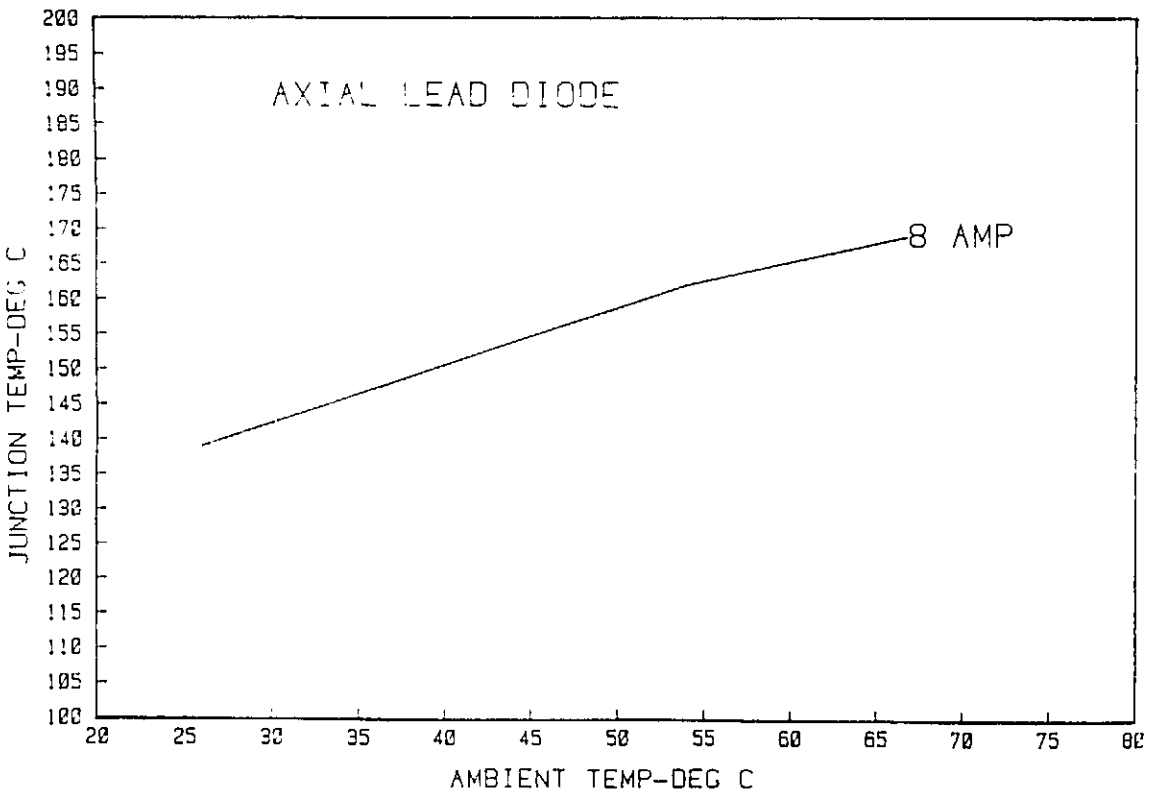
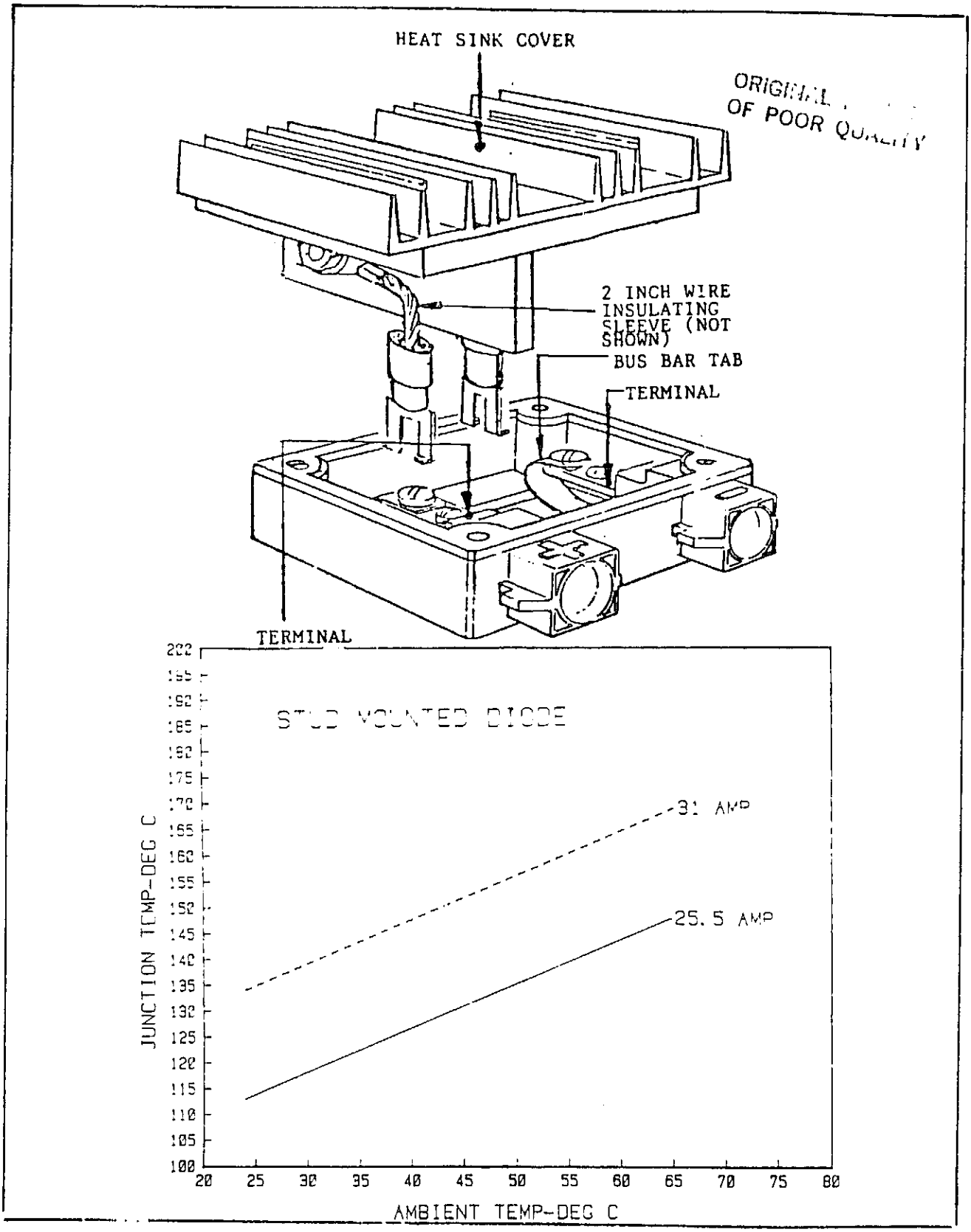


Figure 3-30. AMP, Inc. Junction Box with Plastic Cover



.gure 3-31. AMP, Inc. Junction Box with Heat Sink Cover

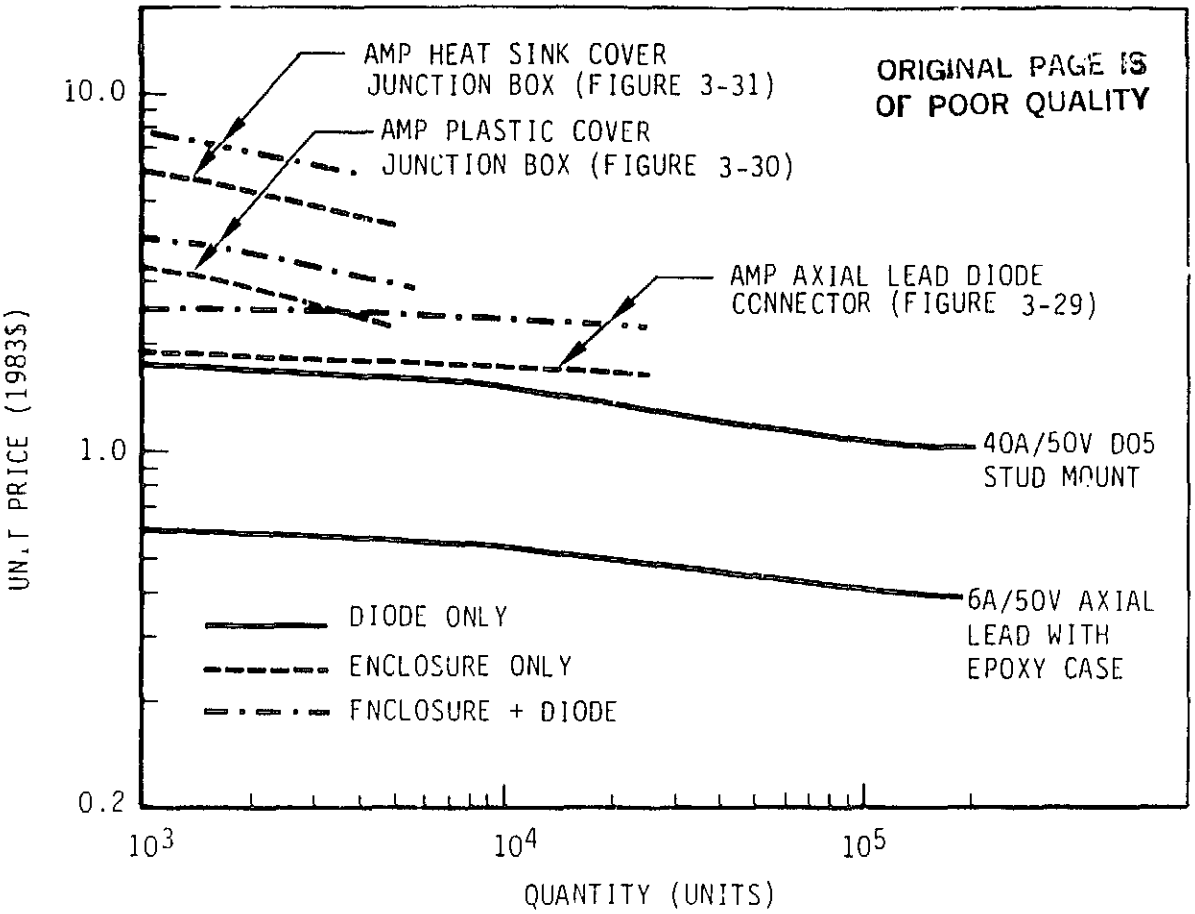


Figure 3-32. Selling Price for Packaged Diodes and Diode Enclosures

Table 3-28. Selling Price (1983 $) of Packaged Diodes in AMP, Inc. Plastic Enclosures

Quantity	Forward Current Capability (Amperes)/Configuration		
	6/In-Line Housing	8/J.B. with Plastic Cover	30/J.B. with Heat Sink Cover
1000	2.50	3.90	7.80
5000	2.35	2.95	5.70
20000	2.15	--	--

3.7.3 COST COMPARISON

Table 3-29 compares the estimated cost per unit of module area .. the two bypass diode integration approaches described above. This comparison assumes that the cost of mounting the plastic enclosure on the module frame or rear surface is included as part of the other module assembly costs and is equal to the cost of positioning and connecting the encapsulated diode/heat spreader assembly within the module laminate. It is important to note that the AMP Inc. plastic enclosure costs do not include the cost of mounting the packaged diode within the enclosure. The footnote to Table 3-29 establishes the cost impact per minute of installation labor. At the 6 ampere bypass current rating level, an examination of these comparative prices would indicate that it might be better to select the AMP Inc. axial lead diode connector (Figure 3-29), but the user should first establish that the installation of the axial lead diode can be accomplished in less than 2.22 minutes per unit $\left\{=\frac{14.25-9.00}{2.36}\right\}$. This installation procedure should include the following steps:

- Removal of cover
- Check diode for continuity and polarity
- Install diode including cutting leads to length and tightening screw terminals
- Replacement of cover

It is apparent from these data that the AMP Inc. plastic covered junction box is not cost effective as a bypass diode enclosure since its power dissipation capability is only slightly better than the axial lead diode connector which has considerably lower weight and size.

Again, at the higher rated current levels, the plastic junction box with the heat sink cover would appear to have a cost advantage over the encapsulated diode approach but the issue is equally clouded by the unaccounted for installation cost of the stud mounted diode. The exposed metal heat sink also creates another installation cost penalty since it introduces the requirement for the attachment of a separate grounding wire.

Table 3-29. Price Comparison Between Bypass Diode Integration Approaches (1983 $/m^2 of module area)

Bypass Diode Integration Approach / Bypass Current Rating (Amp) / Annual Production Rate (m^2 of module area)	Encapsulated Within Module			AMP Inc. Plastic Enclosures **		
	6	12	18	6	8	30
1,000	14.25	9.96	9.06	9.00	9.14	6.20
10,000	10.09	7.37	7.13	7.69	*	3.90
50,000	7.43	5.08	4.96	*	*	*

* No data available

** Does not include the cost of mounting the diode within the enclosure. Using the same methodology applied to the encapsulated diode costing analysis, these prices per m^2 would be increased by the following amounts for each minute of labor required to install a single diode.

Current Rating (Amperes)	Price Increase per Minute of Installation Labor per Diode (1983 $/$m^2$)
6	2.36
8	1.77
30	0.47

Thus, from a cost standpoint there is no obvious advantage for one approach over another. If a junction box is required to accommodate module-to-module interconnecting wiring, it would seem reasonable to include the diode within this enclosure if only one bypass diode is required for the module. If the module electrical design requires multiple bypass diodes or, if a frameless module with non-conductive exposed surface is contemplated, it would seem reasonable to consider the encapsulated diode implementation.

3.8 PARALLEL BYPASS DIODE LOAD SHARING CONSIDERATIONS

3.8.1 PROBLEM STATEMENT

The current sharing among bypass diodes within parallel-connected photovoltaic modules is the subject of this task activity. When identical modules, each containing a bypass diode, are connected in parallel, as illustrated in Figure 3-33, the circuit current is shared among the individual modules. In the normal power generation operating mode each solar cell circuit element will contribute to the total circuit current in accordance with the individual module I-V characteristics so that a common voltage is developed across the parallel-connected group. When circuit operating conditions dictate a reverse voltage bias across a parallel-connected group of modules the individual module bypass diodes will conduct current in the forward direction. This total circuit bypass current will be divided among the individual module diodes in accordance with the forward conducting current-voltage characteristic of each diode so that a common voltage drop is developed across the parallel-connected group. This condition of forward conducting current sharing is illustrated in Figure 3-34 for two parallel bypass diodes, D1 and D2. If these two diodes have identical forward current-voltage characteristics, the total circuit bypass current, I_T, will be divided equally between the two diodes. However, in reality these characteristics will not be identical due to inherent manufacturing tolerance and differences in the operating junction temperature of the two diodes. This imbalance in forward characteristics will result in an unequal division of bypass current between the two parallel paths. This unequal current sharing may cause a diode overtemperature condition due to the fact that the individual bypass diodes are sized to dissipate only the power associated with conducting the module rated short-circuit current. The concern also exists that an initial small

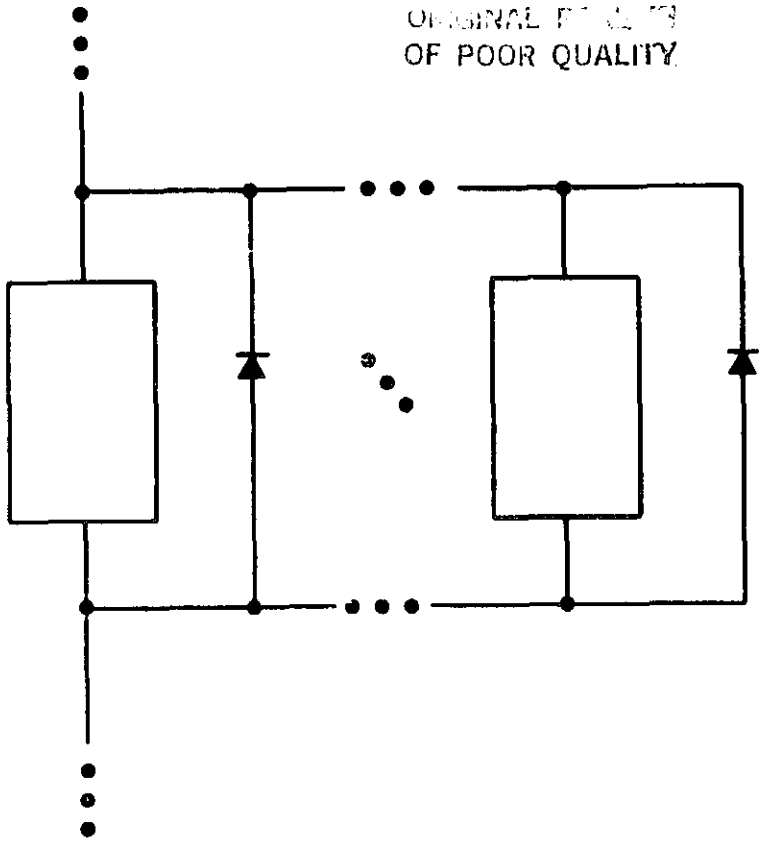


Figure 3-33. Parallel Interconnection of Photovoltaic Modules Containing Individual Bypass Diodes

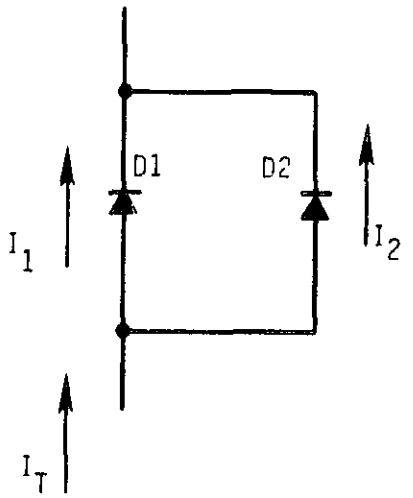


Figure 3-34. Definition of Current Sharing Between a Pair of Parallel Bypass Diodes

imbalance may lead to catastrophic thermal runaway condition where the increased current leads to increased diode junction temperature resulting in still more current imbalance until diode failure results from an over-temperature condition.

The current sharing among parallel diodes of the same type can be equalized by the inclusion of a small series resistance in each bypass path. In addition it is possible to shunt the total bypass current through a single externally-mounted bypass diode which is sized by the array circuit designer to accommodate the entire string short-circuit current.

3.8.2 CIRCUIT ANALYSIS

3.8.2.1 Modelling of Diode Characteristics

As the first step in the circuit analysis of parallel-connected bypass diodes, it is necessary to develop an algebraic expression representing the forward current voltage characteristics of each diode type to be considered. Figure 3-35 shows such a set of temperature-dependent characteristics for a PN junction diode of the type which might be used in a photovoltaic module bypass application. The forward voltage drop (V_f) across this diode can be modelled as a function of forward current (I_f) and junction temperature (T_j) by the following expression:

$$V_f = 0.733635-0.0016945T_j + (0.137915+0.0003367T_j)\log I_f + (0.03641+5.9388\times10^{-5}T_j-4.6085\times10^{-7}T_j^2)(\log I_f)^2$$

which accurately represents these data over the range $0.1 < I_f < 20$ Amperes and $-50 < T_j < 175^{o}C$.

A similar set of characteristics for a typical Schottky diode is given in Figure 3-36. The nature of the variation of these characteristics with temperature is not amenable to a simple expression of the type given above for the PN junction diode, but it is possible to fit these empirical data to a third order polynomial of the form:

$$V_f = A+B\log I_f+C(\log I_f)^2+D(\log I_f)^3$$

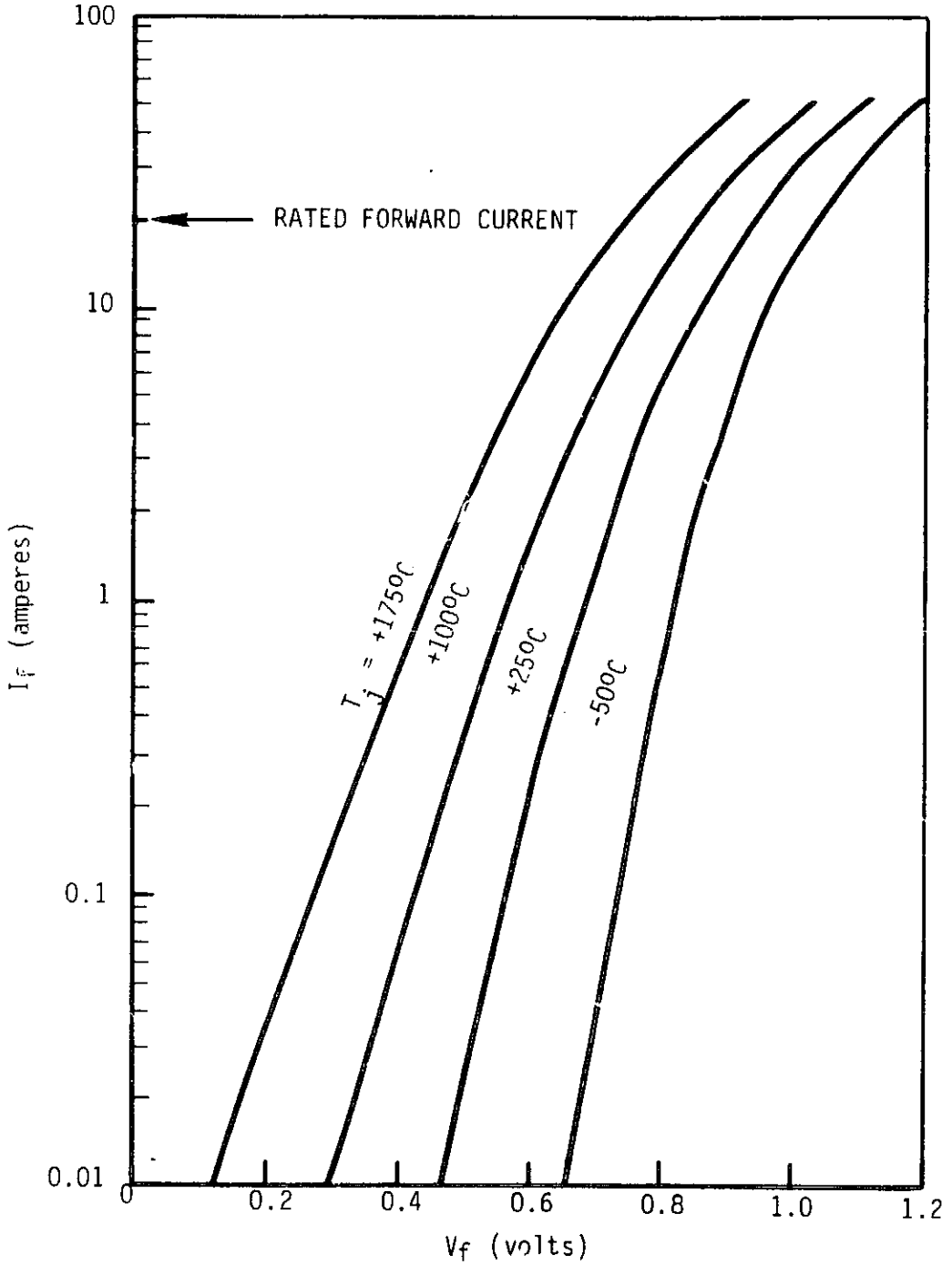


Figure 3-35. Forward Current-Voltage Characteristic for a Typical PN Junction Diode

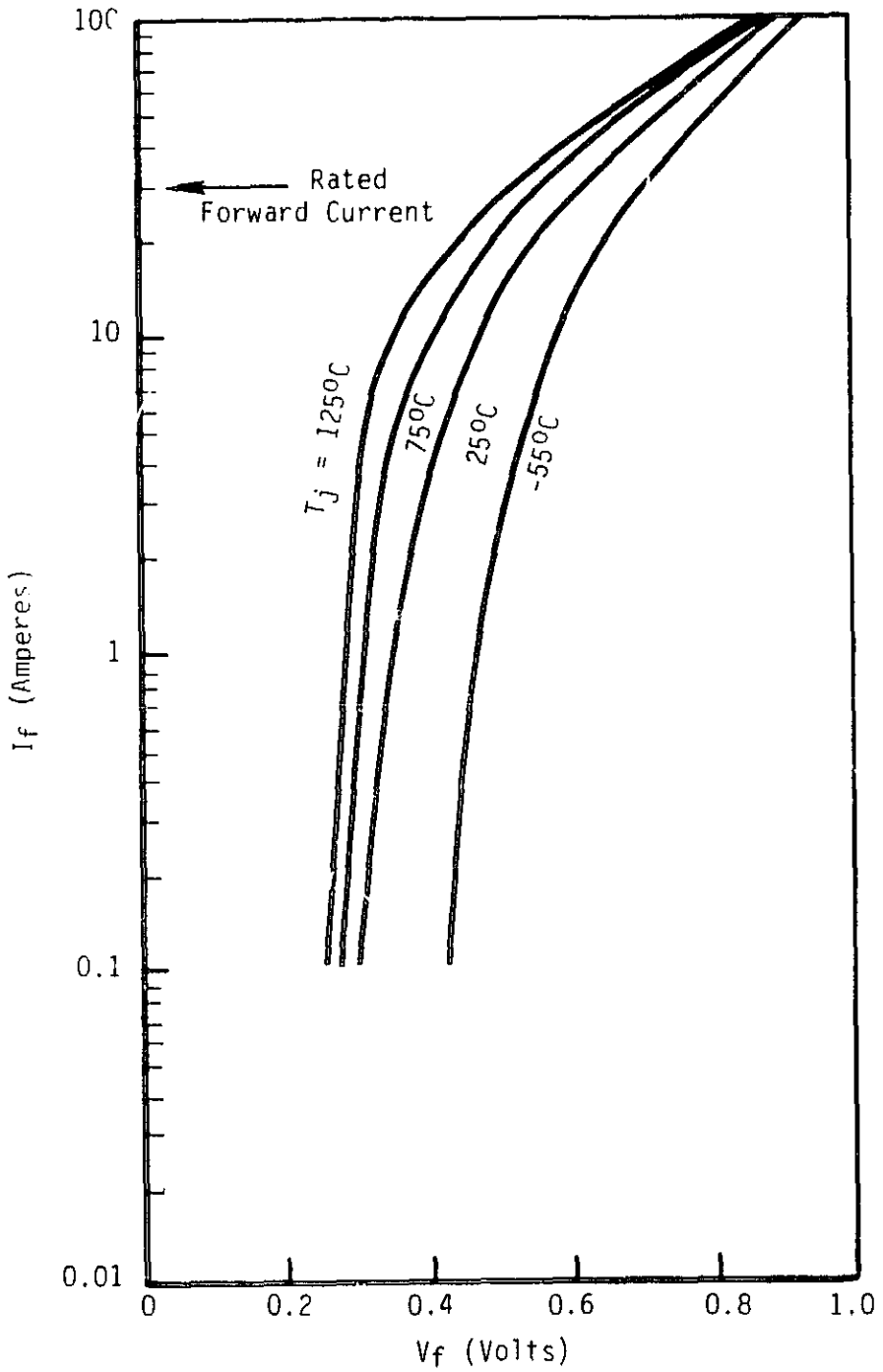


Figure 3-36. Forward Current-Voltage Characteristic for a Typical Schottky Junction Diode

where the values of the coefficients are as given in Table 3-30 for the four junction temperatures. When used in this expression, these coefficients will produce close agreement with the empirical data over the range $0.1 < I_f < 20$ amperes.

Table 3-30. Curve Fitting Coefficients for the Schottky Diode

Junction Temperature ^{o}C	A	B	C	D
-55	0.47728	0.058772	0.027137	0.026379
25	0.3548	0.064366	0.036993	0.029740
75	0.30886	0.016061	0.032102	0.04941
125	0.28276	0.011542	0.029399	0.04419

3.8.2.2 Parallel-Connected Diodes of the Same Type

The results of a circuit analysis of two parallel-connected P/N junction diodes is shown in Figure 3-37 where the ratio of the current flow in each diode is plotted as a function of total bypass current, I_t, for various values of the junction temperature of diode number 2 considering the junction temperature of diode number 1 to be constant at $50^{o}C$. This temperature difference forces a shift in the current-voltage characteristics of the two diodes, as illustrated in Figure 3-38, with the higher temperature diode having a greater current flow at a given forward voltage drop. The two operating conditions shown on Figure 3-38 (points a and b) have been reflected as the corresponding points on Figure 3-37 to illustrate the relationship between the actual operating points on the forward current-voltage characteristics and the results of the circuit analysis. It should be noted that, in this analysis, temperature has been used as the mechanism to force a difference between the two diode characteristics, but differences of this magnitude can also result from the normal variation among individual diodes of the same type and supplier.

Figure 3-37 shows that a significant current imbalance can result as the junction temperature difference is increased. At a total bypass current of

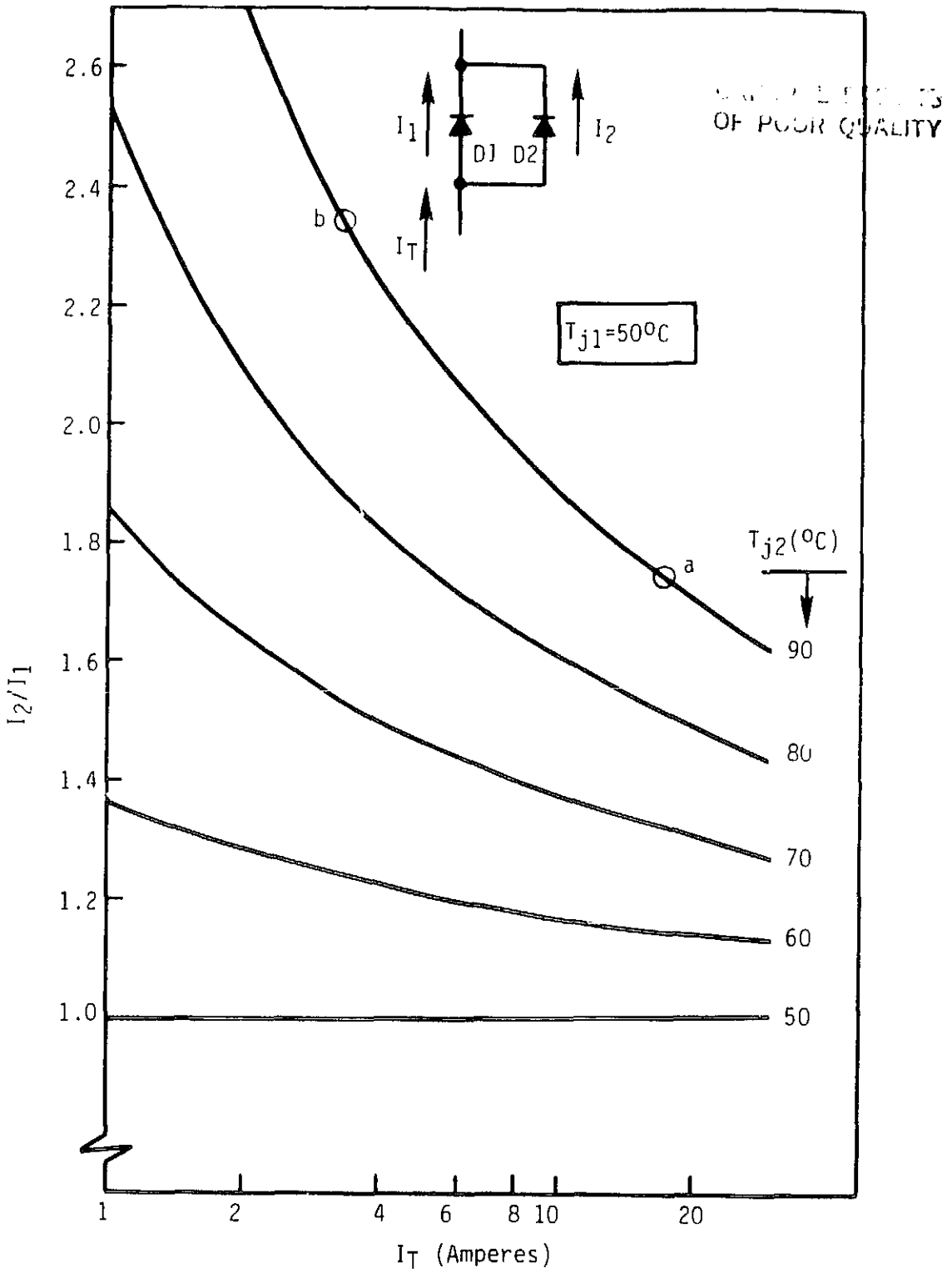


Figure 3-37. Current Sharing Between a Pair of PN Junction Bypass Diodes

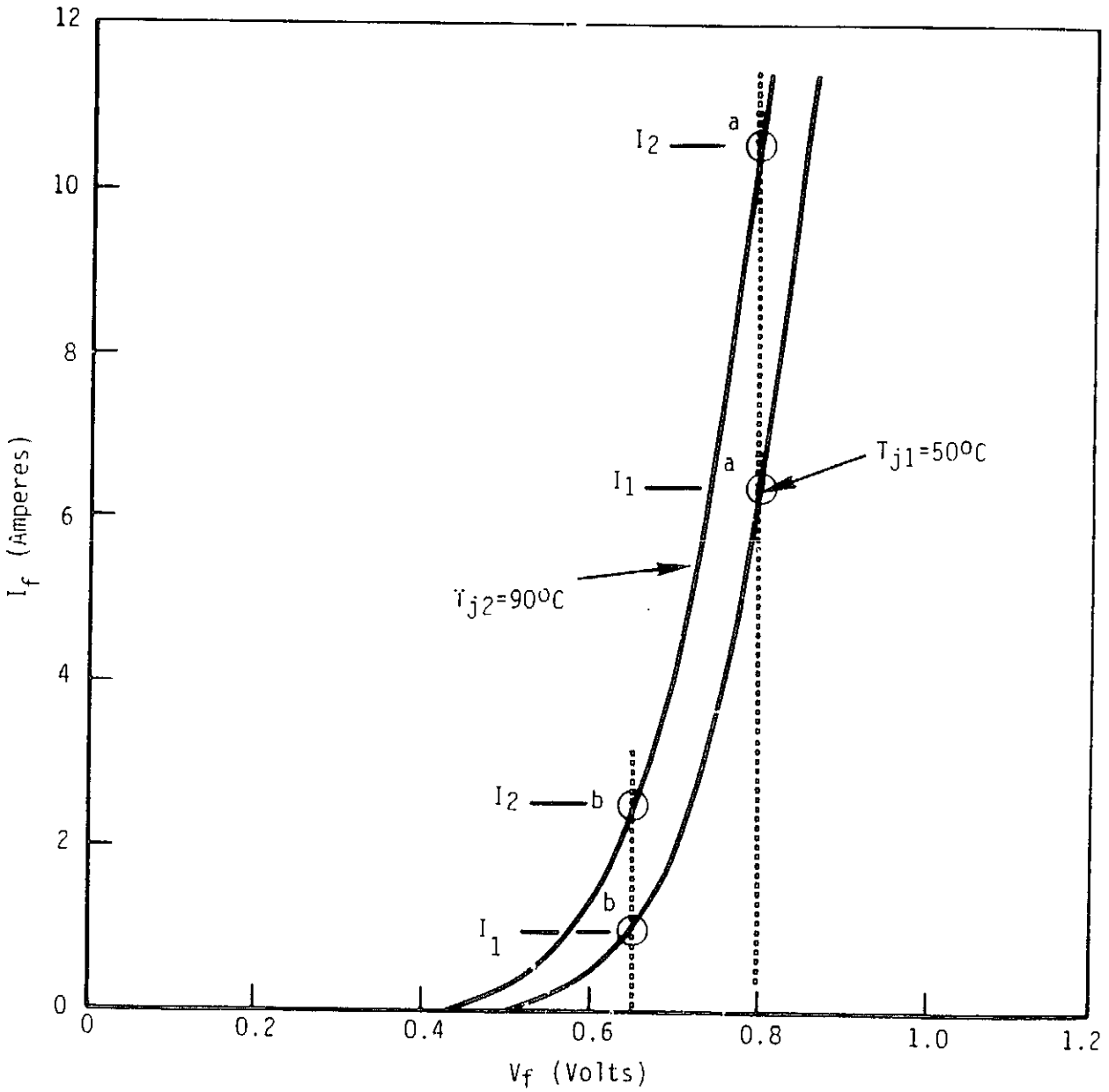


Figure 3-38. Illustration of Current Sharing with Differing Diode Junction Temperatures

30 amperes, the $40^{o}C$ junction temperature difference will result in a current split of 11.46 amperes in diode No. 1 and 18.54 ampere in diode No. 2. If the 30 amperes represents the total rated short-circuit current of the branch circuit and if each individual module bypass diode has been designed to accommodate only the short-circuit current of the module, this diode temperature difference, however derived, will result in 3.54 amperes of excess current in diode No. 2. If this temperature difference was to occur near the upper limit of the allowable junction temperature range, such a current overload could cause this limit to be exceeded.

The addition of a series resistance in each bypass path will reduce the current mismatch as shown in Figure 3-39, where the R=0 curve represents the $T_{j2}=90^{o}C$ curve from Figure 3-37. At 20 amperes of total bypass current, the addition of 0.05 ohms in series with each diode will change the current split from $I_1=7.40/I_2=12.60$ amperes to $I_1=9.55/I_2=10.45$ amperes. The influence of this series resistance is shown graphically in Figure 3-40, where the voltage drop across the series resistance at a given forward current value has been added to the diode voltage drop to obtain the total bypass path potential difference represented by the two dashed curves. Thus, it is apparent from the two operating conditions shown (c and d) that the current mismatch between the parallel paths has been significantly reduced by the change in the slope of the forward conducting characteristic caused by the series resistance. The penalty for this improvement in current sharing is increased total circuit voltage drop and associated power dissipation under forward conducting bypass conditions. The consequences of this increased total voltage drop must be carefully evaluated with respect to the array circut design if there are normal array operating conditions which require multiple bypass diodes within a single branch circuit to conduct at the same time. Under such conditions the increased voltage drop associated with the bypass series resistance may cause a disproportionately large decrease in the output contribution from the affected branch circuit.

Table 3-31 summarizes the power dissipation by component in each of the bypass paths as a function of total current and series resistance value. These data can be used to address the question of whether thermal runaway is possible under any of the conditions considered in this analysis. For a 20 ampere total bypass current, Table 3-31 shows that the diode dissipations of

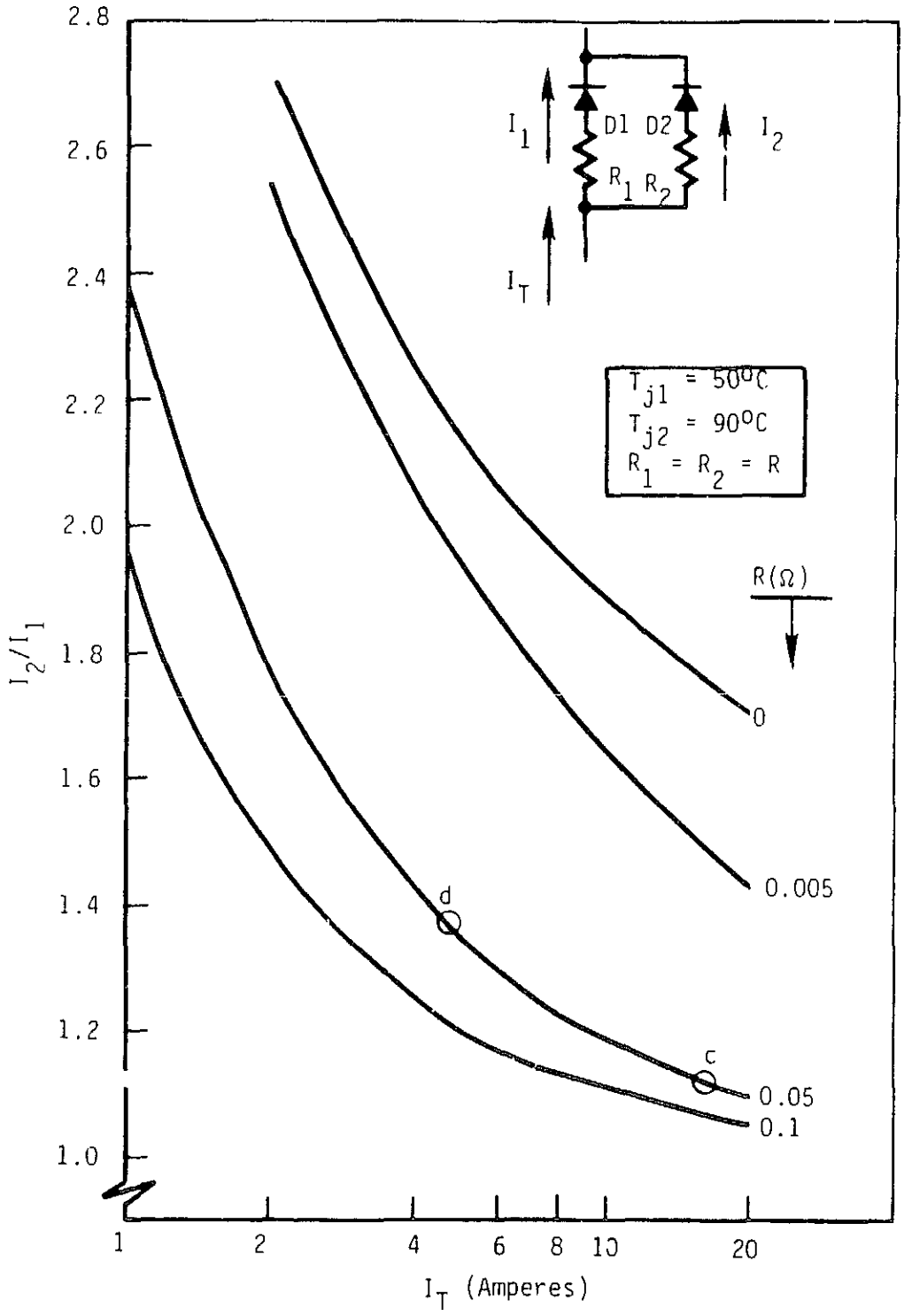
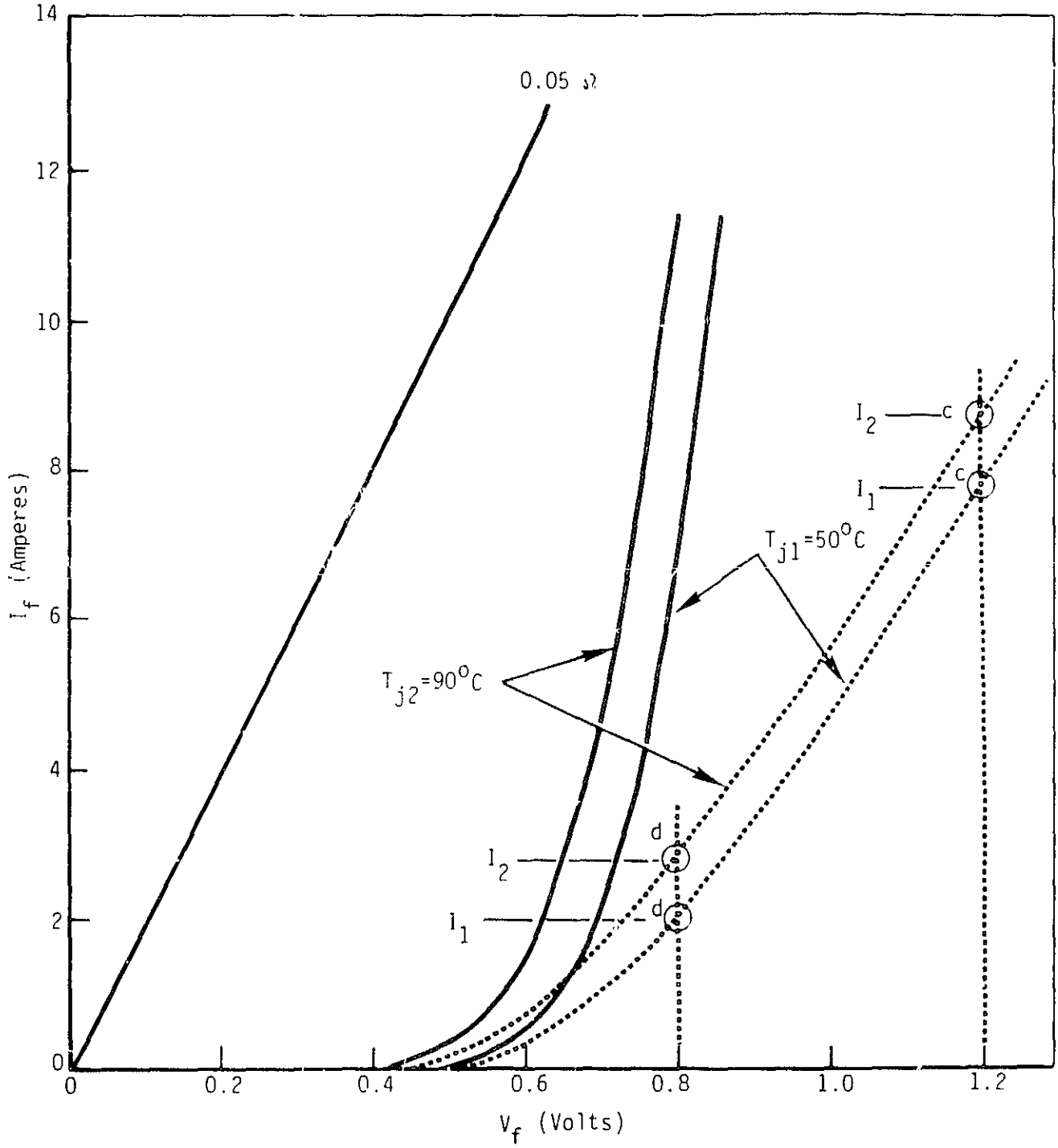


Figure 3-39. Current Sharing Between a Pair of PN Junction Bypass Diodes with Series Resistance in the Bypass Paths



Figur 3-40. Illustration of Current Sharing with Series Resistance in the Bypass Paths

Table 3-31. Summary of Bypass Circuit Power Dissipation*

I_T (Amp)	I_1 (Amp)	I_2 (Amp)	R (ohms)	Power Dissipation by Component (watts)				Total Bypass Circuit Power Dissipation (watts)
				D1	R_1	D2	R_2	
20.	7.40	12.6[illegible]	0	6.01	0	10.23	0	16.24
	8.23	11.77	0.005	6.77	0.34	9.48	0.69	17.28
	9.55	10.45	0.05	8.00	4.56	8.28	5.46	26.30
	9.75	10.25	0.1	8.19	9.51	8.10	10.51	36.31
10.	3.47	6.53	0	2.58	0	4.86	0	7.44
	3.78	6.22	0.005	2.84	0.07	4.60	0.19	7.70
	4.57	5.43	0.05	3.5[illegible]	1.04	3.93	1.47	9.95
	4.75	5.25	0.1	3.67	2.26	3.79	2.76	12.48
5.	1.59	3.41	0	1.08	0	2.33	0	3.41
	1.70	3.30	0.005	1.17	0.014	2.24	0.054	3.48
	2.13	2.87	0.05	1.50	0.226	1.92	0.413	4.06
	2.27	2.73	0.1	1.61	0.513	1.81	0 747	4.68
2.	0.54	1.46	0	0.328	0	0.892	0	1.220
	0.57	1 43	0.005	0.349	0.0016	0.871	0.0102	1.232
	0.72	1.28	0.05	0.452	0.0259	0.768	0.0819	1.328
	0.80	1.20	0.1	0.509	0.0642	0.714	0.1438	1.431
1.	0.219	0.781	0	0.124	0	0.440	0	0.564
	0.228	0.772	0.005	0.129	0.0003	0.435	0.0030	0.567
	0.293	0.707	0.05	0.168	0.0043	0.394	0.0250	0.592
	0.338	0.662	0.1	0.197	0.0114	0.365	0.0438	0.617

* $T_{j1} = 50^{o}C$ and $T_{j2} = 90^{o}C$

6.01 and 10.23 watts can be expected for diodes Nos. 1 and 2, respectively, which are operating with a 40°C temperature difference. When this is compared to the thermal resistance characteristics of two typical bypass diode mounting approaches, as shown in Figure 3-41, it is apparent that these mounting designs will not allow this temperature difference to be developed with 4.22 watts of increased dissipation. Thus, there is no possibility of a thermal runaway if the PN junction diodes are adequately packaged and mounted.

3.8.2.3 Parallel-Connected Diodes of Different Types

In the previous section it was shown that a small resistance in series with each bypass diode could significantly improve the current sharing among individual module bypass diodes of the same type in a parallel-connected group. The additional voltage drop associated with this series resistance when the bypass diodes are required to conduct the circuit current during periods of anomalous module operation due to shadowing or permanent circuit degradation must be carefully evaluated to determine the loss in circuit power generation capability at the system operating voltage.

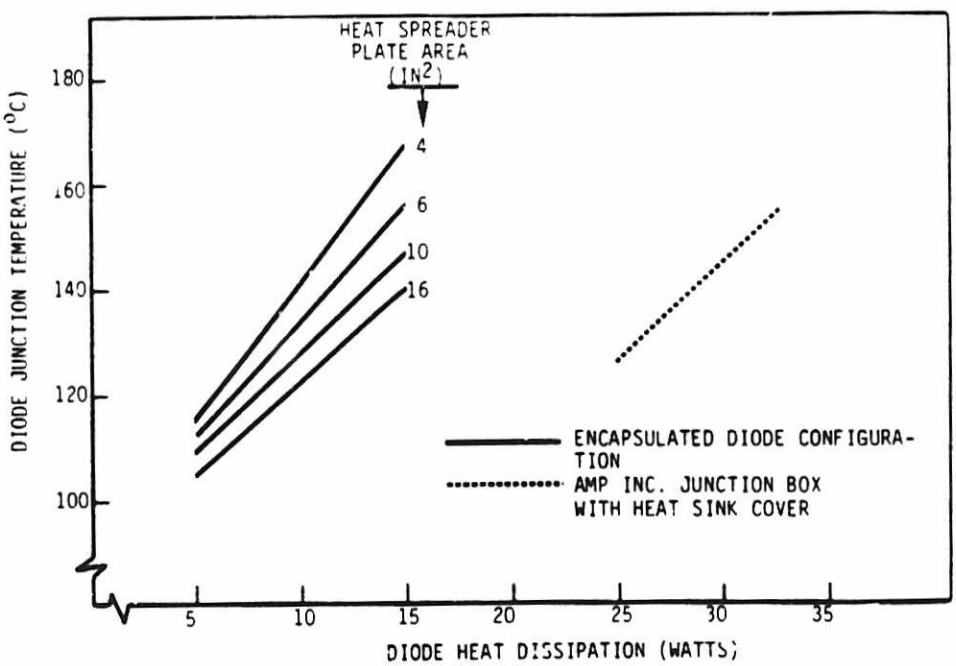


Figure 3-41. The Thermal Resistance of Two Types of Bypass Diode Installations

C-2

Another method for limiting the overcurrent condition in an individual module bypass diode, which does not contribute to an increased voltage drop in the affected circuit, involves the use of an externally-mounted diode as illustrated in Figure 3-42. The external diode must be sized to carry the entire circuit short-circuit current at a voltage drop which is significantly less than that possible through the parallel internal bypass paths. If the internal bypass diodes are PN junction devices, arranged as one series-connected diode per module, then the use of an external Schottky device, with its lower voltage drop at a specified current, will assure the preferrential flow of bypass current through the external circuit. The results of a circuit analysis of this condition are summarized in Figure 3-43, where the current ratio is plotted as a function of both the junction temperature of the PN diode and the resistance in the Schottky diode path.

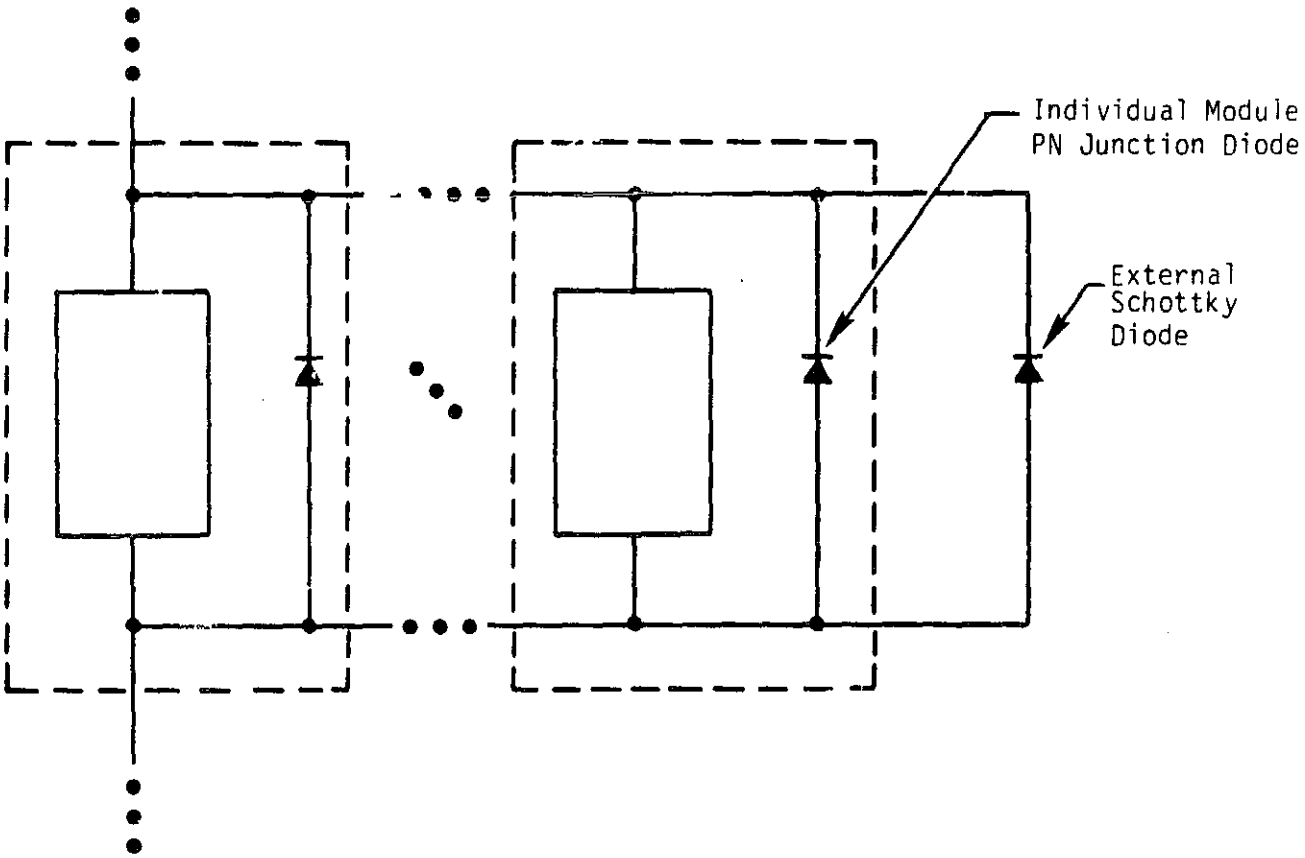


Figure 3-42. Parallel Interconnection of Photovoltaic Modules Containing Individual Bypass Diodes with an External Diode

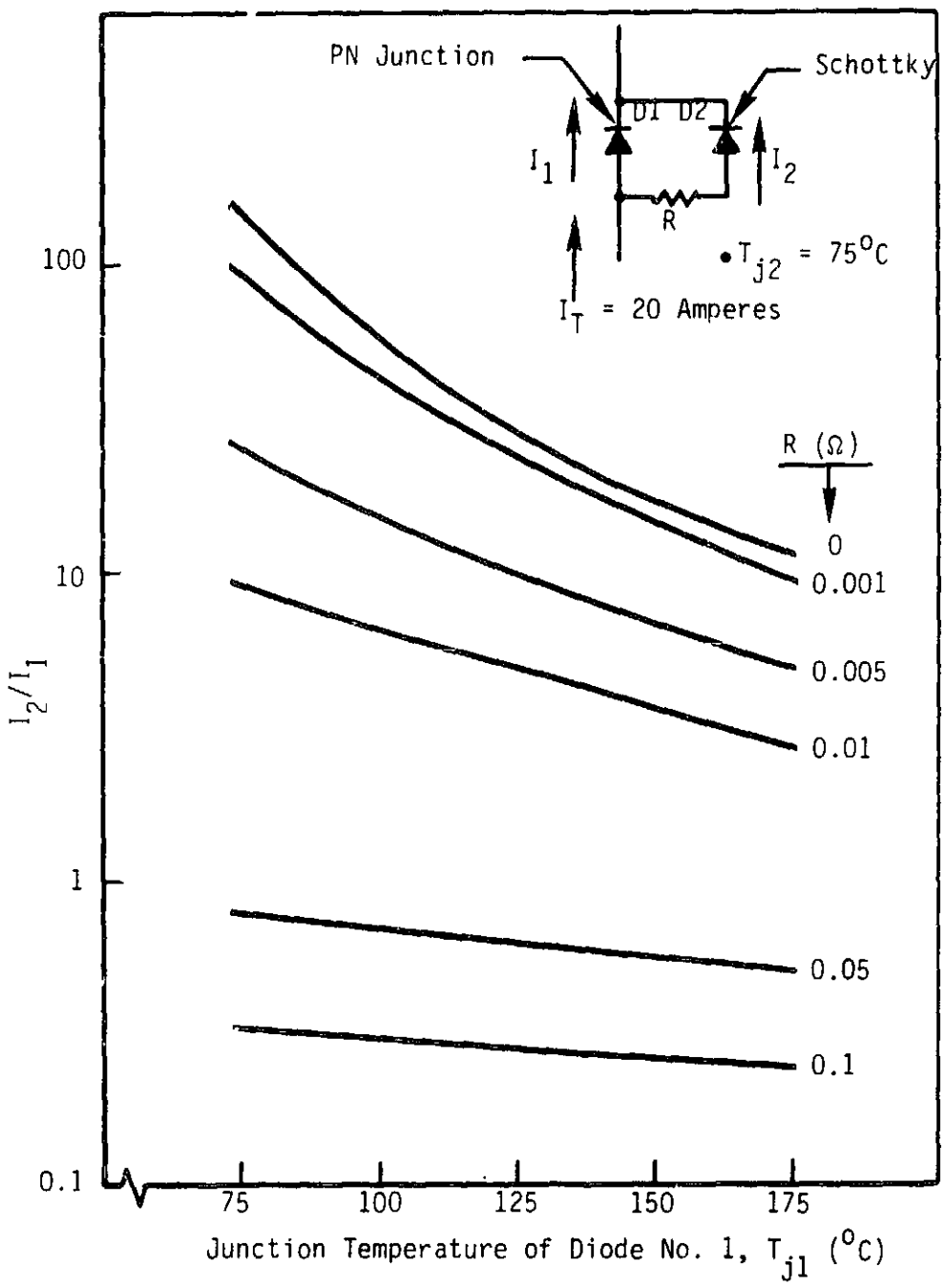


Figure 3-43. Current Sharing Between Parallel PN Junction and Schottky Diodes

This analysis has been performed for a total bypass current of 20 amperes and with the junction temperature of the Schottky diode fixed at 75°C. With no resistance in the Schottky diode path and with equal diode junction temperatures, Figure 3-43 shows that the Schottky diode will carry 160 times more current than the PN junction device. The magnitude of this current difference will decrease somewhat as the junction temperature of the PN diode is increased relative to the Schottky device. With a 100°C junction temperature difference, the Schottky will still carry over 12 times more current than the PN diode. The introduction of series resistance in the Schottky diode path will have a significant effect on this current split.

The addition of 0.01 ohms in series with the Schottky diode (equivalent to 6 feet of the AWG 12 solid copper wire at 25°C) will cause the current in the Schottky to decrease from 160 to 9 times the current in the PN device for the case of a 75°C junction temperature in both diodes. This sensitivity to series resistance in the Schottky diode path must be carefully evaluated as part of the array circuit design if this method of bypass diode protection is to be employed.

3.9 BYPASS DIODE RELIABILITY CONSIDERATIONS

3.9.1 PROBLEM STATEMENT

The reliability of a diode used in a bypass application within a photovoltaic module can be defined as its ability to continue to perform its intended design function under the electrical loading conditions and environmental influences. The failure of a diode used in this application could manifest itself as one or more of the following anomalous conditions:

1. A short-circuit resulting in the loss of the power generated by the cells within the bypassed group and a reduction of the branch circuit voltage which is proportional to the number of series-connected cells within the bypassed group;
2. An open-circuit diode failure resulting in the elimination of the bypass function which could lead to increased solar cell "hot-spot" heating under shadowing or other circuit failure conditions;

3. An increase in the reverse leakage current resulting in an increase in the shunt power loss during normal solar cell circuit operation; or
4. An increase in forward voltage drop at a given current level and temperature which results in increased bypass diode power dissipation under solar cell circuit shadowing or failure conditions.

The first of these possible anomalous conditions is of the most concern since it has an immediate and lasting effect on the circuit output power.

3.9.2 BYPASS DIODE OPERATING CONDITIONS

A photovoltaic module bypass diode operates in a manner which is characterized by the following conditions:

a. Prolonged operation with the periodic application of a relatively low reverse voltage. This reverse voltage will generally be less than 15 vdc and will be applied as 12 hours "ON" followed by 12 hours "OFF". Since there will be negligible diode power dissipation during this period the diode temperature will approximate the solar cell temperature. This temperature will approach the ambient temperature during nighttime or "OFF" periods and will be elevated above the ambient temperature during daylight periods by an amount which varies with the solar intensity and wind speed and direction.

b. Occasional operation in a forward current conduction mode at a current which will vary with the insolation level and circuit loading conditions. As a minimum this forward conduction mode can be assumed to be that associated with the "hot-spot" endurance exposure as defined in UL 1703, "Proposed Standard for Safety - Flat-Plate Photovoltaic Modules and Panels." In this procedure representative cells within the module or panel are subjected to simulated reverse voltage hot-spot heating conditions for a total of 100 hours. If such a module were to contain a bypass diode, the diode would be forward conducting during periods of cell reverse voltage heating resulting in a localized diode heat dissipation.

Thus, for the purposes of establishing a representative bypass diode operating profile over a 20 year array design lifetime, it might be reasonable to include both of these conditions through the formulation of a two part profile with the following features:

1. Reverse voltage operation for 87500 hours at 15 vdc with an annual average bypass diode temperature (T_D) as given by:

$$T_D = mS+T$$

where

S = annual average insolation intensity (kW/m^2)

T = daylight average ambient temperature (^oC)

m = an empirically determined coefficient. A value of 40 is typical of a roof-mounted module installation

The annual average reverse bias bypass diode temperature calculated from this relationship is listed in Table 3-32 for the 26 SOLMET TMY site locations.

2. Operation in the forward conducting mode for 100 hours at a current corresponding to the solar cell circuit short-circuit current at 100 mW/cm^2 AM 1.5 illumination and at the NOCT. The diode temperature shall be calculated at this dissipate condition with an assumed background temperature equal to the NOCT.

3.9.3 RECTIFYING DIODE RELIABILITY

The factors influencing the reliability of discrete semiconductor devices are addressed by Herr, et al., of the General Electric Company in Reference [8]. The usual failure pattern for such components is the familiar "bathtub" curve shown in Figure 3-44. The first portion of this curve is characterized by a sharply increasing and then a steadily decreasing failure rate during the burn-in portion of device life. After this initial burn-in period, where the failures can be attributed to workmanship faults not detected during the manufacturing process, a period of relatively constant failure rate can be expected. The final portion of

8. E.A. Herr, et. al., "Reliability Evaluation and Prediction for Discrete Semiconductors", IEEE Transactions on Reliability, August 1980, Volume R-29 Number 3-Catalogue No. ISSN0018-9529.

Table 3-32. Formulation of the Annual Average Reverse Bias Bypass Diode Temperature

SOLMET Site	Annual Total Latitude Tilt Insolation (kWh/m^2)	Annual Average Insolation Intensity (kW/m^2)	Annual Daylight Average Ambient Temperature (^oC)	Annual Average Reverse Bias Bypass Diode Temperature (^oC)
Albuquerque, NM	2401	0.521	15.6	36.4
Apalachicola, FL	1866	0.399	22.4	38.4
Bismarck, ND	1707	0.374	6.8	21.8
Boston, MA	1421	0.314	11.4	24.0
Brownsville, TX	1868	0.406	25.4	41.6
Cape Hatteras, NC	1747	0.382	18.3	33.6
Caribou, ME	1418	0.310	5.2	17.6
Charleston, SC	1690	0.388	19.8	35.3
Columbia, MD	2058	0.449	14.1	32.1
Dodge City, KS	2055	0.443	14.6	32.3
El Paso, TX	2434	0.536	20.2	41.6
Ely, NV	2230	0.481	9.1	28.3
Fort Worth, TX	1877	0.409	20.7	37.1
Fresno, CA	2169	0.475	18.9	37.9
Great Falls, MT	1715	0.376	8.8	23.8
Lake Charles, LA	1652	0.362	21.4	35.9
Madison, WI	1554	0.345	8.7	22.5
Medford, OR	1699	0.367	13.5	28.2
Miami, FL	1802	0.394	26.3	42.1
Nashville, TN	1589	0.356	16.8	31.0
New York, NY	1402	0.318	13.8	26.5
Omaha, NB	1767	0.385	12.6	28.0
Phoenix, AZ	2394	0.528	24.3	45.4
Santa Maria, CA	2039	0.444	16.1	33.9
Seattle, WA	1299	0.281	11.9	23.1
Washington, DC	1559	0.340	13.6	27.2

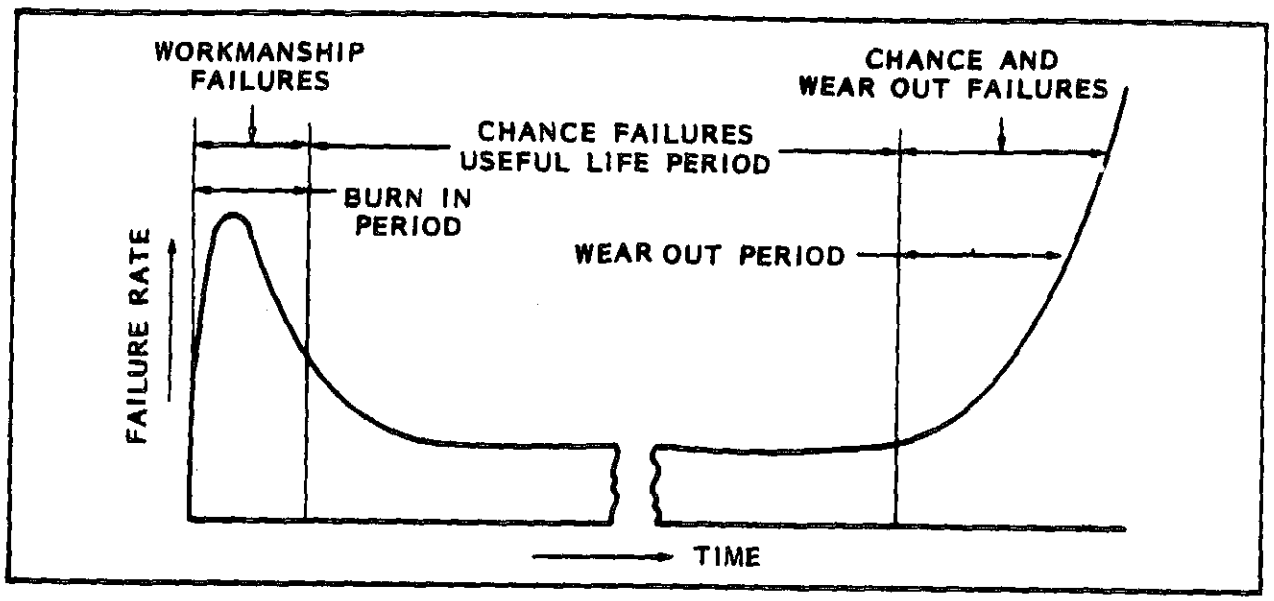


Figure 3-44. Semiconductor Failure Rate As a Function of Time

the failure rate profile is characterized by increasing device failures identified as a wear out phenomena. This portion is extremely difficult to define and will vary depending on the method of fabrication and the applied stress. This increasing failure rate can be introduced by such mechanisms as thermal fatigue of the solders between the silicon die and the mount (due to repeated cycling of junction temperature while the case is at a more or less fixed temperature), by fatigue of internal construction (due to mechanical stress), or by bulk defects. Little data are available from either life tests or system field tests to permit an accurate picture of this portion of the curve. In sharp contrast to the early life failures, that may be characterized as workmanship faults, the failures which occur in the wear out period are believed to be a result of basic design limitations.

Accelerated testing of the two types illustrated in Figure 3-45 is commonly used to evaluate early designs of new products and process changes and to acquire failure rate data. The first of these, called step stress testing, is usually used for exploring the capability of a device in a stress domain of increasing magnitude. The sample size is generally small and the time duration at each stress level is short. Consequently, the results of this testing are not useful in determining failure-in-time patterns because of

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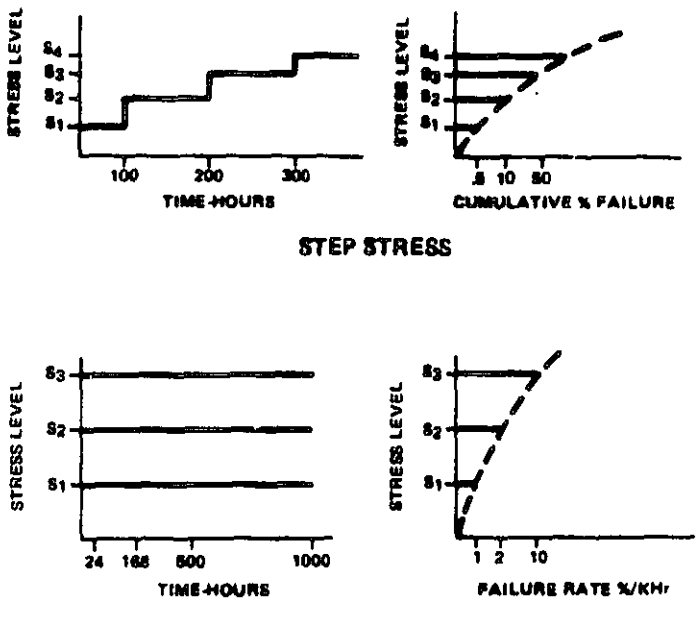

Figure 3-45. Accelerated Testing Options

the cumulative effect of the several levels of stress on the device performance. The stress-in-time tests, which is the second method illustrated in Figure 3-45, is more suited to this objective since device performance is evaluated at constant stress as a function of exposure time. Three levels of stress are commonly used with a sample size of from 20 to 100 or more devices. Each group of samples is subjected to each of the established stress levels for a duration of at least 1000 hours. This testing method can be used to obtain failure rate data which forms the basis for a plot of the type shown in Figure 3-46 for a typical rectifying diode. The predominant failure mechanisms found in semiconductor devices are related to junction temperature and fit the Arrhenius model as shown in the figure. It is important to note that the basis for this failure rate data is a rectifying application with a 60 Hz sinusoidal waveform. The criteria for failure are also consistent with this application and generally include a low threshold of leakage current (10 to 500 μA) at a specified reverse voltage as well as a small change in the forward voltage drop (10 to 100 mV) at a specified forward current.

The data represented by Figure 3-46 applies to the useful life portion of the failure rate curve, and, as such, assumes that the vast majority of the

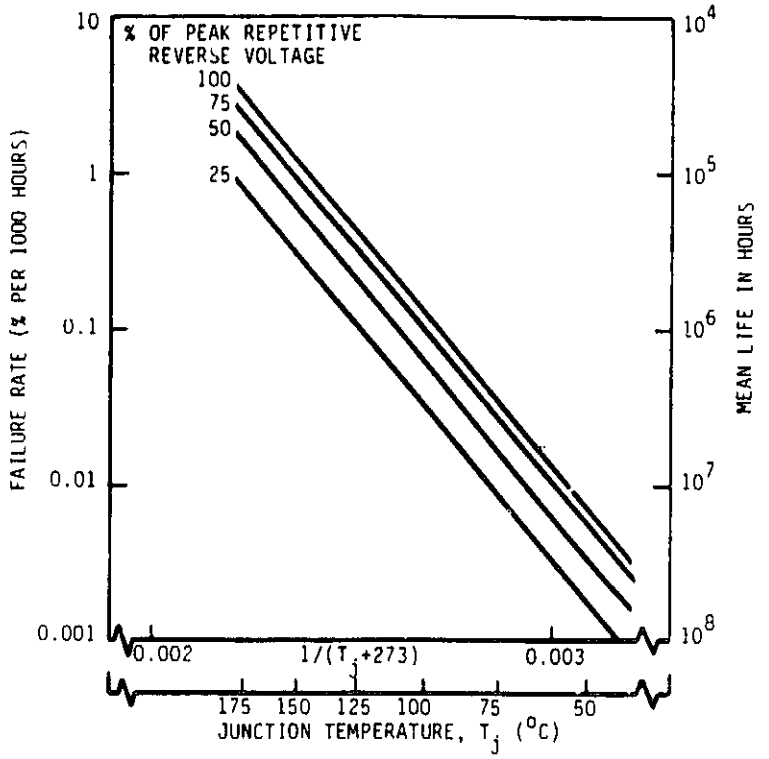

Figure 3-46. Failure Rate for a Typical Rectifying Diode

workmanship failures have been uncovered during a burn-in period. The failure rate during this burn-in period is significantly higher as illustrated by data supplied by Semicon Inc. on power rectifier numbers JANTX1N1184 and JANTX1N1204A. When these two diode types were subjected to the burn-in test as defined in MIL-S-19500 and illustrated in Figure 3-47, failure rates of 3.31 and 3.39 percent resulted for the 1N1184 and 1N1204A diodes, respectively. These burn-in failure rates are 11 and 6 times greater than the 175°C and 100 percent voltage point from Figure 3-46 for the two diode types, respectively.

MIL-HDBK-217D [9] establishes a uniform method for predicting the reliability of electronic equipment. This methodology represents the failure

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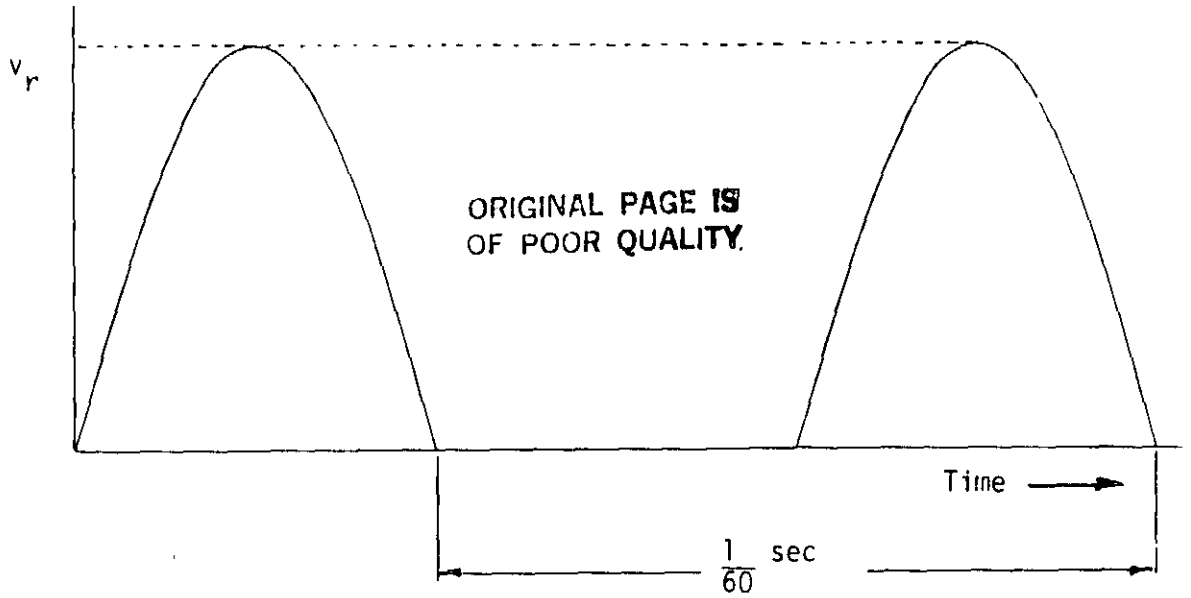
9. MIL-HDBK-217D, "Military Handbook - Reliability Prediction of Electronic Equipment," 15 January 1982.



V_r = 100 v (for 1N1184)
= 400 v (for 1N1204A)

Diode Case Temperature = 175°C

Test Duration = 96 hours (for 1N1184)
= 168 hours (for 1N1204A)

Failure Criteria

ΔI_R = 100 percent or 100 μAdc, whichever is greater (for 1N1184)

= 100 percent or 20 μAdc, whichever is greater (for 1N1204A)

ΔV_f = $\pm$ 0.1 v from the initial value

Figure 3-47. MIL-S-19500 TX-Type Diode Burn-in Test Definition

rates of discrete semiconductor devices by the relationship:

$$\lambda_p = \lambda_b \left(\Pi_E \times \Pi_A \times \Pi_Q \times \Pi_R \times \Pi_{S2} \times \Pi_C \right) \text{ failures}/10^6 \text{ Hours} \qquad \text{Eqn (1)}$$

where λ_b is a base failure rate and the other multiplying factors are application dependent modifiers as described in Table 3-33. General purpose silicon rectifying diodes, which are of interest for photovoltaic bypass applications, are identified as Group IV in accordance with this calculation procedure. The base failure rate for Group IV silicon diodes is given by:

$$\lambda_b = 0.172 \exp \left[\left(\frac{-2138}{273+T+150S} \right) + \left(\frac{273+T+150S}{448} \right)^{17.7} \right] \qquad \text{Eqn (2)}$$

where

T = the operating temperature, ambient or case, as applicable (^oC)

S = the stress ratio of operating electrical stress to rated electrical stress

$$S = \frac{I_{OP}}{I_{MAX}} (CF)$$

I_{OP} = operating average forward current

I_{MAX} = maximum rated average forward current at T_s

T_s = maximum ambient or case temperature at which 100 percent of the rated load can be dissipated without causing the specified maximum junction temperature to be exceeded.

CF = stress correction factor

The stress correction factor (CF) is defined based on the conditions of device rating as enumerated in Table 3-34.

An estimate of the expected part failure rate is obtained by multiplying this base rate by the product of the various modifying factors defined in Eqn (1). Table 3-35 presents the values of these six factors for a general-purpose silicon rectifying diode as obtained from MIL-HDBK-217D.

Table 3-33. Multiplying Factors for Part Failure Rate Models

FACTOR	DESCRIPTION
Π_E	Environment - Accounts for influence of environmental factors other than temperature. Related to application categories
Π_Q	Quality - Accounts for effects of different quality levels.
Π_A	Application - Accounts for effect of application in terms of circuit function.
Π_R	Rating - Accounts for effect of maximum power or current rating.
Π_C	Construction - Accounts for effect of multiple devices in a single package.
Π_{S2}	Voltage Stress - Adjusts model for a second electrical stress (application voltage) in addition to wattage included within λ_b.

For each parameter the appropriate table has been marked to indicate the value which best describes the bypass diode application. The twenty environment categories listed in Table 3-35(a) range from a benign ground, G_B, condition to a cannon launch, C_L, with a fixed ground, G_F, being selected as the most representative for the photovoltaic bypass application. As shown in Table 3-35, the product of the selected values of the six factors equals 614.3.

Using Figure 3-48 as a typical silicon PN junction diode temperature derating curve, and assuming that the diode is operated at a I_{OP}/I_{MAX} ratio of 0.5, the CF value can be calculated as:

Table 3-34. MIL-HDBK-217D Silicon Diode Derating Conditions

Conditions	CF Value	T Value
$T_S = 25^oC$ $175 \leq T_{MAX} \leq 200^oC$	1.0	$T = T_C$
$T_S > 25^oC$ $175 \leq T_{MAX} \leq 200^oC$	$\frac{175-T_S}{150}$	$T = T_C$
$T_S = 25^oC$ $T_{MAX} < 175^oC$	$\frac{T_{MAX}-25}{150}$	$T = T_C + (175-T_{MAX})$
$T_S > 25^oC$ $T_{MAX} < 175^oC$	$\frac{T_{MAX}-T_S}{150}$	$T = T_C + (175-T_{MAX})$

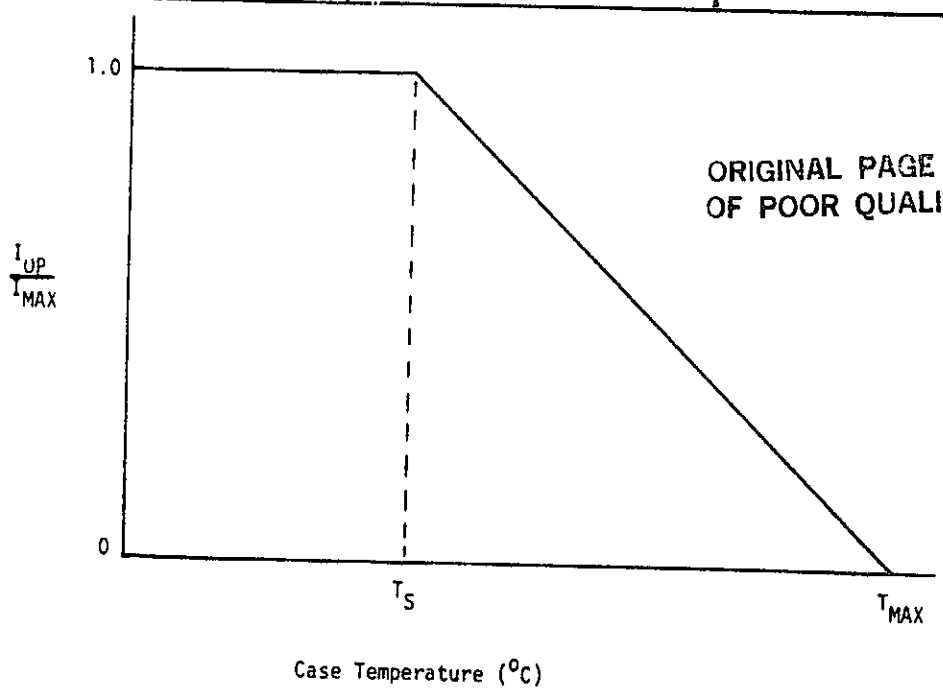


Table 3-35. The Evaluation of Multiplying Factors for General Purpose Silicon Diodes

(a)

Environment	Π_E
G_B	1
S_F	1
G_F	3.9
N_{SB}	4.8
N_S	4.8
A_{IT}	12
M_P	12
M_{FF}	12
M_{FA}	17
G_M	18
N_H	19
N_{UU}	20
A_{UT}	20
N_U	21
A_{IF}	25
A_{RW}	27
U_{SL}	36
A_{UF}	40
M_L	41
C_L	690

(b)

Quality Level	Π_Q
JANTXV	0.15
JANTX	0.3
JAN	1.5
Lower*	7.5
Plastic**	15.0

*Hermetic packaged devices.
**Devices sealed or encapsulated with organic material.

(c)

Contact Construction	Π_C
Metallurgically Bonded	1
Non-metallurgically Bonded (Spring loaded contacts)	2

(d)

Current Rating (amps.)	Π_R
≤ 1	1
1 to 3	1.5
3 to 10	2.0
10 to 20	4.0
20 to 50	10.0

(e)

Application	Π_A
Analog Circuits ($\leq$ 500 ma.)	1.0
Switching (< 500 ma.)	0.6
Power Rectifier ($\geq$ 500 ma.)	1.5
Power Rect. (H.V. Stacks) V max > 600	2.5/junction

(f)

S_2 (Percent)	Π_{S_2}
0 to 60	0.70
70	0.75
80	0.80
90	0.90
100	1.0

Voltage Stress, $S_2 = \frac{\text{Applied } V_R}{\text{Rated } V_R} \times 10$

V_R = diode reverse voltage.

$$\Pi_E \Pi_A \Pi_Q \Pi_R \Pi_{S_2} \Pi_C = 614.3$$

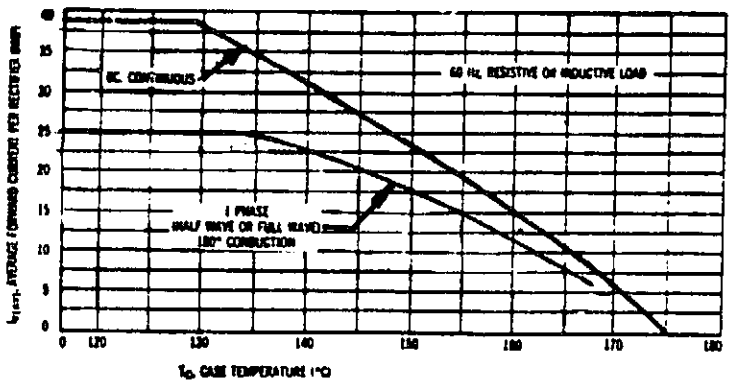


Figure 3-48. Typical Silicon PN Junction Diode Temperature Derating Curves

$$CF = \frac{175-T_S}{150} = \frac{175-129}{150} = 0.307$$

with a corresponding S value of

$$S = \frac{I_{OP}}{I_{MAX}} (CF) = (0.5)(0.307) = 0.154$$

Under these conditions the expected failure rate is given by:

$$\lambda_p = 614.3\ (0.172)\ \exp\left[\left(\frac{-2138}{296+T}\right)+\left(\frac{296+T}{448}\right)^{17.7}\right] \text{ failures}/10^6 \text{ Hours}$$

where

T = the operating diode case temperature (^oC)

This relationship is plotted in Figure 3-49 over the case temperature range from 50 to 175^oC.

3.9.4 ASSESSMENT OF BYPASS DIODE RELIABILITY

The applicability of available diode reliability data of the type described in the previous section to the condition of bypass diode operation was

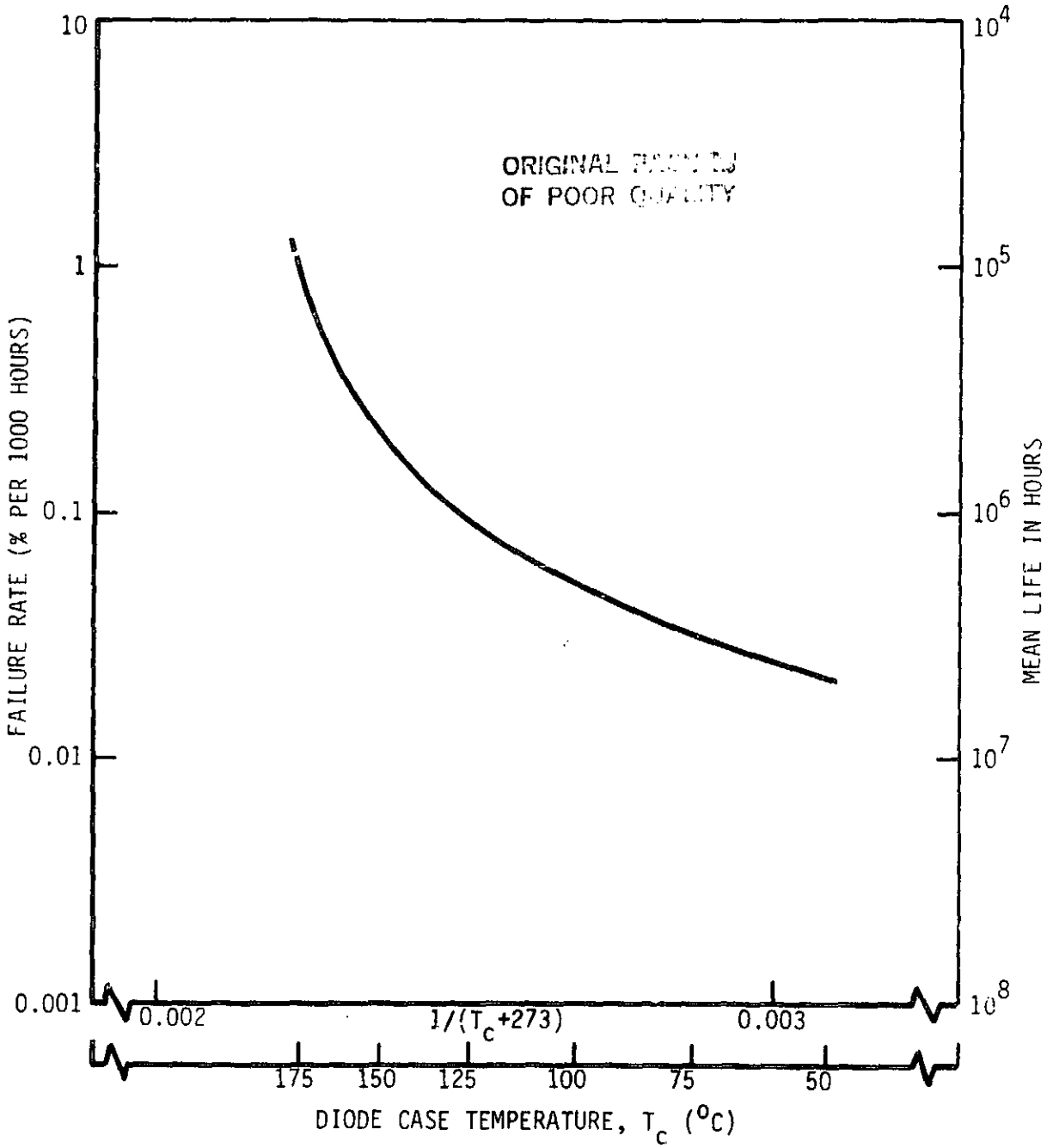


Figure 3-49. Failure Rate of a Silicon Rectifying Diode Using The MIL-HDBK-217D Methodology

addressed through personal contacts with several semiconductor manufacturers. No failure rate data is available for the operation of power diodes in the continuous dc reverse voltage blocking mode which is typical of the normal bypass diode operating condition. There is a general agreement among experts in this field that the continuous dc reverse voltage operation will tend to increase the leakage current with time compared to a normal ac rectifying application. However, the failure limit for reverse voltage leakage current in a photovoltaic module bypass application can be many orders of magnitude higher than that for the power rectifier and still operate satisfactorily. Consider a 6 ampere rated bypass circuit design where a 0.5 percent power loss due to diode leakage is allowed. Under these conditions the circuit can tolerate up to 30 mA of leakage current before the diode is considered to have failed. The reverse leakage current of a typical power rectifying diode is characteristically insensitive to exposure time at a given value of imposed reverse voltage. An order of magnitude increase in exposure time is generally required before a detectable increase in leakage current occurs.

Notwithstanding the obvious shortcomings in the available failure rate data as it might be applicable to the bypass diode operating conditions, it is possible to draw certain conclusions based upon rectifying diode data. For the photovoltaic module bypass application, the diode reliability will be almost exclusively determined by the reverse bias operating conditions since the exposure time under these conditions is many orders of magnitude larger than the expected exposure to a forward conducting operating condition. Fortunately, the average junction temperature under these reverse bias operating conditions is relatively low; with $45^{o}C$ being the maximum expected average temperature for a US site location. Also the magnitude of the reverse voltage is a small fraction of the lowest available rated value for PN junction devices. These two factors combine to yield a low failure rate for this diode application based on the available data. If Figure 3-46 is assumed to represent the failure rate of such diodes, then these conditions should yield 0.000015 failures per 1000 hours of operation or a 0.0013 device failure probability over the 20 year design life of the terrestrial array.

3.10 DIODE CELL THERMAL CYCLE TESTING

Semicon PN junction diode cells of two different sizes and ratings (S10976 and S10977) were soldered to small 0.032 inch thick copper heat spreader plates and subjected to 100 thermal cycles between the temperature extremes of 150 and -40°C. The dual chamber thermal cycling apparatus pictured in Figure 3-50 was used to obtain the temperature profile shown in Figure 3-51. With this apparatus, which conveys the specimens in a wire blanket elevator between the hot chamber at the top and the lower cold chamber, it is possible to obtain cycle time durations of approximately 26 minutes with at least 5 minutes of dwell time at each of the temperature extremes.

Prior to this temperature cycling exposure each of the six specimens of each diode cell type was screened to determine electrical characteristics, both forward and reverse, and to quantify the initial thermal resistance between the device junction and the heat spreader. The equipment pictured in Figure 3-52 was used to determine these thermal resistance values in much the same way as described in Appendix A where individually determined curves of forward voltage drop (at a 0.5 ampere test current) versus temperature are used to determine the junction temperature during high power pulse operation. This power pulse is interrupted on a repetitive 5 percent duty cycle to permit the determination of junction temperature by the measurement of diode forward voltage drop at the established 0.5 ampere test current. Using the previously determined calibration curve and extrapolating the forward voltage drop measurements back to the instant of power pulse interruption it is possible to calculate the device thermal resistance.

The results of these measurements are summarized in Table 3-36 along with the corresponding values obtained after the thermal cycling exposure. In all but two cases there was a significant increase in the thermal resistance between the silicon die and the heat spreader. Such changes are usually indicative of a propagation of the void area in the solder joint and it is probably safe to assume that the solder joint between the diode cell and the heat spreader is more susceptible to this occurrence since it was made using a less fatigue resistant Sn62 solder in an uncontrolled hand soldering operation without the use of forming gas. It is also interesting to note that the largest changes in thermal resistance are associated with the smaller R-type specimens. This appears to be contradictory with the

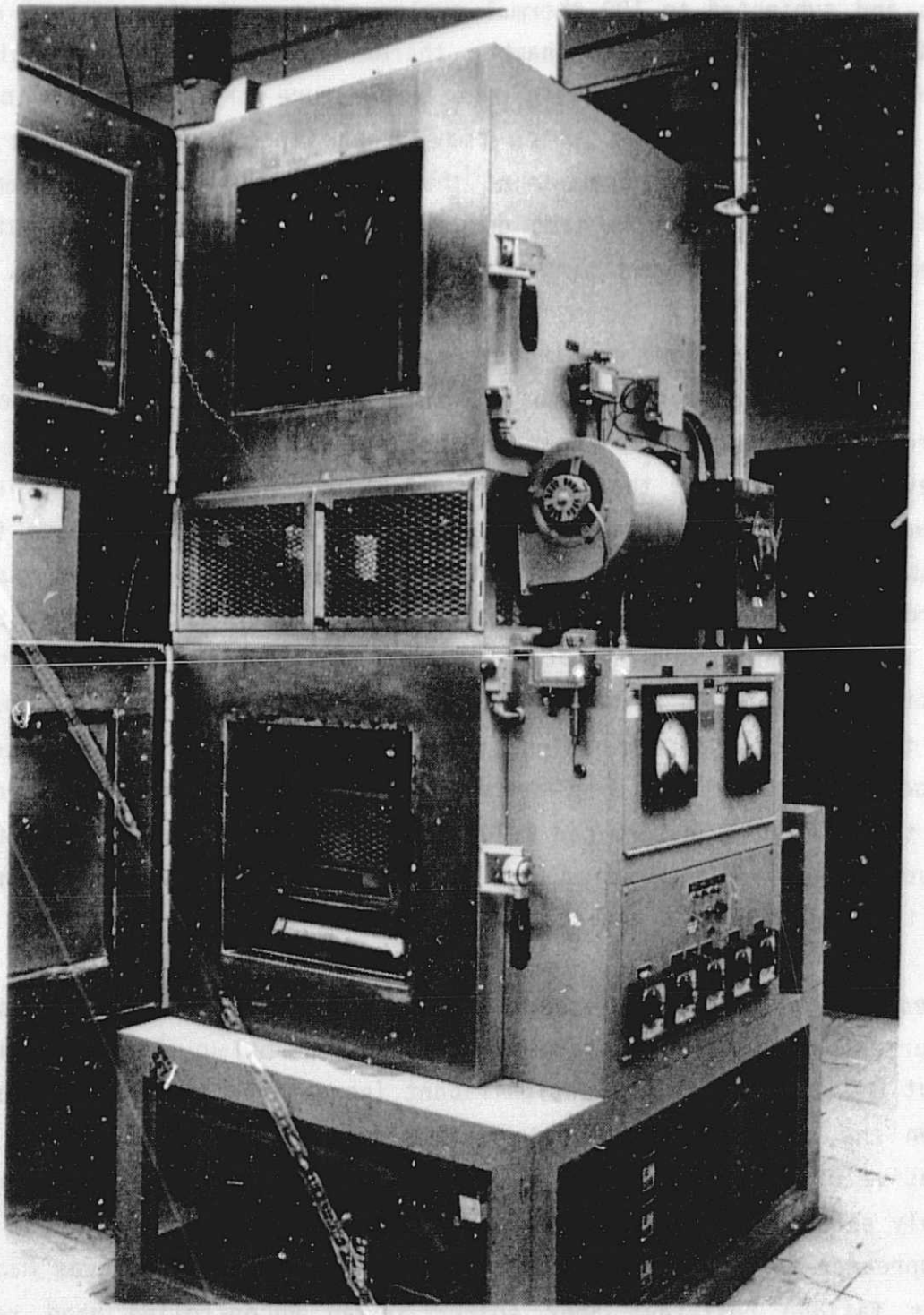


Figure 3-50. Thermal Cycle Test Apparatus

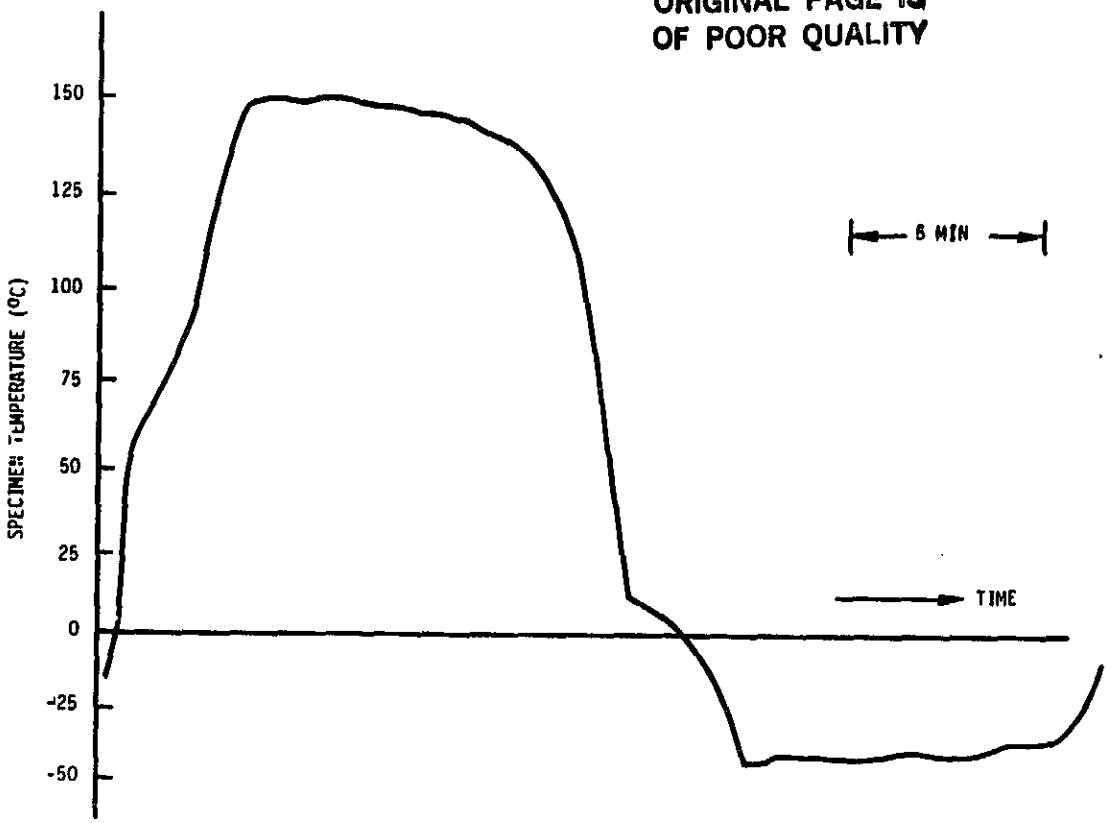
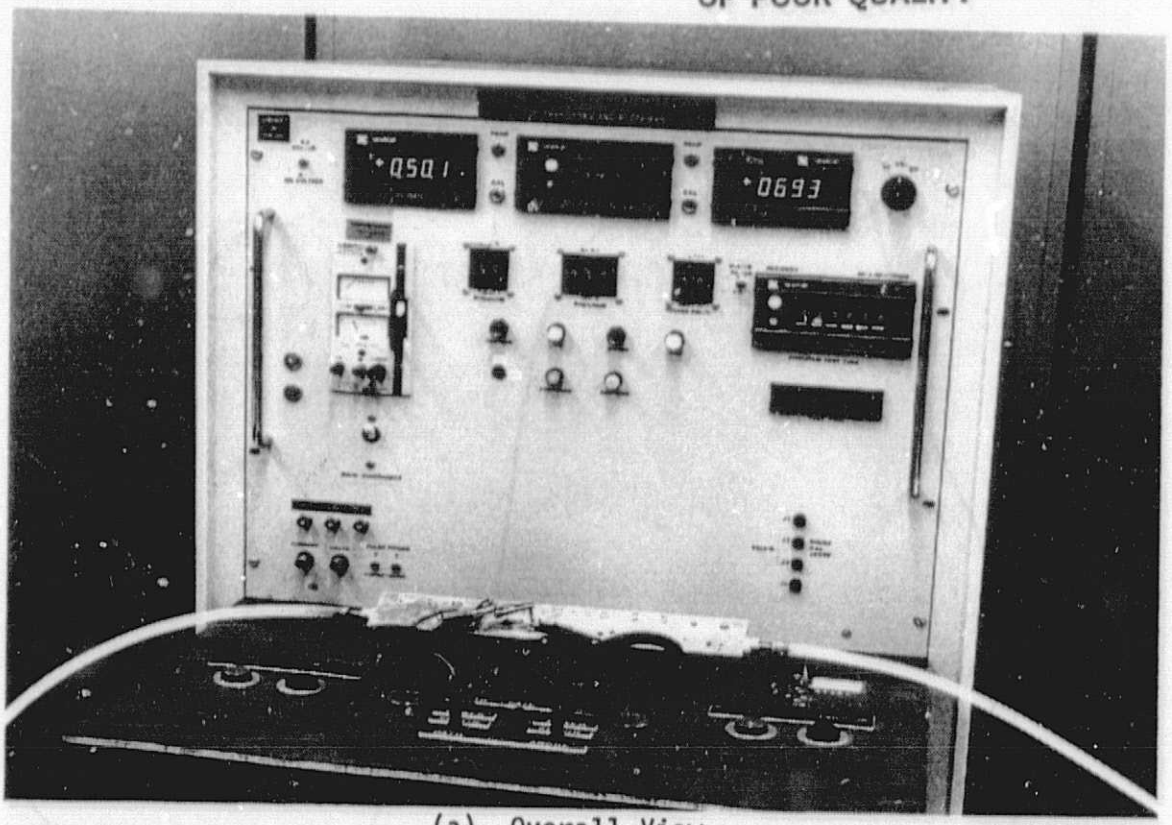


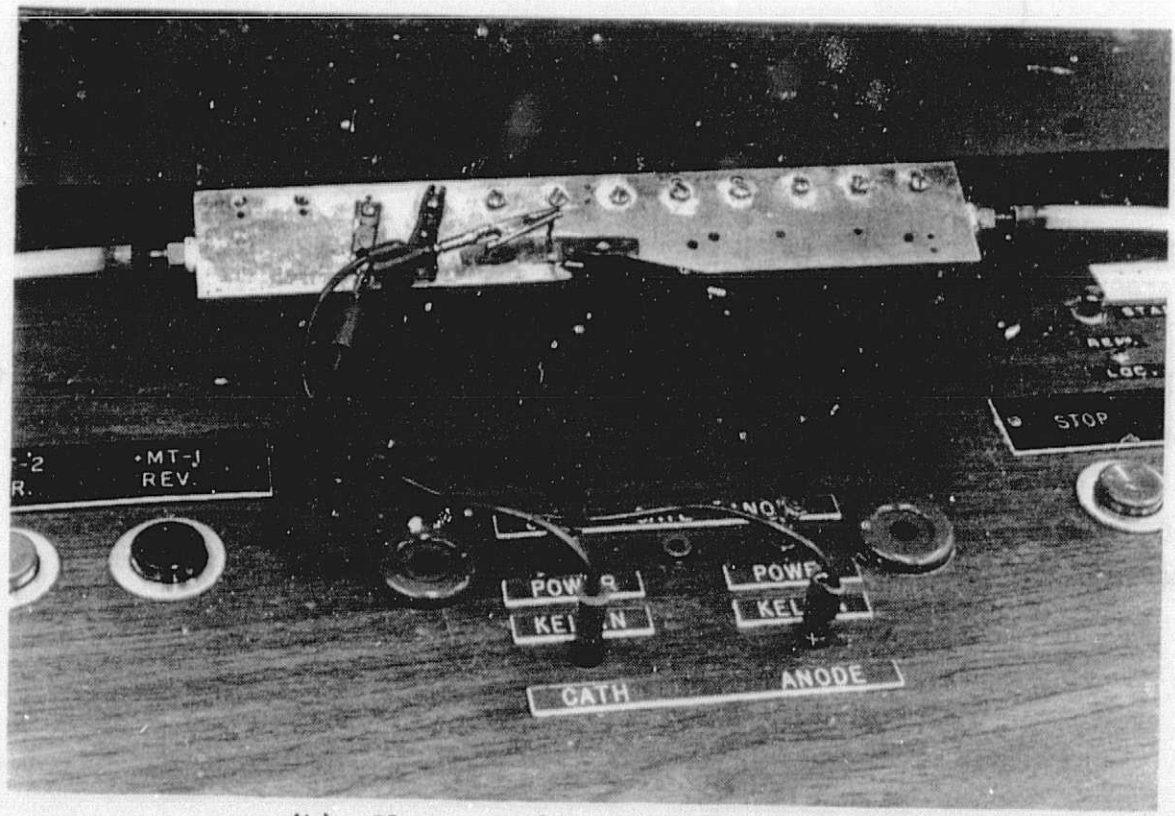
Figure 3-51. Typical Thermal Cycle Temperature Profile

predictions of theory which would assign the larger solder stress to the larger area device.

The electrical properties of the specimen diodes subjected to this temperature cycling exposure were nominal to start and were not significantly degraded by the exposure. In fact in several cases there was an improvement in the high (> 400 volts) reverse voltage stability of the device.



(a) Overall View



(b) Close-up of Specimen Mounting

Figure 3-52. Thermal Resistance Measurement Equipment

Table 3-36. Thermal Resistance Measurements Before and After Temperature Cycling

Specimen Identification Number	Junction-to-Sink Thermal Resistance (°C/watt)[1]		Percent Change
	Before Thermal Cycling	After Thermal Cycling[2]	
R1[3]	0.35	0.58	+ 66.
R2	0.35	0.75	+114.
R3	0.25	0.42	+ 68
R4	0.39	0.80	+105.
R5	0.29	2.00	+590.
R6	0.36	0.70	+ 94.
G1[4]	0.22	0.76	+245.
G2	0.55	0.65	+ 18.
G3	0.22	0.26	+ 18.
G4	0.30	0.52	+ 73.
G5	0.23	0.40	+ 74.
G6	0.26	0.45	+ 73.

(1) Includes the thermal resistance of a grease interface between the cathode plate and the heat sink. The calculated thermal resistance of this interface is 0.2°C/watt based on nominal values for contact area and grease film thickness.

(2) 100 cycles between 150 and -40°C

(3) R designates the S10976 device

(4) G designates the S10977 device

SECTION 4
CONCLUSIONS AND RECOMMENDATIONS

SECTION 4
CONCLUSIONS AND RECOMMENDATIONS

The lamination of bypass diodes within the module encapsulant solves many of the problems associated with the mounting of conventional packaged diodes external to the module, including: (1) the location of a suitable mounting area which is large enough to accommodate the rather bulky diode package and associated heat sink, (2) the electrical isolation of the diode case, which is usually the cathode connection of the diode, from the metallic heat sink, (3) the electrical bonding of the metallic heat sink to the module or array structural ground, and (4) the isolation of the electrically active parts of the bypass diode assembly from contact by personnel.

The soldered assembly of the diode cell to the heat spreader plate can be conveniently laminated on the rear side of the solar cell circuit where direct connections to the circuit terminations are possible. This relatively thin package can be readily accommodated within the existing encapsulant system where it is electrically isolated from the surroundings and environmentally protected.

Pad-mounted PN junction diodes of the type supplied by Semicon as a commercial product line are ideally suited to this application.

The heat spreader plate size required to accommodate the diode heat dissipation associated with a particular short-circuit current rating can be determined from experimental data obtained on representative module segments containing diode/heat spreader assemblies of various sizes. These data yield a recommended plate size versus diode heat dissipation relationship as shown in Figure 4-1. There was a large discrepancy between these experimental results and the predictions of a multi-node thermal model. Further work remains in the improvement of this thermal model to more accurately account for the lateral conduction of heat away from the hot spot.

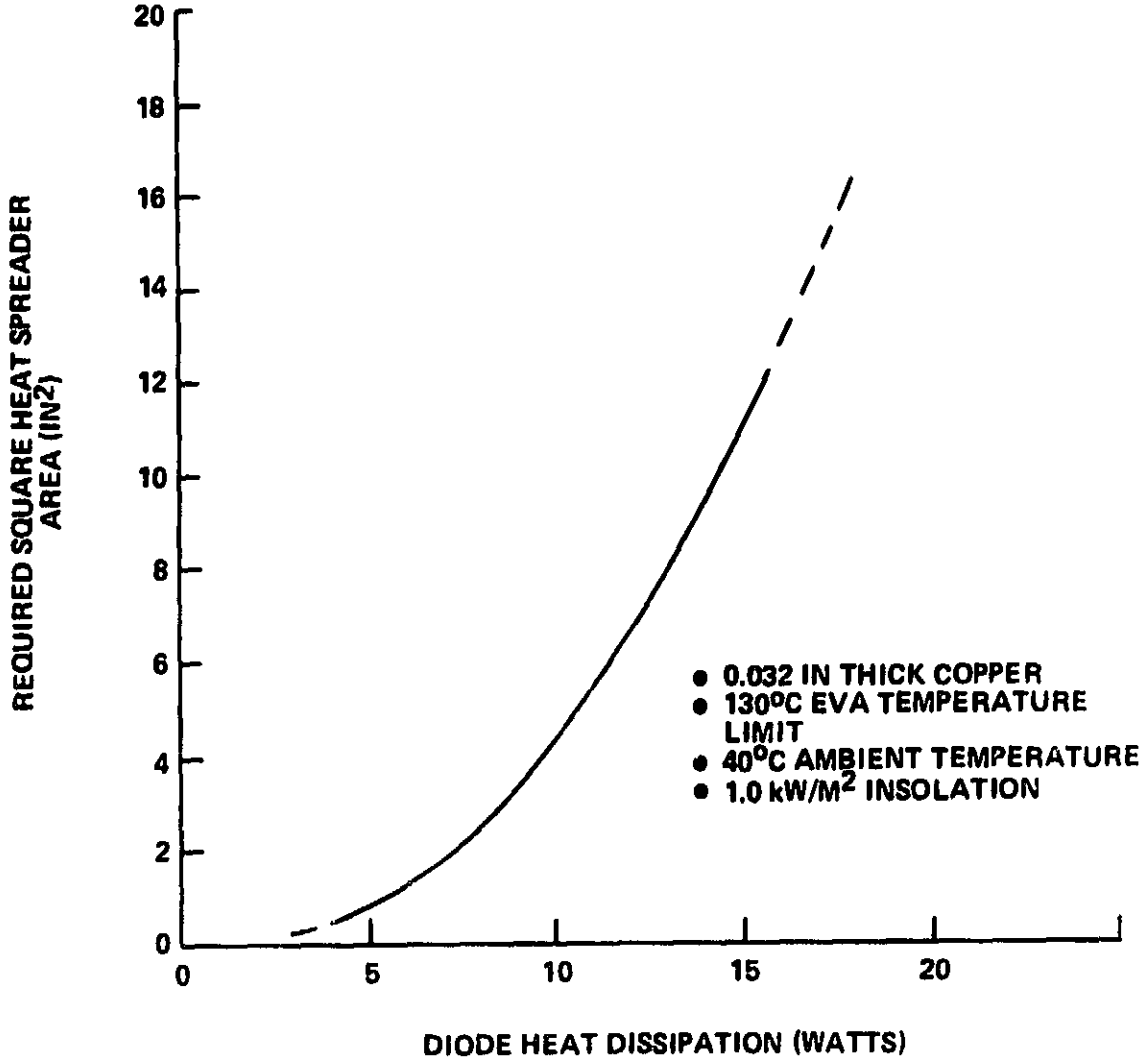


Figure 4-1. Recommended Encapsulated Diode Heat Spreader Plate Size Based on Limited Experimental Data

A comparative cost analysis of the encapsulated diode cell mounting approach versus the external enclosure mounting of a packaged diode has revealed no strong cost related incentive for one approach over another. In cases where the requirement for multiple module bypass diodes would require the repeated penetration of the module encapsulant for connections to externally-mounted diodes, it would seem logical to mount the diodes as an integral part of the encapsulation system so that no intermediate penetrations are required.

The use of a single module-mounted bypass diode must be questioned on the basis of intended function since such an application will not enhance the survivability of the module in the hot-spot heating test environment, as

defined by the proposed UL standard, and the inclusion of a single bypass diode at the module level may only complicate the array circuit design by introducing problems of current sharing among these individual module diodes if the array circuit designer wishes to employ a parallel-connected group of modules as a circuit element. Under such circumstances current sharing among parallel-connected diodes can be forced by the inclusion of an appropriately selected series resistance value in each bypass path. The magnitude of the voltage drop in each forward conducting bypass path will be significantly increased by the presence of this additional resistance. This, in turn, may cause a disproportionately large decrease in the power output capability of the affected branch circuit at the system output voltage which is determined by the maximum power operating point of the unaffected source circuits. This shortcoming can be avoided by the use of an externally-mounted bypass diode which is selected by the array circuit designer and sized to accommodate the bypass current from all parallel-connected modules in the bypass group. Virtually all bypass current will flow through this large external diode if its forward voltage drop, when passing this current, is significantly less than the individual module diodes. Such a situation can exist if the large external diode is a Schottky device and the single module diodes are PN junction devices or if multiple, series-connected PN junction devices are used as module bypass diodes with a single large PN junction diode used as the array bypass diode.

The photovoltaic module bypass application is not particularly demanding relative to the conventional rectifying application for power diodes. The operating environment for a photovoltaic module bypass diode is characterized by a prolonged exposure to a low level reverse voltage (~0 vdc during nighttime periods and typically 15 vdc during daytime periods). Under these reverse voltage conditions the diode temperature varies from near the ambient air temperature during nighttime periods to a temperature approximately equal to the module operating temperature during daytime periods. Occasionally the diode may be required to perform its bypass function by conducting the circuit current in the forward direction. Under these conditions the diode junction temperature could approach the maximum rated value, but the time spent in this mode of operation is several orders of magnitude less than the time spent in the reverse voltage operating mode.

Diode failure rate data is available for a rectifying application where the excitation source is a 60 Hz sinusoidal waveform and where failure is defined as a relatively small change in reverse leakage current. The application of this data to the dc blocking operation of a bypass diode leads to the general conclusion that, with proper design, the bypass diode failure rate will be sufficiently low so that their inclusion can be justified on the basis of an overall array reliability improvement over a 20 year design lifetime.

The thermal resistance between the diode junction and the heat spreader is a critical element in the determination of diode junction temperature (and, hence, reliability) under forward conducting conditions. The stability of this thermal resistance with temperature cycling requires further study in the light of the results from a limited thermal cycling exposure test where twelve specimens were cycled 100 times between the extremes of -40 and 150^{o}C. This temperature cycling exposure, which is unquestionably severe in terms of the magnitude of the temperature extremes, resulted in significant increases in the thermal resistance across the soldered interface between the silicon die and the heat spreader. Such changes in thermal resistance are indicative of the propagation of void areas in the solder joint.

APPENDIX A
THERMAL RESISTANCE MEASUREMENTS
OF
PAD-MOUNTED DIODE CHIPS

APPENDIX A
THERMAL RESISTANCE MEASUREMENTS
OF
PAD-MOUNTED DIODE CHIPS

A.1 TEST ARTICLE CONFIGURATION

Thermal resistance test articles with nickel-plated copper cathode plates and anode straps soldered to the pad-mounted diode chips were fabricated to the configuration shown in Figure A-1. The cathode plates were bent as indicated to provide a uniform area in contact with the test apparatus thermal block that provides a reference heat sink temperature. A thin layer of thermal grease is applied between the diode assembly and the test apparatus thermal block. The clamp shown in Figure A-2 was used to hold the diode to the thermal block.

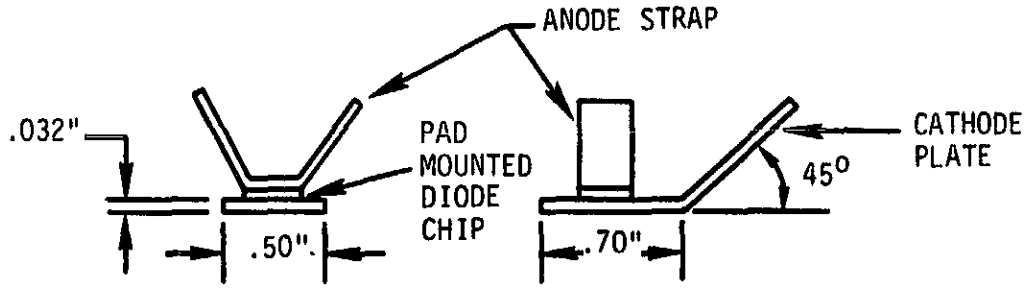


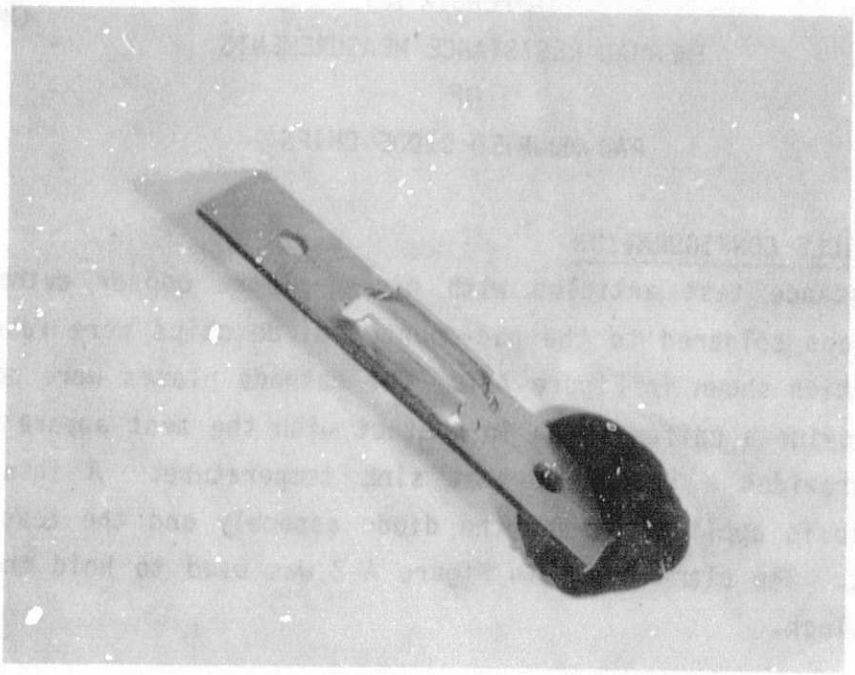
Figure A-1. Thermal Resistance Test Article Configuration

A.2 TEST PROCEDURE

The thermal resistance tests were performed using a computer controlled testing apparatus developed for testing power transistors [10]. In this equipment the forward voltage drop of the test device is utilized as the temperature sensing parameter at some fixed measurement current.

A schematic diagram of the equipment is shown in Figure A-3. The device under test (DUT) is mounted to a massive copper block heat sink using thermal grease to minimize interfacial temperature drop. The block has provision

10 A.J. Yerman, "A Thermal Resistance Tester and Its Use in Designing a 200 Amp Power Darlington Package", GE TIS Report 79GEN012, 1979 GOSAM Symposium, Paper 8.4.



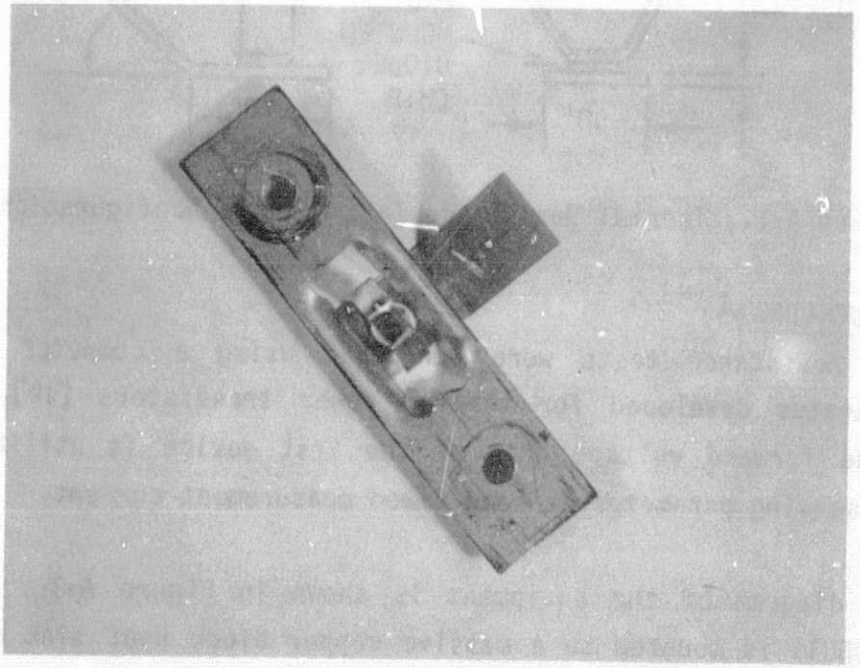


Figure A-2. Diode Holding Clamp

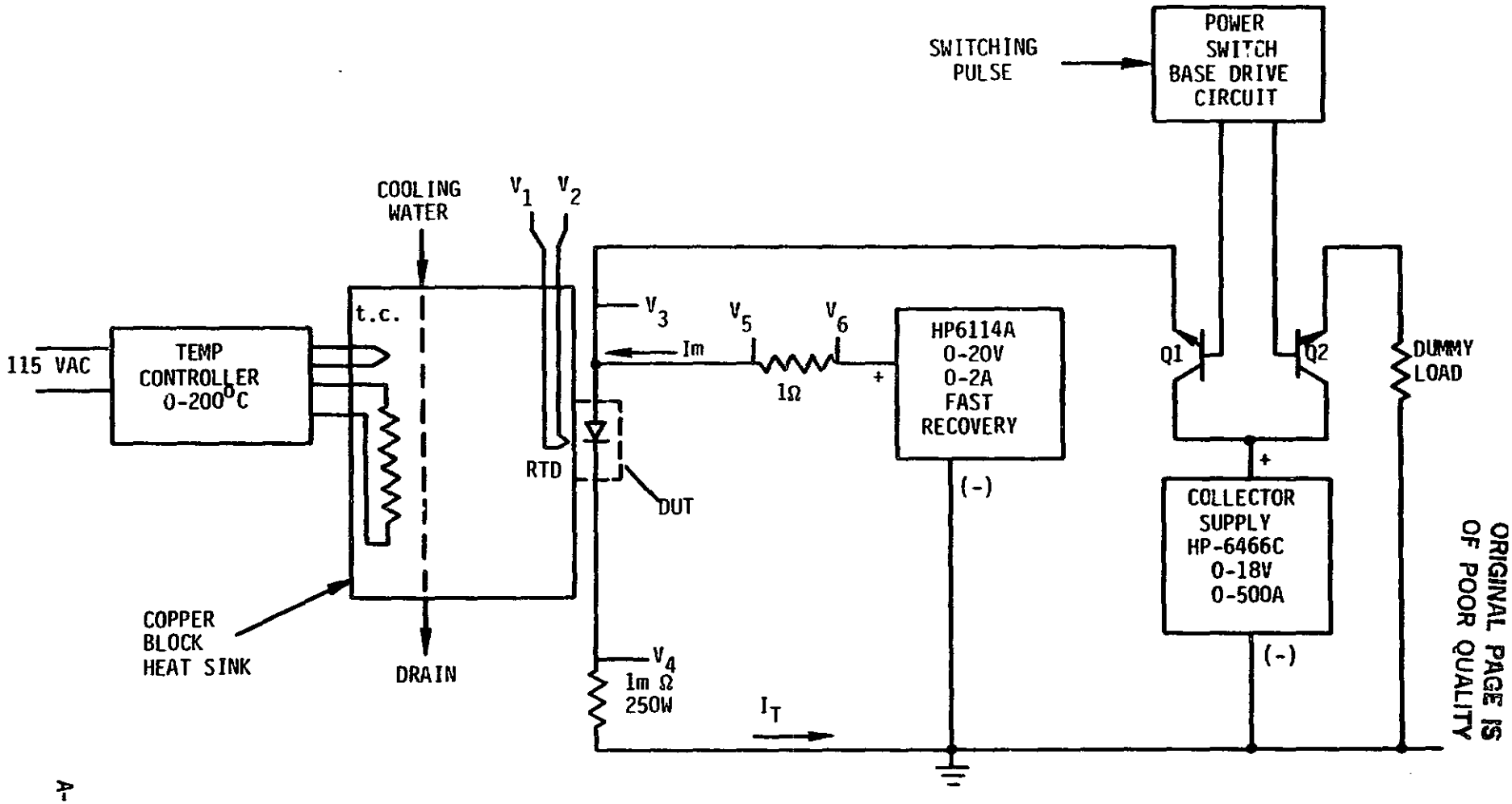


Figure A-3. Schematic Diagram of Thermal Resistance Measurement Equipment

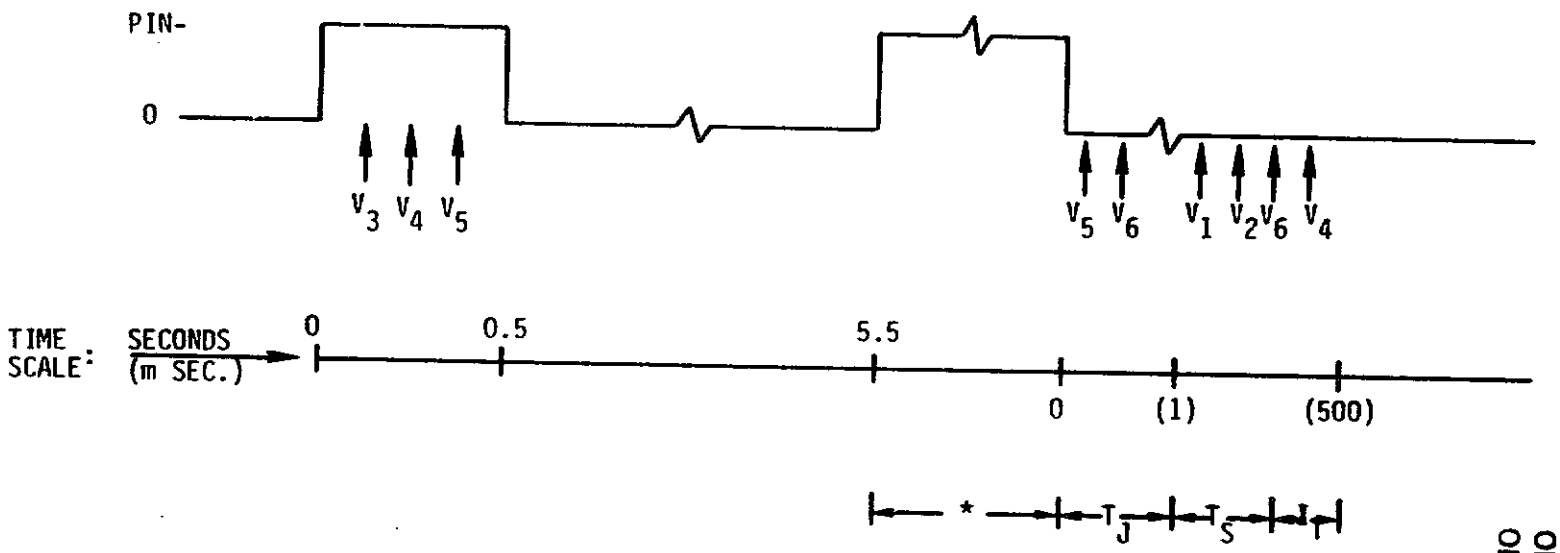
for heating and cooling and its temperature is measured with a platinum resistance temperature detector directly under the spot where the DUT is mounted. This provides the reference heat sink temperature (T_S) for the thermal resistance measurements. The test provides measurements of device junction temperature (T_J) and power dissipated in the DUT and calculated thermal resistance as:

$$R_{\theta_{JS}} = \frac{T_J - T_S}{P_{IN}} \qquad (^{o}C/Watt)$$

The junction temperature of the device is determined by measuring $V_F = V_5 - V_4$ (see Figure A-3 for a diagram of these measurement points) at constant measurement current I_M which is selected to satisfy DUT characteristics. A typical value is 1 ampere. Measurement current is monitored via the voltage drop across a 1 ohm resistor (V_6-V_5). P_{IN} is calculated from measurements of voltage (V_3-V_4) and current (I_T) determined with a precision 0.001 ohm resistor in series with the DUT.

The power dissipated in the device is controlled by the voltage setting of the collector supply. The current from this supply is routed by a pair of 200 ampere power Darlington transistors, Q1 and Q2, operated in push-pull mode so that it flows either into a dummy load or the DUT. This avoids problems associated with the relatively slow recovery time of the collector supply to large current transients. A base drive circuit interfaces Q1 and Q2 to the computer.

The time sequence of computer-controlled operations is illustrated in Figure A-4. Measurement of P_{IN} is made during a brief 0.5 sec power pulse, then after a pause of approximately 5 seconds the test power pulse is turned on. It can be set for any value between 1 msec and 30 sec. Valid measurements are not possible during this interval due to the large current flow and attendant voltages. Approximately 50 μsec after this power pulse is terminated and the transients have settled out and the DUT is cooling, V_5 is measured and stored. After 250 μsec the DUT temperature is measured a second time and from a backward extrapolation of these two measurements T_J is calculated at the time when the power pulse terminated. All voltage measurements are synchronized to the power pulses by the computer.



* CONTROLLABLE PULSE WIDTH RANGE 1m SEC - 30 SEC

Figure A-4. Timing Diagram for Power Control and Measurement

A thermal resistance determination consists of two steps:

1. Calibration of the temperature sensing parameter for the DUT.
2. Measurement of $R_{\theta_{JS}}$

The first step is accomplished by measuring the diode forward voltage at a series of known heat sink temperatures as measured by the platinum resistance temperature detector. A linear regression curve fit of this data provides a calibration curve for converting subsequent V_5 measurements to corresponding T_J values.

Both the first and second steps are carried out under computer control with appropriate safeguards to alert for spurious data or abnormal conditions.

Reported values of $R_{\theta_{JS}}$ are averaged from five separate measurements on each DUT.

A.3 SUMMARY OF TEST RESULTS

Thermal resistance test results are presented in Table A-1. Results were generally consistent with decreasing values of thermal resistance as chip area increased. However, in two cases, higher than anticipated values were obtained for a Semicon 20 amp PN unit (1.6°C/watt) and a Semicon 75 amp Schottky device (1.99°C/watt). X-rays of these two test articles, as shown in Figure A-5, revealed the presence of solder balls which probably indicate poor wetting of the solder. No large voids were evident. A transverse crack detected beneath the 75 amp Schottky device probably accounts for the abnormally high thermal resistance value obtained. A second Semicon 20 amp PN unit was tested and provided a value of 0.95°C/Watt as compared to the original value of 1.6°C/watt. A substitute Semicon 75 amp Schottky sample was not available for retest, and therefore a viable value for this device was not obtained.

The PN units showed a somewhat more consistent decrease in thermal resistance with increased chip area than the Schottky devices. Values of thermal resistance varied from a high of 0.97°C/watt for the smallest unit to a low of 0.45°C/watt for the largest device.

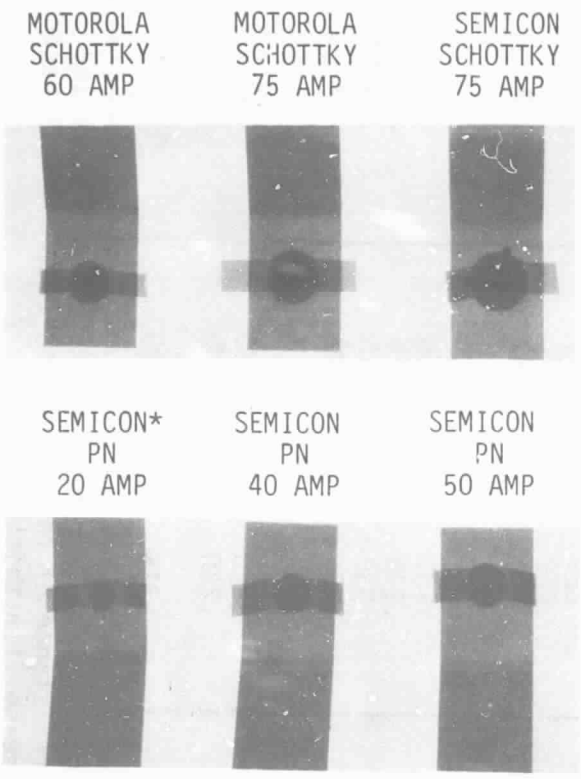
Table A-1. Measured Thermal Resistance - Mounted Type Diode Chips

Diode Mfg	Type	Chip Size (in)	Chip Area (in^2)	Base Pad Diameter (in)	Base Pad Area (in^2)	Measured Thermal Resistance* (^oC/Watt)
Semicon	12A PN	.120 dia.	.0113	.140	.1539	.97
"	20A PN	.140 dia.	.0154	.160	.0201	1.60 **
"	20A PN	.140 dia.	.0154	.160	.0201	.95
"	40A PN	.200 dia.	.0314	.220	.0380	.65
"	40A PN	.200 dia.	.0314	.220	.0380	.57
"	50A PN	.220 dia.	.0380	.240	.0452	.50
Motorola	15A Schottky	.126 sq.	.0159	.182	.0260	.78
"	30A Schottky	.160 sq.	.0256	.230	.0415	.79***
"	60A Schottky	.160 sq.	.0256	.230	.0415	.79***
"	75A Schottky	.200 sq.	.040	.286	.0642	.45
Semicon	15A Schottky	.130 sq.	.0169	.220	.0380	.84
"	30A Schottky	.165 hex (across flats)	.0236	.220	.0380	.72
"	75A Schottky	.210 sq.	.0441	.315	.0779	1.99 **

* Includes the thermal resistance of the grease interface between the cathode plate and the heat sink. The calculated thermal resistance of this interface is 0.3^oC/watt based on nominal value for contact area and grease film thickness.

** X-ray revealed poor wetting of solder; 75 amp Motorola Schottky had large transverse crack

*** Same size chip and pads used by Motorola; 30 amp unit - chrome barrier, 60 amp unit platinum barrier



*INITIAL SEMICON 20 AMP PN JUNCTION DIODE TESTED

Figure A-5. X-Ray Film of Diode Thermal Resistance Test Articles

APPENDIX B

DRAWINGS OF BYPASS DIODE ASSEMBLY

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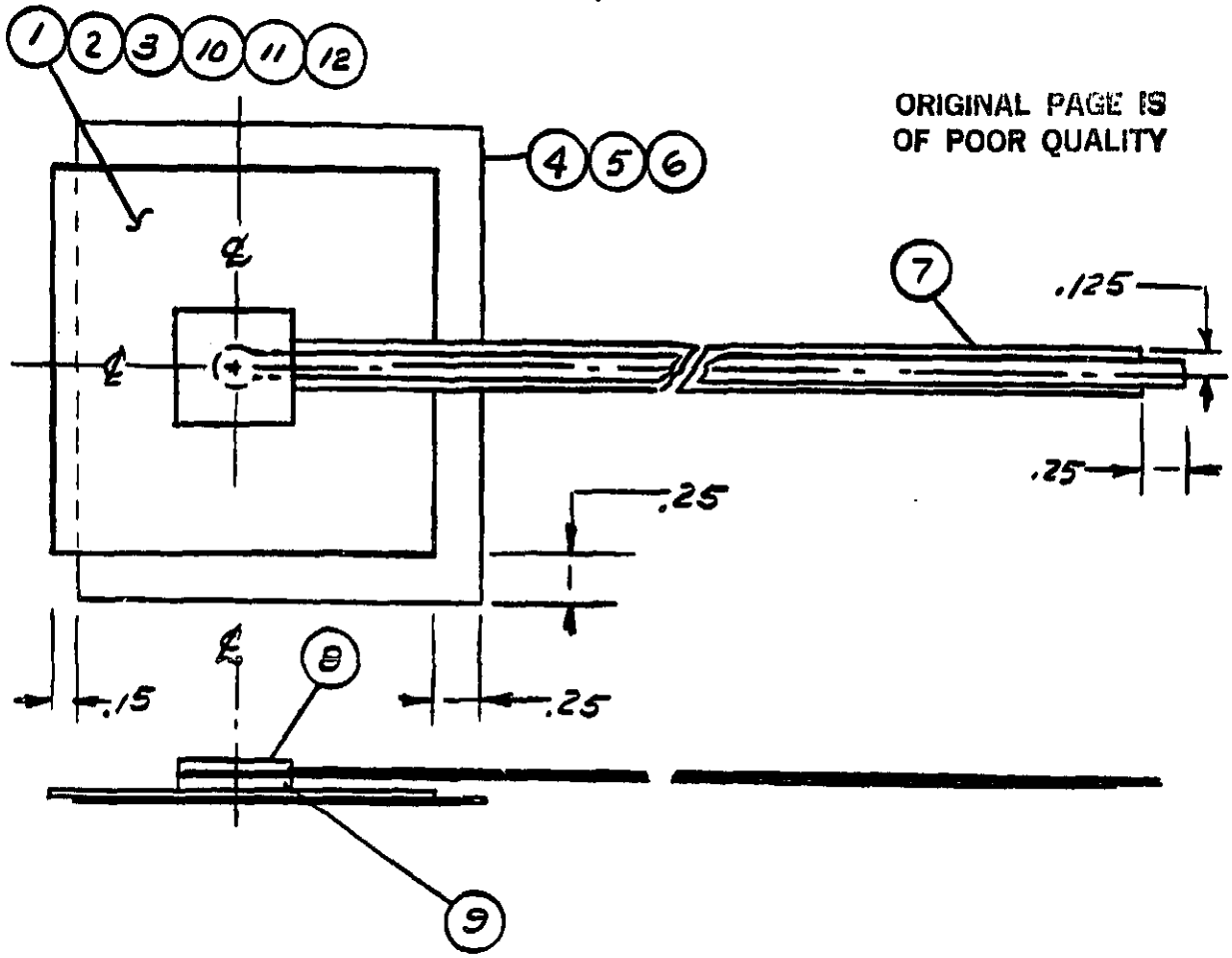

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QUANTITY REQUIRED FOR ASSY NO. G6	G5	G4	G3	G2	G1	PART NO.	NAME	DRAWING NO., DESCRIPTION, MATERIAL, WEIGHT
					1	1	SOLDERED ASSY	SK 022883-1 G1
				1		2	SOLDERED ASSY	SK 022883-1 G2
			1			3	SOLDERED ASSY	SK 022883-1 G3
		1			1	4	CATHODE INSL.	SK021083-1 P1
	1			1		5	CATHODE INSL.	SK021083-1 P2
1			1			6	CATHODE INSL.	SK021083-1 P3
1	1	1	1	1	1	7	ANODE INSL.	SK021083-2 P1
1	1	1	1	1	1	8	THER. BARRIER	SK 020983 P1
1	1	1	1	1	1	9	THER. BARRIER	SK 020983 P2
		1				10	SOLDERED ASSY	SK 022883-1 G4
	1					11	SOLDERED ASSY.	SK 022883-1 G5
1						12	SOLDERED ASSY.	SK 022883-1 G6

ADDED G4-G6

REV 1 - CORRECTED P.N. ERROR IN 1, 2, 3

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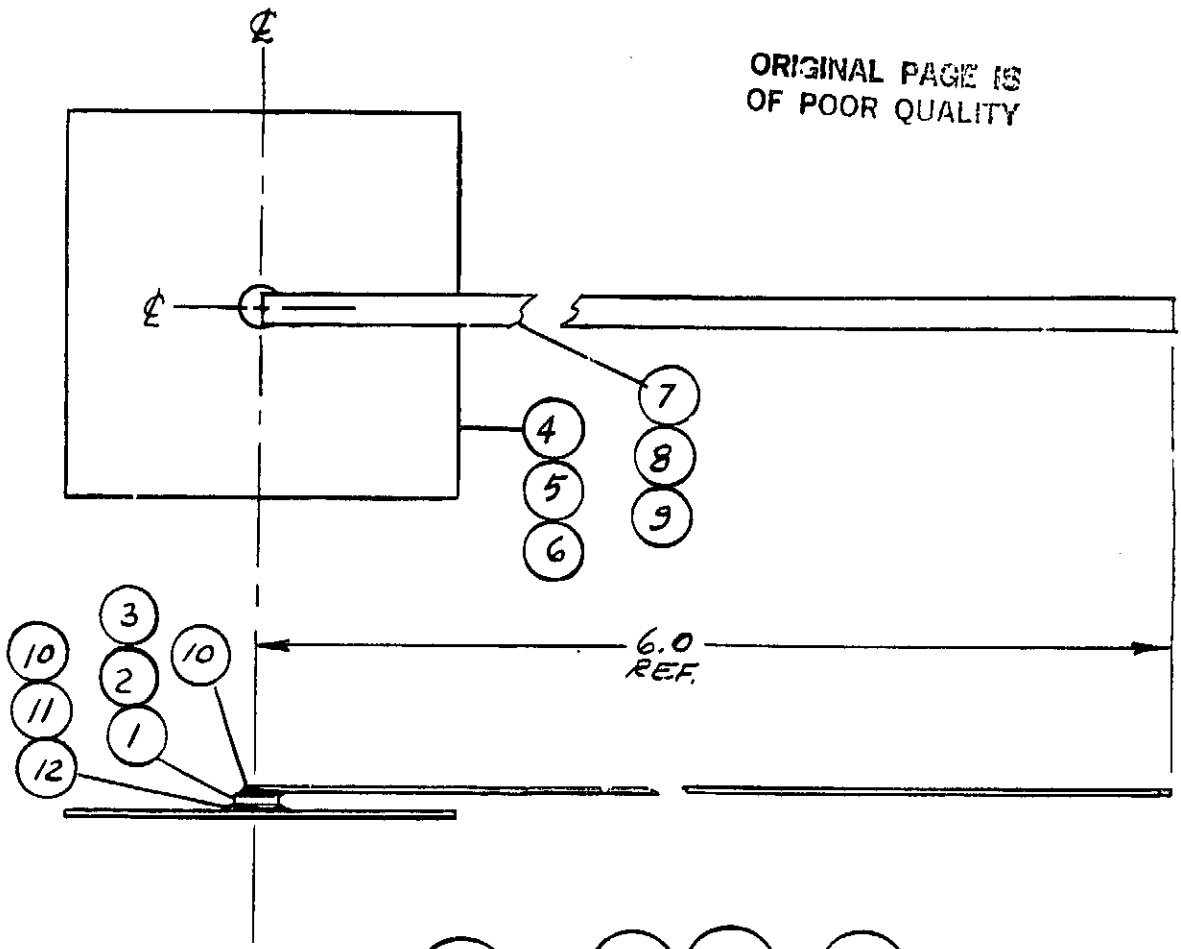

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TITLE
BYPASS DIODE - SOLDERED ASSY.

FIRST MADE FOR

6	5	4	3	2	1	PART NO.	NAME	DRAWING NO., DESCRIPTION, MATERIAL, WEIGHT
		1			1	1	DIODE	20A (.14 DIA)
	1			1		2	DIODE	40A (.20 DIA)
1			1			3	DIODE	50A (.22 DIA)
					1	4	CATHODE HT. PL	SK020983-1 P1
				1		5	CATHODE HT. PL	SK020983-1 P2
			1			6	CATHODE HT. PL	SK020983-1 P3
		1			1	7	ANODE LEAD	SK020983-2 P1
	1			1		8	ANODE LEAD	SK020983-2 P2
1			1			9	ANODE LEAD	SK020983-2 P3
1	1	2	1	1	2	10	SOLDER PREFM.	(.115 DIA)
	1			1		11	SOLDER PREFM.	(.165 DIA)
1			1			12	SOLDER PREFM.	(.216 DIA)
		1				13	CATHODE HT PL.	(ALUM) SK 020983-1 P4
	1					14	CATHODE HT PL	(ALUM) SK 020983-1 P5
1						15	CATHODE HT PL	(ALUM) SK 020983-1 P6

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TITLE

BYPASS DIODE SOLDERED ASSY

FIRST MADE FOR

GROUP NO. AND QUANTITY						PART NO.	NAME	DRAWING NO., DESCRIPTION, MATERIAL, WEIGHT
G12	G11	G10	G9	G8	G7			
		1			1	1	DIODE	20A .14 DIA
	1			1		2	DIODE	40A .20 DIA
1			1			3	DIODE	5A .22 DIA.
					1	4	CATHODE HT PC	SK 022383-1 P1 (COPPER)
				1		5	CATHODE HT PC	SK 022383-1 P2 (COPPER)
			1			6	CATHODE HT PC	SK 022383-1 P3 (COPPER)
		1			1	7	ANODE LEAD	SK 020983-1 P1
	1			1		8	ANODE LEAD	SK 020983-1 P2
1			1			9	ANODE LEAD	SK 020983-1 P3
1	1	2	1	1	2	10	SOLDER PFM	.115 DIA
	1			1		11	SOLDER PFM	.165 DIA
1			1			12	SOLDER PFM	.216 DIA
		1				13	CATHODE HT PLT	SK 022383-1 P4 (ALUM)
	1					14	CATHODE HT PLT	SK 022383-1 P5 (ALUM)
1						15	CATHODE HT PLT	SK 022383-1 P6 (ALUM)

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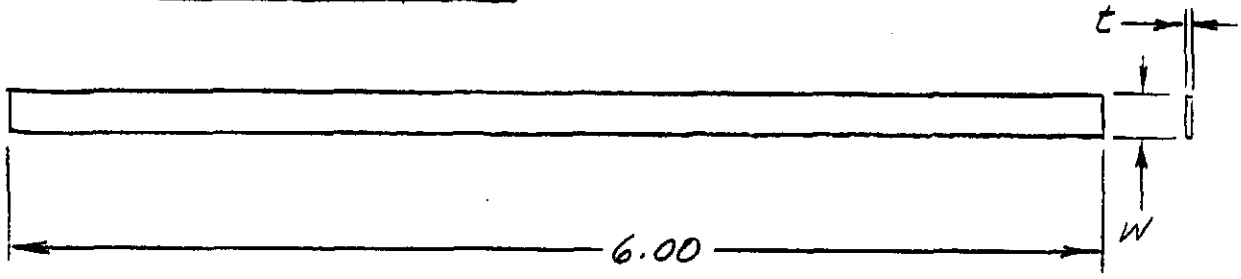
ANODE LEAD

FIRST MADE FOR BYP. DIODE

PART	W	t
1	.12	.005
2	.17	.007
3	.18	.010



NOTES:
1. PART MUST BE FREE OF BURRS AND STRAIGHT WITHIN ±.06

MATL: COPPER ALLOY 110

COATING: TIN PLATE ALL SURFACES EXCEPT ENDS MAY BE BARE.

SCALE: NONE

N.A. SK 022883-1

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		✓			

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SK 020983-1

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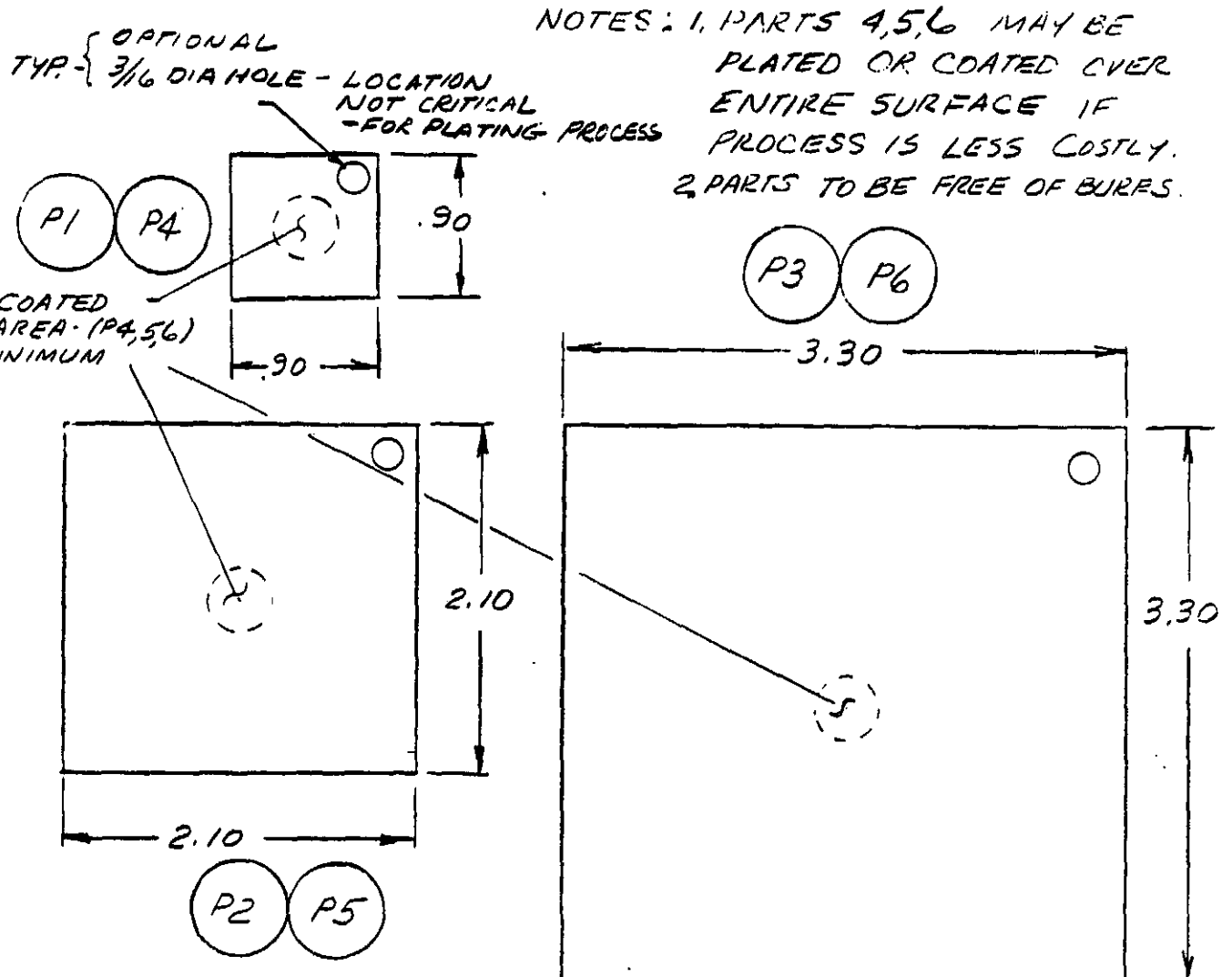
	HEAT SPREADER PLATE, CATHODE		
CONT ON SHEET / SH NO.	FIRST MADE FOR BYP. DIODE		

NOTES: 1. PARTS 4,5,6 MAY BE PLATED OR COATED OVER ENTIRE SURFACE IF PROCESS IS LESS COSTLY.
2. PARTS TO BE FREE OF BURRS.



PT.	MATL	THICK.
1	CU ALLOY 110	.032
2	TIN-COATED ALL SIDES & EDGES	.032
3		.032
4	AL. 1100 ALLOY	.056
5	NICKEL COAT. .38 DIA ONE SIDE MIN.	.056
6		.056

NA. SK 022883-1

UNLESS OTHERWISE SPECIFIED USE	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
	± .03	√	±	±	±

SCALE-FULL

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PRINTS TO

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D MULLINGS			SK 020983-1
ISSUED		LOCATION	CONT ON SHEET B-7

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GENERAL ELECTRIC

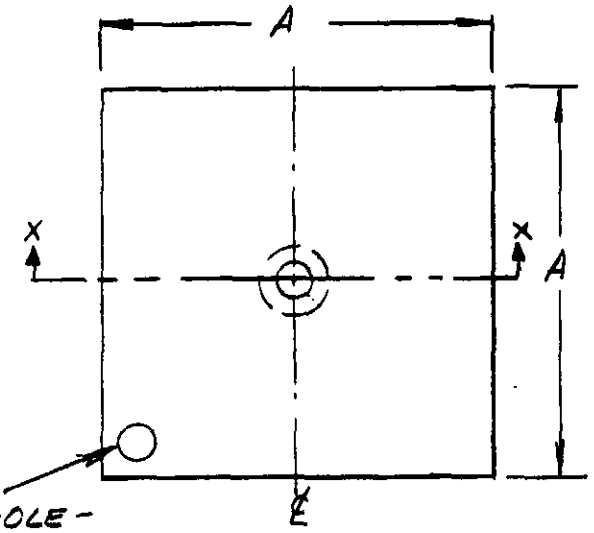
SK 022383-1

REV NO. | TITLE

HEAT SPREADER PLATE - CATHODE

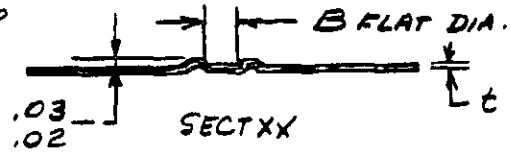
CONT ON SHEET | SH NO. | FIRST MADE FOR BYP. DIODE

ORIGINAL PAGE IS OF POOR QUALITY



PT	A	B	MTL.	THK.
1	.9	.16	CU ALLOY #110 .0002 TIN-COAT	.032
2	2.1	.22		
3	3.3	.24		
4	.9	.16	AL. ALLOY 1100, NICKEL COAT *	.056
5	2.1	.22		
6	3.3	.24		

OPTIONAL .18 DIA HOLE - LOCATION NOT CRITICAL - FOR PLATING PROCESS.



*NOTE
1. NICKEL COATING IS FOR SOLDERING PURPOSE. MAY BE CONFINED TO "B" DIA. AREA, IF ECONOMICAL TO PRODUCE.

NA. SK 022383-1

UNLESS OTHERWISE SPECIFIED USE	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
		✓	±	± .03	±

REVISIONS | PRINTS TO

MADE BY D MULLINGS | APPROVALS | DIV OR DEPT | LOCATION | SK 022383-1

ISSUED | B-8 | CONT ON SHEET | SH NO.

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GENERAL ELECTRIC

SK 021083-1

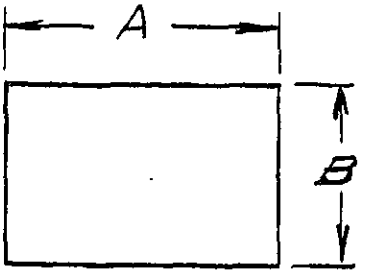
REV NO | TITLE: CATHODE INSULATION | CONT ON SHEET | SH NO.

CONT ON SHEET | SH NO. | FIRST MADE FOR BYP. DIODE

ORIGINAL PAGE IS
OF POOR QUALITY

PT.	"A"	"B"	
1	1.4	1.0	
2	2.6	2.2	
3	3.8	3.4	

NOTE:
MATL. TO BE PROVIDED CUT TO SIZE IN ROLLS OR IN STRIPS OF NOT LESS THAN 10 PARTS / STRIP. WITH RELEASE BACKING.



MATERIAL: ADHESIVE-BACKED POLYESTER M99 TAPE / SILICONE ADHESIVE.
SOURCE: CONNECTICUT HARD RUBBER CO.

NA. SK 030183-1 SCALE - NONE

UNLESS OTHERWISE SPECIFIED USE	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS: FRACTIONS	DECIMALS	ANGLES
		✓	±	± .03	±

REVISIONS | PRINTS TO

MADE BY D MULLINGS | APPROVALS | DIV OR DEPT | LOCATION | SK 021083-1 CONT ON SHEET

ISSUED

FF-803-F (3-79-A)

GENERAL ELECTRIC

SK 020983-3
CONT ON SHEET SH NO.

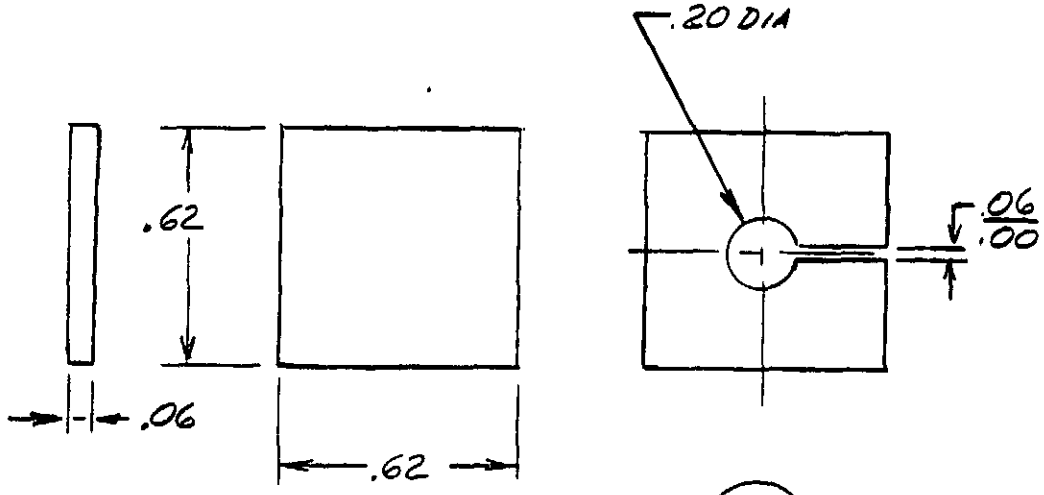
REV NO.

CONT ON SHEET SH NO.

TITLE
THERMAL BARRIER

FIRST MADE FOR

ORIGINAL PAGE IS
OF POOR QUALITY



P1

P2 - SAME AS P1 EXCEPT AS SHOWN.

MATL: SILICONE RUBBER SPONG
ADHESIVE - SILICONE TAPE "STRIP 'N' STICK"
SOURCE: CONNECTICUT HARD RUBBER CO.
SCALE ~ 2X

N.A. SK 030183-1

UNLESS OTHERWISE SPECIFIED USE	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
			FRACTIONS	DECIMALS	ANGLES
	----------	✓	±	± .03	±

REVISIONS

PRINTS TO

MADE BY D.MULLINGS
ISSUED B-10

APPROVALS

DIV OR DEPT
LOCATION

SK020983-3
CONT ON SHEET SH NO.

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GENERAL ELECTRIC

SK 021083 - 2

REV NO | TITLE

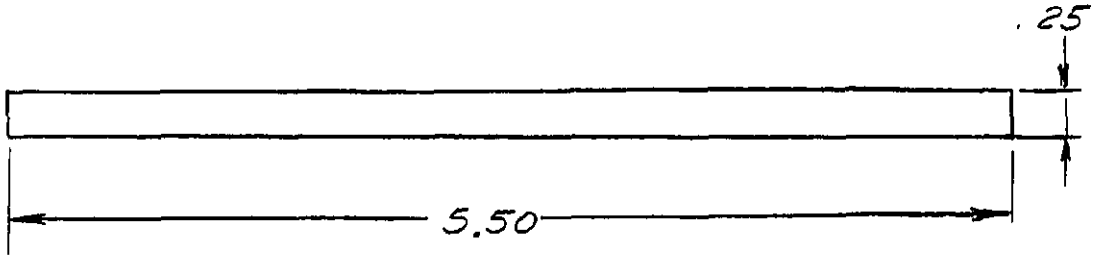
CONT ON SHEET | SH NO.

ANODE INSULATION

CONT ON SHEET | SH NO.

FIRST MADE FOR · BYP. DIODE

ORIGINAL PAGE IS
OF POOR QUALITY



MATL: POLYESTER TAPE
M99 / SILICONE ADHESIVE
SOURCE CONNECTICUT HARD RUBBER

SCALE - NONE

NA. SK 030183 - 1

UNLESS OTHERWISE SPECIFIED USE	APPLIED PRACTICES	SURFACES	TOLERANCES ON MACHINED DIMENSIONS		
			FRACTIONS	DECIMALS	ANGLES
	----------	✓	±	± .03	±

REVISIONS | PRINTS TO

MADE BY	APPROVALS	DIV OR DEPT	
D. MULLINGS			SK 021083 - 2
ISSUED		LOCATION	CONT ON SHEET B-11/12

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