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most efficient procedure on Gaussian channels and affords 4 dB of gain for 4-state trellises and soft-decision demodulation, relative to an uncoded signal having equal bandwidth. With parallel processing available in LSI form, such decoders can operate above 100 Mbps, although we have not yet undertaken an implementation study.

From a fabrication perspective, we have concentrated on the use of GaAs device technology in implementing a modem-on-a-chip(s), of the dual-mode type described above. We have performed a detailed survey of current device developments in linear RF components and switching logic with the result being that such integration is technically feasible and GaAs FET technology is currently available for all functions (RF amplification, mixing, modulators, threshold comparators, video amplifiers, logic, etc.). Many of the necessary building blocks have been demonstrated in laboratories of MMIC manufacturers, indicating that a fully-integrated modem is a reasonable undertaking.

The report is organized as follows, with references and figures numbered by chapter:

Chapter 2 summarizes the work on communications techniques, both modulation and coding, and provides a description of the dual-modem technique. Synchronization procedures are also described.

Chapter 3 provides an assessment of GaAs technology as applied to the more specific problem of a modem development activity.

Chapter 4 summarizes our conclusions and recommendations for further work.

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1. INTRODUCTION

This report summarizes work in support of advanced communication technology development at NASA. Our investigation has merged current developments in communications theory and practice, with state-of-the-art technology in IC fabrication, especially monolithic GaAs technology, to examine the general feasibility of a number of advanced technology digital transmission systems. The principal motivation of this work is toward producing satellite-channel modems with (1) superior throughput, perhaps 2 Gbps; (2) attractive weight and cost; and (3) high RF power and spectrum efficiency. These attributes are of course sought in many communication applications, and we foresee the work described here as important to terrestrial digital radio as well.

The investigation began with a survey of transmission techniques generally applicable to this problem, those possessing reasonably simple architectures capable of monolithic fabrication at high speeds. This included a review of amplitude/phase shift keying (APSK) techniques and the continuous-phase-modulation (CPM) methods, of which MSK represents the simplest case. Our feeling is that while CPM provides constant-envelope modulation designs with very attractive power and spectrum features, the ones which do so are presently too difficult to implement at speeds above 100 Mbps, particularly in any highly-integrated form. A possible exception is the use of MSK-type receivers for binary, $h = 1/2$ CPM schemes, for which good spectral sidelobes are afforded with only fractional dB loss in energy efficiency. On the other hand, for lesser throughput applications, e.g. 56 kbps low-rate satellite links, we feel

CPM has high potential, though still more complicated than simpler APSK methods.

The modulation study evolved into definition of a dual-technique, capable cf performing either QPSK or 16-QASK with simple mode switches. These techniques are highly compatible in that 16-QASK is realizable as a super-position of two QPSK signals, one 6 dB weaker in power than the other. The two choices provide a range of power/bandwidth efficiencies. QPSK is the most energy efficient among uncoded transmission schemes, while QASK has twice the spectral efficiency at a sacrifice of about 4 dB in required average E_b/N_o. A modem to implement either technique is not substantially more difficult than that to implement either alone, and provides the added system flexibility. In addition to its favorable modulation attributes, QPSK/QASK provides a convenient signal base for convolutional coding.

We studied the application of coding for high-speed channels with the principle concern being decoder complexity. Convolutional codes were treated from the perspective of interfacing with the QPSK/QASK modulation technique. The simplest decoding technique is that of threshold decoding, which generally operates on hard-decision demodulator outputs with logic gates to do error correction. Rate one-half codes of reasonable complexity can gain several dB in exchange for a doubling of bandwidth per information bit. On the other hand, the use of similar techniques for r = 3/4 coding onto QASK does not seem to have any utility; basically, the code is not able to correct enough errors to overcome loss in energy per code symbol, and an energy loss ensues, at least for short codes. Maximum likelihood (Viterbi) decoding is the

most efficient procedure on Gaussian channels and affords 4 dB of gain for 4-state trellises and soft-decision demodulation, relative to an uncoded signal having equal bandwidth. With parallel processing available in LSI form, such decoders can operate above 100 Mbps, although we have not yet undertaken an implementation study.

From a fabrication perspective, we have concentrated on the use of GaAs device technology in implementing a modem-on-a-chip(s), of the dual-mode type described above. We have performed a detailed survey of current device developments in linear RF components and switching logic with the result being that such integration is technically feasible and GaAs FET technology is currently available for all functions (RF amplification, mixing, modulators, threshold comparators, video amplifiers, logic, etc.). Many of the necessary building blocks have been demonstrated in laboratories of MMIC manufacturers, indicating that a fully-integrated modem is a reasonable undertaking.

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Chapter 4 summarizes our conclusions and recommendations for further work.

A bibliography compiled during the course of our investigation is included in the Appendix. Articles pertain principally to high-speed devices, especially in GaAs.

2. MODULATION AND CODING EVALUATION

This section summarizes investigation of communications techniques appropriate for an "advanced performance" modem, meaning high-speed (> 1 Gbps), low-cost (capable of monolithic integration), and good energy and spectral properties. We begin with the modulation study.

2.1 MODULATION

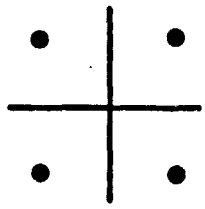
Quadrature-modulation techniques are well-known approaches for achieving good spectral/energy efficiencies with simple hardware. The best known example of this class is QPSK (quadrature phase-shift-keying), which amounts to two BPSK concerns in phase-quadrature. The energy efficiency (E_b/N_o needed) equals that of BPSK, but spectral efficiency is twice as high.

The signals in general are represented as

$$S_i(t) = a_i \cos \omega_c t + b_i \sin \omega_c t \ , \qquad i = 0, 1, \ldots M-1$$

where (a_i, b_i) represents the 2-D coordinate of the ith signal. The set of all such points is known as the signal constellation, and several cases of interest are shown in Figure 2.1 for M = 4, 8, 16, and 32. All but the PSK sets have rectangular geometry such that data decisions are effected by quadrature demodulation, filtering, sampling, and threshold detection. For 8-PSK and 16-PSK, the I and Q samples must be combined linearly to make data decisions.

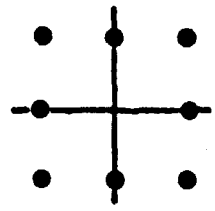
The probability of bit error versus E_b/N_o for these techniques is illustrated in Figure 2.2. These are actually asymptotic expressions in most cases which are most accurate below $P_b = 10^{-4}$. As expected,



$M=4$

$P[E] \sim 2Q\left(\sqrt{2\bar{E}_b/N_0}\right)$

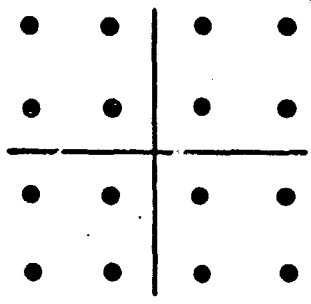
$E_p = \bar{E}$



$M=8$

$P[E] \sim 2Q\left(\sqrt{\bar{E}_b/N_0}\right)$

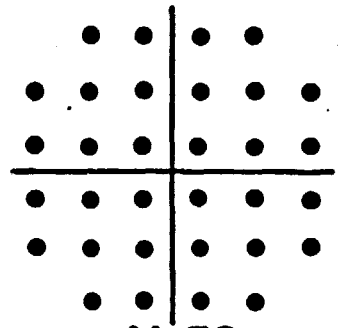
$E_p = 1.33\bar{E}$



$M=16$

$P[E] \sim 4Q\left(\sqrt{0.8\bar{E}_b/N_0}\right)$

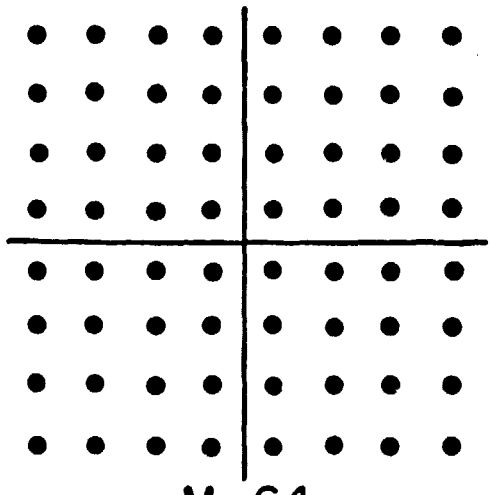
$E_p = 1.8\bar{E}$



$M=32$

$P[E] \sim 4Q\left(\sqrt{0.5\bar{E}_b/N_0}\right)$

$E_p = 1.7\bar{E}$

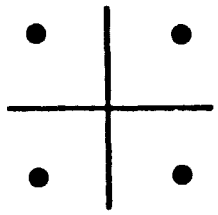


$M=64$

$P[E] \sim 4Q\left(\sqrt{.28\bar{E}_b/N_0}\right)$

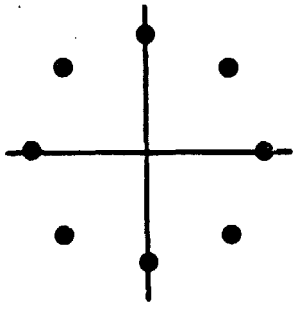
$E_p = 2.3\bar{E}$

Figure 2.1a Rectangular 2-D Constellations



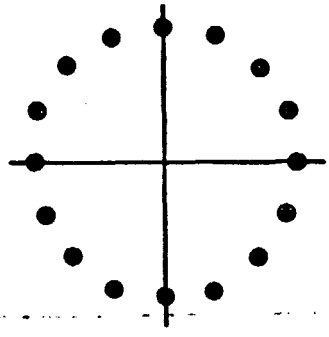
QPSK

$$P[E] \sim 2Q\left(\sqrt{2\bar{E}_b/N_0}\right)$$



8PSK

$$P[E] \sim 2Q\left(\sqrt{0.88\bar{E}_b/N_0}\right)$$



16PSK

$$P[E] \sim 2Q\left(\sqrt{0.59\bar{E}_b/N_0}\right)$$

Figure 2.1b PSK Constellations

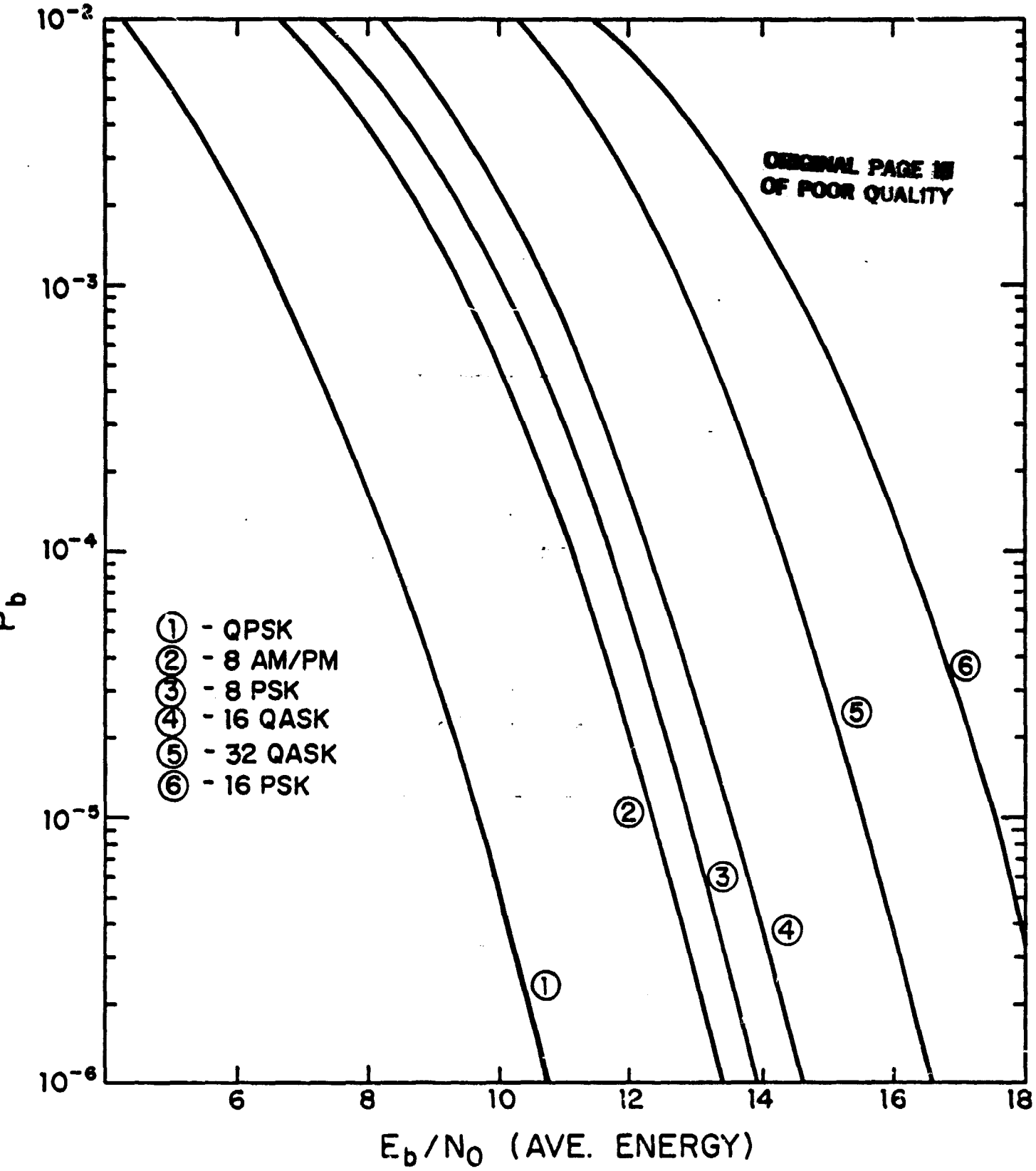


Figure 2.2 Error Performance with Quadature Modulation Schemes

QPSK is the most energy efficient, with 16-PSK requiring about 8 dB more E_b/N_o (average). Several of the schemes have amplitude modulation, and the energy per symbol varies. We have thus plotted performance versus average energy rather than peak energy.

Relative bandwidth of these schemes is easily obtained by observing that if the same quadrature waveshapes are used at the modulator, then the relative bandwidths go as $1/\log_2 M$. For NRZ modulation, the spectra are $\sin^2(x)/x^2$ in form with null-to-null bandwidths given below, with R designating the bit rate.

	B_{n-n}
QPSK	R
8-PSK, 8 AMPM	(2/3)R
16-QASK, 16 PSK	R/2
32-QASK	(2/5)R

Post-modulation filtering would typically be used to remove spectral sidelobes since the sidelobes diminish only as $|f-f_c|^{-2}$.

Pulse-shaping can be used to improve the spectral efficiency. In QPSK systems, spectral raised-cosine shaping with roll-off of 50% is commonly used to provide (ideally) bandlimited signals. In this case the bandwidths are

	B
QPSK	(3/4)R
8-PSK, 8 AMPM	(1/2)R
16-QASK, 16-PSK	(3/8)R
32-QASK	(3/10)R

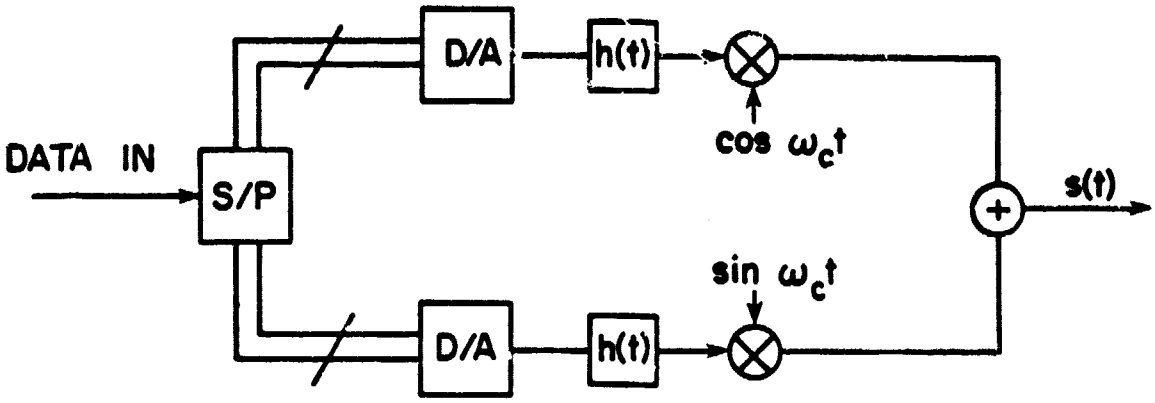
Such shaping is more difficult to implement at high speeds and introduces amplitude-variation into schemes which are ordinarily constant-envelope with NRZ, viz, QPSK and 8-PSK.

Figure 2.3 depicts the general modulator/demodulator diagram for quadrature-modulation schemes, with the necessary synchronization circuitry not shown. It is sometimes advantageous to use staggered modulation whereby the Q channel transitions occur a half-interval displaced from those in the I channel. This improves spectral behavior for NRZ/QPSK on nonlinear channels; for the other schemes staggering has less benefit, as quasi-linear operation is assumed by definition for say 16-QASK.

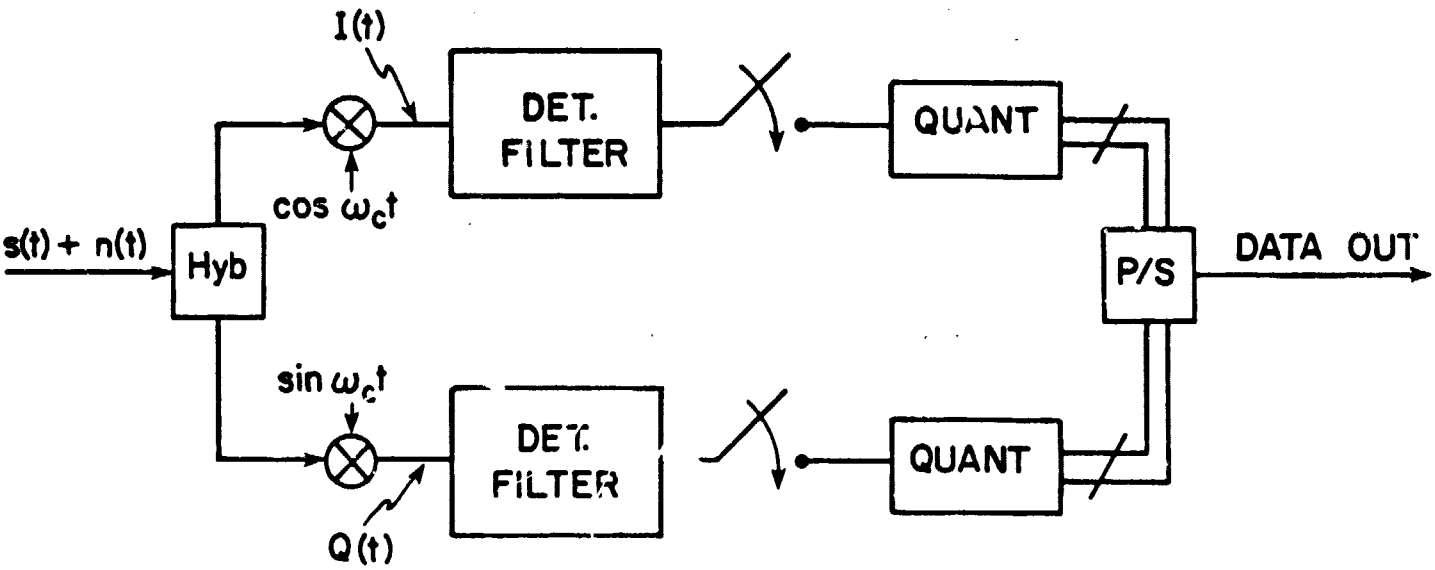
QORC (quadrature-overlapped raised-cosine) modulation [1] is a related technique which uses staggered raised-cosine pulses lasting two intervals in the I/Q channels. This gives a spectrum with essentially no significant sidelobes and mainlobe comparable to that of NRZ/QPSK. A mild intersymbol interference results however, penalizing the detection efficiency by about 1 dB. The envelope ripple for this scheme is held to 3 dB. The same modem structure may be used as in Figure 2.3 with appropriate change of pulse shapes or data filters.

A second general class of modulation is the <u>continuous-phase modulation</u> (CPM) family. These signals are constant-envelope by definition and thus attractive for satellite channels. By smoothly modulating the phase of the carrier, very attractive spectra can be obtained with no post-modulation filtering. These schemes are described by

$$S(t) = A \cos(\omega_c t + \phi(t,d)), \quad nT \le t \le (n+1)T$$



Modulator



Demodulator

NOTES: 1) h(t) is optional spectrum shaping filter

2) quadrature channels may be symbol-staggered

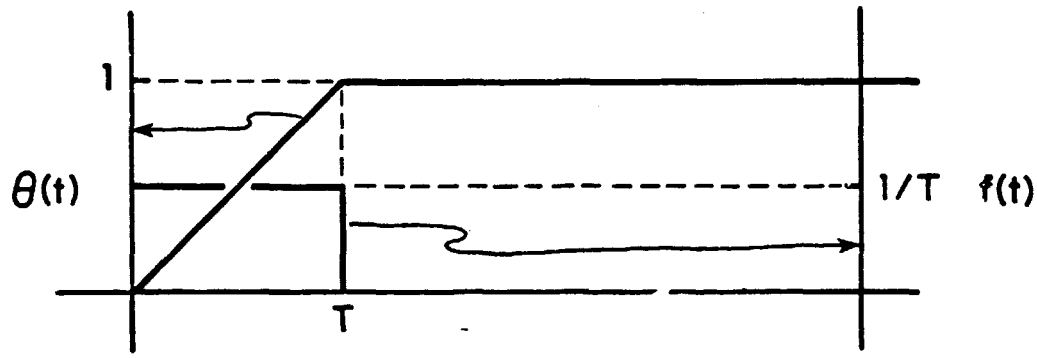
Figure 2.3 General Quadature Modulator Processor

where

$$\phi(t,d) = \sum_{j=1}^{n-1} d_j \, h\pi \, \theta(t-nT),$$

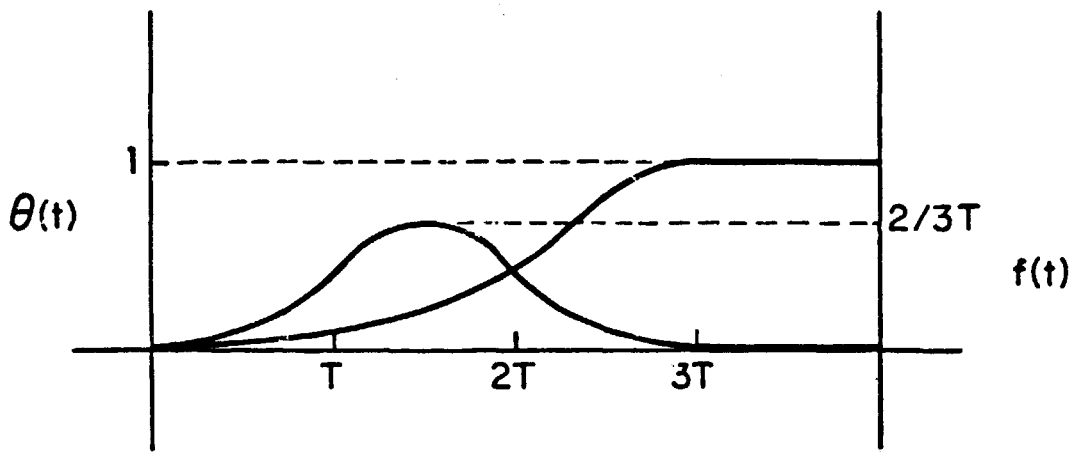
d is the data sequence, h is the modulation index, and $\theta(\bullet)$ is the phase shaping pulse lasting LT seconds. Examples are shown in Figure 2.4 for CPFSK and 3-RC.

The intrinsic memory present in the modulator suggests that a demodulator could exploit this "coding" to improve energy efficiency over a single-interval demodulator. Further, when h is a rational number, the signal may be described by a finite-state trellis, and the Viterbi-demodulator applied to do bit detection. In general cases, this receiver is probably too complex to implement at the rates assumed here, as 16 to 64-state trellises coupled to a correlator bank are typical. In the special case of binary transmission with h = 1/2, however, we are able to utilize rather simple receivers. This is because the quadrature components of the phase modulated signal exhibit an eye-pattern opening every 2T seconds; this has been known for some time for MSK, which is binary CPFSK with h = 1/2. A "parallel" MSK receiver is shown in Figure 2.5a, with a "serial" version shown in Figure 2.5b. Aulin et al. [2] have shown that the use of the MSK receiver may be used on other binary h = 1/2 CPM schemes, e.g. 2-RC and 3-RC. The detection loss due to ISI is amazingly low: 0.1 and 0.7 dB relative to the Viterbi-receiver, respectively. When coupled with the constant-envelope and low sidelobes, this represents a potentially attractive high-speed technique. An MSK receiver has been synthesized at 760 Mbps using SAW devices and microstrip techniques previously [3]. The serial version of



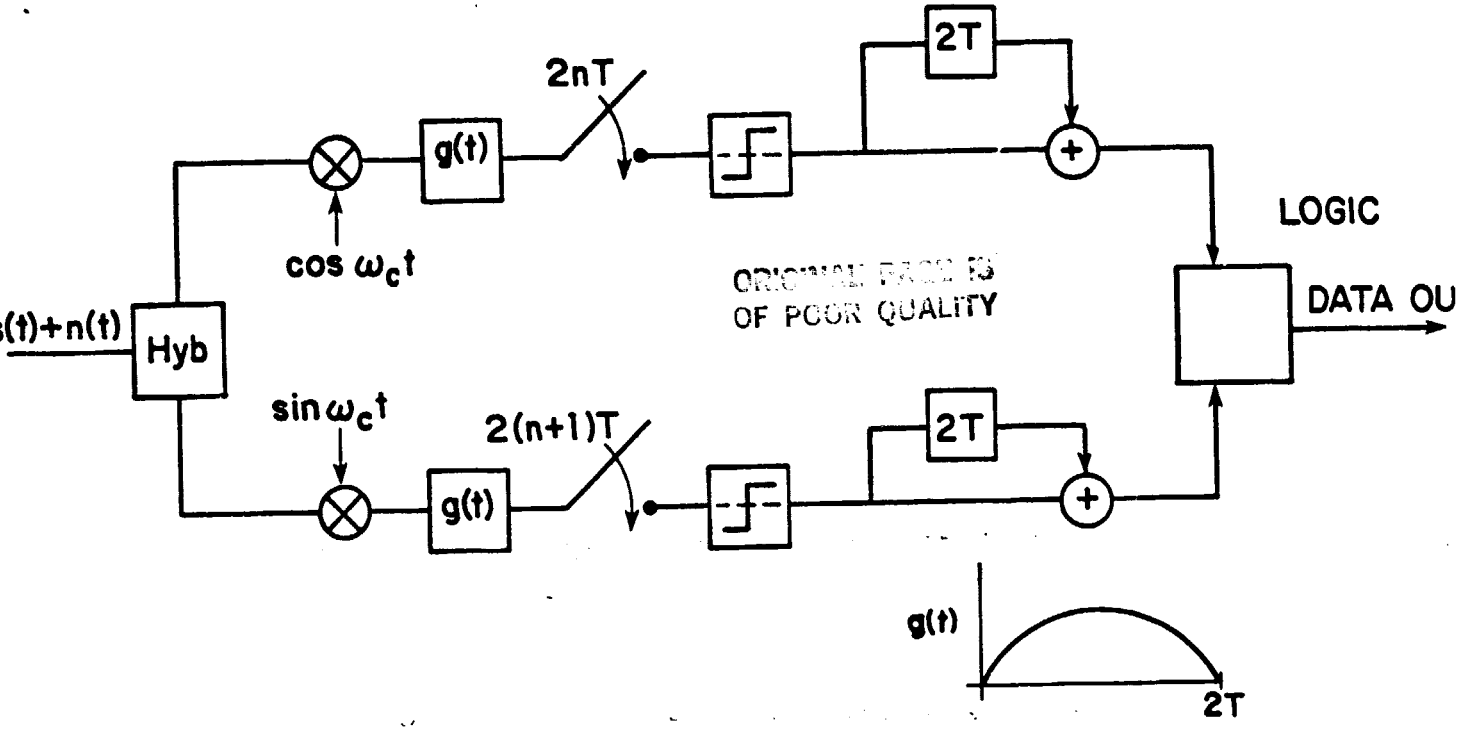
CPFSK Phase Pulse and Frequency Pulse

$$\theta(t) = \int_0^t f(\tau)\, d\tau$$

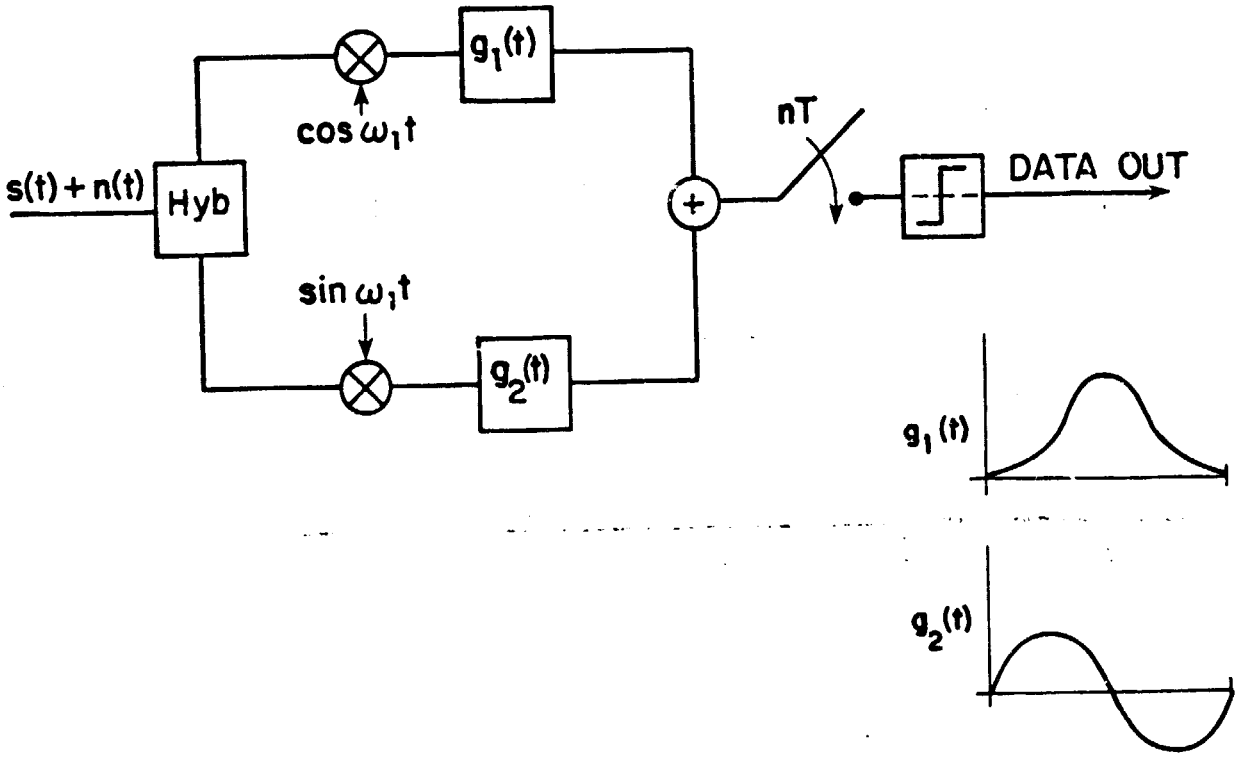


3-RC Phase Pulse and Frequency Pulse

Figure 2.4 CPM Shaping Pulses



"Parallel" Receiver



"Serial" Receiver

Figure 2.5 MSK-Type Receivers

the receiver uses two different filters and a single sampler/comparator. Its complexity is comparable to that of the parallel version but it exhibits high robustness to phase error [4]. The eye pattern remains rather wide-open for phase offsets up to 30°, provided the sampling time is adjusted to compensate.

Tamed FM (TFM) [5] is a partial-response FM scheme designed for ultra-low spectral sidelobes, the name derived from the fact that the modulating signal is a tamed (less wild) version of better known cases. Reference [5] shows a quadrature-type receiver which operates about 1 dB degraded from QPSK efficiency. The pulse shaping necessary to attain the desired spectrum is rather precise, however, and further study is required to assess TFM's utility at very high bit rates.

Figure 2.6a and 2.6b show the power spectral densities of QORC, MSK, 2-RC (h=1/2), 3-RC (h=1/2), and tamed FM versus normalized frequency. As the modulating pulse becomes smoother, we see a dramatic drop in sidelobe levels, with no appreciable change in mainlobe bandwidth.

In summary, the quadrature modulations are simplest to instrument and offer a range of energy and spectral efficiencies. CPM has many attractive properties for bandwidth efficient modulation, but is saddled by complex receivers in the general case. For a special case of binary, h = 1/2, receivers are rather simple and if the energy/spectrum objectives match this case, then CPM provides a good solution. In this case, one perspective on the signal is that it is a partial-response-like quadrature modulation, hence the simpler receivers. This is not

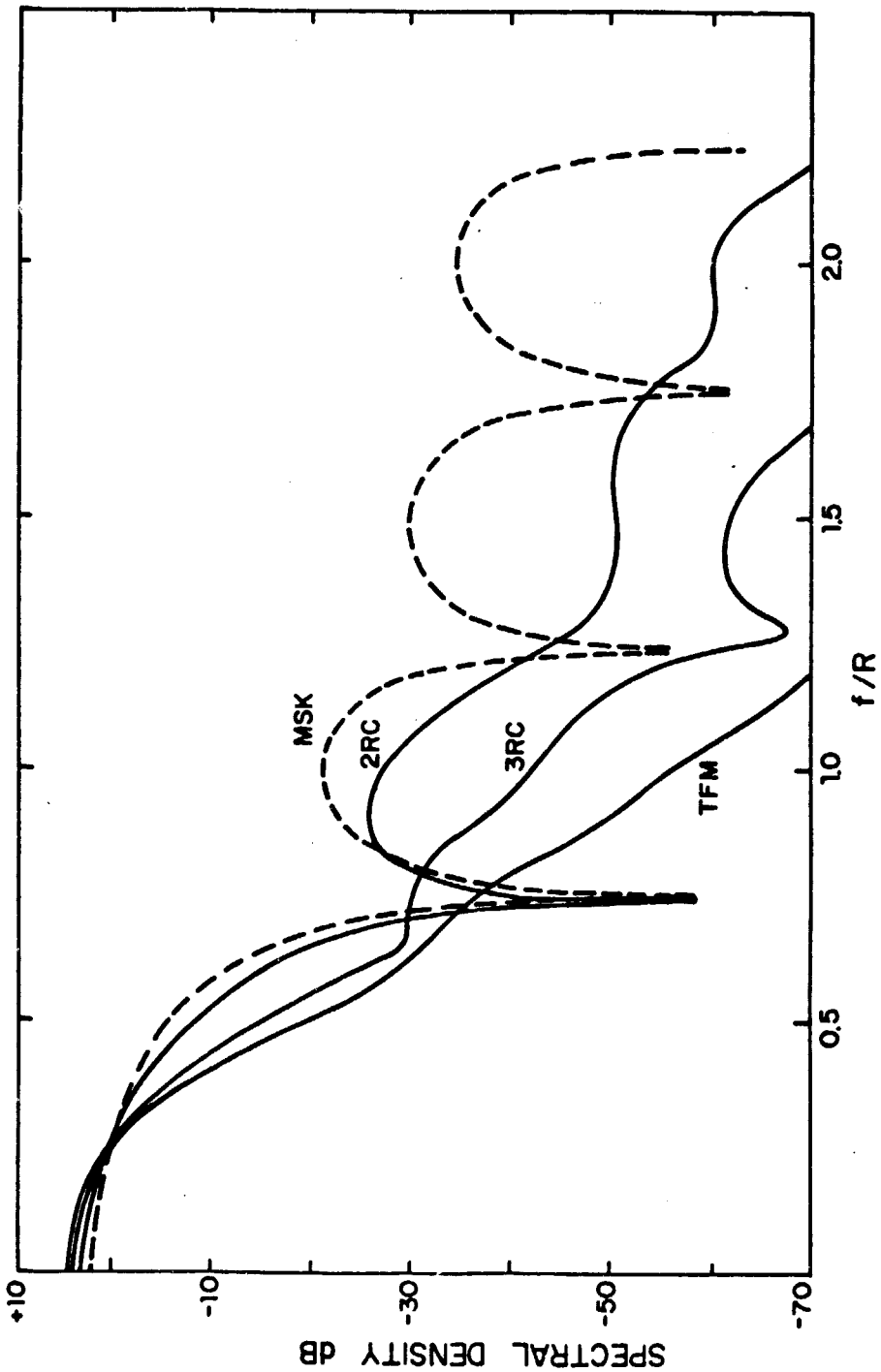


Figure 2.6a Spectra of CPM Signals, h=1/2

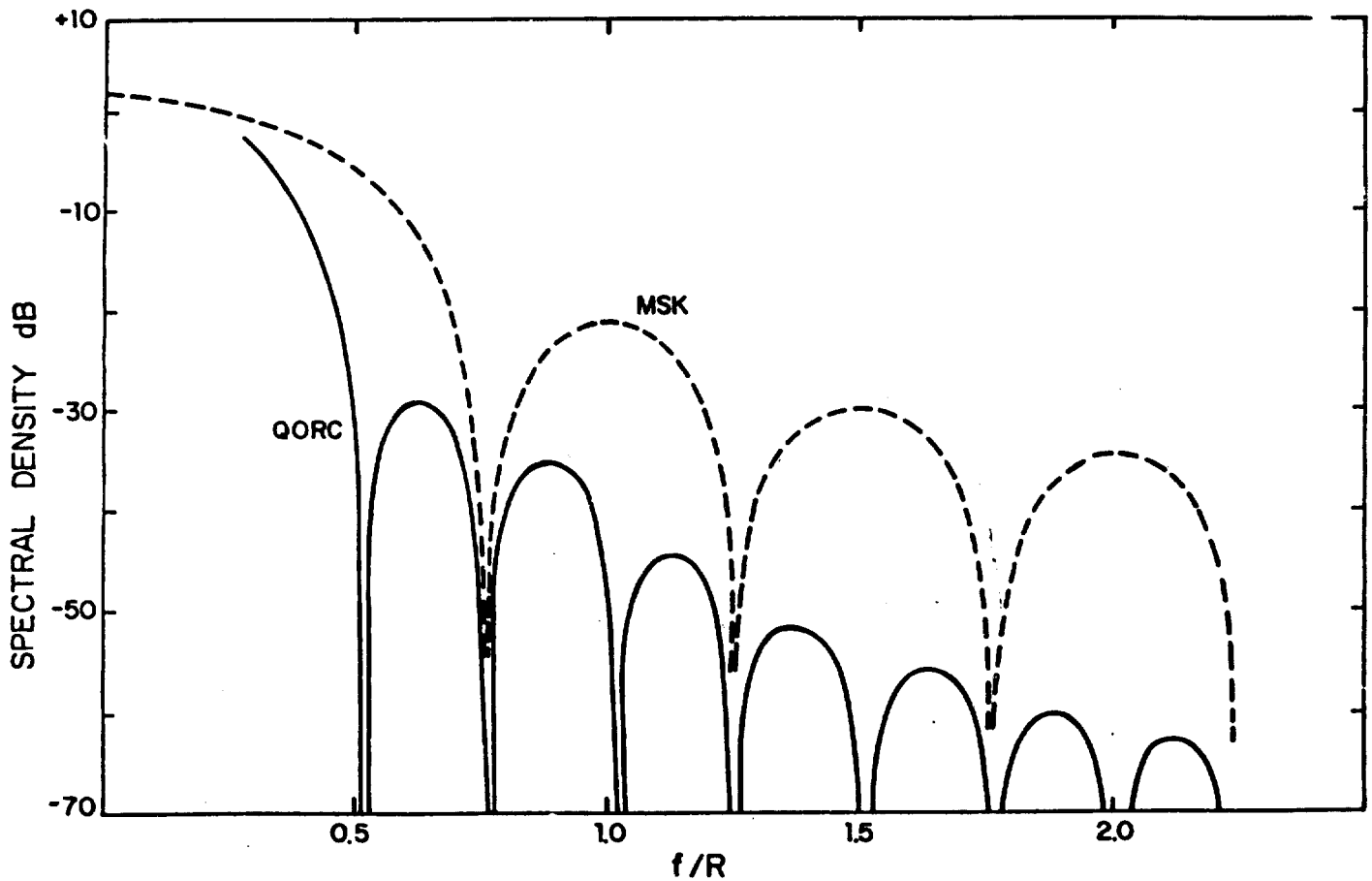


Figure 2.6b Spectra of Quadature Overlapped Raised-Cosine Modulation

strictly correct due to the cos(•) and sin (•) nonlinearity, but sufficiently close that quadrature receivers work well.

2.2 CODING

Forward error control coding is the general technique of inserting redundancy and memory into the transmitted signal, which when exploited by the decoder, will generally provide "coding gain," a savings in E_b/N_o required to achieve a given probability of error. This is in exchange for bandwidth expansion (relative to uncoded transmission with the same modulator) and for increased receiver complexity.

We have focused upon convolutional codes for out study (versus block codes) as being more flexible, since no blocklength need be assumed, and because they are widely regarded as being more powerful for a given complexity level than block codes. Part of this advantage is the ease of doing soft-decision decoding.

Among the ways of decoding convolutional codes, the threshold decoding and Viterbi decoding methods represent the simplest and most complicated methods. We describe the performance of these next as applied to the present investigation.

2.2.1 Convolutional coding with threshold decoding

Threshold decoding [6] represents a simple decoding procedure for decoding of convolutional codes. The technique utilizes systematic codes, with syndrome bits formed by comparing regenerated parity bits with those actually received. When a certain number of syndrome bits exceed a threshold, the decoder infers an error has occurred and corrects the bits about to emerge from a temporary buffer. Since only shift registers and simple gates are needed and the architecture is

pipelined, the decoder can operate as fast as the logic devices permit. Consequently, we briefly investigated application of threshold decoding for very-high-throughput channels.

Normally, the encoded bit stream is used to binary-modulate the carrier, with binary detection at the receiver. This implies a bandwidth expansion of n where the rate is 1/n. In the special case of r = 1/2 coding onto QPSK, we have bandwidth the same as that of uncoded BPSK, and with gray-coding, the detection performance is the same as with binary signalling. Performance for the r = 1/2, QPSK case is shown in Figure 2.7 for several different codes. RJ is the number of orthogonal syndrome checks employed. As a measure of complexity, the shift registers of the encoders and decoders are of length 6, 17, 35, and 55 bits for RJ = 4, 6, 8, and 10, respectively. The results show that the coding gains are rather small at 10^{-5}, between 1 and 2 dB. The results shown are for "definite" decoding; feedback decoding, which removes the effect of "corrected" bit errors from the syndrome register, gains about 0.5 dB more at a slight loss in speed due to feedback requirements.

We also evaluated threshold decoding for r = 2/3 coding onto 8-PSK, with hard-decision decoding assumed. (The usual viewpoint would be to use three serial binary transmissions.) The results were surprisingly poor, however. The qualitative understanding is that by introducing coding, we have diminished greatly the minimum distance between signals (BPSK versus QPSK), giving a sharp increase in symbol error rate. The redundancy built into reasonable codes is not sufficient to overcome this loss, and a net coding loss is found for

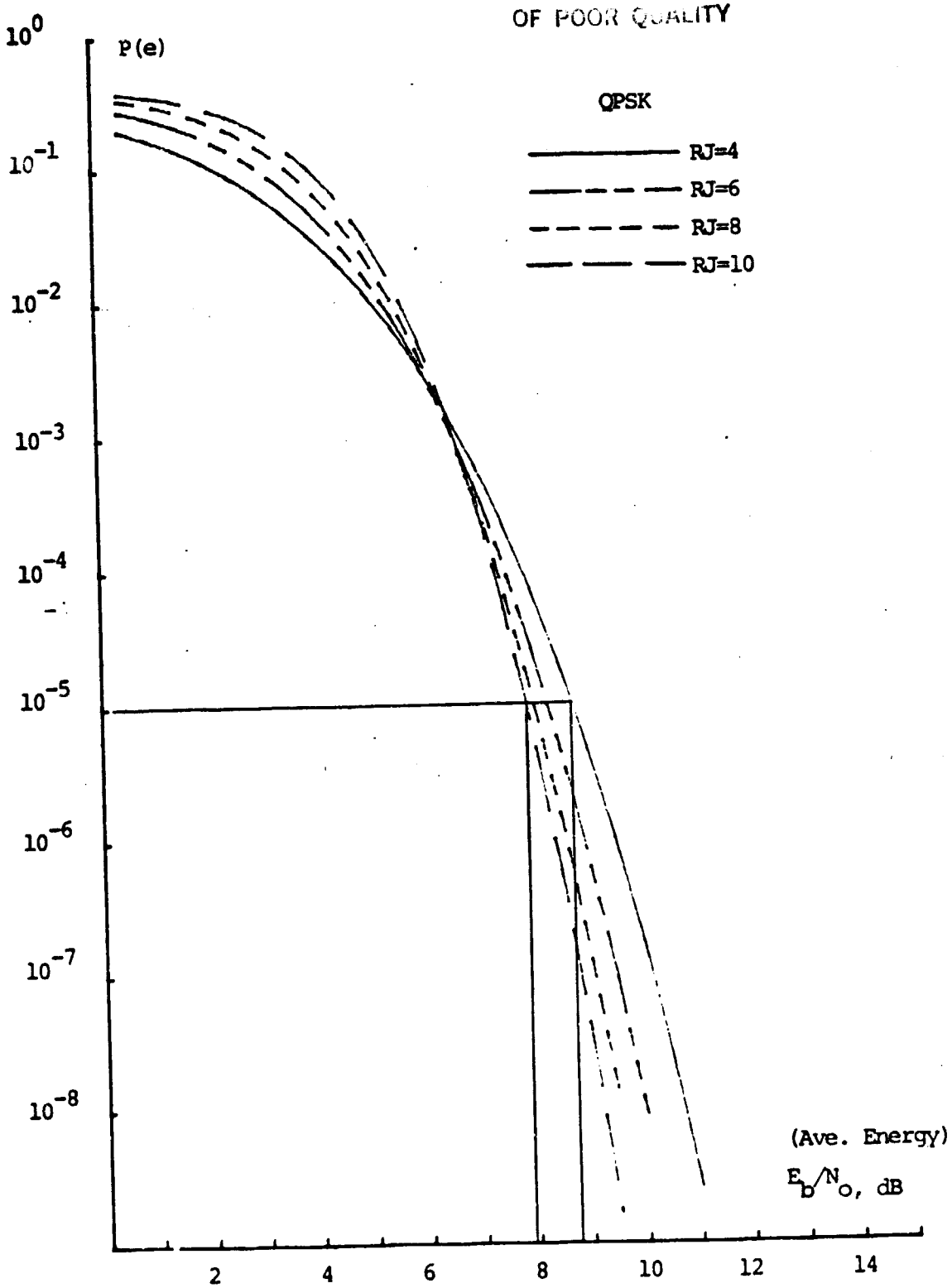


Figure 2.7 Performance of R = 1/2 Coded QPSK with Threshold Decoding

codes with up to 10 syndrome checks. (This is measured against uncoded QPSK, having the same bandwidth; the technique does gain 2-3 dB over uncoded 8-PSK however.)

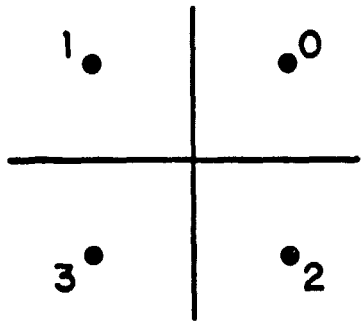
It is possible to perform a soft-decision variation of threshold decoding, providing a gain of nearly 2 dB over hard-decision decoding. This complicates the decoder significantly however, requiring arithmetic operations. At this level of complexity, maximum likelihood (trellis) decoding is probably preferable.

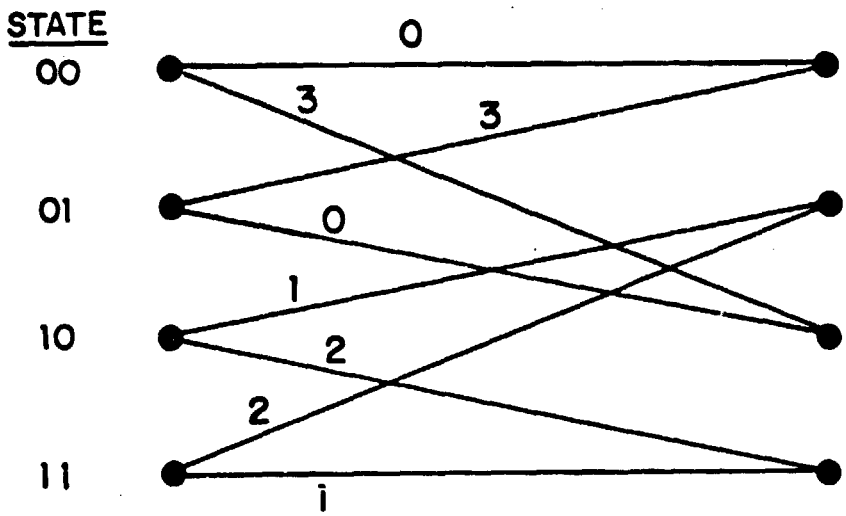
To summarize, threshold decoding gives modest gains for QPSK, but does not mate well with bandwidth efficient modulations such as QASK. Although we have not specifically evaluated the technique with $r = 3/4$ coding onto QASK, the above effect is even worse than for 8-PSK.

2.2.2 Maximum likelihood decoding

Use of the Viterbi algorithm for decoding of convolutional codes is a well-known technique for attaining energy savings on space channels. The complexity of the algorithm depends exponentially on the number of delay or memory cells in the convolutional encoder. We describe 4-state encoder/decoder structures for both QPSK and QASK modulation, a compromise between achievable speed/complexity and coding gain. With 4-states, we can attain about 4 dB improvement in both cases relative to an uncoded modulation having the same bandwidth.

With QPSK modulation, the optimal Hamming distance codes provide the optimal codes in signal space by virtue of the simple antipodal modulation in each quadrature channel. The optimal 4-state (constraint length 3) QPSK code is shown in Figure 2.8a with its associated trellis diagram. The asymptotic probability of bit error





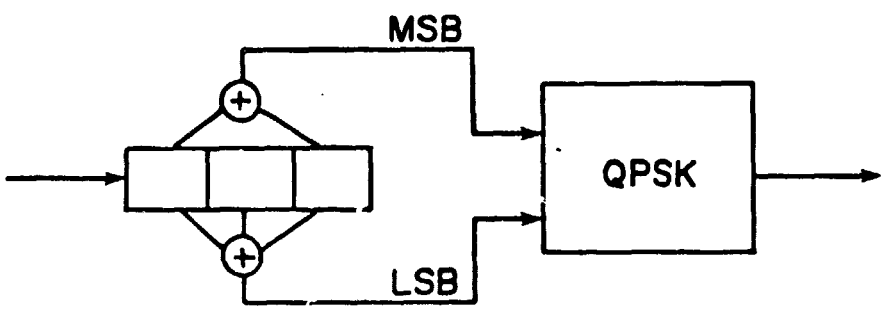


Figure 2.8a. Optimal r=1/2 4-State Code With QPSK

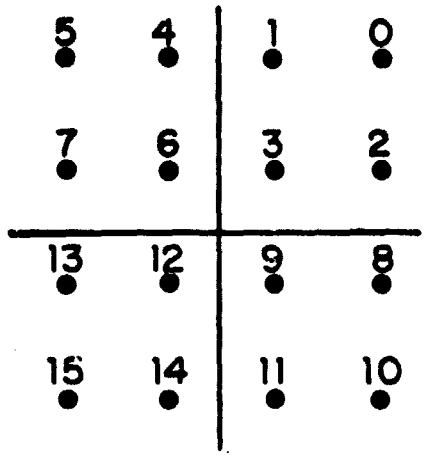
expression for this case is

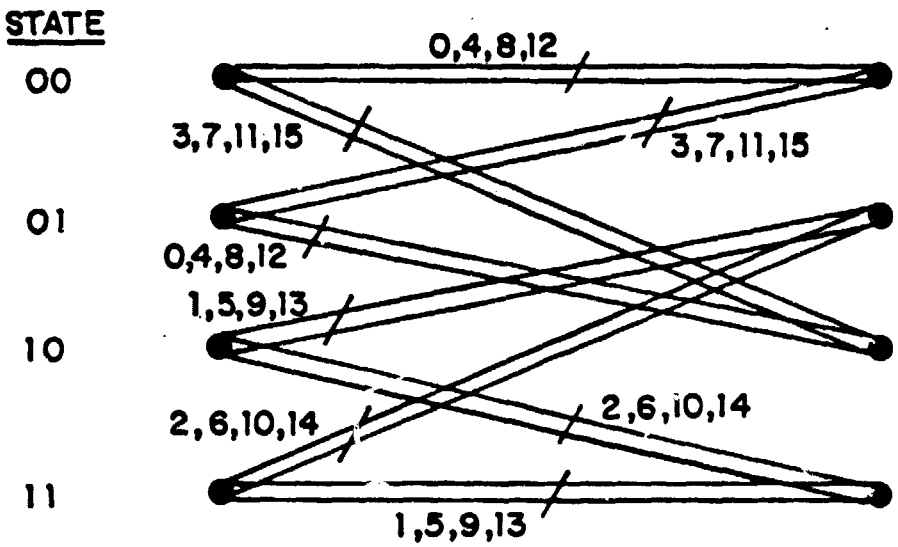
$$P_b \sim Q(\sqrt{\frac{5E_b}{N_o}})$$

which represents a 10 log (2.5) = 4 dB gain over binary PSK, a scheme which has the same bandwidth. (Q(x) denotes the Gaussian integral, sometimes denoted erfc(x).)

For QASK, Ungerboeck [7] produced optimal r = n/n+1 codes, from which the 4-state code is selected for Figure 2.8b. Note we are coding three information bits onto four code symbols, and treat these as a 16-ary symbol. This scheme has the same bandwidth as uncoded 8-PSK, but a coding gain of 4 dB. The trellis labeling of Figure 2.8b pertains to the signal indexing shown in the 16-ary constellation. The ML processor must now score eight paths entering each state, and three-bit wide path maps must also be stored for each state.

Of special interest is the unusual similarity between the encoders and trellis structures for the QPSK and QASK codes. We see that in the r = 3/4 coded case, two of the data bits merely modulate the high-level of a two-level QPSK arrangement, while the third bit is encoded into the low-level in <u>exactly</u> the same fashion that it was in the coded r = 1/2 case. Thus no changes are required to the encoder logic in switching between these modes. Furthermore, the Viterbi decoder architecture is remarkably similar in both cases. By observing that in the coded QASK case that paths enter the states in QPSK groups, we note that a "hard" QPSK decision can be made among each group, and the metric of the winner used to accumulate with previous metrics.





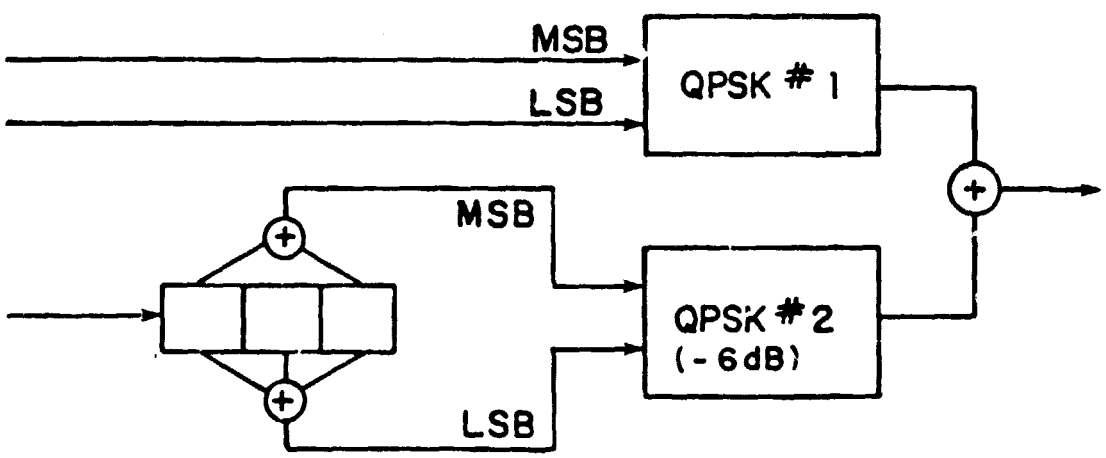


Figure 2.8b. Optimal r=3/4 4-State Code With 16-QASK

We have not undertaken a detailed configuration of the Viterbi decoder in an IC framework, but note that single chip decoders have been constructed for r = 1/2 coded QPSK (or MSK) under NASA sponsorship [8]. These chips operate presently in the 10 Mbps throughput range, and by paralleling, can attain a 200 Mbps throughput. Silicon NMOS technology was used for this development. The constraint length was 5 bits, implying a 16-state decoder; this is roughly a factor of four more complex than the codes described above. We also believe that "analog" Viterbi decoding [9] has merit for further study, especially at high speeds and for shorter codes. Metrics are stored as voltage on a capacitor in this technique, and voltage comparators provide metric comparisons. In addition, no high-speed A/D converter between receiver and decoder is needed.

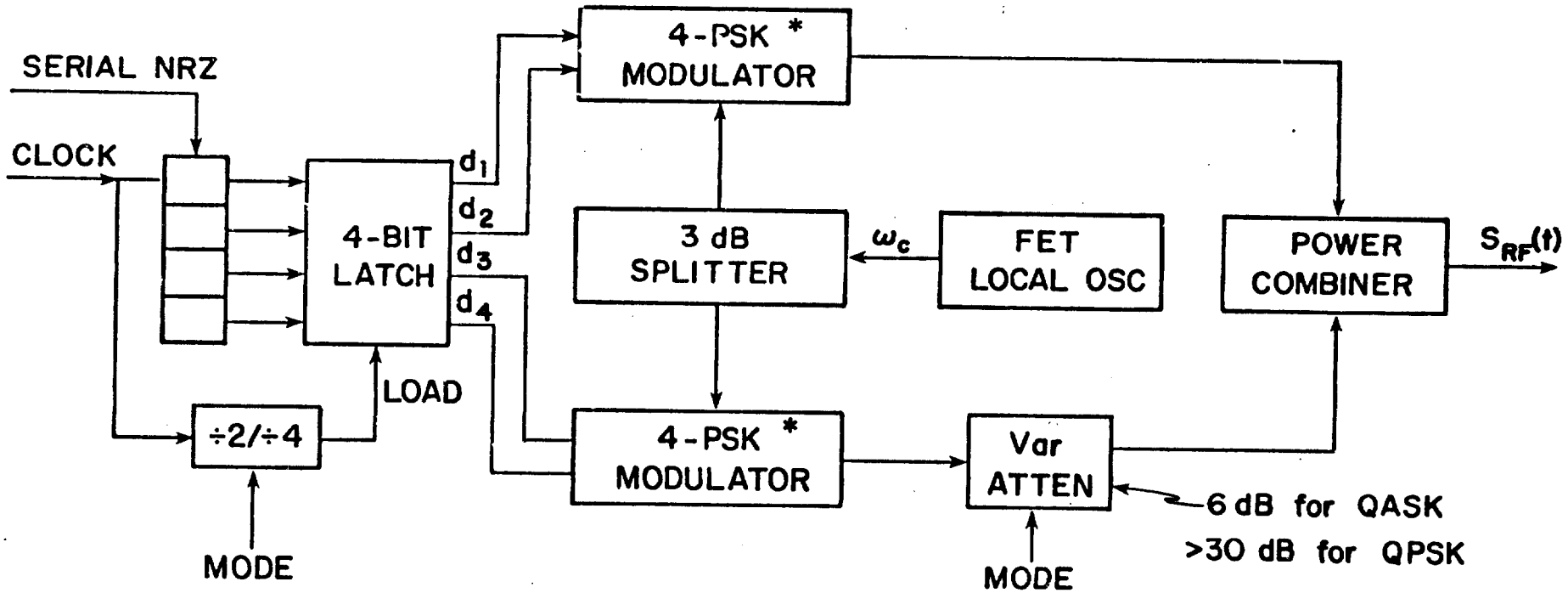
2.3 A MILLIMETER-WAVE GaAs MONOLITHIC DUAL MODEM

We describe a high-speed dual-mode modulator/demodulator architecture for digital satellite communications capable of being fabricated entirely in monolithic gallium-arsenide technology. The technique is referred to as "dual-mode" as it is capable of selectively performing QPSK (quadriphase shift keying) or QASK (quadrature amplitude shift keying), providing a flexibility to meet varying communications requirements with a high-degree of commonality of hardware. We have configured the modem around a nominal throughput of 2 Gbps, using carriers in the 20-30 GHz region, with applications to satellite TDMA trunks or to terrestrial digital radio. These choices are rather flexible however, and the technique could provide a low-cost solution for modems operating at lower rates, e.g. the 1.544 Mbps T1 rate.

The technique to be described has two principle attributes. First, it exhibits a natural marriage of two popular communications techniques which provide a choice of power and spectral efficiencies with essentially common circuitry; this is by virtue of the fact that QASK can be treated as a layered or superposed QPSK modulation. Second, we have emphasized the ability to implement the technique in GaAs monolithic circuit form, and find that all functional blocks are certainly capable of being so fabricated, or in some cases already have been in various research laboratories.

By referring to Figure 2.1, we may see that the 16-QASK signal constellation may be realized in two steps: first, travel from the origin to a location centered in one of the four quadrants, then make another 45 degree travel from that point to one of the 16 signal locations. This process is forming the sum of two QPSK signals, one being half the amplitude or one-fourth the power of the other. This technique has been called superposed modulation, or layered modulation. Because of this property, QASK can be synthesized using two identical QPSK modulators, and QPSK and QASK are highly compatible modulation formats. It is further possible to synthesize 64-QASK using three levels of QPSK in this manner, but this is not of interest here.

This simple property led us to study the details of a dual-modem implementation, one capable of performing either modulation with minor reconfiguration. The basic diagram of the modulator is shown in Figure 2.9, where input serial bits are converted to 2- or 4-bit bytes and fed to two QPSK modulators. If one desires QPSK transmission, the output of the second modulator is merely attenuated by a large amount. Though



* 4-Phase modulator can be realized with path length modulator or dual-gate FET phase shifter

Figure 2.9 Diagram of Dual-Mode Modulator

this small amount of power is wasted (modulation is at a low level) the bits are not lost because the serial-to-parallel converter outputs bits every two bit times. Alternatively, for QASK transmission, the second modulator is attenuated by 6 dB and added to the first modulator output. It is important that this power balance be reasonably accurate, and that the two modulator outputs be combined with the correct phase. More performance detail is given in Chapter 3.

We assume the modulator operates at a fixed symbol rate in either mode, as opposed to a fixed bit rate. This is for reasons of receiver simplification. For example, if we specify a symbol rate of 500 Msps, then the bit rates are 1 Gbps for QPSK and 2 Gbps for QASK. This also means the transmitted signal maintains fixed bandwidth in either mode, and because of the 4 dB difference in energy efficiency shown earlier, in going to QASK we must assume a link capable of providing 7 dB better SNR than that used for QPSK.

The receiver is a standard quadrature demodulator, with two-level decisions in each channel for QPSK and four-level decisions for QASK. Figure 2.10 illustrates this receiver in two parts, first showing the RF-to-baseband conversion process, then the more intricate detection and synchronization circuitry. (This partition is partly conceptual, but also a logical partition should one implement the demod in locks (chips).) Though not indicated, differential encoding and decoding is necessary to resolve a phase ambiguity occurring in the carrier synchronization loop. We describe the synchronization method(s) in more detail in the following section.

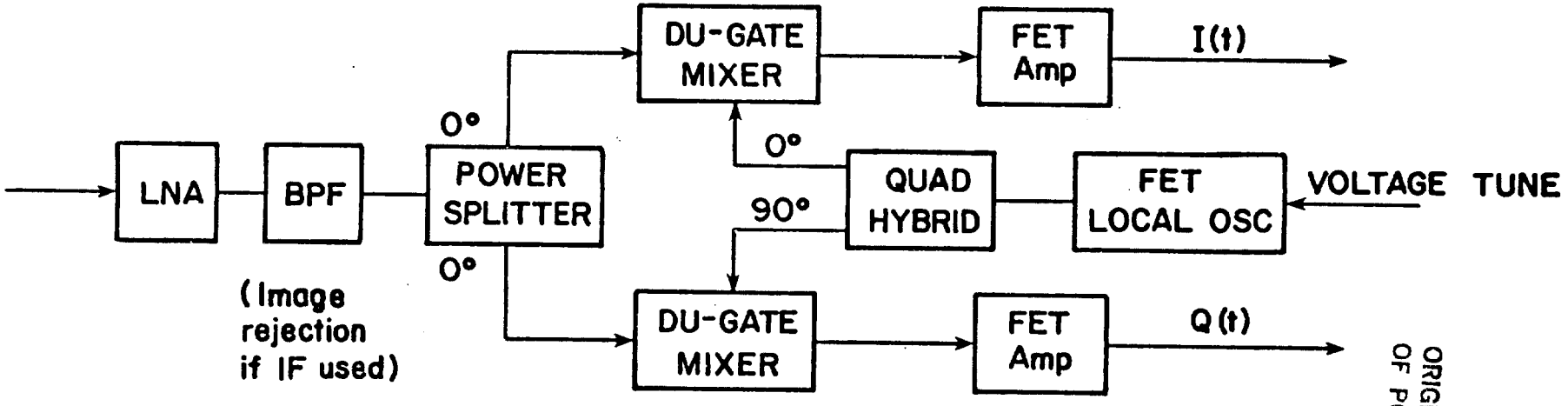


Figure 2.10a MMIC General-Purpose Quadrature Demodulator

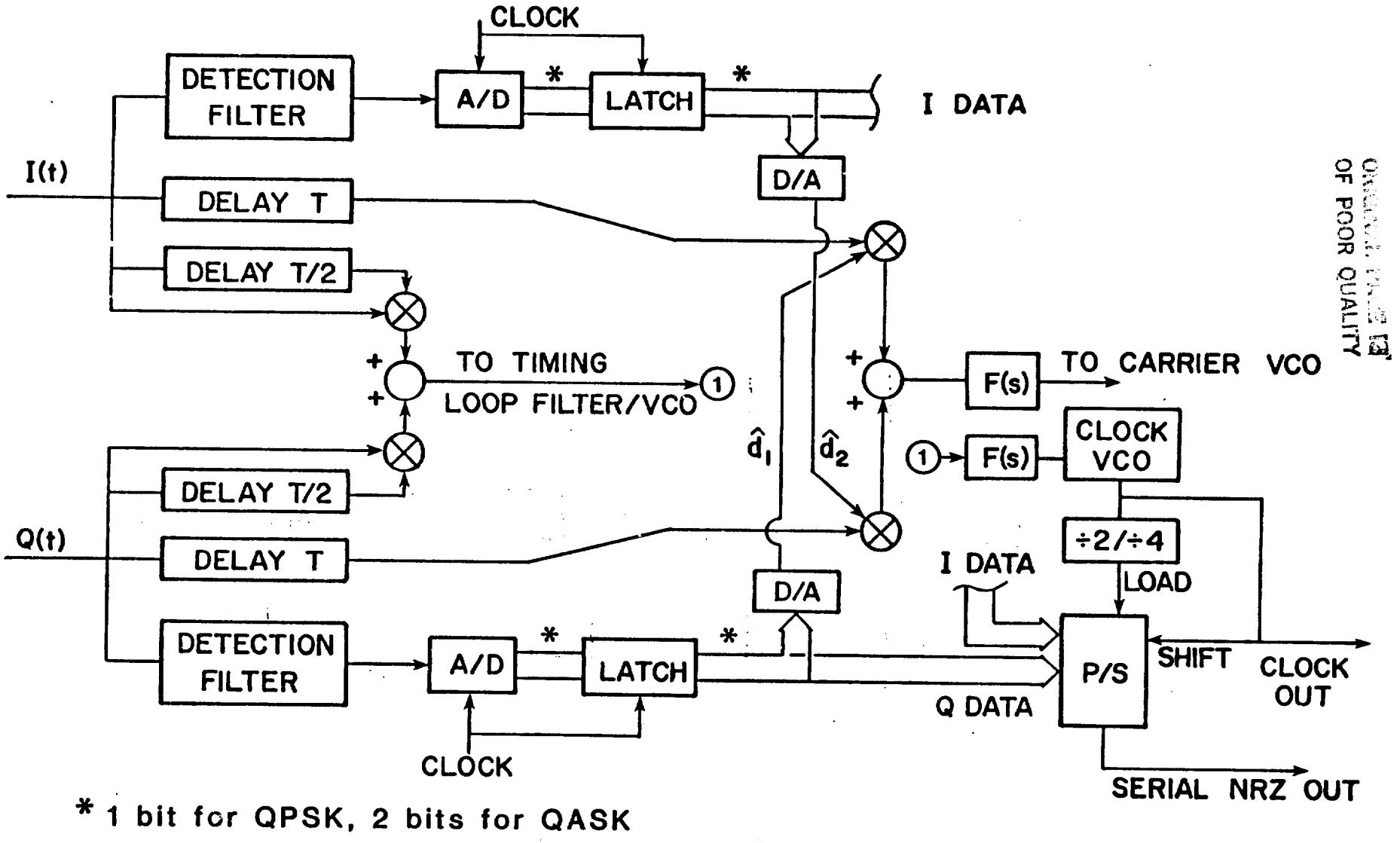


Figure 2.10b Baseband Processor Diagram (Detection, Carrier Synchronization, Symbol Timing)

Ideal data detection, assuming a non-distorting channel, is performed by a matched filter in each channel, followed by a sampler/quantitizer. For the case of NRZ pulse shapes, the integrate-and-dump filter is ideal, but difficult to realize at high speeds; suboptimum passive filters will perform quite near ideal if the bandwidths are chosen appropriately. For pulse-shaped transmission, such as use of raised-cosine (in frequency) pulses, the receiver filter also should have the same response. Again realization of the desired response for high data rates is a design challenge.

In Tables 2.1 and 2.2, we specify the general performance requirements of the various elements of the modulator and demodulator as general inputs to a detailed implementation study.

2.4 SYNCHRONIZATION FOR DUAL-MODE RECEIVER

Carrier phase and symbol timing must be extracted from the received modulated carrier signal. It is important that these parameters be estimated accurately to avoid significant energy degradation, yet with simple algorithms to provide ease of implementation. Commonality of techniques for the two modes is also crucial.

2.4.1 Carrier synchronization techniques for dual-mode receiver

Decision-feedback synchronizers are assumed because of their better performance in noise (lower phase jitter) and the technique generalizes to a variety of quadrature modulation techniques, QPSK and QASK among them. Essentially, the receiver estimates the data and remodulates or removes its effect from a delayed replica to obtain an error signal proportional to phase offset, but not dependent on the data. This process is convergent; if carrier phase error is initially

TABLE 2.1. Modulator Performance Parameters

- 500 M symbols/sec, corresponding to 1 Gbps for QPSK, 2 Gbps for QASK
- interface logic capable of 3 GHz clock rate
- center frequency: selectable in 10-30 GHz range
- frequency stability of oscillator: $\Delta f/f < 5 \times 10^{-6}$ or 100 KHz at 30 GHz
- power output: 0 dBm into 50 Ω, VSWR < 1.5:1
- quadrature phase accuracy to within ±2°; amplitude balance within 0.5 dB
- 2nd layer modulation 6 dB ± 0.5 dB lower in power
- NRZ modulation, bandpass filtering at RF assumed to lower spectral sidelobes, if necessary
- entire modulator on chip; possible off-chip dielectric resonator for FET local oscillator

TABLE 2.2. Demodulator Performance Parameters, MMIC #1

LNA:	f_c = 10 to 30 GHz (TBD) noise figure: 2 to 4 dB, dependent on frequency gain: 25 dB, 3 stages
BPF:	f_c: TBD bandwidth: 2 GHz insertion loss over passband: < 2 dB
Power Splitter:	power split within ±0.5 dB phase equality within ±2°
Dual-Gate Mixer:	conversion gain: +3 dB
FET Video Amp:	bandwidth: 10 KHz - 2 GHz, ±1 dB gain: 50 dB
Quadrature Hybrid:	power split within ±0.5 dB quadrature phase within ±2°
FET Local Oscillator:	f_c (TBD, at designed carrier frequency) voltage tuning range: ±10 MHz, roughly 0.05% of f_c power output: +10 dBm into 50 Ohms phase noise: -90 dBe 10 MHz from f_c frequency stability: $\Delta f/f < 10^{-5}$ over 0-50°C VCO sensitivity: 1 MHz/volt

Demodulator Performance Parameters, MMIC #2

General:	Circuit uses decision-feedback synchronization for carrier with 2-level or 4-level detection in each quadrature arm as appropriate. For additional information on the synchronization technique, see Simon and Smith [10].
Delay Lines:	Bulk delay of one symbol interval, e.g. 2 nsec; delay should be "constant" over 1 MHz to 1 GHz.
Detection Filters:	For NRZ transmission, would ideally be integrate-and-dump, but at high speeds, distributed-circuit low-pass filters with $B \sim 1/T_s$ may be used.

TABLE 2.2 (Continued)

Voltage Comparators:	Binary or 4-level flash converters using biased FET comparators; conversion-time on order of (1/2) T_s. Outputs are decoded and latched, then serialized for data bus.
Multipliers:	Several alternatives are under study. A true analog multiplier is generally shown, but it is possible that one or both of the inputs can be binary quantized, allowing use of logic gates to form the error signal.
Loop Filter:	Active filter providing $F(s) = (s+a)/(s+b)$, $b \ll a$, response. The constant a, along with loop d.c. gain, determines the loop bandwidth, typically on order of 10 MHz.

high say 30°, the temporary error rate is quite high but on the average corrections are in a direction to reduce phase error, which in turn improves the symbol error rate.

A decision feedback receiver for QPSK/QASK is shown in Figure 2.11 [10]. To analyze performance, we first assume the QPSK case, and write the received signal as

$$r(t) = \sqrt{2}(d_1(t) \cos \omega_c t + d_2(t) \sin \omega_c t) + n(t)$$

with $d_1(t)$ and $d_2(t) = \pm A$. For future use, the received symbol power is $2A^2$. We assume $n(t)$ is bandpass Gaussian noise with two-sided spectral density $N_o/2$ w/Hz. Using the bandpass representation:

$$n(t) = \sqrt{2}(n_c(t) \cos \omega_c t + n_q(t) \sin \omega_c t)$$

where $n_c(t)$ and $n_q(t)$ are low-pass independent Gaussian processes with spectral density $N_o/2$ also.

The signal at (1) in Figure 2.11a is $d_1(t)\sin\phi + d_2(t)\cos\phi + n_c(t)\sin\phi + n_q(t)\cos\phi$ which indicates some crosstalk when ϕ, the phase error, is nonzero. Likewise the signal at (2) is $-d_1(t)\cos\phi + d_2(t)\sin\phi - n_c(t)\cos\phi + n_q(t)\sin\phi$.

Now assume in each channel we make polarity decisions by comparing with zero volts. In the I channel we decide d_2 correctly with probability $1 - P_e$ and likewise d_1 is decided in channel 2. At (3) we have

$$e_3(t) = d_1(t)\, \hat{d}_1 \sin \phi + d_2(t)\, \hat{d}_1 \cos \phi + n_c(t)\, \hat{d}_1 \sin \phi + n_q(t)\, \hat{d}_1 \cos \phi$$

At (4)

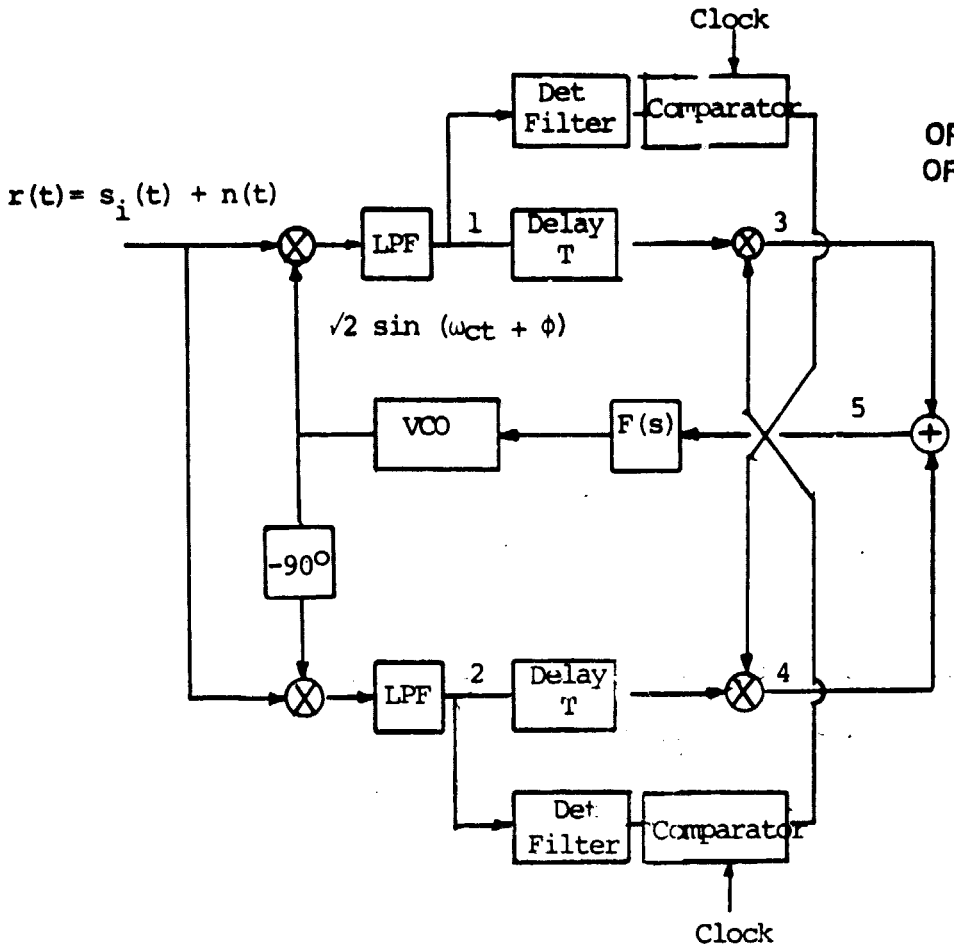


Figure 2.11a Decision-Feedback Carrier Synchronizer for Quadrature Modulation

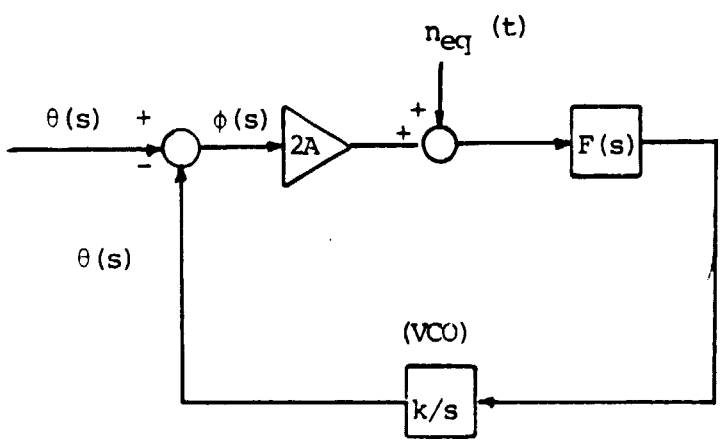


Figure 2.11b Equivalent Linear Model for Phase Tracking

$$e_4(t) = -d_1(t)\,\hat{d}_2 \cos\phi + d_2(t)\,\hat{d}_2 \sin\phi - n_c(t)\,\hat{d}_2 \cos\phi + n_q(t)\,\hat{d}_2 \sin\phi$$

At (5) letting $\hat{d}_1 = \text{sgn}\, d_1$, $\hat{d}_2 = \text{sgn}\, d_2$

$$e_5(t) \approx 2\,(d_1\,\text{sgn}d_1 + d_2\,\text{sgn}d_2)\sin\phi + \cos\phi\,[n_q(t)\,\hat{d}_1 - n_c(t)\,\hat{d}_2] + \sin\phi\,[\hat{d}_1\,n_c(t) + \hat{d}_2\,n_q(t)]$$

If we define

$$n_{eq}(t) = \hat{d}_1\,n_q(t) - \hat{d}_2\,n_c(t)$$

then $n_{eq}(t)$ has spectral density N_o. Also since $\sin\phi \ll \cos\phi$ for normal tracking, the second noise term is negligible. Also, $d_1\,\text{sgn}d_1 + d_2\,\text{sgn}d_2 = 2A$ for QPSK. Thus

$$e_5(t) \approx 2A\,\phi + n_{eq}(t)$$

A linearized model of the loop is shown in Figure 2.10b.

Defining B_L as the one-sided equivalent noise bandwidth of the loop, we may show the phase error variance σ_ϕ^2 is

$$\sigma_\phi^2 = \frac{N_o(2B_L)}{4A^2}$$

Since the average power in the input signal is $2A^2$,

$$\sigma_\phi^2 = \frac{N_o B_L}{P} \quad \text{rad}^2$$

which is the result for tracking a pure carrier in additive noise. The decision feedback loop, assuming linearized analysis and correct decisions, performs as well as an unmodulated signal PLL. It may be shown

that the effect of decision errors is to reduce the loop gain by $(1 - 2P_e)$, and for all other parameters equal, increases the phase error variance by $1/(1 - 2P_e)^2$. However, if we assume the system is designed to estimate the data to better than 1 error per 100 bits, this effect is a negligible degradation to performance.

On the basis of the above, we may give rough design parameters for the loop. Suppose we wish $P_E \approx 10^{-5}$. Then $E_b/N_o \approx 10$ dB for QPSK. This means $P\ T_b/N_o = 10$ or $P/N_o = 10R$. To maintain a 3σ phase error of $9°$ (adequate for QPSK degradation to be a fraction of a dB), then $\sigma \approx 3°$. From the above result.

$$\left(\frac{3}{57}\right)^2 = \frac{N_o B_L}{P} = \frac{B_L}{10R}$$

Thus the loop bandwidth should be

$$B_L \approx R\left(\frac{3}{57}\right)^2 \times 10 \approx .03R$$

or the loop bandwidth should be less than R/30. For R = 1 Gbps, the loop bandwidth can be as large as 30 MHz on SNR considerations alone. Synchronization and frequency tracking constraints may imply a different loop bandwidth however.

It may be shown that the decision-feedback loop has a four-fold phase ambiguity, i.e. there are stable lock points at $n\pi/2$, n = 0, 1, 2, 3. This necessitates either insertion of a known data pattern periodically to resolve this ambiguity or use of differential coding. The latter roughly doubles the error rate but is the preferred alternative.

We now turn to the problem of estimating phase for a modulated QASK system. A first question is whether the above QPSK receiver can adequately perform this task. One has an intuitive feeling it may since the QASK signal is a sum of QPSK signal with another 6 dB weaker QPSK signal. Indeed this is how we analyze the performance.

We write the received signal as

$$r(t) = \sqrt{2}\,[d_1(t)\cos\omega_c t + d_2\sin\omega_c t] +$$

$$\frac{\sqrt{2}}{2}\,[d_3(t)\cos\omega_c t + d_4(t)\sin\omega_c t] + n(t)$$

where again $d_1, \ldots d_4$ are $\pm A$.

At (1) and (2) the signals now are:

$$e_1(t) = d_1(t)\sin\phi + d_2(t)\cos\phi + \frac{1}{2}\,d_3(t)\sin\phi$$

$$+ \frac{1}{2}\,d_4(t)\sin\phi + n_c(t)\sin\phi + n_q(t)\cos\phi$$

$$e_2(t) = -d_1(t)\cos\phi + d_2(t)\sin\phi + -\frac{1}{2}\,d_3(t)\cos\phi$$

$$+ \frac{1}{2}\,d_4(t)\sin\phi - n_c(t)\cos\phi + n_q(t)\sin\phi$$

Again, we decide d_2 in the I channel and d_1 in the Q channel, and call these $\hat{d}_1$ and $\hat{d}_2$, both of size 1. At (3) and (4) we now have

$$e_3(t) = d_1(t)\,\hat{d}_1\sin\phi + d_2(t)\,\hat{d}_1\cos\phi + \frac{1}{2}\,d_3(t)\,\hat{d}_1\sin\phi$$

$$+ \frac{1}{2}\,d_4(t)\,\hat{d}_1\cos\phi + n_c(t)\,\hat{d}_1\sin\phi + n_q(t)\,\hat{d}_1\cos\phi$$

$$e_4(t) = -d_1(t)\,\hat{d}_2\cos\phi + d_2(t)\,\hat{d}_2\sin\phi - \frac{1}{2}\,d_3(t)\,\hat{d}_2\cos\phi$$

$$+ \frac{1}{2}\,d_4(t)\,\hat{d}_2\sin\phi - n_c(t)\,\hat{d}_2\cos\phi + n_q(t)\,\hat{d}_2\sin\phi$$

Then $e_5(t)$, assuming now ϕ is small and that $\hat{d}_1 = \text{sgn } d_1$, $\hat{d}_2 = \text{sgn } d_2$, is

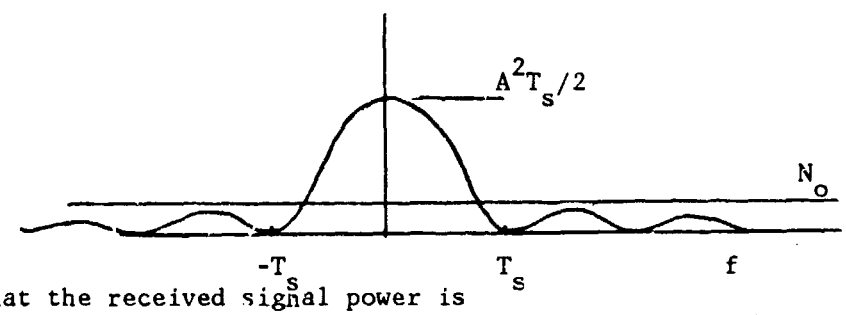
$$e_5(t) = 2A \sin \phi + \frac{A}{2} (\text{sgn}(d_3(t)\, d_1) + \text{sgn}(d_4(t)\, d_2)) \sin \phi$$

$$+ \frac{A}{2} (\text{sgn}(d_4(t)\, d_1) - d_3(t)\, d_2) \cos \phi + [n_c(t)\, \hat{d}_1$$

$$+ n_q(t)\, \hat{d}_2] \sin \phi + [n_q(t)\, \hat{d}_1 - n_c(t)\, \hat{d}_2] \cos \phi$$

$$\simeq 2A\, \phi + [\frac{A}{2} d'(t)] + n_{eq}(t)$$

where $d'(t) \overset{\Delta}{=} d_4(t)\, d_1 - d_3(t)\, d_2$ which is a zero mean <u>ternary</u> random sequence ε (2, 0, -2) at the symbol rate T_s. This middle term has a power spectrum which is $\sin^2(\bullet)/(\bullet)^2$ in form, with average power $A^2/4\ [1/4\ (2^2) + 1/4\ (2^2) + 1/4\ (0^2)] = A^2/2$. The one-sided noise spectral density of this process at the origin $S(0) = A^2 T_s/2$. As before the process $n_{eq}(t)$ has spectral density N_o. Thus spectrally-speaking we have a loop jitter process $n'(t)$ having the sum of these spectra, illustrated below:



Note that the received signal power is

$$P_{ave} = A^2[1.5^2 + 1.5^2 + 2(1.5^2 + .5^2) + (.5^2 + .5)^2]/4 = A^2[2.5]$$

and $E_b = P_{ave}\, T_b = P_{ave}/R_b$

For $P_\xi = 10^{-5}$ with QASK we need $\bar{E}_b/N_o \simeq 14$ dB or

which says

$$P_{ave}/N_oR_b \simeq 25$$

$$2.5A^2/N_oR_b = 25 \text{ or } A^2/N_oR_b = 10$$

Now since $R_b = 4R_s$, then $T_s = 4T_b$ and $A^2T_s/2 = 2A^2/T_b$.

Thus the ratio of spectral densities at the origin above is

$$\frac{2A^2T_b}{N_o} = \frac{A^2}{N_oR_b} = 10$$

at typical performance levels.

Thus we find the data pattern noise due to the second-level of QPSK dominates the additive thermal noise in its effect on loop phase jitter. Assuming the thermal noise level is negligible, we can treat the self-noise, or pattern noise as a wideband noise term, and as above the loop phase error variance is:

$$\sigma_\phi^2 = \frac{S(0)2B_L}{4A^2} = \frac{(A^2T_s/2)2B_L}{4A^2} = \frac{B_LT_s}{4} = B_LT_b$$

This result says we now need to keep B_L quite small to keep $\sigma_\phi \simeq 3°$. Specifically

$$\sigma_\phi^2 = \left(\frac{3}{57}\right)^2 = B_LT_b = \frac{B_L}{R_b}$$

or $B_L \simeq .003\ R_b$. This is roughly one-tenth the value when only QPSK modulation was present. Note also that increasing the SNR does not decrease phase jitter as it usually does; instead we have a residual pattern noise which remains of constant relative intensity. Nonetheless, we can make its effect small if B_L is sufficiently small relative to the data rate.

Thus, we can say the <u>same</u> loop structure will work for both QPSK and QASK, provided the loop bandwidth is sufficiently small to average out pattern jitter.

If this is not acceptable performance the structure of Figure 2.11a will remove the effect of this pattern noise, provided 4-level decisions are made for the I and Q channels. In fact the only difference between the QPSK and QASK versions is how many decision levels are involved and how many levels are fed back. The only real issue is whether a binary-input multiplier suffices (in lieu of an analog multiplier), and whether one wishes to have mode switches for the carrier loop. When full 4-level feedback is used we may again show

$$\sigma_\phi^2 = \frac{N_o B_L}{\bar{P}}$$

where $\bar{P}$ is the average power. Since $\bar{P}$ will be larger for QASK than for QPSK by about 7 dB at a <u>fixed symbol rate</u> to maintain constant P_ε, then the phase error variance will be smaller by a factor of 5, as it must be due to the closer packing of signals.

Using a more refined analysis which calculates the error probability dependence on R/B_L, and E_b/N_o, Simon and Smith [10] show that for $R/B_L > 10$, that the effective SNR loss is less than 0.5 dB. This is consistent with our approximate calculation above.

2.4.2 <u>Symbol timing for QPSK/QASK</u>

To obtain symbol timing directly from the received sygnal, a number of synchronizer structures have been analyzed, ranging from those motivated by optimal estimation theory to very intuitive approaches which nonetheless work well if signal to noise ratio is adequate. Some

structures, such as the early-gate/late-gate or digital transition tracking loop [11] assume a timing reference as part of their operation, and are somewhat more complicated to implement, especially at high data rates. We describe two structures which are compatible with both QPSK and QASK and operate without any timing estimate supplied.

Delay-and-Multiply. The delay-and-multiply synchronizer is shown in Figure 2.12 for a QPSK/QASK receiver. The average of the summer output can be shown to have a Fourier series periodic in T, whose fundamental can be extracted with a narrowband filter, perhaps a PLL. For rectangular pulse modulation, a delay of T/2 maximizes the strength of this fundamental, while for a full spectral raised-cosine pulse shape, the maximizing delay is approximately 0.2T [11].

The same circuit works for QASK, which amounts to four level modulation in each I/Q arm. The strength of the fundamental component depends on the average received power, but the maximizing delays are as for QPSK.

Simplifications of this circuit for high-speed operation may be possible. If binary quantization (sign detection) of the LPF outputs is performed, then the multiplication indicated can be reduced to an exclusive or gate. The SNR performance of the synchronizer will be slightly degraded but can be made adequately high if the filter bandwidth of the post-filters is sufficiently narrow. Roughly speaking, this filter will have a bandwidth about one percent of the symbol rate.

Envelope-derived synchronizer. Another timing technique is that of Lyon [12], also appropriate for both QPSK and QASK. The structure is shown in Figure 2.13. Here we do not require delay lines

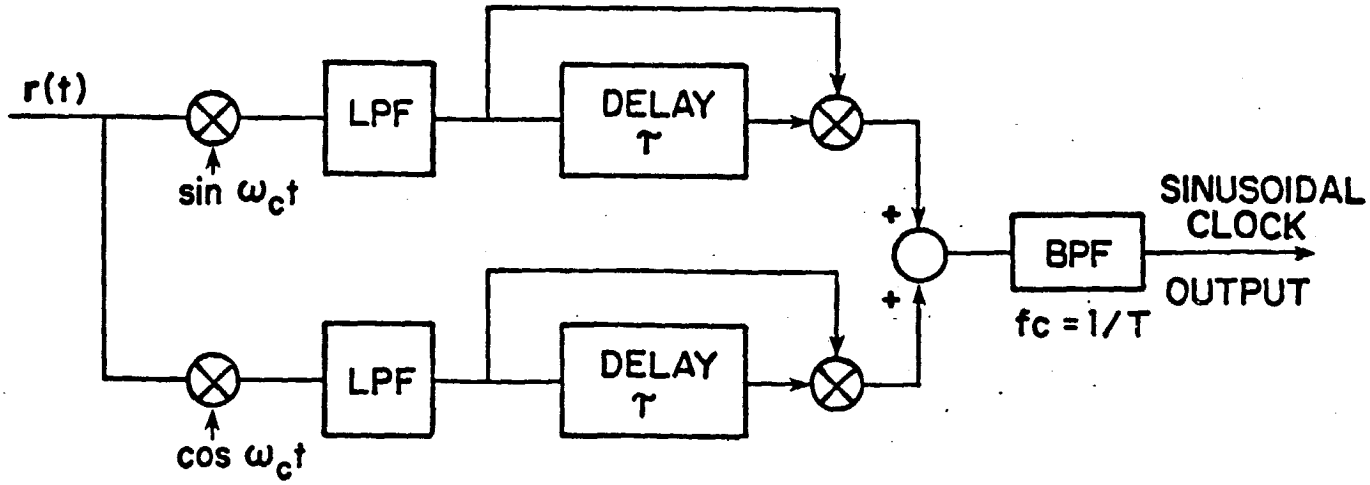


Figure 2.12 Delay and Multiply Synchronizer

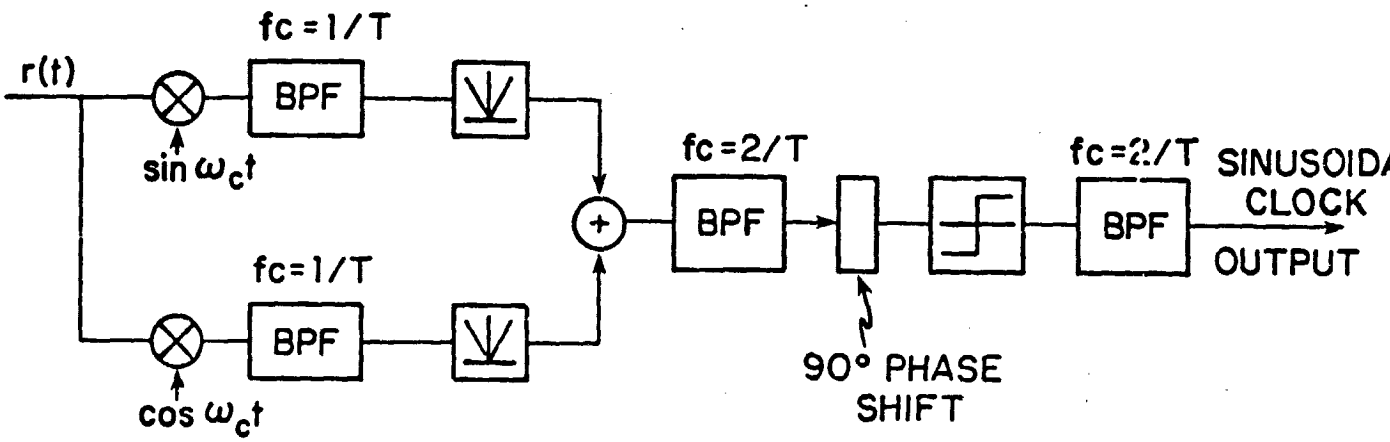


Figure 2.13 Envelope-Derived Symbol Synchronizer

nor multipliers, but substitute bandpass filters and full-wave rectifiers. The filters must be carefully tuned to have even amplitude and odd phase functions about the center frequency, e.g. a single-tuned circuit at $f_c = 1/T$, and a typical Q would be 20-100. This presents the most difficult design challenge, although a narrow-band PLL could be used to replace the post-combiner filter/phase shifter/limiter combination.

Both synchronizers are quite compatible with the basic architecture of the data demodulator and phase tracking loop. The quadrature demodulation is common to all three functions, and the LPF/delay line/multiplier is a structure required in the decision-feedback carrier synchronizer, albeit with different parameters.

As with most synchronizers, lack of data transitions causes the symbol synchronizer to lose lock, and a pseudo-random scrambling of the data stream may be required to induce a sufficient density of transitions during long runs of 1's or 0's in the data.

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3. GaAs DEVICE TECHNOLOGY

The second principal component of this study has been an exploration of the use of gallium arsenide (GaAs) monolithic circuit technology for implementing an advanced performance modem on a "chip," or several chips. GaAs has attracted widespread attention in the last decade for very high speed logic circuitry, and for low-noise microwave amplifiers. Silicon technology, though much further developed, cannot attain the performance levels of GaAs devices, principally due to the much higher electron mobility and peak velocity of GaAs.

The GaAs MESFET is the basic building block of most GaAs circuits, and can function as a low-noise, small signal amplifier up to 30 GHz region, or in a switching mode to implement logic gates and simple digital functions at clock speeds of 5 GHz. Other functions performed by MESFETs are active mixing, particularly with dual-gate FETs, and oscillators, again past 30 GHz. Power amplifier FET's are also under widespread development, but are not a concern for this study.

As mentioned, GaAs technology lags well behind silicon technology in terms of large scale integrated circuits and certainly in terms of commercial development. This is mainly due to earlier difficulties in achieving adequate semi-insulating GaAs crystalline materials, and the fact that silicon technology was formerly adequate for nearly all electronic applications. Lately, the situation is rapidly changing, spurred on by superior device performances reported by research laboratories, and by increased support from government sources for integration of functions in GaAs. Commercially, most major

semiconductor firms have active research programs in GaAs circuitry, or are starting pilot lines for simple devices.

We have undertaken the general characterization of a monolithic integrated circuit on GaAs around the framework of the dual-modem described in Chapter 2. This modem reflects state-of-the-art communications technology, and we felt at the outset that circuit integration of the modem was technically within reach. Many of the functional elements have been demonstrated at or beyond the performance levels we seek, but integration and process compatibility, chip complexity, size, and power remained unexamined.

The potential for such a GaAs modem is discussed below in several basic functional headings: transmission lines on GaAs; logic; small-signal amplifiers, mixers, oscillators, and A/D converters.

3.1 COMPONENT DISCUSSIONS

3.1.1 Transmission Lines

In RF signal processing, transmission line techniques are used in microwave integrated circuits to do impedance matching, filtering, and hybrid combining. The theory for such distributed circuits is well-developed, and the only reason for discussing lines here is to point out that semi-insulating GaAs substrates are dielectrics ($\varepsilon_{eff} \approx 9$) with low loss tangent ($\delta = 5\times10^{-4}$), and all the normal functions can be implemented on GaAs together with the active devices in one medium. It is interesting to note that the simplest passive RF devices, such as branchline 3-dB hybrids, are larger consumers of substrate area compared to electronic devices. This is because the transmission line

lengths are on the order of $\lambda/4$, and for say 20 GHz operation, $\lambda/4$ represents a physical length of about 1 mm in GaAs.

Fifty ohm lines are standard designs in microwave IC's (impedances can run from 20 to 200 ohms as well). Assuming a 200 μm thick GaAs substrate above a metallic plane, a 50 ohm line will be about 200 μm wide. Of course, the substrate thickness can be varied some to suit but physical and processing constraints are more important than the effect on impedance.

3.1.2 GaAs Digital Logic

The logic types investigated in this study include enhancement mode FET (E-MESFET), enhancement-depletion FET (E/D-MESFET), low pinch off voltage FET logic (LPFL), Schottky diode FET logic (SDFL) and buffered FET logic (BFL).[1] Basic circuit configurations are shown in Figure 3.1 through 3.4. The propagation delays, clock frequencies, and maximum gate count are compared in Table 3.1. For these devices, switching speeds are roughly inversely proportional to the gate length to roughly L = 0.3 μm ([1], p. 661) whereas the gate power is roughly proportional to the gate length. A tentative goal for the modem design is for the logic to operate at 3 GHz. This does not serve as a limitation with 0.5 μm technology since all of the logic types operate at this frequency.

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[1]JFETs have not been considered since the technology lags that of other devices. Development is impeded by lack of a suitable p-type dopant implant, increased complexity and difficulty in fabrication ([1], p. 598).

BUFFERED FET LOGIC

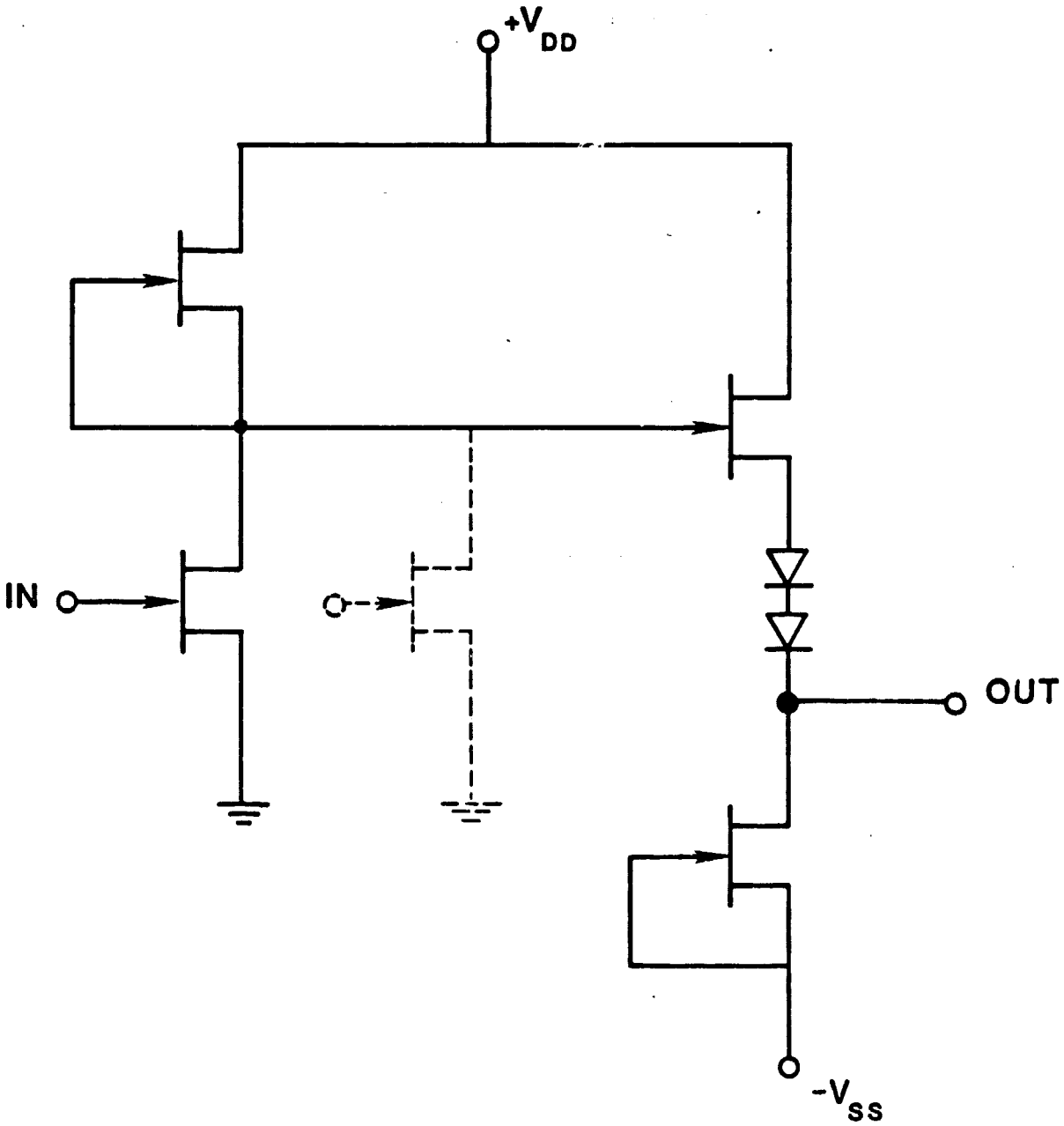


Figure 3.1 Inverter Gate, with Dashed FET Indicating NOR Geometry

LOW PINCHOFF VOLTAGE FET LOGIC

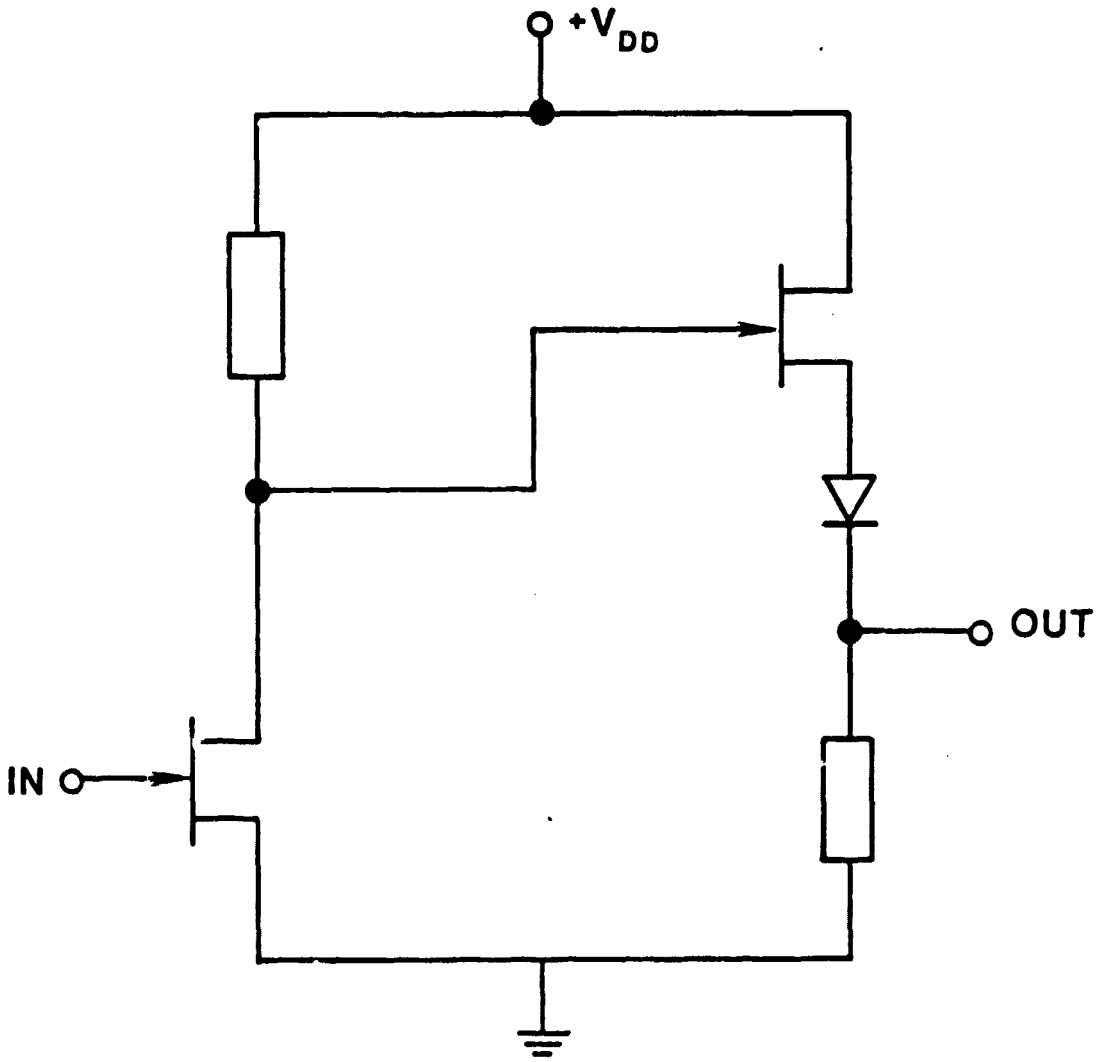


Figure 3.2 LDFL Inverter Gate. Boxes are Typically Resistors but may be active (FET) devices. Note similarity to buffered and direct coupled logic diagrams

DIRECT COUPLED FET LOGIC

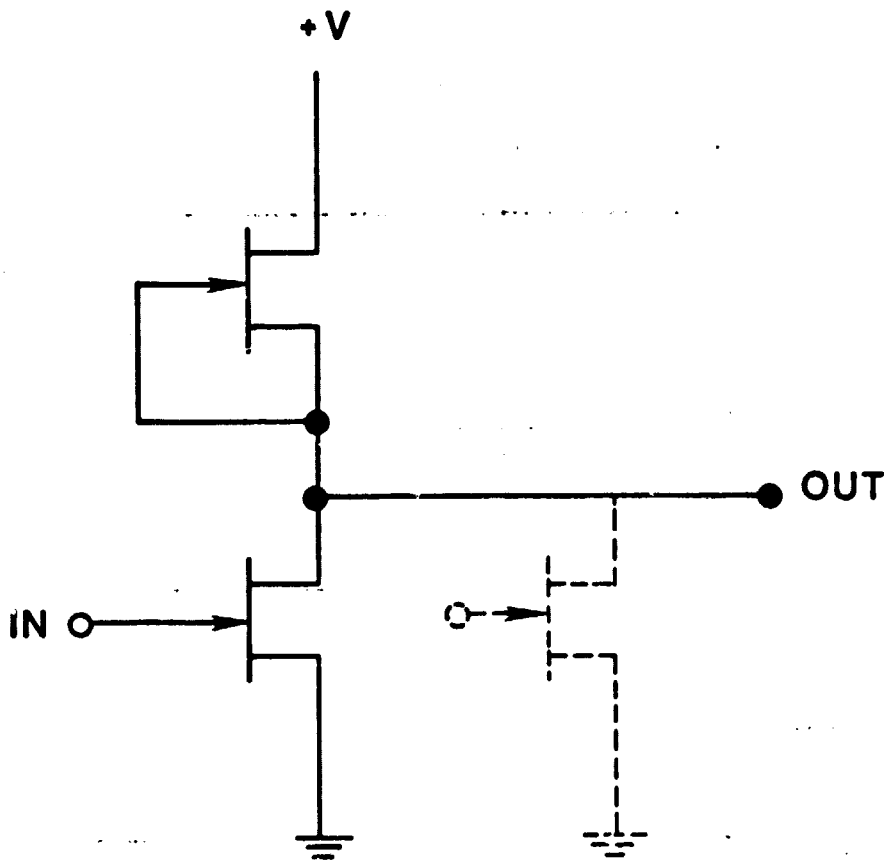


Figure 3.3 Direct Coupled Inverter Logic Gate with Enhancement Mode Input FET and Active (depletion FET) Load. Active load may be replaced by a resistor. Dashed enhancement FET shows NOR gate geometry.

SCHOTTKY DIODE FET LOGIC

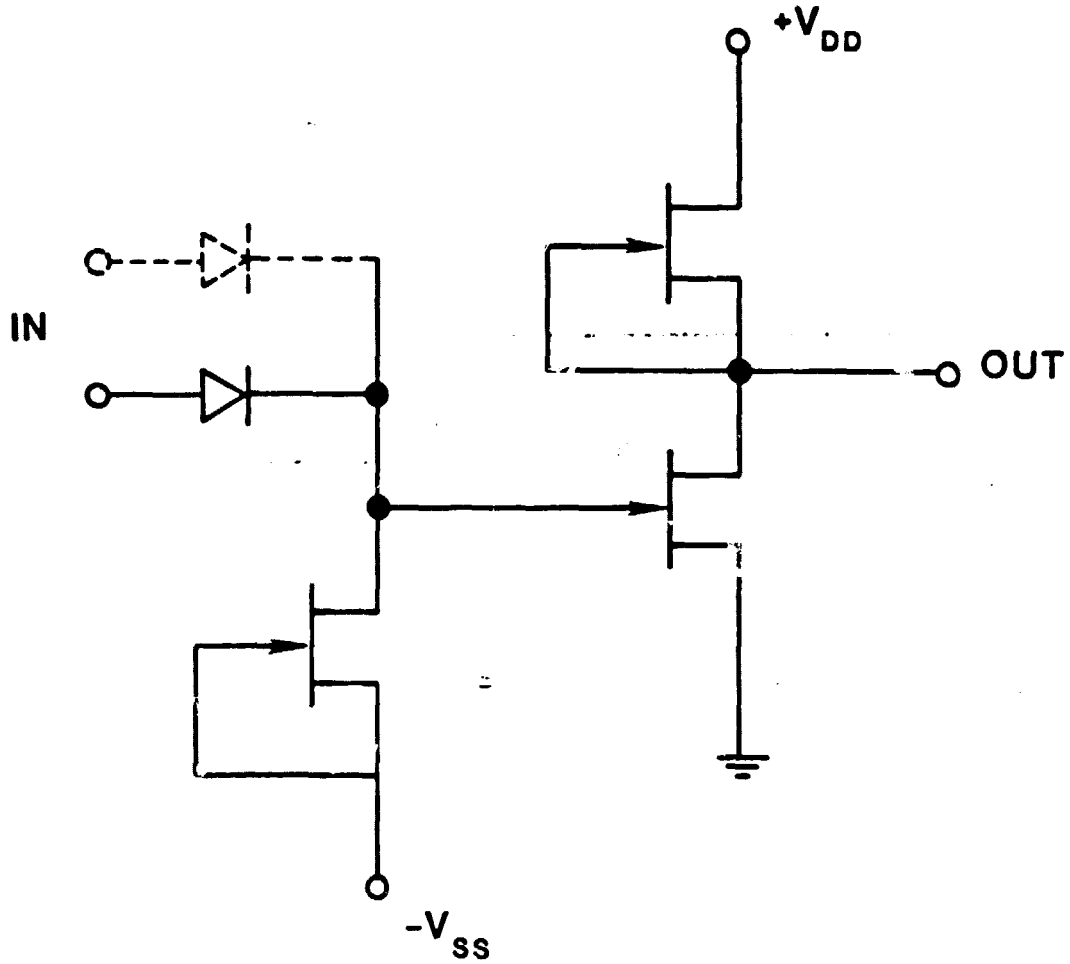


Figure 3.4 Schottky Diode Inverter Logic Gate where dashed diode shows NOR geometry

TABLE 3.1. Comparison of Logic Types

FET Operation	Direct Coupled enhancement mode normally off	Low Pinch off quasi normally off	Schottky Diode depletion mode normally on	Buffered FET depletion mode normally on
Pinchoff voltage (V)	0 to +0.1	0	-1.0	-1 to -2.5
Pinchoff tolerance	very tight	tolerant	tolerant	most tolerant
Voltage supplies (V)	-1 to -1.5	+2.5	+2, -1.5	+3 to +4, -1.5 to -3.5
Voltage swing (V)	0.5	0.8	0.5 to 2	~ 2.5
Power per Gate (mW)	0.01 to 1	0.5 to 2	0.5 to 2	2 to 40
Propagation Delay (ps)	100 to 500	100 to 150	70 to 120	60 to 100
Packing density (gates/mm^2)	1000 achieved LSI	400	400 achieved LSI	200

In development of a monolithic chip containing both digital logic and microwave FETs, considerations of both feasibility and fabrication compatibility are important. The logic must function near 2 GHz, while the amplification, mixing and detection functions occur 0-4 GHz for IF and 20-30 GHz for RF. While the devices for logic and microwave functions are widely different, the materials, geometry, and doping profile must be similar and compatible if the design is to be realized as a monolithic chip. In determining compatibility of the various device types for monolithic IC realization, complexity and difficulty in fabrication are recognized and an important restriction. With this consideration "compatible" will be partially defined as the ability to restrict the design to having two channel types, i.e., channels of two heights or two doping profiles.

The operating characteristics of the various logic types are presented and examined for performance compatibility and current achievements. Discussion is based on < 0.5 μm technology needed for high frequency LNA fabrication [2].

3.1.2.1 Buffered FET Logic. BFL has the distinct advantage of offering the fastest switching speed and the easiest to control fabrication of all the logic types. The relative ease in fabrication stems from the large and less rigid control required for the pinchoff voltage. This relatively large voltage swing of ≈ 2.5 V also results in good noise immunity. BFL is fabricated with a minimum pinchoff voltage of approximately -1.5 volts, which is roughly the maximum V_p expected for the high frequency (≈ 20 GHz) low noise amplifier. This difference in pinchoff voltage is somewhat incompatible with the low noise

amplifier and would require different conductive layers for the logic and amplifier sections of the design. The low "on" state resistance of BFL is compatible with switching FETs possibly needed in path length modulators.

The very high speed capabilities of BFL have been shown in Liechti et al. ([23], p. 998). A 5 Gbps (up to 6.5 Gbps) 8:1 parallel to serial converter was constructed with 600 active devices (400 MESFET and 230 diodes), utilizing the full available power budget of 2W per chip. Channels 0.25 μm deep with $n \leq 2.5 \times 10^{17}$ cm^{-3} were formed with 500 KeV Se implants at 6×10^{12} cm^{-2} through a 0.8 μm thick Al mask. To lower the channel and diode resistances, n^+ regions were implanted with 500 KeV Si to 1×10^{13} cm^{-2} dose, then annealed in Si_3N_4 encapsulation at 850°C for 15 minutes. Ohmic contacts were formed by evaporation of NiCr, Ge and Au, and recessed, 1.0 μm, Cr-Pt-Au gates using liftoff and SiO_2 capping were employed. Second layer interconnects were formed with 1 μm Ti-Pt-Au delineated by argon ion milling. Driver MESFETs used +4.5V and -3.5V supply voltages, 10 mW power, 60 ps propagation delay (unity fan in and fan out) with 2.5 V logic swings. This example shows the very high speed and high power consumption of BFL.

The primary disadvantage of BFL, relative to this modem application, is the high power consumption which limits the gate density to about 10^3 gates/chip. This is about the expected density of the modem design (vicinity of 1000 to 2000 gates). The minimum power dissipation of BFL is at the point of exceeding the maximum of the allowable power dissipation (~ 2 watts) on the chip ([1], p. 599; [2], p. 379).

3.1.2.2 Low Pinchoff FET Logic, Schottky Diode FET Logic. The main motivation behind the development of LPFL was to avoid the fabrication problems of direct coupled FET logic (DCFL) by allowing twice the flexibility in the range of V_P control ([19], p. 574) and yet maintain nearly the same simple circuit approach as DCFL. After investigating LPFL, little advantage can be found over SDFL. SDFL is roughly 25% faster ([3], p. 294; [11], p. 293) and offers a more flexible design and fabrication scheme. The gates may be designed to operate at very low pinchoff voltages and logic swings (i.e. V_P=0.5, ΔV=0.5) or by adding a level shift diode higher pinchoff voltages and higher logic swings may be used ([1], p. 673). This would increase noise immunity and speed at the expense of increased power. SDFL requires more V_P control than LPFL for a given design. The range of V_P in LPFL is = 0.0 ± 0.2 volts.

Another important disadvantage of LPFL is the apparent lack of compatibility with line switching MESFETs of the phase modulators and with LNAs. Based on a survey of the channel characteristics of these devices, LPFL will have too small a pinchoff voltage for low channel resistance line switches and LNAs. The channel requirements will be investigated in more detail with MESFET computer models. Since the technology available for tighter V_P control is developing rapidly, and since V_P control in SDFL is not a paramount problem, LPFL is not as popular as DCFL or SDFL and does not seem a likely choice in selection of a logic type.

3.1.2.3 Direct Coupled FET Logic: Enhancement MESFET, Enhancement/Depletion MESFET. Enhancement and enhancement/depletion

MESFET logic offer the convenience of requiring only one power supply (1-2 volts). Also, both have similar circuit configurations which are the simplest of all the other logic types (see Figure 3.4). The main difference between the two is that the load in E/D-MESFET logic consists of a depletion FET while in E-MESFET logic the load consists of an ohmic, usually epitaxial, resistor. This FET load gives E/D-MESFET logic increased speed and a much sharper output voltage swing than the resistor load since its pull-up characteristics are parabolic (constant current), and thus stronger ([1], p. 644; [2], p. 377). Both logic types require very precise control of the pinchoff voltage for the switching FET, i.e. ±.03 to ±.05 volts ([1], 615). This requires controlling the channel thickness to within ±20® ([1], p. 587), a current technological challenge. From compatibility with LNA fabrication considerations, no advantage is obtained with E-MESFET since the additional channel for the depletion mode LNA is necessary anyway. E/D MESFET logic requires two different channel configurations. The depletion FET channel V_P has a wide range; V_P = -0.85 to -1.5 [4,5] and is compatible with the depletion mode LNA. This flexibility stems from the D-MESFET's application as a constant current source. Within a wide range of V_P, the channel width is adjusted to give the required current needed to balance the gate's rise and fall times. Thus E/D MESFET logic is chosen over E-MESFET logic.

The highest level of integration of E/D MESFET logic found is a 1 kb static RAM reported by Ino et al. [22]. The FETs employed highly doped, n^+Si ion implanted layers close to the gate, in order to increase the speed by decreasing channel resistances. Gate lengths for

both FETs are 1 μm and the driver, transfer, and depletion FETs widths are 9, 4 and 4 μm, respectively. Supply voltage is 0.7 to 1.5 volts and logic swing ~ 0.6 volts. The n^+ - n^+ spacing is 1.5 μm. Annealing was performed with Si_3N_4 encapsulation. SiO_2 deposition and gate-liftoff were employed. This chip contains a total of 7084 FETs (4811 E-FETs and 2273 D-FETs).

Another example of LSI with E/D MESFET logic is presented by Fujitsu Laboratories ([4] p. 6). The chip is a 6.4 ps, 6 x 6 bit multiplier with 408 NOR gates comprising 1284 enhancement and depletion FETs dissipating 173 mW at V_s = 1.5 volts. Propagation delay per gate is 210 to 260 ps, dissipating 0.35 mW/gate at V_s = 1.5 volts. Fabrication techniques included a self-aligned gate 2 μm long. The FETs were fabricated with Si^+ ion implantation at 59 KeV with a dosage of 1.1×10^{12} cm^{-2} for the enhancement FETs and 2.1×10^{19} cm^{-2} for the depletion FETs. Self-aligned n^+ regions were formed with Si implantation at 175 KeV and a dosage of 1.7×10^{13} cm^{-2}. Annealing was performed with 0.1 μm SiO_2 encapsulation. Gates and first level interconnects were delineated via TiW sputtering and reactive ion etching. Au-Ge-Au ohmic contacts were formed by liftoff and Ti-Au was used as a second level interconnect. This example shows the low power-high integration level and speed (≈ 2 Gpbs) capabilities of E/D MESFET logic.

3.1.2.4 Comparison of E/D MESFET and SDFL. Further consideration of E/D MESFET and SDFL is necessary to determine applicability and compatibility with the system proposed. The switching diodes and the D-MESFET (V_p ≈ -1.0, ([1], p. 588)), of SDFL do not require, but usually use, two different doping profiles to optimize the

speed of the switching diodes. Selective ion implantation is usually used to accomplish this optimization ([1], p. 680; [2], p. 373). Although SDFL requires careful pinchoff control to obtain a low V_P ([1], p. 598; [2], p. 373) and balanced driving capability, V_P does not have to be controlled as carefully as in DCFL (±30 to ±50 mV) SDFL tolerates a V_P deviation three times greater, respectively ([12], p. 574). For this reason DCFL development has lagged behind SDFL technologies. However, both have recently achieved LSI. DCFL stands to gain the most from technological achievements in V_P control expected in the near future.

Another advantage of SDFL is higher noise immunity due to larger voltage swings (0.5→1.4 V) ([3], p. 294). The primary disadvantage is that SDFL uses 5 to 10 times the power of E/D logic ([1], p. 588). Doping concentrations used for both the LNAs and logic circuits are in the "typical" range of 1.2×10^{17} cm^{-3} to 2.5×10^{17} cm^{-3}. Both logic types have pinchoff voltages that would allow fabrication of channels with acceptably low "on" resistances needed for parallel "reflected" line switches as well as channel characteristics compatible with LNAs. The technologies involved in fabricating DCFL and LNA circuits have been closely paralleled, exchanging techniques to obtain similar characteristics. In particular the techniques involving V_P controls, channel resistances, contact resistances and gate size, have been shared ([7], p. 88). This is considered an important advantage for the compatibility of the logic types (particularly E/D-logic) and LNAs. In conclusion both SDFL and E/D-MESFET logic

should be strongly considered as compatible logic types for this modem development.

3.1.3 High Frequency GaAs Low Noise Amplifiers (LNA)

The preliminary receiver modem design consists of an RF (20-30 GHz) amplification stage, followed by quadrature detection processes. A high gain, low noise RF amplification stage is necessary to minimize noise contributions from the mixing and baseband amplification.

Typical low noise amplifiers have a channel doping $N_d = 1\text{-}3 \times 10^{17}$ cm^{-3} and a height of 1000-2000Å ([1], p. 177). Noise reaches a minimum around 2.5×10^{17} cm^{-3}, whereas gain begins to saturate near 3×10^{17} cm^{-3} for a gate length of 0.5 μm.

The largest noise sources are the source and gate resistances. Source resistance may be decreased by recessing the gate (increase S-G channel height), increasing the doping of the source and drain region (ion implantation of contacts), or decreasing the source-gate separation. Device geometry can be optimized to minimize these parasitics ([10], p. 181) and thus minimize the noise ([7], p. 87; [8], p. 944) without changing the channel height.

The most outstanding performance of GaAs LNAs noted to date has been reported by Watkins and Schellenberg ([24] p. 145). This 1/4 x 30 μm interdigitated MESFET demonstrates 5.0 dB gain at 52 to 62 GHz with a 7.1 db NF at 60 GHz. The best performance at 30 GHz is 2.6 dB noise figure with 8.3 dB gain. These devices were formed by either ion implantation or VPE techniques with VPE showing both superior gain and noise figure performance.

For integrated microwave amplification, E. Watkins, J. M. Schellenberg and H. Yamasaki [25] have reported a 27.5 to 30 GHz GaAs FET amplifier with 4.6 dB NF and 17.5 dB gain. Three stages of amplification were used. The first and second stages consist of 0.25 x 75 μm FETs with total periphery of 150 μm. The third stage consists of 0.5 x 50 μm FETs with total periphery of 100 μm. The gates were delineated by direct electron beam lithography. These amplifiers are employed in a receiver containing a 25-30 GHz dual gate FET mixer with a 10 dB NF and a dielectrically stabilized FET oscillator. This concept of RF amplification and establishment of the noise figure, followed by demodulation, appears to be the most suitable process for the receiver modem.

From the description of FET geometry for logic and microwave applications, it is noted that in all cases, the geometry is extremely similar with the exception of channel heights and widths. Low noise amplifiers typically have wider gates for smaller source-gate resistance. The implanted channel dopant is usually Si, occasionally Se, while S often is used for deep n^+ contact, implants [12].

Preliminary investigations into the design and compatibility of GaAs FET devices has begun through the included computer generated performance curves. The important design parameters, pinchoff voltage, gain, and carrier concentration have been compared for variations in each. The curves are based on a recessed gate structure (Figure 3.14) with ion implanted source and drain contact doping of 10^{18} cm^{-3}, a layer thickness of 0.25 μm, source-gate spacing of 0.5 μm and gate-contact implant spacing of 0.03 μm. The design also assumes

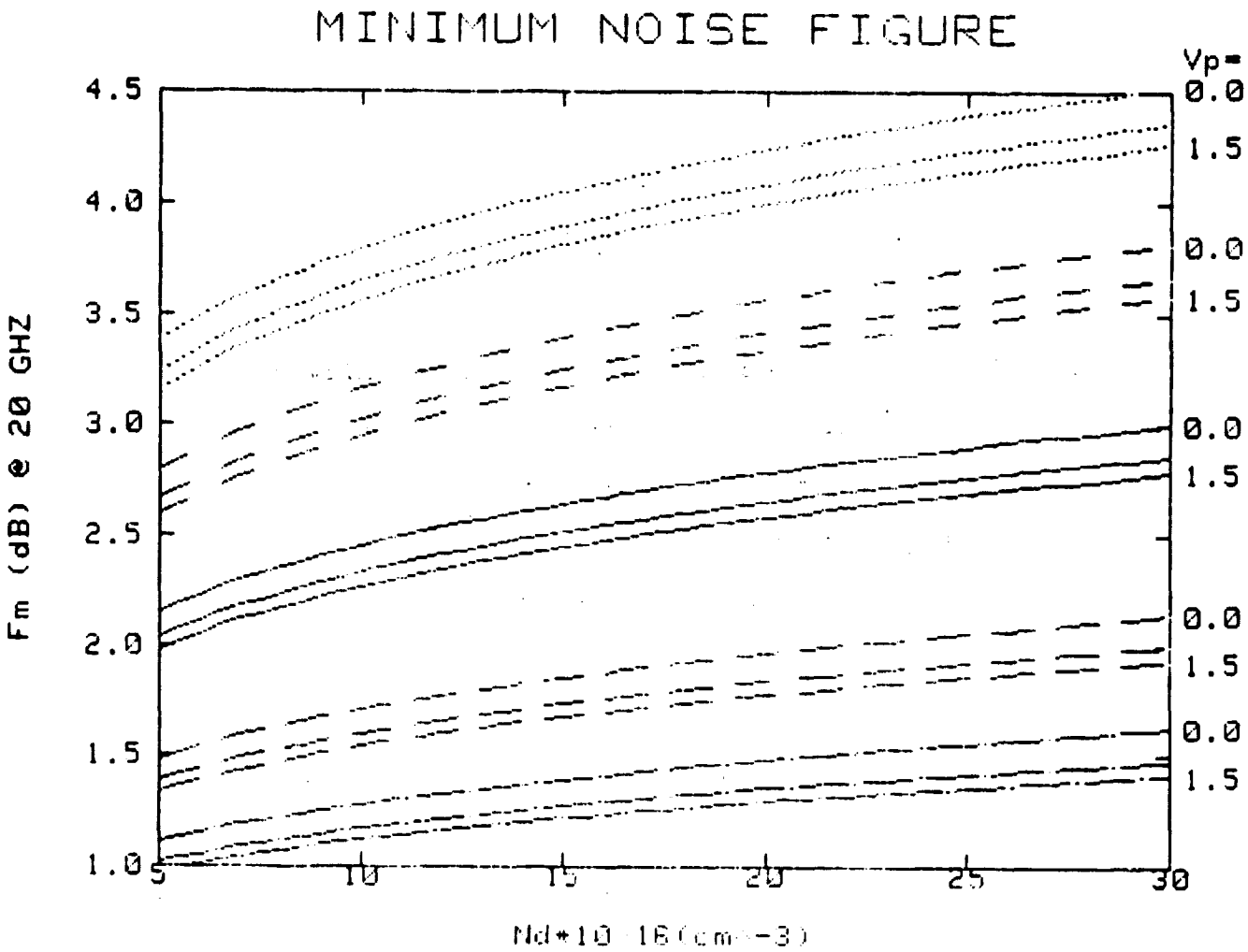
heavily doped (ion implanted) source and drain contacts, and considers surface depletion effects on the channel.

Figures 3.5 through 3.9 show the dependency of available gain, noise figure, optimum source impedance, and pinchoff voltage on device parameters such as gate length, gate width and channel doping. As an example of application of these curves in preliminary design, choose 0.3 μm gate length FET with doping of 10^{17} cm^{-3}. Figure 3.5 indicates the noise figure when properly matched will be about 1.6 dB for 50 μm finger widths, with a pinchoff voltage of about 0.75 volts. To achieve this pinchoff voltage, Figure 3.6 indicates a channel height of 0.14 μm is required. From Figure 3.7, the maximum available gain per stage is about 8 dB for 50 μm gate widths with V_p = 0.75 and gate length = 0.3 μm. The optimum source resistance and reactance are 5 ohms and -3 ohms, respectively.

3.1.4 Mixers

Active mixers having conversion gain can be readily fabricated using GaAs dual-gate MESFETs [2]. The local oscillator signal is relatively strong compared to the RF signal to be mixed to a lower frequency, and when applied to one of the gates, controls the small signal transconductance, g_m, in periodic manner, thus giving the desired product operation. By careful tuning of the match at input and output, conversion gains of 10 dB can be obtained (compared to the 6 dB loss typical of Schottky diode mixers), even with L.O. levels on the order of 0 dB or less.

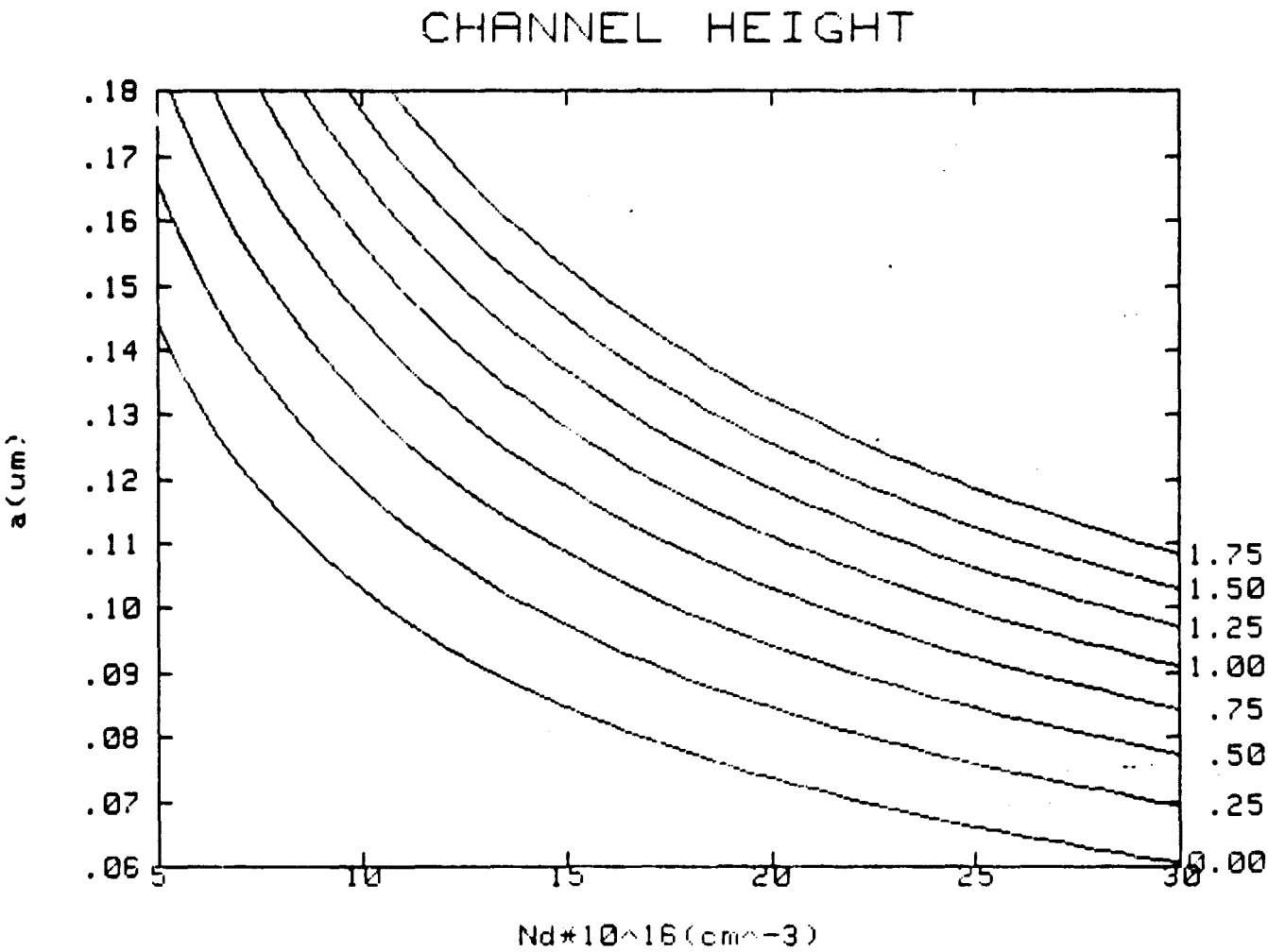
Figure 3.10 illustrates the basic circuit of the dual-gate mixer; device geometries are important in establishing good conversion



THIS GRAPH SHOWS THE GaAS MESFET LNA MINIMUM NOISE FIGURE .vs. THE CHANNEL CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0,.75, AND 1.5, AND PARALLEL GATE SEGMENT (FINGER) WIDTHS Z1=0.0, .05, .1, .15, AND .2 (mm).

Z1= 0(BROKEN SOLID), .05(LARGE DASH), .1(SOLID) .15(SHORT DASH), .2(DOTTED)
L=.3(um), h=.5(um), f=20 GHZ, INDP. OF Z

Figure 3.5



THIS GRAPH SHOWS THE RELATIONSHIP BETWEEN THE GaAs MESFET ACTIVE CHANNEL EFFECTIVE HEIGHT AND THE CARRIER CONCENTRATION FOR VARIOUS PINCHOFF VOLTAGES. THIS CAN BE USED, TOGETHER WITH THE OTHER GRAPHS ON MESFETS CHARACTERISTICS, TO FIND THE CHANNEL HEIGHT FOR A GIVEN PINCHOFF VOLTAGE AND CARRIER CONCENTRATION.

Figure 3.6

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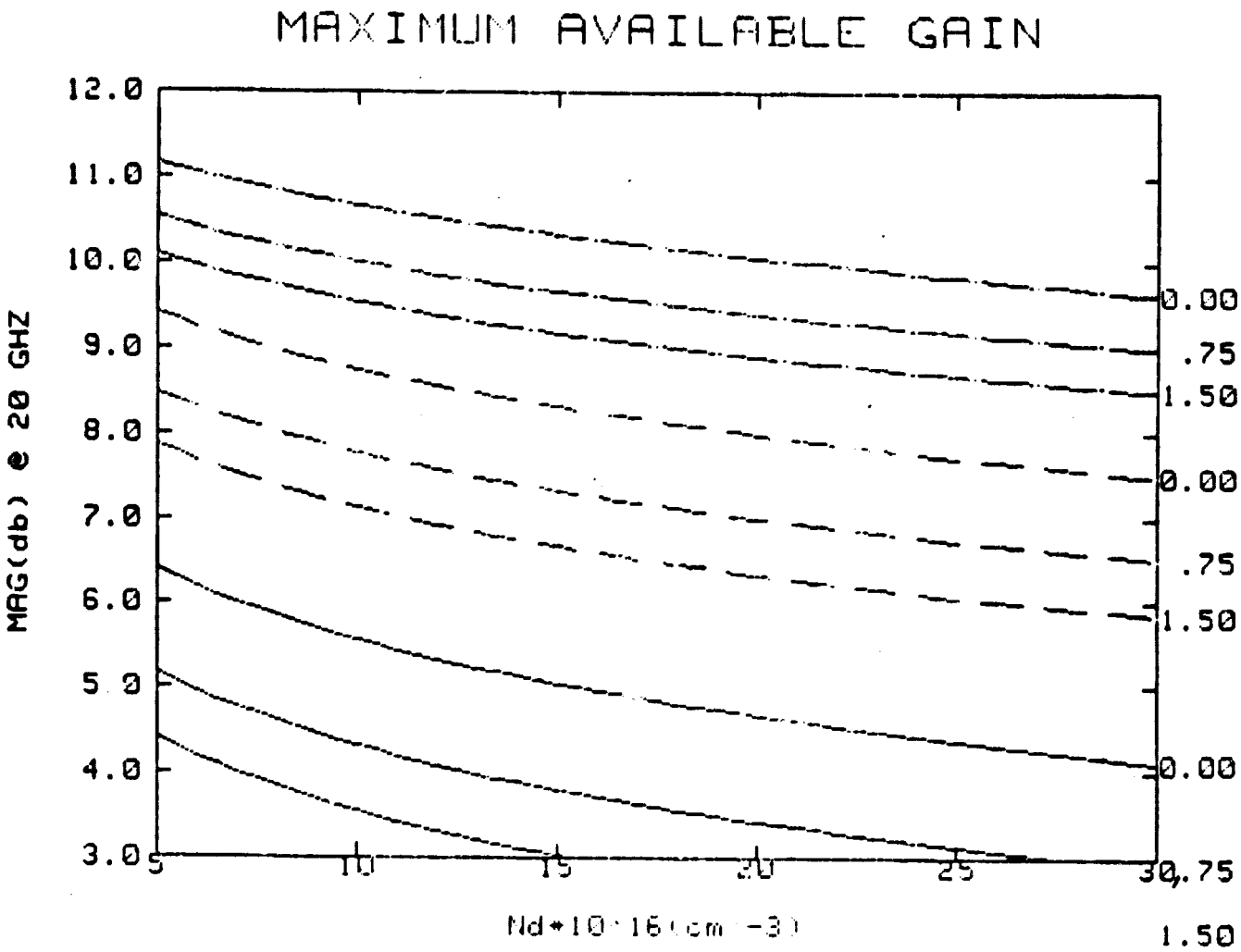
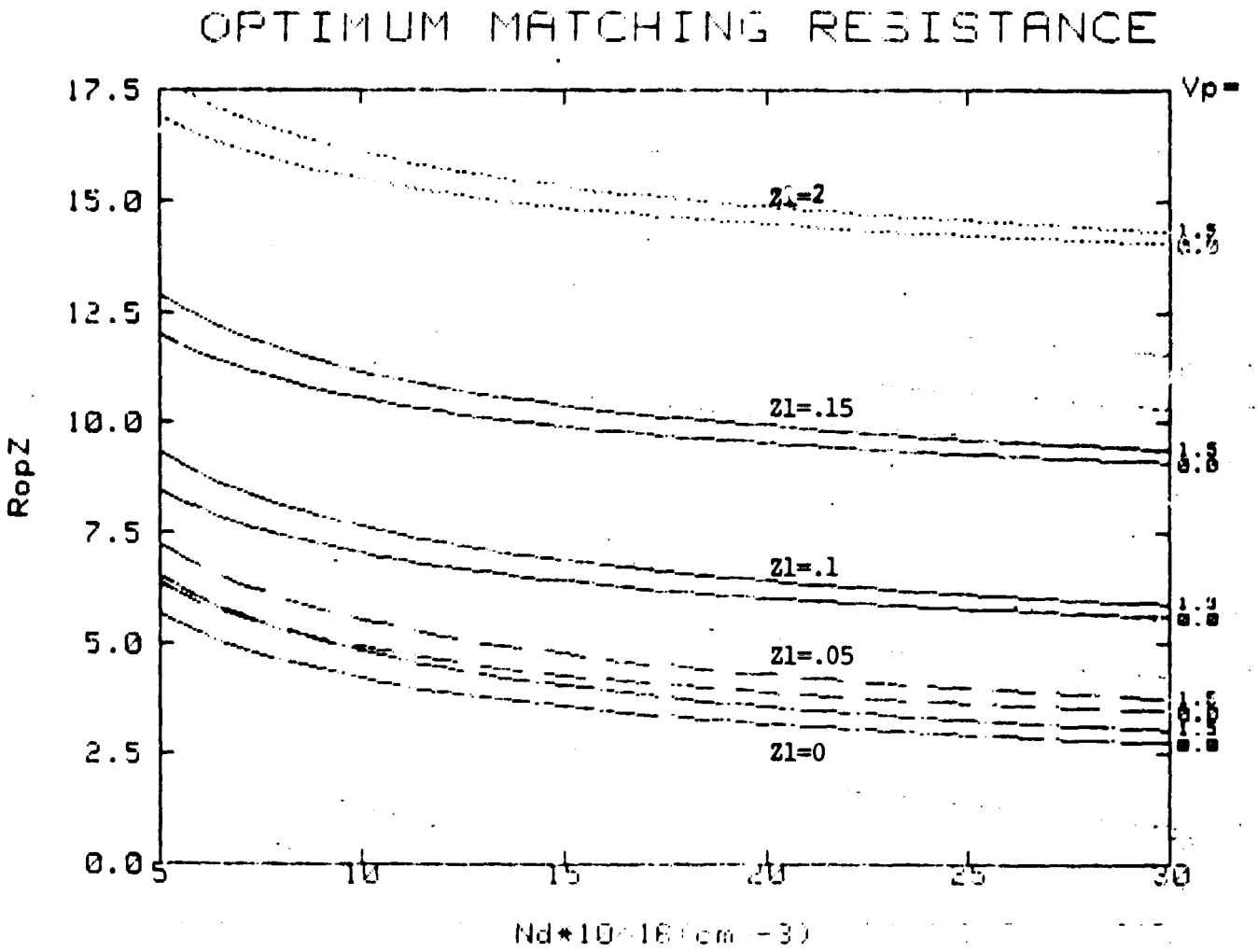


THIS GRAPH SHOWS THE GaAs MESFET LNA MAXIMUM AVAILABLE GAIN .vs. THE CHANNEL CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0, .75 AND 1.5, AND GATE SEGMENT WIDTHS (FINGERS) Z1=0.0, .05, AND .1(um).

Z1= 0(BROKEN SOLID), .05(LARGE DASH), AND, .1(SOLID)
Vs=1.4*10^7(cm/s), L=.3(um), h=.5(um), f=20 GHZ, INDP. OF Z

IT IS ASSUMED THAT BOTH THE SOURCE-LEAD INDUCTANCE AND THE DRAIN-GATE FEEDBACK CAPACITANCE ARE SMALL AND SO THEY ARE NEGLECTED.

Figure 3.7



THIS GRAPH SHOWS THE GaAS MESFET LNA OPTIMUM MATCHING RESISTANCE .VS. THE CHANNEL CARRIER CONCENTRATION FOR PINCHOFF VOLTAGES Vp=0.0 AND 1.3, AND PARALLEL GATE SEGMENT WIDTHS Z1=0.0, .05, .1, .15, AND .2 (mm).

Z1= 0(BROKEN SOLID), .05(LARGE DASH), .1(SOLID) .15(SHORT DASH), .2(DOTTED)
L=.3(um), h=.5(um), f=20 GHZ, INDP. OF Z

Figure 3.8

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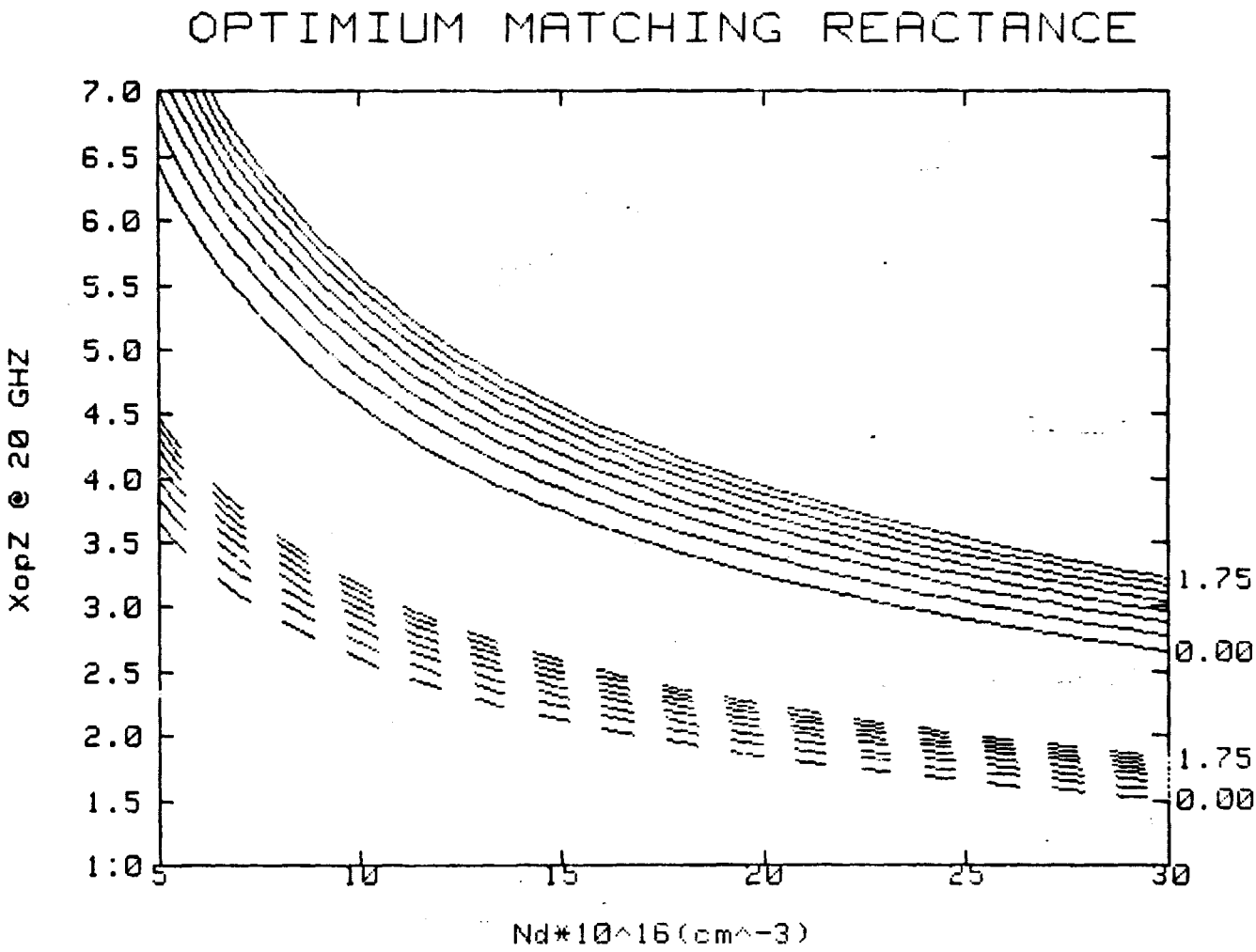

THIS GRAPH SHOWS THE RELATIONSHIP BETWEEN THE LNA. GaAs GATE REACTANCE (PER UNIT GATE WIDTH (mm) .VS. CARRIER CONC.,FOR VARIOUS PINCHOFF VOLTAGES.

GATE LENGTH = .3(SOLID LINE), =.7(DASHED LINE)

Figure 3.9

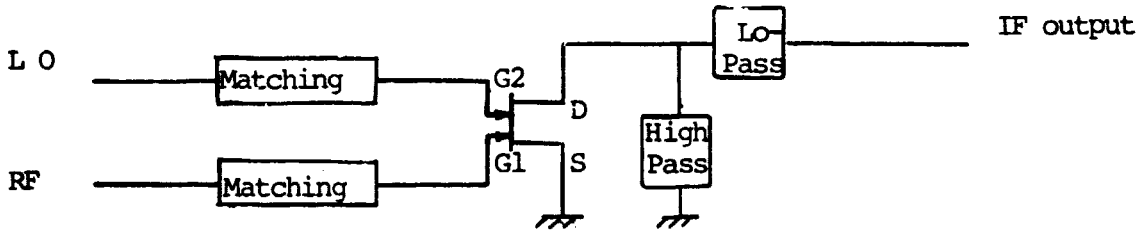

Figure 3.10 Dual-Gate MESFET Mixer

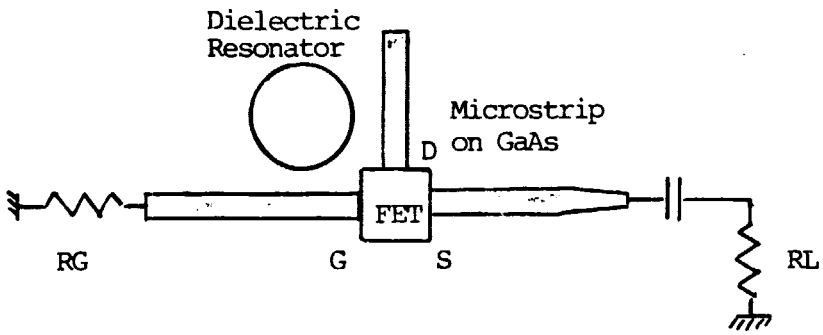

Figure 3.11 FET Dielectrically-Stabilized Oscillator

efficiency when operated at 30 GHz; however the sub-micron gate length technology achieved for low-noise amplifiers at these high frequencies are adequate to afford proper mixing.

In the modem block diagram shown in Chapter 2 we assumed direct-conversion to baseband in the receiver, meaning the L.O. is at the desired RF carrier frequency. This has the obvious advantage of avoiding IF stages and additional mixers, oscillators, etc., and eliminates the image noise problem as well. This homodyne detection has usually been avoided in other receivers for several reasons: (1) 1/f noise of diode mixers predominates at low frequencies, requiring considerable RF gain to overcome this noise source; (2) it is difficult to achieve any channel selectivity at RF (would require tunable narrow-band filters) and adjacent channel signals must be extracted at baseband at the mixer output; and (3) frequency-tuning and bandpass filtering is more easily done at an IF frequency. We believe these concerns are not so important for the case at hand because the signal is rather wideband (~ 1 GHz) making it necessary that the IF be probably 3 GHz or higher anyway, and we believe channel tuning and selectivity can also be handled, due to the wide bandwidths involved. Direct conversion does argue for large RF gain to overcome 1/f noise and to help the problem of I and Q channels needing equal gain. In monolithic form, this extra RF gain required over a heterodyne receiver is a relatively cheap commodity.

3.1.5 Oscillators

Microwave-frequency signal sources have traditionally been obtained by frequency-multiplying of a low-frequency (~ 100 MHz) crystal

source, or by Gunn-effect devices. The former approach is complex circuit-wise, needing filters to extract the proper harmonic and is inefficient as well. Gunn oscillators are also inefficient (DC-to-RF) and have rather poor phase noise characteristics. Recently GaAs MESFETs have become popular at high frequencies, particularly when stabilized with a high resonator in the feedback loop. This resonator is typically a dielectric "pill" placed adjacent to a transmission line, to which coupling is very good at a desired frequency. The resonator is basically a resonant cavity whose size determines its resonant frequency, hence the oscillation frequency of the circuit. Earlier materials had poor temperature stability, causing the frequency to shift with temperature. Barium titanate is a preferred dielectric now which has greatly reduced the temperature sensitivity.

As was the case for the transmission line devices, the resonator itself makes the oscillator relatively large. Figure 3.11 shows a schematic diagram for a dielectric resonator oscillator.

An oscillator stability of about 5 ppm (5×10^{-6}) at the transmitter, on a 20 GHz carrier, gives a frequency uncertainty of 100 KHz. This is small considering the channel bandwidth of at least 1 GHz, and the fact that the receiver phase lock loop will synchronize to carrier offsets of perhaps 10 MHz. The stability above can be relaxed somewhat if difficult to achieve.

The local oscillator of the receiver can perhaps avoid the resonator-stabilization and use transmission line coupling for the feedback condition. We, in fact, desire this oscillator to be voltage-tunable over ±10 MHz, obtained typically by d.c. biasing a

varactor diode to achieve a variable capacitor. The long-term stability of the receive oscillator must only be good enough to allow synchronization to the transmitted signal.

3.1.6 Comparators, or A/D Converters

In the digital detection portion of the receiver, a filtered I or Q channel signal must be compared with zero in the QPSK case, or with a three-level set of thresholds in the QASK case. In A/D converter parlance we need a 1-bit or 2-bit converter, respectively. The conversion time must be a fraction of the symbol time (2 nsecs), assumed to be 0.5 nsec. The flash-comparator structure is not complex due to the small number of thresholds. Upadhyayula et al. [27] recently reported a GaAs MESFET 3-bit converter capable of conversion in 0.2 nsec with power consumption of about 400 mwatts for 2-bit conversion. The circuit of Figure 3.12 shows their comparator circuit. In the QASK case these would be three such comparators, whose outputs are decoded by simple gates to 2-bits per sample and latched. The voltage thresholds are determined by the ratio of the width of the load FET to that of the switch FET, parameters which can be tightly controlled. FET pinchoff voltages of 5-6 volts were used, assuming a 2 volt input signal. Doping was 10^{17} cm^{-3}, with 1 μm gate lengths employed.

3.2 GaAs IC FABRICATION PROCESSES

Conductive channel formation on GaAs is accomplished through two basic methods: epitaxial layer growth or ion-implantation. Epitaxial layers have been used on a variety of discrete GaAs devices since the late 1960's including the optical devices (lasers, photodetectors and LED's) and the microwave (FET, IMPATT and Gunn) devices. A large

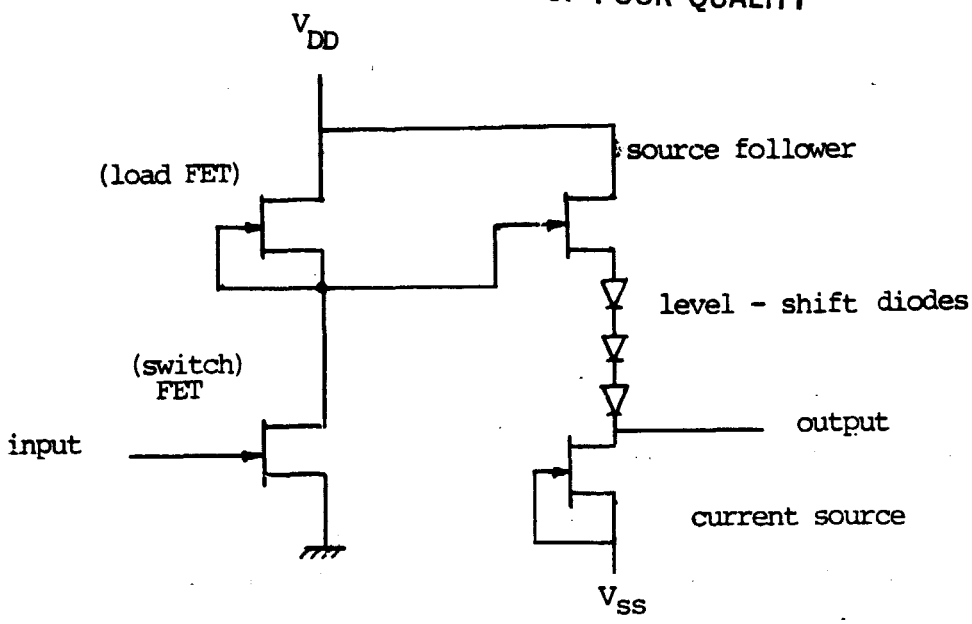

Figure 3.12 Voltage Comparator

fabrication technology base has been accumulated for device processing. Ion implantation technology in GaAs has only advanced in the past five years with the availability of high quality semi-insulating Czochralski grown GaAs. The advantage of round wafers allows automated processing whereas the previously available Bridgman grown substrates were "D" shaped and somewhat irregular.

3.2.1 Epitaxial processes

A variety of epitaxial processes have been used in FET fabrication namely: liquid phase epitaxy, chemical vapor deposition, and molecular beam epitaxy.

Liquid Phase Epitaxy (LPE) is used for discrete microwave FET fabrication because it is simple and a much less expensive process. Layer thickness control and variation is extremely difficult to maintain and precise etching is usually required to achieve the correct layer thickness. It is not easily used for IC fabrication because of the large variation of layer thickness over a wafer, and also is typically a single wafer process. Scaling the process for throughput of multiple wafers has been achieved but not with the precise layer doping and thickness control necessary for IC fabrication.

Chemical Vapor Deposition (CVD) or Vapor Phase Epitaxy (VPE) has been the method of choice for large area GaAs substrates because of the very uniform layer doping and thickness. Also, the system is easily scaled so that multiple wafers may be processed in a single run. A wide range of doping concentrations are achievable and thin layers (< 1000Å) are possible using computer controlled gas flow systems. Three different transport systems are typically used: $AsCl_3$, AsH_3, and metal

organic (MOCVD), all of which have been shown to achieve similar results in terms of uniformity, layer thickness control, and device performance. The $AsCl_3$ process has a slight advantage in crystal quality and repeatability ([1], p. 96) but that advantage may be overshadowed by the excellent thickness control (±100 A) available in MOCVD.

Molecular Beam Epitaxy (MBE) exhibits very good layer thickness and doping control (±few percent), easily variable doping and extremely abrupt layer interfaces. Heterojunctions are easily accomplished as are varying doping profiles. Until recently MBE was only used for research but machines with 2 inch substrate capability are now available. The system is quite expensive (> $500,000) and although MBE is a single wafer at a time process, a few wafers per hour may be fabricated in a single machine. MBE offers potential advantages where extremely thin layers or multiple layers of varying doping are necessary.

3.2.2 Ion Implantation

Ion implantation (II) allows precise control of thickness and doping of the active channel. Through recent improvements in annealing cycles, extremely high activation (~90%) and channel thickness control are achieved. Multiple dose and energy implants may be used to fabricate conducting pathways of differing resistivity, and also to tailor the channel layer profile somewhat. Abrupt changes in carrier profile are not feasible. The important advantages of ion-implantation are the ability to control the pinchoff voltage, the relative ease of fabrication, and allowance for processing of multiple three or four inch diameter wafers in a single run. Also, ion implantation allows a

ION IMPLANTED SELF ALIGNED GATE FET

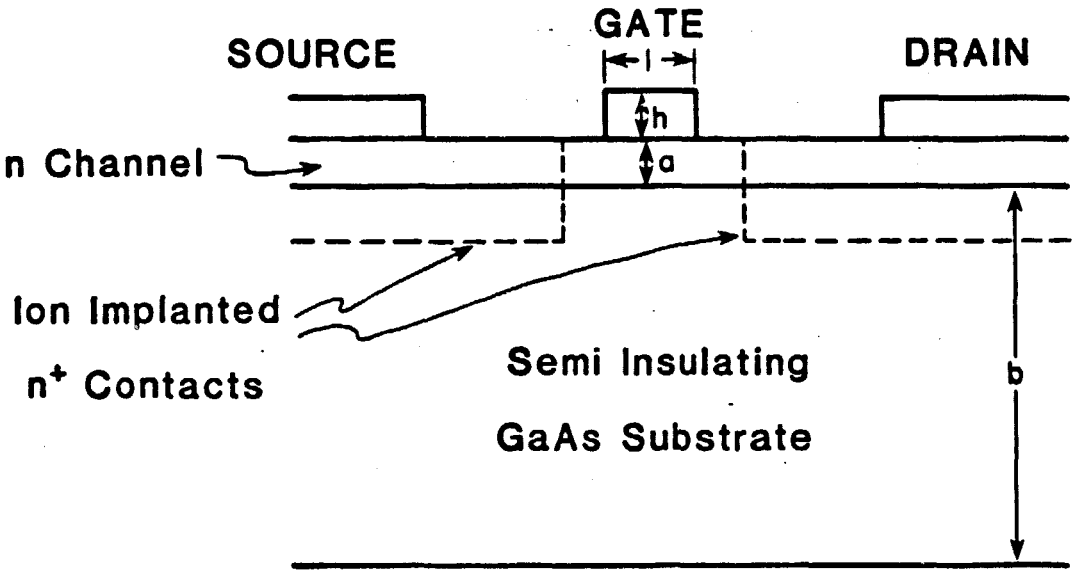

Figure 3.13 Self-Aligned Gate FET

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RECESSED GATE FET

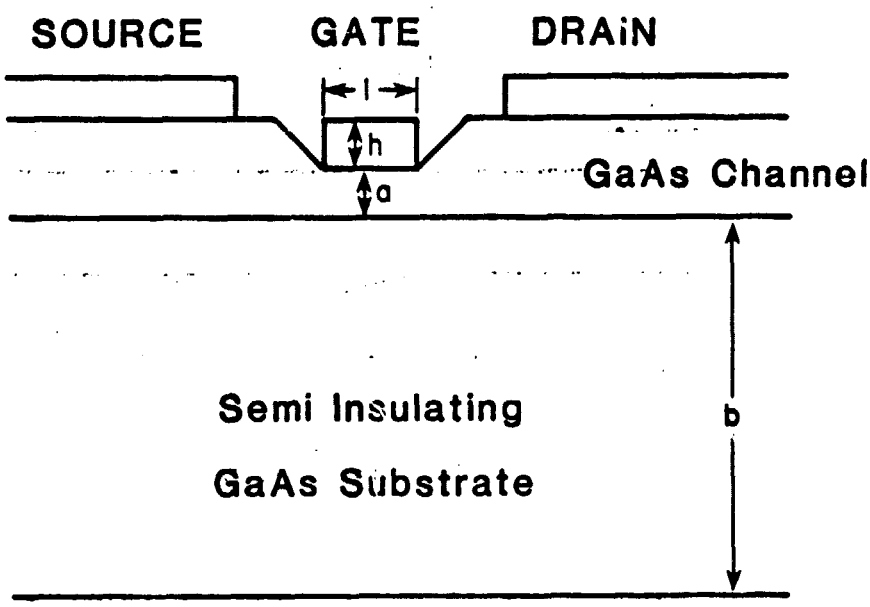

Figure 3.14 Recessed Gate FET Geometry

self-aligned gate process where the gate metalization acts as the mask for source and drain contacts, thereby neglecting the need for careful mask reregistration in the gate area. Self-alignment is particularly important in IC fabrication where gate spacing and positional accuracy must be maintained over a large area (> $1mm^2$) and a large number of devices (> 1000).

IC's may be fabricated by ion-implantation directly into a semi-insulating GaAs substrate, or into an epitaxial layer. Initial work utilized implantation into epitaxial layers to achieve the high crystal quality and low defect structure of epitaxial material and the doping control of implantation. Direct implantation into a GaAs substrates has become a viable process with recent improvements in crystal defects and thermal stability of LEC GaAs substrates. In addition, a totally ion implanted process has fewer processing steps and therefore is simpler and has potential to be a higher yield and less expensive process.

3.2.3 Self-Aligned Gate Process

The self-aligned gate process has recently been exploited for remedying the problems of precise mask alignment for channel doping and gate delineation. Two critical factors limiting MESFET performances and yield in conventional IC processing are the precise gate recess etch used in V_p control and the precise gate alignment relative to existing channel regions for reducing the source resistance. Ions are often implanted under the source and drain contacts to reduce the contact resistances, and between the gate and the source and drain to reduce the channel resistances. The spacing between the n^+ region and the gate is

typically between 500Å to 2000Å. Shorter spacings give higher capacitances and longer spacings yield high channel resistances. The self-aligned gate process avoids the problem of needing critical mask alignment in forming these small spacings by using the gate metal (buried contact technique) or the gate metal resist (T-gate technique) as an n^+ ion mask.

In the buried contact technique, the gate metal is delineated, its resist removed, and n^+ ions are implanted with the gate metal as a mask. This results in zero spacing between the n^+ region and the gate metal, thus causing increased capacitance. In the T-gate technique the gate is delineated by a plasma etch that results in a gate length shorter than the overhanging gate resist. Next, ions are implanted, resulting in an n^+ region-gate spacing of length equal to the length of the resist overhang. With proper resist overhang length, the gate capacitance is not increased and the increased channel resistance is negligible.

3.2.4 Process Assessment and Conclusions

Direct ion-implantation into a semi-insulating GaAs substrate has been shown capable of producing both digital logic and low noise amplifier structures necessary for this modem development. Pinchoff voltage control is easily achieved and self-alignment of the gate offers less restrictive processing tolerances. Large area substrates may be used, thereby decreasing the cost per chip and potentially increasing yield and uniformity. Epitaxial IC processes are also reported in the literature but the advantages of precise V_p control, the ability to use

multiple implantations, and the continual improvement in the implantation process give ion-implantation the distinct advantage.

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4. CONCLUSIONS

Advanced communications techniques have been studied for application to future communication satellite needs, with the assumption of roughly 1-2 Gbps channel throughputs. This assumption led us to focus on quadrature modulation techniques and simple continuous phase modulation techniques as power and bandwidth efficient methods which are relatively easy to realize in hardware. Out of this study has come the definition of a dual-mode (QPSK/QASK) technique which affords a high-level of system flexibility with very little hardware reconfiguration. We believe this technique is a good candidate for circuit integration in monolithic form to produce a several chip modem handling Gbps rate.

In parallel we have investigated current GaAs technology as it applies to such a modem development. No significant technical barriers seem in the way, with integration and compatability issues remaining foremost. The GaAs MESFET provides a building block capable of performing all of the various linear and nonlinear device functions of amplification, phase modulation, mixing, threshold detection, etc.

Our recommendations for further work are:

(1) Further analyze the dual-modem technique, especially the synchronization and data filters, to be able to clearly define the performance requirements; some of this work is currently being studied with aid of a lower speed (1 Mbps) prototype modem operating at a 10 MHz carrier frequency.

(2) Study the binary CPM, $h = 1/2$ schemes with regard to very high-speed implementation with quadrature-type receivers; synchronization circuitry is a key item here as well.

(3) Characterize at the chip level the functional design of the modem in GaAs monolithic circuit forms. This will produce a more detailed picture of the chip area required, its gate complexity, and the power requirements. Recommendations on device geometry and processing techniques will also be produced.

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