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DEVELOPMENT AND FABRICATION OF AN AUGMENTED POWER TRANSISTOR

M. J. Geisler, F. E. Hill, and J. A. Ostop
Westinghouse R&D Center

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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16 Abstract

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An important aspect of this program has been the development of a passivating glass technique to shield the device high-voltage junction from moisture and ionic contaminants. One other major task has been the development of an isolated package that separates the thermal and electrical interfaces. A new method has been found to alloy the transistors to the molybdenum disc at a relatively low temperature.

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1. SUMMARY

The main objective of this program has been the development of device design and processing techniques for the fabrication of an augmented power transistor capable of fast-switching and high-voltage power conversion. The major device goals have been sustaining voltages in the range of 800 to 1000 V at 80 A and 50 A, respectively, at a gain of 14. The transistor switching rise and fall times were to have been both less than 0.5 μsec.

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The measured electrical performance compares well with the predicted optimum design specified in the original proposed design. A 40 mm diameter transistor has been fabricated with seven times the emitter area of the earlier 23 mm diameter device.

2. INTRODUCTION

It has been well established that the bipolar transistor is the preferred power-switching component for a large number of power electronics applications. It is a fast and efficient switch and relatively easy to manufacture when compared with other devices which have similar performance capabilities. Presently, there are two important trends in the transistor industry. One trend is to increase the device area so that high currents and higher voltages can be achieved. The second trend involves improvements in characterization methods and an understanding of the turn-on and turn-off process. Only a few years ago the bipolar power transistor was viewed as a mature device with little opportunity for major technical advancements. Since the late 1970s, high-voltage fast-switching transistors have progressed from the 1 cm^2 (D60) conducting area to the present 7 cm^2 area, which represents an increase in current-handling capability of seven times. Increases in sustaining voltage can also be made using this area factor, although the factor is governed by a square law relationship which makes it more economical to switch power at high currents than at high voltages.

This report describes work which makes use of results obtained under previous NASA contracts, NAS3-18916, NAS3-21380, and NAS3-21949, to develop a 40 mm diameter bipolar transistor. The device uses the well-developed triple-diffused process which combines high current densities with the ability to operate at high switching frequencies. With a collector-emitter sustaining voltage $V_{CEO}(sus)$ between 800 V and 1000 V, the device is capable of a power-switching product of approximately 60 KVA with an h_{FE} of 14 at 80 amperes.

A new glass passivation method has been developed for this device, capable of shielding against ionic contaminants with excellent

humidity resistance. In addition, the glass passivant, containing a negative charge, permits a large bevel angle at the slice edge resulting in a considerable saving in fusion area.

An added feature of the design is the encapsulation of the transistor into a power module that separates the electrical and thermal interfaces and dissipates at least 1100 watts of power.

This fast-switching device is expected to be used in high-power, pulsewidth-modulated applications where efficiency, size, and weight are at a premium. Some typical applications are motor speed control, 20 KHz arc welding, and pulsewidth-modulated voltage regulators. Transistors with very large current-voltage products are also desirable for urban mass transit vehicle auxiliary power supplies where small size and low weight improve the competitive position.

3. TRANSISTOR DESIGN

3.1 Background

The power-handling capability of a bipolar transistor is limited by its sustaining voltage and current-handling capacity. Its performance when operated as a high-power switch can be characterized by the device current gain, current density, saturation voltage, and switching times. A transistor design model developed during previous NASA programs has been used to predict minimum emitter area and collector material parameters for the designated voltage and current range. Newer design models have also been developed to predict forward safe-operating area, edge-termination field characteristics due to glass passivation, and device packaging and mounting constraints.

3.2 Design Procedure

The design of a high-power transistor switch must meet a number of requirements besides those of high-current gain and sustaining voltage. Limits must be imposed on switching times, peak current gain, reverse junction currents, steady-state power dissipation, and second breakdown performance. Many of these requirements can be met by making adjustments in the device design or processing, leaving the transistor optimization primarily dependent on the base impurity density, the collector concentration and width, and emitter area. With the transistor design model that was used, the optimization technique has been narrowed to a simple quadratic equation. This, along with the collector breakdown voltage relation, is used to find the minimum emitter area for a particular combination of device variables. The minimum area in some cases may conflict with switching times and peak current gain and, when applicable, priorities must be assigned.

Under conditions of base widening for a highly interdigitated emitter, the current gain in the common emitter configuration is given by Equation 1[1] as

$$h_{FE} = \frac{h_{FEO}}{1 + \frac{Q_O}{Q_B}\left(\frac{I_C}{I_O} + \frac{I_O}{I_C} - 2\right)} \qquad [1]$$

where I_O is the maximum collector current, G_B is the total acceptors per cm^2 in the metallurgical base region, and h_{FE} is the peak current gain. The quantities I_O and Q_O are related to the collector-emitter voltage V_{CE} where:

$$I_O = A_e\, q\, \mu_n\, N_D\, V_{CB}/W_n \qquad [2]$$

and

$$Q_O = N_D\, W_n\, (q\, V_{CB}/4KT) \quad . \qquad [3]$$

In the above expressions A_E is the effective emitter area, N_D is the collector impurity concentration, W_N is the collector-basewidth, and μ_N the electron mobility. The collector voltage V_{CE} is then:

$$V_{CE} = V_{CB} - V_{BE} \qquad [4]$$

where V_{be} is the base-emitter voltage.

Substitution of Equations 2, 3, and 4 into 1 yields the quadratic in A_E which can be solved to yield an optimum emitter area for a given collector current and gain. The input data and optimum design are shown in the computer output of Figure 1. In the output listing it can be seen that for the 1000 V sustaining voltage design, the effective emitter area is 7.68 cm^2. Table 1 shows the complete listing of material variables for both the 1000 V and 800 V design. A compromise in the design has to be made to be able to fabricate devices in the

New Input Data

$V_{CE} = 2.5$ V	$I_C = 50.0$ A
$V_{CEO}(sus) = 1000.0$ V	$h_{FE} = 14.0$
$T_J = 25.0°C$	$\tau = 50.0\ \mu s$
$DC = 23.0\ cm^2/s$	$\Delta E = .050$ eV

At Ref. Temp. the Program Uses:

$\mu_{CO}(25.0°C) = 1300.0\ cm^2/V\text{-}s$

$Ge = 7.48E+013\ cm^{-4}/s$

At T_J These Values Apply:

$\mu_{CO}(25.0°C) = 1300.0\ cm^2/V\text{-}s$

$Ge = 7.48E+013\ cm^{-4}/s$

Optimum Design

$AE = 7.68E+000\ cm^2$	$h_{FEO} = 28.9$
$N_C = 5.69E+013\ cm^{-3}$	$m = .750$
$W_C = 133.6\ \mu m$	$BV_{CBO} = 2093$ V
Rho, C = 84.5 Ohm-cm	$\tau = 50.0\ \mu s$

Figure 1. Input and output parameters for 1000 V design.

range of voltage and desired current since the collector material parameters are different for each voltage and current range. The higher resistivity was chosen for the background material so that the larger voltage was achievable and both collector-base thicknesses were processed to obtain the desired current levels at a gain of 14.

In the interest of knowing what performance can be obtained with the existing fusion area, an optional analysis was performed for this device by determining the maximum current possible for a current gain of

Table 1. Program Parameters

Symbol	Description	Value	
V_{CEO} (sus)	Sustaining Voltage	800V	1000V
I_c	Collector Current	80A	50A
W_c	Metallurgical Collector Width	104 μm	134 μm
N_c	Collector Donor Density	$5.69 \times 10^{13} cm^{-3}$	$7.0 \times 10^{13} cm^{-3}$
h_{FE}	Current Gain	14	14
h_{FEO}	Peak Gain	30.8	28.9
A_e	Effective Emitter Area	6.44 cm^2	7.68 cm^2

14 and 1000 V sustaining voltage. Figure 2 shows the computer output for the fixed emitter area showing the required collector parameters to obtain this maximum collector current. Using this analysis then, a curve of maximum collector current with respect to sustaining voltage was determined and is shown in Figure 3. The dotted curve shows the penalty that must be paid in current to offset the effect of current crowding in the emitter. The curve shows the family of devices possible with this fusion diameter; however, at currents above 100 A, some alteration of the emitter fingers must be made along with a means of reducing the voltage drop in the base due to the very high base currents. A narrowing of the emitter fingers would also require an adjustment in the emitter preform and the base drop could be reduced by the addition of a base insert (see contract # NAS3-18916). Photolithography and emitter patterning techniques also become more difficult as the maximum I_c is increased and emitter fingers become narrower.

3.3 Mask Design

To determine the mask layout for a high-current transistor it is necessary to know how the emitter current density varies over the fusion area; this is determined in first-order approximation by the sheet resistances of the base and emitter metallization and base diffusion. In reality, a uniformly current-distributed emitter never occurs because base current flow under the emitter results in current crowding at very high collector currents. An optimally designed emitter will be wide enough to be within the resolution of the photoresist and accommodate the emitter preform, and narrow enough to make the fingers efficient in the current-crowded mode. For the 80 A device which has a current density of 11.5 A/cm^2, an emitter finger width of 20 mils will make the most efficient use of the available area and be able to accommodate an emitter preform with fingers slightly narrower than the emitter metallization. For no change in the 7.68 cm^2 emitter area, any increase at all in the emitter current must be accompanied by a decrease in emitter finger width depending on the current value. The periphery of the total

New Input Data

V_{CE} = 2.5 V	Ae = 7.6 cm
V_{CEO} (sus) = 1000.0 V	H_{FE} = 14.0
TJ = 25.0 Deg. C	τ = 50.0 μs
DC = 23.0 cm^2/s	ΔE = .050 eV

At Ref. Temp. the Program Uses
μCO(25.0 C) = 1300.0 cm^2/V–s
Ge = 7.48E + 013 cm^–4–s

At TJ These Values Apply·
μCO (25.0 C) = 1300.0 cm^2/V–s
Ge = 7.48E + 013 cm^–4–s

Optimum Design

IC = 4.95E + 001 Amps	h_{FEO} = 28.9
NC = 5.69E + 013 cm^ –3	m = .750
WC = 133.6 μm	BVCBO = 2093 V
Rho. C = 84.5 Ohm-cm	τ = 50.0 μs

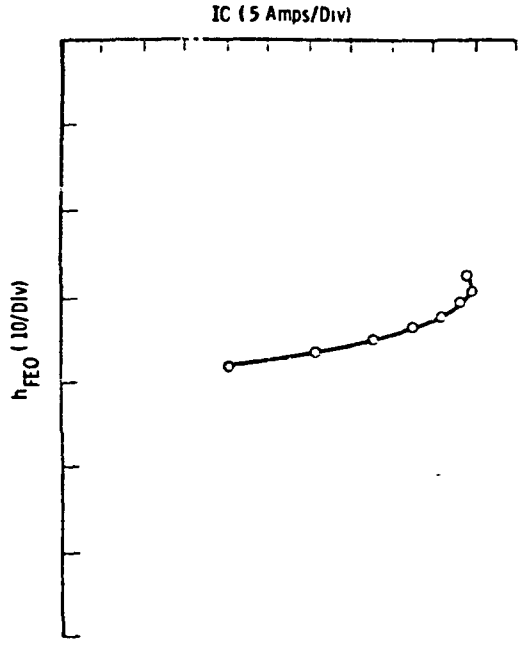


Figure 2. Maximized curve of collector current for 1000 V case.

Curve 743957-A

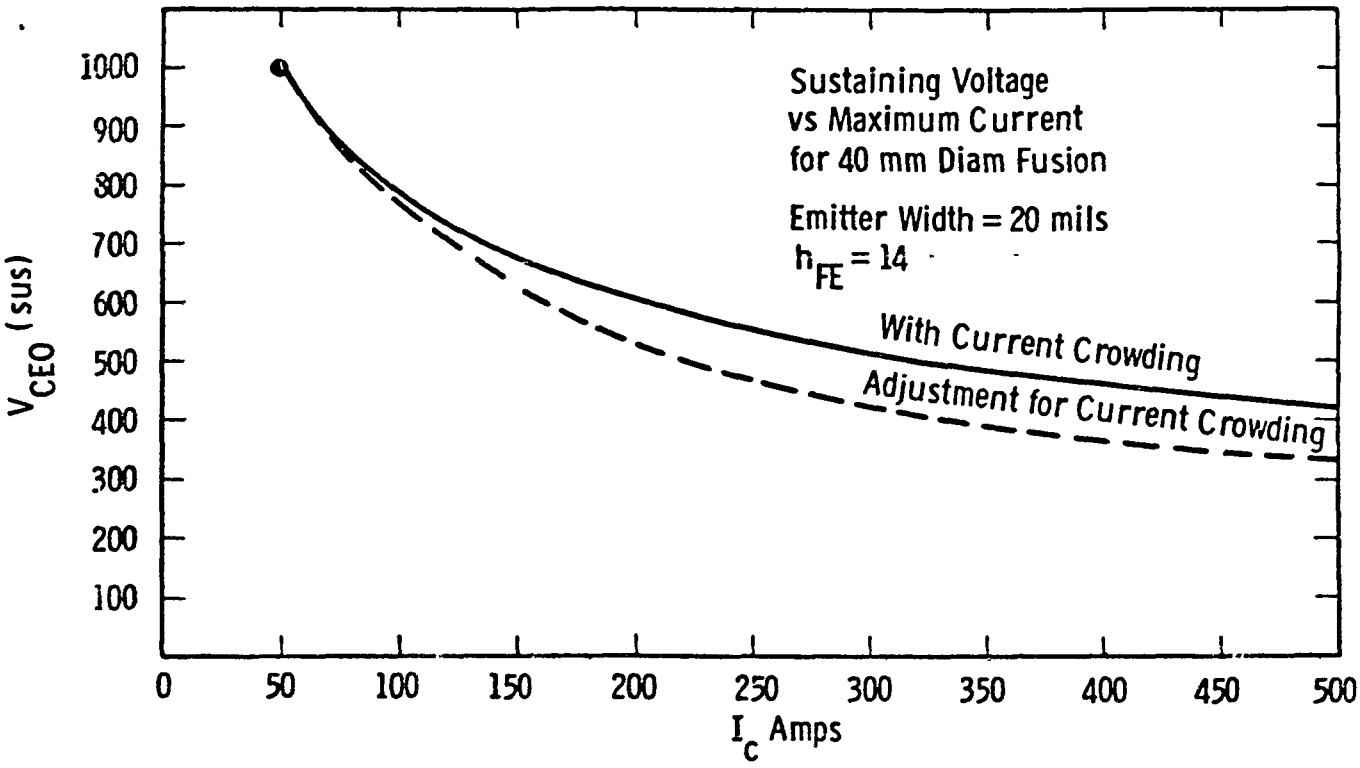


Figure 3. Sustaining voltage versus maximum current.

area for the 80 A design is approximately 3 meters in total length; therefore, any decrease in emitter width will require an increase in this periphery to accommodate the same effective area as calculated in the original computer output.

A 40 mm mask set has been designed using the above 80 A design rules, although this set can also be used on the 50 A device since the current level is lower. The metallization mask shown in Figure 4 is designed with 4 mil wide base fingers, a 3 mil separation between base and emitter, and a 30 mil trunk width. These are adequate to reduce the base contact voltage drop and deliver the required current to the emitter region. A 10 μm thick aluminum metallization is also required to implement the above design rules. This metallization is approximately

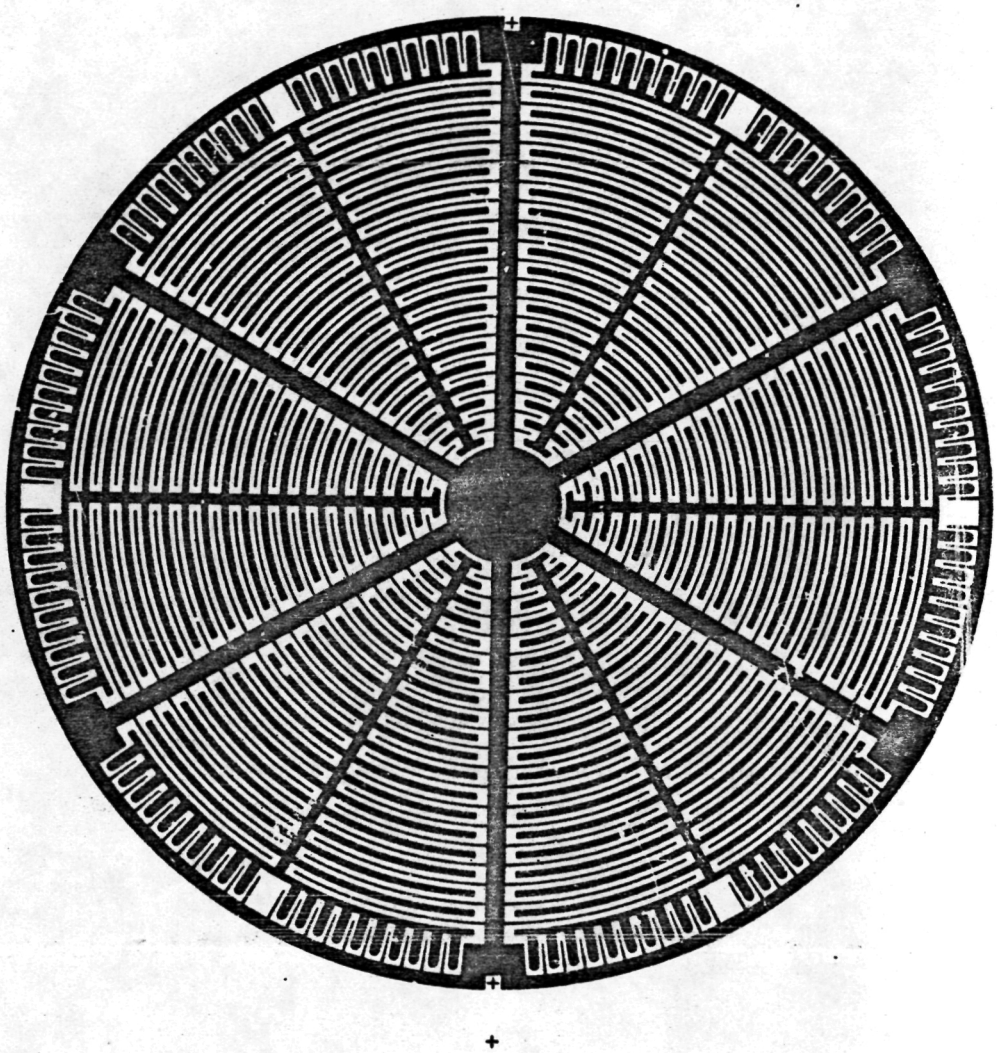


Figure 4. Metallization mask showing 40 mm layout.

twice the thickness of the aluminum used on previous fusions fabricated by the bipolar process. An allowance in mask dimension was made to compensate for the etch factor on this thickness of aluminum. A reinforcement bar was also included on the emitter preform mask for added support of the larger molybdenum disc.

3.4 Junction Termination

Power semiconductors with base regions extending to the device edge require some method for reducing the electric field and passivating the junction at the semiconductor surface. Various junction termination methods are available that reduce the surface avalanche breakdown below that of the semiconductor bulk breakdown. Contouring or shaping of the edge of the semiconductor has been done by many in the past to spread the voltage and reduce the field at the junction surface. With a negative bevel, the surface is mechanically ground so that it intersects the plane of the junction at an acute angle, usually 6° or less for breakdown voltages less than about 800 V, depending on the resistivity of the background material. For higher breakdown voltages, however, much shallower bevel angles are required and these tend to be very wasteful of surface area. For example, a 1° bevel which is required for a 1000 $V_{CEO}(sus)$ bipolar transistor will consume approximately 2 cm^2 more area than a 6° bevel. Since the total emitter area for this device is 7.68 cm^2, this represents an approximately 25% increase in the current rating of the transistor if a 6° bevel is used rather than the 1° bevel.

One method[2] that requires very little area of the available top surface of the fusion is the substrate etch technique shown in Figure 5. The etch technique proceeds from the substrate side of the wafer requiring only a very narrow isolation etch at the top surface of the device. Figure 6 shows the breakdown voltage of a junction with and without the substrate etch groove. The upper curve is the breakdown of the junction with the isolation groove only and the lower shows the improvement in breakdown voltage provided by the substrate etch.

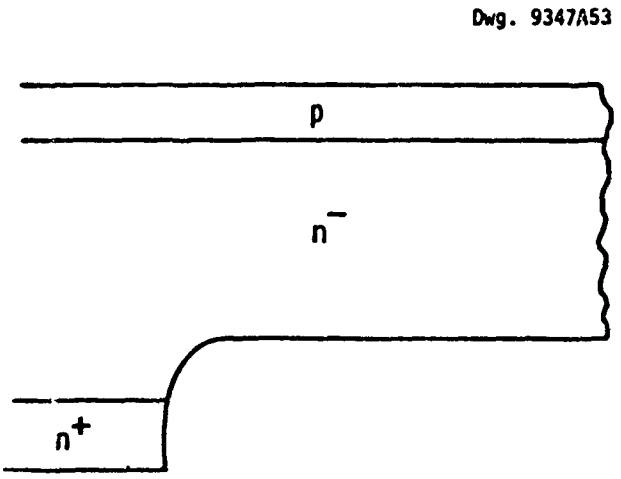
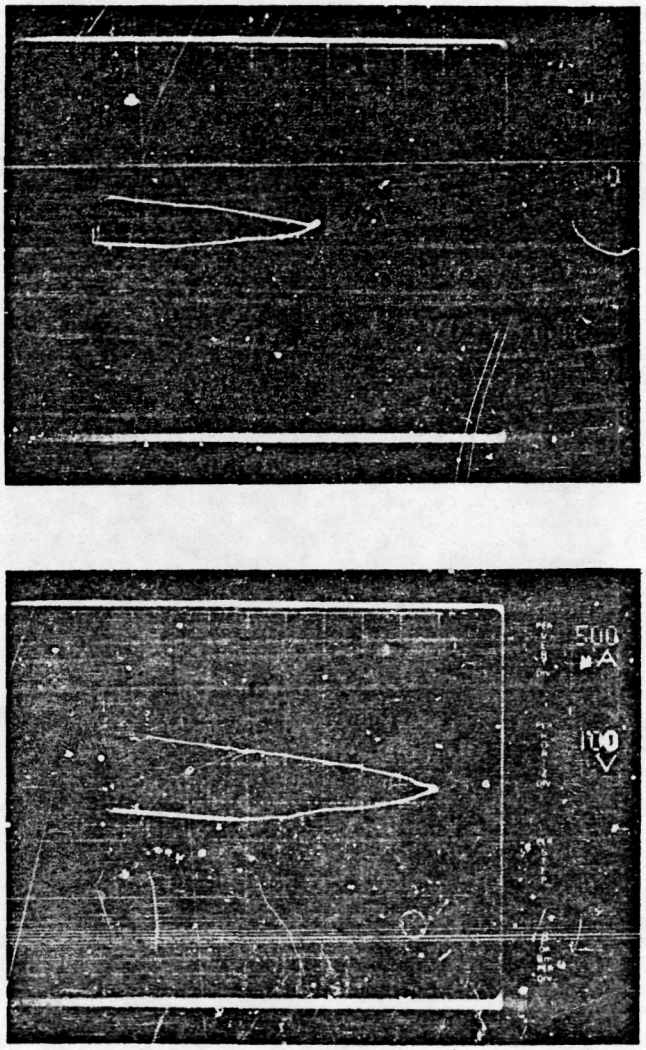


Figure 5. Substrate etch geometry for reducing surface field.

The main disadvantage of this method is the high loss in yield attributed to breakage at the edge of the wafer. This breakage is due primarily to the strain put on the fusion during the compressive force applied when the devices are packaged. A number of devices were made using this technique with sustaining voltages above 1200 V, but yields were very low due to the breakage described above.

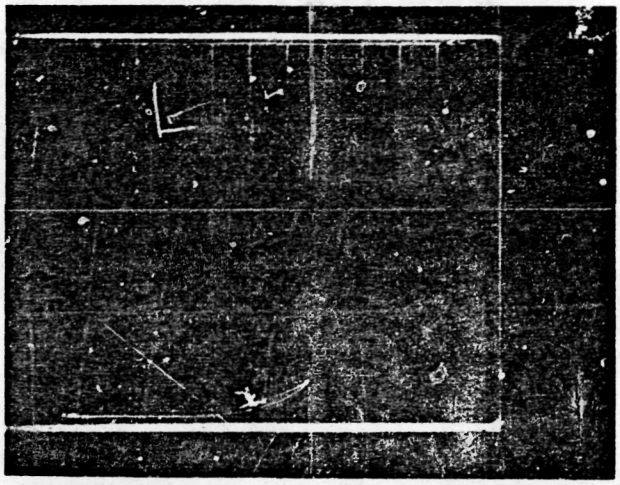
A higher yield process achieves the same high blocking voltage using a 6° bevel and a negatively charged passivating glass. The glass contains several metallic oxides and when fired to the silicon surface produces a spreading of the voltage at the surface reducing the maximum field. This has the same effect as a negative bevel such that in reducing the field it transfers the breakdown of the junction to the bulk-limiting condition. When used in conjunction with the 6° bevel, a breakdown voltage at the junction of 1800 V is possible for a background resistivity of 85 ohm-cm. An example of the improvement in breakdown voltage using this glass is shown in Figure 7, which shows the junction



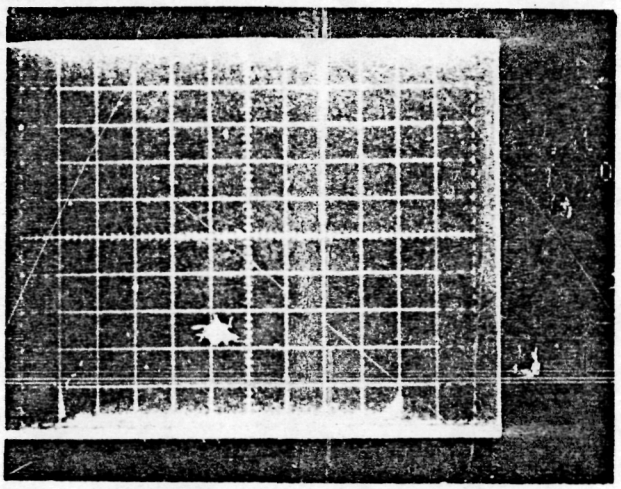
With Isolation Groove Only

With Isolation Groove and Substrate Etch Groove

Figure 6. Breakdown before and after substrate etch groove.



Edge Termination With Bevel Only



Edge Termination With Bevel and Glass

Figure 7. Breakdown before and after glass passivation.

breakdown before and after the application of the glass. As seen, the breakdown voltage is increased from 1300 V to 1800 V by the negative charge in the glass.

The effect of this glass can be analyzed further by calculation of the potential distribution at the junction coated with glass with the edge perpendicular to the plane of the junction. The objective is to solve the Poisson equation in two dimensions using

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = - \frac{q}{\epsilon_0 \epsilon_S} \left[N_D(x,y - N_A(x,y) \right] , \qquad [5]$$

in the semiconductor bulk, and

$$\frac{\partial V^2}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = - \frac{1}{\epsilon_0 \epsilon_G} (Q_G) \qquad [6]$$

in the glass,

where ϵ_0 is the dielectric constant of free space, ϵ_S is the dielectric constant of silicon, ϵ_G is the dielectric constant of glass, and Q_G is the charge density in the glass. Standard numerical methods are used in the calculation of the potential distribution in a glass with zero charge and a glass with negative charge. Potential distributions calculated for the two cases are shown in Figure 8 and Figure 9, which also show the equifield lines. In Figure 8 for a glass dielectric constant of 10, reverse bias voltage of 1500 V, and zero glass charge, $Q_G = 0$, the maximum field occurs at the surface so that breakdown will occur there rather than in the bulk. In Figure 9, $Q_G = -2 \times 10^{14}$ cm^{-3} and the maximum field occurs within the bulk; thus, the breakdown will take place in the bulk. As for an exact breakdown voltage determination, it is difficult to predict a specific field distribution; however, we do know how the field is distributed for a particular negative charge. When the negative bevel is added along with the negative glass, the distribution also becomes very complicated and it becomes even more difficult to predict the breakdown voltage of the junction.

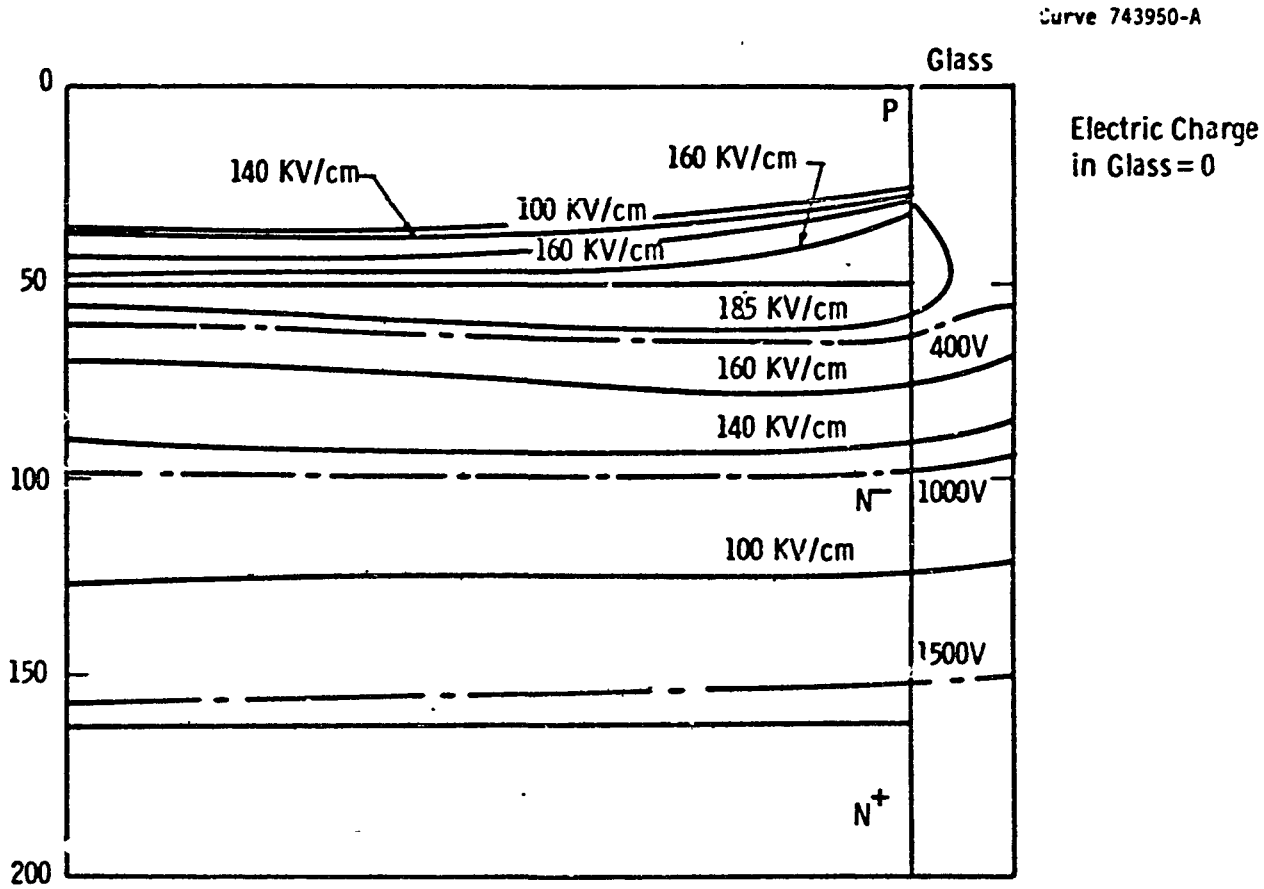
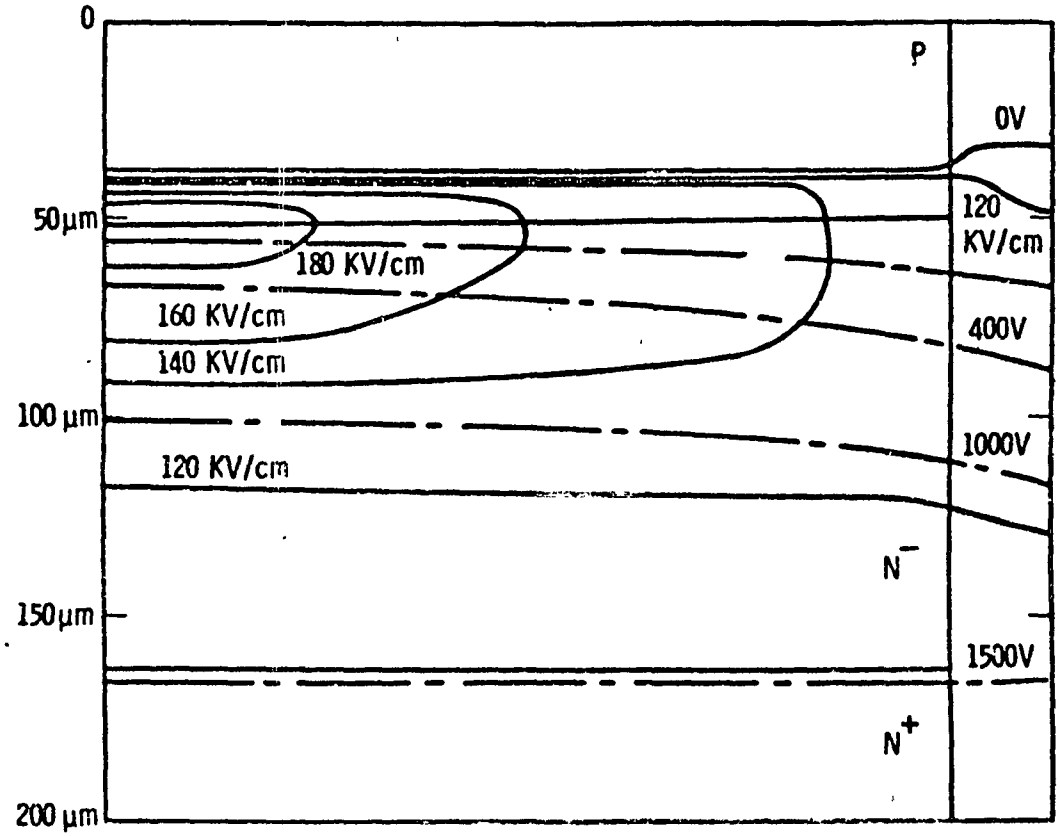


Figure 8. Equipotential and equifield lines at V_{app} = 1500 V for glass with no charge.

Curve 743951-A



Electric Charge in Glass = $-2 \times 10^{14} cm^{-3}$

Figure 9. Equipotential and equified lines at V_{app} = 1500 V for glass with negative charge.

4. PROCESS INVESTIGATION

4.1 Diffusion

The ability to combine a high-voltage breakdown and high current density while switching at high speed stems for the most part from the triple diffusion process. Two different methods of base diffusion were investigated during the course of this program with the aim of using the process giving the highest yield and best device characteristics. The closed-tube aluminum gallium process was used primarily because of the success obtained with this process in the diffusion of bipolar transistors on previous development programs. An alternate diffusion method, the open-tube gallium process, was also investigated because of its potential saving in process steps. This process also has the added advantage of higher yield because of the limited amount of slice handling as compared to the closed-tube process. The disadvantage with this process, however, is the low lifetime that is usually obtained. Lifetimes such as 50 μsec and 100 μsec are routinely obtained with the closed-tube process, but lifetimes over 20 μsec are difficult to obtain with the open-tube process. A minimum of 25 μsec is required in order for the emitter to be efficient enough to produce the desired current gain. Gettering methods which increase lifetime by removing impurities from the bulk material have been used with some success, although time did not allow further study of this diffusion.

4.2 Junction Termination

In order to avoid the problem of premature surface breakdown while using the least amount of surface fusion area, two different junction termination schemes were investigated. In one method, the substrate etch technique, a group of slices of 90 ohm-cm resistivity

were first diffused with a 3 mil deep phosphorus diffusion, then lapped to remove the N^+ region from one of the sides. Into this N^- region a 30 μ deep p-type region was diffused to form a junction in the N^- region capable of supporting 1800 volts when breakdown is not limited by the surface edge. By means of a photoresist mask, a narrow isolation groove was etched into the top surface to a depth of 3 mils. An edge profile of the etched slice in Figure 10 shows both the isolation groove and the lower substrate etch. For the lower substrate etch groove to be effective it must be deep enough to penetrate the upper depletion layer before the layer reaches the lower N^+ diffused region and must be at least as wide as the N^- region. The y parameter and x parameter must then both be greater than 3 mils. The primary advantages of this method are that the technique requires no more surface area than needed for the upper isolation groove and also that the lower etch groove can be mechanically etched with no need of registration with other surface geometries. The main disadvantage is the loss of device yield because of breakage at the edge of the slice when pressure is applied at the surface during encapsulation. This strain is concentrated at the etch grooves when the slice is alloyed and the slice and molybdenum backing disc are placed in compression and the combination assumes approximately a 1 mil bow.

An alternate junction edge-termination technique which also does not require an unusually large amount of fusion area is a negative bevel used in conjunction with a negatively charged glass. The glass has the effect of repelling electrons near the surface thereby lowering the electric field. This effect has been described in Section 3.4.

4.3 Glass Passivation

Glass passivation has been utilized in the past at the Semiconductor Division production facility for passivating high-voltage diodes and thyristors; however, conventional types of organic resins (alizerin, RTV, etc.) are still being used to passivate the high-voltage bipolar transistor. Due primarily to the high cost and processing

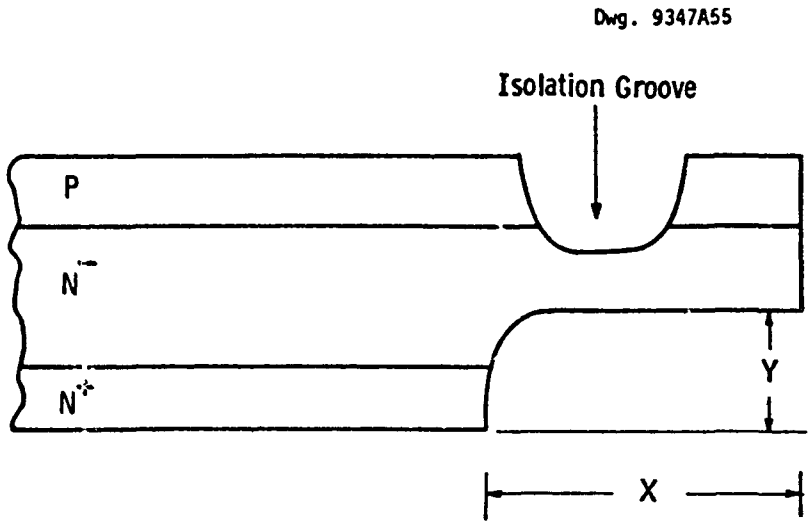


Figure 10. Slice edge profile showing substrate etch and junction isolation groove.

complexities, this process has not been used although it is highly desirable. There are a number of requirements for a glass passivant to be an effective barrier against ionic contaminants and moisture, yet not be sensitive to device temperature and processing procedures. Alkali ions in concentrations as low as a few hundredths of one percent, especially adjacent to the junction, result in serious instability of the junction. Along with this the coefficient of thermal expansion of the glass must match as closely as possible that of silicon to prevent cracking of the glass at the silicon interface. An ordinarily useful silicon dioxide film has a glass network structure that is very porous and is not a good barrier against moisture or alkali ions. If we were to use just simple glass, this substance would be attacked very easily because of its porous structure. With the addition of several metallic

oxides such as PbO and ZnO, the glass network is made very fine and mobile ionic free carriers and moisture can be kept free of the surface.

Glasses that contain a high percentage of zinc oxide have been used successfully as a passivating glass in the fabrication of the 40 mm transistor. The glass is a composite and also contains proportional amounts of boron oxide, alumina, and lead oxides to make it very closely match the thermal coefficient of expansion of silicon. The thermal expansion of silicon is very low ($3.3 \times 10^{-6}/^{o}K$) and, generally, glasses matching this thermal expansion have melting temperatures far too high for semiconductor devices. The thermal coefficient of expansion of this composite glass is $3.6 \times 10^{-6}/^{o}K$ and can be fired at 720°C with no harm to the silicon. Table 2 shows different glass types and some of their characteristics that make them attractive as silicon surface passivants. As seen in the table, one of the disadvantages in the use of this glass is the susceptibility to attack by acids. These are normally present in the aluminum and oxide removal steps, and the glass must be protected by some covering such as photoresist to prevent attack and in some cases a dry etch (plasma) must be used. The photoresist is then removed by a dry plasma etch or burned off during the final aluminum sintering step.

Another process constraint when using glass is that the melting temperature of the glass cannot be exceeded during the subsequent alloy step that bonds the fusion to the molybdenum backing disc. Reflowing of the glass tends to upset the firing-annealing cycle, which would be difficult to control during the alloy step. This problem can be avoided if the glass firing is done before the alloy and the alloy is carried out at a lower temperature.

4.3.1 Glass Application

The application of the glass to the silicon interface can be done in any of the number of ways shown in Figure 11. Silkscreening has been found to be the most efficient means of applying the glass for the following reasons:

Table 2. Glass Characteristics

Dwg. 4263B19

Type	Melting Temp	Layer Thickness	Coefi (Si = 3.3×10^{-6}/K)	Typ. App.	Chem. Behavior
ZnO Composite Base	700-730°C	> 50 µm	3.6×10^{-6}/K	H.V. Bipolar Diodes	Unstable in Acids
PbO, ZnO, B_2O_3, SiO_2	680-700°C	< 15 µm	4.6×10^{-6}/K	H.V. Bipolar Diodes	Unstable in Acids
B_2O_3	680-700°C	< 10 µm	4.7×10^{-6}/K	Thyristors	Stable in Acids Other Than HF
Al_2O_3	900-920°C	< 20 µm	3.95×10^{-6}/K	Thyristors	Stable in Acids Other Than HF

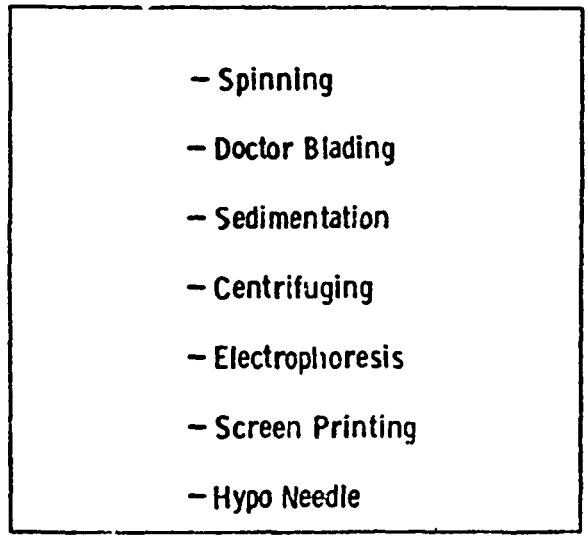


Figure 11. Methods of glass application.

1. selective application,
2. low incidence of voids in the mixture, and
3. production-oriented process.

An automatic thick-film screen printer which is used to apply the glass to the slice edge is shown in Figure 12. The glass is transferred to the slice in the form of a 1.5% solution of cellulose in butyl carbitol mixed with the glass powder. A small printing void in the glass near the junction can have a serious effect on the breakdown voltage of the junction. Given below are some of the common screen-printing problems along with their solutions.

- Composition of Material. Voids and pinholes are caused by poor screen snap-off and clogged screens. Low-viscosity glass will result in poor screen peel from the surface as well as pinholes. Clogged screens are the result of allowing the glass to dry on the screen between applications.

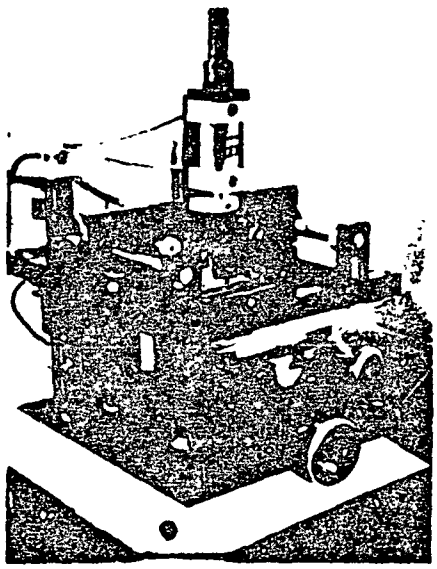


Figure 12. Screen printer for applying glass passivation.

- Printing Screen. The principal way to obtain correct glass thickness is to use the screen with the correct mesh count, wire diameter, and emulsion thickness. Generally speaking, a wider mesh will give a thicker glass but image resolution is better on narrower meshes.

The glass film screen-printing process contains many variables that must be controlled to obtain optimum results.

After the glass is applied to the surface and baked, the mixture is fired to bind it to the silicon interface. The temperature firing cycle and time interval are shown in Figure 13. The critical parts of the cycle are the glass-firing step and the annealing step, which relieves the stresses formed during cooling. Annealing of the glass is only needed to improve electrical results and lower current leakage levels. Shown in Figure 14 are some reverse breakdown characteristics relative to the firing cycle and their probable cause. The breakdown voltage characteristics of the junction before and after glass application are shown in Figure 7. It can be seen that the breakdown voltage is raised from 600 V to 1200 V after application of the negatively charged glass.

4.4 Alloying and Substrate Bonding

After the glass has been fired, an 80 mil thick molybdenum disc is then fastened to the bottom of the fusion by means of an alloyed aluminum contact. Aluminum 10 μm thick is evaporated onto the mating surfaces of the fusion and molybdenum then alloyed at a temperature below the glass-firing temperature. The attachment of the molybdenum disc to the fusion produces a warping or bimetallic effect between the two members that is dependent on molybdenum thickness, silicon thickness, and solder-freezing temperature. The optimum thickness for the molybdenum can be determined from solution of the Navier equation as shown in Appendix I. Figure 15 shows the amount of bow and the resulting stresses in the silicon plotted against the molybdenum substrate thickness. The silicon interface stress remains relatively constant no matter what the molybdenum thickness, but the surface stress varies greatly. It is actually zero at a moly thickness of 15 mils when

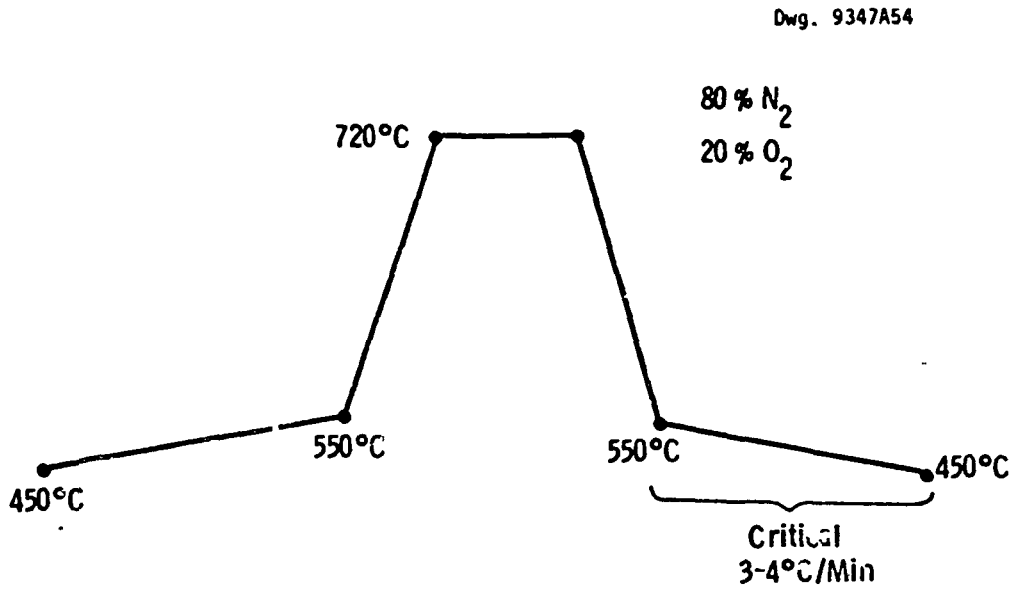


Figure 13. Glass-firing cycle.

it changes from being in tension to being in compression. Figure 16 shows the amount of bow versus moly thickness with the device diameter as a running parameter. A measured reading of .001 inch on the 1.5 inch diameter combination compares favorably well with calculations.

Alloy bonding of the slice to the molybdenum disc also presents the problem of an uneven solder penetration. The temperature and time cycle are shown in Figure 17 with the process being performed in a vacuum furnace. To reduce the penetration of aluminum into the silicon, the temperature excursion from 570°C to 600°C must be made as quickly as possible.

Excellent physical and electrical bonds have been made with this method shown by the ultrasonic scans in Figure 18. Good bonds are evidenced by an all-black image; any voids in the alloy appear as white spots in the scan. On the left the silicon wafer broken away from the moly verifies these particular measurements.

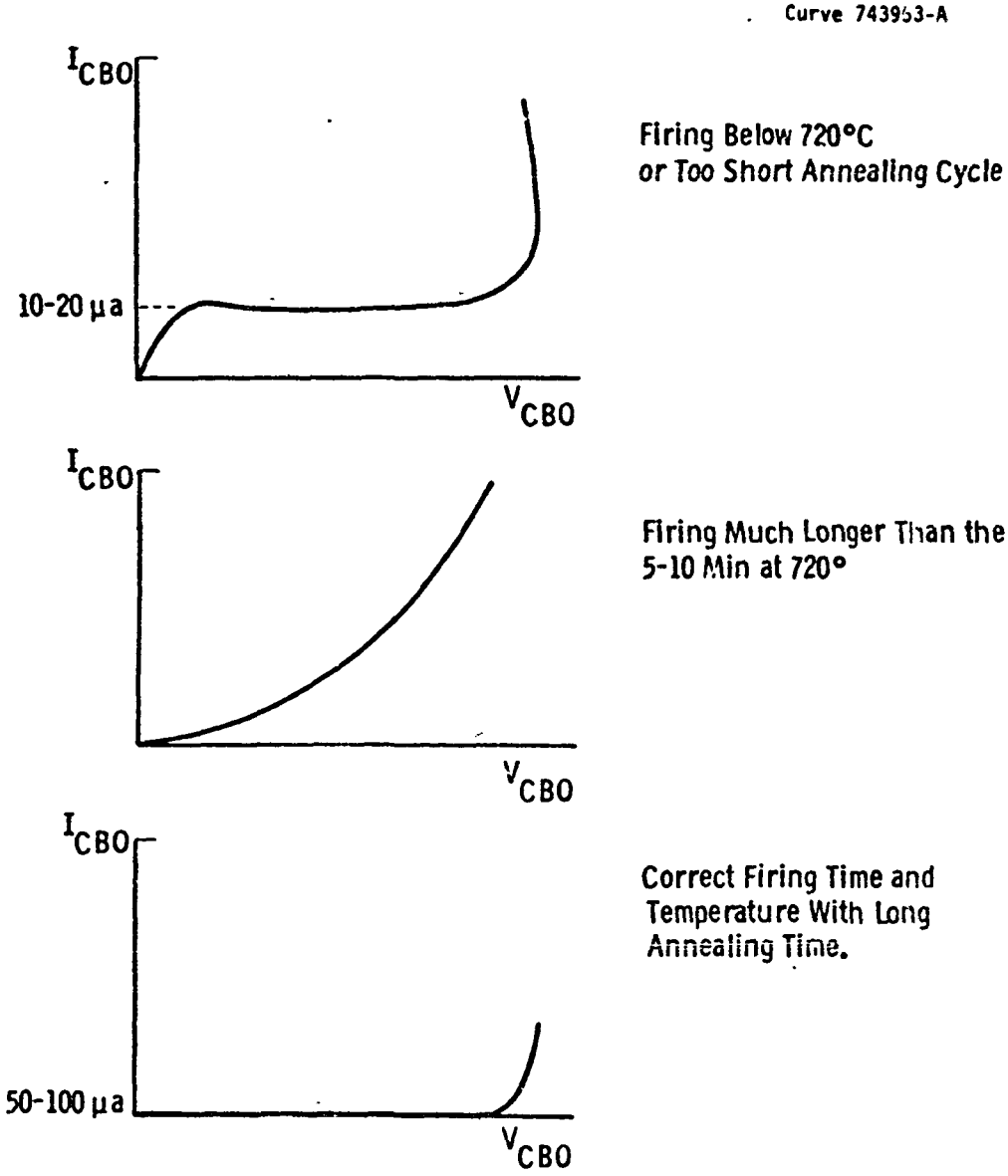


Figure 14. Reverse breakdown characteristics and their probable cause.

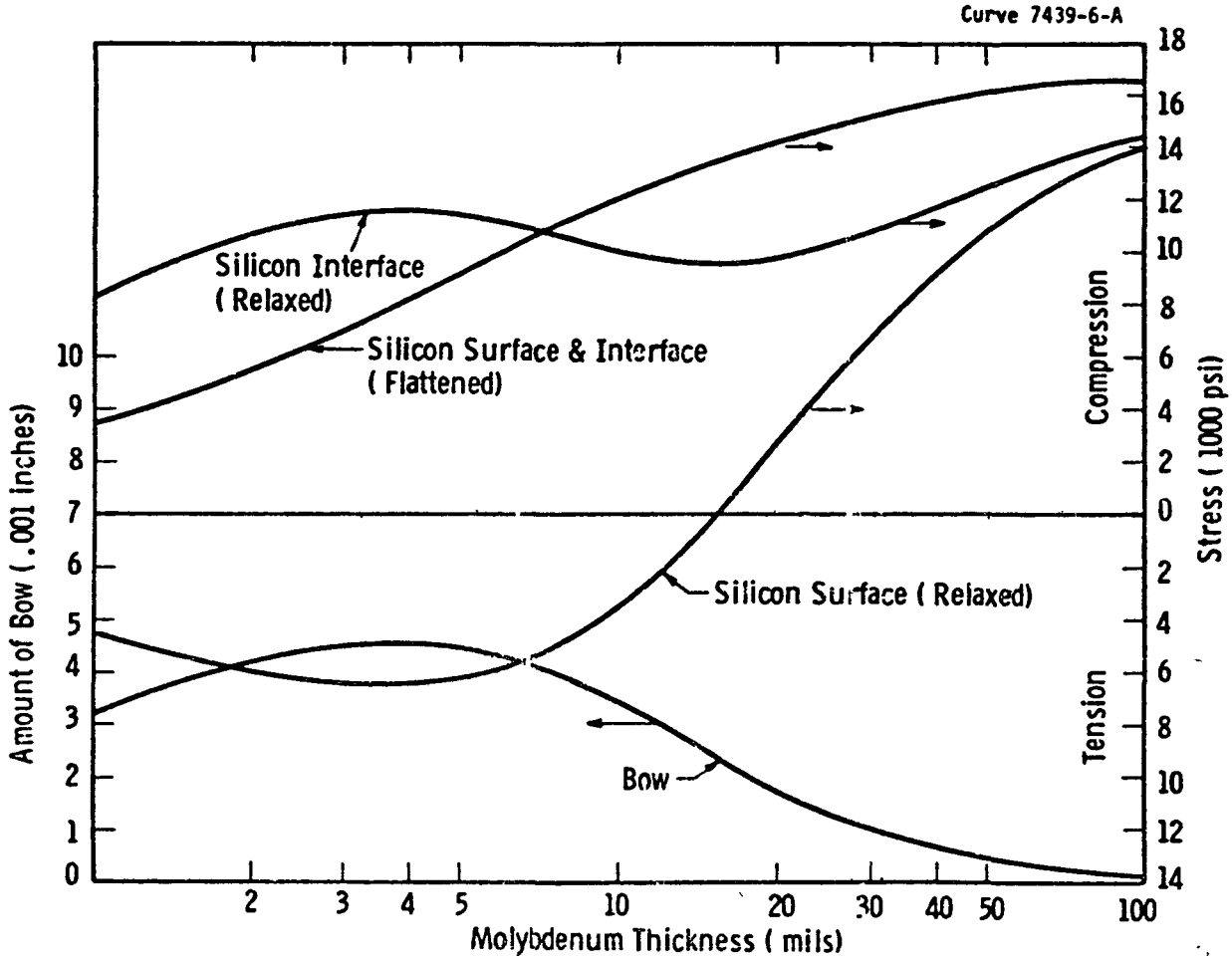


Figure 15. Amount of bow and stress versus molybdenum thickness.

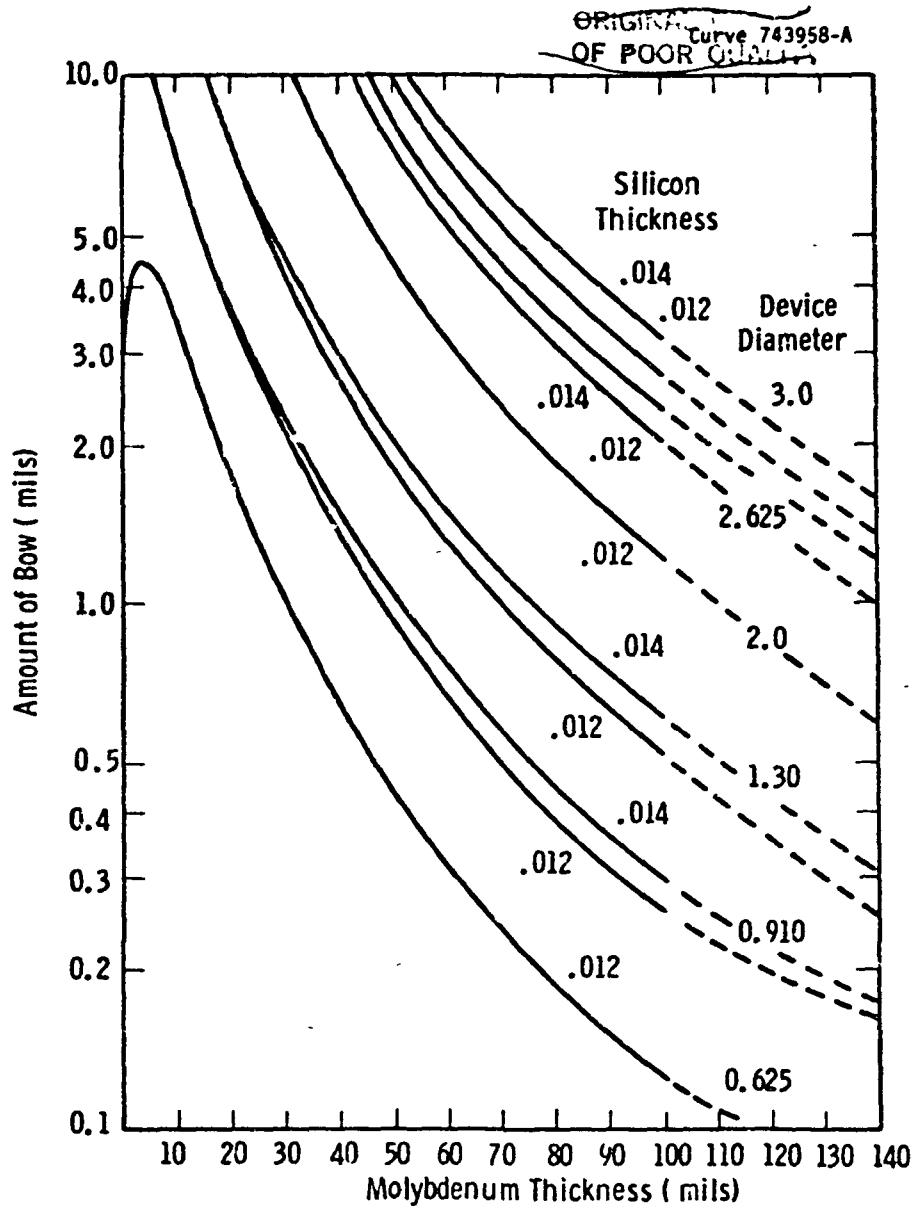


Figure 16. Effect of diameter and moly substrate thickness on device bow.

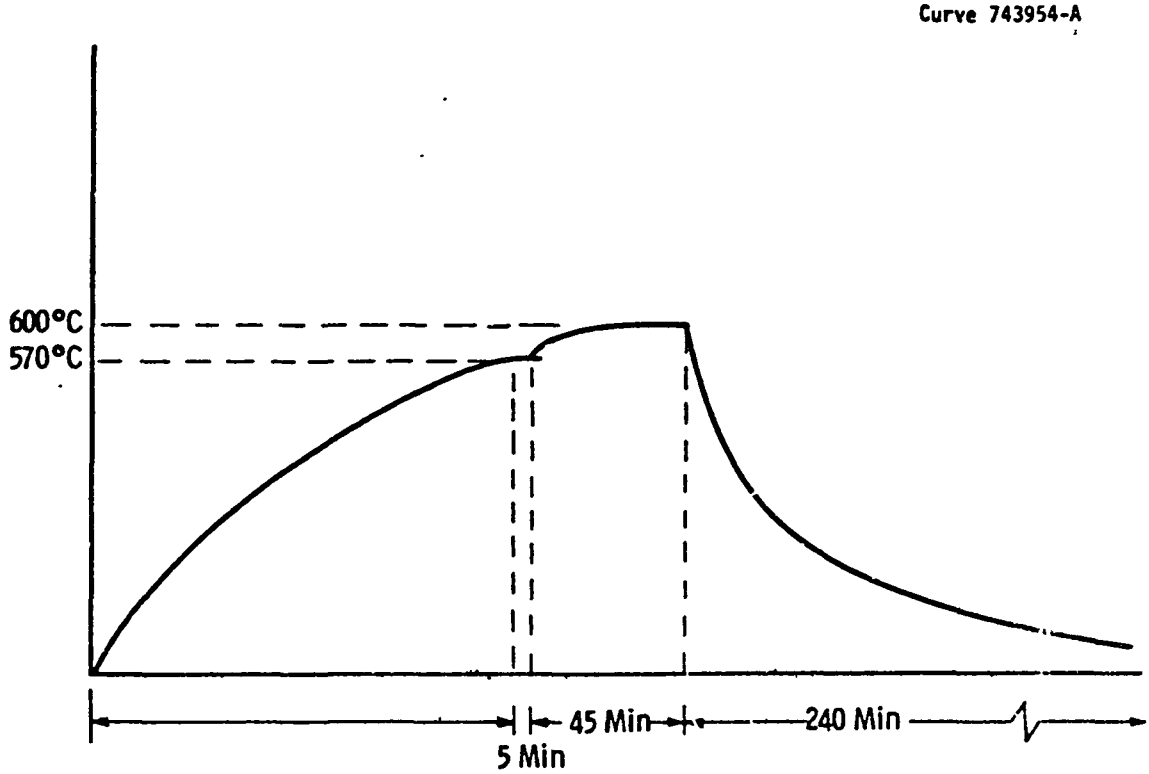


Figure 17. Alloy temperature and time cycle.

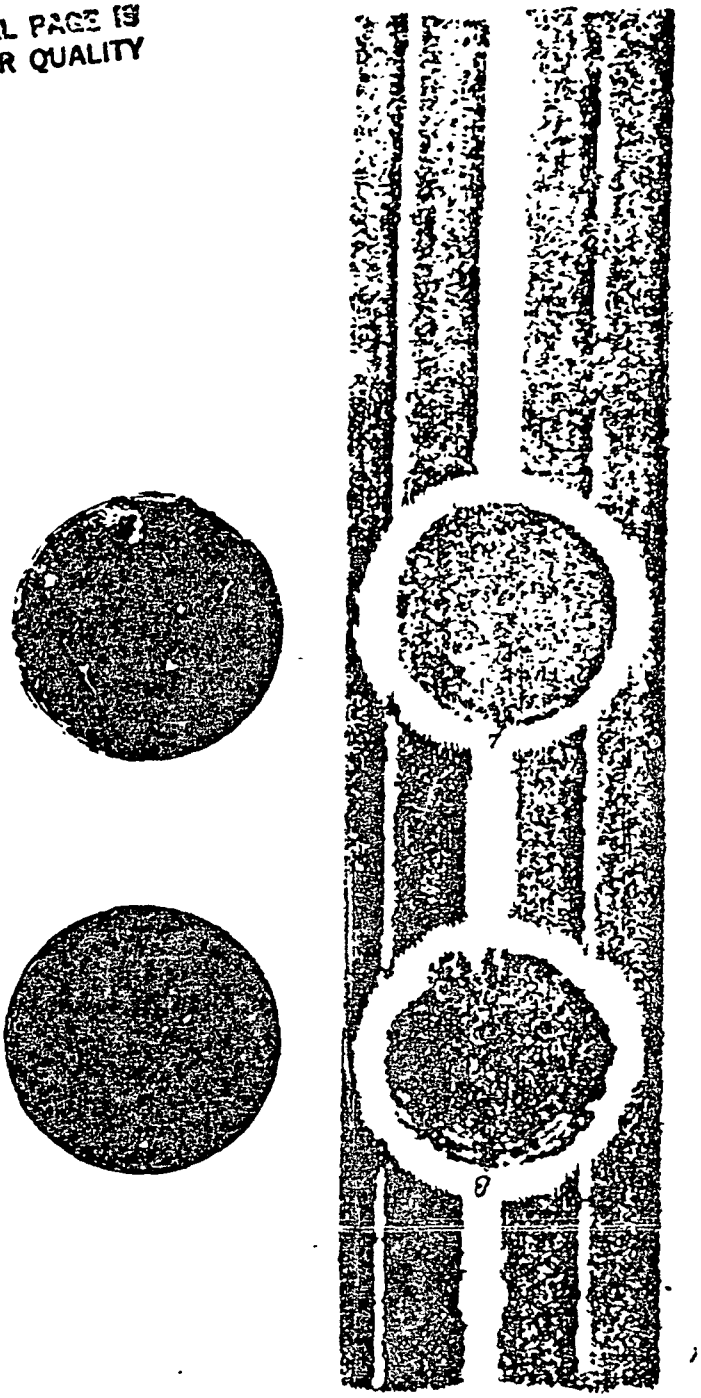


Figure 18. Ultrasonic scans and their corresponding bonds.

5. DEVICE FABRICATION

The 40 mm device fabrication process consists of a four-mask sequence with the process that essentially was developed under previous contracts such as NAS3-18916. Changes have been made in this process to accommodate the different glass passivation and alloy steps explained in the previous sections. A flow diagram indicating the various steps and appropriate cross sections is shown in Figure 19. The starting material in this case is an 85 ohm-cm n-type substrate 15 mils thick. The slices are as sawed and do not require any special surface finish. Into this slice is diffused a 3.0 mil deep phosphorus dopant which serves as the lower n^+ collector contact. After deep diffusion, one 3 mil region is removed by lapping and polishing to expose the n^- region for diffusion of an Al-Ga base diffusion. This is followed by a boron diffusion to increase the surface concentration and prevent conversion of the surface during the emitter diffusion. After the base diffusion, the slices undergo a photoresist step and phosphorus emitter diffusion deep enough to provide the desired h_{FEO} of 30.

After the diffusions are completed, the slices are edge beveled to a 6^o angle then spin etched and put through a screen-printing glass deposition step. Processing the slices further, the glass is fired after which an aluminum evaporation is performed on the back of the slice and one surface of the molybdenum disc. The slice and moly are next alloyed and another photoresist mask is used to open base and emitter contacts. An aluminum evaporation is again performed on the surface of the slice and another photoresist mask is applied to delineate the device contacts. Sintering of the contacts takes place at 550^oC, then a molybdenum preform is attached to the emitter contacts to complete the process. A picture of the completed fusion is shown in Figure 20.

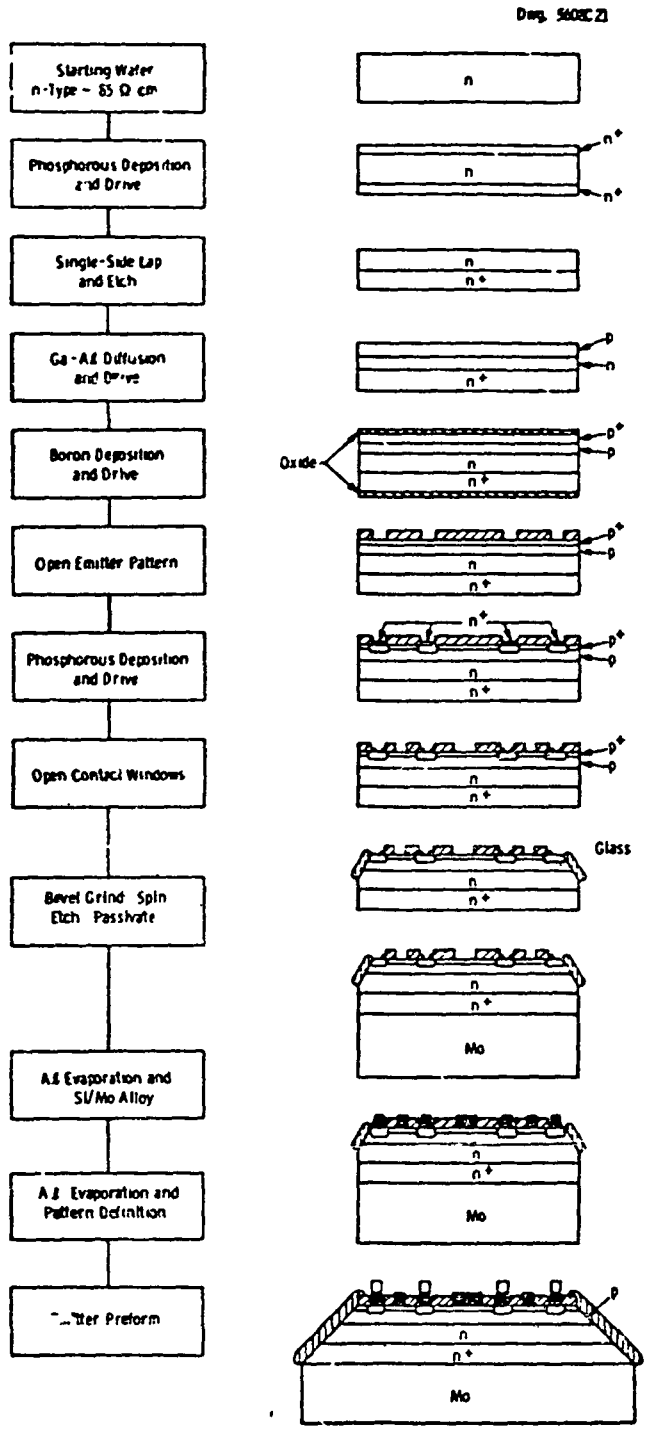


Figure 19. Process flow diagram.

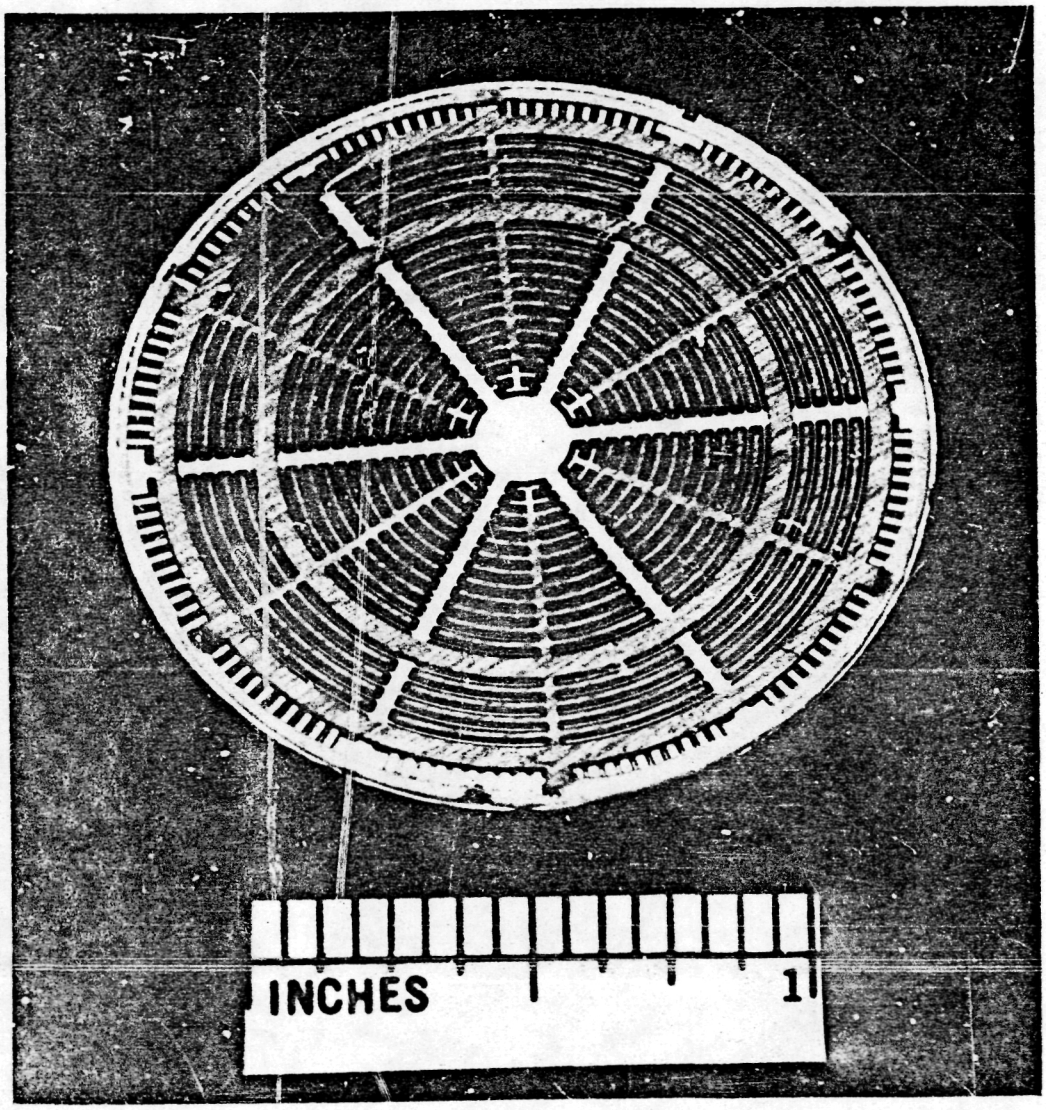


Figure 20. A 40 mm fusion.

6. PACKAGING

One of the main contract goals was that of packaging the device into an encapsulation that physically separates the transistor thermal and electrical interfaces. Originally the packaging task was contracted out to an outside vendor, Thermal Associates, Inc., to encapsulate the fusion into their size-18 isolated, modular, epoxy-bonded package. This vendor after a considerable length of time was not able to deliver a packaged device within the electrical specification; the contract agreement was therefore terminated.

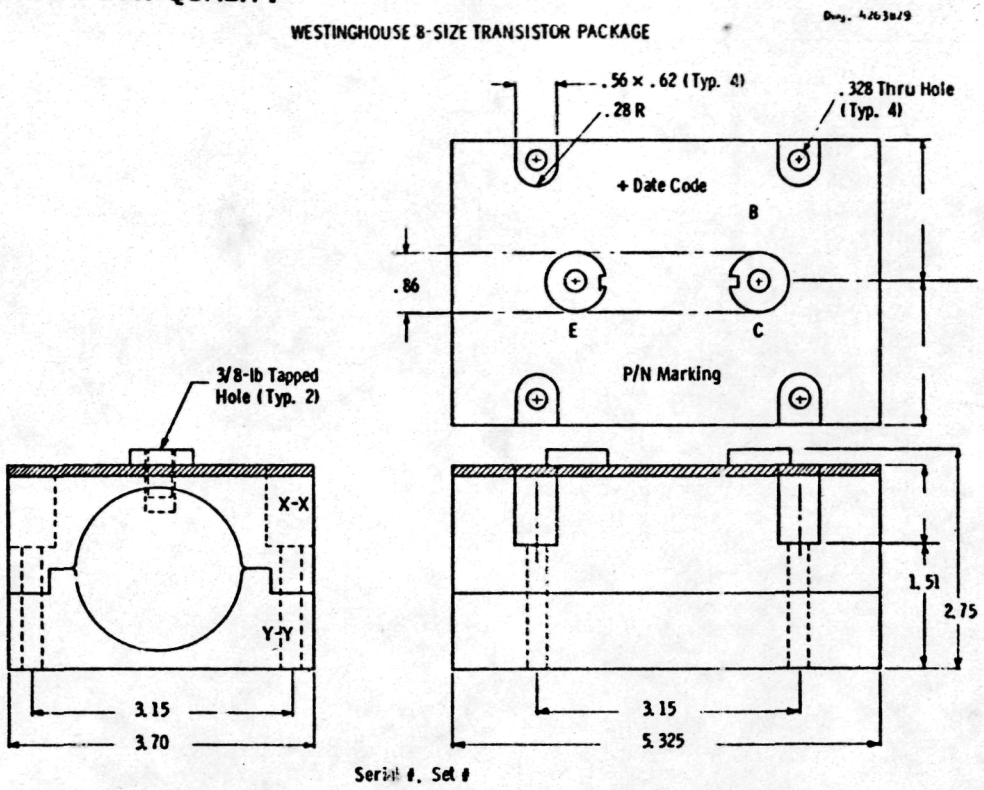
As an alternate approach, the following device delivery conditions were agreed to by NASA.

(a) Delivery of ten devices packaged into a modified Westinghouse T7S0 unit that will conform to the original packaging contract goals.

(b) Delivery of 30 fusions packaged in a Westinghouse 9-size flat package to pass all specifications other than the isolation requirement.

(c) Delivery of ten unpackaged devices to pass all specifications as measured in the fusion test package.

The modular power semiconductor described in (a) provides electrical isolation of the contained semiconductor while providing thermally conductive paths to the case. A sketch of the modified unit, which utilizes the "CBE" approach to mounting the fusion, double-side cooling, and an insulation system to provide up to 2500 VAC (min), Hi-pot case isolation is shown in Figure 21. A photograph of the package is also shown in Figure 21, and the specifications for this unit are shown in Table 3. For option (b) the cathode of the 9-size package was machined to fit the emitter preform of the 40 mm device and a teflon locator was added to center the device on the anode stage.



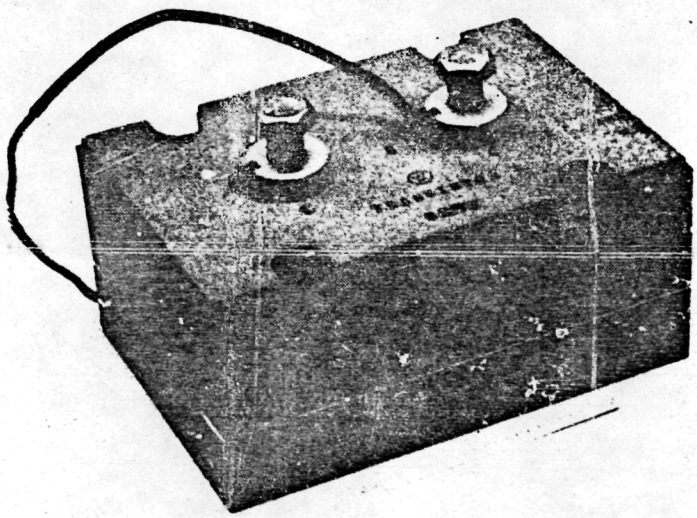


Figure 21. T7SO Semiconductor Package.

Table 3

T7S0 Device Specifications

1. Hi-pot (case isolation). . . . . 2500 VAC (min.)
2. CDIV (corona). . . . . 1000 V_{RMS} (min.)
3. $R_{\theta JC}$ (air-cooled design) . . . . . 1°C/watt (max.)
4. Size (air-cooled). . . . . 3.7" W x 2.75" H x 5.33" L
5. Other Features
   - Thermistor temperature monitor each device, isolated (2500 VAC) penetrations)
   - .50" dia. electrical connections (penetration)
   - Gate, gate potential leads (penetrations)
   - Internal hermetic devices
   - > 1" strike and creep between terminals
6. Air-cooled design to be capable of 250 through 550 ARMS, < 1600 volt device
7. Design must use UL materials

7. ELECTRICAL PERFORMANCE

7.1 Current-Gain Data

The electrical characteristics were measured for each device to reveal the h_{FE}, $V_{CEO}(sus)$, $V_{CE}(sat)$, and V_{CBO}. Switching measurements and FSOA were also made on typical devices and were found to be reasonably close from run to run.

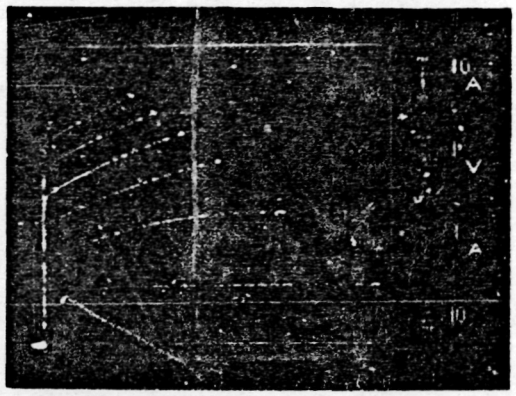
Figures 22 and 23 show three levels of current transistor characteristics for the 80 A and 50 A, respectively. The curves were obtained using a 576 Techtronix curve tracer and high-power pulse attachment. It can be seen that a gain of 14 is evident at both the 80 A and 50 A level. For both curves it can also be seen that the $V_{CE}(sat)$ is less than the 1 V design goal that is specified.

To show how these transistor parameters compare with the design goals, a curve of measured current gain versus collector current for both devices is shown in Figure 24, and for comparison the $G = h_{FE}\ I_O$ asymptote for each device is also shown. As can be seen, the measured curves are above the asymptote at the 50 A and 80 A current levels.

Figure 25 shows the distribution of $h_{FE}\ I_c$ versus $V_{CEO}(sus)$ for two runs each of different collector-base thickness. The curve shows the profound influence of the collector-base thickness on the high current gain and sustaining voltage. More importantly it is also evident that these values agree very closely with the predicted values from the computer readout of Figure 1.

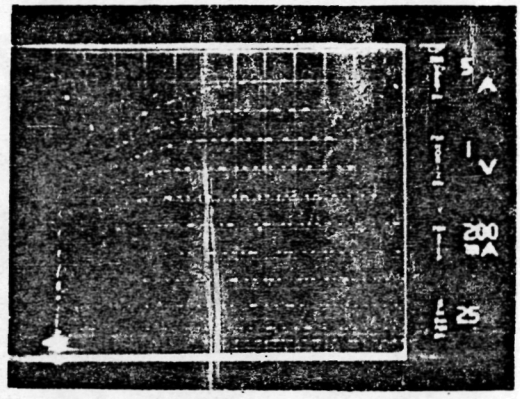
7.2 Switching Measurements

Switching measurements were made on these devices using a test circuit which simulates the waveforms seen in a typical switching

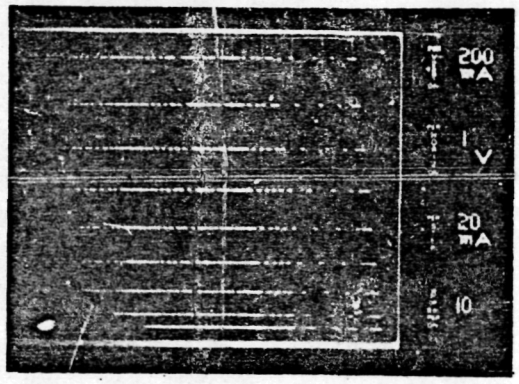


Device #
12D2-2

High Current

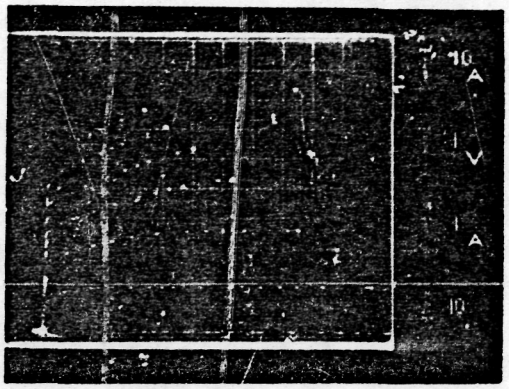


Medium Current



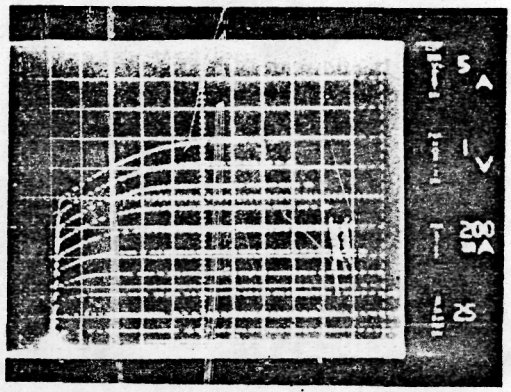
Low Current

Figure 22. Collector characteristics for the 800 V device.

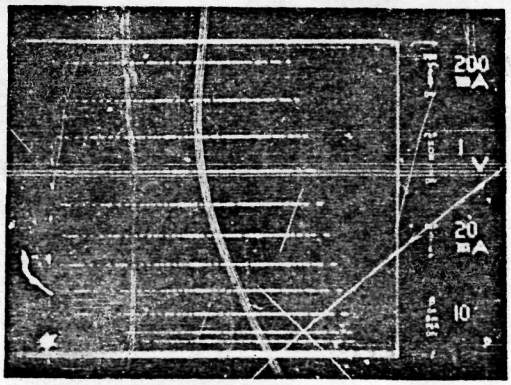


Device #
12D4-20

High Current



Medium Current



Low Current

Figure 23. Collector characteristics for the 1000 V device.

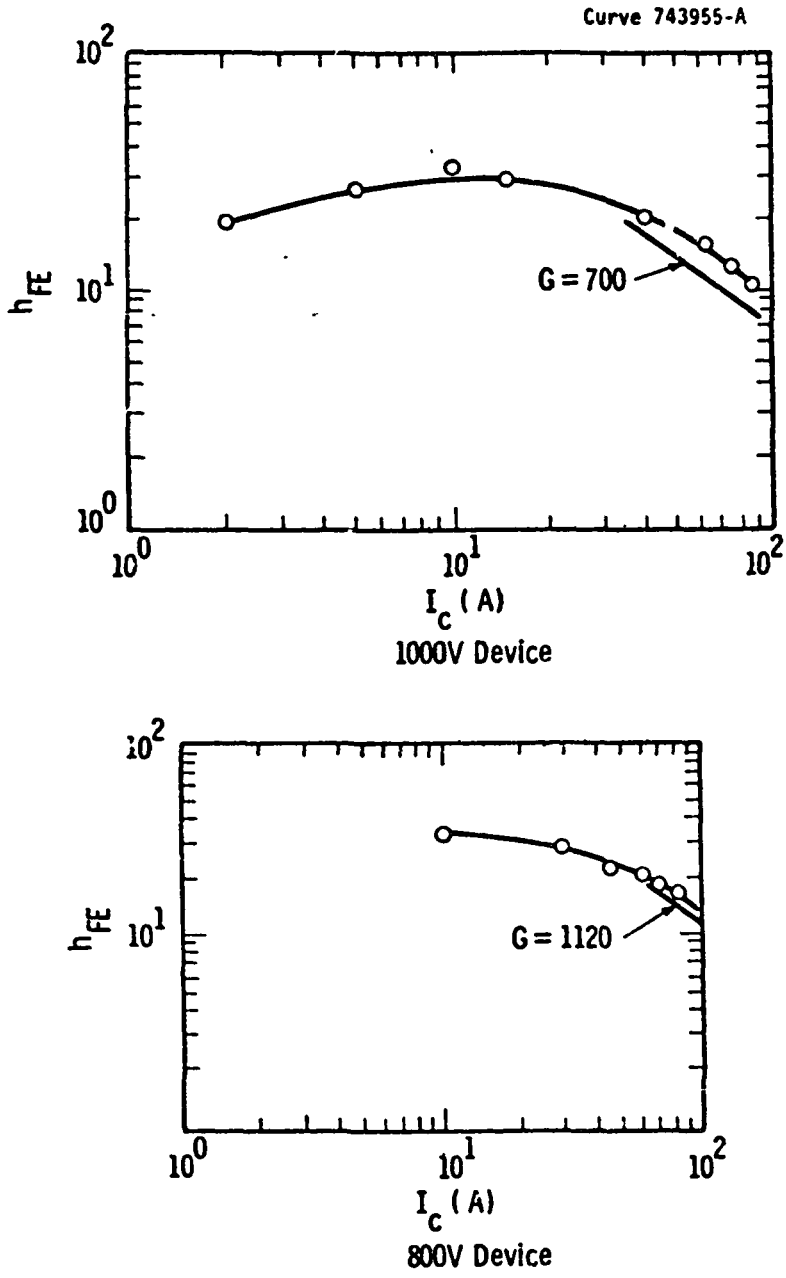


Figure 24. Current gain versus collector current for 1000 V and 800 V device.

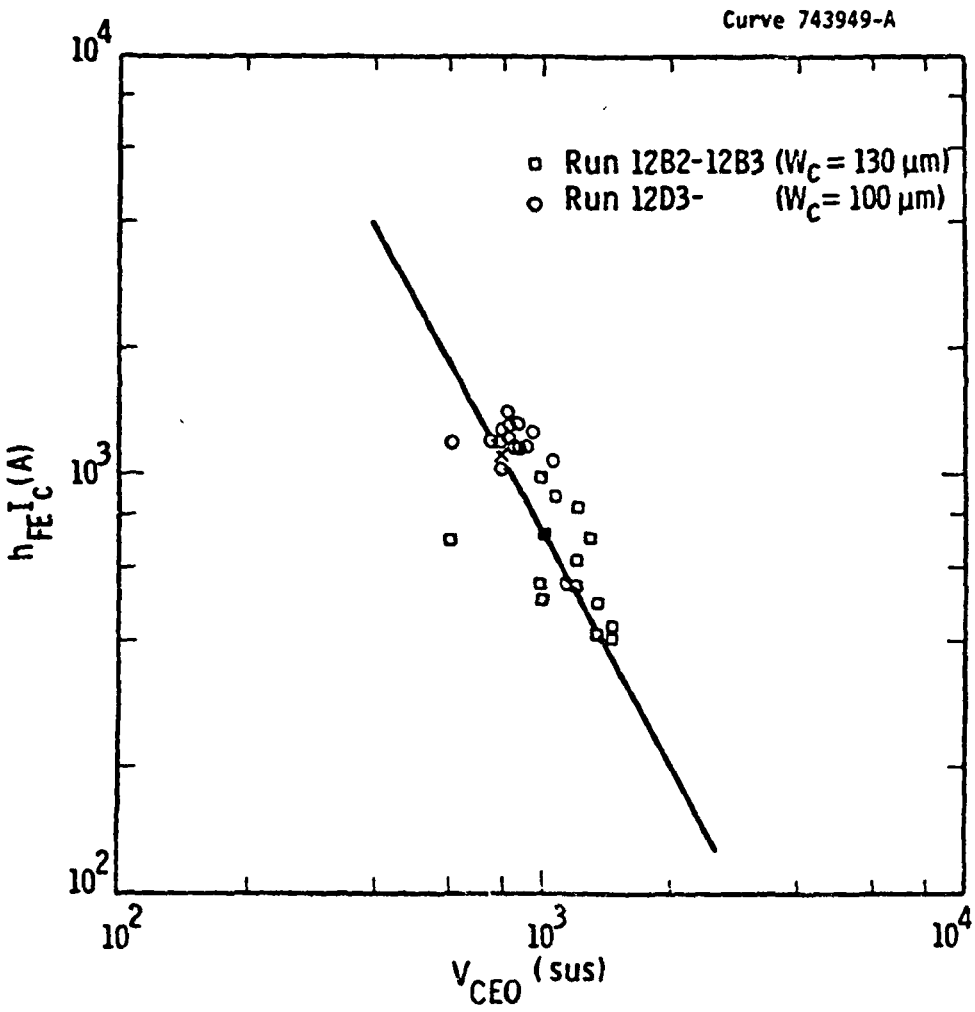


Figure 25. Measured and theoretical current gain product versus sustaining voltage.

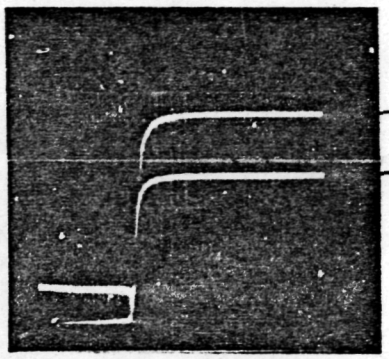
regulator circuit. The base-switching square wave pulses are at low duty cycle permitting steady-state conditions to be reached in the inductor during switching and keeping turn-on and turn-off losses and temperature fluctuations very low. Turn-on and turn-off switching waveforms are shown in Figure 26. Both curves show the 10% to 90% rise and fall times to be less than the contract goal of 0.5 μsec. Measurements were made at V_{CC} = 300 V, I_C = 50 A, and I_{BON} and I_{BOFF} = 5 A as specified by the test. Figure 27 shows the turn-on delay and storage time for the same device. The upper curve shows turn-on delay to be less than .1 μsec; however, storage time is approximately 5 μsec, which is somewhat higher than the design goal. High storage times can be attributed to the exceptionally high lifetime characteristic of the closed-tube, triple-diffusion process. The low-lifetime/low-storage time combination conflicts with the need for high-lifetime/high-emitter efficiency. A compromise must be made here since lifetimes greater than 50 μsec only serve to increase storage time with very little increase in emitter efficiency.

For a more realistic picture of device performance, switching energies were also measured. The switching energies are more descriptive of device performance because measurement does not need to take into account the shape of the collector current and voltage waveforms. Measurement is made by integrating the power curve. The power turn-off waveform shown in Figure 28 is a worst-case situation in which the peak power is in excess of 15 kW (50 A at 300 V). The energy dissipated here during turn-off is approximately 5 mJ, which permits switching frequencies to 50 KHz at 50 A collector current.

The turn-on and turn-off energies have been measured for values of peak collector current up to 80 A as shown in Figure 29.

It has been shown in previous work[3] that the safe operating frequency for a transistor can be defined by

$$SOF = \left[\frac{T_{JMAX} - T_A}{R_{\theta JC} + R_{\theta CA}} - P_{ON}\,\delta\right] / (E_{ON} + E_{OFF}) \qquad [7]$$



Device 12D-1-10

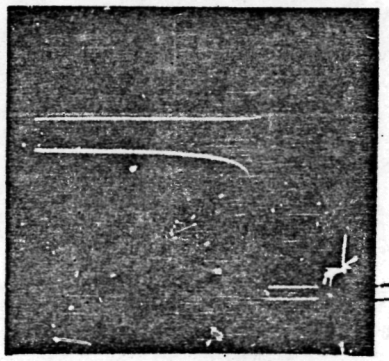
V_{CE} = 50 V/Div

I_C = 10 A/Div

t = 1 µs/Div

V_{CC} = 300 V

Turn-On Waveforms for Transistor 12D1-10



V_{CE} = 50 V/Div

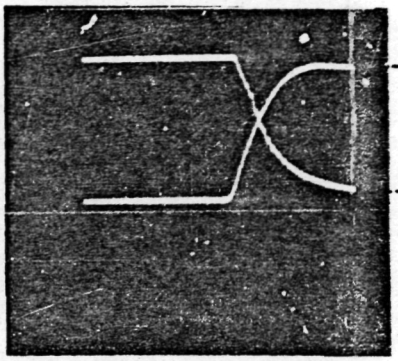
I_C = 10 A/Div

t = 1 µs/Div

V_{CC} = 300 V

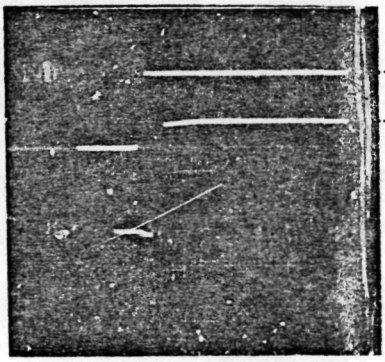
Turn-Off Waveforms for Transistor 12D1-10

Figure 26. Turn-on and turn-off waveforms.



I_C = 10 A/Div
$I_{B_{On}}$ = 1 A/Div
t = 0.2 µs/Div
V_{CC} = 300 V

Turn-On Delay Waveform for Transistor 12D1-10



I_C = 25 A/Div
$I_{B_{On}}$ = 1 A/Div
t = 2.5 µs
$I_{B_{On}}$ = 5 A
V_{CC} = 300 V

Turn-Off Waveform for Transistor 12D1-10 Showing Storage Time

Figure 27. Turn-on delay and storage time for typical transistor.

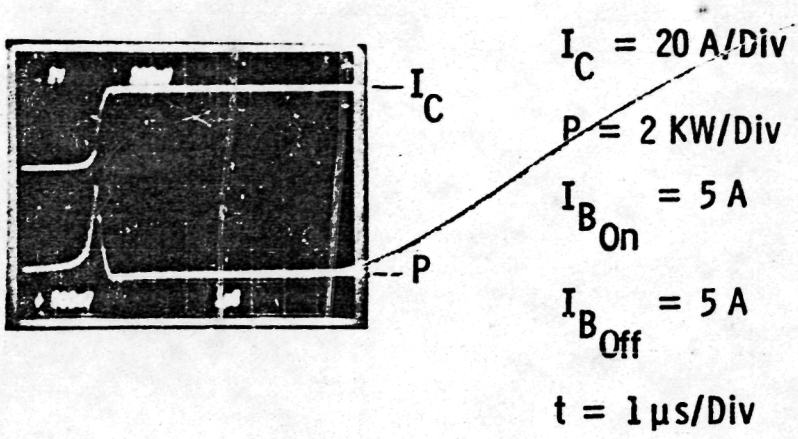


Figure 28. Power turn-off waveforms for typical transistor.

where

T_J = junction temperature
T_A = ambient temperature
$R_{\theta JC}$ = junction to case thermal resistance
$R_{\theta CA}$ = case to ambient
P_{ON} = conduction power
δ = .9

As an example we consider the case where I_C = 50 A, T_J max = 150°C, and V_{CE}(sat) = .5 at 150°C; then SOF = 50 KHz, which assumes a conduction power of 22 watts. For the 80 A device the SOF = 30 KHz because of increases in E_{OFF} and E_{ON} as well as conduction losses. It must be remembered that E_{ON} and E_{OFF} as well as the conduction losses are all subject to the I_{BON} and I_{BOFF} base currents.

7.3 Forward Safe-Operating Area Measurements

The device parameters which are important in determining the forward safe-operating area are the emitter and base resistance, the

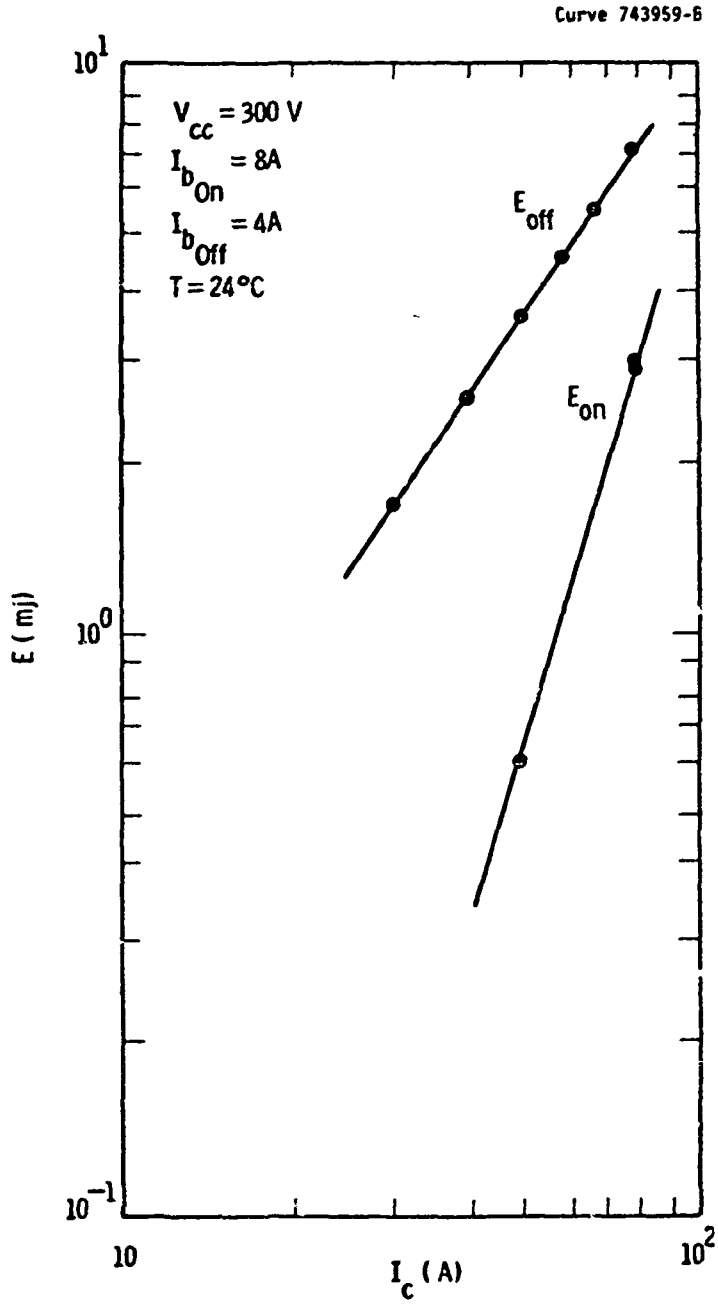


Figure 29. Turn-on and turn-off energies versus collector current.

magnitude and temperature dependence of h_{FE}, and the thermal resistance of the device and heat sink. The theoretical FSOA curves for the 8-size bipolar transistor are shown in Figure 30. These curves were calculated using measured transient thermal impedance data assuming that the device becomes unstable at a designated junction-to-case temperature. A two-dimensional model has been developed by Hower[4] which gives good agreement with measured results. Figure 30 shows the calculated forward SOA for a typical device as well as a measured point at low current. These curves were calculated for R_E = .55 mΩ and a $R_{\theta JC}$ = .023, both of which have been verified by measurement.

Curve 744254-A

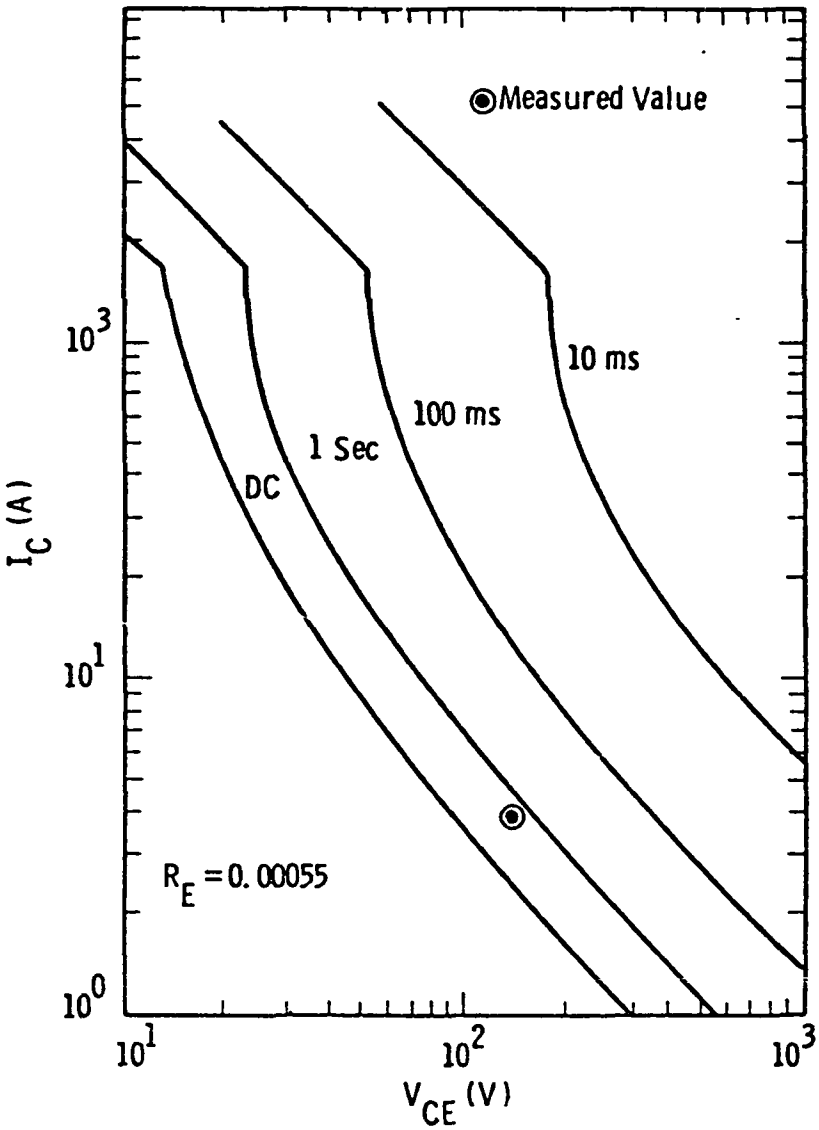


Figure 30. Forward SOA for different pulse times.

8. CONCLUSIONS

We have successfully fabricated bipolar transistors with $V_{CEO}(sus)$ in the range of 800 to 1000 V at current levels of 80 A and 50, respectively, at an h_{FE} of 14. A permanent-type passivation glass has been developed that will not only shield the device from ionic contaminants and moisture but will also aid in obtaining higher voltages and current by reducing the amount of area needed for junction contouring. In addition, a new low-temperature molybdenum to silicon alloy has been developed that will decrease wafer bow and thereby increase yield. A viable package has been used to provide heat transfer and the electrical isolation of the collector up to 2500 V RMS.

A total of 50 transistors have been supplied that meet the target goals and a complete listing of the measured test results is given in Appendix II.

9. REFERENCES

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2. V. A. Temple, "A Substrate Etch Geometry for Near Ideal Breakdown Voltage in p-n Junction Devices," IEEE Trans. on Elect. Dev. ED-24, 1977, pp. 1077-1081.

3. P. L. Hower, J. B. Brewster. and M. Morozowich, "A New Method of Characterizing the Switching Performance of Power Transistors," IEEE Ind. App. Soc. Conf. Record, 1978.

4. P. L. Hower and W. G. Enithoven, "Emitter Current Crowding in High-Voltage Transistors," IEEE Trans. on Elec. Dev., ED-25 April 1978, pp. 465-471.

APPENDIX I

Solution of the Navier Equation for Radius of Curvature

The radius of curvature R is given by:

$$R = \frac{1}{6\,a\,(t_s + t_m)} \left\{ a\,(t_s + t_m)^2 + \left(Z\,t_s - \frac{1}{Z}\,t_m\right)^2 \right\}$$

where:

t_s, t_m = thickness silicon, moly

a = (expansion coeff difference) × (temp. change)

$= (\alpha_{Mo} - \alpha_{Si}) \times \Delta T^{\circ}K$

$$Z = \sqrt{\frac{M_s t_s}{M_m t_m}}$$

$$M = \frac{2\mu E}{4\mu - E}$$

μ = Poisson's ratio for each material

$$E = \frac{\mu(3\lambda + 2\mu)}{\lambda + u}$$

λ = Rigidity modulus for each material

As a general rule, if $t_m > t_s$, the radius of bevel is given approximately by:

$$R = \frac{M_m + t_m^2}{6\,a\,M_s t_s}$$

APPENDIX II

Measured Test Results

Transistor No.	V_{CEO}(sus)	V_{CEO}(")	I_B(A) 50	I_B(A) 80	V_{CE}(sat)(V)	h_{FE}	
Nonpackaged 8-size							
12B2-6	1020	1400	3.0		.38	16.6	
12D3-1	1008	1480	3.8		.40	14.0	
12B3-2	1000	1000	3.8		.42	14.0	
12C1-7	1030	1450	3.2		.52	16.0	
12B3-6	1200	1320	3.0		.38	16.6	
12B2-2	1020	1100	3.2		.42	16.0	(Etch Groove)
12B1-8-2	1300	1450	3.5		.35	14.0	
12B1-8-3	1040	1400	3.5		.40	14.0	
12C-1-2	1200	1300	3.2		.35	15.6	
12D-1-4	850	950		5.1	.60	15.7	
12D-1-9	820	1200		4.8	.55	16.7	
12B2-3	200	200	3.2		.40	15.6	Dummy
12D1-6	200	200	2.8		.65	17.8	Dummy
Packaged 8-Size in T7S0 Package							
12C4-2	1020	1250	3.5		.40	14.2	
12B2-5	1000	1100	3.5		.42	14.2	
12C2-2	1000	1100	3.6		.50	14.0	
12C2-1	1100	1300	3.8		.52	14.0	
12C3-3	1100	1280	3.4		.42	14.7	
12D3-7	850	980		5.6	.42	14.2	
12D3-4	800	1000		5.8	.44	14.0	
12D3-6	880	990		5.3	.55	15.0	
12D3-2	850	900		5.8	.50	14.0	
12D3-8	823	1050		5.8	.38	14.0	
Packaged 8-Size in Flat-Pak							
12D1-11	860	1380		4.8	.70	16.6	
12D1-10	850	1300		4.8	.70	16.6	
12B3-1	1300	1180	3.5		.45	14.2	
12B3-2	1200	1300	3.0		.35	16.6	
12B3-4	1080	1580	2.8		.40	17.8	
12B3-5	1000	1620	3.5		.42	14.2	
12B3-3	900	1000		5.2	.20	15.3	
12D4-1	1000	1600	3.5		.40	14.2	

Transistor No.	V_{CEO}(sus)	V_{CEO}(V)	I_B(A) 50	80	V_{CE}(sat)(V)	h_{FE}
12D4-3	1050	1580	3.0		.25	16.6
12D4-4	1100	1450	3.8		.20	14.0
12D4-5	800	1200		5.2	.50	15.3
12D4-6	1100	1450	3.0		.22	16.6
12D4-7	1050	1400	3.0		.20	16.6
12D4-10	1005	1425	3.2		.20	15.0
12D4-11	1050	1480	3.1		.20	15.0
12D4-13	1080	1350	3.2		.28	15.0
12D4-14	1000	1220		5.6	.40	14.1
12D4-17	1080	1200	3.5		.20	14.2
12D4-18	1400	1630	3.0		.20	16.6
12D4-19	1010	1230	3.0		.20	16.6
12D4-20	1020	1238	3.0		.20	16.6
12D2-1	800	1380		5.0	.80	16.0
12D2-2	950	1500		5.0	.60	16.0
12D2-3	840	1650		5.1	.70	15.7
12D2-4	820	1480		4.6	.60	17.4
12D2-5	800	1450		5.1	.90	15.7
12D2-6	795	1200		5.2	.90	15.0
12D2-7	860	1500		5.8	.70	14
12D2-8	840	1500		5.8	.80	14
12D2-9	850	1600		5.8	.70	14

APPENDIX III

Target Characteristics for Augmented High-Voltage Power-Switching Transistors

Symbol	Characteristics with Test Conditions	Value	Units
$V_{CEO}(sus)$	Collector-Emitter Sustaining Voltage @ i_C = 2-0 mA, I_B = 0, 300-μs pulse	800 min 1000 max	Volts
V_{CBO}	Collector-Base Voltage at I_C = 200 mA	$>V_{CEO}(sus)$	Volts
$h_{FE}I_C$	Max Gain - Collector Current Product @ V_{CE} = 2.5 V		
	• $V_{CEO}(sus)$ = 800 V	1120	Amperes
	• $V_{CEO}(sus)$ = 1000 V	700	Amperes
I_B	Max Base Current		
	• Pulsed (<2% Duty Cycle)	100	Amperes
	• Continuous DC	60	Amperes
I_C (peak)	Max Collector Current, pulsed @ V_{CE} = 2.5 V		
	• $V_{CEO}(sus)$ = 800 V	500	Amperes
	• $V_{CEO}(sus)$ = 1000 V	300	Amperes
I_C (continuous)	Max Collector Current, continuous @ V_{CE} = 2.5 V		
	• $V_{CEO}(sus)$ = 800 V	225	Amperes
	• $V_{CEO}(sus)$ = 1000 V	140	Amperes
h_{FE}	DC Current gain for $V_{CEO}(sus)$ = 800 V		
	• I_C = 80 A @ V_{CE} = 2.5 V	14	
h_{FE}	DC current gain for $V_{CEO}(sus)$ = 1000 V		
	• I_C = 50 A @ V_{CE} = 2.5 V	14	

Symbol	Characteristics with Test Conditions	Value	Units
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage @		
	• I_C = 80 A, I_B = 8 A, $V_{CEO}(sus)$ = 800 V	1.0	Volt
	• I_C = 50 A, I_B = 5 A, $V_{CEO}(sus)$ = 1000 V	1.0	Volt
$V_{BE}(sat)$	Base-Emitter Saturation Voltage @ same parameters as for V_{CE}, above	1.2	Volt
$R_{\theta JC}$	Thermal Resistance Junction to Case	<0.1	°C/Watt
P_T	Power Dissipation at Case Temperature, T_c = 75°C	1250	Watts
T_J	Operating and Storage Junction Temperature Range	-50 to 200	°C
t_D*	Turn-On Delay	0.1	μsec
t_r*	Rise Time (10 to 90% I_C)	0.5	μsec
t_s*	Storage Time	2.5	μsec
t_f*	Fall Time (90 to 10% I_C)	0.5	μsec
	Operating Environment	Typical Space Vacuum and Zero "8"	
	Non-operating Survivability	Typical Spacecraft Launch Shock and Vibration	

*All switching times measured with resistive load, supply voltage, V_{CC} = 300 V, I_C = 50 A, I_{B1} = I_{B2} = 5 A using 100-μs pulses with duty cycle <2%.

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