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MICROWAVE MONOLITHIC INTEGRATED CIRCUIT DEVELOPMENT FOR FUTURE SPACEBORNE PHASED ARRAY ANTENNAS

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Abstract

The development of fully monolithic gallium arsenide (GaAs) receive and transmit modules suitable for phased array antenna applications in the 30/20 gigahertz bands is presented. Specifications and various design approaches to achieve the design goals are described. Initial design and performance of submodules and associated active and passive components are presented. A tradeoff study summary is presented highlighting the advantages of distributed amplifier approach compared to the conventional single power source designs.

Introduction

Studies have identified the use of multiple scanning beam antenna systems as a major factor in achieving minimum cost and efficient use of the frequency and orbital resources for the future generation of the communications satellite systems. The Advanced Communications Technology Satellite (ACTS), scheduled for launch in the late 1980's will employ the scanning beam antenna technology in the 20/30 gigahertz bands to maximize the operating efficiency. Future communications satellite systems may use monolithic receive and transmit module technology which is expected to further increase the system operating efficiency. In support of the development of advanced antenna concepts, a key area therefore, is the development of compatible monolithic receive and transmit modules at the above stated frequencies.

Gallium arsenide (GaAs) monlithic microwave integrated circuits (MMIC) offer substantial performance advantages in the proposed frequencies of interest. Since entire microwave circuits can be fabricated on a single chip, utilizing deposition, epitaxy and ion implantation techniques, the resulting circuit is free of parasitics, losses and component value uncertainties normally associated with wire bonds and other external interconnects. Monolithic circuits can therefore be designed, developed and produced for optimum performance with no circuit adjustments after assembly.

In addition to monolithic circuit performance advantages mentioned, additional, very attractive advantages are offered by microwave monolithic integrated circuits in areas of cost, weight per function and reliability. As technology matures and substantial volumes of production are achieved, all advantages will be more fully realized.

NASA Lewis Research Center is pursuing the following MMIC developments which promise maximum impact for the future communications systems in the 30/20 GHz frequency range.

30 GHz Monolithic Receive Module

Two parallel efforts to develop a 30 GHz monolithic receive module are in progress at Hughes-Torrance Research Center (HAC-TRC) and Honeywell Corporate Technology Center (H-CTC). The receive module's performance goals are listed in Table 1. The module's final configuration, consisting of four functional submodules integrated on a single chip is shown in Fig. 1. Basic technologies employed in the fabrication include sub-micron gate length field effect transistor (FET) fabrication using refractory metalization systems, ion implantation for low noise amplification and microstrip circuitry fabricated on semi-insulating gallium arsenide (GaAs) substrate.

Since the receive module's intended application is for steerable phased array antennas where a large number of receive - transmit elements is employed, a possible element might be a waveguide radiator. Figures 2 and 3 show a proposed module layout and its possible incorporation in a waveguide radiator (fixture) employing suitable waveguide to microstrip transitions[1] with control and power connections.

Low Noise Amplifier Submodule (LNA)

The design and fabrication approaches chosen by both contractors in the development of the low noise amplifier modules are similar. Sub half-micron gate length FET's have been designed and are in process of fabrication for use in the low noise amplifiers. Both conventional photolithography supplemented by the E-beam lithography are used for circuit and active component fabrication. Since LNA submodules are still in the final design and early fabrication stages, only preliminary test results are available. Figure 4 shows the Hughes LNA design, its calculated characteristics and component layout. Significantly better results are expected in the FET gain and noise performance areas in the future. Typical low noise FET performance in the band of interest is expected to improve by approximately 1 dB during the duration of this development effort. Consequently, the module noise figure goal of 5 dB or less is expected to be achieved without difficulty. Figure 5 shows the initial amplifier design employed by Honeywell. A single gate FET version of the amplifier is expected to be used in the LNA. Noise performance is similar to the Hughes version described above.

Phase Shifter Submodule

Possibly the most challenging part of the proposed effort to develop a monolithic receive module is the development of the phase shifter submodule. The performance goals of the submodule require its operation at five different phase states between zero and 180 degrees controlled by a digital input signal. The phase shifter is to use a true time delay phase shift scheme, where in any state of the phase shifter the total module phase shift is proportional to frequency within the 27.5 to 30 gigahertz passband.

A large variety of monolithic phase shifters has been developed for various applications. Most of these phase shifters were designed and built at X-band frequencies or lower where area per phase shift bit requirements were relatively large. At 30 gigahertz, the area requirements will be reduced by about a factor of four, making the approach more practical, although more challenging problems are expected in the areas of insertion loss, phase error and circuit yield.

Both contractors are investigating the designs of digital phase shifters based on switched transmission line configuration using large periphery unbiased FET's as RF switches. Phase shifting is accomplished by true time delay between the differential electrical length of microstrip lines in the circuit. Two of the most common rf switch circuits in use employ FET's either in shunt or series-mounted configuration. Figure 6 shows a single bit phase shifter in a shunt mounted FET switch configuration. Honeywell's initial approach was to build a single bit (180°) switched line phase shifter employing 300 micron gate periphery power FET's as switches in a shunt mounted configuration. The FET dc on resistance exhibited was 11 to 14 ohms.[2] The insertion loss per bit was approximately 4 dB over the 27.5 to 30 gigahertz band.

A subsequent improvement in dc on resistance by a factor of 1.5 to 2 has been achieved by fabricating the switch FET's by the use of the self-aligned gate (SAG) technology.[3] Generally, the SAG phase shifters to date have achieved about 2.5 dB/bit insertion loss over the band mentioned above. It is expected that future 30 gigahertz phase shifters could be fabricated with an insertion loss of 1.5/dB bit. A comparison of measured and calculated insertion loss for a SAG phase shifter is shown in Fig. 7. Honeywell's design for an improved phase shifter employing four series FET switches fabricated by SAG technique is shown in Fig. 8. The design features a more compact layout with no rf grounding requirements which promises lower insertion loss and better phase performance.

Hughes' initial approach was to investigate an analog phase shifter as shown in Fig. 9. The phase shifter is based on a branch line coupler approach which is very simple and occupies a relatively small area. Although not a true time delay phase shifter, it's simplicity and projected high circuit yield makes it a good candidate for further investigation. A 30 gigahertz Lange coupler has been fabricated and the investigation of its characteristics continues. Identical Shottky-barrier diodes are connected in series with the inductors to ground. By proper biasing of the diodes their capacitance can be varied which subsequently changes the phase of the transmitted signal. Loaded line circuit designs are being considered for the two minor bits of 11.25 and 22.5 degrees. While they do not provide true time delay, these designs are considerably smaller and are projected to introduce negligible phase errors.

Gain Control Submodule

As shown in Table 1, the receive module RF/IF gain performance goal stipulates that maximum gain be equal or greater than 30 dB with six intermediate steps as shown. The intermediate gain steps are commanded using a digital signal. Two different approaches in controlling the receive module gain are presented in Fig. 1. Honeywell's proposed approach is to control the gain at rf while the Hughes' proposed approach is to vary the module gain at IF. Both approaches utilize dual gate FET's where variation of second gate bias controls the gain of the amplifier. Figures 10 and 11 show the proposed circuit and submodule layout designs. Both designs are preliminary and changes are expected before final designs are approved.

Since both submodules depend on gain variation due to FET bias voltage changes a digital to analog converter will be required for each approach. Designs and proven fabrication techniques exist for digital to analog converters and no difficulties are expected in this area. It is expected that the submodule sizes for both approaches, including the D/A converter circuitry, will be approximately 1 mm x 2 mm.

RF-IF Submodule

The RF-IF submodule's two main functions are to convert the 27.5 to 30 gigahertz input rf signal to the specified IF frequency in a mixer and to amplify the external reference signal which serves as a local escillator input to the mixer. Both contractors chose to amplify the given 15 microwatt reference signal to serve as the local oscillator. A multistage, low noise, high gain monolithic amplifier will be developed for this purpose.

Although no final design choices have been made, Hughes' choice for the mixer design was a dual gate FET while Honeywell's baseline approach was a balanced Shottky diode mixer with a rat race hybrid. The IF amplifier, required in Honeywell's approach (see Fig. 1) is expected to be a simple, low gain, low noise figure monolithic type, operating in the suggested IF frequency band between 4 and 8 gigahertz. No experimental results are available for this submodule at present.

20 GHz Transmit Module

A monolithic transmit module is under development at Rockwell International, Thousand Oaks, California. The technology goals for the 30-month contract are given in Table 2. The MMIC module uses a microstrip approach in which all active and passive devices are fabricated on a GaAs substrate. Figure 12, shows a block diagram for an initial layout of the fully monolithic transmit module chip. The module consists of five cascaded single bit phase shifters each employing a switched line approach using FET devices for switches. The digital control circuitry portion accepts a TTL input signal and provides the signals to switch in or out each of the five phase shifters. A two-stage buffer amplifier follows the phase shifters to compensate for the phase shifter losses. Finally, a three-stage power amplifier completes the module. The chip size is 4.8 mm by 6.4 mm, however this initial design layout includes diagnostic test circuitry and the final layout could produce a smaller chip size. It was determined that a staged development for the fully monolithic transmit module was the most feasible approach to follow. This consisted of a design for the fully monolithic module and then a division of the total circuit into submodule designs which were of a suitable scale for fabrication, characterization and evaluation.

The first phase of the work consisted of developing submodules demonstrating the phase shifter, digital control and power amplifier functions. The initial mask set consisted of the following nine submodule chips: digital control circuitry; one-stage buffer amplifier and discrete FET, two-stage buffer amplifier; wafer test circuitry; and five phase shifter submodules of 11.25°, 22.5°, 45°, 90°, and 180° bits. Total reticle size is is 4.8 mm x 4.8 mm and contains the nine 1.5 mm x 1.5 mm size chips and separation channels. A photo of a typical chip (two-stage buffer amplifier submodule) is shown in Fig. 13. A second mask set consisted of submodule chips of the full three-stage power amplifier and various one and two stage combinations of this full three-stage amplifier.

The design approach for these submodule developments was accomplished by the extensive use of computer aided design (CAD). The CAD included equivalent circuits for the FET's, accurate modeling of passive elements and careful characterization of parasitics and inter-element coupling. The objectives of the design were minimal chip size with high yield processing and low potential cost to provide reliable modules meeting the goals of Table 2.

With approximately two-thirds of the program completed, submodules have been fabricated and tested demonstrating all of the necessary circuit functions, however design refinements are still required. More detailed information on the design, fabrication and test of the two-stage buffer amplifier and three-stage power amplifier submodule developments have been reported by Petersen and Gupta[4,5] of Rockwell. The 20 GHz two-stage buffer amplifier development is probably the most advanced as seen in Fig. 14 which shows the predicted and measured gain results. The three-stage power amplifier submodule operated but at a reduced gain level. A saturated output power of approximately +21 dBm was measured across the 2.5 GHz band, with the goal being +23 dBm. The phase shifter submodules also operated but with an approximate 3.5 dB insertion loss (goal of 2.5 dB) per phase shifter bit.

Although the submodules still require further development, sufficient information has been obtained and design iterations developed that the mask set for the fully monolithic transmit module has been designed and fabricated. The remaining time of this contractual effort will continue with the fabrication, test and evaluation of the fully monolithic transmit module.

20 GHz Variable Power Amplifier (VPA) Module

Texas Instruments is presently developing a 20 GHz monolithic variable power amplifier module. The performance goals of this monolithic amplifier module are shown in Table 3. The objective is to develop a 17.7 to 20.2 GHz monolithic GaAs variable power amplifier exhibiting high efficiency at various output power levels. The amplitude control provides for five output power states at nominal levels 500, 125, 50, and 12.5 mW and zero. The amplitude control is to operate on a digital basis and be TTL compatible.

Development Approach

This development program uses a four-stage dual-gate FET amplifier design approach. A block diagram of the VPA module is shown in Fig. 15. The second gates of all the FET's are connected with interstage matching networks as shown. Digital control inputs for gain control are converted to analog voltage using a digital to analog (D/A) converter. The nominal gains as a function of the control voltage V_{g2} are also shown.

The VPA module is divided into two submodules, the amplifier module and the amplitude control module. The two modules will be monolithically integrated later onto a single 4.5 mm x 1.5 mm GaAs chip. Dual-gate power FET devices suitable for 20 GHz operation were first developed. These devices are to be incorporated into the four-stage amplifier module. Concurrently, a four-stage single-gate FET monolithic amplifier module for 20 GHz operation and the D/A converter module for amplitude control were also developed.

Four-Stage, Single-Gate Amplifier

For the four-stage, single-gate amplifier, GaAs FET's with gate widths of 300 um were used in the first and second stages while FET's with gate widths of 600 um and 1500 um were used in the third and fourth stage, respectively. FET equivalent circuit models were used for the amplifier design. High impedance transmission lines with a characteristic impedance of 70 ohms were used for impedance matching. The required capacitors were implemented with the metal-insulator-metal (MIM) silicon nitride overlay types. The chip size is 4.4 mm x 1.4 mm.

At midpoint of the program, the four-stage, single-gate amplifier showed good gain control with either changing gate bias or changing drain bias. The amplifier has a gain of at least 18 dB across the 18 to 20 GHz frequency band. It was anticipated that with a minor design iteration (increased interstage drain matching inductances), an output power of at least 500 mW with 20 dB gain can be achieved.

Dual-Gate FET

Dual-gate FET models with cascade connected common-sources, common-gate stages were obtained by comparing measured devices S parameters with models generated from SUPER-COMPACT. The element values of the models were obtained by optimization.

Hybrid single-stage dual-gate FET amplifiers with gate width up to 1200 um have achieved gains in excess of 10 dB over the 18 to 20 GHz band with a range of gain control greater than 30 dB.

Using the measured S parameters, complete dual-gate equivalent circuit models have been obtained for amplifier design. A four-stage, dual-gate amplifier based on complete device models for the different stages has been designed. A gain in excess of 25 dB was predicted. Figure 16 shows the computed gain-frequency response and input/output VSWR performance.

Amplitude Control Module

A TTL compatible four-bit integrated D/A converter was developed during the the first year of the program. Figure 17 shows the circuit of this converter, which is designed to control the gain of dual-gate FET's. Details on the operation of this D/A converter have been reported in the Electronic Letters[6].

Multiple Beam Antennas - Conventional vs Distributed Amplifier Approach

In order to gain a more in-depth understanding of the use of the distributed amplifiers in a spaceborne communications system, a tradeoff study was conducted by NASA Lewis where a conventional amplifier (TWT) was compared to a distributed amplifier (MMIC) approach. An operational communications satellite concept,[7] proposed for the Advanced Communications Technology Satellite (ACTS), employing conventional amplifiers feeding a six scanning beam antenna system was compared to the same system employing distributed amplifiers. The system antenna and radiofrequency power requirements for each beam are shown in Table 4. The proposed east/west CONUS coverage scenario utilizing six sectors employing scanning beams is shown in Fig. 18. Fixed beams shown were not included as part of this exercise. Figure 19 shows the DC power requirement per sector beam for a conventional amplifier (TWT) utilizing conventional variable power dividers to achieve the required beam scan. This system, referred to as "System A" uses 1982 technology and is the reference system for our comparison. Figures 20 and 21 show the resulting DC power budgets for sector beams utilizing distributed amplifier approaches (MMIC) and 1987 technology. As shown, the total efficiency per scan beam is higher for the cases where a distributed amplifier approach is used. "System B" is utilizing two spacecraft antennas with separate receive/transmit feeds. "System C", also using a distributed amplifier approach, employs a single reflector antenna concept with separate receive/transmit feeds. By incorporating the "System C" separate receive/transmit feed assembly into a single receive/transmit feed utilizing common receive/transmit horns with orthomode transducers a further reduction of weight and cost is possible. This approach is presented as "System D". The three distributed amplifier approaches, compared to a specific conventional amplifier approach, show that significant improvement can be gained in efficiency, weight and cost by the use of properly designed systems employing MMIC modules. Tables 5 and 6 show the summary of the tradeoff exercise for the four systems described. The implementation of the distributed amplifier approach in a specific scan beam system resulted in a 25 percent decrease of total DC power, a 60 percent decrease in system weight (antenna, feed, amplifiers and heat rejection) and a 5 percent increase in the efficiency of the final RF amplifier for the scan feed array. Initial estimates also indicate that the cost required for the distributed amplifier receive/transmit arrays for scan beams will be less than half of that required for conventional amplifiers.

Conclusion

An overview of the microwave monolithic integrated circuit receive and transmit module development has been presented. NASA Lewis is pursuing those MMIC developments in the 30/20 gigahertz frequency range that promise maximum system impact. Studies have identified the use of multiple scanning beam antennas as a major factor in achieving minimum cost and efficient use of frequency and orbital resources for future generation of communication satellites. Initial designs for the 20 gigahertz transmit and 30 gigahertz receive MMIC modules indicate that the proposed approach is sound and has the potential for considerable improvement over the conventional (TWT) approach. The results of NASA tradeoff study indicate that the distributed amplifier approach offers significant improvement in areas of DC power, system weight and system cost.

References

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5. Petersen, W. C., and Gupta, A. K., "A Three-Stage Power Amplifier for a 20 GHz Monolithic Transmit Module," to be published in the GaAs IC Symposium to be held in Phoenix, Arizona, on Oct. 25-27, 1983.

6. Saunier, P., Kim, B., and Frensley, W. R., "GaAs Integrated Digital-to-Analogue Convertor for Control of Power Dual-Gate FET's," Electronic Letters, Vol. 19, No. 5, March 3, 1983, pp. 162-163.

7. "30/20 GHz Spacecraft Multiple Beam Antenna System; Task 1 Report: Development of Operational System Concepts," TRW Systems Group, Document No. A005, Feb. 1981.

TABLE 1. - RECEIVE MODULE PERFORMANCE GOALS

Design parameter	Performance goal
RF band	27.5 to 30 GHz
IF center frequency	Between 4 to 8 GHz
Noise figure at room temperature	≤5 dB
RF/IF gain	≥30 dB at highest level of gain control
Gain control	At least six levels; 30, 27, 24, 20, 17 dB and Off
Phase control	5 bits; each bit ±3° band center
Module power consumption	250 mW in all states except OFF. In OFF state, 25 mW.
Phase and gain control	Operate on digital input.
Mechanical design	Fully monolithic construction; compatible with 30 GHz spaceborne phased array applications.
Unit cost	Less than $1000 (1980 dollars) in unit buys of 5000 or more

TABLE 2. - TRANSMIT MODULE PERFORMANCE GOALS

Design parameter	Performance goal
RF band	17.7 to 20.2 GHz
RF power cut	≥200 mW
Gain	≥16 dB
Efficiency	>15 percent
Phase control	Operate on digital input
Mechanical design	Fully monolithic
Unit cost	$100 (1980 dollars, buys > 5000)

TABLE 3. - VARIABLE POWER AMPLIFIER MODULE PERFORMANCE GOALS

Design parameter	Performance goal
RF band	17.7 to 20.2 GHz
RF power cut	0 to 0.5 W (variable)
Gain	20 dB max. (variable)
Efficiency	15 percent/6 percent
Amplitude control	Operate on digital input
Mechanical design	Fully Monolithic
Unit cost	$760 (1980 dollars) in unit buys of 1000 or more

TABLE 4. - SYSTEM REQUIREMENTS

EIRP per beam	67 dBW
S/C antenna gain (min.)	53 dBW
Scan loss (max.)	2.5 dB
Aperture	13.5 ft
Spot size	0.3 to 0.4 deg
Conus sectors	6
Frequency, R/T	30 GHz/20 GHz

TABLE 5. - POWER/WEIGHT SUMMARY

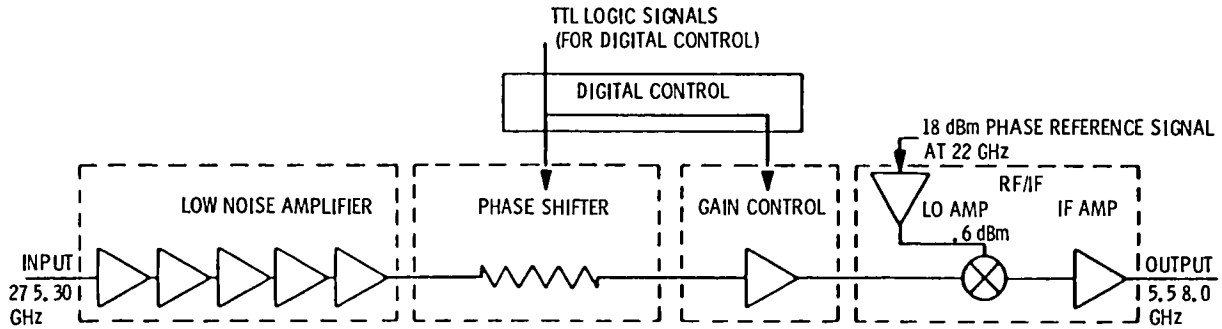
Technology	Prf(tot), W	System weight (ant/feed + amp + hp), lbs	Pdc/(tot), W	Tsw, nsec	Efficiency, percent
'82 System A 4 ANT/4 FEED TWT/VPD	150	774.2	1032	500	14.5
'87 System B 2 ANT/4 FEED MMIC	[a]400	319.5	2160	<1	18.5
'87 System C 1 ANT/2 FEED MMIC	150	307.5	765	<1	19.6
'87 System D 1 ANT/1 FEED MMIC	150	278	765	<1	19.6

[a]System B has 8/3 capacity of Systems A, C and D.

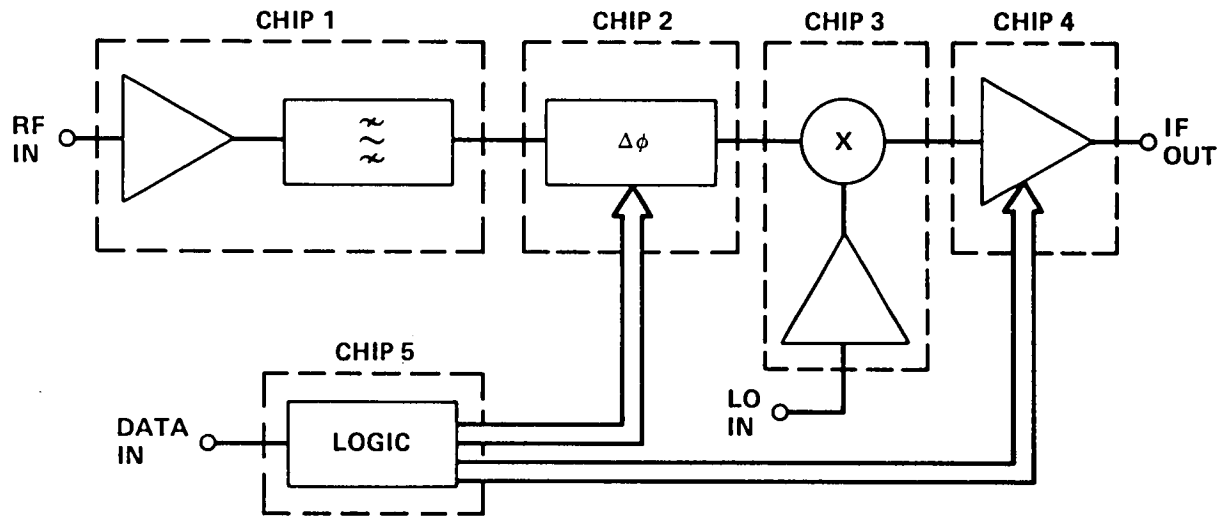
TABLE 6. - COST/WEIGHT SUMMARY

	'82 Tech	'87 Tech		
	System A 4 ANT/4 FEEDS TWT + VPD	System B 2 ANT/4 FEEDS MMIC	System C 1 ANT/2 FEEDS MMIC	System D 1 ANT/1 FEED MMIC
Antenna cost ($M)	23.7	[a]33.0	20.7	18.5
TWT + PPS cost ($M) (scan beams, 6 + 3 TWT's and PPS @ $3M/ea)	27	———	——	——
Total	50.7	33.0	20.7	18.5
$ Saved over System A ($M) (conventional)	——	17.74	31.2	33.2
Weight saved over System A (lbs)	——	455 lbs	467 lbs	496 lbs

[a]System B has 8/3 capacity of Systems A, C and D.



(a) Honeywell approach.



(b) Hughes approach.

Figure 1. - Block diagram of receiver.

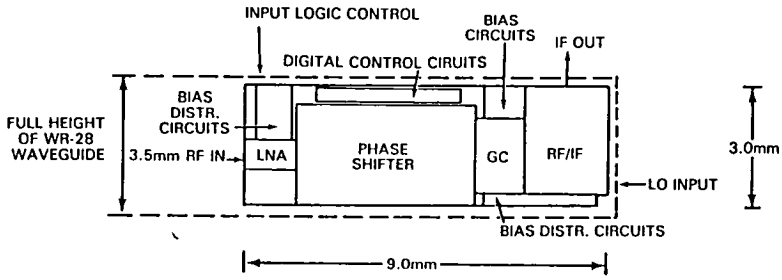


Figure 2. - Receive module layout.

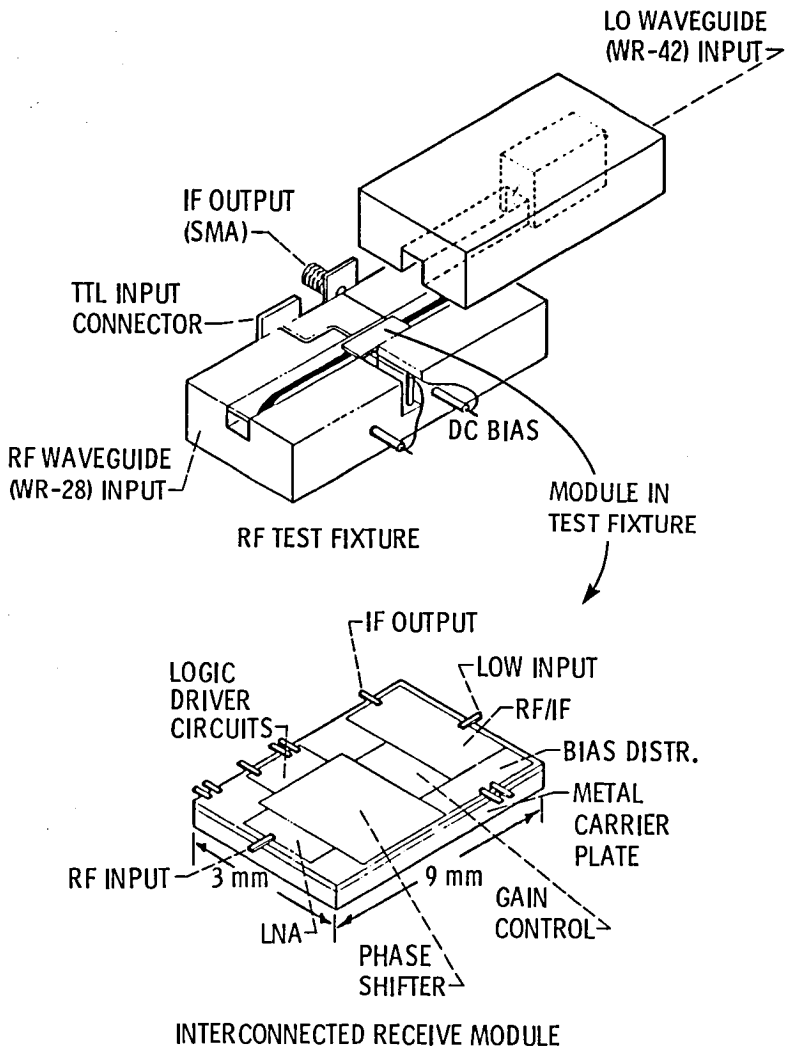


Figure 3. - Receive module and RF test fixture.

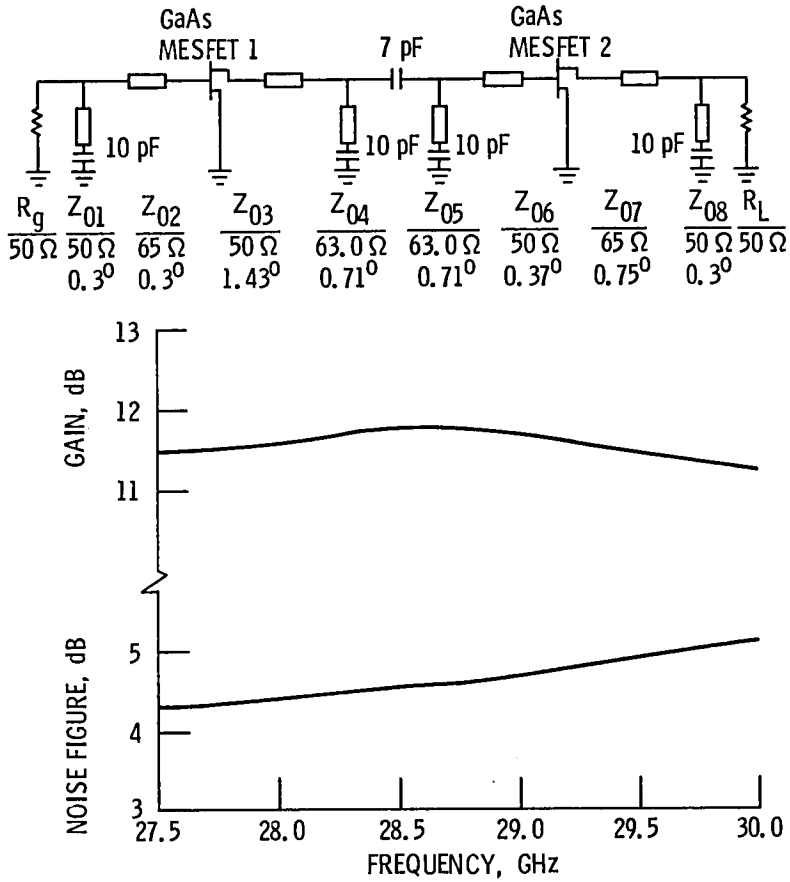


Figure 4. - Design for monolithic LNA (HAC-TRC).

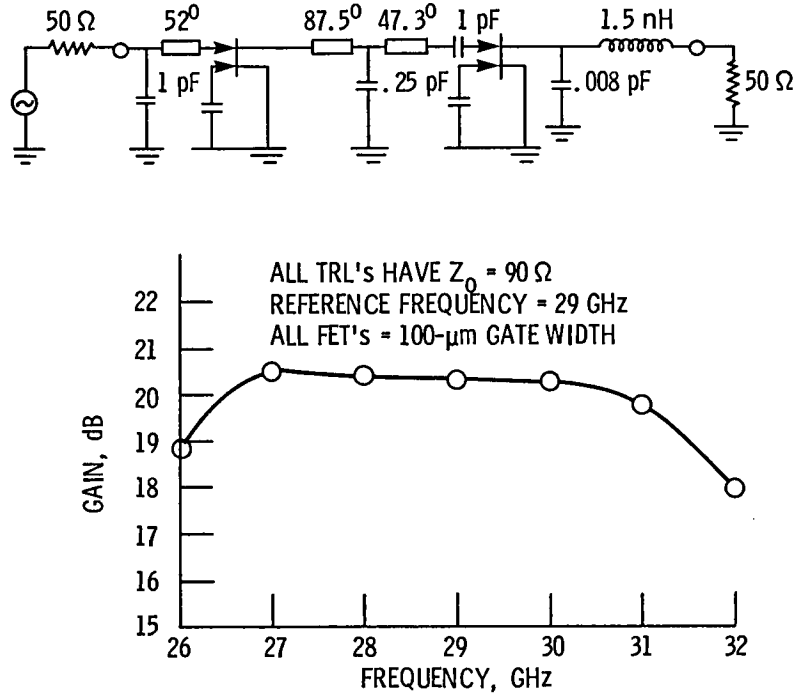
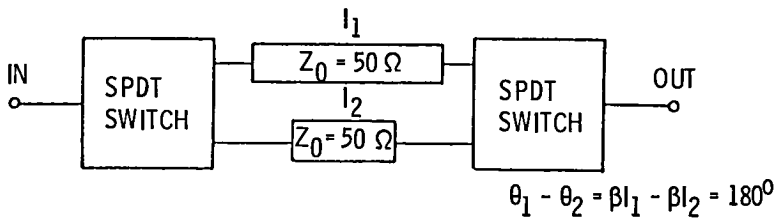
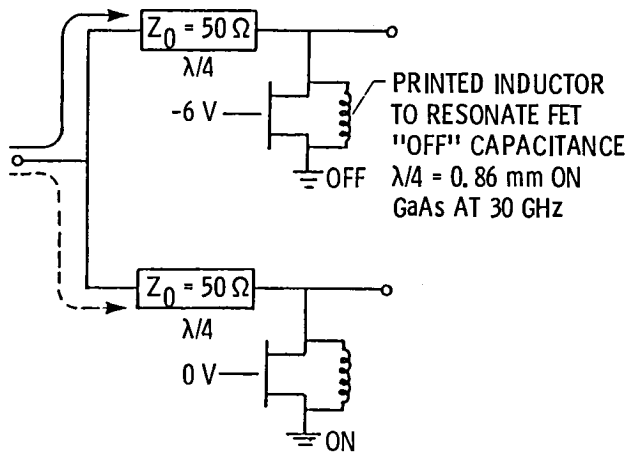


Figure 5. - Design for monolithic dual gate amplifier (MH-CTC).



(a) One-bit phase shifter.



(b) SPDT switch using unbiased FET's.

Figure 6. - Schematic diagram of one-bit phase shifter.

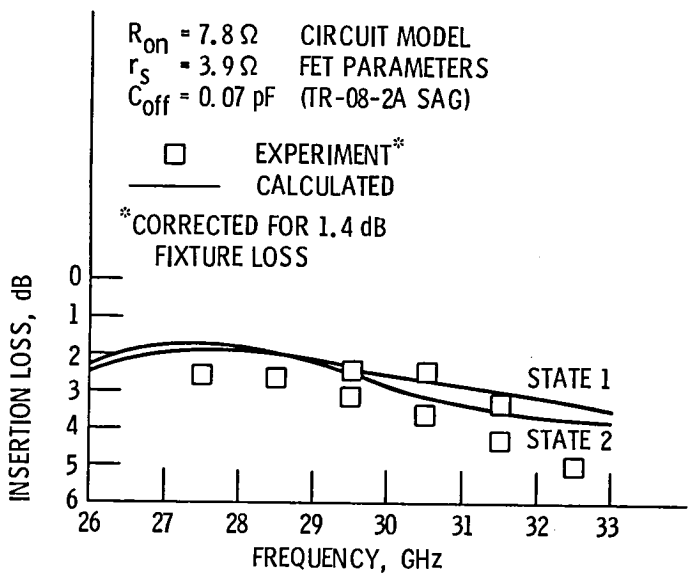


Figure 7. - Comparison of measured and calculated insertion loss for SAG phase shifter.

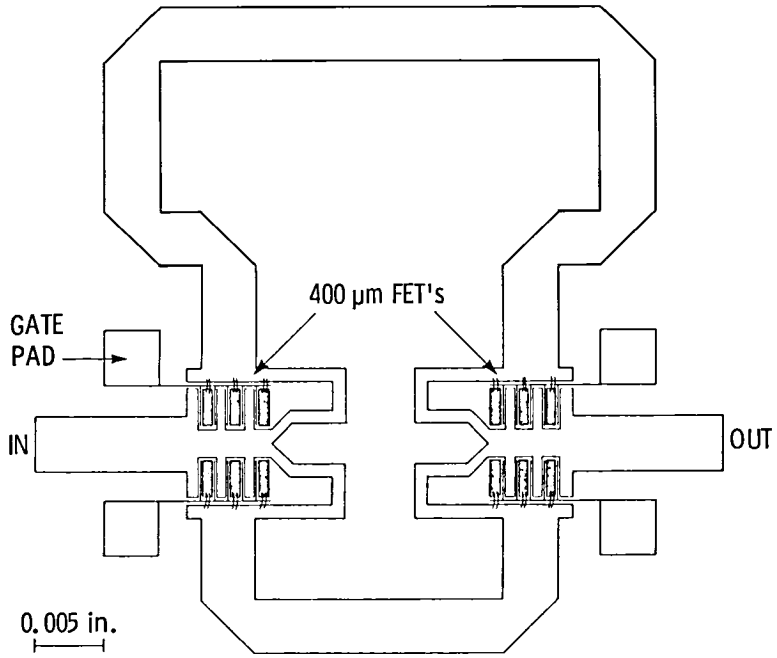


Figure 8. - Layout of 180^0 bit using four series FET switches.

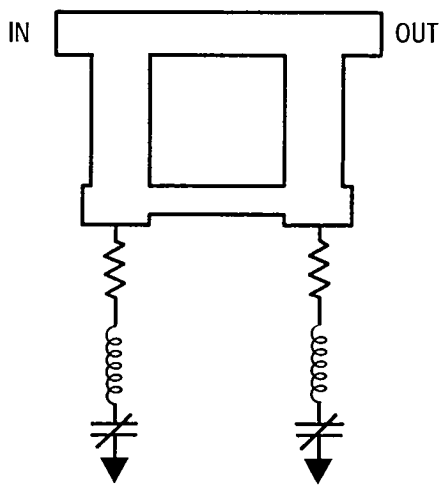


Figure 9. - Analog phase shifter.

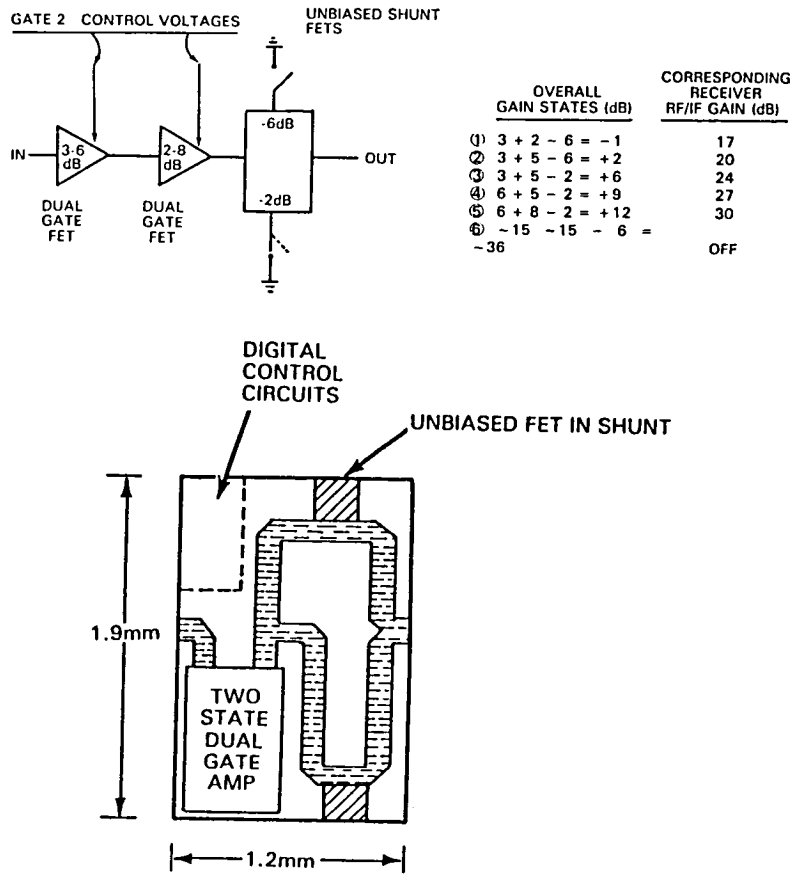
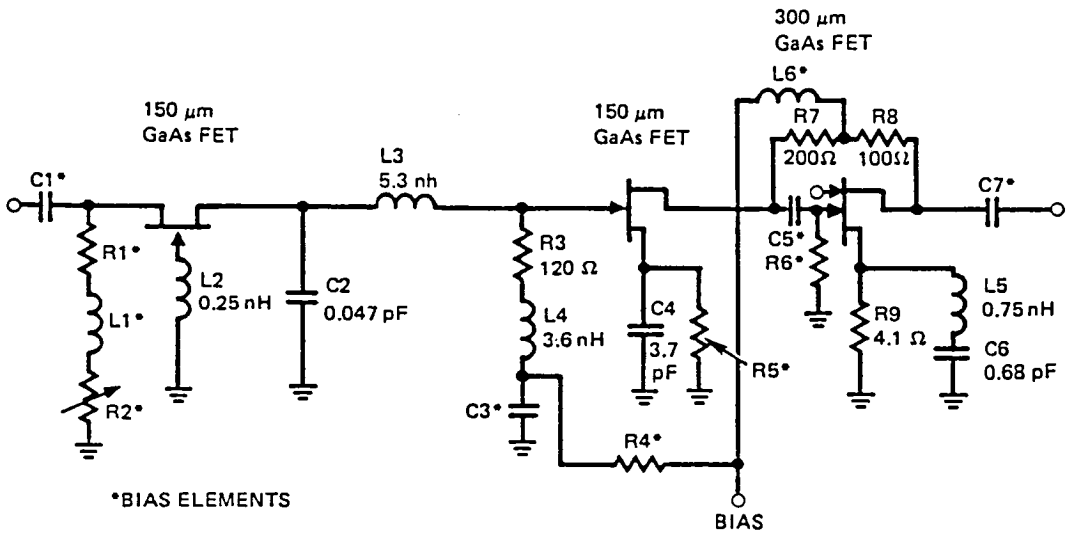
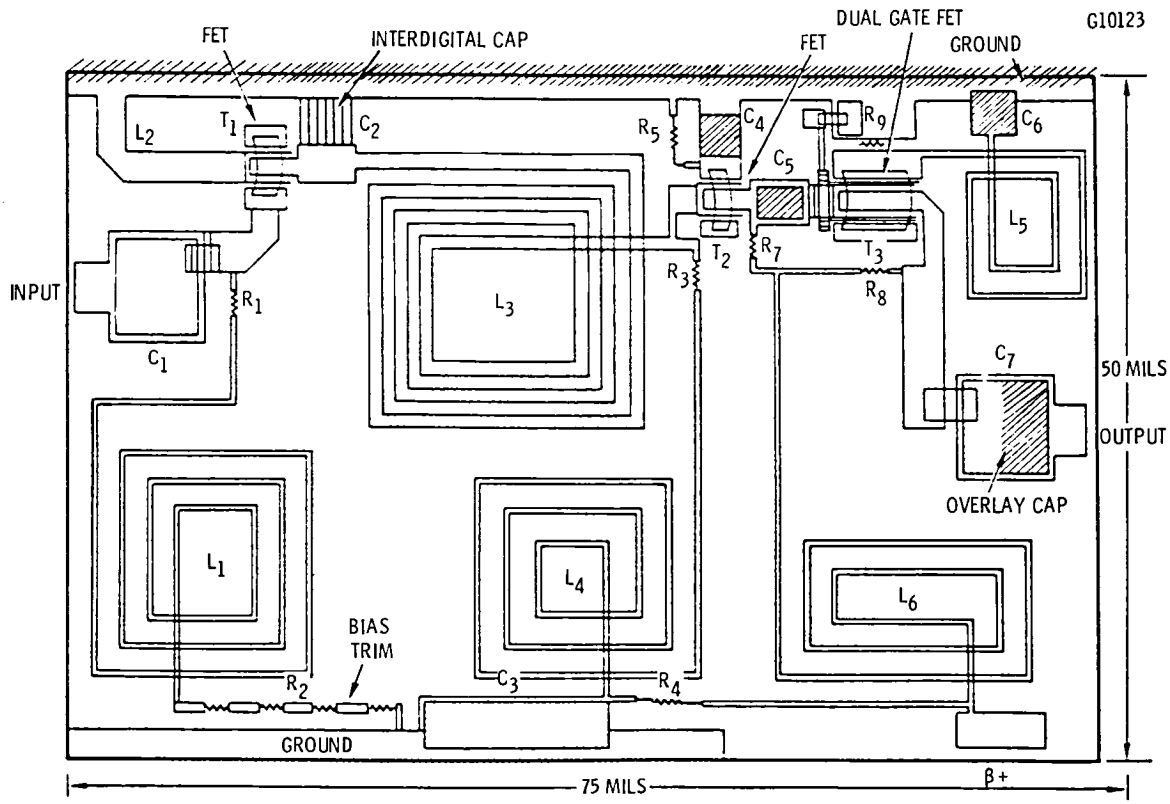


Figure 10. - Gain control design and chip layout (MH-CTC).



(a) Circuit diagram of three stage GaAs IC amplifier.



(b) Chip layout of three stage amplifier.

Figure 11. - Gain control submodule (HAC-TRC).

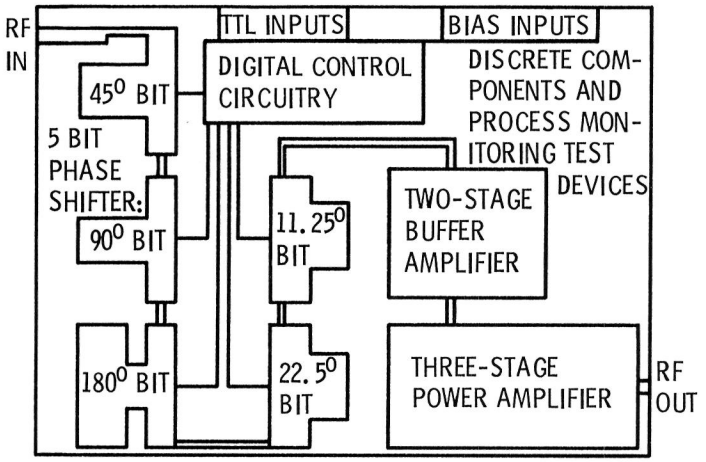


Figure 12. - Block diagram of the 20 GHz monolithic transmit module.

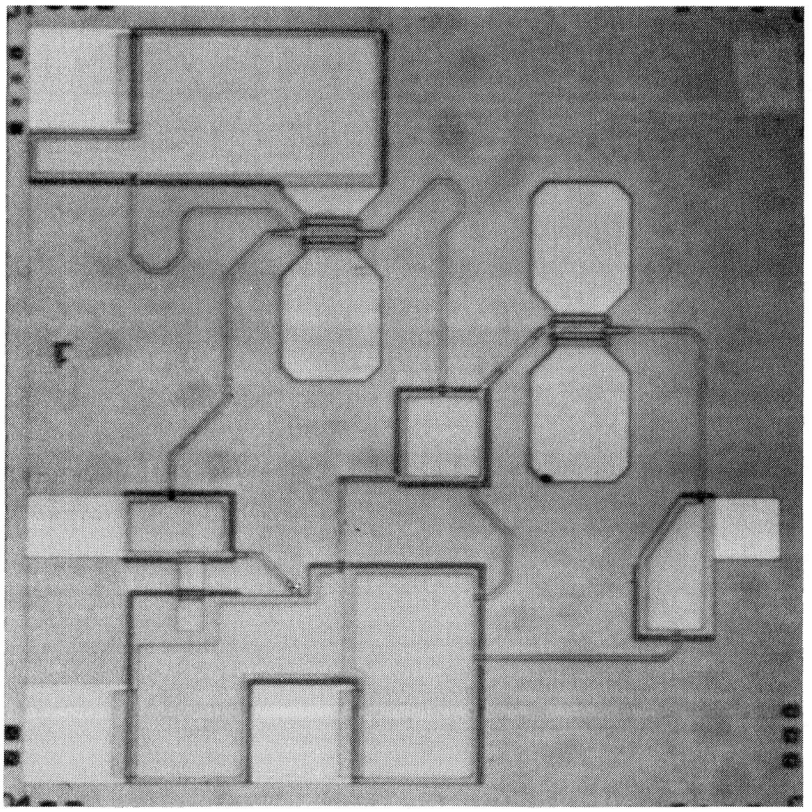


Figure 13. - Photograph of two-stage buffer amplifier.

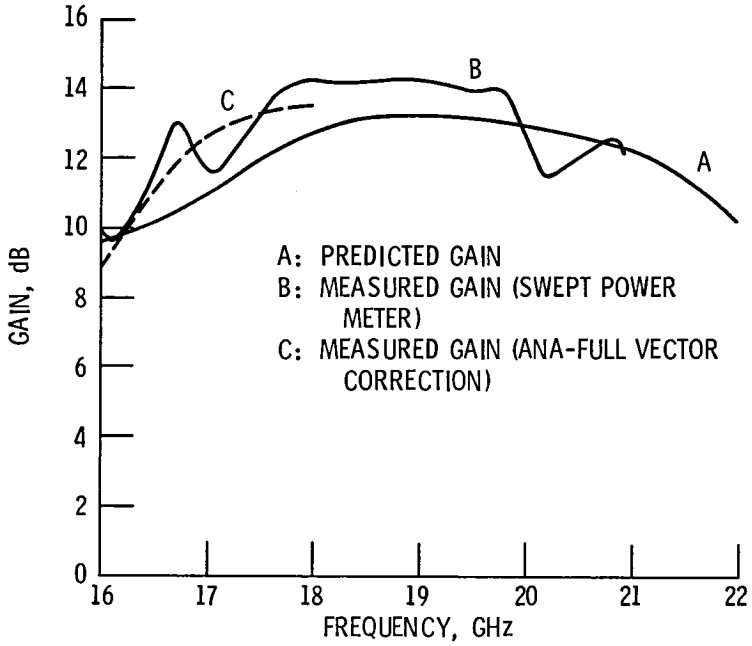
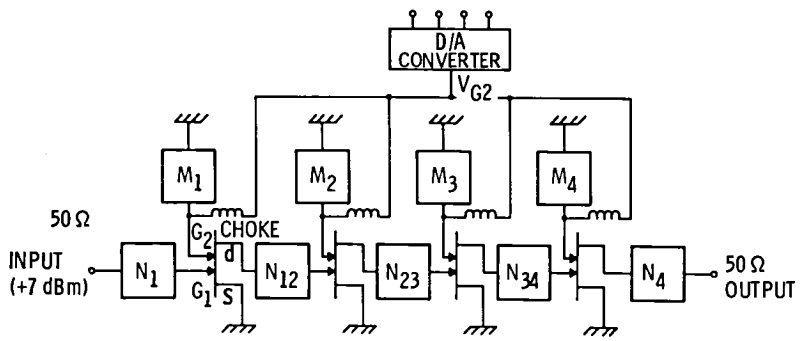


Figure 14. - Measured gain of the 20 GHz two-stage amplifier.



CONTROL VOLTAGE	300 µm	300 µm	600 µm	1500 µm	TOTAL GAIN, dB	OUTPUT POWER, mW
V_{G2} (1)	6	5	5	4	20	500
V_{G2} (2)	4.5	3.5	3.5	2.5	14	125
V_{G2} (3)	3.5	2.5	2.5	1.5	10	50
V_{G2} (4)	2.0	1.0	1.0	0	4	12.5
V_{G2} (5)	~-20	~-20	~-20	~-20	~-80	-----

Figure 15. - A GaAs VPA module with dual-gate FET amplifier and D/A converter.

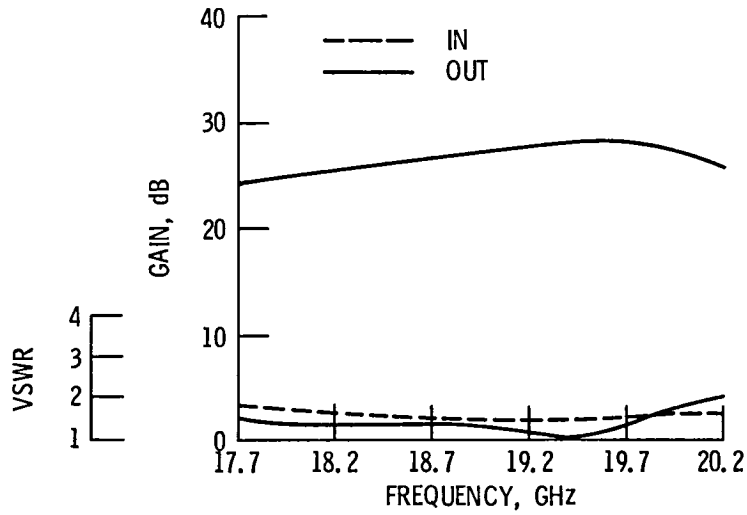


Figure 16. - Predicted performance of a four-stage dual-gate FET amplifier using complete cascode-connected device models.

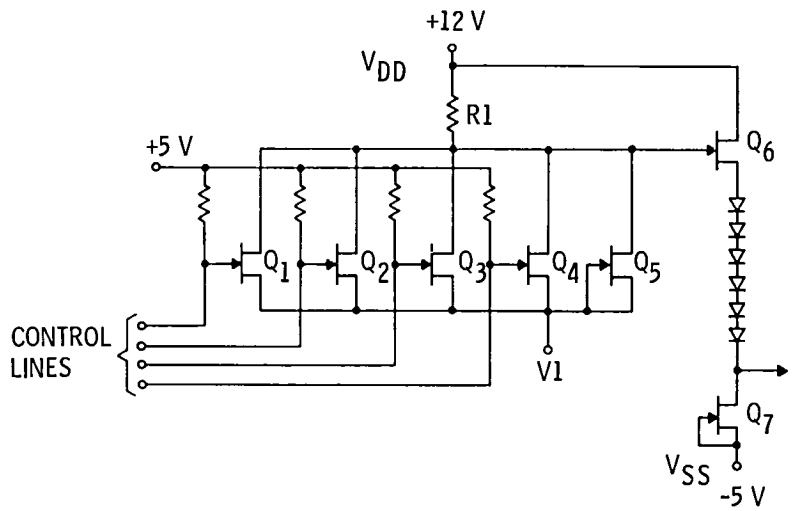


Figure 17. - Circuit diagram for the amplitude control logic submodule.

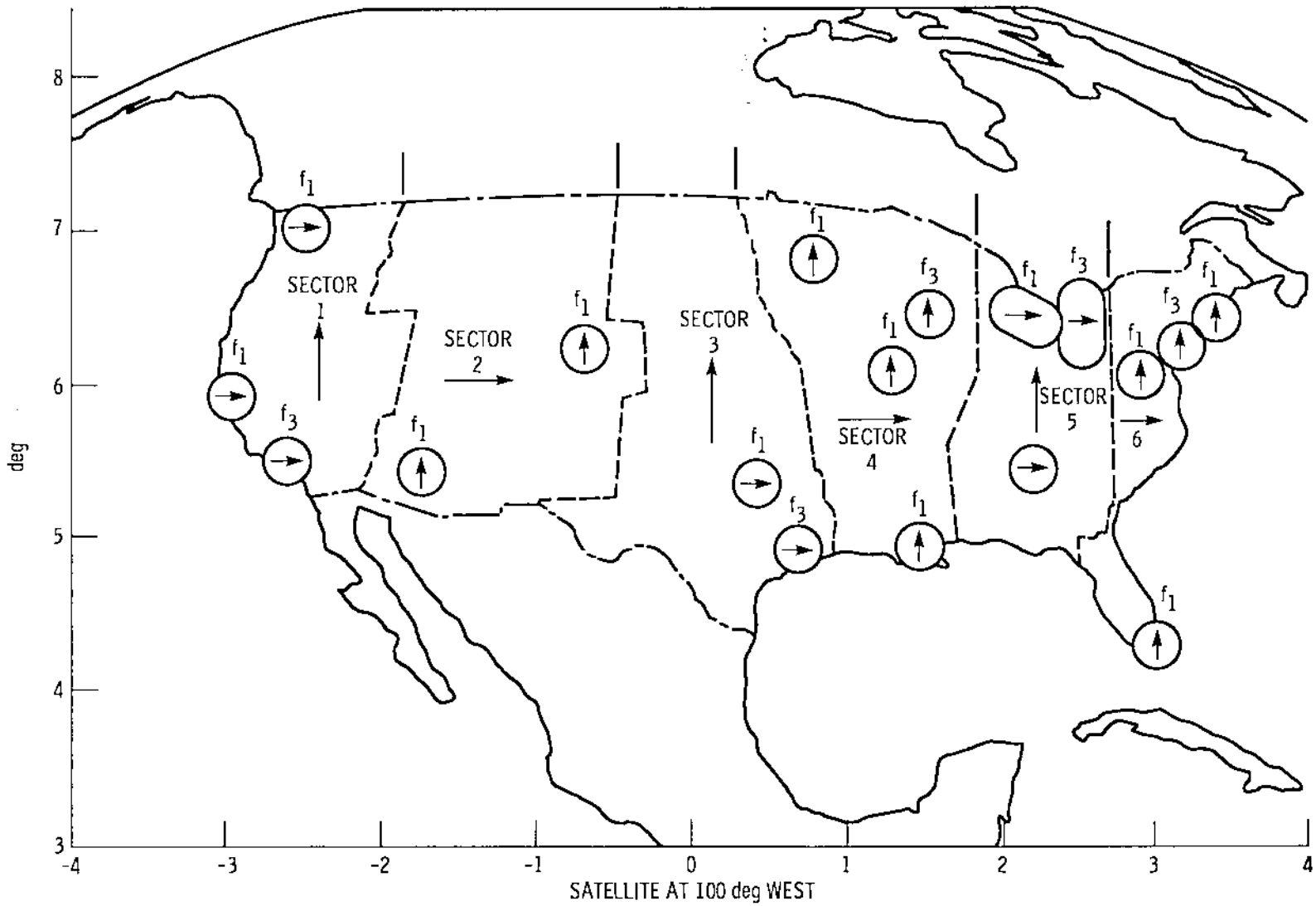
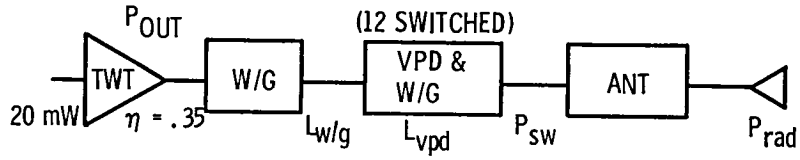


Figure 18. - Fixed beam and scanning beam antenna coverage scenario.



EIRP	G_{ant}	P_{rad}	$L_{w/g}$	L_{vpd}	P_{out}	P_{sw}	P_{dc}/BM	EFF
67 dBW	53 dB	25 W	0.4 dB	3.0 dB	55 W	15 W	172 W*	14.5%

FOR 6 SECTOR BEAMS

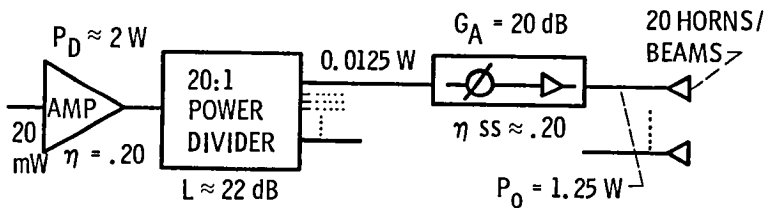
Pdc_{TOT} = 6 x 172 W = 1032 W

*INCLUDES VPD SWITCHING POWER PER BEAM
10 W (20 GHz VPD) + 5 W (30 GHz VPD) = 15 W/BEAM

20 GHz VPD SWITCHING POWER (10 KHz) 0.78 W

30 GHz VPD SWITCHING POWER (10 KHz) 0.41 W

Figure 19. - System A power summary.



EIRP	G_{ant}	P_{rad}/BM	P_{SWITCH}	P_{dc}/BM	EFF
67 dBW	53 dB	25 W	< 1 W	135 W*	18.5%

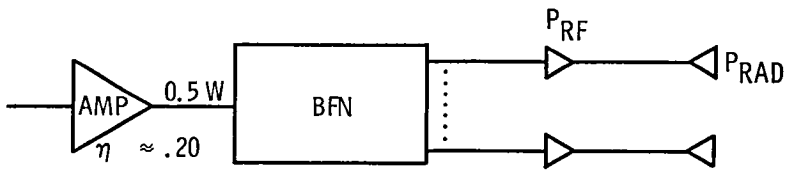
P_{dc}/BM = 20 x (5 x 1.25 W) + (5 x 2 W) = 135 W

P_{dc} TOTAL = 135 W x 16 (BEAMS) = 2160 WATTS**

*INCLUDES 10 W OF DC POWER REQUIRED FOR DRIVER; PHASE SHIFTER SWITCHING POWER IS NEGLIGIBLE

**SYSTEM B HAS 8/3 x CAPACITY OF THE OTHER 3 SYSTEMS

Figure 20. - System B power summary.



EIRP	G_{ant}	P_{rad}	#ELEM	PRF	η	P_{dc}/MOD	P_{dc}/BM	P_{sw}	EFF
67 dBW	53.dB	25 W	500	0.05 W	.20	0.25	127.5*	< 1 W	19.6%

FOR 6 SECTOR BEAMS

$$P_{dc\ TOTAL} = 6\ (127.5\ W) = 765\ W$$

Figure 21. - System C power summary.

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16. Abstract

The development of fully monolithic gallium arsenide (GaAs) receive and transmit modules suitable for phased array antenna applications in the 30/20 gigahertz bands is presented. Specifications and various design approaches to achieve the design goals are described. Initial design and performance of submodules and associated active and passive components are presented. A tradeoff study summary is presented highlighting the advantages of distributed amplifier approach compared to the conventional single power source designs.

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