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30/20 GHz SPACECRAFT GaAs FET SOLID STATE TRANSMITTER FOR TRUNKING AND CUSTOMER-PREMISE-SERVICE APPLICATIONS

FINAL REPORT

FOR

CONTRACT NO. NAS3-22504

Prepared for
National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135

29 August 1983

Prepared by
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16. Abstract

This report describes work at Texas Instruments on NASA Contract No. NAS3-22504. The objective of this contract was to develop a 20 GHz transmitter to (1) demonstrate the feasibility of providing an efficient, reliable, lightweight GaAs FET transmitter by the end of fiscal year 1982; (2) be the proof of concept (POC) model for a flight-qualified transmitter to be used on a 30/20 GHz communication system in 1985; and (3) provide an advanced data base for use in communication payload definitions and design studies. The POC model power output goal is 6 to 7.5 W over the 17.7 to 20.2 GHz frequency range.

Our approach was to combine sixteen 30 dB 0.5 W amplifier modules. By combining a large number of modules, we satisfied the requirement for a graceful degradation. If one module fails we show that the output power drops by only 0.43 dB. Also, by incorporating all the gain stages within the combiner the overall combining efficiency is maximized.

We developed a 16 way waveguide divider combiner. Waveguide was chosen to minimize the insertion loss associated with such a large corporate feed structure. Tests showed that the 16 way insertion loss was less than 0.5 dB. To minimize loss, a direct transition from waveguide to microstrip, using a finline on duroid substrate, was developed. Excellent results were obtained; two transitions mounted back to back had an insertion loss less than 0.5 dB over the full bandwidth. Progress was also made in the device area. At the end of the contract, FETs

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fabricated on MBE grown material, demonstrated superior performances. For example, a 600 μm device was capable of 320 mW output power with 5 dB gain and 26.6% efficiency at 21 GHz.

The 16 module amplifier gave 8.95 W saturated output power with 30 dB gain. The overall efficiency was 9%. The 3 dB bandwidth was 2.5 GHz. At 17.7 GHz the amplifier had 5 W output power and at 20.2 GHz it still had 4.4 W.

The amplifier failed during noise measurement. Two problems were identified. The resistorless Wilkenson combiner of the sixth stage was potentially unstable. Also all the drain bias lines were tied together and all the gate bias lines were tied together so that a transient was able to propagate throughout the amplifier. When the amplifier was rebuilt the Wilkenson combiner was eliminated and a single MBE 1350 μm device was used with subsequent power output reduction. Also four power supply regulators (one per quad) were used for the gate and drain bias lines. Following these modifications, stable operation was demonstrated at a lower power level. The amplifier was burned-in for 24 hours before shipment. The 3.5 W output power (with 30 dB gain) was consistent with the use of a single 1350 μm device in the sixth stages.

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SECTION I
EXECUTIVE SUMMARY

This report describes work at Texas Instruments on NASA Contract No. NAS3-22504. The objective of this contract was to develop a 20 GHz transmitter to (1) demonstrate the feasibility of providing an efficient, reliable, lightweight GaAs FET transmitter by the end of fiscal year 1982; (2) be the proof of concept (POC) model for a flight-qualified transmitter to be used on a 30/20 GHz communication system in 1985; and (3) provide an advanced data base for use in communication payload definitions and design studies. The POC model power output goal is 6 to 7.5 W over the 17.7 to 20.2 GHz frequency range.

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We developed a 16 way waveguide divider combiner. Waveguide was chosen to minimize the excess insertion loss associated with such a large corporate feed structure. Tests showed that the 16 way insertion loss was less than 0.5 dB. To minimize loss a direct transition from waveguide to microstrip, using a finline on a duroid substrate, was developed. Excellent results were obtained; two transitions mounted back to back had an insertion loss less than 0.5 dB over the full bandwidth. Progress was also made in the device area. At the end of the contract, FETs fabricated on MBE grown material, demonstrated superior performances. For example, a 600 μm device was capable of 320 mW output power with 5 dB gain and 26.6% efficiency at 21 GHz.

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The amplifier failed during noise measurement. Two problems were identified. The resistorless Wilkenson combiner of the sixth stage was potentially unstable. Also all the drain bias lines were tied together and all the gate bias lines were tied together so that a transient was able to propagate throughout the amplifier. When the amplifier was rebuilt the Wilkenson combiner was eliminated and a single MBE 1530 μm device was used with subsequent power output reduction. Also four power supply regulators (one per quad) were used for the gate and drain bias lines. After these modifications, stable operation was demonstrated at a lower power level. The amplifier was burned-in for 24 hours before shipment. The 3.5 W output power (with 30 dB gain) was consistent with the use of a single 1350 μm device in the sixth stages.

SECTION II
OVERALL TRANSMITTER DESIGN

A. Electrical Description

The limited power output capability of a single multicell FET chip requires the use of circuit-level power combining. For this program, the single chip saturated output power is 1 W for a 2.5 mm gate width FET over a 17 to 21 GHz frequency. At saturated power levels, however, third order intermodulation products may be as high as 15 dBc, or even 10 dBc. Consequently, the drive level must be reduced to achieve more linear operation. Available data from a six-stage, 15 GHz, 100 mW FET preamplifier indicate a reduction of as much as 2.5 dB from saturated power output power may be required to achieve less than 20 dBc third order intermodulation distortion. This implies that to achieve the 7.5 W transmitter output power and linearity goal, at least 14 amplifiers, each having an output stage using a 1 W device, must be circuit combined. Since several stages of binary power splitting (number of divider/combiner branches = 2^n, n is the number of stages) can be realized with a corporate (or tree) structure of 3 dB directional couplers, a 16 way waveguide manifold incorporating four port magic tees is used for the input divider, and also for the output combiner. These two manifolds connect to 16 multistage 31 dB gain module amplifiers that are constructed using microstrip technology.

The choice of waveguide over microstrip dividing combining is dictated by the requirement of maximum efficiency. Microstrip power dividing or combining, although more compact, is considerably more lossy. The approach using a large number of modules (16 versus 8 or 4) was chosen because it maximizes the graceful degradation character of the transmitter amplifier. It can be shown that because of the isolated amplifier modules and the scattering matrix of the H-plane waveguide T, one module failure will cause only a 0.43 dB degradation

in total transmitter output power. Certainly, having a single driver amplifier would jeopardize the entire transmitter performance in case of a device failure in the driver stages. The gain is incorporated entirely within the 16 modules so that the total combining efficiency is greater if high gain modules are used. Figure 1 shows curves of added power combining efficiency versus combiner loss with amplifier gain as a parameter. Two things are evident from this figure. First it is important to combine high gain modules so the majority of loss is restricted to the output combining network. Second, a 0.5 dB excess insertion loss results in a combining efficiency of about 89%. It should be noted that these curves assume identical amplifiers in the actual case; phasing and amplitude variations between modules will affect the total power combining efficiency. This again meets the requirement of a low loss divider/combiner.

Figure 2 is a block diagram of the combining manifold. The 16 way waveguide combiner is described in Section II.B. The amplifier modules consist of six stages to achieve a gain of about 31 dB. FET gate width used in the stages ranges from 150 μm to 2 x 1350 μm. Figure 3 is a block diagram of a single amplifier module showing the gain and output power budget as it was originally designed (changes made during the program are described later). To interface the waveguide with the microstrip FET amplifiers, low-loss microstrip-to-waveguide transistors are incorporated at the input and output of each module. These transistors and their performances are described in Section II.C.

B. 16 Way Combining Manifolds

Figure 4 is a block diagram of the combining manifold. Waveguide magic tees, with the fourth port terminated, are used to achieve both 3 dB power splitting and isolation between ports. The waveguide size is WR-51 (15 to 22 GHz). Figure 5 shows the 20 GHz manifold structure. It is dip-braze fabricated from several precision aluminum subassemblies, including the magic

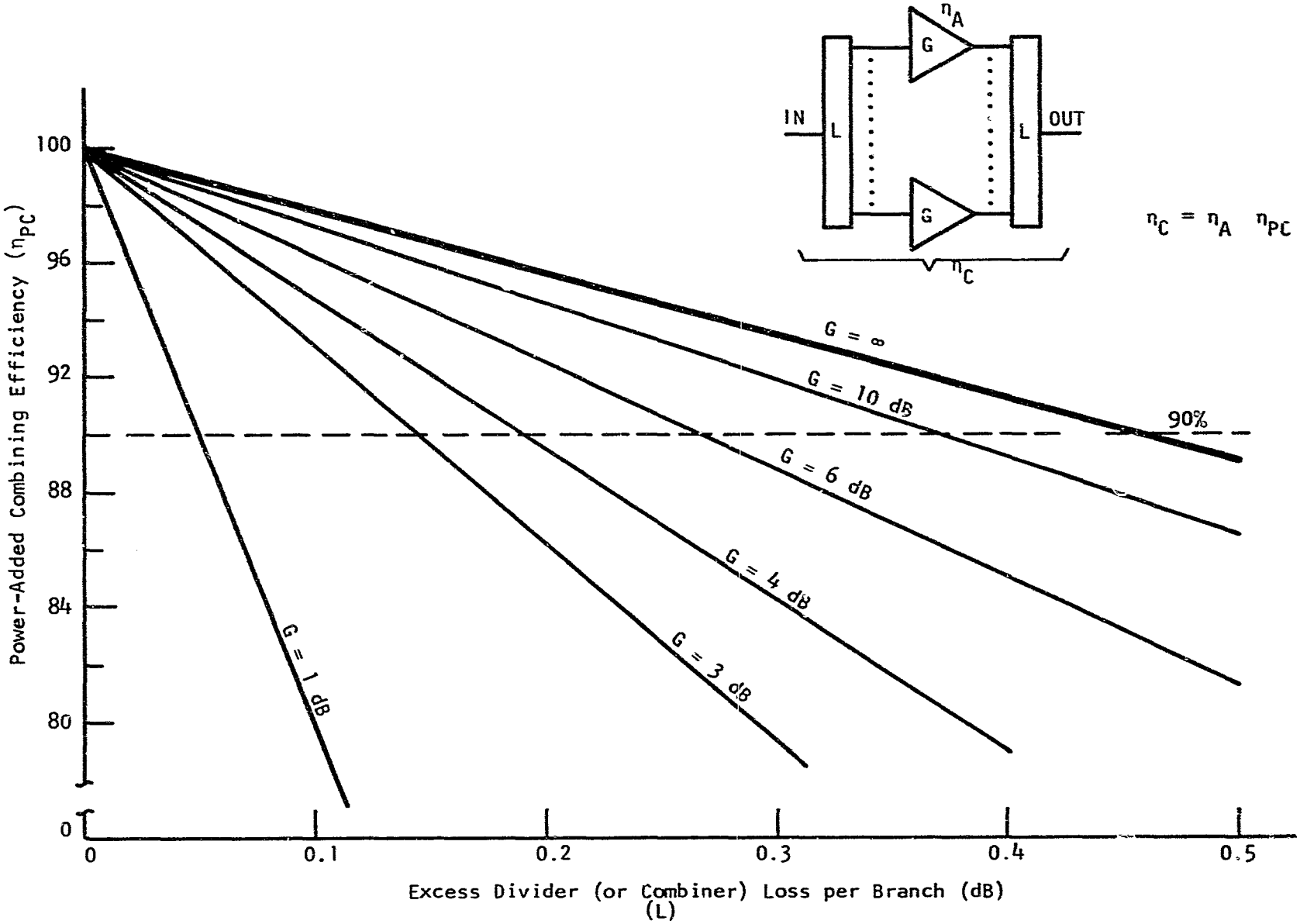


Figure 1 Added Power Combining Efficiency vs Combiner Loss with Amplifier Gain as a Parameter

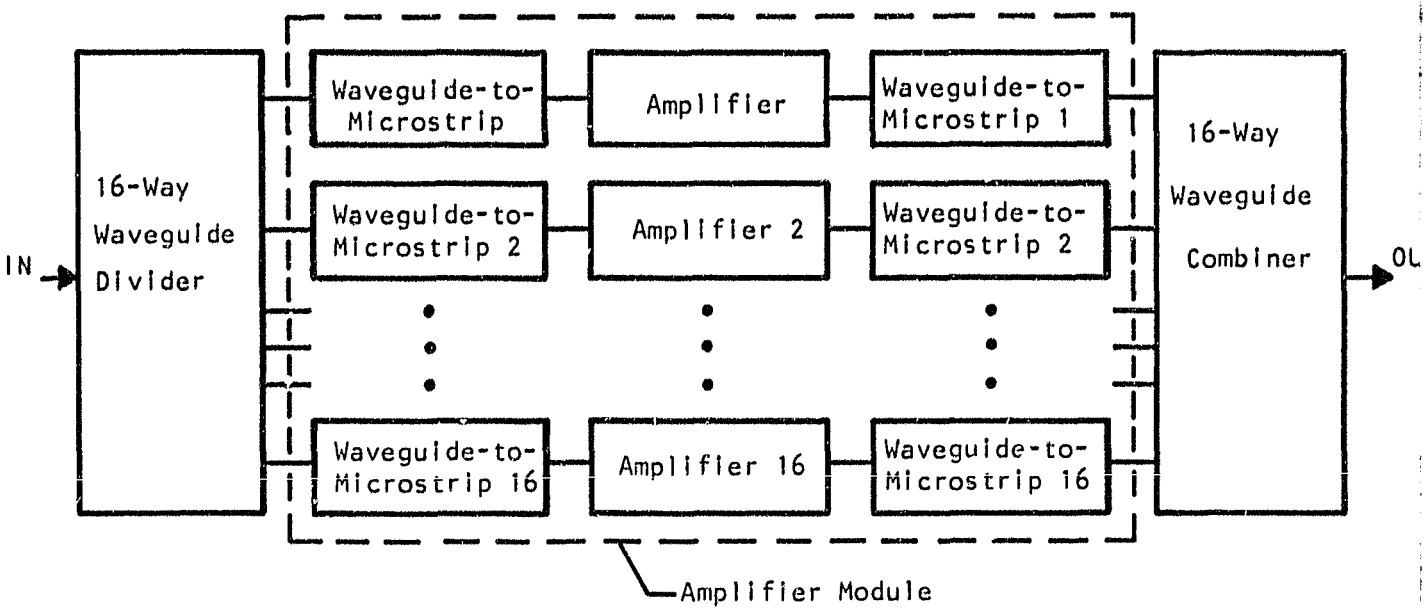
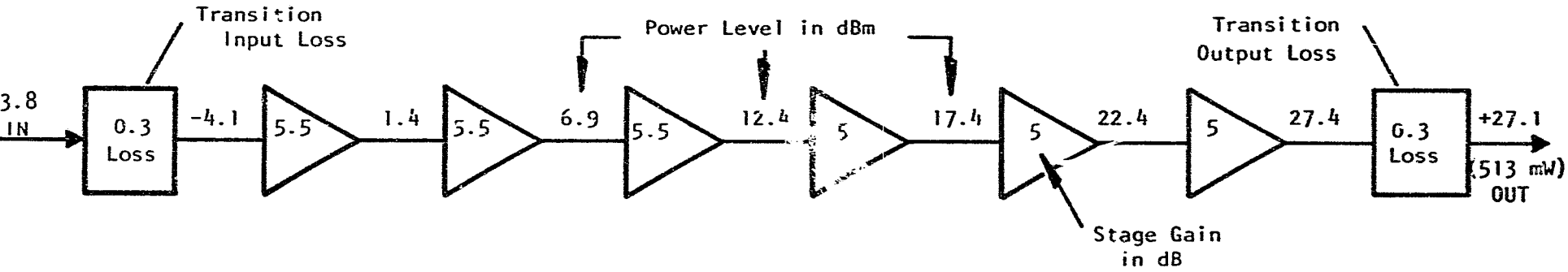


Figure 2 Block Diagram of General Design Approach



Gain Stage	1	2	3	4	5	6
FET Gate Width (μm)	150	150	150	300	600	2,500

FET Type: Recently Developed Laboratory Devices (π-Gate FETs)

Total Module Gain - 30.9 dB

Module Output Power - 512 mW

Figure 3 Block Diagram of 31 dB Amplifier Module

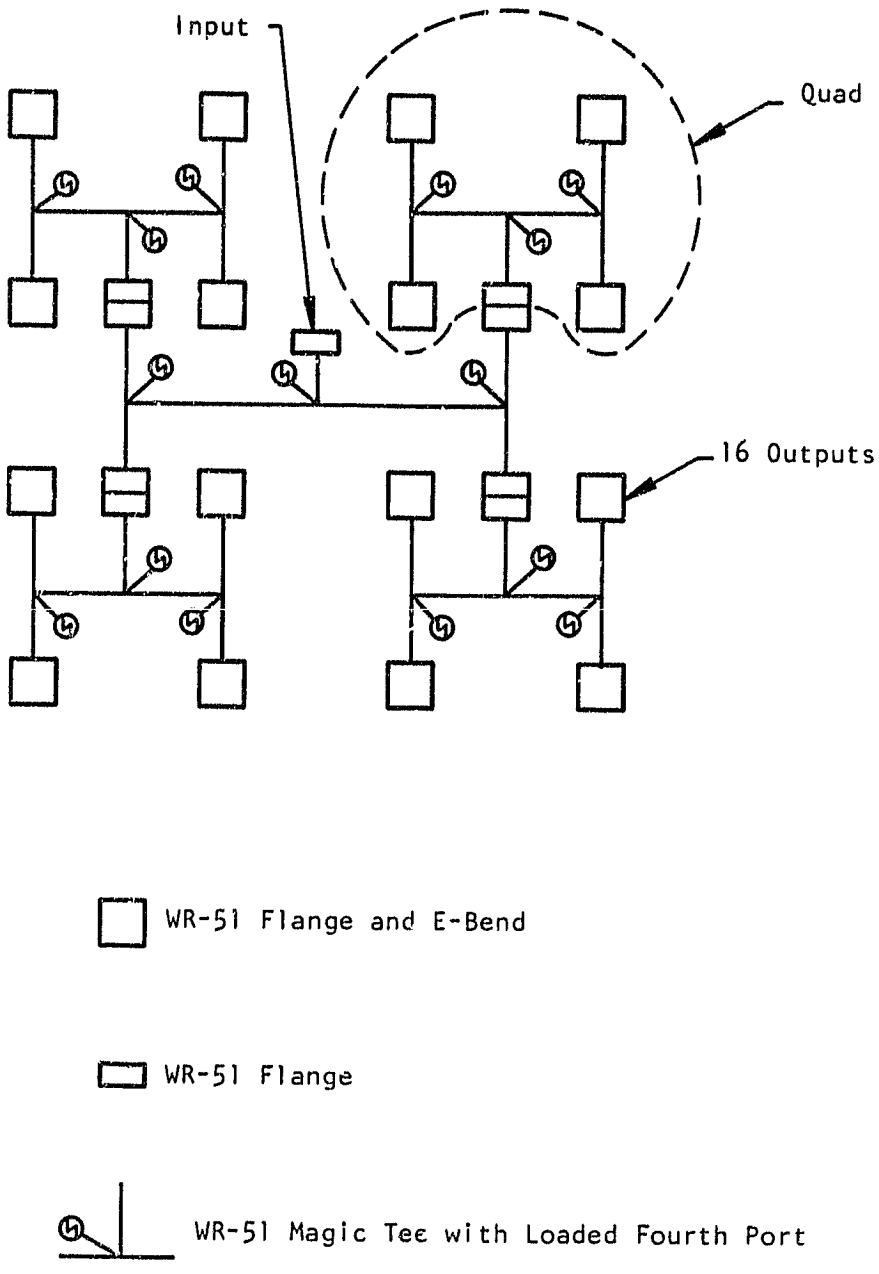


Figure 4 Block Diagram of Power Divider/Combiner

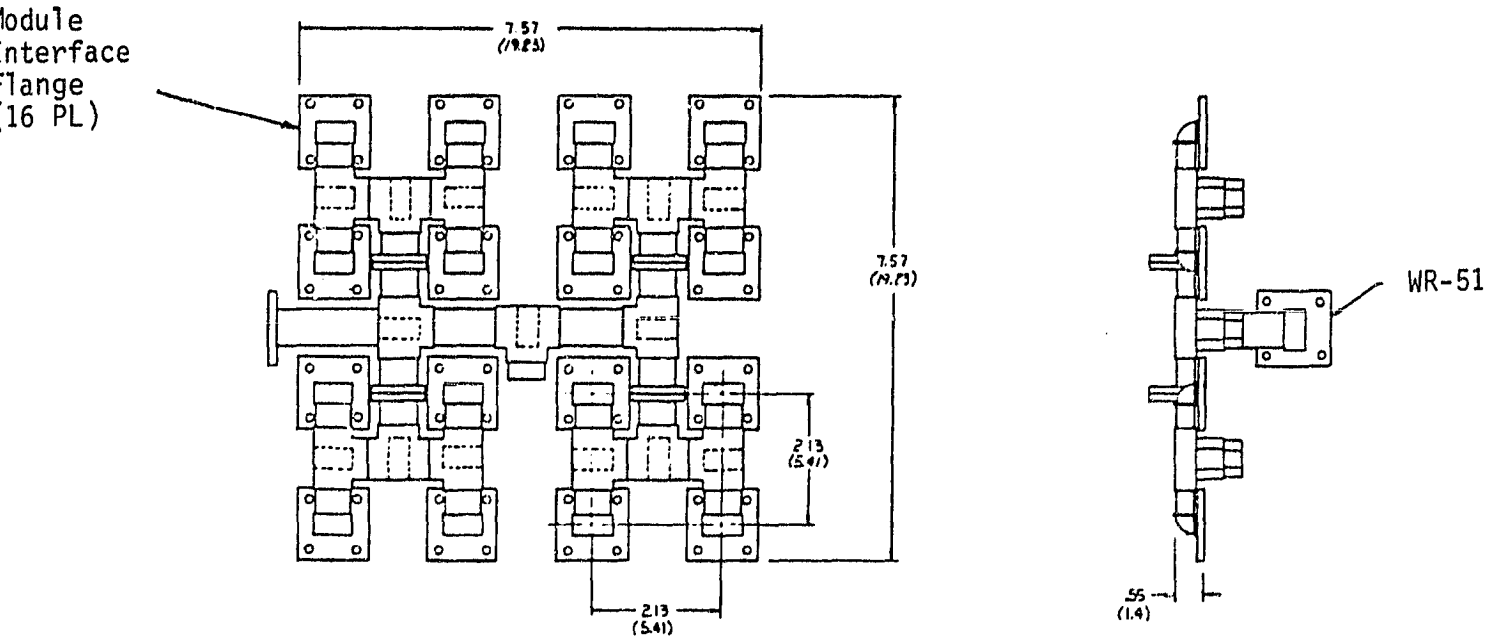


Figure 5 20 GHz Amplifier Manifold

tee sections, which are individual four port castings. The plan dimensions of the manifold alone are [9.3 (7.6) x 19.3 (7.6) $cm^2/in.^2$]. The fourth port of the magic tee is less than 2.5 cm (1 in.) in length.

Figure 6 shows the results obtained from the two quad manifolds used as splitter and combiner with all ports properly loaded. The manifolds are separated by four pieces of WR-51 waveguide that are the same length as the amplifier modules. The results show a mean value of approximately 0.3 dB excess loss for both manifolds. This level gives a combining efficiency between 90 to 94% for a single sixteen way combiner/splitter. Figure 7 shows the balance and insertion loss for the four ports of the quad. These measurements were made by observing one port while the three remaining ports were loaded with WR-51 waveguide terminations.

C. Waveguide to Microstrip Transition

To minimize loss, a direct transition from waveguide to microstrip is preferred over a scheme that uses an interim coaxial section. Such a transition, having a loss of only 0.25 dB from 17.7 to 19.7 GHz, has been reported by van Heuven[1] who presents measurements that characterize the transition and design details. Figure 8 shows a diagram of the transition. A dielectric substrate is inserted along the length of the waveguide, dividing the width of the guide in two equal parts. Two tapered ridges etched on opposite sides of the substrate capture the incoming energy and trap it between two parallel strips that form a balance line with the dielectric medium. Since the ridges short to the breadwalls of the guide, the waveguide TE10 mode is supressed, and energy is transferred to the balanced line etched on the substrate. A balun converts the balance line to a standard 50 Ω microstrip line. The ground plane of the microstrip also shorts to the broadwalls of the guide, dividing it into two separate chambers. The microstrip side of the substrate thus is enclosed by a waveguide whose cutoff frequency is far from the waveguide band.

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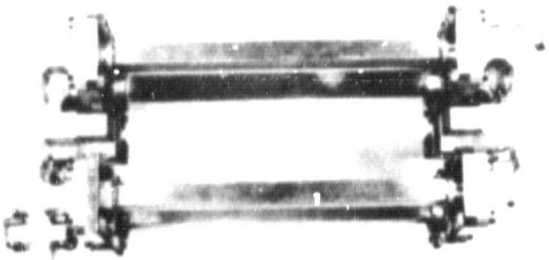
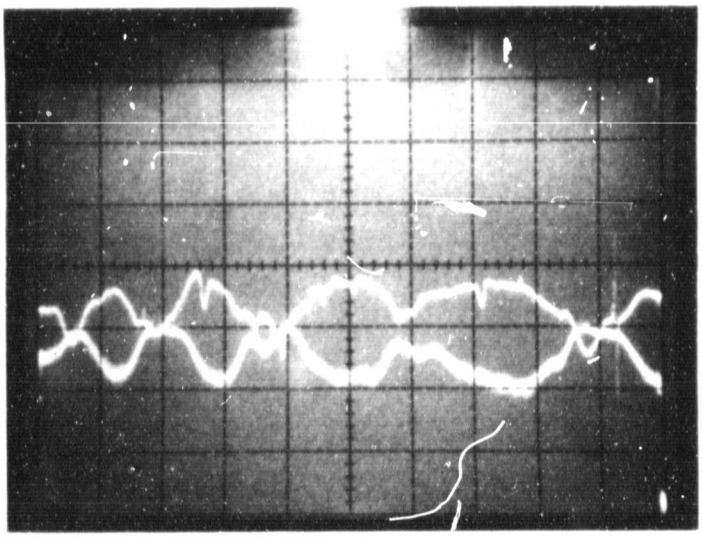
1. J. H. C. van Heuven, "A New Integrated Waveguide-Microstrip Transition," IEEE Trans. Microwave Theory Tech. MTT-24, 144 (1976).





Top Trace
CL Ret 6 dB
0 5 dB/div

Bottom Trace
Input Return Loss
CL Ref 0 dB
10 dB/div

Frequency Range 17.7 to 20.2 GHz

Figure 6 Excess Loss of Pair of Waveguide Manifolds

Lower Trace
Return Loss
Ref C. L. 0dB
10 dB/div

Frequency 17.7 - 20.2 GHz
Top Trace
Ref C. L. -6.3 dB
0.5 dB/div

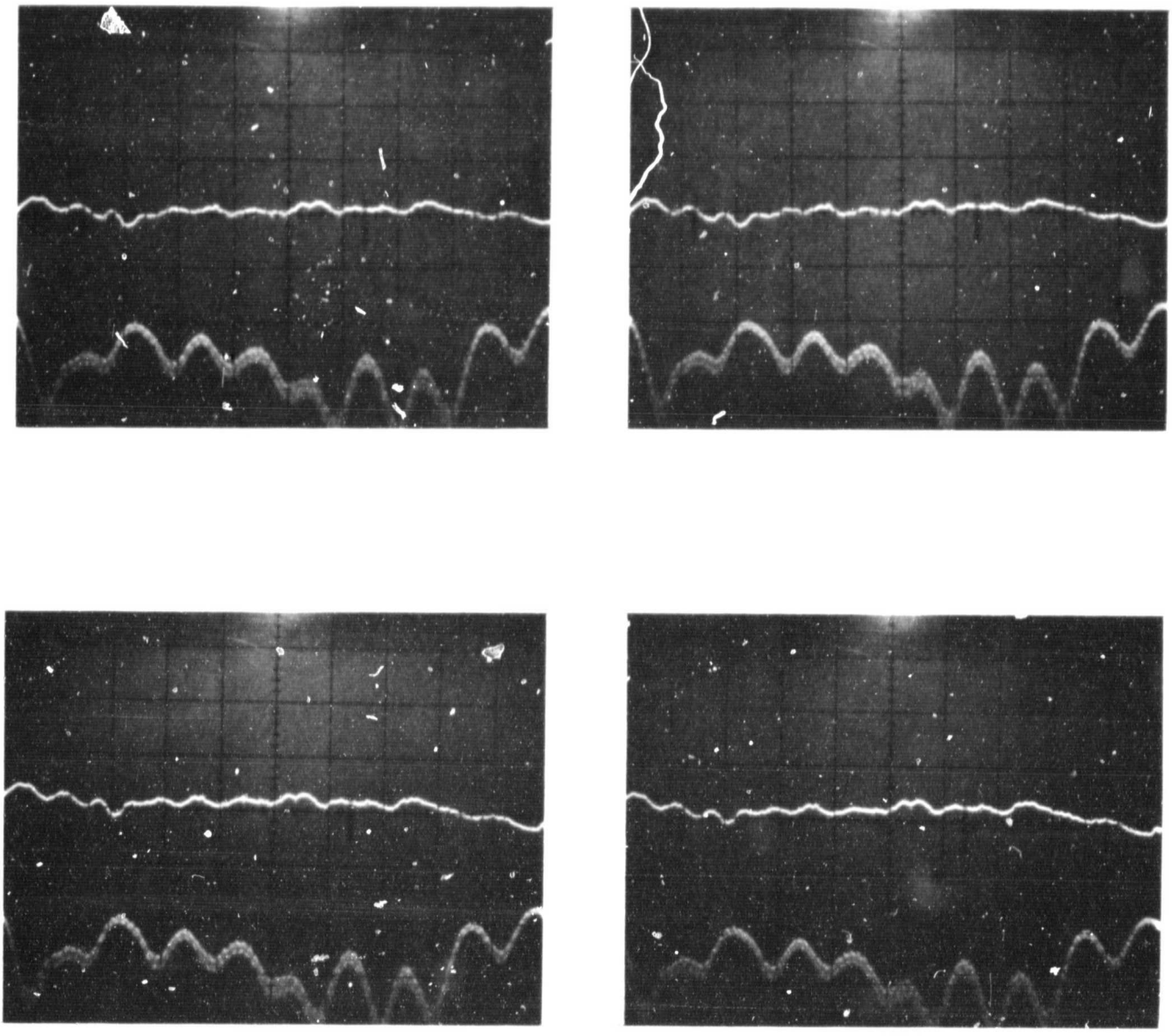


Figure 7 Amplitude Balance of Four Ports of Quad No. 1

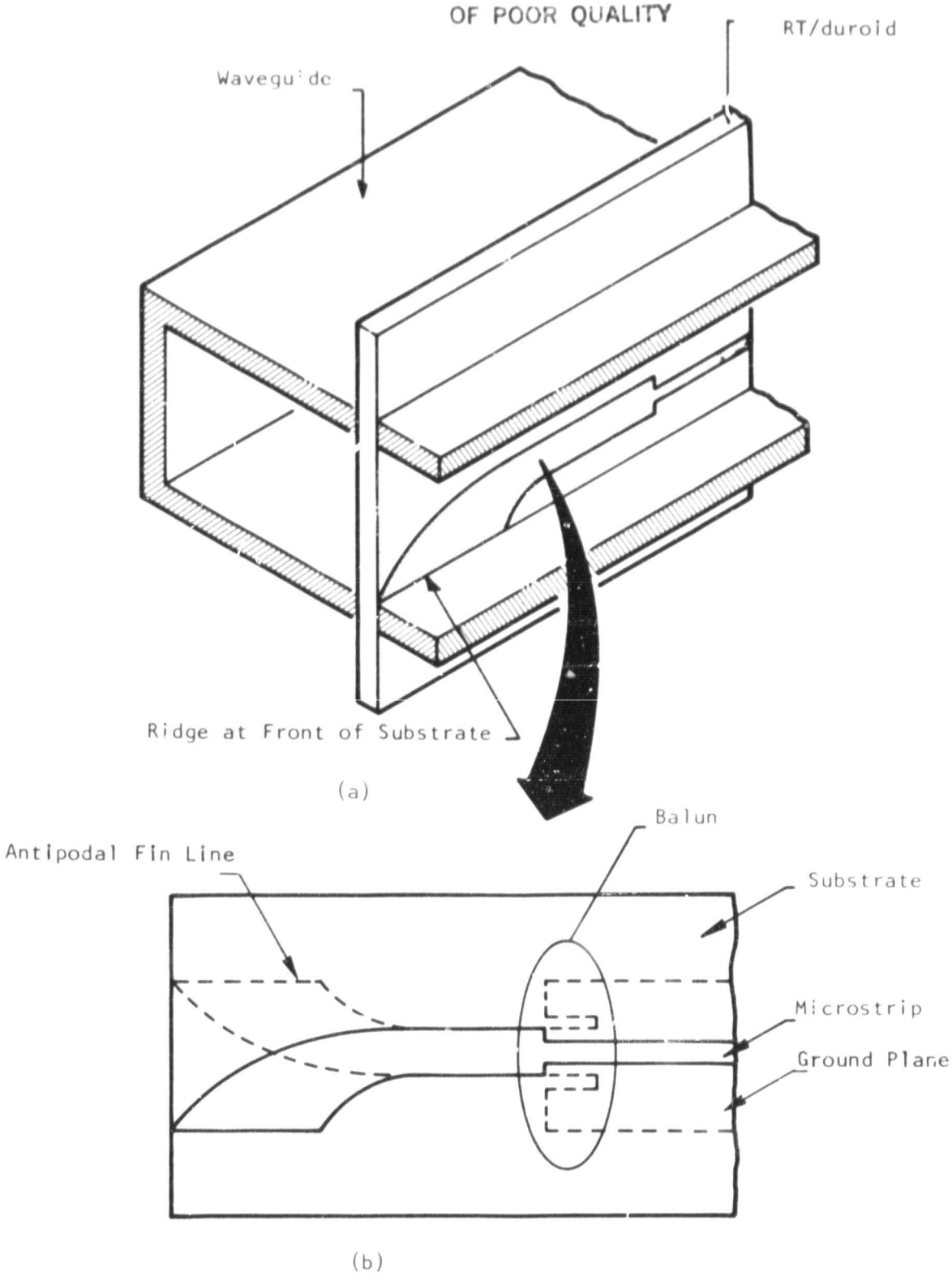


Figure 8 A Low-Loss Transition from Waveguide to Microstrip
(a) Outline of the substrate inserted in the waveguide.
(b) Position of the planar circuit in the waveguide.

Preliminary tests were run on the waveguide-to-microstrip transition test st ucture, shown in Figure 9, with quartz as a dielectric. The initial evaluation demonstrated that the approximate dimensions proposed by van Heuven were suitable starting values. Over the 18.5 to 19.5 GHz band, two transitions back-to-back had 2 to 5 dB insertion loss. Optimization focused on the evaluation of the balun section; a minor alteration in line width in the balanced section and a more gradual taper in the fin-line portion were introduced. A transition was then designed and fabricated on 0.25 mm thick RT/duroid. Good electrical contact of the waveguide to the circuit could be made with mechanical pressure without the risk of substrate breakage as with the case of fused quartz. Significant improvement was demonstrated. After minor tuning on the fin portion of the transition circuit, the performances shown in Figure 10 were observed. Insertion loss is less than 0.5 dB for the two transitions across the 17.7 to 20.2 GHz band. Return loss is limited by the characteristics of the commercial WR-62 to WR-51 waveguide transition. Several circuits were fabricated and repeatable performances were demonstrated.

D. Mechanical Design

Mechanical components of the amplifier consist of sixteen amplifier modules, two waveguide 16 way combining manifolds, and a thermal conduction system. A summary of the relevant mechanical data is shown in Table 1(a). Table 1(b) lists the thermal design constraints.

1. Module Amplifier

Figures 11 and 12 show details of the 31 dB module amplifier. The carrier blocks are housed entirely within the opening of a WR-51 waveguide. The cutaway view of the module (Figure 12) shows the location of the copper carrier blocks and the microstrip-to-waveguide transition. The module length, including the waveguide flanges, is 11.8 cm (4.6 in.).

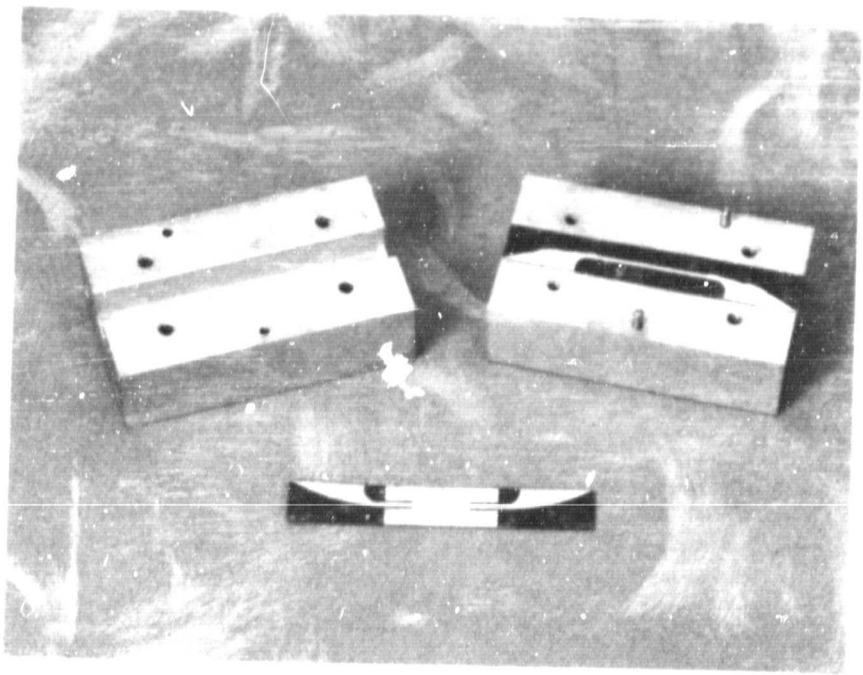
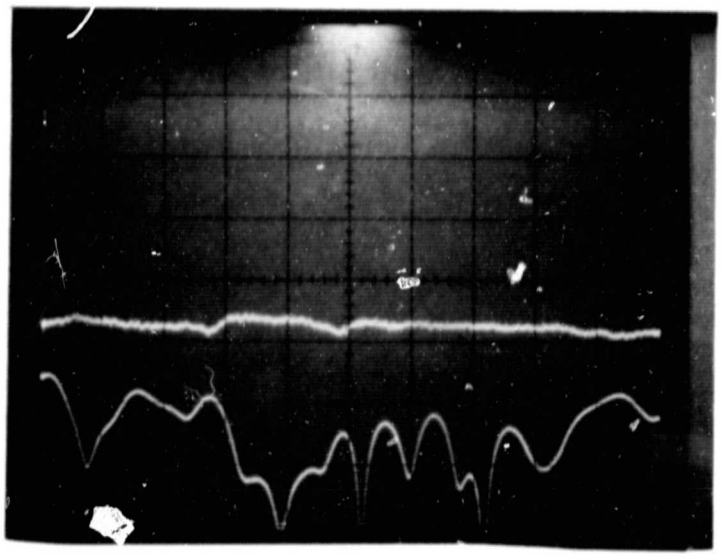


Figure 9 Waveguide-to-Microstrip Transition
Test Fixture and Test Circuit



Vertical: 0.5 dB/div for Insertion Loss (Upper Trace)
Reference: Center Graticule Line
10 dB/div for Return Loss (Lower Trace)
Reference: Center Graticule Line
Horizontal: 250 MHz/div; 17.7 to 20.2 GHz

Figure 10 Frequency Response of Transition Test Circuit
(Two Transitions Back-to-Back)

Table 1(a)

20 GHz Amplifier Assembly Mechanical Data

Assembly Components

Amplifier Module (16)

Manifold (2)

Thermal Conduction System

rf Interface

Input - WR-51 Waveguide

Output - WR-51 Waveguide

dc Power Interface

MS Type Connector

Mounting

Interface surface to be used for mounting as well as heat transfer

Size

8.75 in. x 8.25 in. x 6.96 in.

These are maximum dimensions

Volume 502 $in.^3$ (max)

Table 1(b)

Thermal Characteristics

Total power dissipated per module	4.6 W Max
Device/mounting block interface temperature	100°C Max
Heat sink temperature range	0 - 75°C
Maximum temperature difference between any two modules	10°C

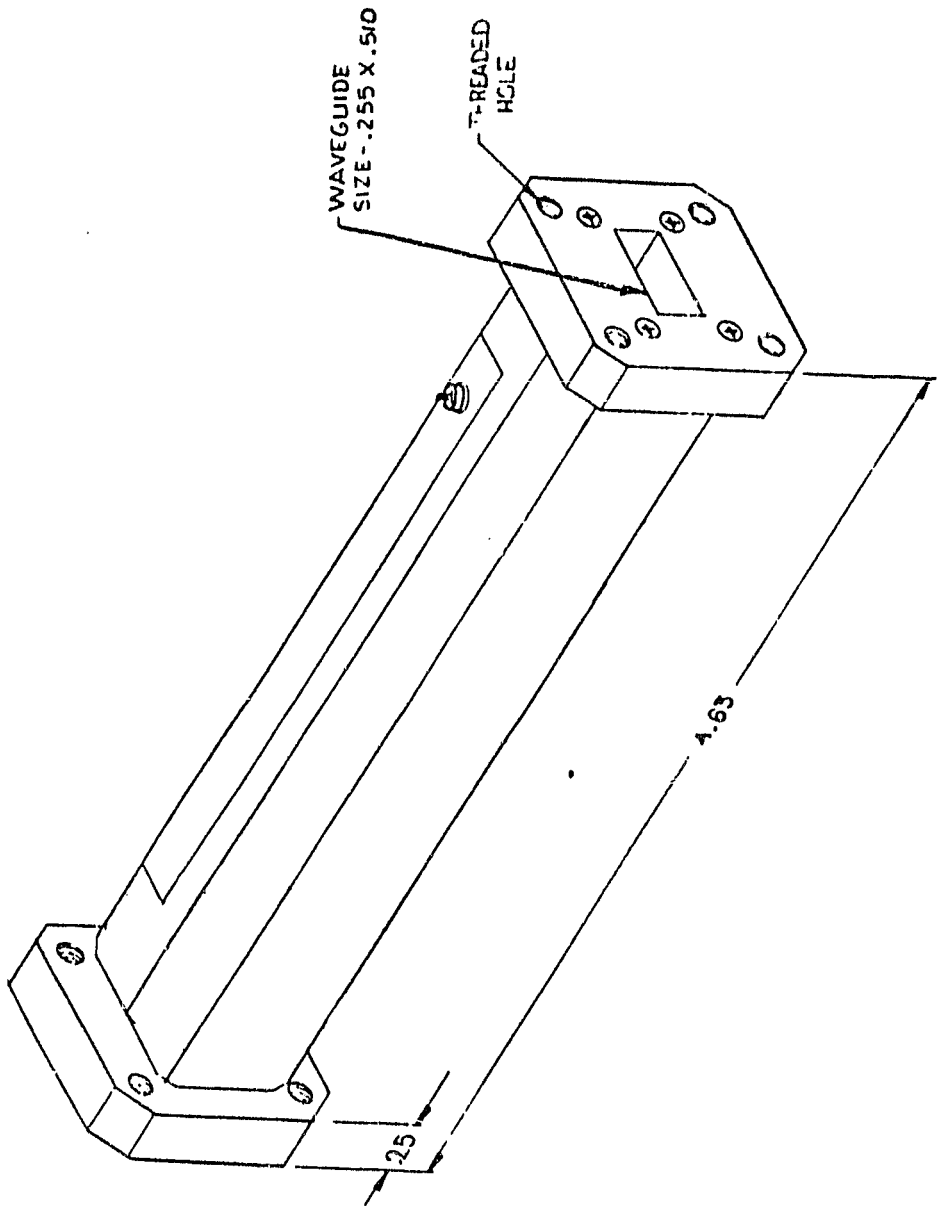
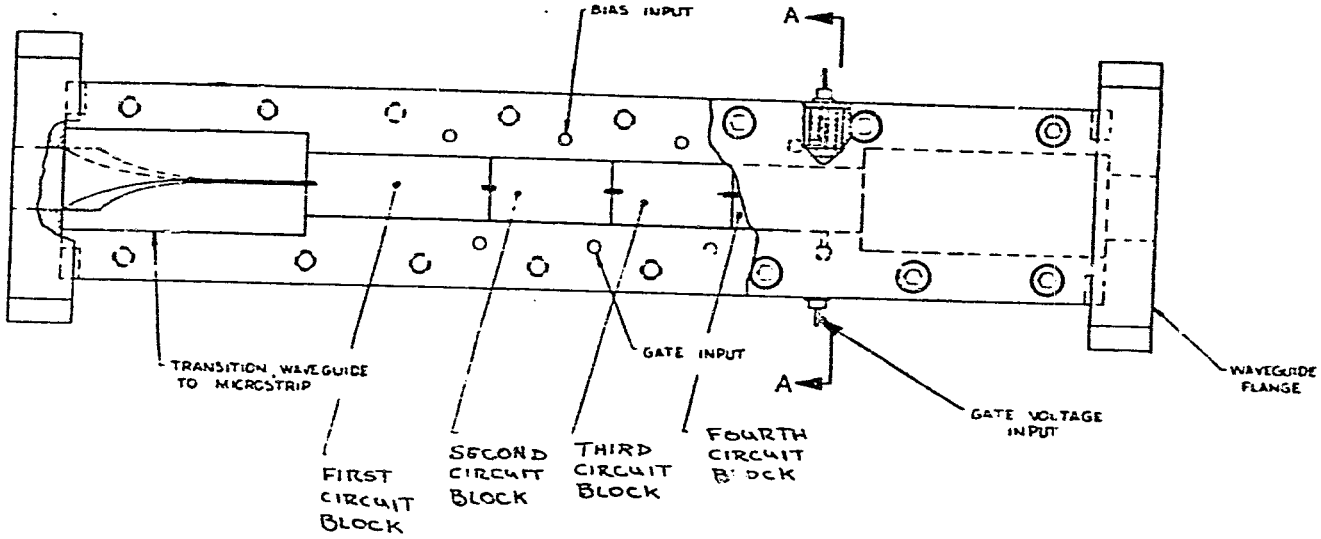
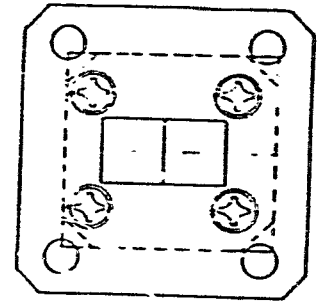
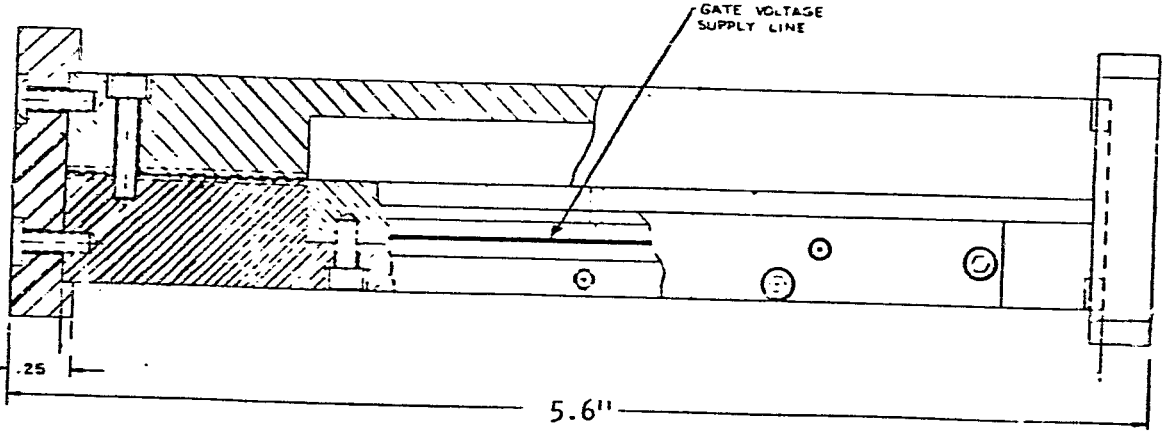


Figure 11 Amplifier Module Configuration







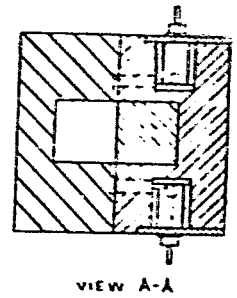


Figure 12 Amplifier Module Assembly

2. Thermal Conduction System

Two configurations for amplifier assembly were investigated, the differences being the manner in which thermal energy is removed from the modules and in the external heat sink interface. Each configuration was designed to have thermal energy conduction path cross-sectional areas such that the variance in temperature of all the modules would not exceed 10°C and internal device temperature would not exceed 100°C with a 75°C heat sink temperature.

One configuration uses two heat sink interface plates. Half the modules are attached to each plate, which minimizes the conductive path length between the modules and the heat sink interface plates. It also reduces the amount of heat to be transferred to an external heat sink from each interface attachment surface. Figure 13 shows this design option.

The second configuration (Figure 14) has a single interface surface to the external heat sink. This configuration requires larger cross-sectional areas to conduct the thermal energy due to the larger lengths from same modules to the heat sink interface plate. Although this design carries a slight weight penalty, only a single external heat sink is required.

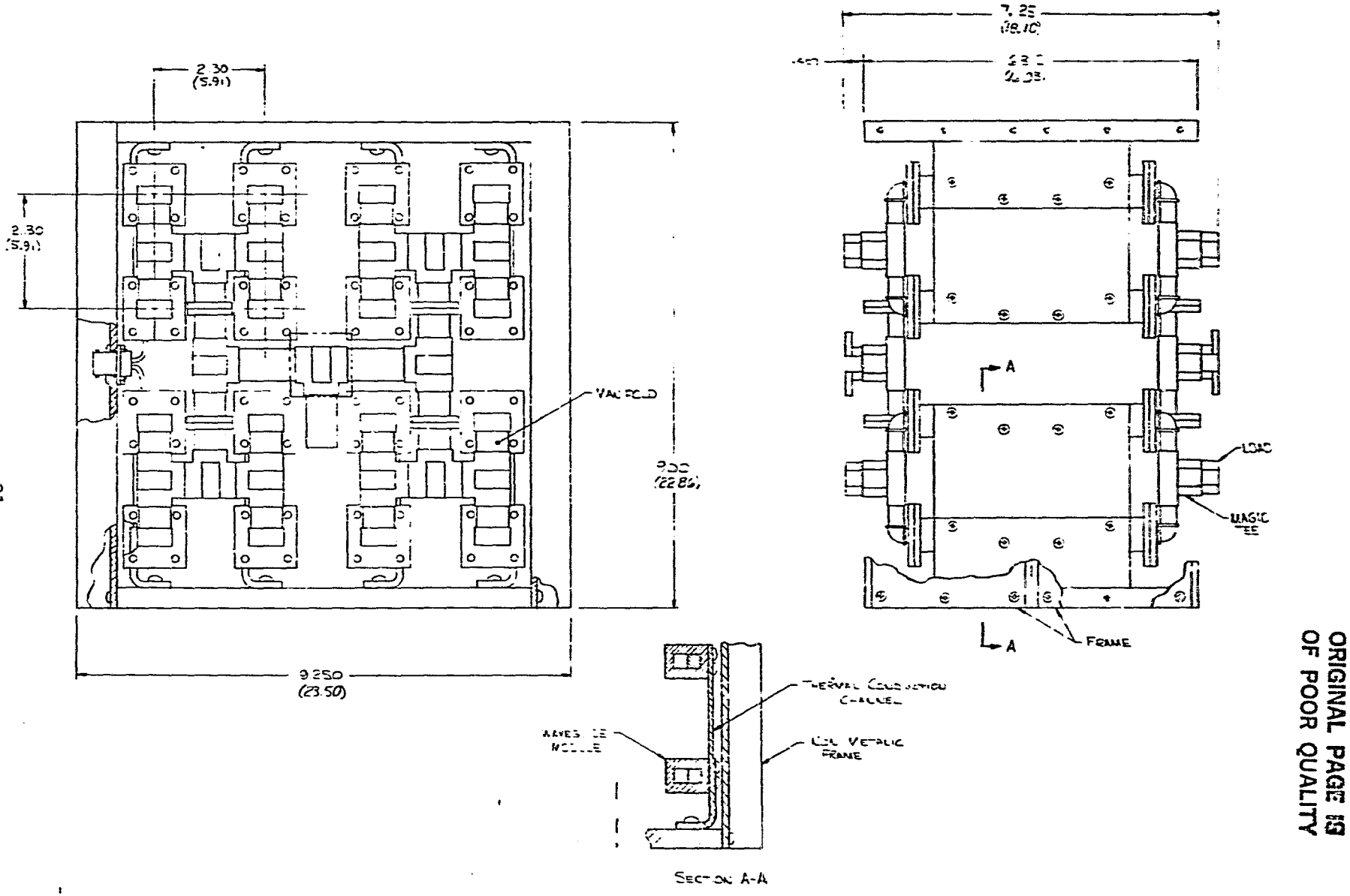


Figure 13 20 GHz Amplifier Assembly Dual Heat Sink Configuration

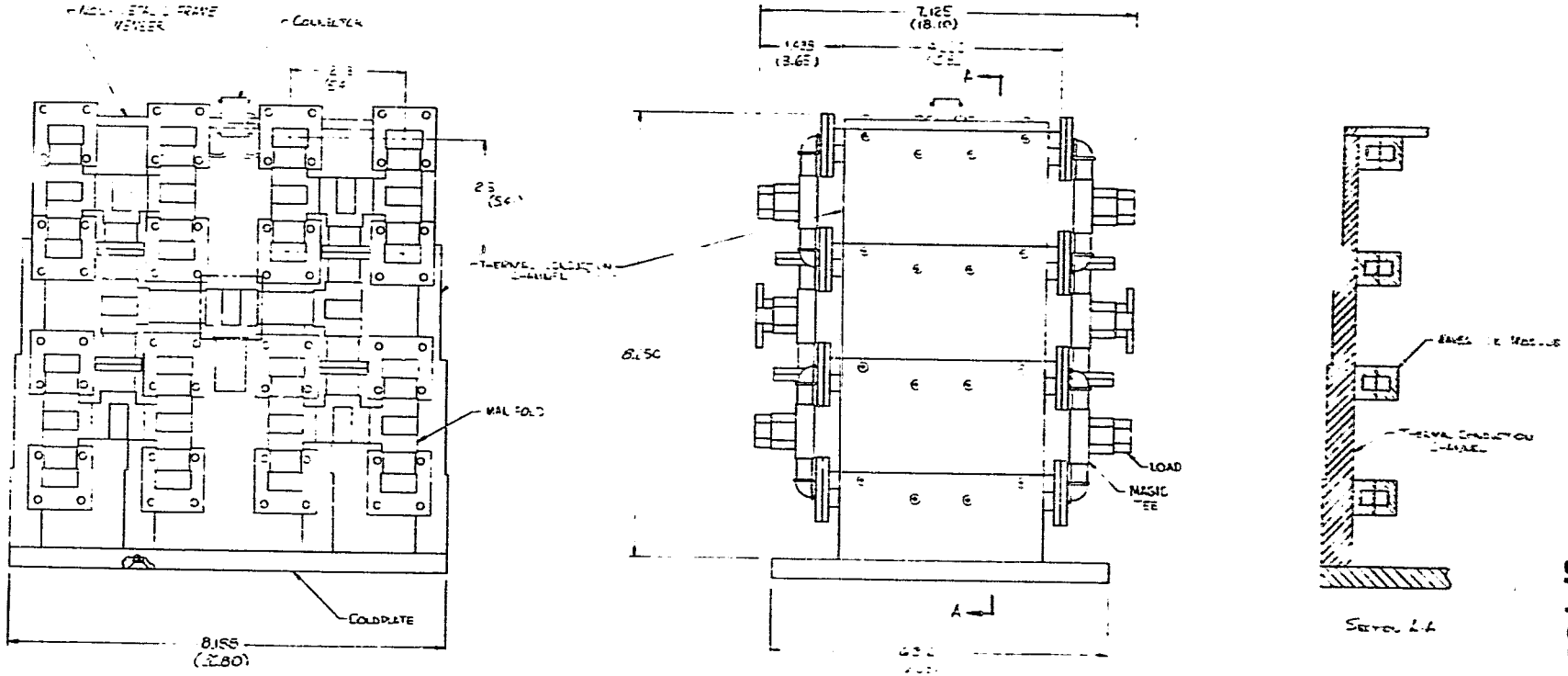


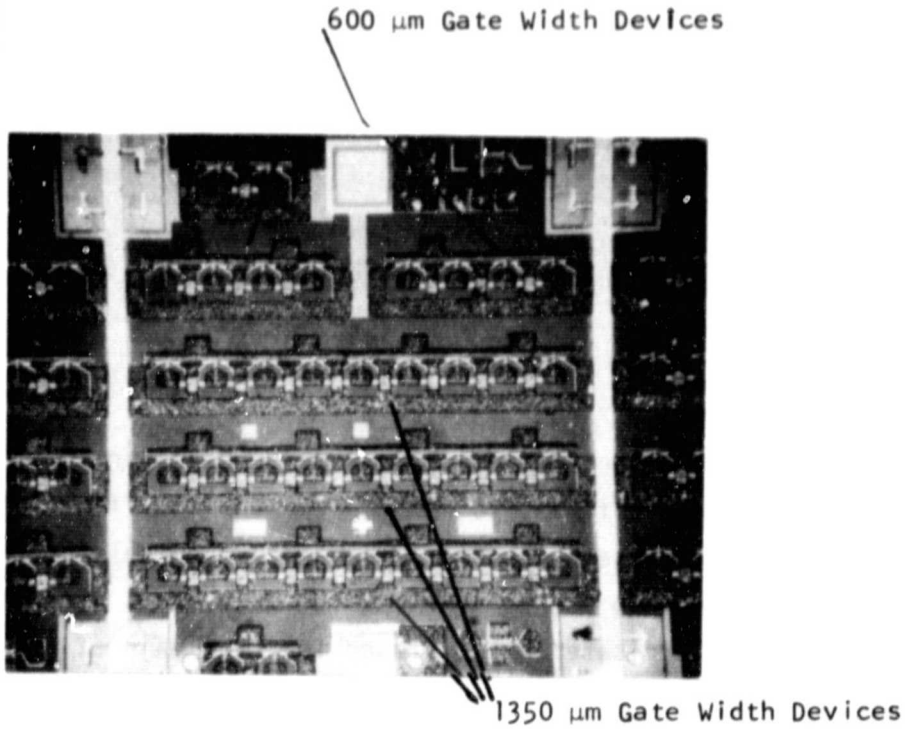
Figure 14 20 GHz Amplifier Assembly Single Surface Heat Sink Configuration

SECTION III
FET DESIGN

A. Power Devices

Several types of devices have been studied for this project. At the time the proposal was written, it was thought that the final stage device would have multiple parallel gate fingers. These devices would have 2400 μm gate width and a via etched to each source pad for grounding. The photomasks for the devices were fabricated but we found that the gain of via devices was not as high as expected.

During the contract period a new device (the π-gate device) was designed and tested by TI. The best devices from the design had significantly better microwave performance than the best of many device processing runs with the multiple parallel gate design. As is described in Section D.1, the amplifier module was designed with the new devices. Figure 15 shows two photographs of a slice during processing. The devices have a single long gate strip with multiple gate pads. The slice has 1.35 mm, 0.6 mm, and 0.3 mm gate width devices with nine, four, and two gate pads respectively. A single chip (1.35 mm gate width) is 0.3 mm x 1.5 mm x 0.1 mm thick and has a large source grounding bar extending the length of the chip on one side. The sources are connected to the source grounding bar by plated gold air bridges. The multiple gate pads are interconnected by metallization on the chip. Figure 16(a) and 16(b) show a 1350 μm and 600 μm device. The high gain of the π-gate devices can be attributed to several factors. The better isolation results from lower source lead inductance and lower gate-drain feedback capacitance. The latter is caused by smaller pads, coupled with the pads being spread out. It is thought that performance is also improved by more symmetric feeding of the gates. Another advantage of this structure for high frequency operation is that with the large number of widely spaced gate and drain bond wires, the inductance can be very low and the device input capacitance can be resonated at very high frequencies with the bond wires. The best microwave results with these devices are 675 mW



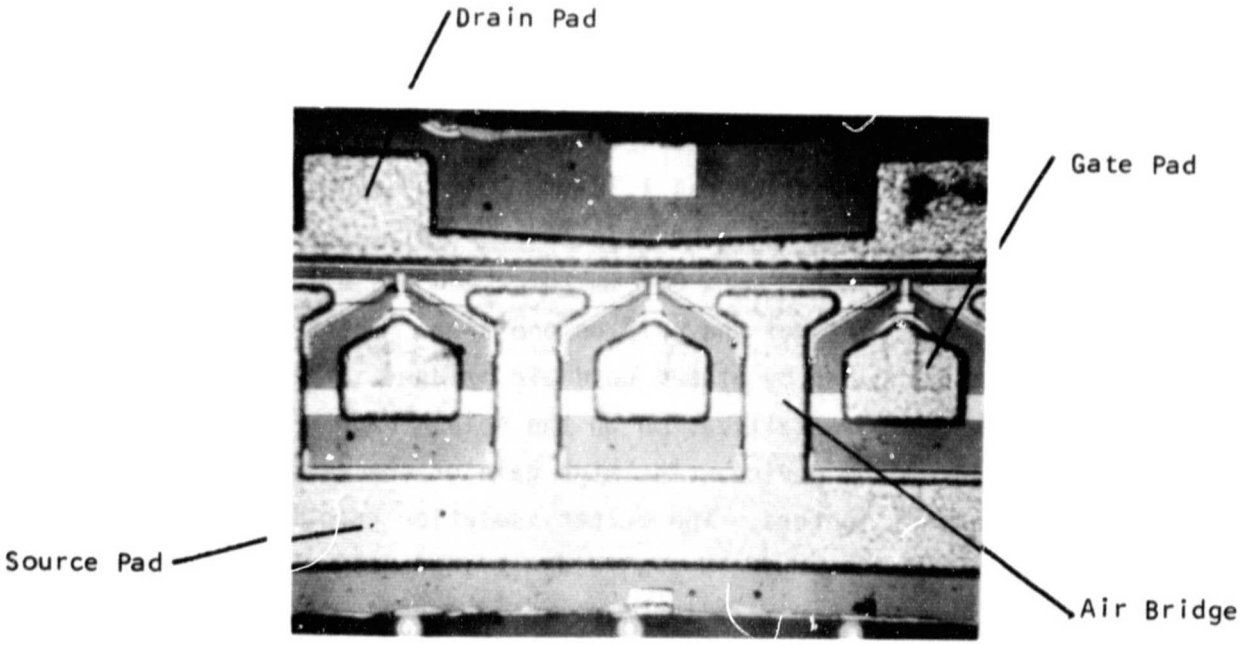
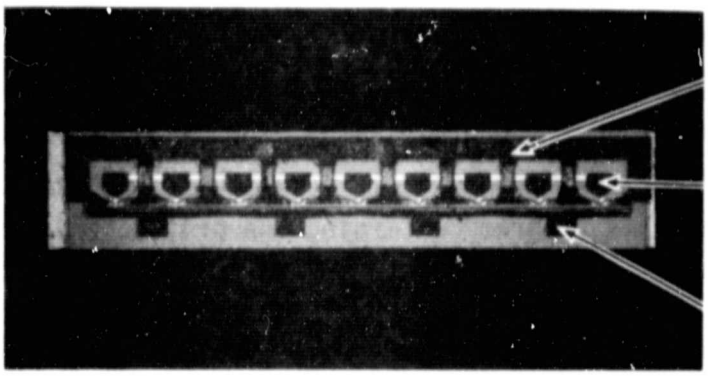


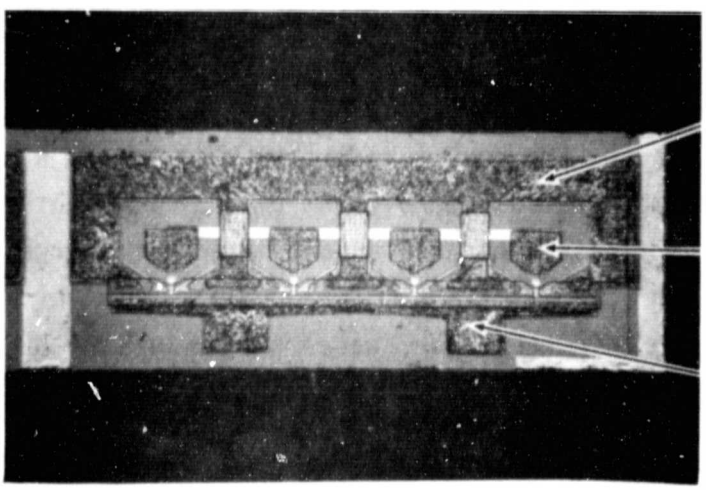
Figure 15 π - Gate Devices During Fabrication



Chip Dimensions

1.5×0.3 mm^2

Figure 16(a) 1350 μm Gate Width FET



Chip Dimensions

0.76×0.3 mm^2

Figure 16(b) 600 μm Gate Width FET

with 5.8 dB gain at 20.5 GHz from a 1.35 mm device and 1 W with 4 dB gain at 19.7 GHz from two 1.35 mm devices mounted side-by-side. Two other mask sets for 900 μm and 1800 μm π-gate devices were also available. Considerable insight was gained during this program concerning the critical parameters of power devices.

Doping level

Extensive experiments showed that optimum doping level for operation at 20 GHz was 2.3 to 2.5 x 10^{17}. Higher doping gives too small a gate-drain breakdown and saturated output power is consequently lower. A lower doping level tends to yield lower gain.

Source resistance and source drain spacing

The source to drain resistance (which includes the source and drain contact resistance plus the channel resistance) is a parasitic element of the FET. Values as small as possible are desirable for maximum gain. Our initial design had a 5 μm source drain spacing for easy e-beam gate alignment. When a 3 μm source drain spacing was implemented, improvement of ≈ 1 dB in saturated output power was observed. These findings were later confirmed by a large signal model developed under another contract. An increase in the value of the source resistance of a 1350 μm from 1 Ω to 2 Ω decreases the power at 1 dB compression by ≈ 0.6 dB

Influence of the gate recess shape

The width of the gate recess was found to be critical to the saturated output power. A gate recess wider than the gate metal [as shown in Figure 17(a)] gives a large small signal gain but a small output power (1.5 dB under maximal value). A recess only slightly wider than the gate metal gives maximum saturated power [see Figure 17(c)].

(a) Device with High Output Power

(b) Device with Moderate Output Power

(c) Device with Low Output Power

Figure 17 Device SEM Photographs

Since a large data base was available for device performance at 15 GHz all slices were first evaluated at this frequency.

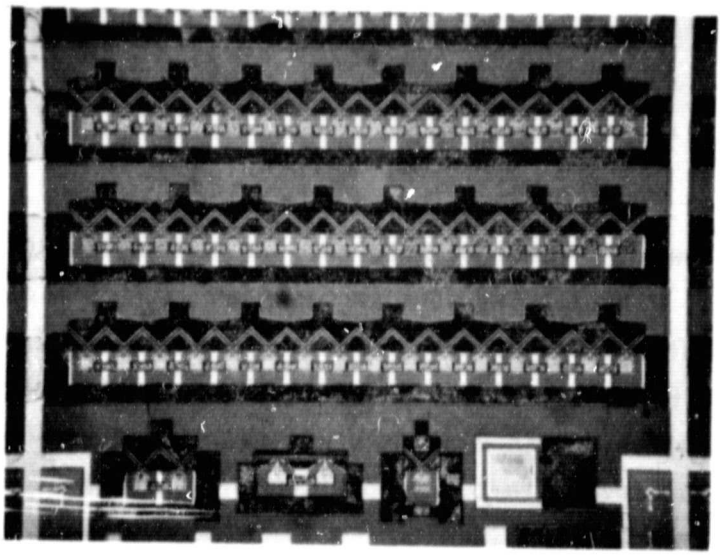
Performance for a good 600 μm device is:

small signal gain V_{ds} = 5 V P_{in} = 8 dBm	9.5 to 10.5 dB
output power with 6 dB gain	26 dBm
output power with 4 dB gain	26.5 dBm

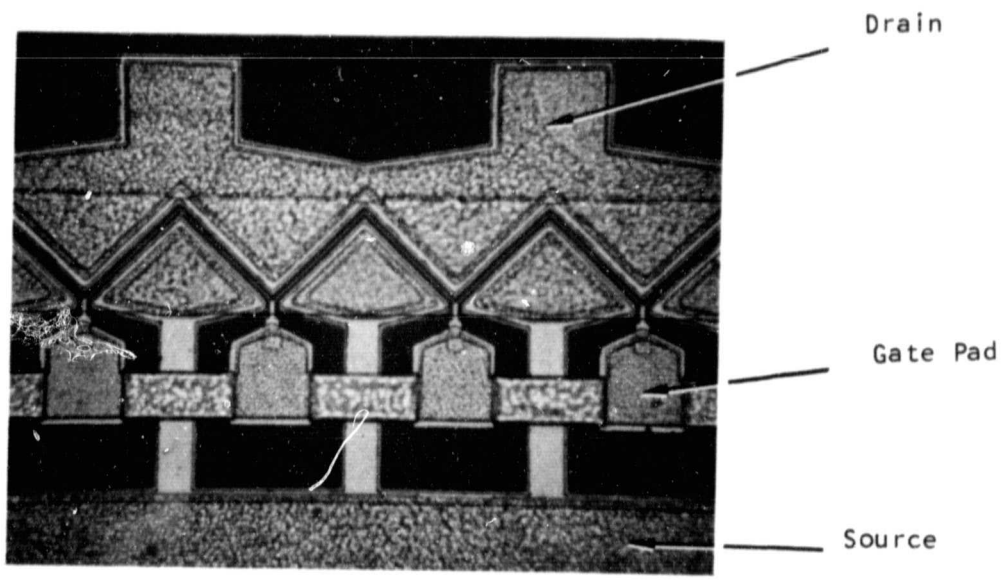
For the best 1350 μm gate width device the following performance has been achieved:

Frequency	Gain	Output Power
15 GHz	6 dB	29.6 dBm
	5 dB	30.0 dBm
18 GHz	5 dB	28.7 dBm
	4 dB	29.5 dBm

An extension of the π-gate device design was studied during the program. The chip has approximately twice the gate width (2500 μm). This is accomplished by increasing the chip size to 2 mm and orienting the gates at an angle so the gate stripe appears to zigzag down the chip. Figure 18 shows the device as it appears on the slice. Figure 18(a) shows test structures that include a 300 μm



(a)



(b)

Figure 18 Photographs of Zig-Zag Gate Devices During Fabrication

gate width FET with a straight gate and the corresponding device using the zigzag design. Difficulties were encountered with this device. The zigzag gate is difficult to define with e-beam. Also the impedance level at 20 GHz is very low (1.5 to 2 Ω) and matching to 50 Ω at this frequency is difficult. Although 1.4 W with 4 dB gain was obtained at 15 GHz, the approach using a single 2500 μm device in the output stage was abandoned.

At the conclusion of the program TI had available a molecular beam epitaxy (MBE) machine that was used to grow FET structures. A 1 μm undoped buffer layer was deposited, followed by a 0.3 μm nGaAs active layer doped to 2.5×10^{17} cm^{-3} with Si and a 0.1 μm n^+ GaAs contact layer doped to 4×10^{18} cm^{-3} with Sn. The 1350 μm π-gate devices were fabricated with the standard processing technique. However, after source-drain alloying, a first 2 μm wide stripe was defined by e-beam lithography in the center of the 5 μm source-drain spacing. A recess was wet etched in the n^+ and n layers until the current reached 700 mA/mm gate width (see Figure 19). The 0.5 μm gate was defined in the center of the first recess in a second e-beam exposure step. A second recess step brought the current down to 500 to 550 mA/mm gate width. The devices had a pinch-off voltage of 3.0 to 3.5 V and a transconductance of 165 mS/mm gate width. Figure 29 shows the I-V characteristics of a 560 μm gate width device.

These devices had the best performance we have ever observed. At 19.3 GHz a 1350 μm device was capable of producing 900 mW output power with 4.5 dB gain and 21.3% power-added efficiency. At 21 GHz these figures were 710 mW with 4.5 dB and 17% power-added efficiency. Table 2 summarizes the performance at 19.3 GHz and 21 GHz. The 600 μm devices were also tested. A power-added efficiency of 26.6% was obtained at 21 GHz with an output power of 316 mW and 5 dB gain. Other results at 21 GHz and 22 GHz are summarized in Table 3. These devices were used in the final delivered amplifier.

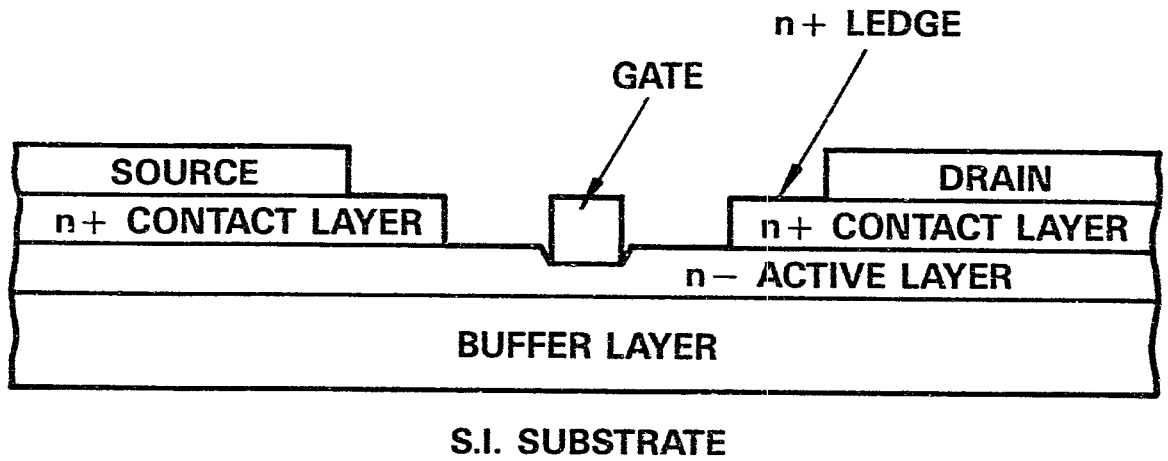


Figure 19 n^+-Ledge Channel Structure

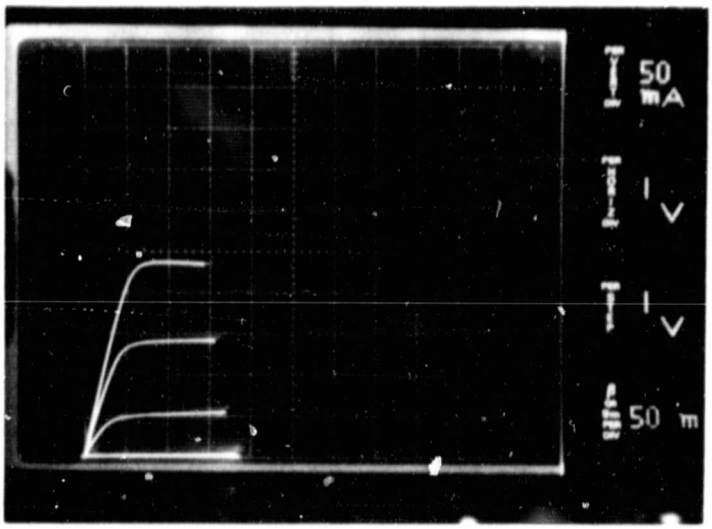


Figure 20 -V Characteristics of a 560 μm Gate Width Device

Table 2

Performance of a MBE 1350 μm FET

Frequency	Output power	Gain	Power-added efficiency
19.3 GHz	900 mW	4.5 dB	21.3%
19.3 GHz	800 mW	5.0 dB	19.3%
19.3 GHz	710 mW	5.5 dB	21.7%
21.0 GHz	710 mW	4.5 dB	17.0%
21.0 GHz	630 mW	5.0 dB	18.3%
21.0 GHz	560 mW	5.5 dB	17.7%

Table 3

Performance of a MBE 560 μm FET

Frequency	Output power	Gain	Power-added efficiency
21.0 GHz	316 mW	5.0 dB	26.6%
21.0 GHz	280 mW	5.5 dB	16.8%
21.0 GHz	140 mW	8.5 dB	9.0%
22.0 GHz	224 mW	5.5 dB	16.0%
22.0 GHz	252 mW	5.0 dB	13.6%
22.0 GHz	281 mW	4.0 dB	17.4%

On-chip matched FET

To eliminate the need to rely on a discrete L-C-L lumped element matching network where the critical inductance from the gate to the capacitor is provided by bond wires, an 1800 μm π-gate device with an integrated on-chip matching network was designed. The circuit described in detail in Section IV, brings the low input impedance of the FET to a nominal 12.5 Ω for broadband matching. The FET, with a chip size of 2 x 1.4 mm^2, is shown in Figure 21(a). A large bonding pad on the 50 μm thick substrate is used to provide a 1 pF capacitance to ground. Twelve 5 μm wide and 1 mm long microstrip lines connect each gate feed to the bonding pad. The front surface processing is conventional. The microstrip lines and bonding pads are gold plated to a 3 μm thickness. The wafer is ground to 6 mils, mounted on a sapphire disk and thinned down to 50 μm by rotary etch. The 50 x 50 μm^2 holes are aligned with an IR aligner. Reactive ion etching is used to achieve high aspect ratio of the vias. Ti/Au is evaporated and 50 μm thick gold is plated on the heat sink. The devices are then sawed. Figure 21(b) shows the back surface of a chip with the clearly visible 13 source vias. When narrow band tuning was performed on the drain side, the device was capable of ~ 1 W output power at 17 GHz with 5 dB gain and 18% power-added efficiency. With the output tuned for broadband operation, 630 mW was achieved with 4 dB gain from 17 to 20.5 GHz.

Small signal devices

A mask set to produce 150 μm and 300 μm gate width devices was designed. Each 2 x 2 mm^2 field contains eleven 300 μm devices and eighteen 150 μm devices plus test patterns for contact resistance measurement and doping profiling (see Figure 22). The 150 μm device is the conventional type (see Figure 23) with two 75 μm wide gate strips, the drain is 50 μm wide and the gate pads are 100 μm wide for easy bonding. The source-drain spacing is 5 μm. An air bridge is not used to connect the source. The 300 μm device is of the π-type. Two

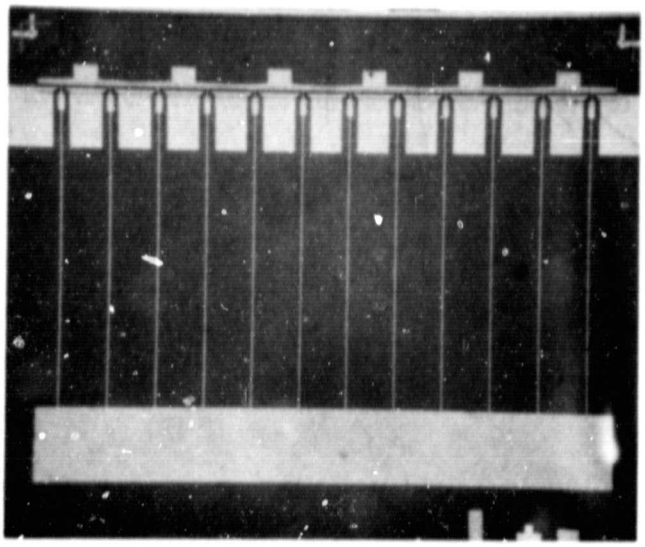


Figure 21(a) 1800 μm with On-Chip Matching Network
Front Surface

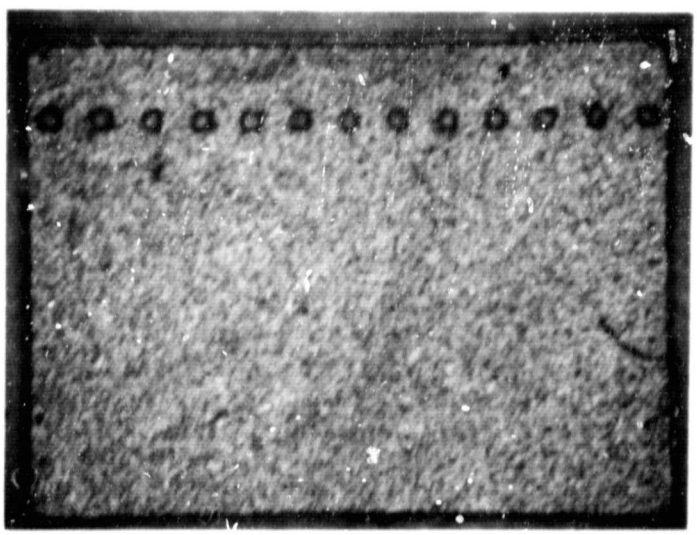


Figure 21(b) 1800 μm with On-Chip Matching Network
Back Surface

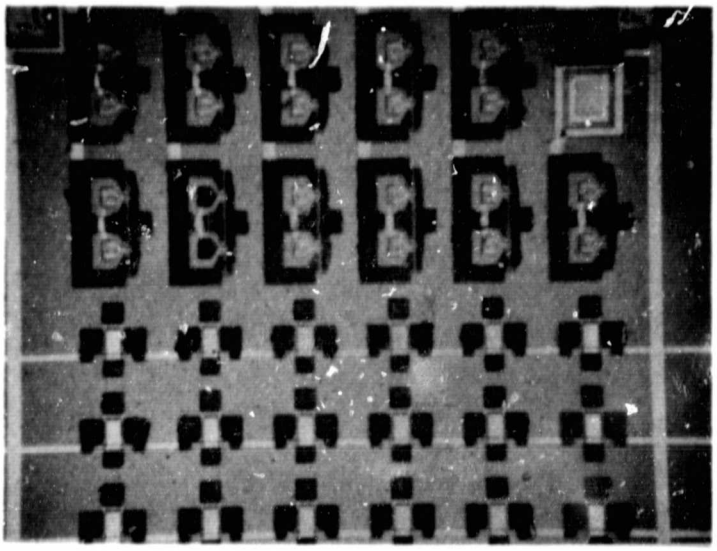


Figure 22 One e-Beam Field of 150 μm and 300 μm Gate Width Devices

Chip Size 208 µm x 236 µm

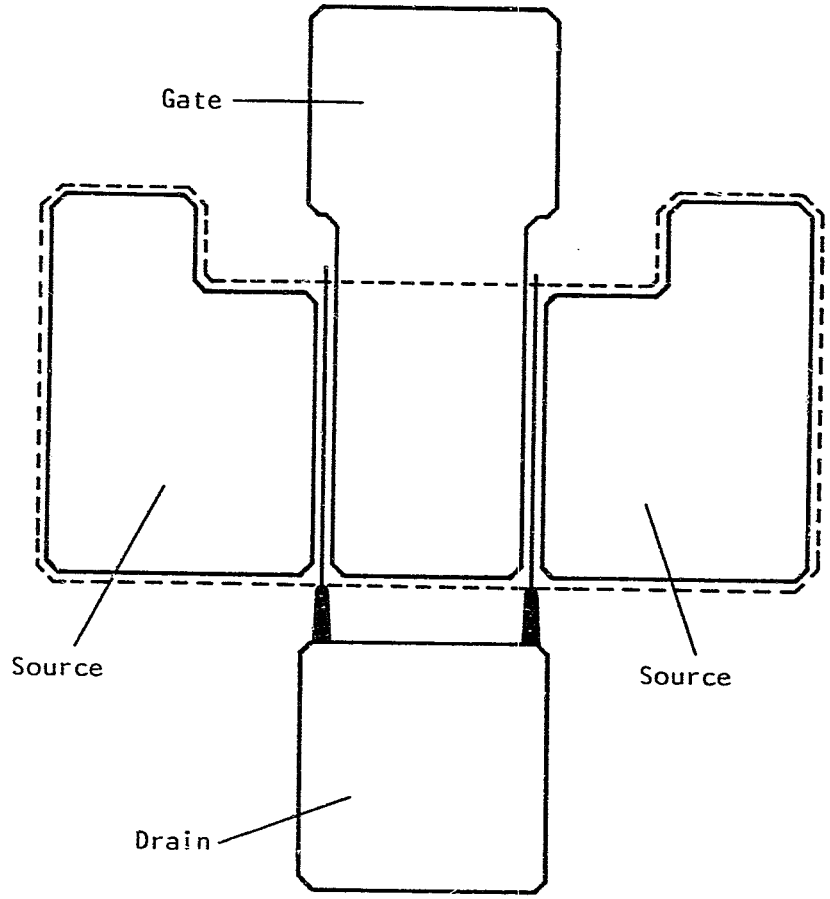


Figure 23 150 µm Gate Width Device

requirements had to be met in the design of the mask; for best e-beam stripe definition all the gates have to be parallel, and they must step over the mesa in the same direction. Therefore, the mesa of the 300 μm device is formed of three islands and the gate runs, as indicated on Figure 24. Amplifier results using these devices are presented in Section IV. The best performances at 15 GHz are:

Small Signal	Output Power	Output Power
V_{DS} = 5 V	a· 6 dB gain	at 4 dB gain
10.1 to 10.7 dB	23 to 23.4 dBm	23.5 to 24 dBm

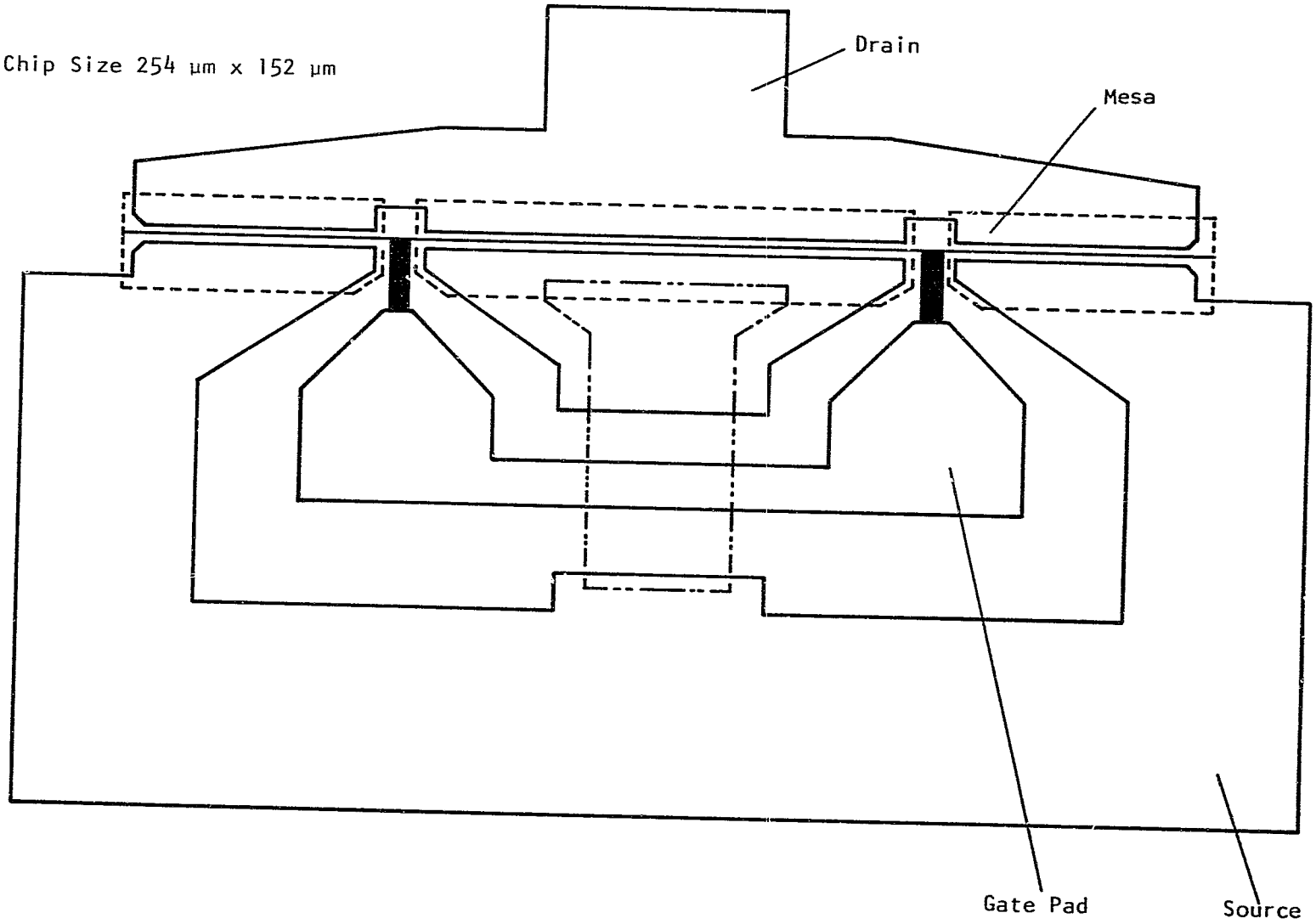


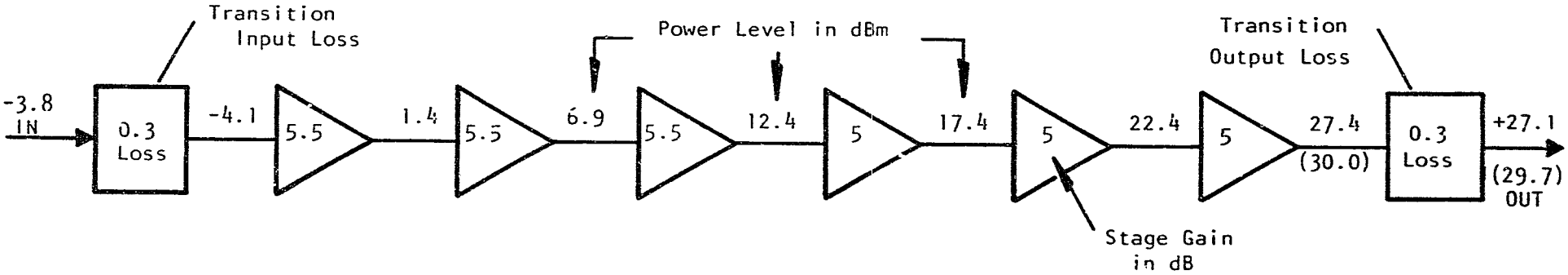
Figure 24 300 µm Gate Width Device

SECTION IV
MODULE DESIGN DEVELOPMENT

The initial block diagram of the 31 dB amplifier module is shown in Figure 25. The first three stages are 150 μm gate width devices. The 600 μm device of the fifth stage drives the 2 x 1350 μm device of the last stage. A typical carrier block with microstrip impedance matching circuit is shown in Figure 26. The length of the different carriers is noted.

Amplifier circuit design was accomplished with scattering matrix parameters that were generated from device equivalent circuit models. These lumped element models were derived from rf characterization data measured on an automatic network analyzer over the 2 to 18 GHz band of frequency. In addition, slotted line measurements were made at selected frequencies to confirm the accuracy of the ANA data. Figure 27 shows a typical example of the equivalent circuit model for a 600 μm gate width FET.

The amplifiers are first designed on a single stage basis, assuming an ideal 50 Ω generator and load, using a computer optimization routine that is commercially available. Once acceptable results are obtained the modeled stages are then cascaded and further selected optimization is performed to obtain the desired characteristics for the multistage amplifier. Once an acceptable design is obtained a first pass evaluation prototype circuit is fabricated for the various stages. The circuits are then evaluated on the bench under actual operating conditions and compared to the circuit model predictions. Seldom do the evaluation circuits give the exact computer predicted performance, especially at the higher frequencies. This is caused primarily by circuit parasitics and variations in device characteristics that have not been included in the model. As a result several iterations are usually performed to obtain a reproducible circuit.

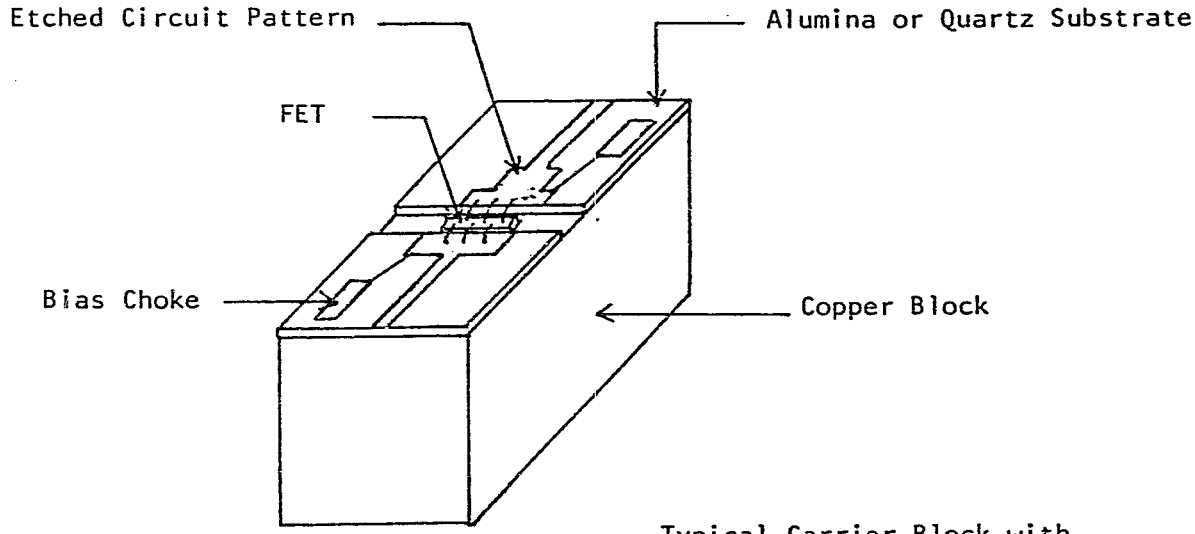


Gain Stage	1	2	3	4	5	6
evice Gate Width (μm)	150	150	150	300	600	2500
evice Current (mA)	30	30	30	60	120	500
evice Voltage (V)	6.0 (8.0)	6.0 (8.0)	6.0 (8.0)	6.0 (8.0)	6.0 (8.0)	6.0 (8.0)
tage Efficiency (%)	0.55	1.9	6.9	10.4	16.5	12.5 (17)

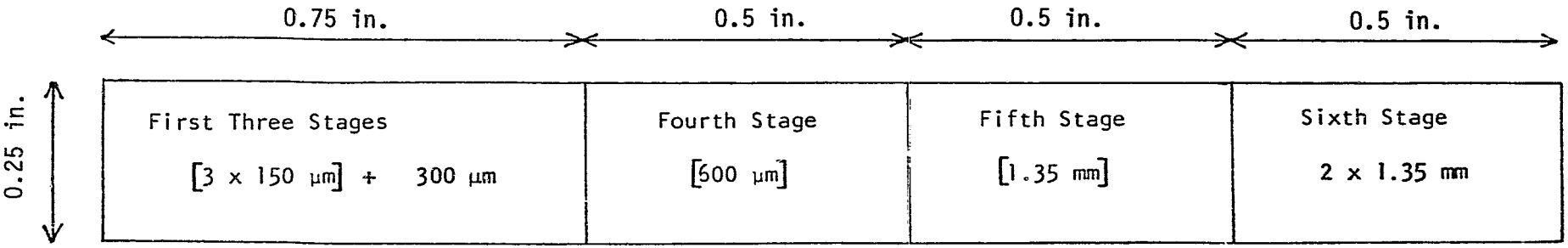
Total Module Gain - 30.9 dB
Module Output Power - 513 mW
DC Input Power - 4.62 W (6.2 W)
Module Efficiency - 11% (15%)

Figure 25 Block Diagram of 31 dB Amplifier Module Including Bias Schedule

Note: Numbers in parenthesis are relevant to power saturated operation.



Typical Carrier Block with
Microstrip Impedance Matching
Circuit



Length of Four Blocks - 2.25 in.
Transition Length - ∿ 1.50 in. each
Total Module Length - ∿ 5.25 in.

Figure 26 FET Carrier Blocks

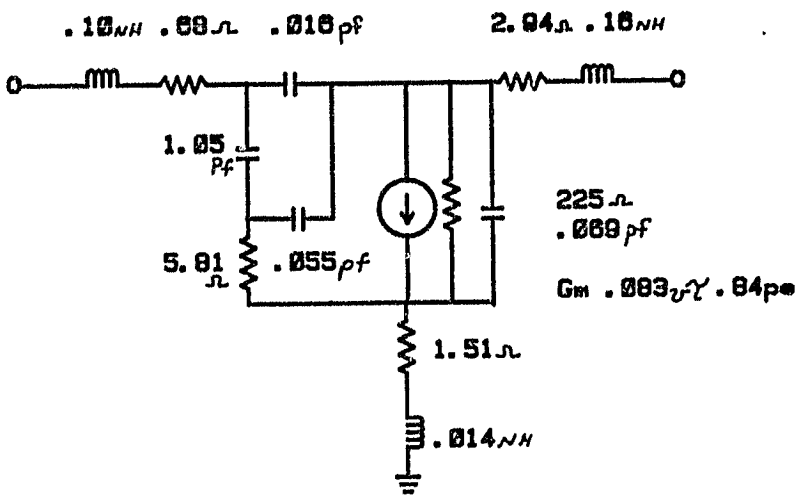


Figure 27 Equivalent Circuit Model for 600 μm FET

Impedance matching at input and output is accomplished using lumped and distributed circuit elements. The distributed components are etched on the alumina or quartz substrates, while lumped inductors and capacitors are realized with 25 μm diameter bond wire and discrete high dielectric chip capacitors, respectively. For example, in the sixth stage amplifier a pair of 1.35 mm gate width FETs is used. Figure 28 shows the circuit layout for the sixth stage amplifier, while Figure 29 shows the corresponding circuit schematic. The quartz substrates on which the microstrip distributed circuits, the discrete impedance matching capacitors, and the pair of 1.35 mm FETs are etched are mounted on a copper carrier block or package whose dimensions are 1.3 x 0.64 x 0.62 cm. Precise lengths of bond wires (25 μm diameter) interconnect these elements and are used as the lumped inductors in the impedance matching circuits. The in-package lumped and distributed impedance matching networks transform the 50 Ω input impedance to a level of about 2 or 3 Ω for each 1.35 mm FET. A single Wilkenson type combiner, less the isolation resistor, is used to power combine the two FET chips. Each half of the circuit between the 71 Ω lines of the Wilkenson power splitter/combiner combinations is simply the circuit used for the fifth stage amplifier where a single 1.35 mm gate width FET is used.

- The small signal gain characteristics for a 150 μm gate width FET amplifier from 17.7 to 20.2 GHz are shown in Figure 30. Typically 6 to 7 dB is obtained across the band.

- The small signal gain characteristics for a 300 μm FET amplifier with 5 to 6 dB gain across the band are shown in Figure 31.

In the initial design, the first three stages used 150 μm gate width devices and the fourth stage used a 300 μm gate width FET. Marginal performance was obtained for the overall bandwidth while the gain was acceptable. Figure 32 shows the 1 dB gain compression output over the frequency band of 17.7 to 20.2 GHz. This level is approximately 1.5 dB lower than the output

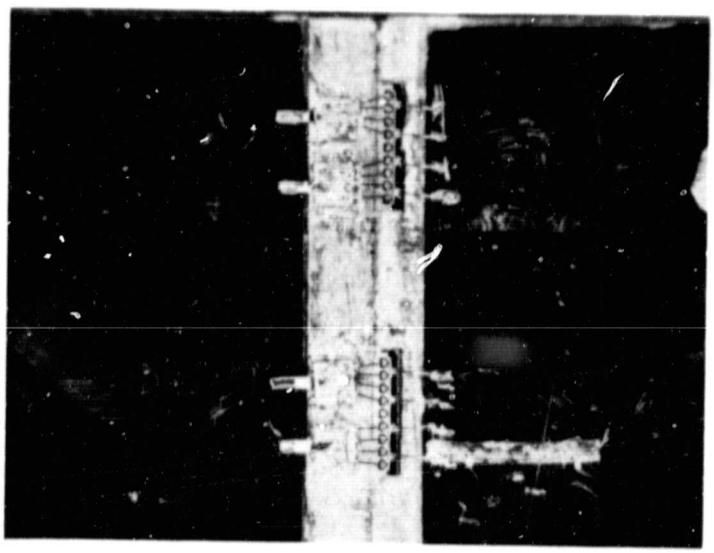
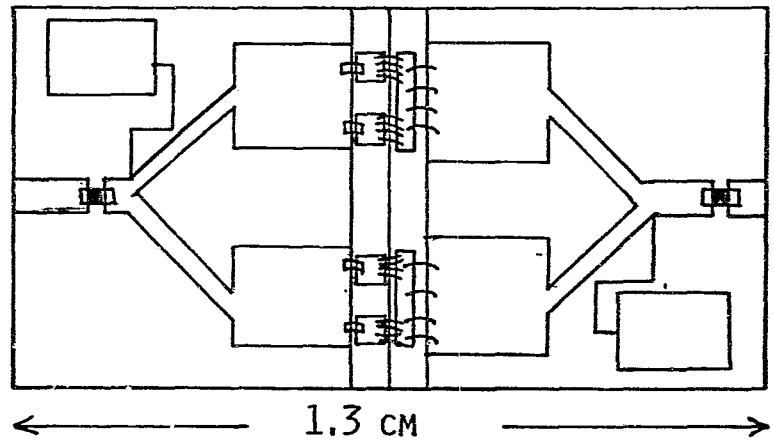
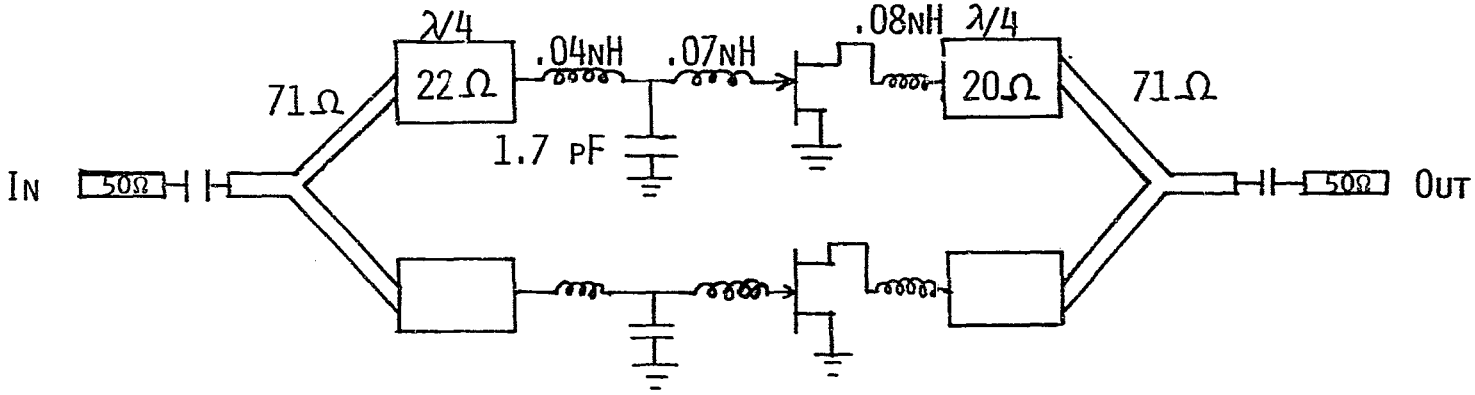


Figure 28 Sixth Stage Amplifier

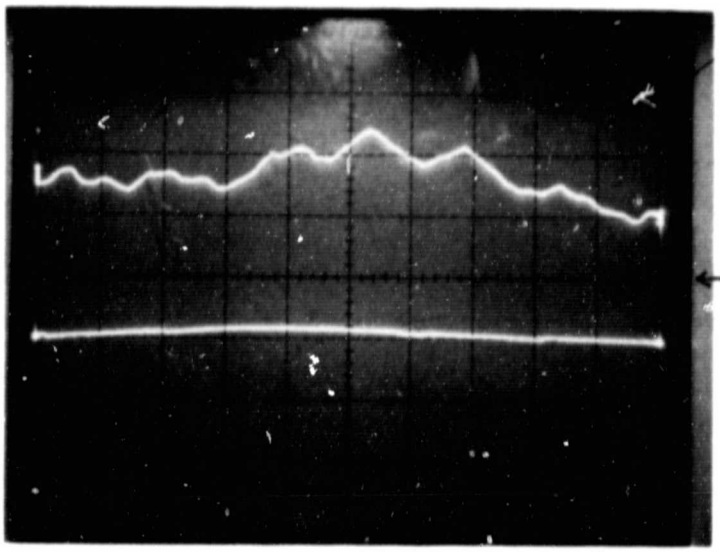


Physical Circuit



2 x 1.35 mm
FETs
Circuit Schematic

Figure 29 Sixth Stage Amplifier



Vertical: Top Trace (Gain): 1 dB/div
Lower Trace (Return Loss): 10 dB/div
Horizontal: 220 MHz/div, Range 17.7 to 20.2 GHz
Bias Conditions: V_d = 8 V; I_D = 30 mA; V_G = -1.0 V
Slice: 96IH

Figure 30 Small Signal Gain for a 150 μm Gate Width FET "Breadboard" Amplifier

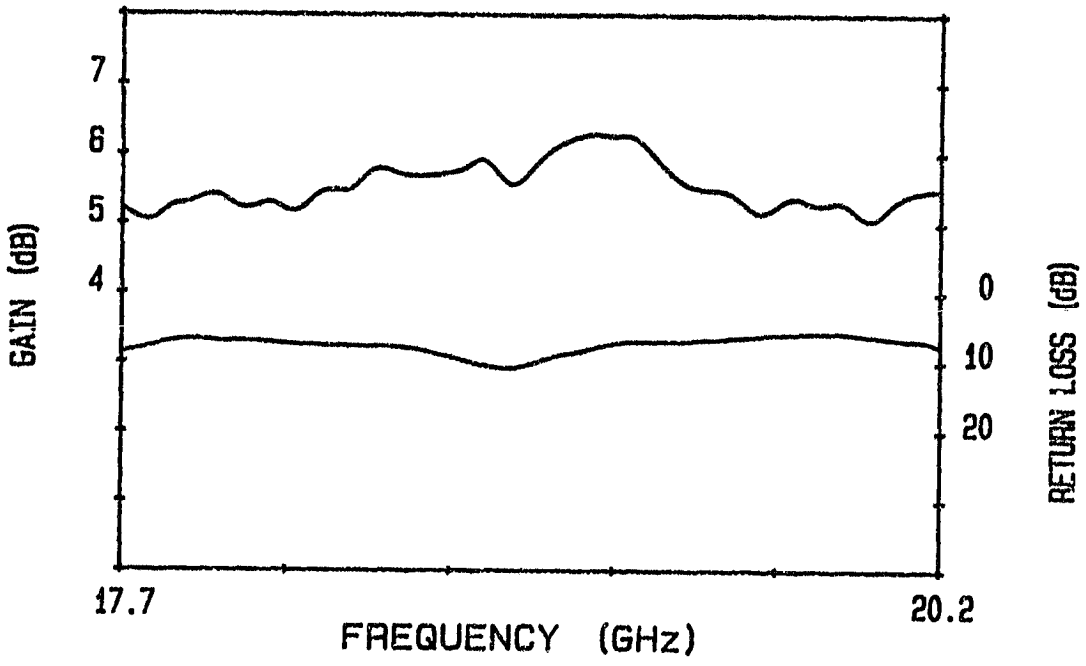
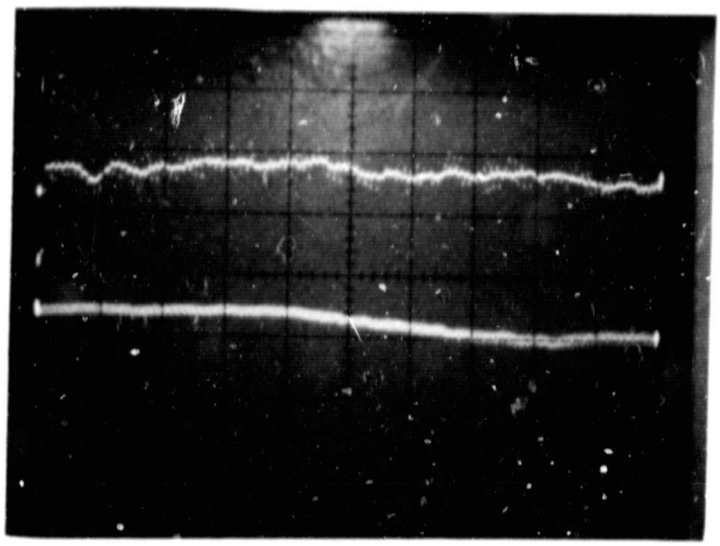


Figure 31 Gain Characteristics for a 300 μm Gate Width FET Amplifier



Vertical: Top Trace (Gain) - 1 dB/div
Reference: Center Line is +20 dB Gain (+15 dBm)
Lower Trace (Return Loss): 10 dB/div
Reference: Center Line

Horizontal: 230 MHz/div. Range 17.7 to 20.2 GHz

Input Power - 5 dBm

Bias Voltage - V_d = 6 V; I_d = 150 mA

Figure 32 Gain and Return Loss Characteristic for a Four-Stage FET Amplifier

power projected while the 21.5 dB gain for the first four stages is almost in exact agreement. A new four-stage amplifier was realized and tested. The new design used two stages of 150 μm gate width devices followed by a 300 μm and 600 μm gate width FET respectively. Figure 33 shows the small signal gain versus frequency characteristic, the gain compression characteristic at 19.0 GHz, and the detail of the circuit realization. Another iteration was made and a lumped element matching for the 600 μm device was implemented. Figure 34 illustrates the improved input matching that has been obtained. The lower trace is the input return loss. The small signal gain characteristic for the first four amplifier stages is shown in Figure 35, from 17 to 22 GHz. The markers are at 17.7 and 20.2 GHz.

- Fifth stage 1350 μm

The gain characteristic for a 1350 μm gate width amplifier is shown in Figure 36; the input power is 18 dBm, the gain reference is 4 dB. The entire band is covered and the gain is 6 ± 1 dB. Figure 37 is the gain compression curve at 19 GHz for a 1350 μm π-gate FET in a fifth stage amplifier circuit. The small signal gain is 6 dB and the 1 dB compression point is 26.6 dBm.

- Sixth stage

The configuation of the sixth stage was described earlier. Figure 38 shows the gain response with a 23.4 dBm input power. A gain of 4 dB was obtained across the band.

After tuning each of the individual stages, they were assembled in six-stage modules and retuned. The gain characteristics of the first module amplifier are shown in Figure 39. At mid band a gain of 31 dB at an output power level of 0.55 W was achieved. A gain roll-off at lower frequencies was attributed to an interblock grounding problem. The second module was fitted in

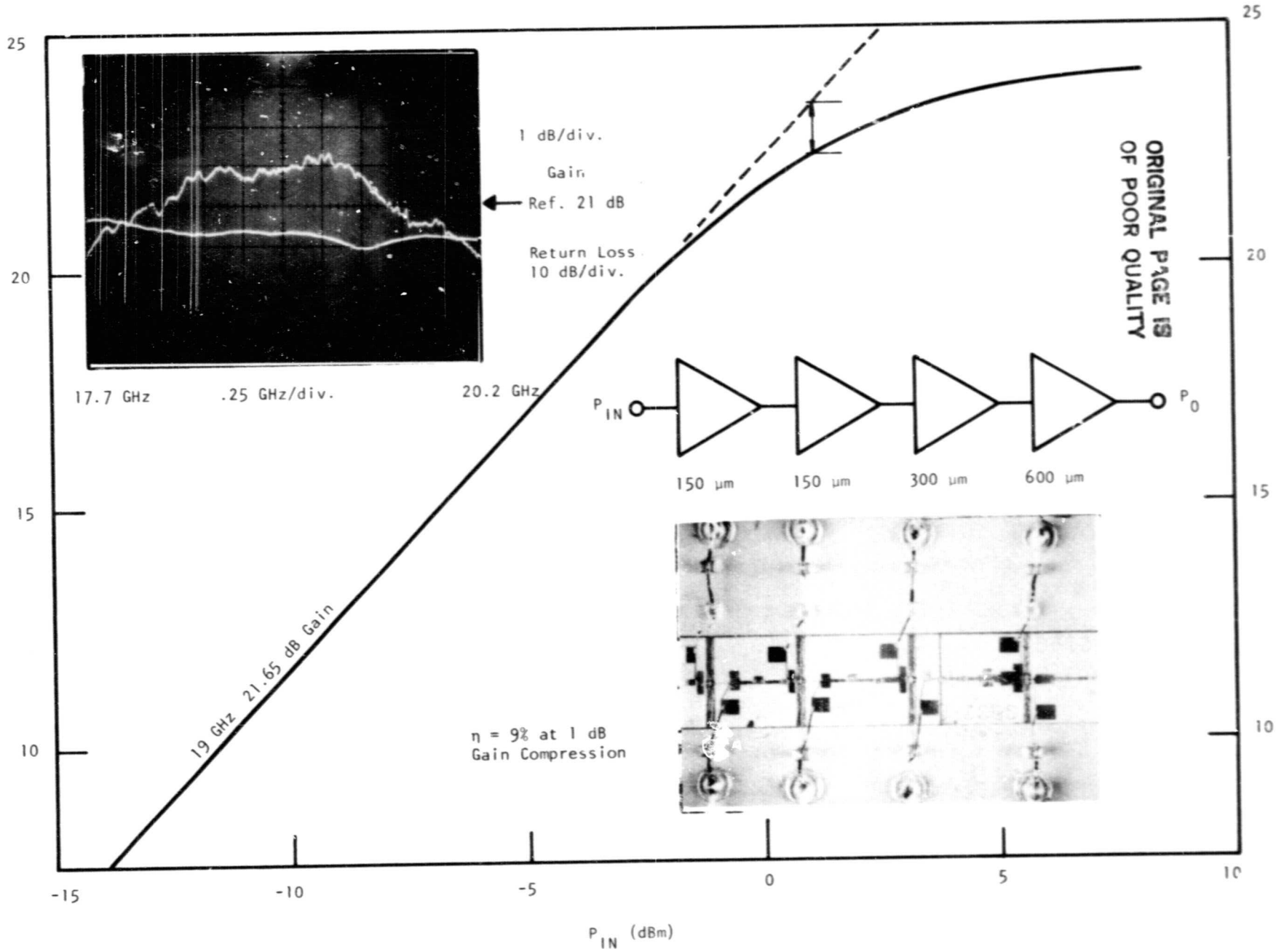
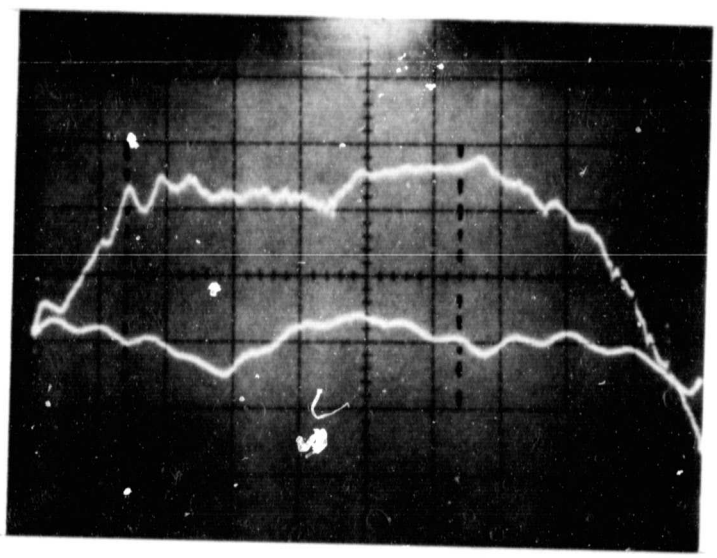


Figure 33 New Four-Stage Amplifier

Return Loss
(Lower Trace)

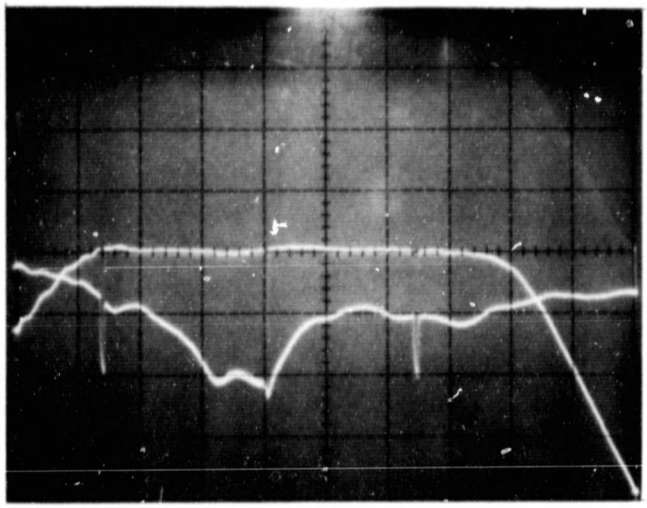


Gain
(Top Trace)

Reference 0 dB at
Center Line 10 dB/div

Reference 4 dB
Center Line
1 dB/div

Figure 34 Gain and Input Matching of Fourth Amplifier Stage
Frequency 17.7 to 22 GHz



Gain (Top Trace): Ref 20 dB at center, 1 dB/div
Return Loss (Bottom Trace): Ref 0 dB at center, 10 dB/div
Frequency 17.7 to 22 GHz
Input Power: 10 dBm
Markers: 17.7, 19, 20.2 GHz

Figure 35 Small Signal Gain for the First Four Stages

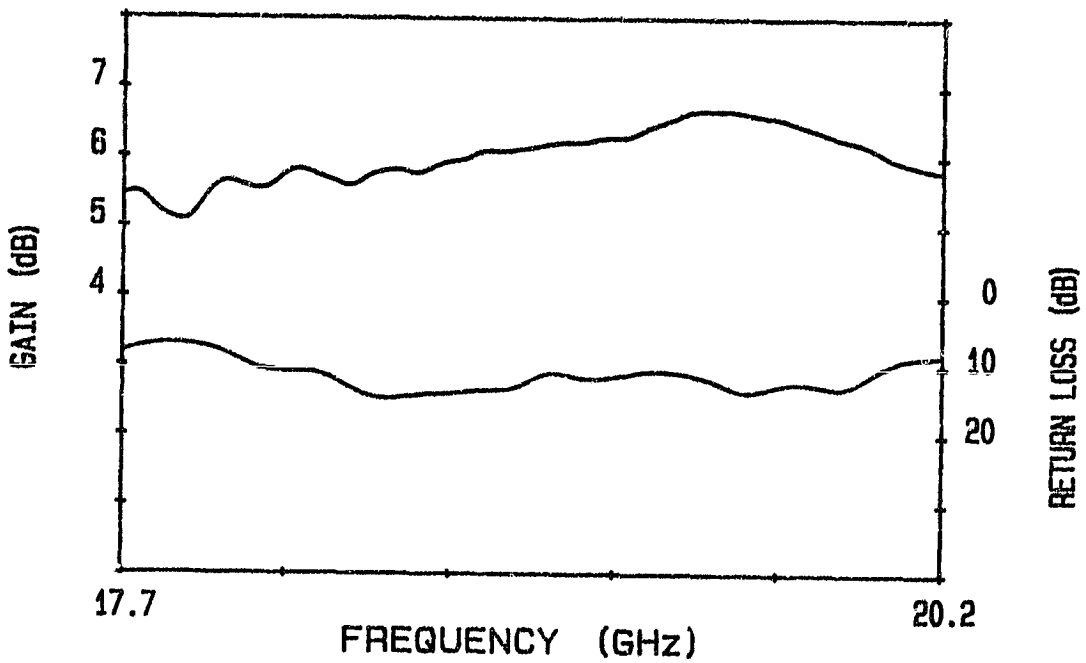


Figure 36 Gain Characteristics for a 1350 μm Gate Width FET Amplifier

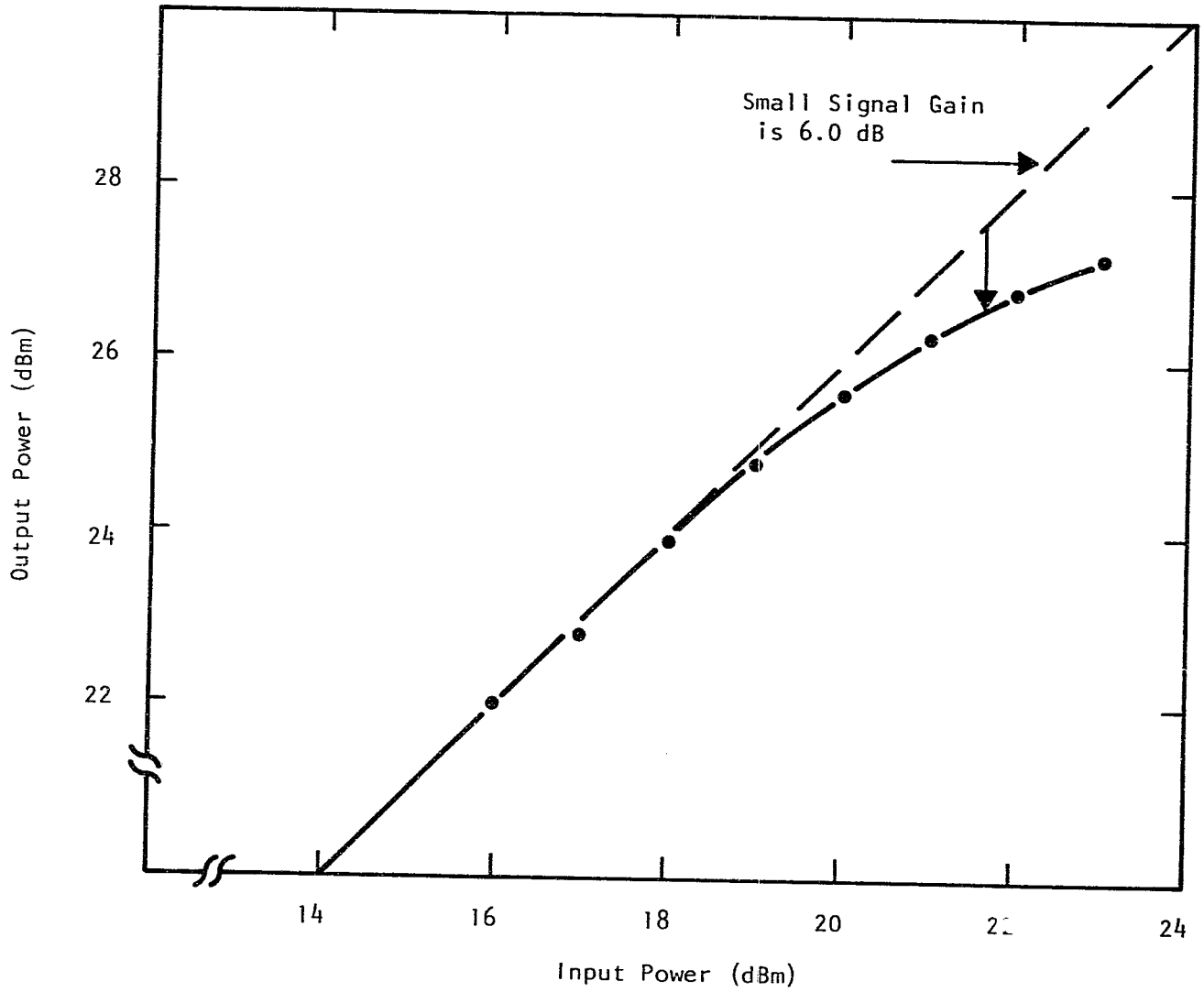
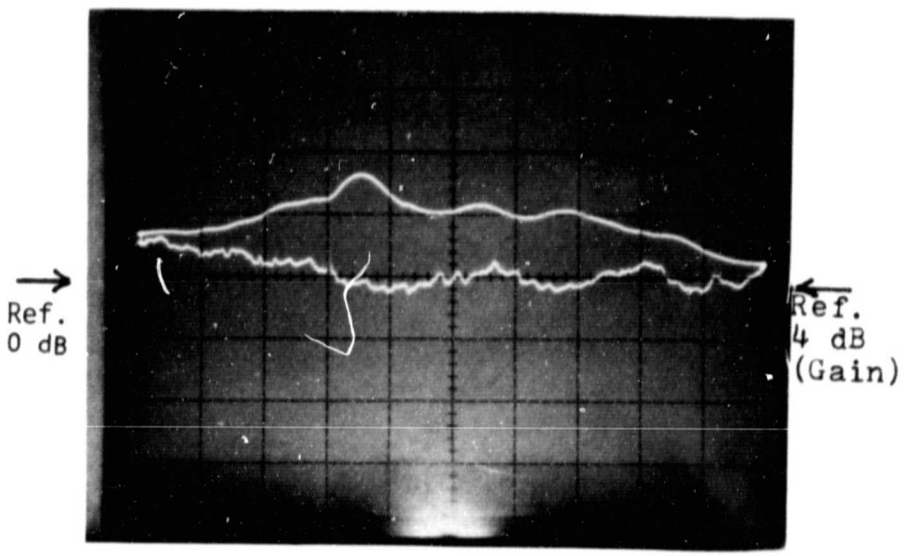


Figure 37 Gain Compression Curve for 1350 µm π-Gate FET
(In Fifth Stage Amplifier Circuit)

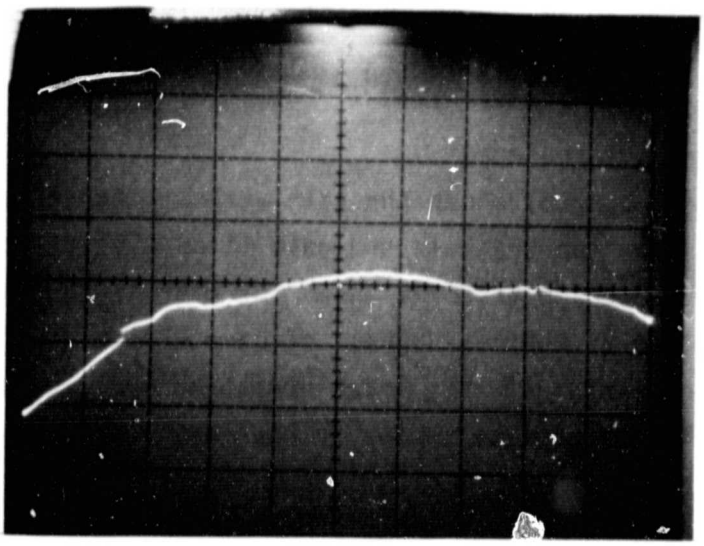


Input Power = 23.4 dBm

Vertical: Top Trace (Gain): 1 dB/div
Lower Trace (Return Loss): 10 dB/div

Horizontal: 250 MHz/div, 17.7 to 20.2 GHz

Figure 38 Sixth Stage Performance



P_{IN} =-3.8 dBm

P_{OUT} = 27.4 dBm @ 19.2 GHz

V_D = 7.2 V

I_D = 983 mA

η = 7.8%

Vertical: 5 dB/div
Reference is Center Graticule Line at 30 dB

Horizontal: 250 MHz/div, 17.7 to 20.2 GHz

Figure 39 First Six-Stage Module Performance

the production housing shown in Figure 40 and the grounding problem improved considerably over the original amplifier module. The gain obtained was 30.0 dB with center line reference 1 dB/div. The frequency band shown is 17.7 GHz to 20.2 GHz (Figure 41).

- Assembly and performance of the quads

Figure 42 (a), (b), (c), and (d) shows the gain versus frequency of each of the first four modules. The top trace is the gain (1 dB/div) relative to the center line (+ 30 dB). The center trace is shown for clarity in that the output (top trace) is operating at various degrees of compression over the frequency band and a linear cancellation of this input variation would give false indication. The center line is representative of 26.2 dBm at 19 GHz. The lower trace is the return loss of the module (10 dB/div).

A necessary condition for efficient combining of the modules is that their phases track. The phases of the different modules were measured on a phase bridge. The gain and phase of each amplifier module is shown in Figure 43. The smoothed traces are caused by the bridge being operated at 0.1 kHz bandwidth. Each phase has been normalized to the center line to compare the variation of one module relative to another. The figures indicate that the amplifiers have been designed with the upper band edge too close to the operating band edge (20.2 GHz). Some roll-off is also possibly a result of the degree of saturation at which each amplifier module is operated. One further possible variation that has not been verified, is that the phase bridge is referenced to a length of WR-42 waveguide and the internal operating mechanisms (microstrip line, transformers, bumped element bond wires, and devices) do not necessarily exhibit the same degrees of dispersion as this reference. Table 4 gives a breakdown of the variations measured at 19 GHz for the different amplifier modules. The second column of data is computed from the equivalent length of WR-42 waveguide required to return the phase reference to the center line when the amplifier is substituted in place of a physically equal length of WR-51 waveguide. The electrical length of this piece of WR-51 waveguide is

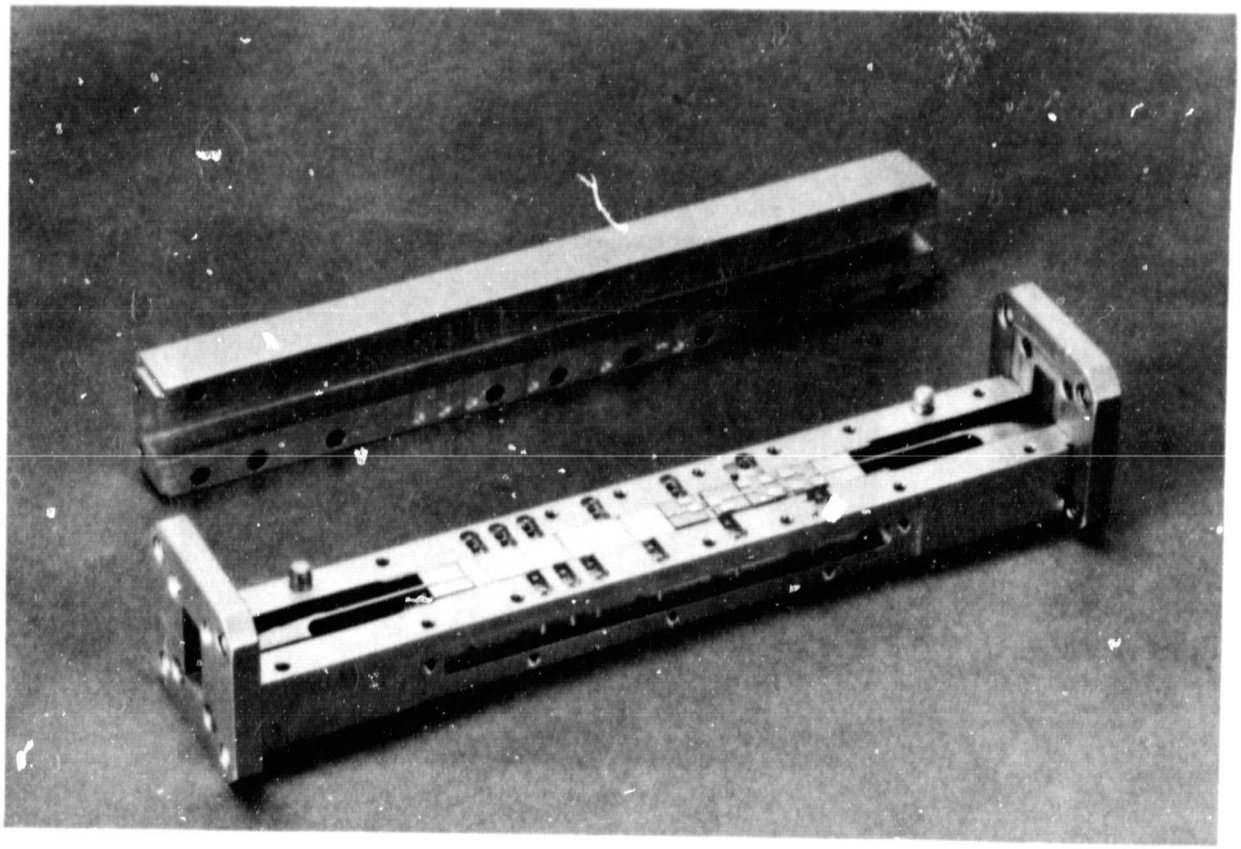
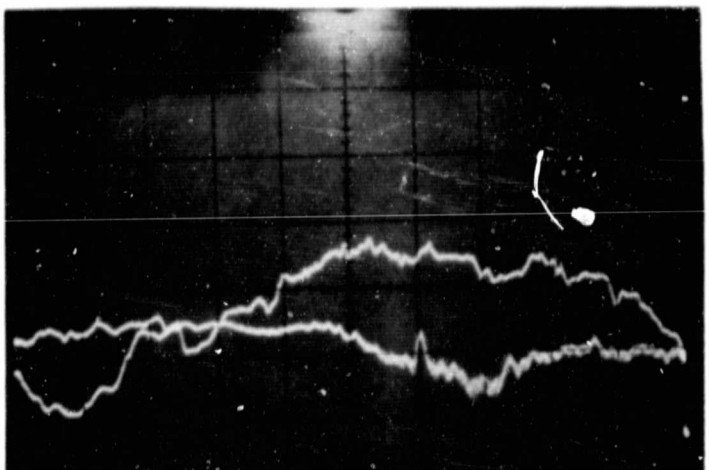


Figure 40 20 GHz Module Amplifier

Return Loss
(Lower Trace)



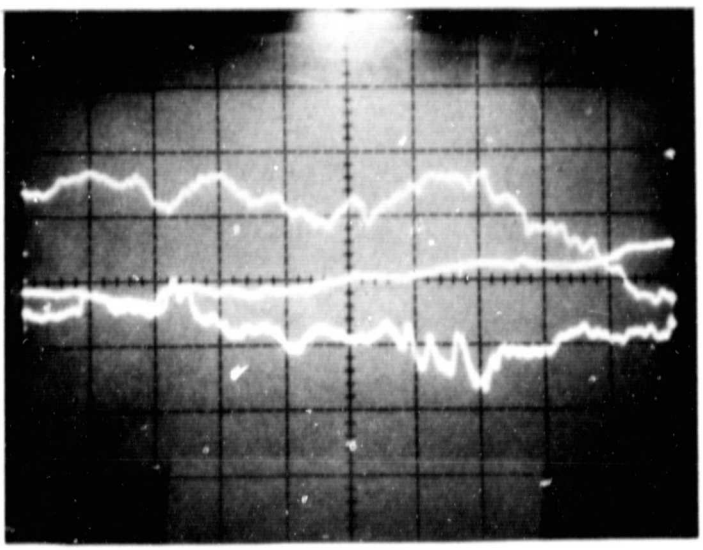
Gain
(Top Trace)

Reference 0 dB at
Center Line 10 dB/div

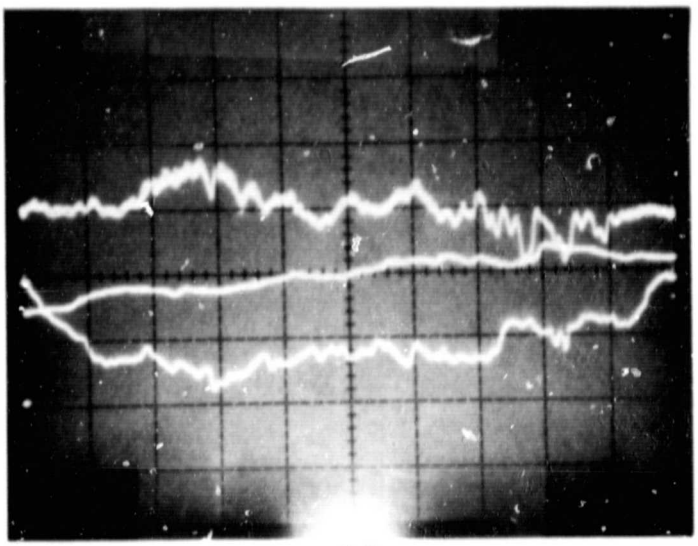
Reference +30
at Center Li
1 dB/div

Figure 41 Second Six-Stage Module Performance Frequency
17.7 to 20.2 GHz

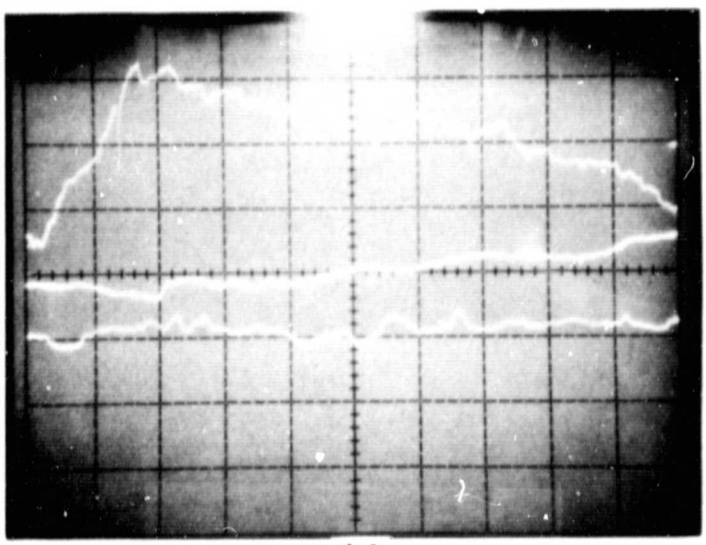
Center Trace
Input Reference 1 dB/div
Frequency Range 17.7 to 20.2 GHz



(a)

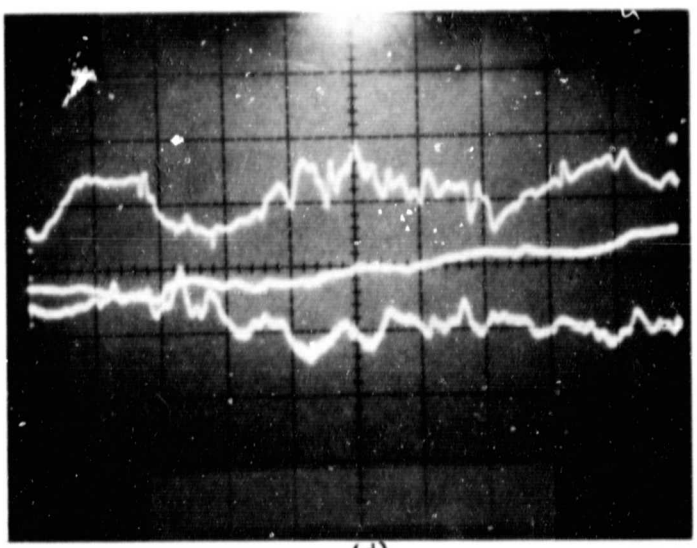


(b)



(c)

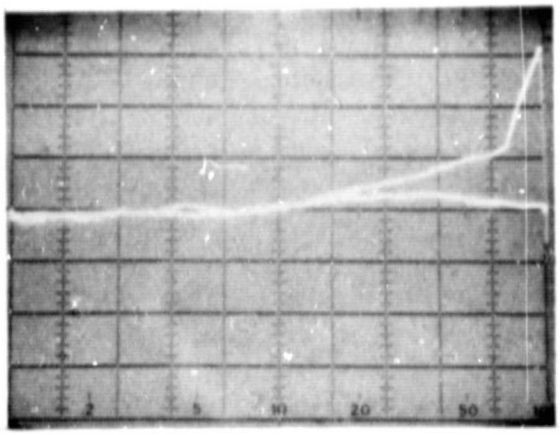
Return Loss 10 dB/div



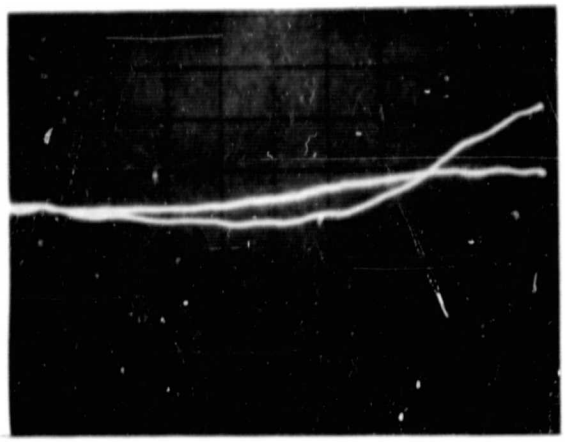
(d)

Gain 1 dB/div

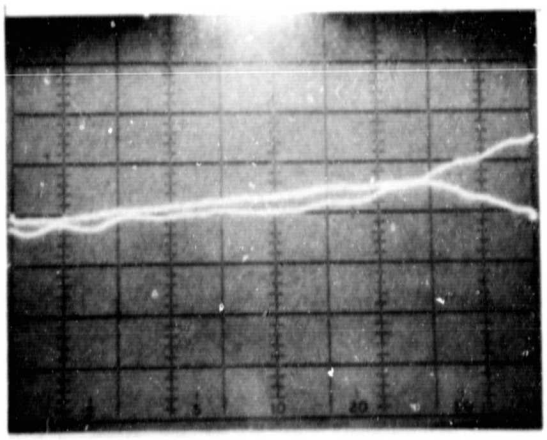
Figure 42 Ga'n vs Frequency for Each Module



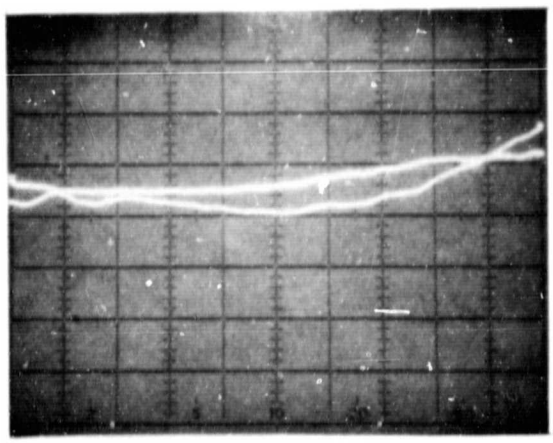
(a)



(b)



(c)



(d)

18 to 20 GHz
Phase 45°/div
Amplitude 1 dB/div

BW 0.1 kHz
Reference Offset 180°

Figure 43 Module Amplitude and Phase Data

Table 4

Performance Data for Module Amplifiers

Module No.	Electrical Length (deg)	Insertion Length (deg)	Gain (dB)	(deg) Phase dev. From mean	(dB) Gain dev. From mean
1	1962.9	4987.8	33.0	+17.7	+0.8
2	1952.0	4976.8	31.6	+6.8	-0.6
3	1921.6	4946.5	32.7	-23.6	+0.5
4	1927.8	4952.7	31.6	-13.3	-0.6

$$*\text{Mean Phase} = \frac{1}{4} \sum_{M=1}^{4} \text{Phase (M)}$$

$$\text{Mean Gain} = \frac{1}{4} \sum_{M=1}^{4} \text{Gain (M)}$$

Data Reference 19 GHz

dc input 7.2 V at 3.68 A

rf P_{IN} = +2.4 dBm = 1.7 MW

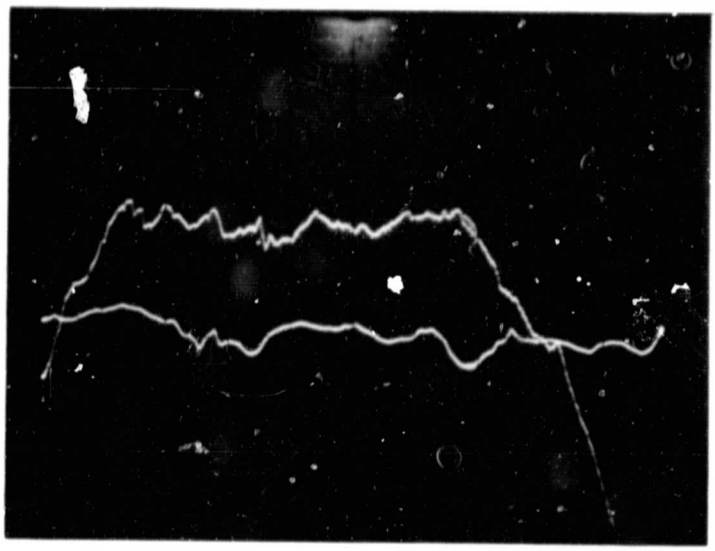
rf P_O = 2344 mW

$$\text{PAE} = \frac{(2344 - 1.7) \times 100}{(7.2 \times 3.68 \times 1000)} = 8.84\%$$

approximately 3025 degrees at 19 GHz. The phase variations that were observed on the modules are shown (column 5) to be approximately ± 20° with a gain deviation of approximately ± 0.7 dB when driven from their nominal input levels. The power added efficiency is computed as 8.84% based on the power output, power input, and dc data at 19 GHz with nominal input drive level.

Figure 44 shows the output versus frequency for the quad of modules. The upper end of the band is rolled off apparently because of the phase irregularities of the individual amplifier modules. The lower trace is the return loss at the input to the manifold. The 1 dB bandwidth is approximately 1.6 GHz and the 3 dB bandwidth is 2.1 GHz. Table 5 is a listing of the P_o versus P_{in} at 19 GHz of the quad and the gain compression experienced. The data show that the quad is being operated at slightly over 1 dB gain compression with the nominal input level of 2.4 dBm. The maximum saturated power output with approximately 7 dB of overdrive is 2.43 W. Figure 45 is a graph of the data shown in Table 5. Figure 46 shows the output saturation with input drive level over the 17.7 to 20.2 GHz band. It illustrates that the upper end of the operating band saturates at a lower input drive level and that to present a flat response, the linear gain and saturation characteristics were traded off against one another to accomplish this end over frequency. This figure shows that the quad of modules can withstand up to a 7 dB overdrive on the input without disasterous effects.

All the individual modules were then individually tuned for best response over the desired bandwidth. These modules were grouped in pairs and retuned, using only minor gate bias adjustments. (This is allowable since the gate bias is accomplished using a voltage divider arrangement.) The adjustments were made while observing the output response of the modules over the entire band (attempting to accomplish both absolute gain and maximum power output at the same time). The modules were driven by a single magic tee splitter and power combiner using an identical tee (same as those used in the waveguide combiners).



Top Trace Gain 1 dB/div C L ref +30 dB
P_0 (dBm) 1 dBm/div C L ref +33 dBm
Bottom Trace Input Return Loss 10 dB/div C L ref 0 dB

Figure 44 Quad of Module Amplifiers Gain and P_0 (dBm) vs Frequency

Note: Frequency Range 17.7 to 20.2 GHz
1 dB BW $\approx$ 1.6 GHz
3 dB BW $\approx$ 2.1 GHz

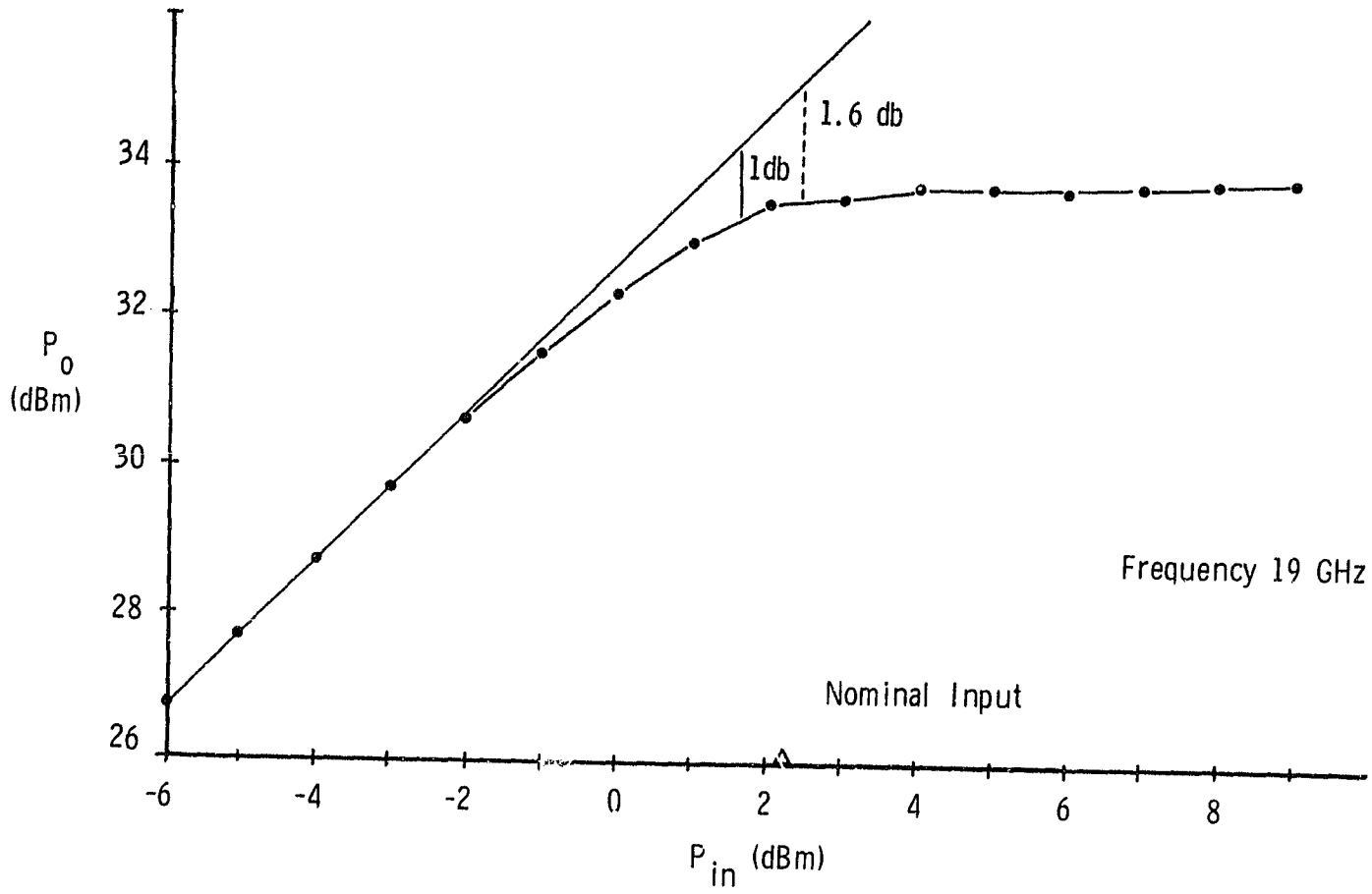
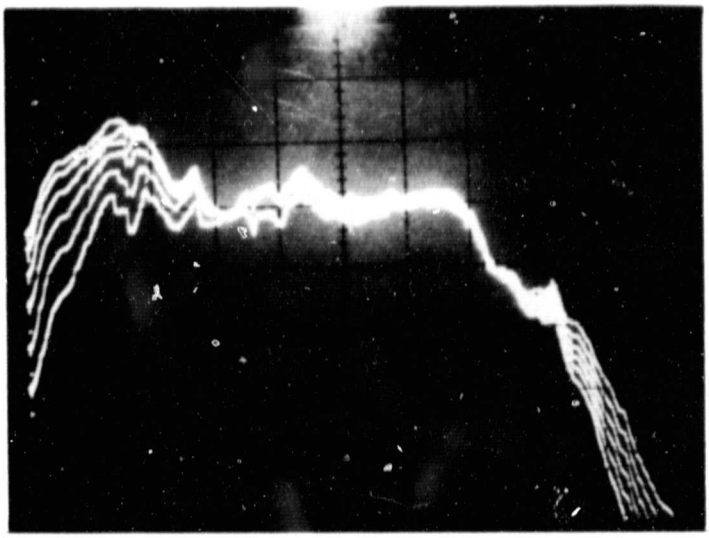


Figure 45 P_O vs P_{IN} for Quad of Amplifier Modules Data from Table 5

Table 5
P_O vs P_{IN} at 19 GHz

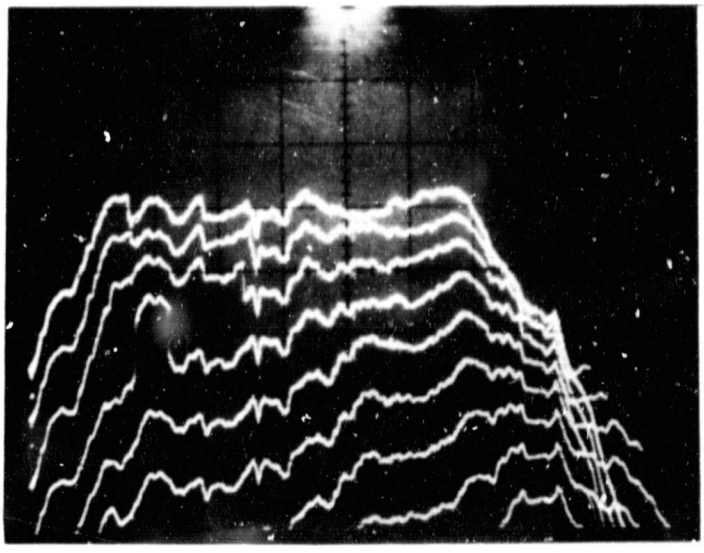
	P_{IN}(dBm)	P_O(dBm)	P_O(W)	Gain (dB)	
	9	33.85	2.43	24.85	
	8	33.80	2.39	25.8	
	7	33.75	2.37	26.75	
	6	33.70	2.34	27.7	
	5	33.75	2.37	28.75	
	4	33.75	2.37	29.75	
Nominal Input →	3	33.60	2.29	30.6	
	2	33.5	2.24	31.5	
	1	33.0	1.99	32.0	← 1 comp.
	0	32.3	1.69	32.3	
	-1	31.5	1.41	32.5	
	-2	30.6	1.15	32.6	
	-3	29.7	0.93	32.7	
	-4	28.7	0.74	32.7	
	-5	27.6	0.59	32.7	
	-6	26.7	0.47	32.7	



Bottom Trace
Output with
Nominal Input
(+2.4 dBm)

Upper Traces
1 dB Step Increas
in Input Drive

(a)



Top Trace
Output With
Nominal Input
(+2.4 dBm)

Lower Traces
1 dB Step
Reduction in Inpu
Drive

(b)

Frequency Range 17.7 to 20.2 GHz

Figure 46 P_0 vs P_{IN} vs Frequency

The output power of the four assembled quads is shown as Figure 47. The proof of concept amplifier (see Figure 48) was assembled and preliminary test were run. The peak output power of 8.95 W occured at 18.6 GHz with 1 dB bandwidth of 18.025 GHz to 19.725 GHz. This saturated power was obtained at a 9.1% power added efficiency. The 3 dB bandwidth is in excess of 2.5 GHz. This power was measured immediately after turn on with a cold plate temperature of 20°C. A slight power sag was observed until thermal stability was achieved. The output power versus frequency and the amplifier gain versus frequency are shown in Figures 49 and 50. At 17.7 GHz the power is more than 5 W and at 20.2 GHz it is more than 4.4 W.

During noise measurement, the amplifier failed. The burn-out was attributed to a kink in the supply line. Extensive damage occured and only a few FETs were saved. Inadequate protection on the bias network was the cause of the burnout; all the gate lines were tied together and all the drain lines were tied together. A transient was able to propagate throughout the amplifier.

The amplifier was rebuilt with the following changes. The biasing network was completely redesigned. Appropriate resistor stabilization was introduced in the first three stages. Also the Wilkenson combiner without isolation resistors was found to be a potential source of oscillation. Since time was too short for a redesign of the 2700 μm gate width stage, it was decided to use a single 1350 μm gate width device in a fifth stage configuration in conjunction with the MBE devices described previously in this report.

The individual modules were retuned. The output power characteristics are shown in Figure 51 for a module into 6 dB compression. The modules were tuned to the same gain behavior and the quads were assembled. The output power was optimized by varying the gate bias voltage on each module. Figure 52 shows a quad output power when 2 dB into compression. Figure 53 shows the output power of the overall sixteen way amplifier 2 dB into compression. Table 6 shows the required and actual amplifier performances.

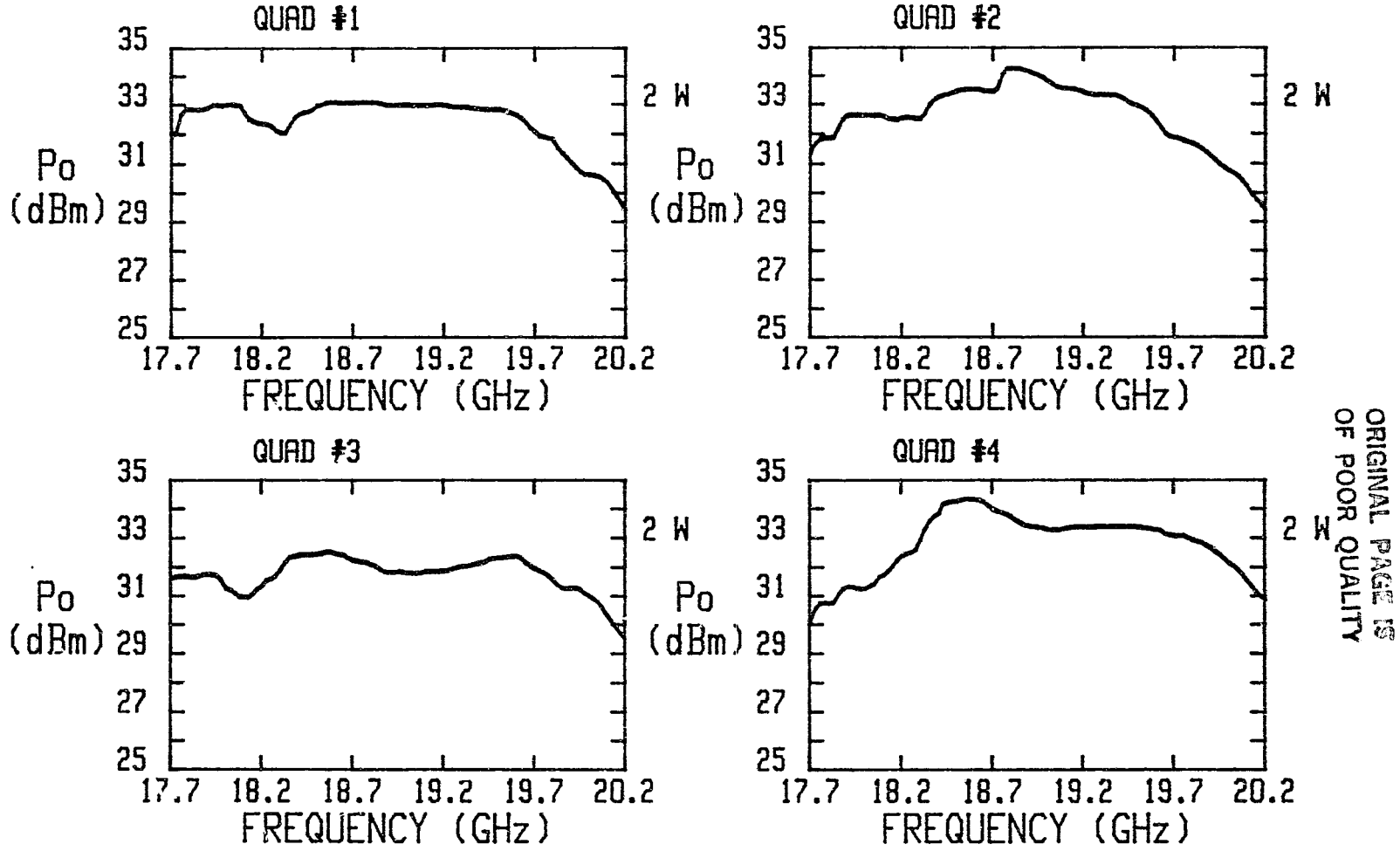


Figure 47 Quad Amplifier Output Power Performance

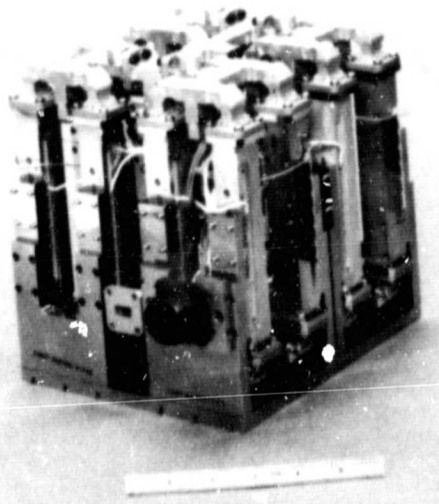


Figure 48 16-Module "Proof of Concept" Amplifier

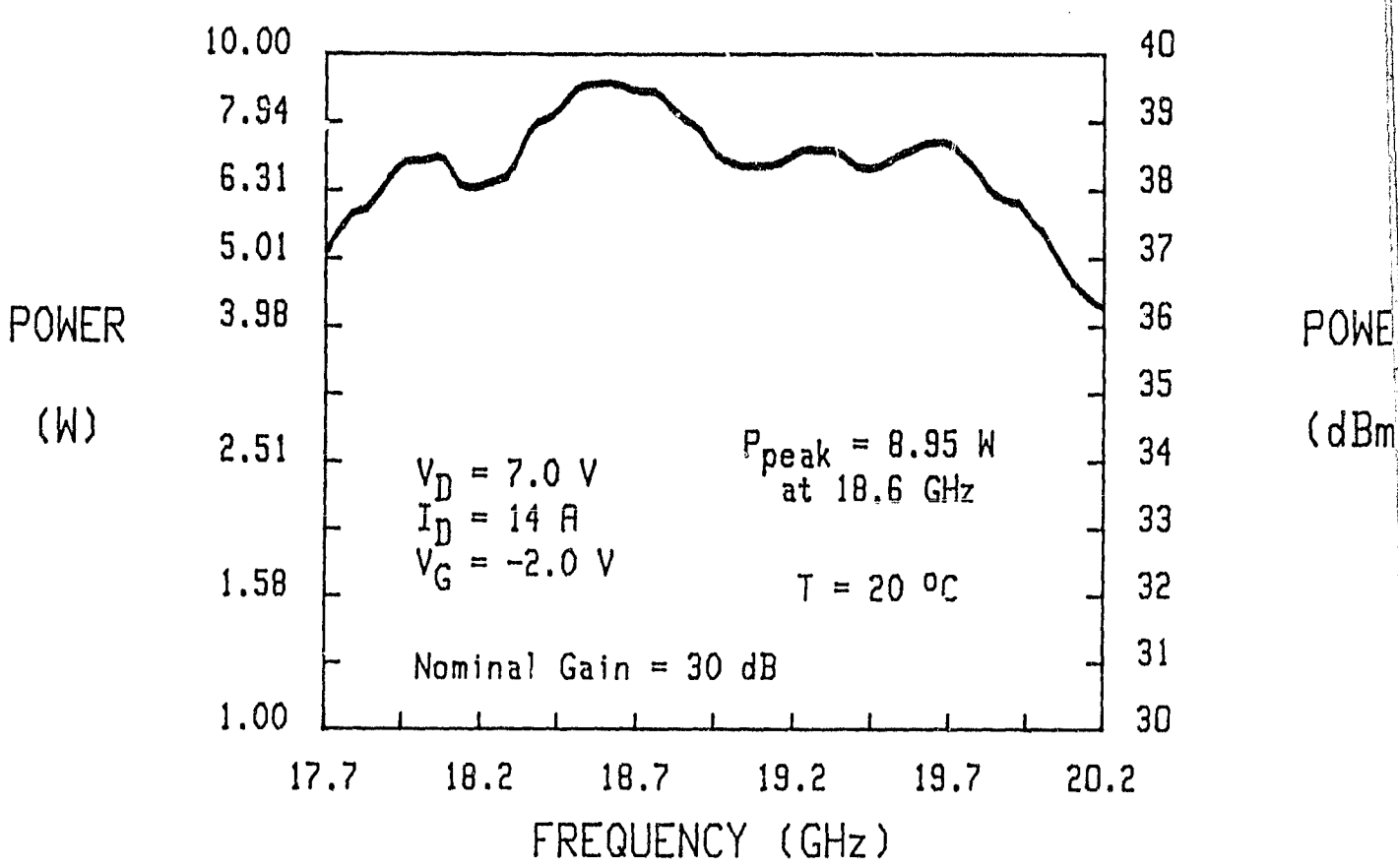


Figure 49 Performance of a 16-Module Amplifier.

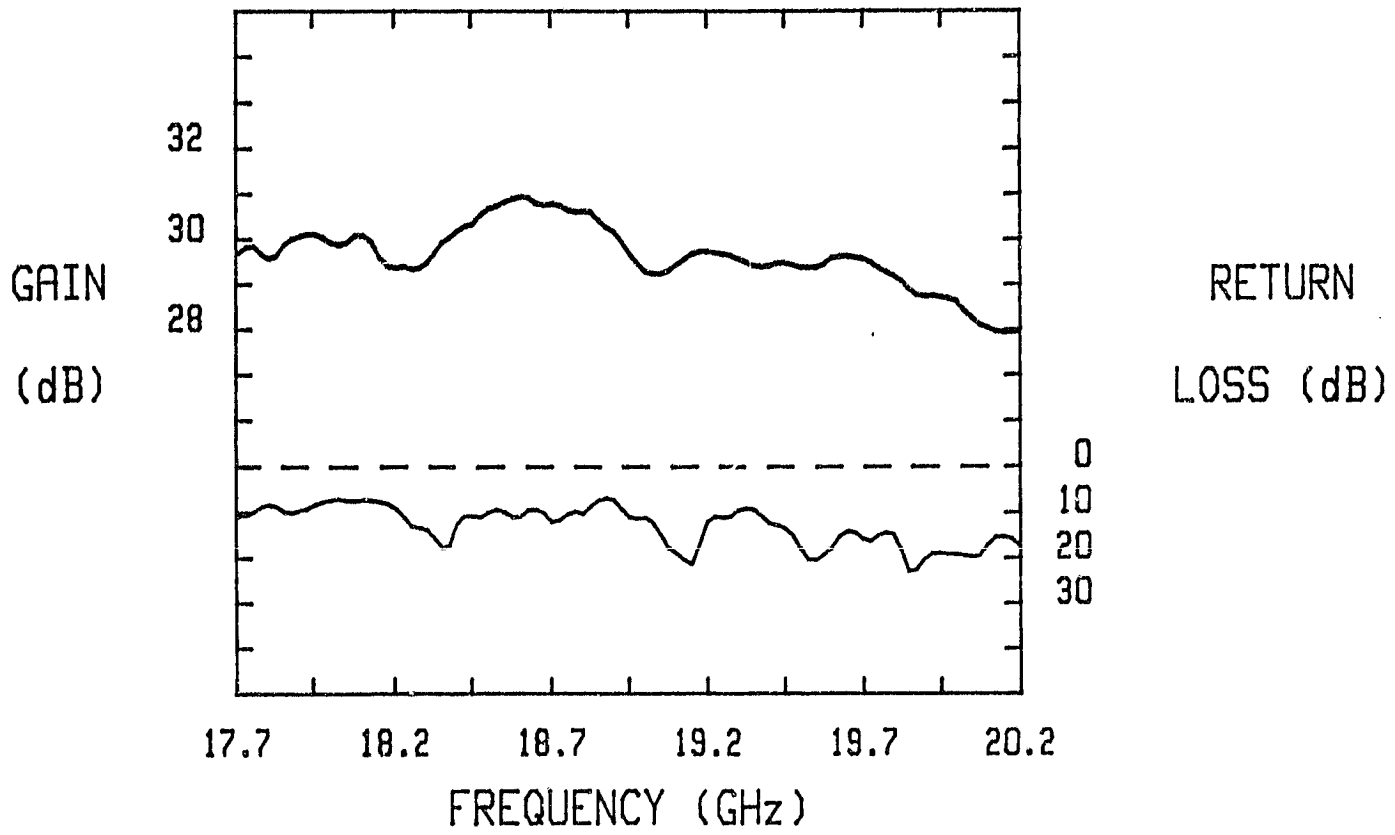


Figure 50 Performance of 16-Module Amplifier.

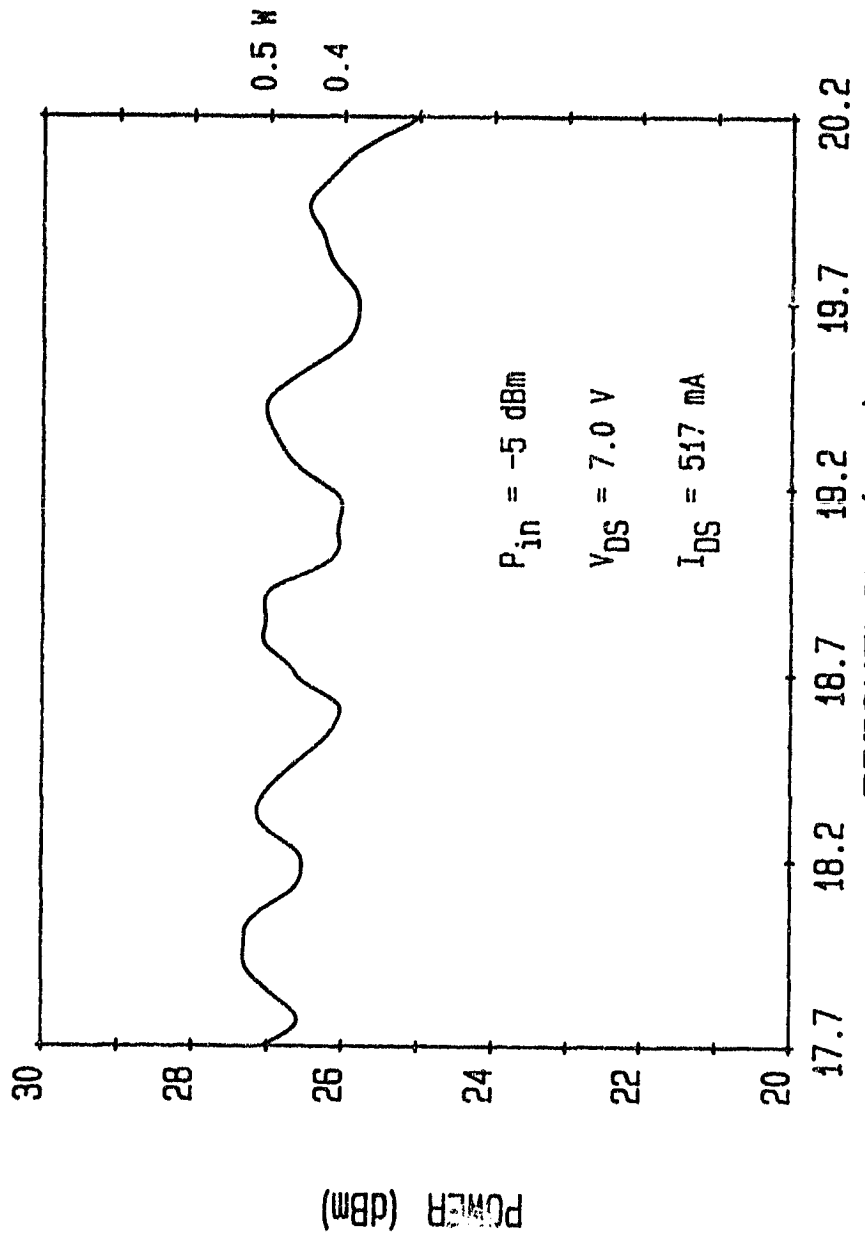


Figure 51 Six-Stage FET Amplifier Performance

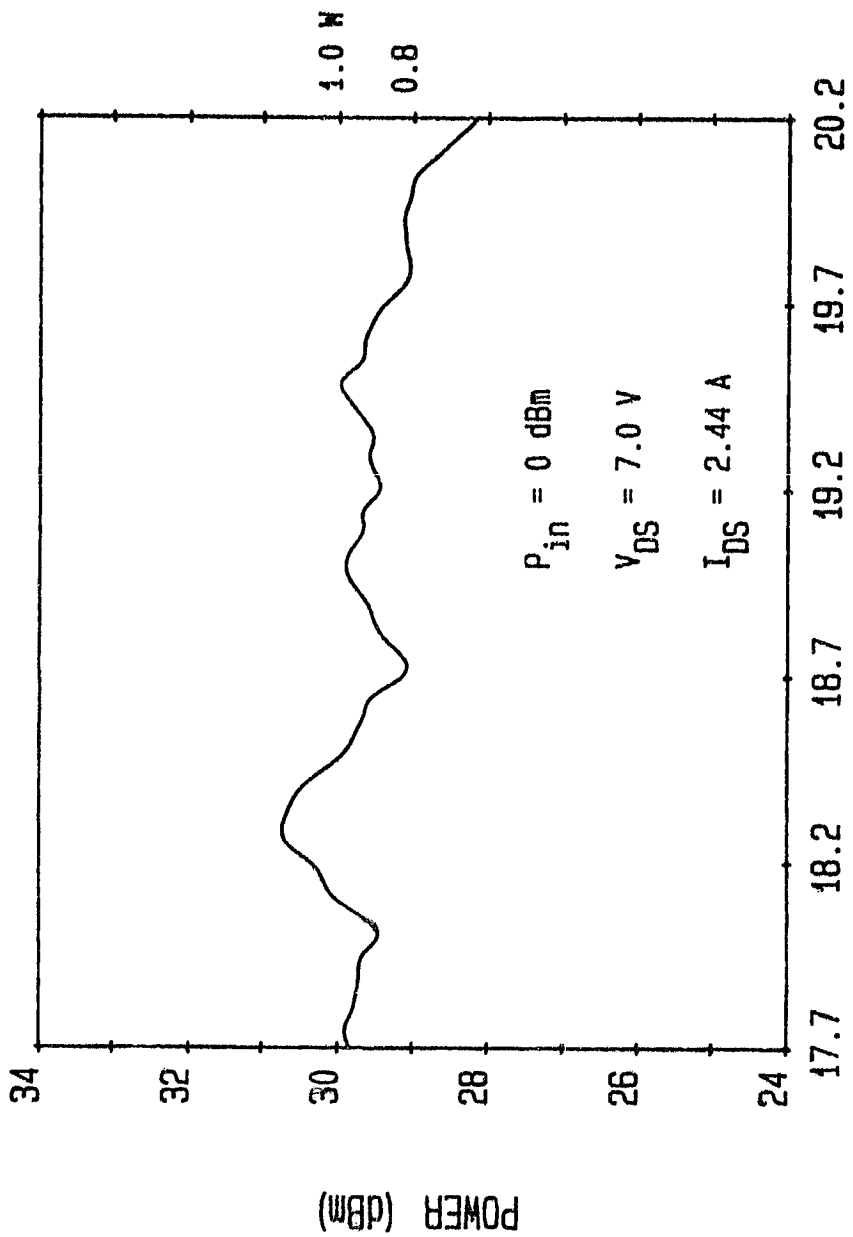


Figure 52 Quad Amplifier Performance

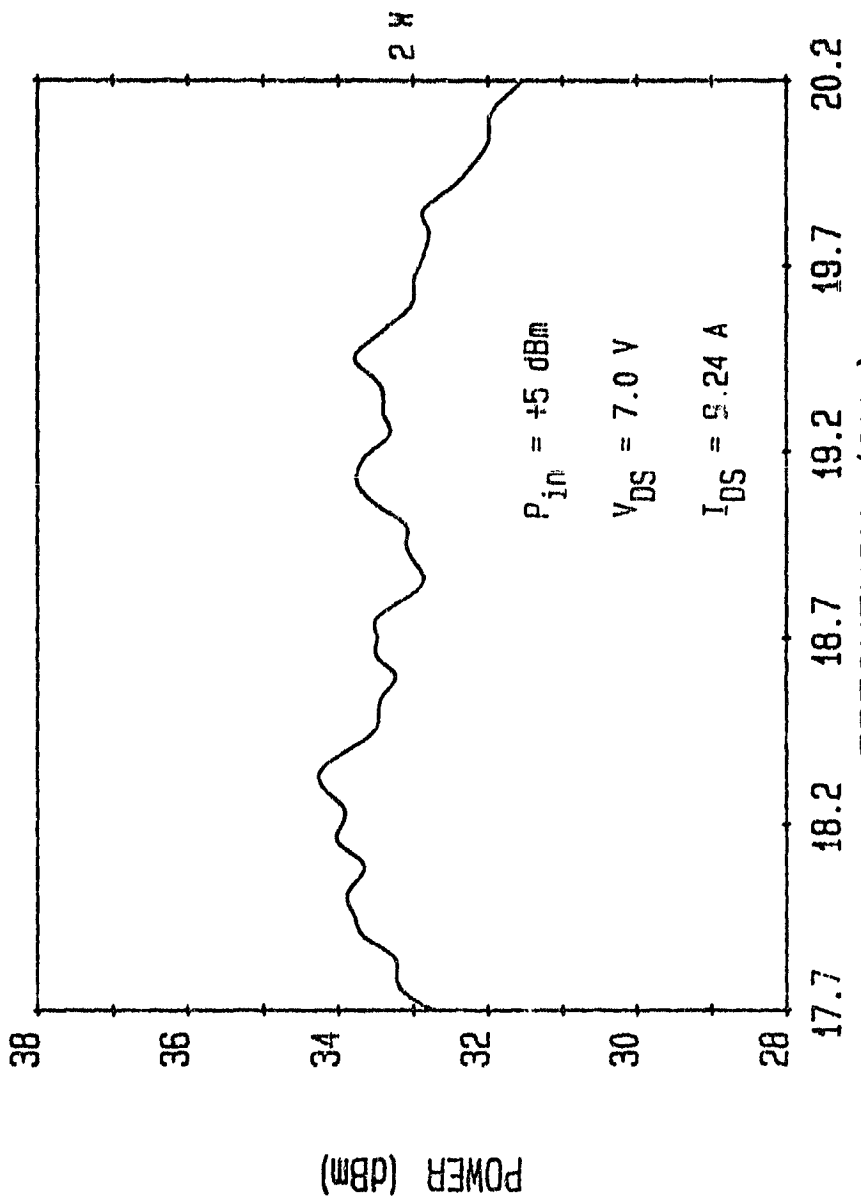


Figure 53 Sixteen-Way Amplifier Performance

Table 6

Required and Actual Amplifier Performances

	Required Performances	First Amplifier Performances	Rebuilt Amplifier Performances
rf Band	17.7 - 20 2 GHz	17.6 - 20.1 (3 dB)	17.5 - 20.2 (3 dB)
Output Power	6.0 to 7.5 W	8.95 W	3 W
Gain	30 dB	30 dB	30 dB

SECTION V
CONCLUSION

During the course of the program, the feasibility of an 8 W, 17.7 to 20.2 GHz, 30 dB gain amplifier was demonstrated. The goal of 20% power added efficiency was out of reach, as was stated early in our proposal.

The key achievements were:

- 30 dB gain 0.5 W output power amplifier modules.
- 16 way waveguide divider/combiner with less that 0.3 dB insertion loss across the 17.7 to 20.2 GHz bandwidth.
- Direct waveguide to microstrip transition with less than 0.5 dB insertion loss.