https://ntrs.nasa.gov/search.jsp?R=19840012669 2020-03-20T23:51:58+00:00Z

NASA-CR-168326
19840012669

30-GHz MONOLITHIC RECEIVE MODULE

First Annual Report for Period
November 3, 1982-October 31,1983

Contract No. NAS3-23356

March 1984

LIBRARY COPY

APR 10 1984

LANGLEY RESEARCH CENTER
LIBRARY, NASA
HAMPTON, VIRGINIA

For
National Aeronautical and Space Administration
Lewis Research Center
Communication and Propulsion Section

Honeywell

Physical Sciences Center

ENTER:

COMMAND IS MISSING

====================

****** AUTOMATIC END SEARCH BYPASS *****
SEARCH TITLE
DATE/FILE 03-14-85/N
****** BEGIN SEARCH BYPASS ******
DATE/FILE 3-14-85/N
PRIMARY DATA BASE ONLINE
SET NO.OF NO.OF DESCRIPTION OF SET
NO. REC. OCC. (+=OR, *=AND, -=NOT)
--- ----- ----- --------------------

DISPLAY 84N20737/2

84N20737*# ISSUE 11 PAGE 1642 CATEGORY 32 RPT#: NASA-CR-168326 NAS 1.26:168326 AR-1 CNT#: NAS3-23356 83/12/00 93 PAGES UNCLASSIFIED DOCUMENT

UTTL: The 30-GHz monolithic receive module TLSP: Annual Report, 3 Nov. 1982 - 31 Oct. 1983

AUTH: A/SOKOLOV, V.; B/GEDDES, J.; C/BAUHAHN, P.

CORP: Honeywell, Inc., Bloomington, Minn. CSS: (Physical Sciences Center.)

AVAIL.NTIS SAP: HC A05/MF A01

MAJS: /*ANTENNA ARRAYS/*EXTREMELY HIGH FREQUENCIES/*GATES (CIRCUITS)/*INTEGRATED CIRCUITS/*ION IMPLANTATION/*RECEIVERS

MINS: / AMPLIFIERS/ ANTENNA FEEDS/ ELECTRONIC MODULES/ FABRICATION/ FIELD EFFECT TRANSISTORS/ GALLIUM ARSENIDES/ PHASE SHIFT

ABA: A.R.H.

ABS: Key requirements for a 30 GHz GaAs monolithic receive module for spaceborne communication antenna feed array applications include an overall receive module noise figure of 5 dB, a 30 dB RF to IF gain with six levels of intermediate gain control, a five-bit phase shifter, and a maximum power consumption of 250 mW. The RF designs for each of the four submodules (low noise amplifier, some gain control, phase shifter, and RF to IF sub-module) are presented. Except for the phase shifter, high frequency, low noise FETs with sub-half micron gate lengths are employed in the submodules. For the gain control, a two stage dual gate FET

ENTER:

30 GHz Monolithic Receive Module

First Annual Report for Period

November 3, 1982 - October 31, 1983

Contract No. NAS3-23356

Prepared By

Honeywell Physical Sciences Center

10701 Lyndale Avenue South, Bloomington, MN 55420

V. Sokolov, J. Geddes, P. Bauhahn

Phone (612) 887-4452

For

NASA-Lewis Research Center

Communication and Propulsion Section

21000 Brookpark Road

Cleveland, OH 44135

Al Downey, Technical Manager

Mail Stop 54-5

Approved V. Sokolov Date 16 November 1983 T. C. Lee

V. Sokolov
Program Manager

T. C. Lee
Department Manager

47119

N84-20739#

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-168326		

4. Title and Subtitle	5. Report Date
30 GHz Monolithic Receive Module First Annual Report for Period November 3, 1982 - October 31, 1983	December 1983
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
V. Sokolov, J. Geddes, P. Bauhahn	
	10. Work Unit No.

9. Performing Organization Name and Address	11. Contract or Grant No.
Honeywell Corporate Technology Center 10701 Lyndale Avenue South, Bloomington, Minnesota 55420	NAS3-23356
	13. Type of Report and Period Covered

12. Sponsoring Agency Name and Address	13. Type of Report and Period Covered
	Annual, 11-3-82 to 10-31-83
National Aeronautics and Space Administration Washington, D.C. 25046	14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, Alan N. Downey, Space Communications Division, NASA
Lewis Research Center, Cleveland, Ohio 44135

16. Abstract

This report describes the first year's progress on a four year program to develop a 30 GHz GaAs monolithic receive module for spaceborne communication antenna feed array applications. Key requirements included on overall receive module noise figure of 5 dB, a 30 dB RF to IF gain with six levels of intermediate gain control, a five-bit phase shifter, and a maximum power consumption of 250 mW.

RF designs for each of the four sub-modules (low noise amplifier, gain control, phase shifter, and RF to IF sub-module) are presented. Except for the phase shifter, high frequency, low noise FETs with sub-half micron gate lengths are employed in the sub-modules. For the gain control a two stage dual gate FET amplifier is used. The phase shifter is of the passive switched line type and consists of 5-bits. It uses relatively large gate width FETs (with zero drain to source bias) as the switching elements. A 20 GHz local oscillator buffer amplifier, a FET compatible balanced mixer, and a 5-8 GHz IF amplifier constitute the RF/IF sub-module.

A novel approach to the phase shifter fabrication using ion implantation and a self-aligned gate technique is described. This method of phase shifter fabrication holds promise in reducing RF losses at high frequencies. Preliminary RF results obtained on such phase shifters are also presented.

17. Key Words (Suggested by Author(s))		18. Distribution Statement
Ion Implantation	30/20 Communications Satellite	Unclassified - Unlimited
MM-Wave Monolithic Circuits	Ka-Band Receiver	
GaAs Monlithic Circuits	Monolithic Mixer	
Low Noise FETs		
Phase Shifter		
Self-Aligned Gate		

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified		

* For sale by the National Technical Information Service, Springfield, Virginia 22161

NASA Annual Report

Table of Contents

NASA Annual Report

List of Figures

List of Figures (Continued)

List of Figures (Concluded)

List of Tables

I. SUMMARY

The objective of the four year program is to develop a 30 GHz monolithic receive module for communication antenna feed array applications, and to deliver submodules and 30 GHz monolithic receive modules for experimental evaluation. Key requirements include an overall receive module noise figure of 5 dB, a 30 dB RF to IF gain with six levels of intermediate gain control, a 5 bit phase shifter, and a maximum power consumption of 250 mW. In addition, the monolithic receive module design addresses a cost goal of less than $1,000 (1980 dollars) per receive module in unit buys of 5,000 or more, and a mechanical configuration that is applicable to a space-borne phased array system. These requirements are summarized as performance goals in Table S-1.

The design of the monolithic module (Task I) includes a partioning of the receiver into four submodule functions: the low noise amplifier (LNA), the 5-bit phase shifter (PS), gain control (GC) and the RF/IF frequency down-conversion function as shown in Figure S-1. The PS, GC, RF/IF and LNA functions embodied in the monolithic receive module are also developed as individual submodules, each fabricated on a separate chip (Tasks II-V respectively), and designed so as to permit their interconnection to form the interconnected receive module (Task VI).

During the first year of the program work has concentrated on device and circuit design (Task I) and the fabrication and evaluation of the phase shifter (Task II) as well as the initial development of the gain control (Task III) submodules. Consequently, Section II of this report discusses, for the

most part, the details of the progress made on the first three tasks. Nevertheless, since many of the tasks have overlap, especially in the design area, the work accomplished in the first year is also applicable to the development of the other two submodules. For example, in the case of the gain control amplifier, the first mask set includes 100 micron gate width low noise FETs which are also required for both the RF/IF and the LNA submodules. Highlights of specific accomplishments during the first year are outlined in the following..

Overall Monolithic Receive Module Design - Figure S-2 shows the functional configuration for the monolithic receive module and also indicates nominal gains, noise figures, dc power consumption, and overall noise and gain performance for each submodule element and the complete receive module. The low noise amplifier provides sufficiently high gain (32 dB) and low noise operation to be the major determining factor in establishing the required 5 dB noise figure for the overall receiver. To achieve this type of performance it is expected that sub-half micron gate length FETs with 100 micron gate widths will be required.

The phase shifter is a 5-bit passive device and utilizes self-aligned gate (SAG) switching FETs to achieve low insertion loss. The switches are used to switch between transmission lines of different electrical lengths to achieve true time delay phase shifting for the larger phase shifts (180°, 90° and 45° bits), and to switch in reactive loading on the lines to accomplish the smaller phase shifts (22° and 11° bits). A SAG FET approach utilizing series switches has been chosen as the base line approach to the phase shifter

development.

Gain control is accomplished by a dual gate amplifier in conjunction with a passive switched attenuator. The former utilizes 100 micron low noise dual gate FETs, while the switched attenuator uses the switching FET technology developed in the switched line phase shifter.

Finally, the RF/IF submodule incorporates Schottky diodes in a balanced mixer configuration to accomplish the frequency translation to IF (5.5 - 8 GHz). Again, a low noise amplifier is used to provide a suitable LO signal at 22 GHz to drive the balanced mixer. A unique feature of the design is that the Schottky diodes are FET compatible in that fabrication of the diodes as well as the FETs in the LO and IF amplifiers can be done on the same chip.

To address the cost goal for the monolithic receive module the basic fabrication approach is ion implantation into semi-insulating GaAs.

Design and Initial Fabrication of the Multi-Bit Phase Shifter - Figure S-3 shows a representative design of a 180° bit using series, 400 micron gatewidth FET switches. The series switch design reduces the required GaAs area over an equivalent shunt design (tested early in the program) by nearly a factor of two. It also introduces less parasitic reactance due to a more compact layout. Figure S-4 shows the actual 4-bit phase shifter fabricated by the SAG technique on the 0.15 mm thick GaAs wafer. The first three bits (180°, 90°, 45°) are switched line phase shifters and the last bit (22°) is a loaded line phase shifter.

Figure S-5 shows the measured differential insertion phase for the two states of the 180°bit across a 5 GHz band (27.5-32.5 GHz). Except for a constant offset of about 7°, (which can be easily compensated for in the final design) the measured curve follows exceptionally well the ideal time delay characteristic corresponding to 6.3°/GHz. The insertion loss measured on this first run of SAG phase shifters using series FETs is about 3.5-4 dB (excluding fixture loss). This is about 1 dB worse than the best SAG results obtained on earlier versions of the 180° bit using shunt FET switches.

Similar results were obtained on the 90° and 45° bits. It is expected, however, that with an optimized SAG process, an insertion loss of about 1.5 - 2 dB per bit will be achieved.

Design of a 100 Micron Gate-Width, Sub-Half-Micron Gate Length FET - To achieve the required noise performance of the 30 GHz LNA, a FET with a noise figure of not greater than 4 dB and with an associated gain of at least 6 dB must be developed. Based on extensive device design and circuit considerations, a 100 micron gate-width, and sub-half-micron gate length FET has been designed. Figure S-6 shows the computer generated layout of the 100 micron FET. The gate consists of two 50 micron fingers, each having a gate length of about 0.25 microns. This configuration was determined to be best suited for achieving low noise and high gain operation at 30 GHz and yet be consistent with impedance matching schemes which are realizable in monolithic form.

From an analysis of the specific fabrication related design parameters, an equivalent circuit shown in Figure S-7 was derived for the 100 micron FET. As shown in the figure, the predicted performance of the FET, as calculated from the equivalent circuit, includes a maximum available gain of 8 dB and a noise figure minimum of 2.5 dB at 32 GHz.

With the equivalent circuit established, a preliminary design of a five stage LNA was completed using the 100 micron FETs in a single-ended cascade as shown in Figure S-8. The computer optimized amplifier design predicts a gain of about 32.5 dB from 27-31 GHz.

Design and Initial Fabrication of the Gain Control Submodule - The gain control (GC) is accomplished by incorporating a two-stage dual gate FET amplifier and controlling the second gate voltage to vary the RF gain. A passive switched line attenuator follows the amplifier to add an additional attenuation bit. To date, work has been initiated on the development of the dual gate FET amplifier.

Figure S-9 shows the initial layout of the two-stage gain control amplifier, as generated by the CALMA computerized layout system. The dual gate FETs have 100 micron wide by 0.3 micron long gate stripes, and are based on the design and fabrication of the single gate 100 micron FETs used in the front-end LNA. On-chip silicon nitride capacitors are used to RF ground the second gate of each dual gate FET, yet permit application of a DC control voltage for the gain control function. All DC bias distribution and filtering is also included on the chip layout.

Finally, Figure S-10 shows the computed response of the two-stage gain control amplifier in its maximum gain state. The inset also shows the details of the circuit schematic whose corresponding layout is shown in the previous Figure, S-9. Over the band of interest the computed gain is 20.3 $\pm$ .2 dB.

Clearly, the designs developed during the first year are either starting points (as in the gain control submodule) or interim designs (as in the case of the phase shifter submodule) which will be updated as the experimental data base is obtained. Nevertheless, the results of the theoretical and computer calculations discussed above serve as guidelines for further device and circuit development which will lead to the final designs of the receiver submodules and the monolithic receive module.

The following Section II presents the details of the progress made during the first year of the program by task numbers.

Table S-1. NASA's Key Performance Goals

Design Parameter	Performance Goal
RF Band	27.5 - 30 GHz
IF Center Frequency	Between 4-8 GHz
Noise Figure at Room Temperature	$\leq$ 5 dB
RF/IF Gain	$\geq$ 30 dB at highest level of gain control
Gain Control	At least six levels; 30, 27, 24, 20, 17 dB and Off.
Phase Control	5 bits; each bit $\pm 3^{o}$ at band center
Module Power Consumption	250 mW in all states except OFF. In OFF state, 25 mW.
Phase and Gain Control	Operate on digital input.
Mechanical Design	Fully monolithic construction; compatible with 30 GHz spaceborne phased array applications.
Unit Cost	Less than $1000 (1980 dollars) in unit buys of 5000 or more

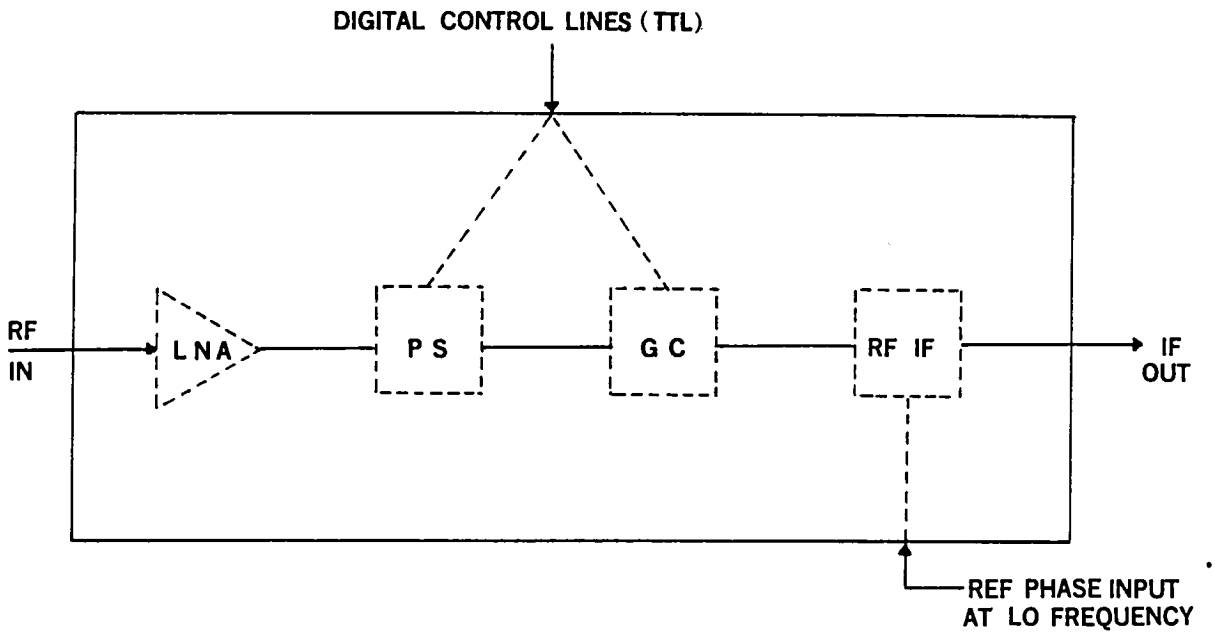


Figure S-1. Submodule Functions of Receive Module

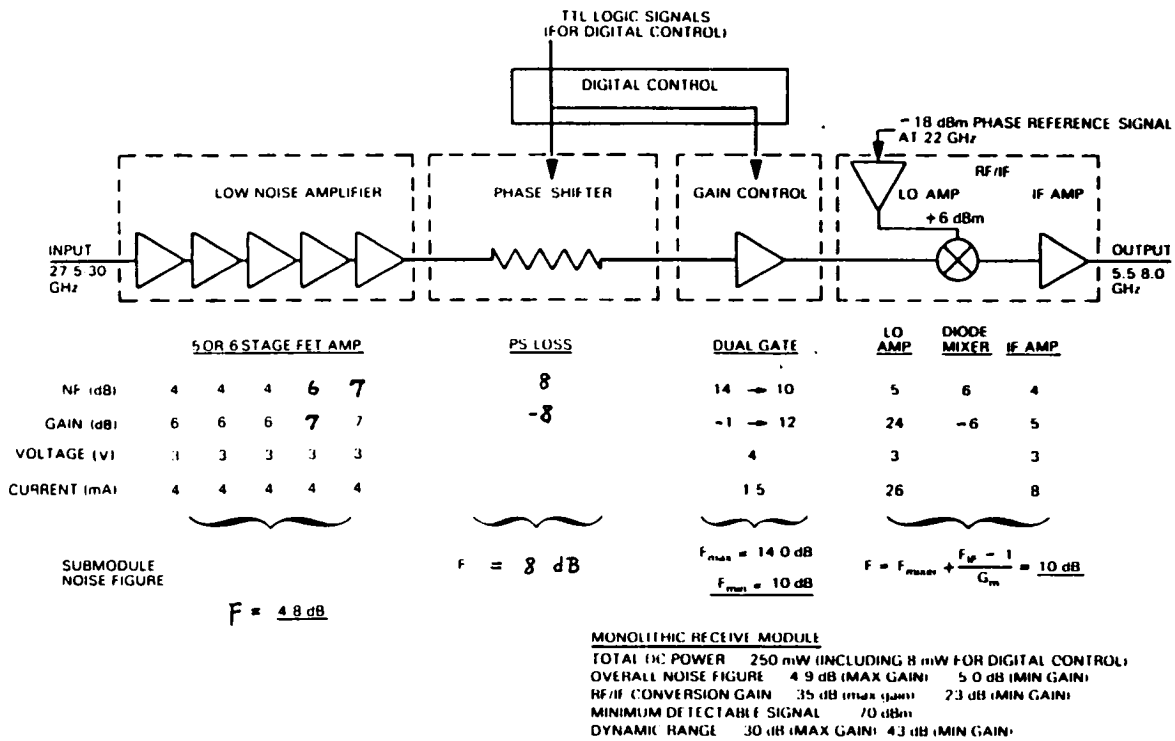


Figure S-2. Block Diagram of Overall Monolithic Receiver

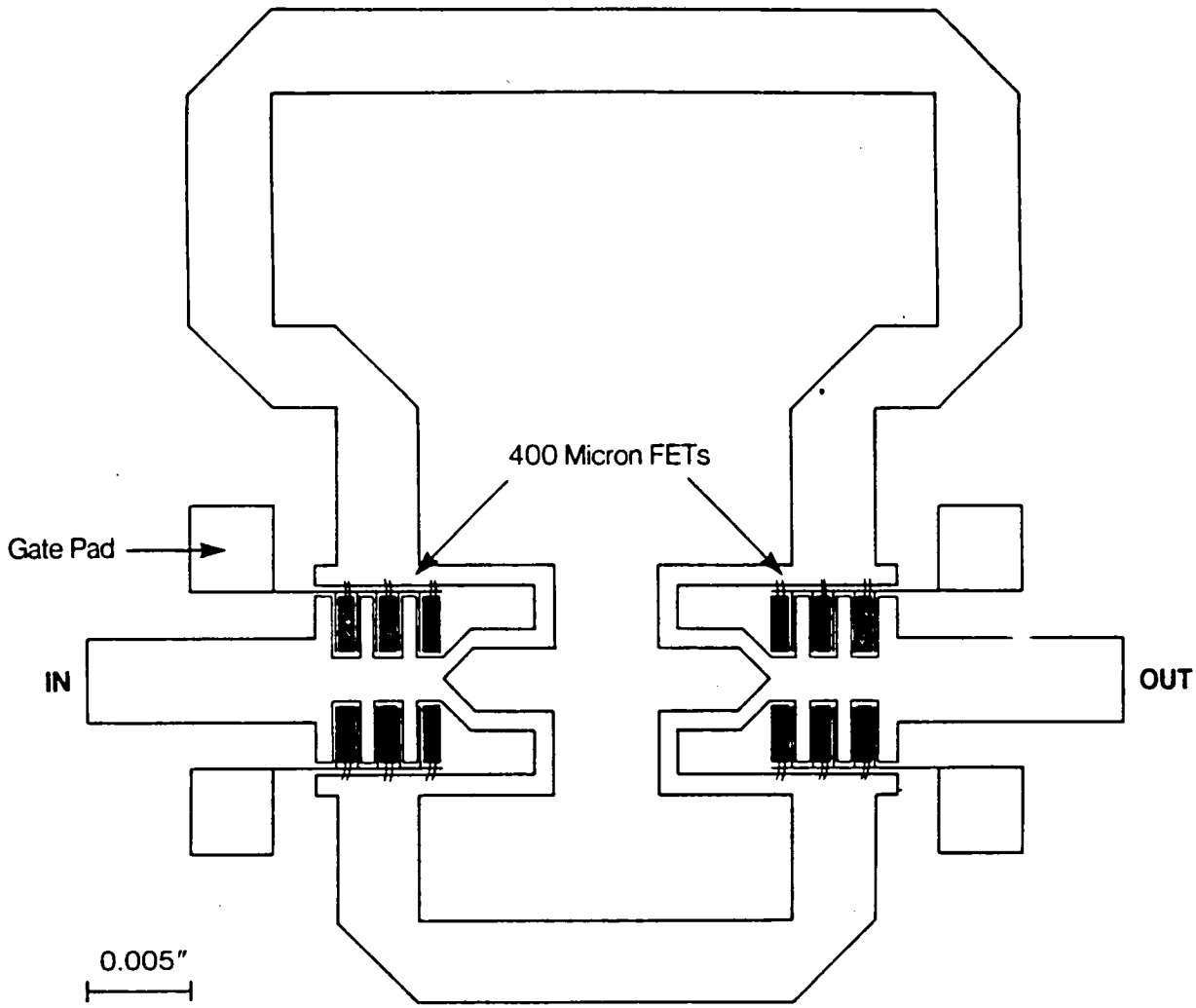
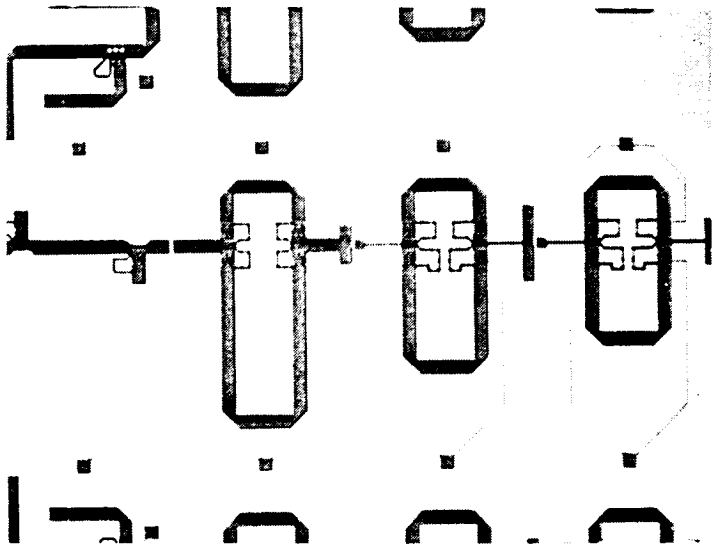
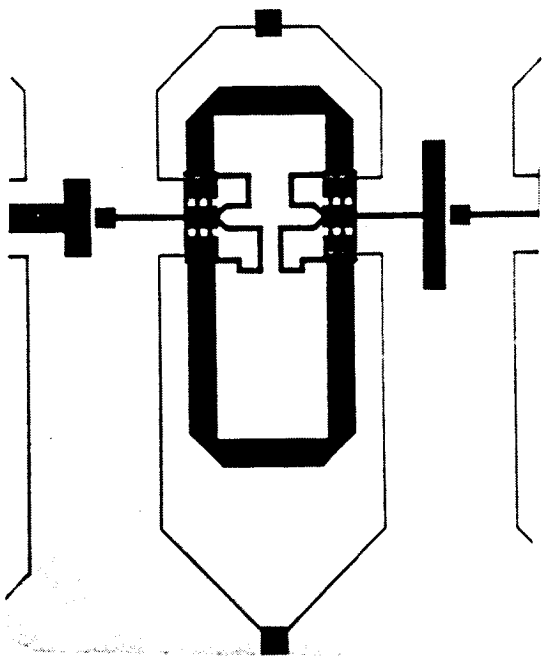


Figure S-3. Layout of 180° Bit Using Four Series FET Switches



(a)



(b)

Figure S-4. Photomicrographs of SAG Phase Shifter Circuits on a Processed Wafer
a) The four bit phase shifter (45°, 90°, 180°, 22°) using series FET switches
b) Enlarged view of 180°bit

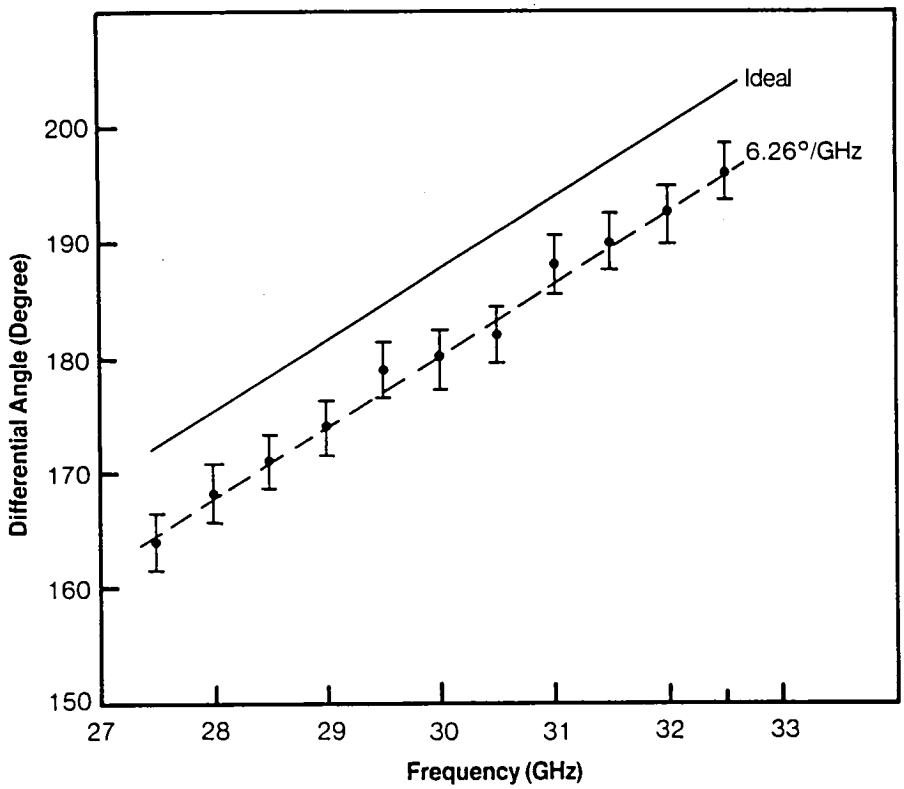


Figure S-5. Calculated and Measured Differential Phase Shift for 180° Phase Shifter

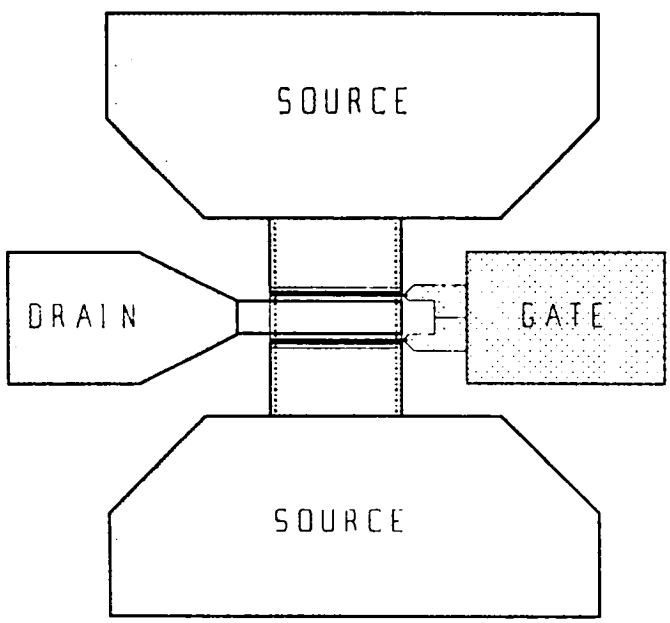
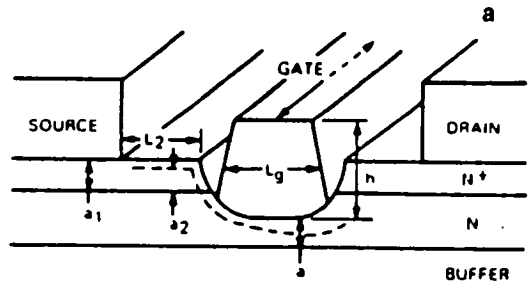
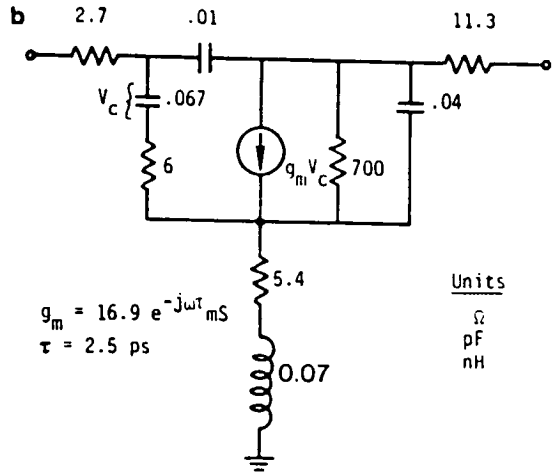


Figure S-6. CALMA Layout for 100 Micron Gate Width Low Noise FET



Gate length	L_g	= 0.25 microns
Unit gate width	w	= 50 microns
Channel thickness	a	= 0.15 microns
Doping density	N	= 2.5×10^{17}
Total gate width	Z	= 100 microns
Gate-source spacing	L_{sg}	= .75 microns
Gate metal thickness	h	= 0.5 microns
Specific contact resistance	r_c	= 10^{-6} ohm-cm^2
	a_1	= 0.22
	a_2	= 0.15
	N_1	= 2.5×10^{17}
	N_2	= 2.5×10^{17}

Calculated noise figure = 2.5 dB at 32 GHz



MAG = { 9.3 dB @ 27 GHz; 7.8 dB @ 33 GHz }

Figure S-7. Low Noise FET Design

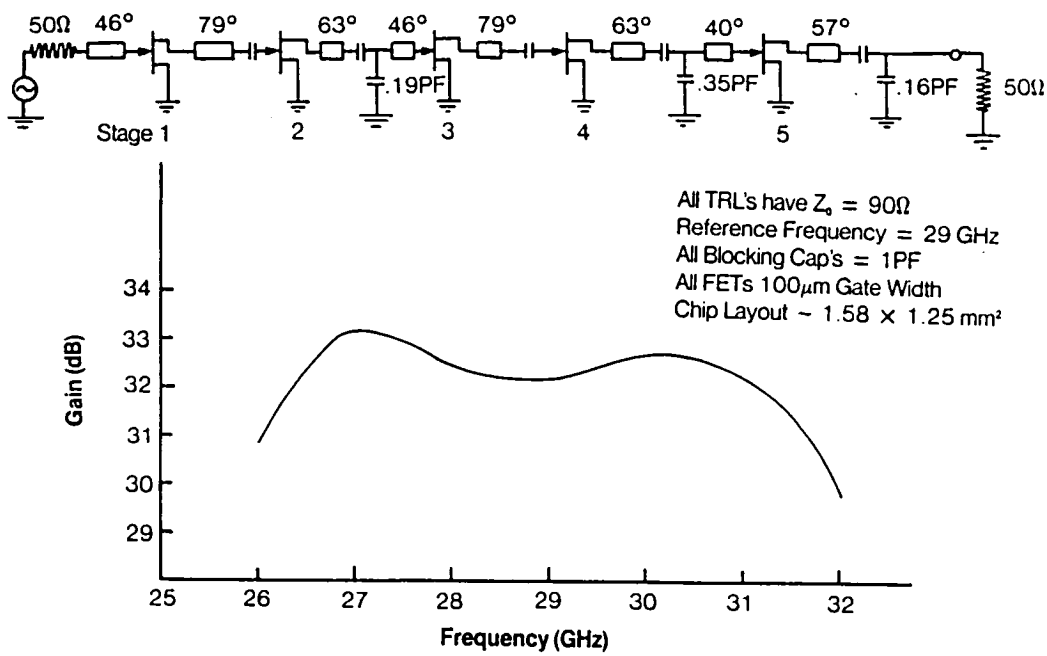


Figure S-8. Design for Monolithic Five-Stage Amplifier

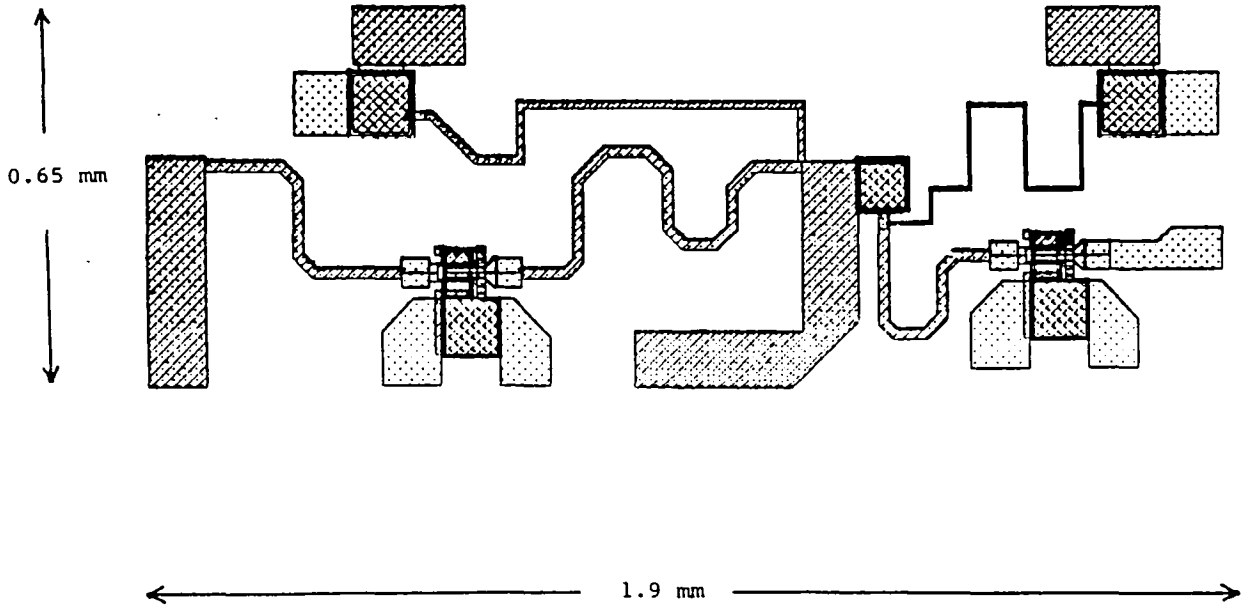


Figure S-9. CALMA Layout for First Two Stages of Gain Control Amplifier

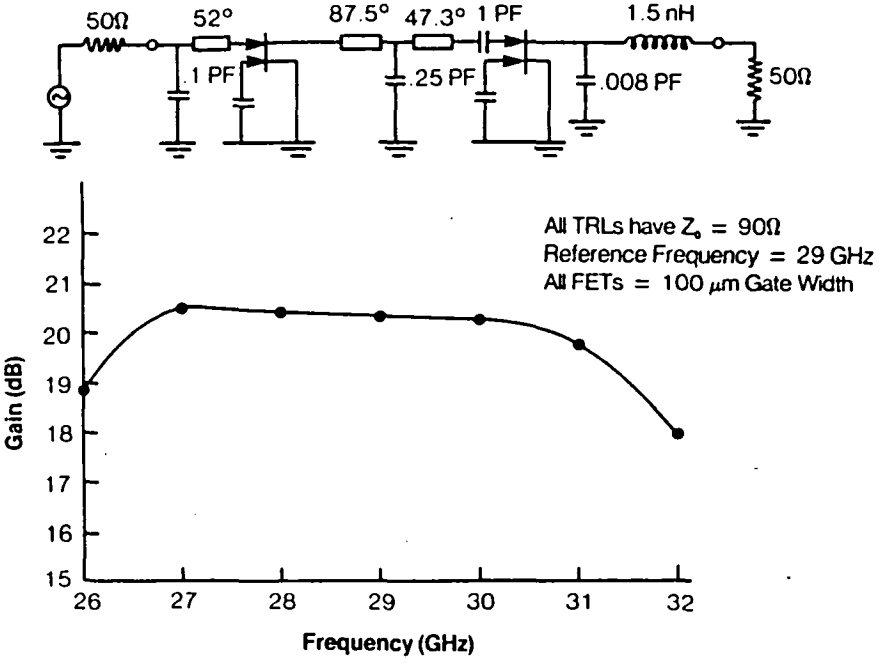


Figure S-10. Design for Monolithic 2-Stage Dual-Gate Amplifier

The reverse of this page is blank.

II. PROGRAM PROGRESS BY TASKS

The objective of the 4 year program is to develop a 30 GHz monolithic receive module for communication antenna feed array applications, and to deliver submodules and 30 GHz monolithic receive modules for experimental evaluation. Key performance and design goals are shown in Table 1.

1.0 Receive Module Design - Task I

A major portion of the first year's work was directed towards device and circuit design. This includes the detailed design of a 30 GHz monolithic receive module and four submodules. The submodules are a low noise amplifier (LNA), a phase shifter (PS), a gain control (GC), and an RF/IF submodule. The submodules are designed to function either independently or interconnected to form a complete functioning receive module. Accomplishments include the design of low noise 30 GHz FETs, switching FETs for phase shifter applications, amplifier and mixer designs as well as the design of switched line multi-bit phase shifters. To address the cost goal of less than $1000 per monolithic receive module, ion implantation is the baseline materials technology approach.

1.1 Circuit Design and Test Plan

The circuit design effort addressed the design of each submodule including interface specifications, as well as the overall receive module. Since the phase shifter submodules are the first to be scheduled for delivery in the

second year of the program, a more comprehensive design was completed for this submodule than, for example, for the RF/IF or LNA submodules which are scheduled for delivery towards the end of the third year of the program. In fact, two fabrication iterations of the phase shifter development were completed and evaluated during the first year. In addition, a test plan for testing each of the submodules as well as the receive module in accordance with the design parameters was also completed and approved by the NASA Technical Manager.

The following subsections deal with the specific circuit design details completed for Task I of the program.

1.1.1 Overall Receiver

The functional configuration for the monolithic receive module is shown in Figure 1 which also indicates nominal gains, noise figures, dc power consumption, and overall noise and gain performance for each submodule element and the complete receive module.

The first module function to be performed is low noise RF amplification, followed by RF phase shifting and gain control using submicron GaAs FETs. Frequency down-conversion and amplification at the IF is performed with a balanced mixer, which consists of a pair of monolithically integrated Schottky barrier diodes and a GaAs FET IF amplifier. The local oscillator signal is supplied by the LO amplifier, which raises the reference 22 GHz LO signal to +6 dBm. This LO power is sufficient to drive the pair of mixer diodes. To

maintain a low level of LO noise, the LO amplifier is designed for a 5 dB noise figure.

The phase shifter is a passive device and makes use of self-aligned gate (SAG) FETs to reduce resistive losses in the channels. Since each submodule must be capable of individual characterization and must therefore function as a separate unit, the gain control function is implemented at RF (in contrast to an approach that would realize part of the gain control function at IF).

The LNA consists of five FET stages with an overall noise figure of approximately 4.8 dB and a gain of 32 dB. The LNA gain is high enough that its noise figure determines to within 0.2 dB the noise figure of the total receive module. This is necessary due to the losses and noise figures associated with the phase shifter, gain control and RF/IF functions.

The gain control function follows the phase shifter because it is expected that the noise contribution of the gain control during minimum gain setting will be greater than that of the phase shifter. Specifically, the phase shifter is budgeted for 8 dB loss while the gain control amplifier during minimum gain settings has a 1 dB loss and a 14 dB noise figure. This approach is verified by Friis' formula (as well as common engineering sense), which shows that the overall noise figure of the two functions is lowest if the phase shifter is placed ahead of the gain control. It may be noted that the higher noise in the gain control is due primarily to the noisy dual-gate FETs during the lower levels of amplification.

The local oscillator frequency is at 22 GHz, with a resultant 5.5 to 8.0 GHz IF. With this choice of LO frequency the image band is in the range from 14.0 to 16.5 GHz. Good image rejection is achieved because the image band is located below the cutoff frequency of the WR-28 waveguide (f_{cutoff} = 21.1 GHz). In the case of a WR-28 waveguide input to the LNA (as during submodule RF testing), the image band will be automatically cut off by the waveguide. Furthermore, the image band is sufficiently removed from the passband of the LNA that a 30 dB or greater rejection will be accomplished due to the passband characteristics.

Submodule Integration and Chip Layout Design - The four submodules are interconnected on a single 3 x 9 mm^2 carrier plate to form the interconnected receive module, as depicted in Figure 2. Connections between the four chips are made with beam leads and thermocompression, or ultrasonic bonding.

For module and submodule testing the rf input interface is a WR-28 waveguide (26.5-40 GHz), while the LO input interface is a WR-42 waveguide (18-26 GHz). Fin-line waveguide-to-microstrip transitions are used at both the RF and LO interfaces. The IF output is taken off the chip by a 50 ohm microstrip line to an SMA output connector. Bias and TTL signals are routed from the chip to external connectors via appropriate printed circuit boards.

An important feature of the test fixture is that the chip is enclosed in a waveguide below cutoff. This provides inherent rf shielding and good isolation characteristics between the input and output as well as image band rejection.

The ultimate goal of the program is to achieve a fully monolithic 30 GHz receiver chip. This approach, if practical, will be implemented towards the end of the program and will be based on the designs and results of the interconnected module.

1.1.2 Phase Shifter Design

The phase shifter submodule makes use of switched transmission line lengths and passive FET switches. Two phase shifter circuit designs (as well as two fabrication approaches - discussed in Section II-1.2 and II-2.0) were tested. Initially a test circuit incorporating FET switches in shunt with the transmission lines were used. This design was employed at first because it was considered a more conservative approach and served as an experimental basis for the following design iterations. The second approach uses FET switches in series with the transmission lines. It has two advantages over the former design in that top-side RF grounding can be avoided and the microstrip circuit layout requires less GaAs area.

RF Losses - An important design consideration is the dissipative loss associated with the switches and the microstrip lines. As shown in the following, the dominant losses occur in the passive FETs.

Microstrip-line loss is calculated to be about 0.15 dB per wavelength at 30 GHz based on metal losses only and a gold thickness of 1.5 μm for a 50 Ω line on 0.2 mm thick semi-insulating GaAs [4].

For the switching FETs, however, RF losses are much greater and are primarily associated with the parasitic resistances of the device. Figure 3 shows simplified equivalent circuits for an ON and OFF FET, namely a single resistor for the ON (low impedance) state and a series resistor-capacitor combination for the OFF (high impedance) state [2-5]. The capacitor C_{off} is the total pinchoff capacitance between source and drain, and the resistor r_s is the total series residual resistance at pinchoff (undepleted channel resistance plus source and drain contact resistance). To increase the RF impedance of the OFF state, an inductor L parallel resonates the RC combination. For this case, the effective RF OFF resistance at resonance, R_{off}, is closely approximated by $R_{off} = Q^2_c r_s = (\omega r_s C)^{-2} r_s = (\ C)^{-2} r_s^{-1}$. Note that the ratio R_{off}/R_{on} is to first order, just the figure of merit $\hat{Q}$ as defined by Kurokawa and Schlosser for a switching device switching between two impedance states Z_1 and Z_2.

It can be shown that

$$\hat{Q}^2 \cong (R_{on} r_s)^{-1} \ (\omega C)^{-2} = R_{off}/R_{on} \quad [2, 3]$$

It is clear that the figure of merit degrades with frequency and has smaller values at millimeter-wave frequencies than at lower microwave frequencies. To maintain the figure of merit high it is essential to reduce R_{on} and r_s (and C if possible).

A specific example of an ideal RF switch incorporating conventional power FETs

for the switching devices can illustrate the losses incurred at 30 GHz. For a typical 300 μm power FET, R_{on} = 11-14Ω and with C = 0.07 pF and r_s = 5Ω, R_{off} is about 1000Ω at 30 GHz. By choosing these ON and OFF resistance values and using them in an ideal SPDT switch configuration as shown in the inset of Figure 4, we can calculate the ideal insertion loss and isolation of a single switch at center frequency. Furthermore, by scaling R_{on}, r_s, and C for other gate widths, an estimate can be made of the best compromise between isolation and insertion loss. Note that this leaves the figure of merit $\hat{Q}$ invariant. These considerations are summarized in Figure 4 where the insertion loss and isolation at 30 GHz are calculated as a function of gate width for two different $\hat{Q}$ values. Note that for the dashed curves which represent a reduction in R_{on} and r_s (14Ω to 4.7Ω and 5Ω to 2.4Ω, respectively), the loss is reduced by 0.6 dB at a gate width of 300 μm, for a single SPDT switch. For a four-bit switched line phase shifter this amounts to nearly 5 dB less insertion loss. As shown in Section II-1.2.1 such reductions in the parasitic resistance are possible using the self-aligned fabrication process.

First Design: 180° - 1 Bit Phase Shifter (Shunt FETs) - Figure 5 shows the chip layout for the 180° bit. Four switching FETs are used to RF switch between two microstrip lines whose differential electrical length is equal to 180° at center frequency. The FETs are passive in the sense that no dc bias is applied to the drain and only a switching voltage (0,-6V) is used at the gate [4-6]. The circuit utilizes a pair of SPDT switches realized by four, 300 μm gate width FETs in shunt across the 50Ω transmission lines with each FET located at a distance of $\lambda g/4$ (0.8 mm at 30 GHz on GaAs) from either the

input or output T-junction.

The circuit layout is conservative in that the area required (chip dimensions are 3 x 2.67 x 0.2 mm^3) has not been minimized. This was done to ensure that the coupling between adjacent sections of transmission lines would be negligible thereby facilitating evaluation of initial RF performance results. The 0.2 mm substrate thickness was chosen as a compromise between increased microstrip transmission line loss and extraneous capacitive parasitics (thinner substrate), and increased circuit layout dimensions (thicker substrate). Pads are provided at the edge of the chip for grounding. For these tests, ground connection is accomplished by a series resonant circuit consisting of an external 0.1 pF capacitor (bottom plate soldered to ground) and a mesh wire inductor connecting from the capacitor top plate to the grounding pad on the chip. To increase the high impedance state (V=-6V), a short section of line printed on the chip is used to resonate the pinchoff capacitance between drain and source ($C \cong 0.07$ pF) for each FET. High impedance to the gate terminal is provided by bonding wire inductance.

Second Design: Multi-Bit Phase Shifter (Series FETs) - To improve the expected performance of our multi-bit phase shifter, a series switch design was implemented. A representative layout for a 180° bit is shown in Figure 6. Four, 400 micron gatewidth unbiased FETs with five 80 micron fingers per FET, are used in the series configuration. The area per bit is almost halved from that of a shunt design. Figure 7 shows the calculated differential phase. Over a 4 GHz band the differential phase characteristic is within 2° of the ideal curve. For an assumed ON resistance of 9Ω and a pinch-off residual

series resistance and capacitance of 4.5 Ω and .09 pF respectively, the loss is about 2.3 dB per bit.

The design of a 3-bit phase shifter using series FET switches is similar to the 180° bit except that differential line lengths of 45°, 90°, and 180° are used. To improve insertion loss and phase tracking accuracy over the band, impedance matching elements (a short section of high impedance line and a shunt stub) are used for the 45° and 90° bits. All three bits use exclusively series switches. The layout for all 3-bits is realized in an area of 2.5 x 4.1 mm^2.

Figure 8 shows the calculated differential insertion phase results for all eight states over the 25 to 33 GHz frequency band. The calculated values (shown as discrete points) are shown relative to the ideal characteristics, i.e., time delays corresponding to the various phase states. The results show that over the band of interest the calculated values are within 2 or 3 degrees of the ideal curve. For these calculations the computer program COMPACT was used. The circuit model included 12 switching FETs, interconnecting transmission lines and matching networks. For the OFF state, the FET switches were represented by a 4.5Ω resistor in series with a pinch-off capacitance of .09 pF, and the combination parallel resonated by a high impedance 90 Ω transmission line. The ON states were modeled by a simple series resistance of 9Ω (and the 90Ω transmission line in parallel).

Figure 9 shows the "envelope" for the insertion loss for all eight states. All losses in the switching FETs and losses in the transmission lines were

included in the calculations. Over the band of interest the insertion loss is about 6.5 to 7 dB, with a spread of about 0.5 to .75 dB.

1.1.3 Gain Control

The gain control submodule is required to provide five levels of RF to IF gain (30, 27, 24, 20 and 17 dB) and an off state. To maintain the noise figure of the receive module at 5 dB, the worst case noise figure for the gain control submodule is budgeted at 14 dB.

Two critical requirements of this submodule dictate to a large extent its design: the requirement for a 1 dB attenuation state with a noise figure of 14 dB or better, and a +12 dB gain state with an allowable insertion phase change of no more than $\pm 5^{o}$ over the full 13 dB gain range. Also, the upper gain level is limited to a maximum of +12 dB to ensure a 30 dB dynamic range for the overall receiver. Higher gains and subsequent higher drive levels would result in overdriving the mixer, thus reducing the 1 dB gain compression point of the receive module.

The requirements cited above will be met with dual-gate FET amplifiers by controlling the second gate voltage. The dual gate FET with a 0.5 micron gate length is expected to provide a maximum gain of about 10 dB at 30 GHz. By controlling the second gate voltage, the gain can be adjusted at least over a 20 dB dynamic range to an attenuation state of -10 dB.

Two problems arise in using only one dual-gate device for gain control: noise and phase shift. Liechti [7] and others have shown that the noise figure, although not much degraded from a single gate device during maximum gain, degrades drastically as the device is driven toward an attenuation state. For example, at 10 GHz, Liechti shows an 11 dB degradation from a 4.1 dB noise figure at an associated gain of 12.8 dB, to a 15 dB noise figure at a gain of 2 dB. The insertion phase shift, as a function of the second gate voltage, also varies considerably as the dual-gate FET is brought from a gain state to an attenuation state. Thus, a single amplifier, although having considerably greater than 13 dB dynamic range in gain, is inadequate from a noise and phase shift point of view.

To overcome these deficiencies, a two-stage dual-gate FET amplifier, followed by a variable passive attenuator, is used for the gain control submodule, as shown in Figure 10. The first stage has gain states of 3 and 6 dB, while the second stage amplifier has three gain states of 2, 5 and 8 dB. These states are achieved by applying proper control voltages to the second gate. The switched attenuator makes use of the passive SPDT switch (described in earlier sections) to form two switchable paths of unequal loss. The majority of the loss in the path of minimum attenuation (-2 dB path) resides in the series unbiased FETs. In the second path, a 4 dB increase in attenuation is required. This can be realized easily by incorporating either a thin film series resistor evaporated onto the substrate for a section of the 50 ohm line, or high resistivity selective ion implants can be incorporated beneath the microstrip line to form a lossy section of line. Note that the tolerance of the loss is not very critical, i.e., on the order of 1 dB, since changes of

this magnitude can be compensated by the dual gate amplifiers. Some unwanted phase shift in the dual gate amplifiers can likewise be compensated for by the switched attenuation, by altering the length of one of the paths.

Preliminary Design - For initial development, a two-stage dual-gate FET amplifier design is employed. The design is based on the 100 micron gate width FET discussed in Section II-1.2.2. A cascode connection of two such FETs are used for the equivalent circuit of a dual gate FET. (Common source first stage, common gate second stage [7]).

Figure 11 shows the circuit schematic and the computer optimized gain characteristic for the two stage dual gate amplifier. From 27 to 30 GHz the gain is 20.4 $\pm$ 0.1 dB. The input and interstage networks are on-chip while the output impedance matching network includes a bond wire inductor. This last feature is incorporated to facilitate initial rf circuit evaluation. Development and testing of the passive switched attenuator portion of the gain control is being done in parallel with the initial phase shifter development discussed earlier. Subsequent iterations of the gain control will include the passive attenuator on the same chip.

1.1.4 RF/IF Submodule

The RF/IF submodule has three functions:

- o Convert the 27.5 to 30 GHz input RF signal to the IF (5.5 GHz) in a mixer.
- o Amplify an external reference signal to provide a local oscillator

input (22 GHz) to the mixer.

o Amplify and buffer the mixer IF output to drive the IF amplifiers.

The technical approaches for achieving these functions are discussed below.

Balanced Schottky Diode Mixer - Our baseline mixer design approach will be the balanced Schottky diode mixer with a rat race hybrid which is shown integrated with the other elements of the RF/IF submodule in Figure 12. The input signal, inserted on the right side of the chip, is shifted in phase by 90° to one mixer diode, and 270° to the other. The diodes are connected 180° out of phase to suppress noise from the local oscillator amplifier and reference signal, while combining the IF signals in phase. The diodes are connected to IF frequency and dc ground by vias through the substrate; open circuited stubs are used to ensure a high quality ground for the signal and local oscillator.

The mixer employs a pair of surface oriented Schottky barrier diodes so that fabrication is compatible with that of the FETs. Efforts to develop such diodes have been successful in the past. The best diodes, using thick active layers, have cutoff frequencies greater than 200 GHz [8, 9]. Recent results [9] were obtained using many small diodes in parallel to lower the overall series resistance. The diodes to be used in this program will be an extension of these techniques as indicated in Figure 13. By decreasing the capacitance of the individual diodes while maintaining an approximately constant value of series resistance these methods should be useful at 30 GHz.

22 GHz LO Amplifier - The requirements for the 22 GHz local oscillator include a gain of 24 dB and a noise figure of 5 dB. Other than frequency, the

requirements are similar to the RF low noise amplifier used for the "front end" of the receiver. Consequently the 100 micron gate width FETs discussed in Section II-1.2.2 which are designed for the RF LNA are also used for the LO amplifier.

To assess the noise figure and gain trade-offs for the 100 micron FET at 22 GHz, the noise figure and gain circles were calculated and plotted on the Smith Chart as shown in Figure 14. The 3 stage amplifier shown in Figure 1 and 15 is designed to achieve the required 24 dB total gain and yet realize the source impedance (e.g., $z_s = .6 + j\ 1.2$) as seen by the first stage especially, to be in the region of minimum noise using Figure 14 as a guideline.

The theoretical calculation of the total gain over the frequency range from 20 GHz to 24 GHz is shown in Figure 15, and is about 26 dB. The overall gain flatness is within 0.3 dB, and the layout estimated area about 2.44 x .53 mm^2.

IF Amplifier - The IF amplifier is primarily needed to buffer the mixer output to drive lower impedance transmission lines. The requirements include 5 dB gain from 5.5 to 8 GHz. A preliminary design using a 150 micron FET equivalent circuit in a single stage common source configuration was developed. The circuit design makes use of the so-called "lossy" match technique, i.e., frequency dependent resistive loss is used to obtain flat gain over a 60% fractional bandwidth. A gain of about 6 dB is achieved from 5 to 9 GHz.

1.1.5 30 GHz Low Noise Amplifier Submodule

Five stages of GaAs FET amplification are used in the LNA. The first three stages are designed for a noise figure of 4 dB and an associated gain of 6 dB, while the last two stages are budgeted for slightly higher gains and noise figures as was shown previously in Figure 1. The number of LNA stages is chosen large enough to achieve sufficient front end gain to minimize the effects of noise figure contributions and losses of following submodule components on the total noise figure of the receive module, which is to be 5 dB.

Because of the low dc power consumption budget (3V and 20 mA for the complete LNA) and the theoretically predicted improvement of device noise figure with smaller gate widths, the FETs used in the LNA have gate widths of 100 microns (and sub-half-micron gate lengths as discussed in Section II-1.2.2). Although even smaller gate widths are desirable from an efficiency and noise figure point of view, a lower limit on gate width exists because of impedance matching considerations. In particular, too small a gate width results in high impedance levels which are difficult to match to 50 ohms (especially for the FET output circuit). This is due to design constraints imposed by the physical limitations of monolithically fabricated reactive circuit elements. The most direct consequence of this difficulty is bandwidth reduction due to large impedance transformation ratios.

An initial design for the five stage amplifier is shown in Figure 16. The FET equivalent circuit discussed in Section II-1.2.2 is used for the FET devices.

As shown in the figure the gain is the required 32 dB ± .5 dB from 27 to 31 GHz. Input impedance matching takes into account the gain/noise figure trade-off (see Section II-1.2.2) especially for the first stage. As shown in the figure the design utilizes similar circuit elements which are relatively easy to realize monolithically on a 0.15 mm thick substrate.

It should be noted that the design activity and resulting circuit schematics presented above are strictly starting points for the development of the various receiver functions. They serve to define the design methodology for subsequent design iterations. As experimental data is obtained the various equivalent circuits will be up-dated and revised for final design implementation.

1.2 Device Design

During the first year device design centered around the low noise 100 micron gate width FET, and the 400 micron switching FET for implementation in the passive phase shifters. For the switching FET the primary goal is to reduce the channel resistance and resistive parasitics of the device to minimize the insertion loss of the 30 GHz SPDT switches used in the switched line phase shifters. For the 100 micron FETs the goal is to achieve a device performance of at least 4 dB noise figure with an associated gain of 6 dB at 30 GHz. As shown in this section it is expected that sub-half-micron gate lengths will be required.

1.2.1 SAG FET for Phase Shifter

By using a n^+ implant self-aligned FET [10] switch in the phase shifters two objectives can be achieved: First, realization of a low value of ON resistance for minimizing insertion loss, and second, low power consumption for minimizing the overall DC power consumption of the receive module. The latter objective is met because the switching FETs are basically "unbiased" FETs, where only a control voltage is applied to the gate electrodes.

The principle factor limiting the reduction of the "ON" resistance of the self-aligned structure is the sheet resistance of the channel. The calculated sheet resistance under the gate as a function of gate-to-channel voltage for a relatively heavy implant of 5×10^{12} silicon atoms/cm^2 is shown in Figure 17. This calculation includes the effect of the varying depletion depth under the gate. The maximum electric field in the device for complete depletion (pinchoff) is approximately 480Kv/cm, assuming a Gaussian doping profile.

The sheet resistance shown was calculated using a mobility of 4000 cm^2/v-sec independent of doping. Increasing the implant energy decreases the channel sheet resistance at the price of a larger pinchoff voltage. Some reduction can be achieved by forward biasing the gate but the sheet resistance valves shown in Figure 17 are probably close to the best which can be achieved.

Combining the channel resistance with ohmic contacts (line resistance) and self-aligned n^+ region the source-drain resistance shown in Figure 18 is calculated. The resistance given in this figure is conservative in that n^+ sheet resistances of 100 ohms/square and line resistances less than 0.1 ohm-mm

are expected to be achieved in an optimum SAG process. For example, with a 5 source-drain resistance (the ON state) it is expected that the insertion loss per bit should be between 1.5 and 2 dB.

1.2.2 100 Micron Low Noise FET

The 100 micron gate width .25 micron gate length low noise FET is the critical element in the low noise receiver front end. This section describes the design of the 100 micron gate width FET. The description of the FET design is separated into three subsections: 1) Rationale for Low Noise FET Design which describes the basic reasoning used to determine the requirement for a .25 micron gate length and 100 micron gate width, 2) Low Noise FET Equivalent Circuit which describes the calculations used to arrive at an equivalent circuit for the FET and 3) Gain and Noise Circle Calculations which describes the calculation of tradeoffs in circuit matching for gain and noise figure based on the equivalent circuit model.

Rationale for Low Noise FET Design - The FET required for use in the low noise amplifier must have a 4.0 dB noise figure with a 6 dB associated gain per stage to achieve overall receive module noise figure of 5 dB.

The device design must consider material and geometric parameters that impact the following requirements:

- o Low noise figure
- o High frequency gain
- o Low power consumption

Device design requirements for a low noise figure can be identified from Fukui's noise equation [11, 12] which is known to give a good relationship between device parameters and an experimentally measured noise figure.

$$F = 10 \log_{10} \left\{ 1 + kf \left(\frac{NL^5}{a} \right)^{1/6} \left[\frac{3.3\rho w^2}{hL} + 0.6w^2 \left(\frac{\rho f}{hL} \right)^{1/2} \right. \right. \\ \left. \left. \frac{1.8L_{sg}}{N_2 a_2} + \left(\frac{0.18 r_c}{N_1 a_1} \right)^{1/2} \right]^{1/2} \right\} \tag{1}$$

where

F = noise figure (dB)

L = gate length (microns)

k = noise coefficient dependent on material (typically 0.033 to 0.040)

L_{sg} = gate to source spacing (microns)

r_c = specific contact resistance (10^{-6} ohm-cm^2)

ρ = gate metal resistivity (10^{-6} ohm-cm^2)

w = unit gate width (mm)

a = channel thickness beneath the gate (microns)

a_1 = channel thickness beneath the source (microns)

a_2 = channel thickness in region 2 (microns)

N = carrier concentration in the active channel (10^{16}cm^{-3})

N_1 = effective carrier concentration beneath the source (10^{16}cm^{-3})

N_2 = effective carrier concentration in region 2 (10^{16}cm^{-3})

h = gate metal thickness (microns)

f = frequency (GHz)

The various thickness regions (a_1, a_2), identified in Figure 19 are due to recess etching. Surface depletion must be taken into account when determining a_2. The first two terms in brackets in equation (1) are due to the gate metal resistance. The first term is the dc gate resistance; the second term is due to skin effect. Term three is due to the material resistance in region two. The fourth term is the contact resistance. Equation (1) can also be written

$$F = 10 \log_{10} [1 + C(R_S + R_g)^{1/2}] \quad (2)$$

where R_S is the source resistance, R_g is the gate resistance, and C is a constant dependent on material, frequency, gate length, doping density, and channel layer thickness.

Examining equation (1) shows that the device requirements for a low noise figure are:

- o Gate length should be as short as possible.
- o Gate metal resistance should be low so $R_g \leq R_S$. This implies low metal resistivity and thick gate metal.
- o Source resistance should be as low as possible. This implies low contact resistance and increased doping density and thickness in the regions between the source and gate.

Requirements for high gain can be identified from the equation for the unilateral gain, G_u, of a FET [13].

$$G_u = \frac{[g_m/(2\pi C_{gs})]^2}{(2f)^2} \cdot \frac{1}{[G_{ds}(R_g+R_s)+2\pi f_t R_g C_{dg}]} \tag{3}$$

where

g_m = transconductance

C_{gs} = gate-source capacitance

C_{dg} = drain-gate capacitance

G_{ds} = output conductance

f_t = unity current gain frequency $g_m/(2\pi C_{gs})$

The transconductance and gate-source capacitance can be expressed in terms of material and geometric parameters.

So that

$$\frac{g_m}{2\pi C_{gs}} = \frac{V_s}{2\pi L}$$

where

v_s = saturation velocity of electrons in the channel

and

$$G_u = \frac{V_s^2}{16\pi^2 L^2} \left[\frac{1}{G_{ds}(R_g+R_s)+\frac{V_s}{L}R_g C_{dg}}\right] \tag{4}$$

Equation (4) indicates that some of the requirements for high gain are the same as for a low noise figure, i.e., gate length should be as short as possible and gate and source resistances should be low. In addition, both G_{ds} and C_{dg} should be made as low as possible.

Power consumption is another consideration in the FET design for this application. The power consumption is given by the product of the drain source voltage and the drain current. A reasonable value for the drain source voltage is 3 volts. If the drain current is 4 milliamps, the I_{dss} of the FET will be 10 times the low noise bias value, or 40 milliamps. The I_{dss} is related to material and geometric parameters by

$$I_{dss} \leq q\, N\, v_s\, Z(a-d)$$

when the FET operates in the velocity saturated mode.

where

d = zero bias depletion width = 0.067 micron

a = channel thickness = 0.15 microns

$v_s = 10^7$ cm/sec

$N = 2.5 \times 10^{17}$ cm^{-3}

So the total gate width Z must be:

$$Z \leq 120 \text{ microns}$$

Since 120 microns is too long for a unit gate width, the gate will be broken up into two sections. We use a 100 micron total gate width, with a unit gate width of 50 microns. This gate width will give a reasonable impedance for

matching networks.

Combining the requirements for low noise, high gain and low power consumption gives the FET constraints that impact the final design. The gain is increased and the noise figure is reduced by minimizing the gate length.

The factors which limit the amount of gate length reduction are:

- o E-beam lithography processing limits for reproducibility.
- o Channel thickness and doping control implied by channel dimensions for best performance.

Consideration of these factors with present processing technology makes a 0.25 micron gate, a channel layer 0.15 micron thick, and 2.5×10^{17} cm^{-3} doping reasonable choices for the device structure.

Gain and noise figure are also enhanced by minimizing the gate and source resistance. The gate resistance can be reduced by using increased metal thickness and low resistance metals to fabricate the gate. The source resistance is most strongly affected by the doping between the source and gate, the geometry of this region and ohmic contact quality. Initially, we will use a source-gate spacing of 1 micron to ease alignment requirements, but it is expected that advances in technology will permit reduction of this dimension. Other techniques which will be employed to minimize the source resistance are (1) recessed gate, (2) optimized doping profiles and (3) n^+ surface layers with advanced contacting metallurgy for optimum ohmic contact characteristics.

FET design parameters and a calculated noise figure based on this discussion are given in Table 2.

A final design consideration is the output conductance and drain gate capacitance of the FET. Although a formula for the output conductance was developed by Pucel, Haus, and Statz [14], it predicts a G_{ds} much lower than is actually measured on FETs. It is believed this is due to substrate conduction [15, 16] near the high field region. In an ion implanted FET, the output conductance is undoubtedly influenced by implant distribution and the substrate quality, although the output conductance can be decreased by the use of an $Al_xGa_{1-x}As$ buffer layer [16] or an insulating region between the channel layer and substrate [17]. We do not believe the increase in processing complexity is warranted.

FET performance is influenced by a complex relationship between equivalent circuit element values that are affected by materials and processing limitations. Therefore, the final FET design will be achieved through experimental measurements and computer aided modeling.

Low Noise FET Equivalent Circuit - As discussed in the preceeding section, a 100 micron gate width FET with a .25 micron gate length is required to meet the gain and noise figure goals for the rf receiver. To design the multistage amplifier an equivalent circuit model for the FET is needed. This section will describe the equivalent circuit model for the FET and the procedure used to arrive at the element values used in the model.

The equivalent circuit model for the FET is shown in Figure 19b. Some of the element values are calculated from theory while others are determined by measurement or scaling. The FET gate width is chosen to be 100 microns to ease input matching requirements and minimize the effects of phase shift of the 30 GHz input signal along the gate.

The circuit elements that can be calculated from material parameters and device geometry are: the gate resistance R_g, the input capacitance C_{gs}, the transconductance g_m, the source resistance R_s, the drain resistance R_c, and the phase shift factor τ. These element values were calculated from the following equations:

$$R_g = \frac{\rho w}{3n^2 hL} = 2.7\Omega$$

$$R_s = R_c + R_{sg} = 5.4\Omega$$

$$R_c = \frac{\sqrt{\rho_{s1}\rho_c}}{Z} = 1.8\Omega$$

$$R_{sg} = \frac{\rho_{s2} L_{sg}}{Z} = 3.6\Omega$$

ρ_{S1} = sheet resistance of semiconductor material beneath the ohmic

$$= \frac{1}{Nq\,\mu a_1} = 325 \text{ ohms per square}$$

q = electron charge = 1.6×10^{-19} coulombs

μ = electron mobility = 3500 cm/v-sec

ρ_{S2} = sheet resistance of material in source-gate opening excluding surface depleted region = $\frac{1}{Nq\,\mu a_2}$ = 476 ohms per square

$$R_d = R_c + R_{dg} = 11.3 \text{ ohms}$$

$$R_c = \frac{\sqrt{\rho_{S1}\rho_c}}{Z} = 1.8 \text{ ohms}$$

$$R_{dg} = \frac{\rho_{S2} L_{dg}}{Z} = 9.5 \text{ ohms}$$

L_{dg} = 2 microns

$$C_{gs} = \frac{1}{\sqrt{2}} \; LZ \left(\frac{\epsilon_o \epsilon_r qN}{2(\phi_{bi} - Vg)}\right)^{1/2}$$

$\epsilon_o = 8.854 \times 10^{-14}$ fd/cm

$\epsilon_r = 12.5$

ϕ_{bi} = built in potential = .8V

V_g = applied gate voltage = 0V

L = L_{eff} = effective gate length = physical gate length plus active layer thickness to correct for fringing capacitance = 0.4 microns

$$g_m = V_S Z \left[\frac{qN\epsilon_o\epsilon_r}{2(\phi_{bi}-V_g)}\right] = 16.9 \text{ mmho}$$

V_S = Saturation velocity = 10^7 cm/sec

$$\tau = \frac{L}{V_s} = 2.5 \text{ psec}$$

The remaining equivalent circuit elements: the drain-gate capacitance C_{dg}, the drain-source capacitance C_{ds}, the resistance Ri and the output resistance Ro cannot be accurately modeled. Our approach is to use existing publications on quarter micron gate FETs [18-20] together with COMPACT analysis of the equivalent circuit to estimate values for these elements. For these elements we have chosen the values:

R_o = 700 ohms

C_{dg} = .01 pf

C_{ds} = .04 pf

R_i = 6 ohms

The complete equivalent circuit together with a table of critical FET parameters are given in Figure 19. The calculated maximum available gain is 8 dB at 32 GHz. Fukui's noise equation predicts a noise figure of 2.5 dB for the FET model. All design equations are based on a uniform doping model which is typical for FETs made with VPE material. The use of ion implanted material should not significantly change these values.

Gain and Noise Circle Calculations - Using COMPACT the S parameters for the FET equivalent circuit were calculated as given in Table 3. Noise parameters for the FET can be calculated according to a paper by Fukui [21, 22] using:

$$F_{min} = 1 + .016\ f\ C_{gs}\ \sqrt{\frac{R_g + R_s}{g_m}}$$

$$R_n = 0.8/g_m$$

$$X_{op} = 160/(f\ C_{gs})$$

$$R_{op} = 2.2\ \left[\frac{1}{4g_m} + R_g + R_s\right]$$

where

f = frequency in GHz

C_{gs} = capacitance in pf

g_m = transconductance in ohms

R_g = gate resistance in ohms

R_s = source resistance in ohms

Fukui's model, on which these calculations are based, does not consider the effect of source inductance or gate drain capacitance on high frequency noise figure. The effect of the feedback elements on noise were calculated using a program for the HP41C written by Suter [23]. Gain circles are calculated using another HP41C program, GCIR.

Using these HP41C programs the gain and noise circles for the FET input and output planes can be calculated. For the Fukui noise analysis the equivalent circuit does not include C_{dg} or L_s. By using the S parameters for the model with no C_{dg} or L_s (Table 4a) with no C_{dg} but with L_s, (Table 4b), and with both L_s and C_{dg} (Table 5), the noise circles for the input plane can be calculated as shown in Figures 20 and 21. These figures illustrate the tradeoff between gain and noise figure. The noise figure reduction for the case including C_{dg} and L_s may be in error since the calculation model assumes C_{dg} is connected in shunt from the input terminal to the output terminal. In any case, the modelling gives a good indication of the gain-noise figure tradeoff since there is not a large change in the gain and noise figure circles. In a similar way the gain circles for the FET output plane are calculated and the results are shown in Figure 22.

A final item of interest that can be calculated is the variation of gain and

noise figure with changes in source and gate resistance. This type of calculation has been used by Yamasaki and Schellenberg [24] to show that the gate resistance has a stronger influence on high frequency gain that the source resistance. Since the maximum available gain G_{max} is affected by stability considerations they use the unilateral gain, G_u, for comparison. We have calculated the effect of gate and source resistance on maximum available gain and noise figure and plotted the results as shown in Figures 23 and 24. The maximum available gain was calculated using COMPACT and the noise figure using Fukui's noise equation. These graphs indicate that both source and gate resistances have a significant affect on gain and noise figure. High source resistance can cause the FET to become unstable. In summary, these calculations of gain and noise circles based on a model for a .25 micron gate length, 100 micron gate width, GaAs FET indicates that the noise figure and gain requirements for the front end of the NASA low noise receiver can be met with reasonable matching networks.

2.0 Phase Shifter Fabrication and Evaluation - Task II

During the first year results were obtained on two phase shifter mask set designs; the single 180° bit phase shifter using shunt FETs and a more comprehensive mask set that includes multi-bit phase shifters using series FET switches. Two fabrication approaches were also tested; one uses standard power FET fabrication and a second approach employs a new self-aligned gate (SAG) fabrication technique for reduced parasitic resistive losses in the switching FETs. Much of the work, which is still incomplete, has been to develop a reproducible and reliable SAG fabrication process. Nevertheless, preliminary RF results have been obtained on SAG phase shifters which have been sufficiently encouraging to commit our final design and fabrication approach to the SAG technique.

To put the SAG results in perspective we present typical phase shifter results for the 180° bit using conventionally fabricated devices. For one run, typical FET ON resistance, R_{on}, as measured on the curve tracer, ranged between 12.5 and 15.5 ohms on dc good phase shifter chips. For circuit modeling a value of $R_{on} = 14\,\Omega$, a residual series resistance, $r = 7\,\Omega$, and a pinch-off capacitance of .07 pF was used to compare with the measured results [2]. Figures 25, 26a and 26b show the measured insertion phase, the rf test fixture (cover removed), and the measured insertion loss (including 1.4 dB fixture loss) respectively for one of the phase shifter chips.

The RF test fixture has in-line WR-28 waveguide input and output ports. Antipodel finline transitions fabricated on 0.25 mm thick RT/duroid are

employed to transition from waveguide to microstrip. The 1.4 dB fixture loss includes mismatch loss (.4-.6 dB) as well as dissipative loss in the total circuit comprising the transitions and interfaces to the GaAs chip. Figure 27 shows the phase data plotted together with the calculated results. Note the calculated results are in closer agreement with the measurements when a 0.1 pF shunt capacitance is included for each of the four FETs in the circuit model (see reference [2] for details). This parasitic capacitance is associated with the layout metallization of the FETs and can be decreased as will be shown below in the series FET switch design.

2.1 Results for 180° SAG Phase Shifter Using Shunt FETs

Figure 28a shows the encouraging results obtained for the insertion loss for the two phase states across the 27.5 to 32.5 GHz band. As seen from the CRT traces, the insertion loss including test fixture loss is between 4 and 5 dB in the band of interest, 27.5 to 30 GHz. This is in contrast to 6 to 8 dB loss for the corresponding measurements made on the conventional phase shifter chip as was shown above. Figure 29 shows the comparison between the calculated and measured results including the 1.4 dB test fixture correction. As shown in the figure the calculated values are based on the values of the FET parameters measured off test FETs on the SAG wafer. The reasonable agreement obtained justifies the use of our simple equivalent circuit model used for the ON and OFF FETs. Additionally, it should be noted that this wafer demonstrated a limited amount of surface conduction (conversion) which could account for some of the discrepency between measured and calculated values as the circuit model does not include such effects.

Finally, Figure 28b shows the measured differential insertion phase for the SAG phase shifter, from 27.5 to 30 GHz. Over this band the phase is within 20° of the calculated curve. Note, again, the tendency for the differential phase to decrease towards the upper half of the band.

2.2 Results From Second Mask Set Using SAG Series Switches

A comprehensive mask set has been developed that includes multi-bit phase shifters. Figure 30 shows photomicrographs of some of the circuit patterns on the finished wafers. Figure 30a shows the four bit phase shifter network (45°, 90°, 180°, 22°) while Figure 30b is an enlarged view of the 90 bit. These phase shifters employ 400 micron gate width series FETs for the switching devices. The 180°, 90° and 45° bits are switched line types, while the 22° bit is of the loaded line type. To date, one SAG fabrication run has been completed. As seen in the following, the RF insertion phase results for the individual bits (180°, 90° and 45°) support the predicted advantage of the series switch circuit design. Unfortunately our first run had low yield and did not attain the low resistance values (<8Ω) we were hoping for due to several fabrication related problems. These are presently being corrected for the second run. Nevertheless, phase shift data obtained on the individual bits is quite encouraging.

Figures 31-33 show the measured differential phase for the three bits across the 27.5-32.5 GHz band and the comparison with the ideal time delay characteristics. The measured data is taken with the H.P. network analyzer

using the 26-40 GHz waveguide reflection-transmission test set. Although displaced downwards by about 7°, the measured data follows closely the desired slope of the characteristic. Note the improvement from previous phase data using the shunt design. This improvement is primarily due to the more optimized layout and the reduction in reactive parasitics. Figures 34 through 36 show the actual measured data for the insertion differential phase, the insertion loss, and the return loss respectively from 27.5 to 32.5 GHz for the 180° and 45° bits. In Figure 35 the insertion loss includes the fixture loss of about 1.4 dB and is better than the results obtained with conventionally fabricated FETs but worse than the best SAG result obtained on the 180° bit using shunt FETs.

3.0 Gain Control Fabrication - Task III

The mask design for the first iteration of the gain control is complete. The layout contains the following circuits and devices:

- o 100 micron gate width low noise FET.
- o Low noise FET with stub input matching.
- o Low noise FET with capacitor matching
- o Dual gate 100 micron gate width FET.
- o Dual gate FET with capacitor matching.
- o Two stage dual gate amplifier for gain control.
- o Test patterns for in-process testing.

Each device or circuit is expanded into an array or reticle of devices in the actual layout. For example, the 100 micron gate width FET device is expanded into a 4.87 by 4.87 mm array containing 198 FETs and 1 test pattern for in-process testing. Each FET die is 300 μm by 300 μm. The layout for the single gate FET is shown in Figure 37. A second example is the two-stage amplifier.

The two-stage amplifier reticle occupies the same area as the the 100 micron FET reticle. The two-stage amplifier reticle contains only twelve two-stage amplifiers and one in-process test pattern. The two-stage amplifier shown in Figure 38, has a 1.9mm x .65mm chip size. The single and dual gate FETs with capacitor matching are combined in a single reticle so there is a total of five separate reticles. Two of the reticles, the 100 micron FET and the 100 micron FET with stub input matching, do not require nitride or air bridge

processing. The remaining three reticles all require nitride and air bridge processing. Since the processing without nitride or air bridges requires fewer steps it makes sense to separate these reticles into two groups; 1) the 100 micron FET group, and 2) the two-stage amplifier group. For the 100 micron FET group all layers except the final pad metal layer are done by e-beam lithography. The two-stage amplifier group requires four optical levels after e-beam processing: 1) the circuit metal level, 2) the dielectric patterning level, 3) the second level metal and 4) the air bridge level. The optical masks for these levels will be made on the Cambridge e-beam system.

3.1 100 Micron FET

The first fabrication runs will include only the 100 micron FET group. The 100 micron devices will be tested to check the validity of the FET model discussed in Section II-1.2.2. The initial run will be fabricated on ion implanted LEC substrate material. The material has been implanted with 5 x 10^{12} ions/cm^2 of silicon at 120 Kev and annealed for 30 minutes at 850°C in an arsenic overpressure. The measured sheet resistance of the implanted and annealed material is 600 ohms per square compared to a calculated sheet resistance of 538 ohms per square. This indicates that the activation is high, on the order of 90 percent. However, CV profiling (See Figure 39) indicates that the peak carrier concentration is lower than the theoretical value and there is some spreading of the implant distribution.

3.2 Dual Gate Amplifier

The layout for the dual gate FET amplifier has been completed according to the design discussed in Section 1.1.3. Fabrication of the dual gate amplifier will begin after completion of the first 100 micron FET runs.

4.0 RF/IF and LNA Submodule Fabrication and Evaluation - Tasks IV and V

Tasks IV and V are scheduled to begin in the second year of the program. Development of the low noise amplifier has actually started during the first year with the design and initial fabrication of the 100 micron gate width FET included in the gain control mask set (discussed in Section II-1.2.2 and II-3.1).

5.0 Submodule Integration and Receive Module Development - Tasks VI and VII

Tasks VI and VII are scheduled to begin in the third and fourth year of the program. The designs for both the integrated module and the monolithic module was discussed in Section II-1.1.1.

6.0 Product Assurance and Reporting - Tasks IX and X

A product assurance program has been implemented in accordance with the requirements of Section 3.4 of the RFP. Log books concerning device and circuit fabrication and development have been utilized from the outset of the program.

Reports have included an updated work plan, monthly technical progress reports, as well as monthly and quarterly financial and management reports (533M, 533Q, 533P) as required under the contract.

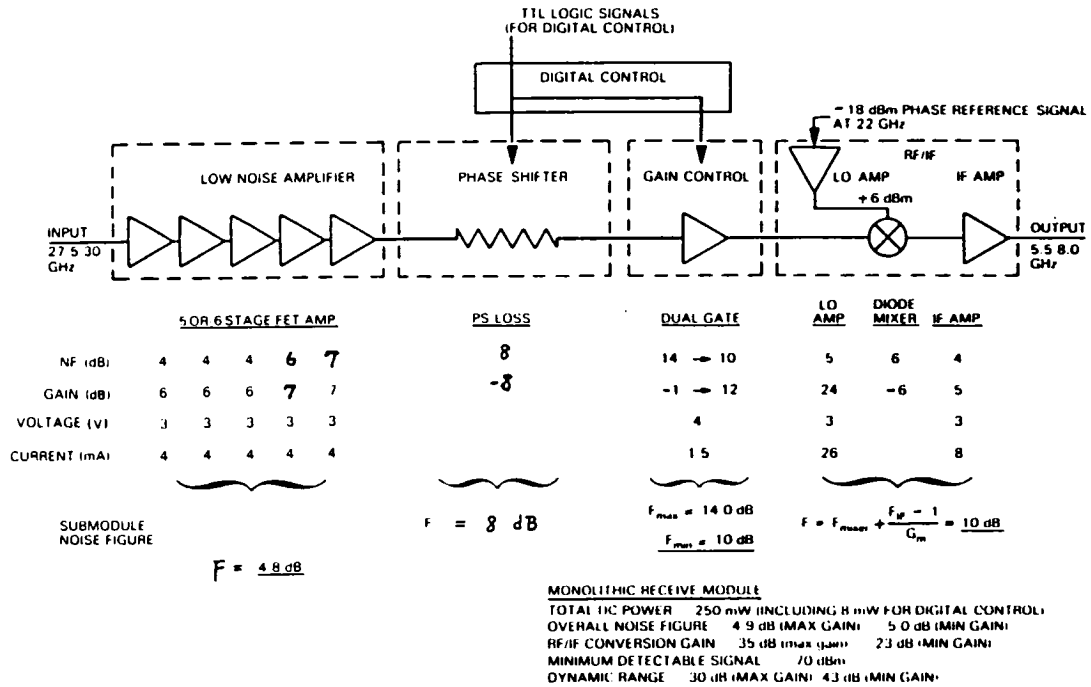


Figure 1. Block Diagram of Overall Monolithic Receiver

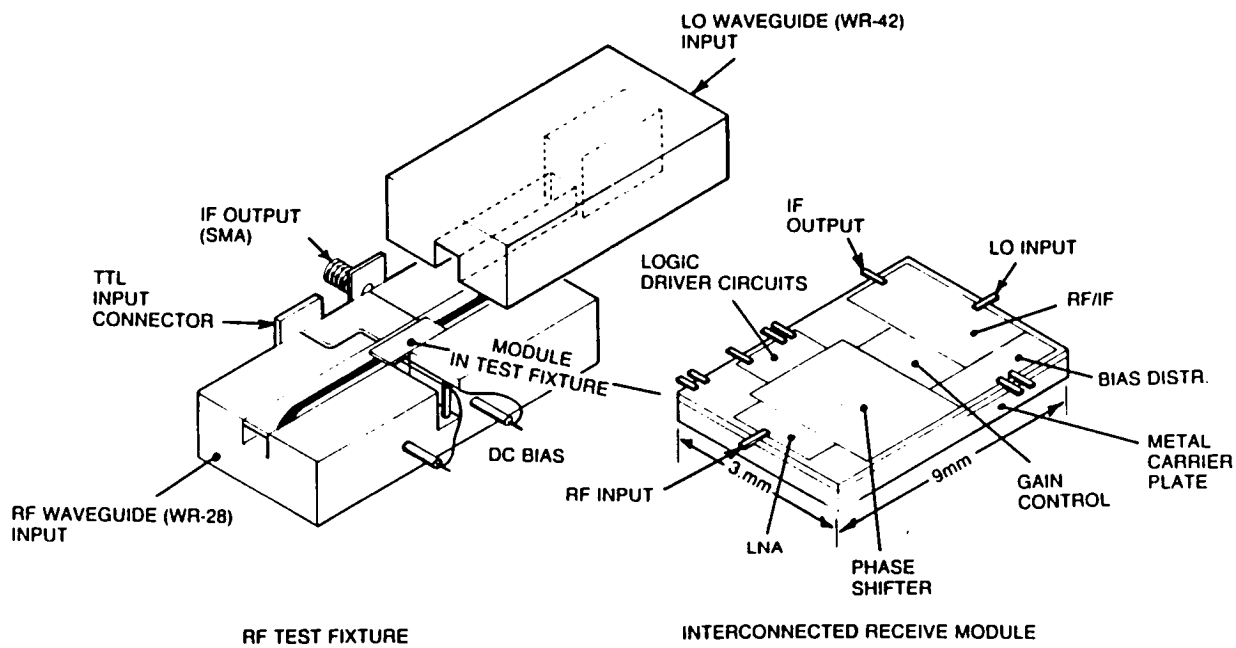
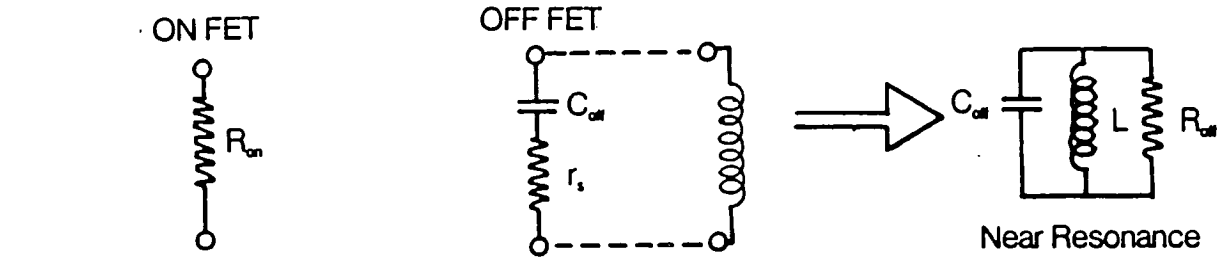


Figure 2. Interconnected Receive Module and RF Test Fixture



$Q_c = (\omega r_s C_{off})^{-1}$
ω_o = Center Band Radian Frequency
$L = (\omega_o^2 C_{off})^{-1}$ = External Inductor

Switch Figure of Merit, $\hat{Q}$;

$$\hat{Q}^2 \cong [(\omega C_{OFF})^2 r_S R_{ON}]^{-1} = \frac{R_{OFF}}{R_{ON}}$$

Example: $\hat{Q}^2|_{10GHz} = 738$
$\hat{Q}^2|_{30GHz} = 82$

Figure 3. Simplified Equivalent Circuits for ON and OFF FETs

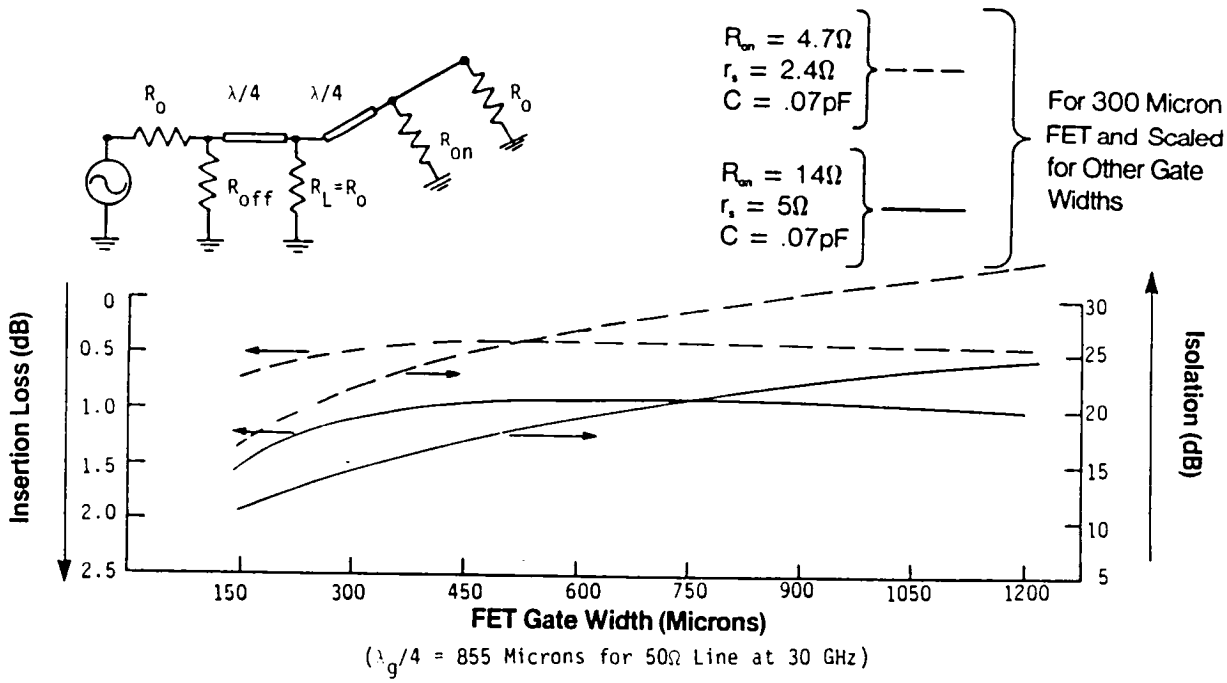


Figure 4. Insertion Loss and Isolation versus Gate Width

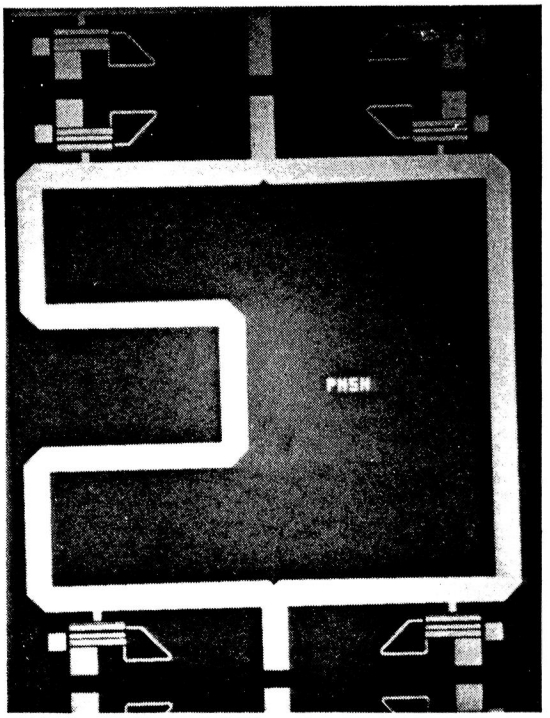


Figure 5. Chip Layout for 180° Bit

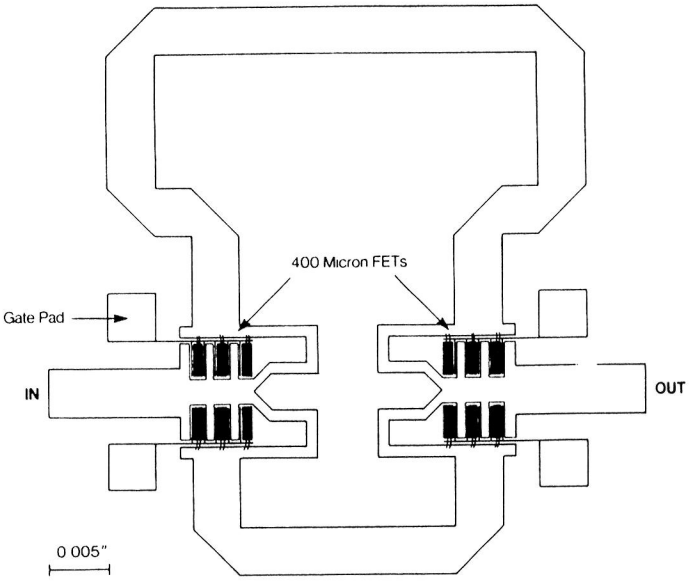


Figure 6. Layout of 180° Bit Using Four Series FET Switches

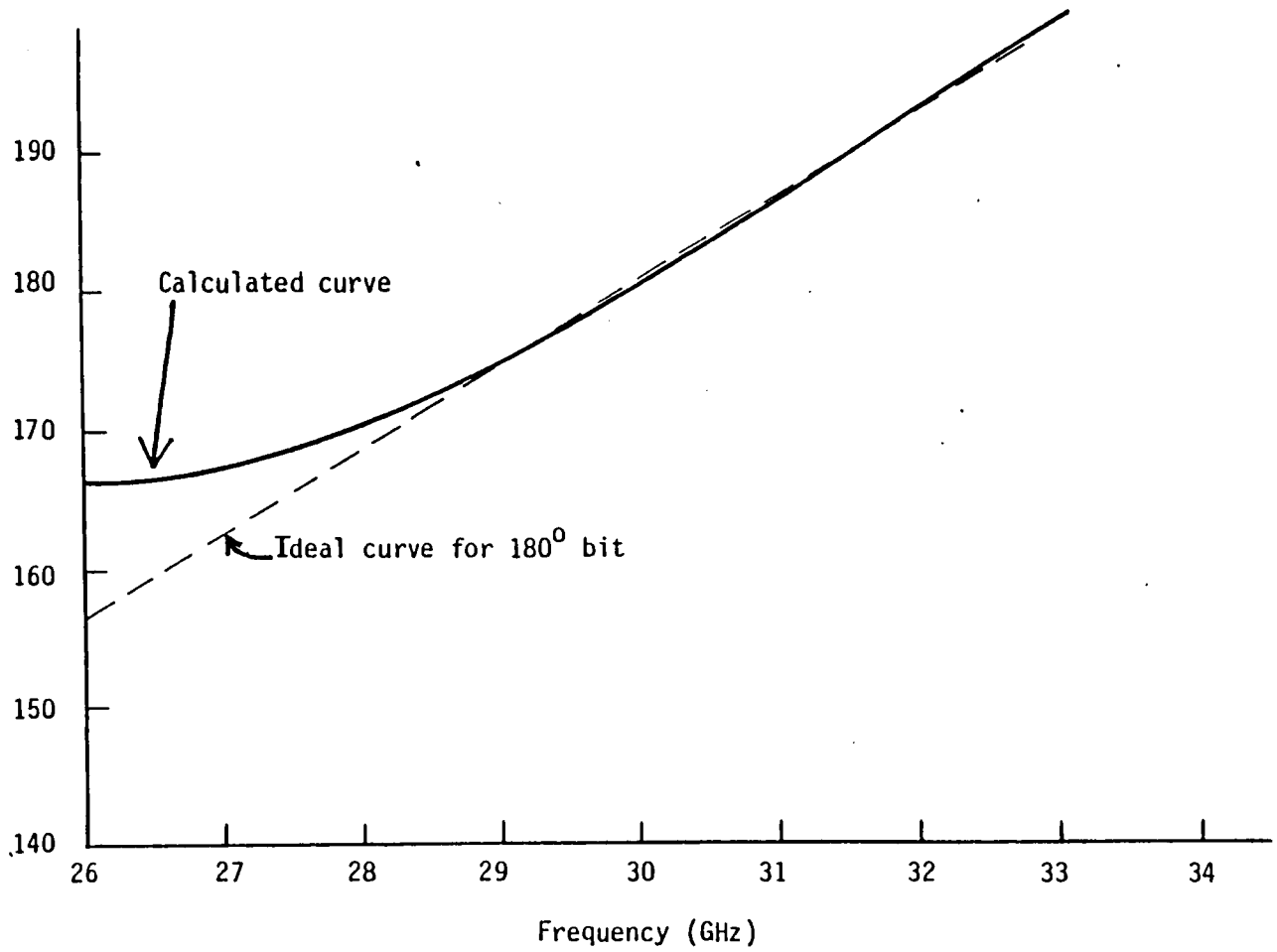


Figure 7. Computer Calculated Results for 180° Phase Bit Using Series Switches

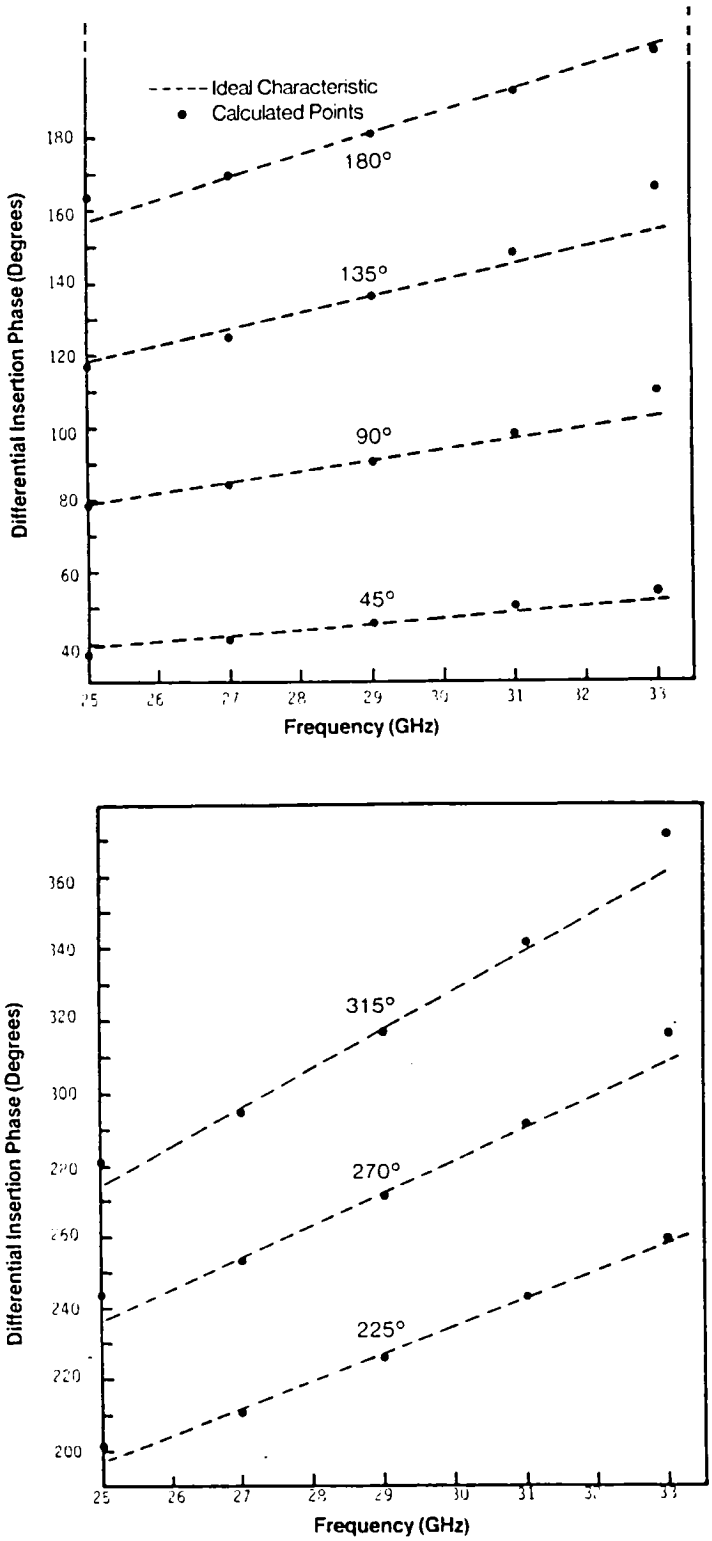


Figure 8. Calculated Differential Insertion Phase for 3-Bit Phase Shifter (180°, 90°, 45° Bits) Using Series FET Switches

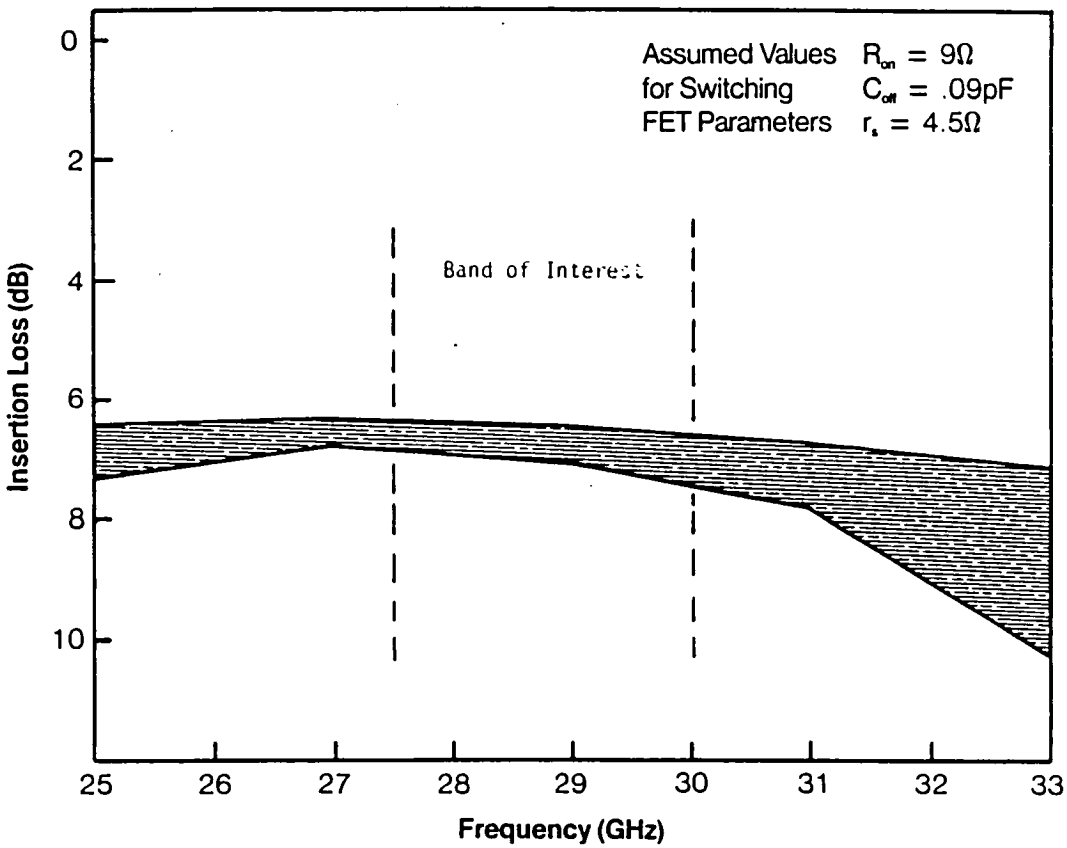
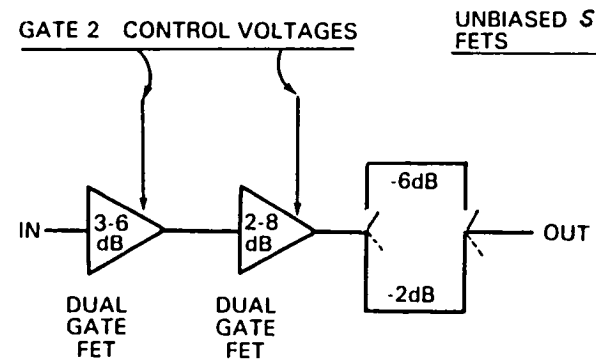


Figure 9. Calculated Insertion Loss "Envelope" for Eight States of 3-Bit Phase Shifter



GAIN STATES (dB)	(G_1) 3,6	(G_2) 2,5,8
ASSOCIATED NOISE FIGURE (dB)	(F_1) 10,9	(F_2) 14,10,10
VOLTAGE(V)	4	4
MAX. CURRENT (mA)		8

OVERALL GAIN STATES (dB)	CORRESPONDING RECEIVER RF/IF GAIN (dB)
① 3 + 2 − 6 = −1	17
② 3 + 5 − 6 = +2	20
③ 3 + 5 − 2 = +6	24
④ 6 + 5 − 2 = +9	27
⑤ 6 + 8 − 2 = +12	30
⑥ −15 −15 − 6 = −36	OFF

WORST CASE NOISE FIGURE (STATE ①)

$$F_{MAX} = F_1 + \frac{F_2 - 1}{G_1} + \frac{L - 1}{G_1 G_2} = 13.6\text{dB}$$

BEST CASE NOISE FIGURE (STATE ⑤)

F_{MIN} = 10.1

Figure 10. Gain Control Design

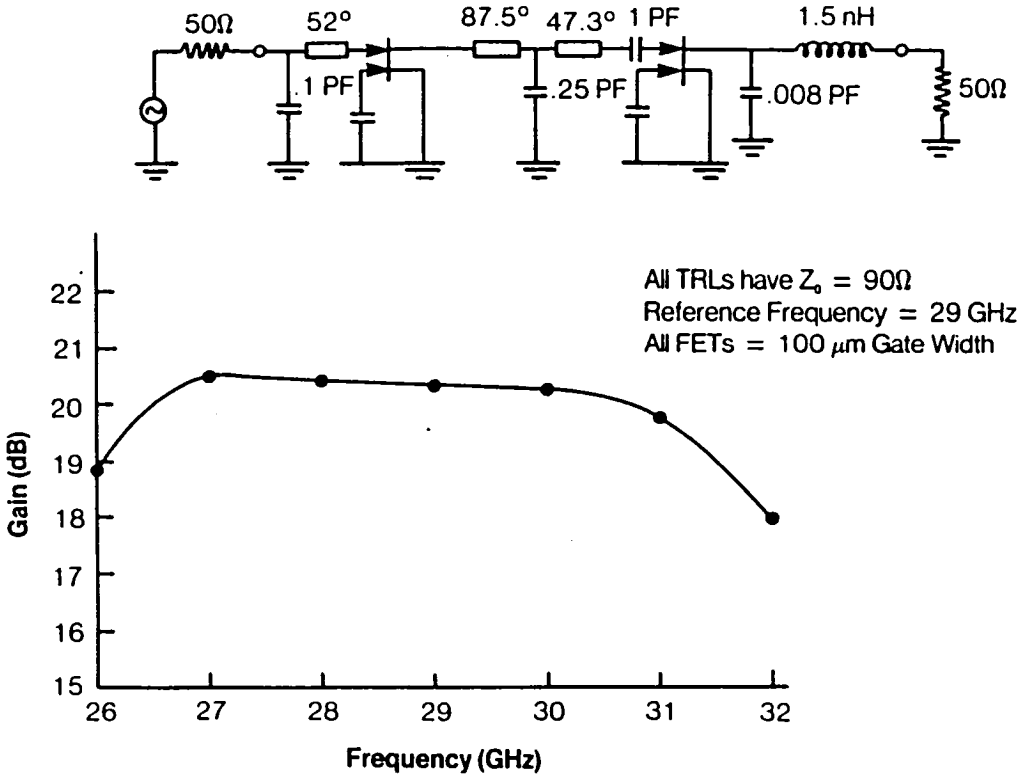


Figure 11. Design for Monolithic 2-Stage Dual-Gate Amplifier

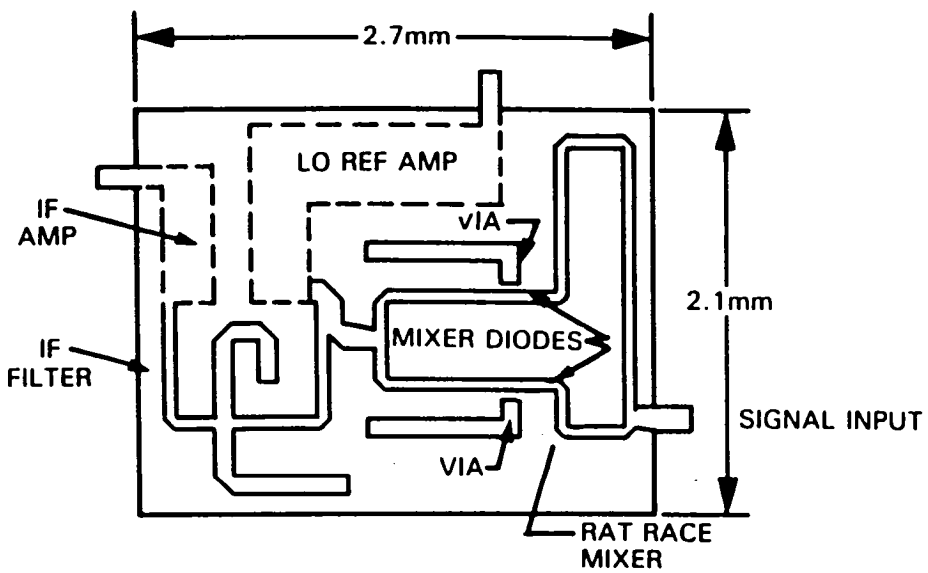


Figure 12. RF/IF Submodule with Rat Race Hybrid

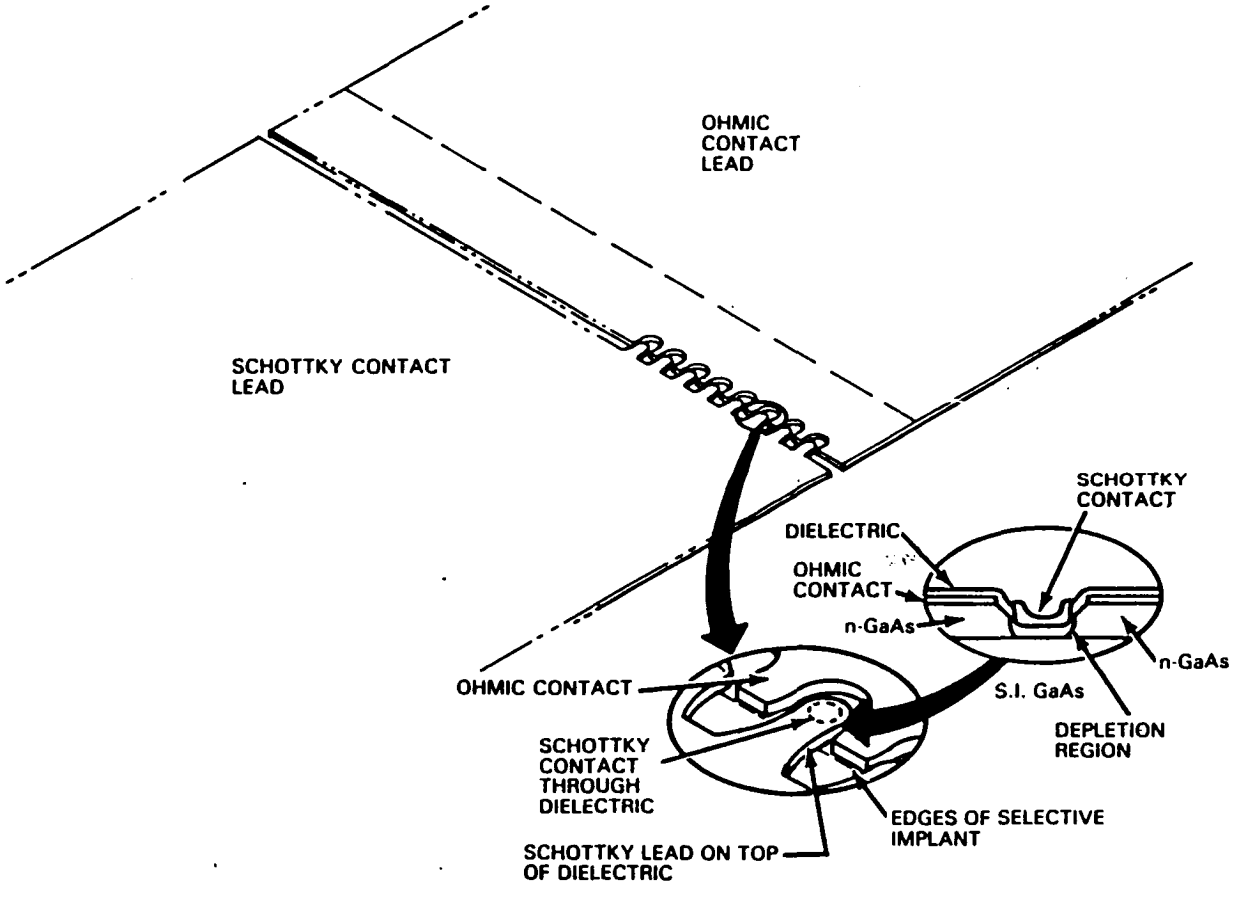


Figure 13. Diode Structure for High Mixer Performance and Fabrication Simplicity

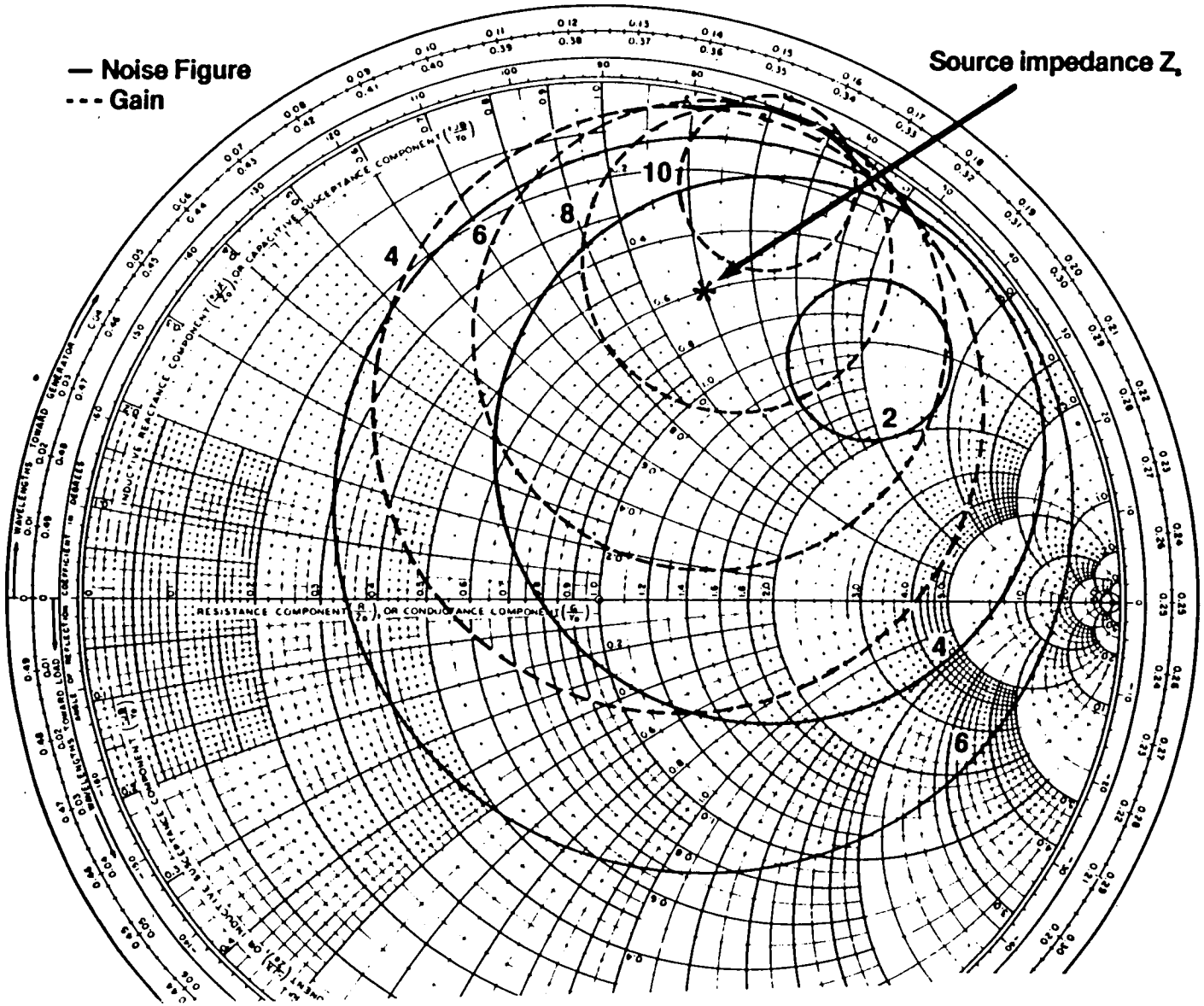


Figure 14. Noise Figure and Gain Circles for First Stage of 22 GHz Amplifier

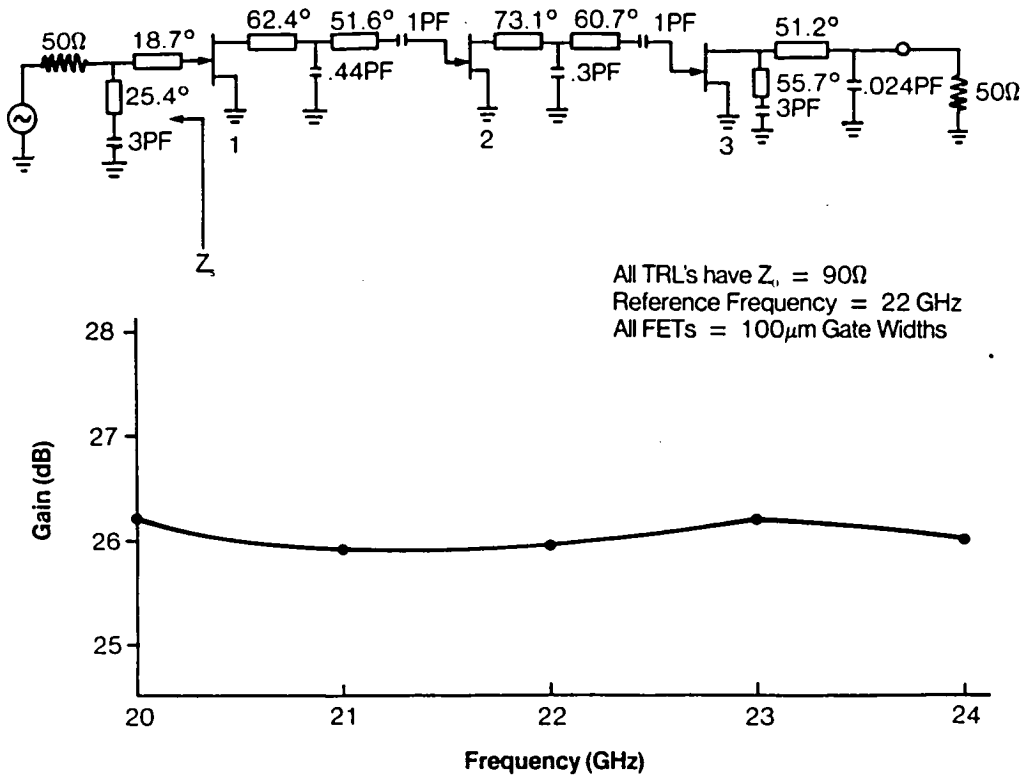


Figure 15. Design for Monolithic 22 GHz Amplifier

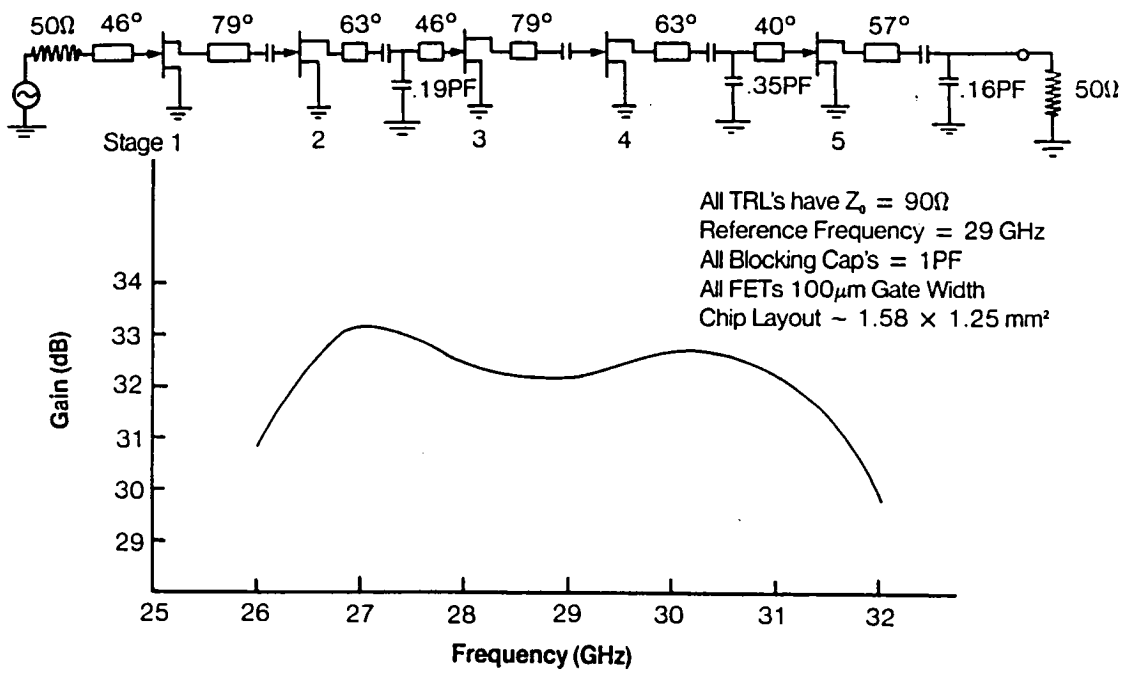


Figure 16. Design for Monolithic Five-Stage Amplifier

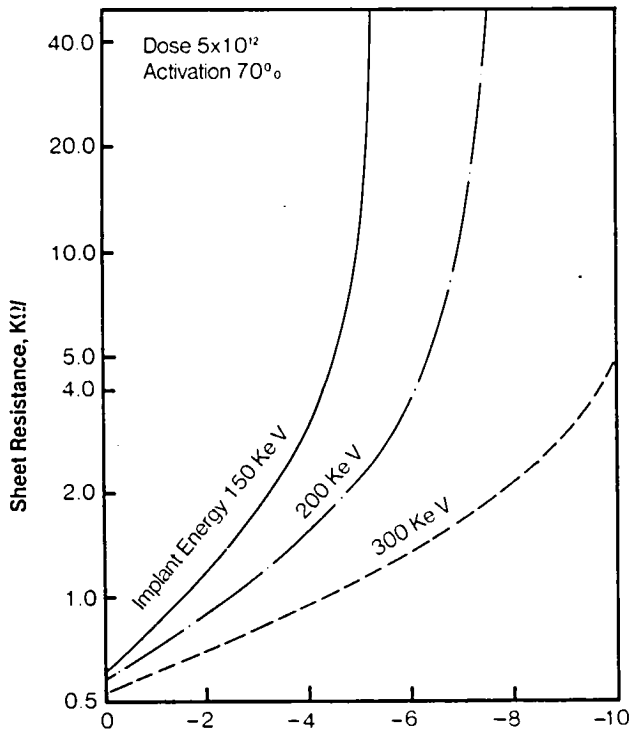


Figure 17. Channel Sheet Resistance versus Gate-to-Channel Voltage for Different Implant Energies

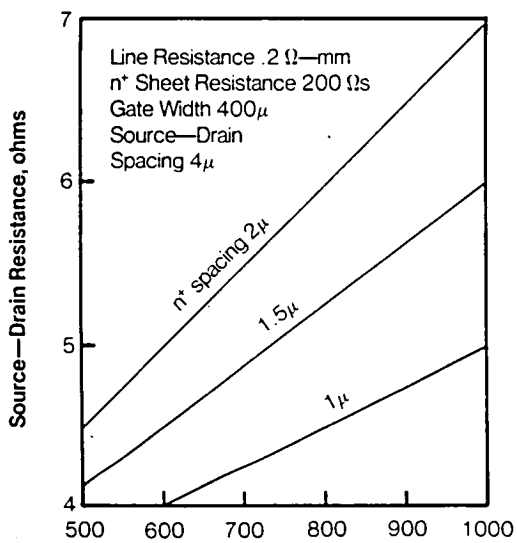
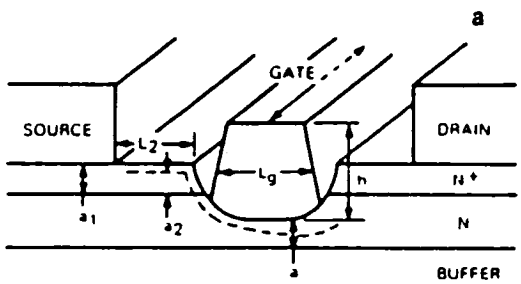


Figure 18. Source-Drain Resistance versus Channel Sheet Resistance



Gate length	L_g	= 0.25 microns
Unit gate width	w	= 50 microns
Channel thickness	a	= 0.15 microns
Doping density	N	= 2.5×10^{17}
Total gate width	Z	= 100 microns
Gate-source spacing	L_{sg}	= .75 microns
Gate metal thickness	h	= 0.5 microns
Specific contact resistance	r_c	= 10^{-6} ohm-cm^2
	a_1	= 0.22
	a_2	= 0.15
	N_1	= 2.5×10^{17}
	N_2	= 2.5×10^{17}

Calculated noise figure = 2.5 dB at 32 GHz

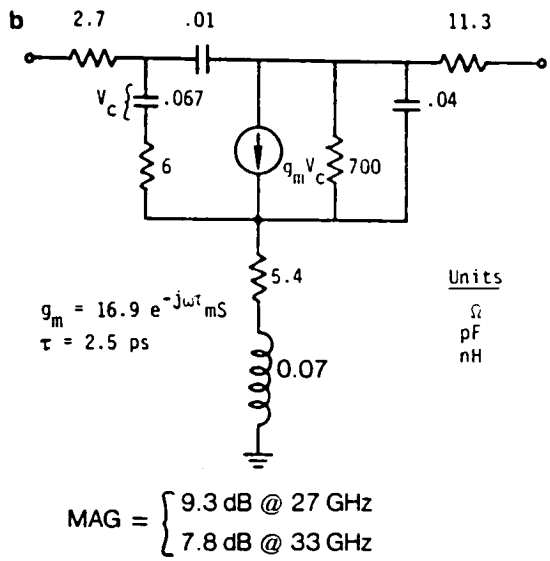


Figure 19. 100 x 0.25 Micron Low Noise FET Design
a) Device parameters
b) Equivalent Circuit

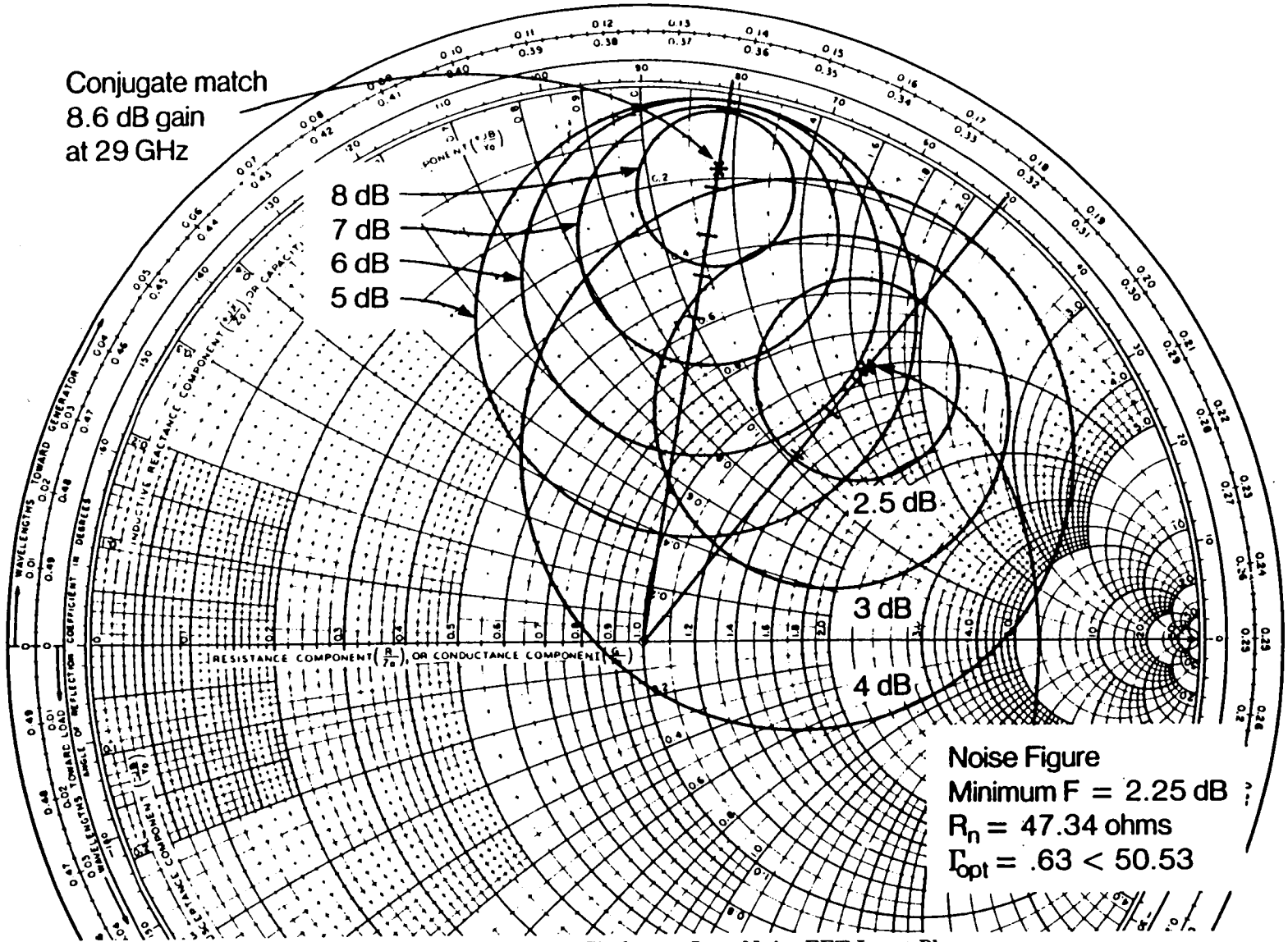


Figure 20. Gain and Noise Circles for Low Noise FET Input Plane
- No C_{dg} or Ls for Noise Circles

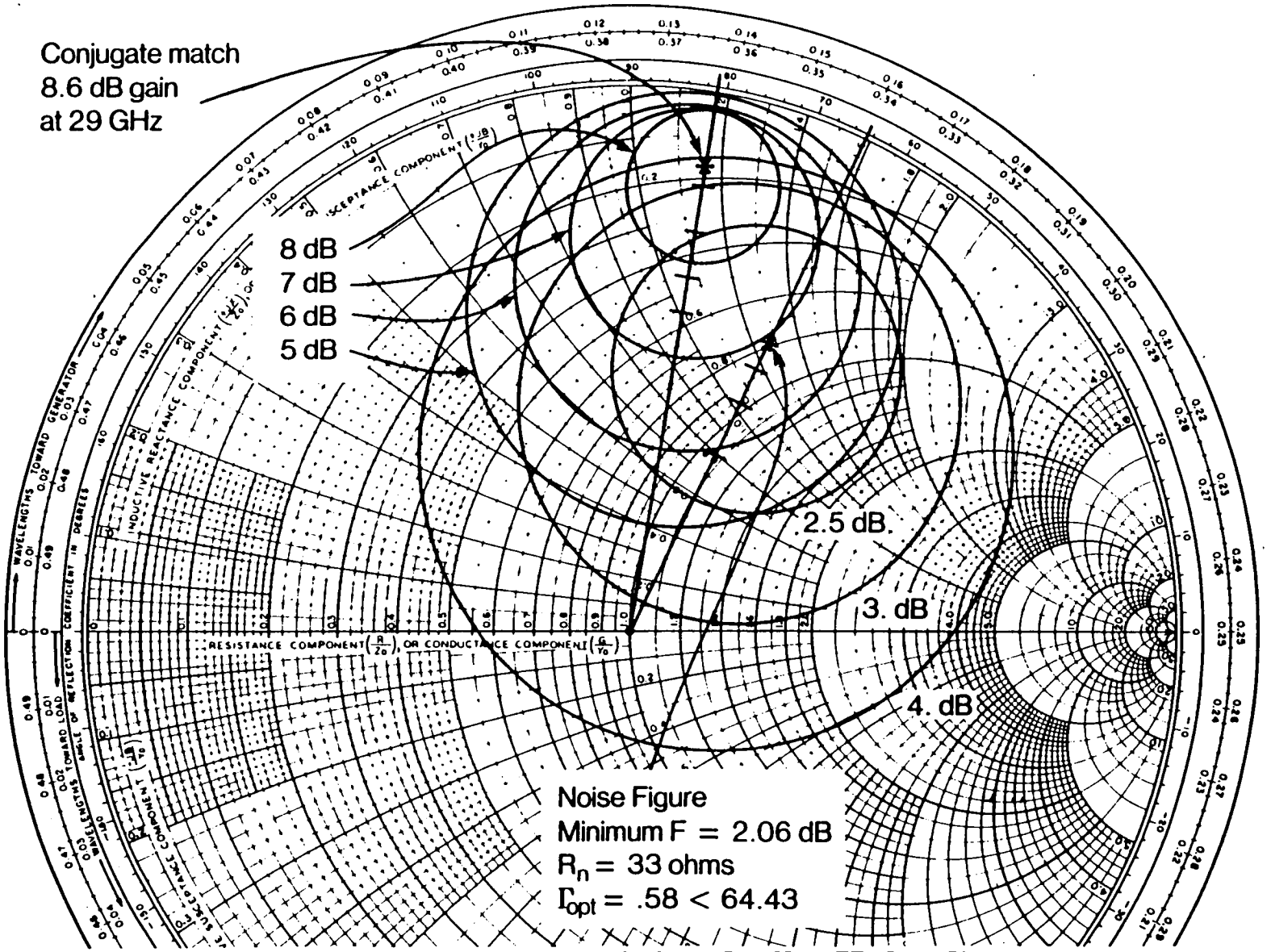


Figure 21. Gain and Noise Figure Circles for Low Noise FET Input Plane Including C_{dg} and Ls

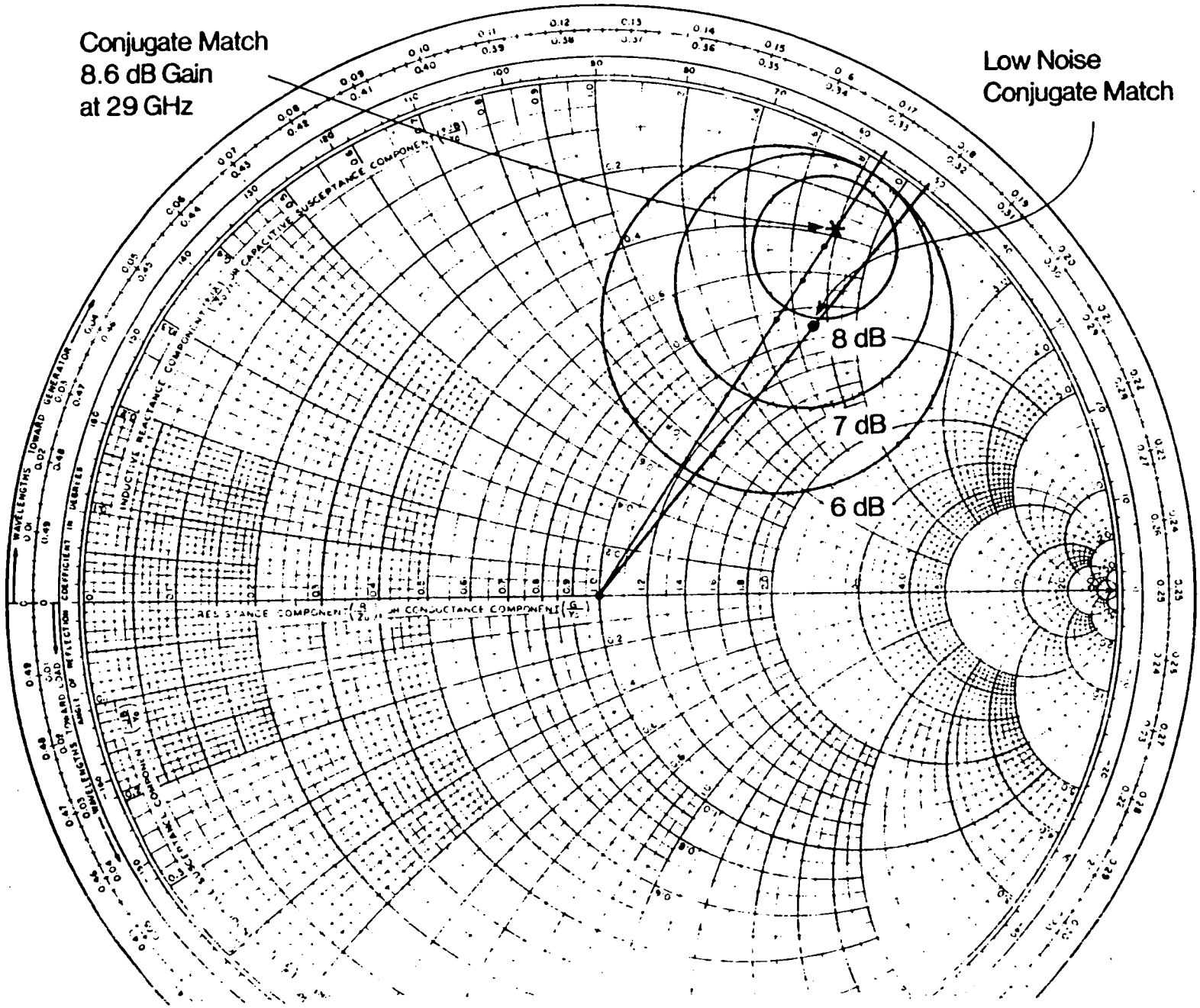


Figure 22. Gain Circles for Low Noise FET Output Plane

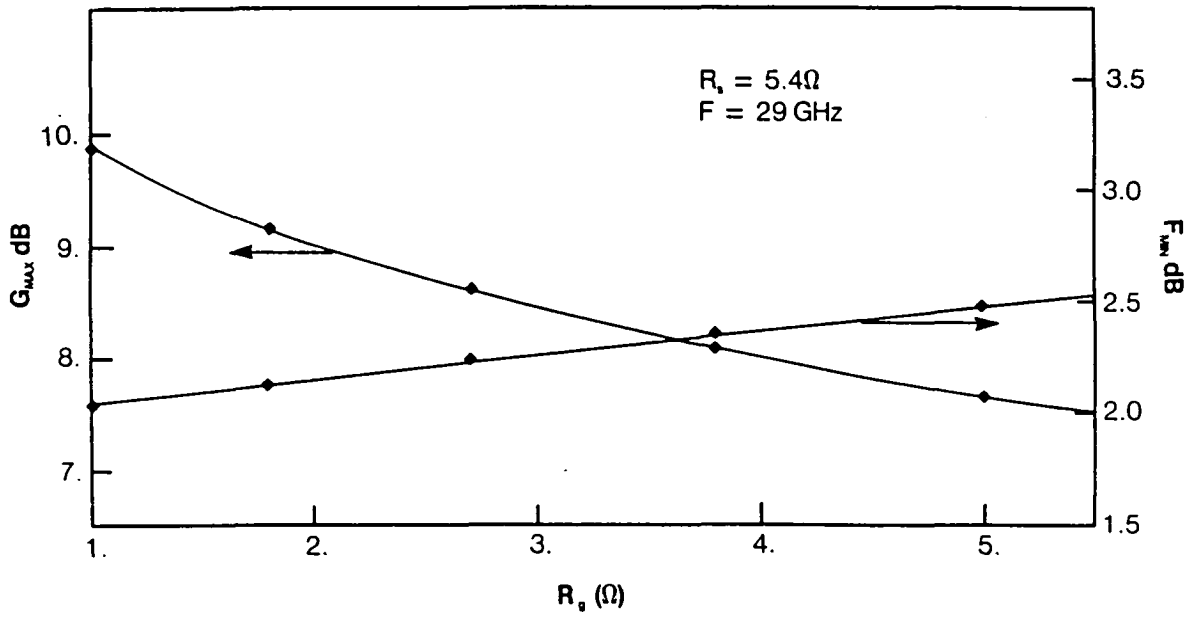


Figure 23. Effect of Gate Resistance on 29 GHz Gain and Noise Figure

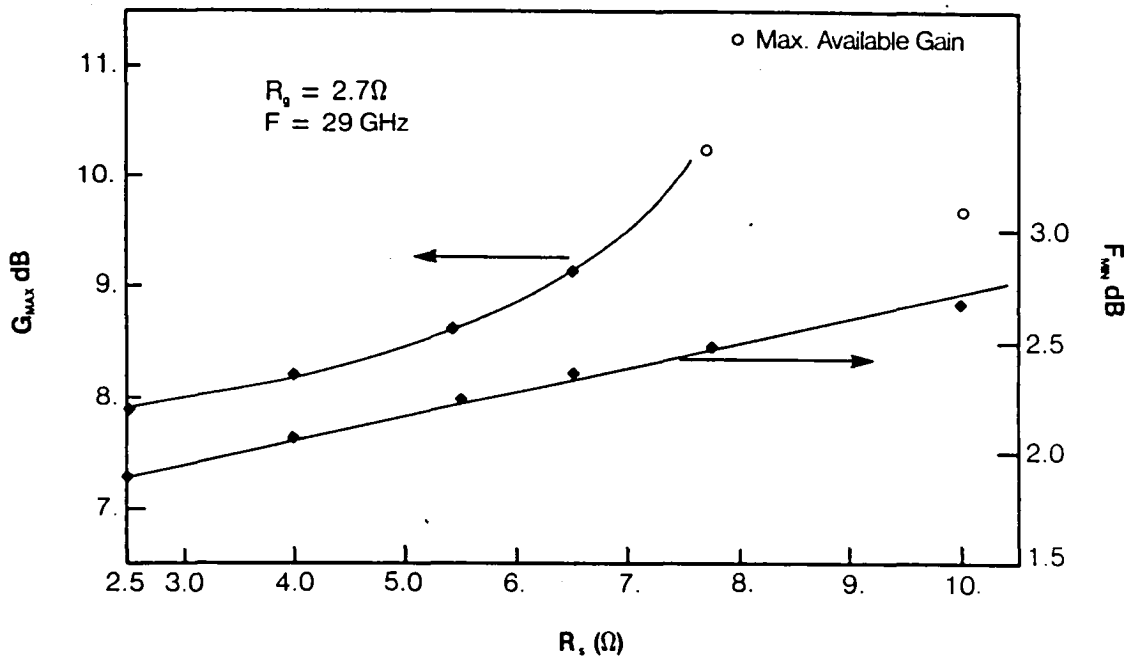


Figure 24. Effect of Source Resistance on 29 GHz Gain and Noise Figure

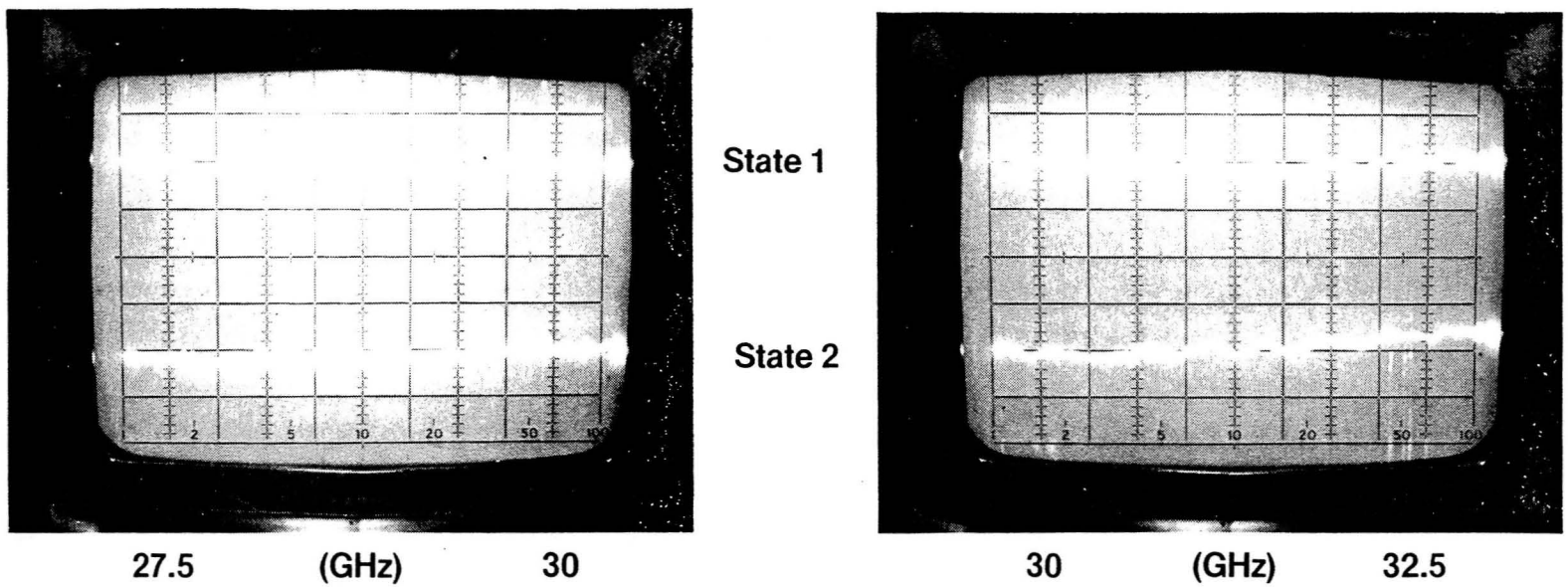
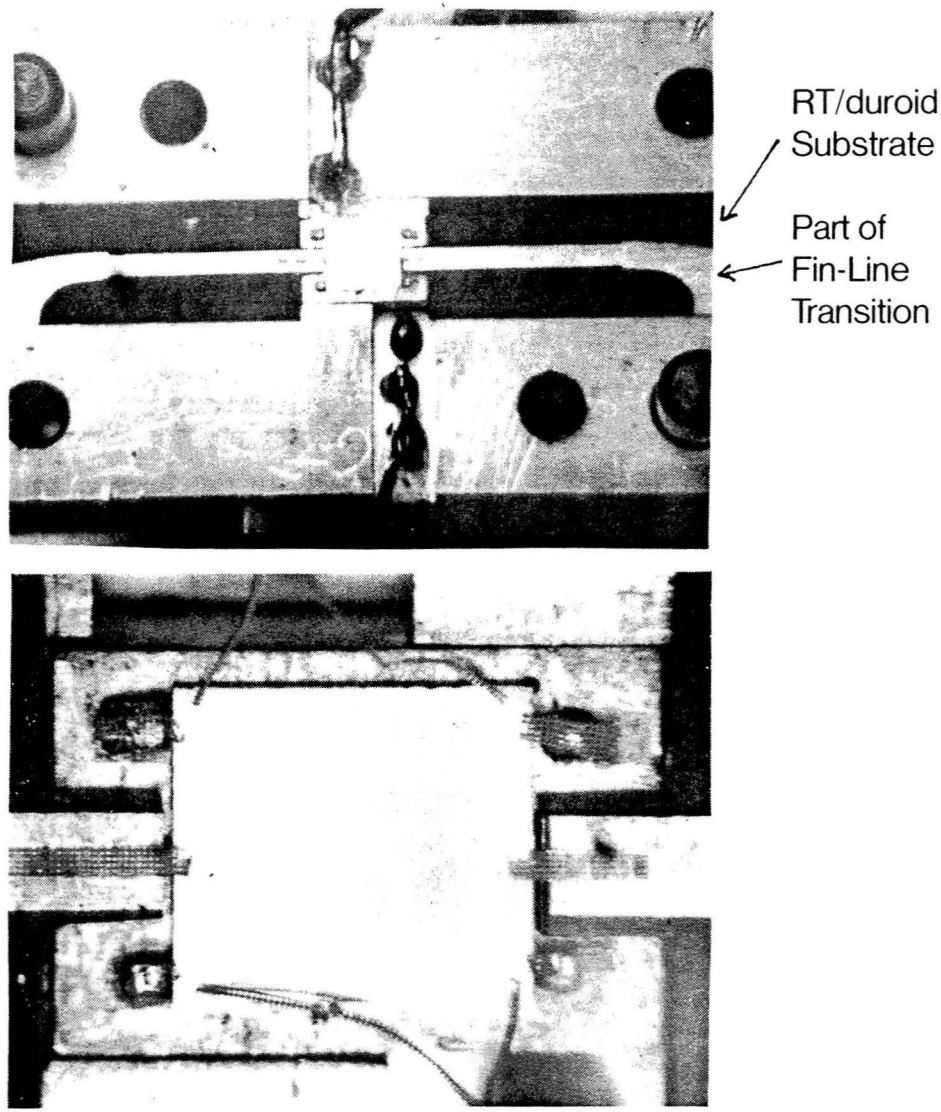
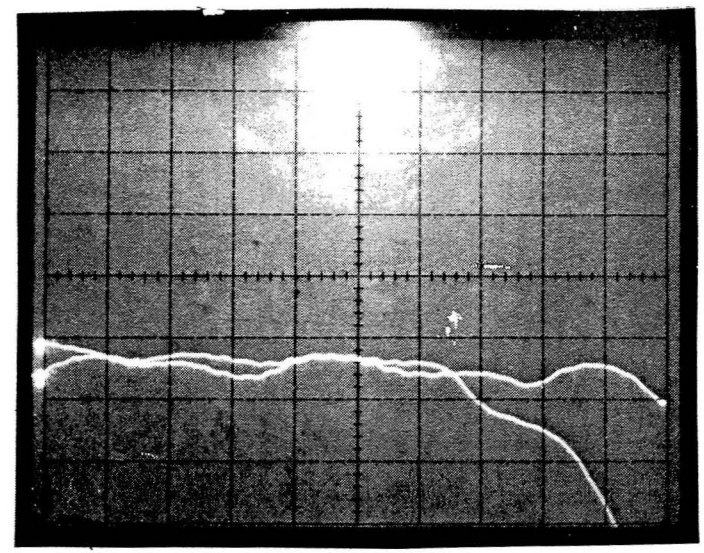


Figure 25. Insertion Phase for 180° Phase Shifter (TR061A)
As Measured on the Network Analyzer



(Test Fixture and Chip)

Insertion Loss



Vertical: 5 dB/div
Horizontal: 26.5 - 37 GHz
Reference: Center Line

Figure 26. Test Fixture and Measured Insertion Loss for the Two States of the 180° Phase Shifter

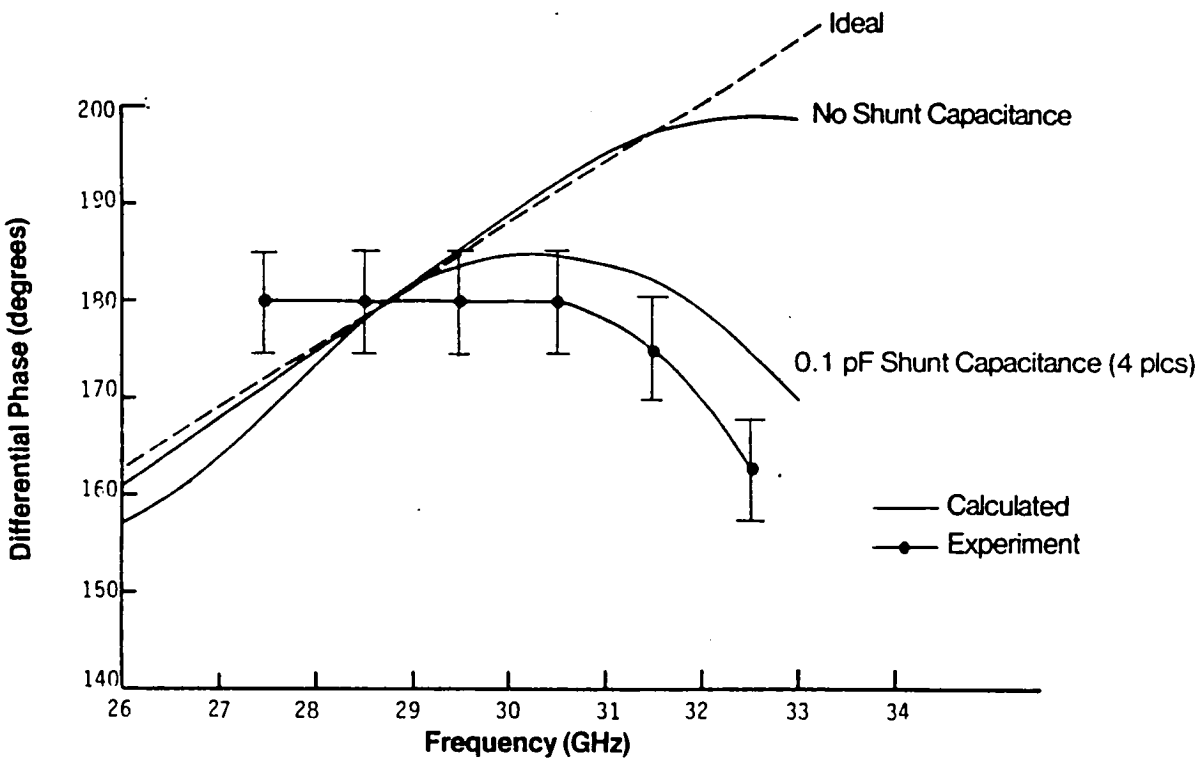
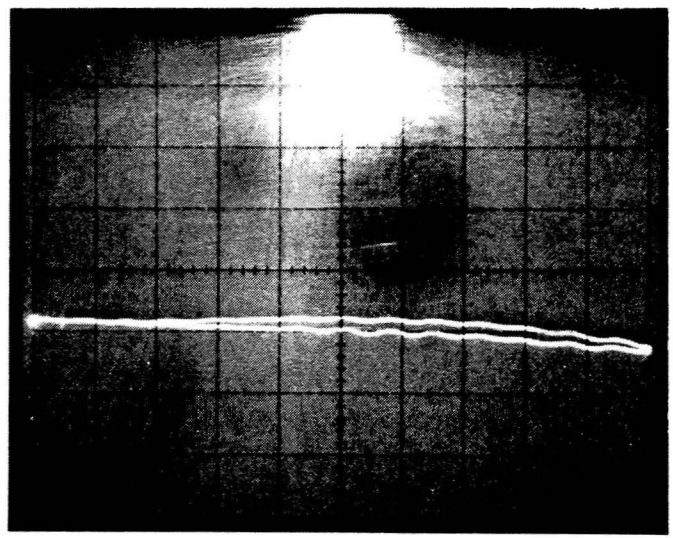


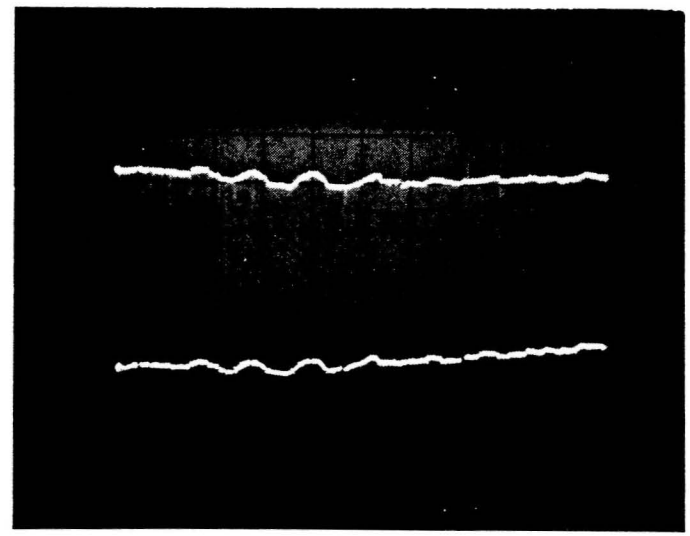
Figure 27. Calculated and Measured Differential Phase Shift for 180° Phase Shifter (TR061A)

Insertion Loss



Vertical: 5 dB/div
Reference: Center Line
Horizontal: 500 MHz/div: 27.5 - 32.5 GHz

Differential Insertion Phase



Vertical: 45°/div
Horizontal: 250 MHz/div; 27.5 - 30 GHz

Figure 28. Measured RF Results for SAG 180° 1-Bit Phase Shifter

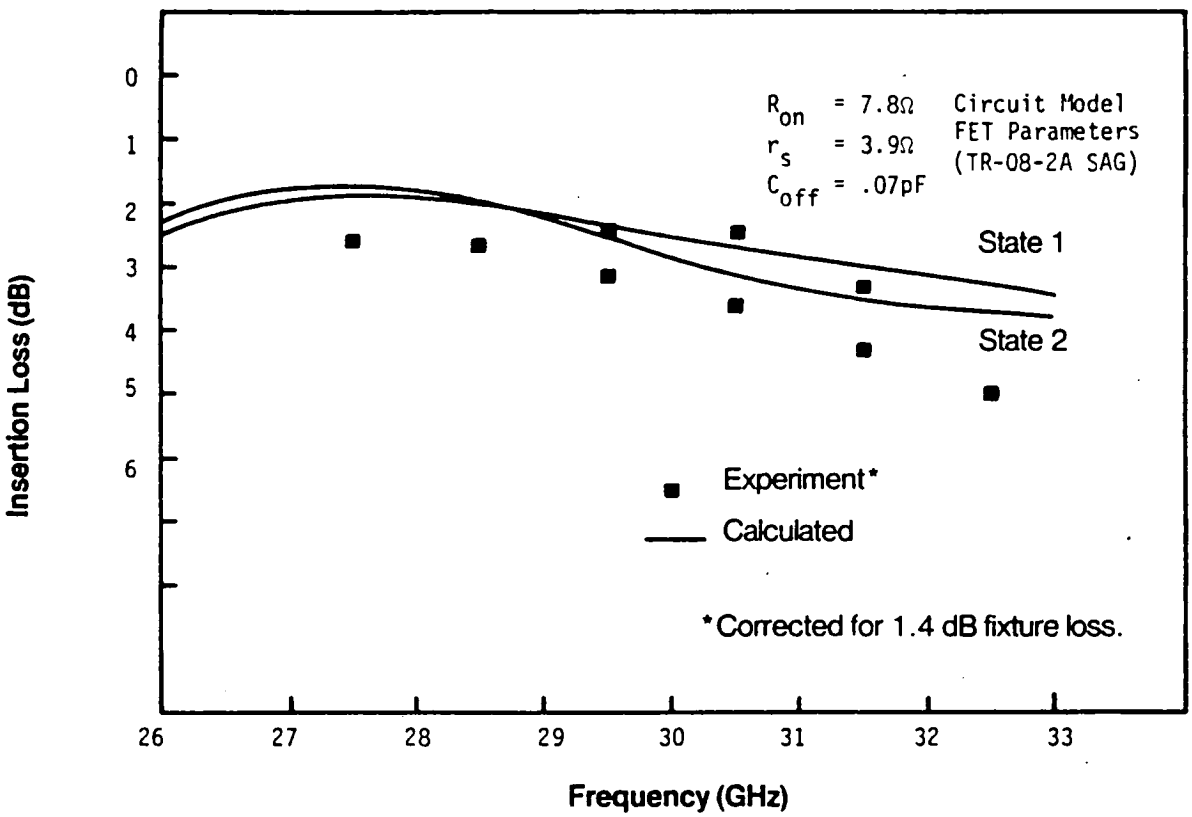
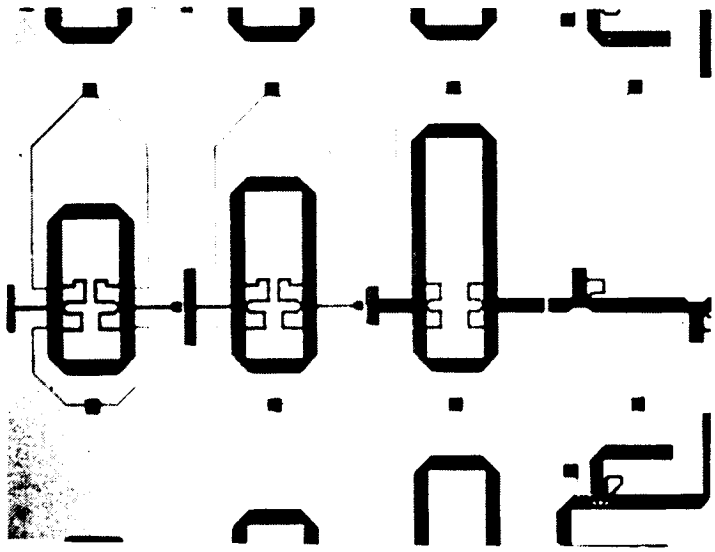
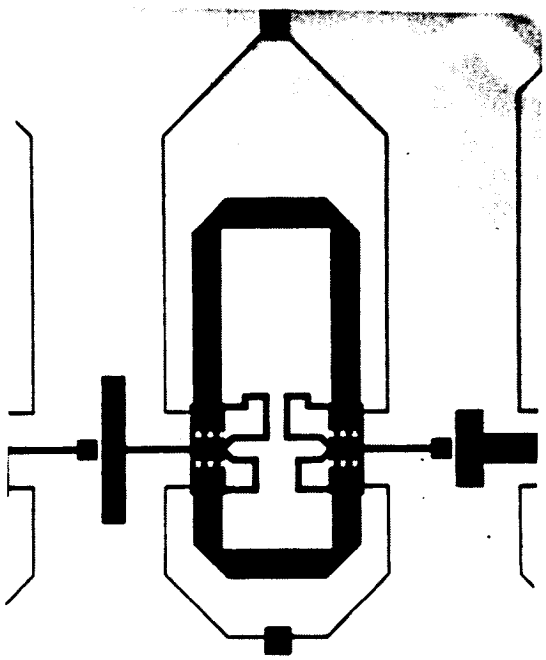


Figure 29. Comparison of Measured and Calculated Insertion Loss for SAG Phase Shifter



(a)



(b)

Figure 30. Photomicrographs of SAG Phase Shifter Circuits on a Processed Wafer
a) The four bit phase shifter (45°, 90°, 180°, 22°)
b) Enlarged view of 90° bit

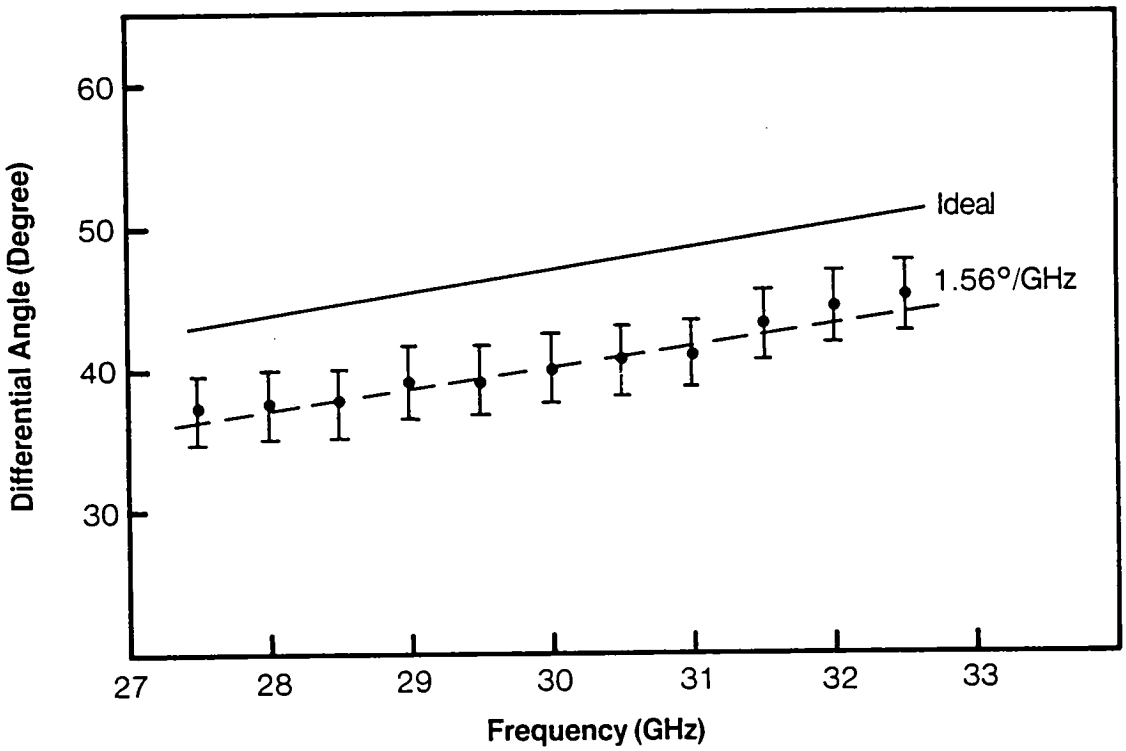


Figure 31. Calculated and Measured Differential Phase Shift for 45° Phase Shifter

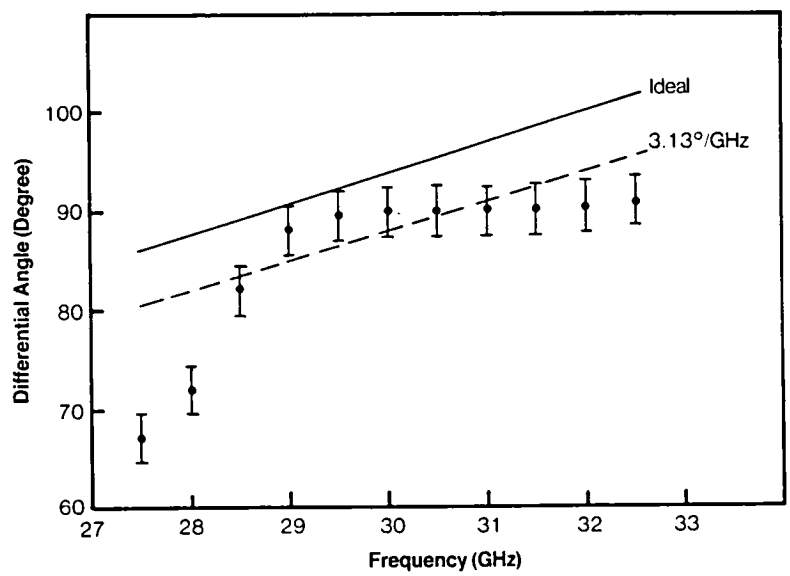


Figure 32. Calculated and Measured Differential Phase Shift for 90° Phase Shifter

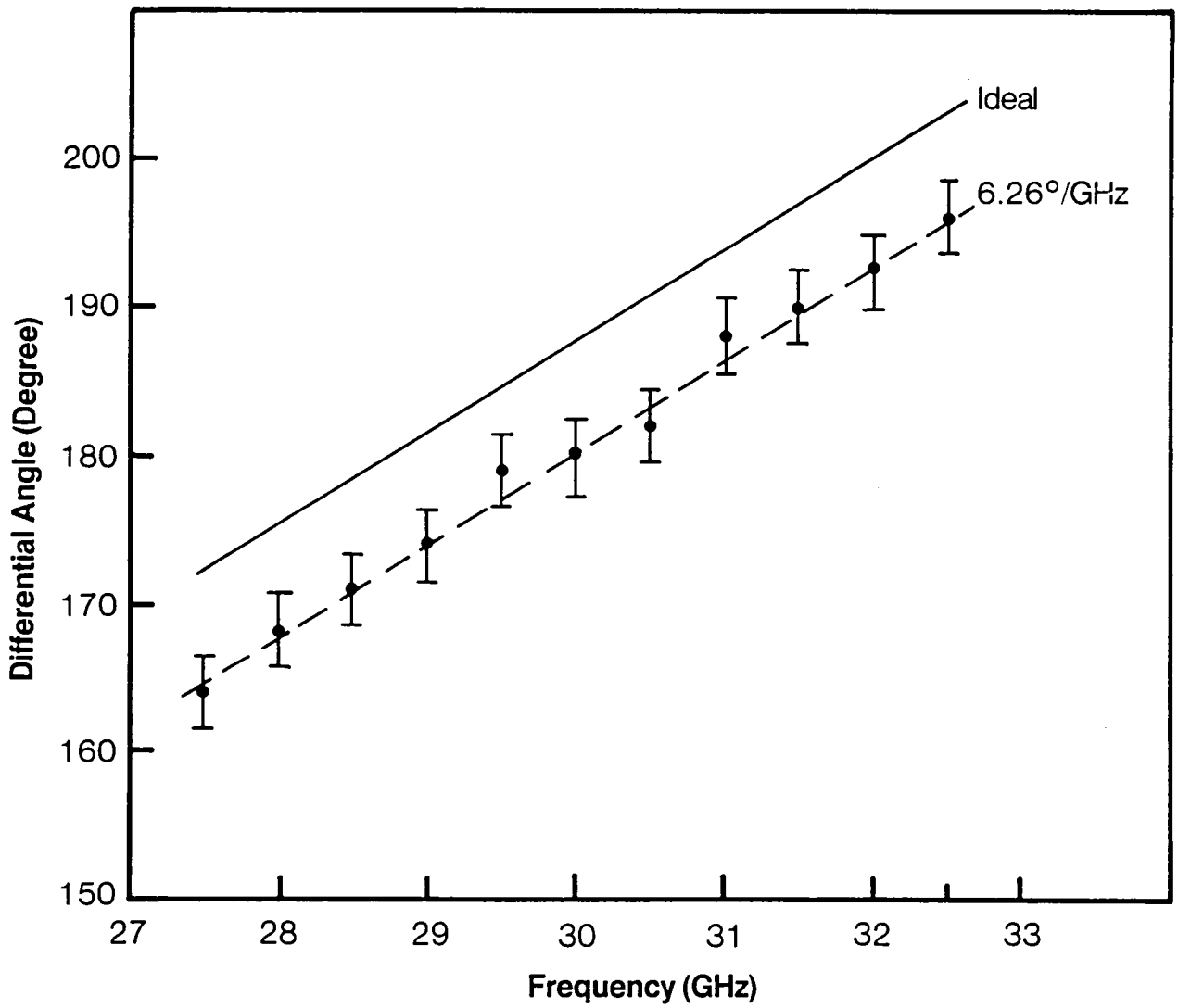


Figure 33. Calculated and Measured Differential Phase Shift for 180° Phase Shifter

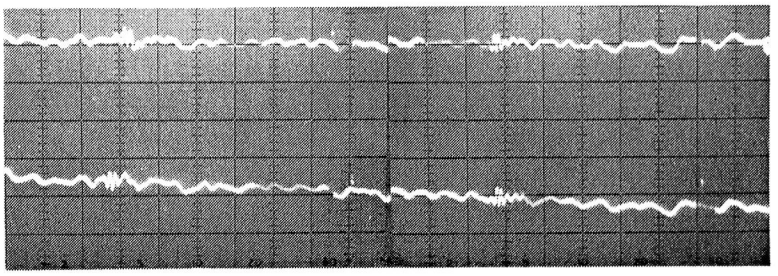


Figure 34. 180° Phase Shifter Vertical = 45°/div.
Horizontal = 27.5 - 32.5 GHz, 500 MHz/div.

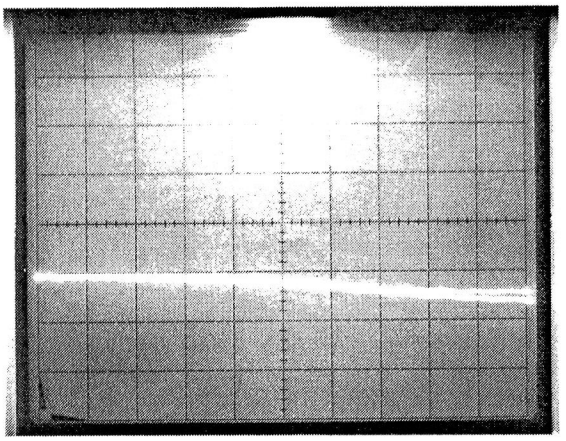


Figure 35. 45° Bit Insertion Loss
Vertical = 5 dB/div.
Horizontal = 27.5 - 32.5 GHz
Reference = Center line

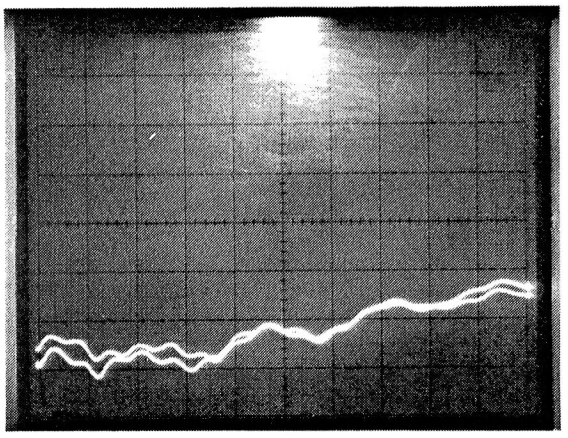


Figure 36. 45° Bit Return Loss
Vertical = 10 dB/div.
Horizontal = 27.5 - 32.5 GHz
Reference = Center line

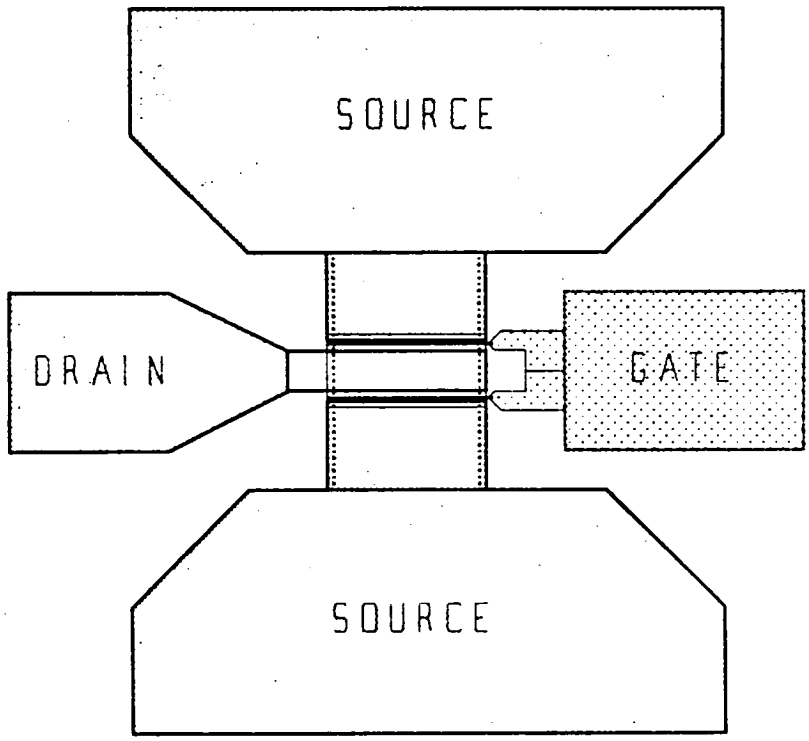


Figure 37. CALMA Layout for 100 Micron Gate Width Low Noise FET

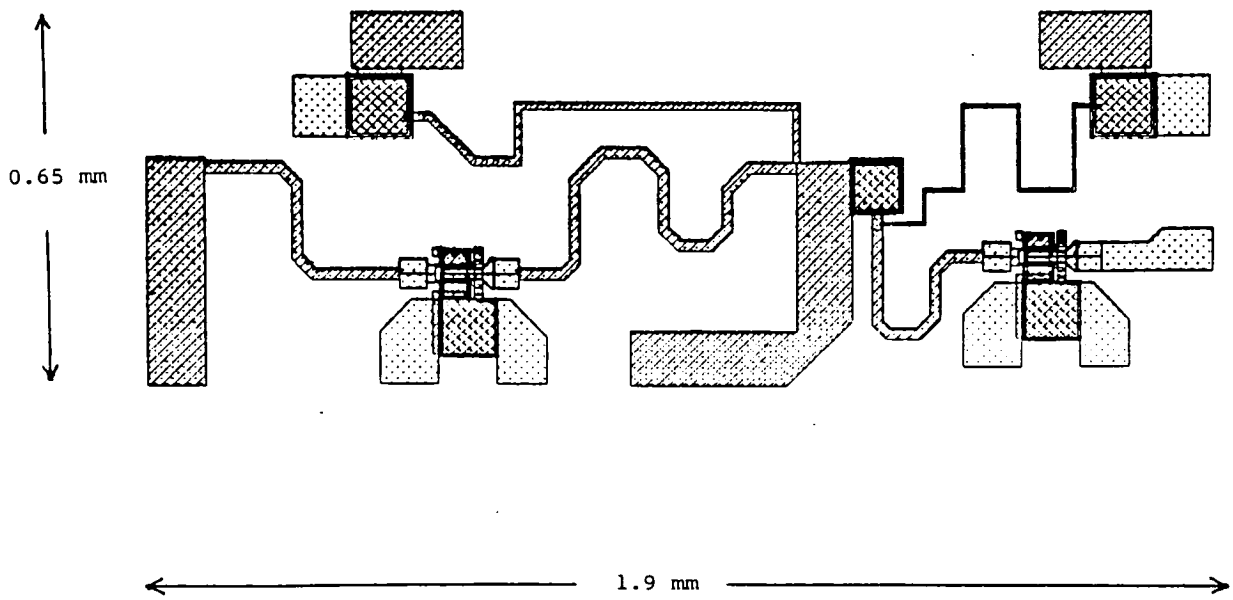


Figure 38. CALMA Layout for First Two Stages of Gain Control Amplifier

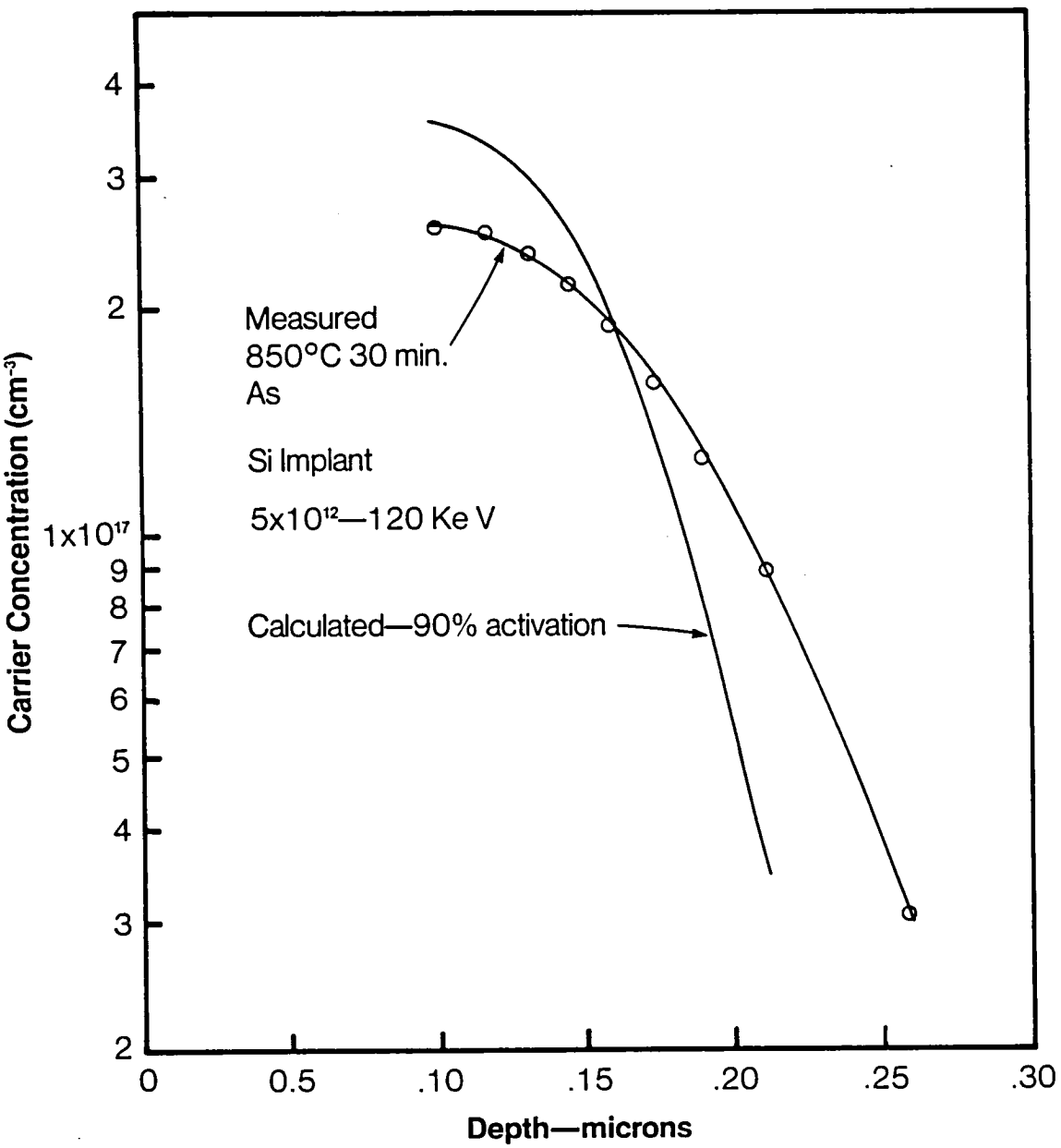


Figure 39. Profile of Ion Implant

Table 1. NASA's Key Performance Goals

Design Parameter	Performance Goal
RF Band	27.5 - 30 GHz
IF Center Frequency	Between 4-8 GHz
Noise Figure at Room Temperature	≤ 5 dB
RF/IF Gain	≥ 30 dB at highest level of gain control
Gain Control	At least six levels; 30, 27, 24, 20, 17 dB and Off.
Phase Control	5 bits; each bit $\pm 3^{o}$ at band center
Module Power Consumption	250 mW in all states except OFF. In OFF state, 25 mW.
Phase and Gain Control	Operate on digital input.
Mechanical Design	Fully monolithic construction; compatible with 30 GHz spaceborne phased array applications.
Unit Cost	Less than $1000 (1980 dollars) in unit buys of 5000 or more

Table 2. Proposed Initial Low-Noise FET Design

GATE LENGTH	L = 0.25 MICRONS
UNIT GATE WIDTH	W = 50 MICRONS
CHANNEL THICKNESS	A = 0.15 MICRONS
DOPING DENSITY	$N = 2.5 \times 10^{17}$
TOTAL GATE WIDTH	Z = 100 MICRONS
GATE-SOURCE SPACING	L_{SG} = 0.75 MICRONS
GATE METAL RESISTIVITY	$\rho = 4 \times 10^{-6}$ OHM-CM
SPECIFIC CONTACT RESISTANCE	$R_C = 10^{-6}$ OHM-CM^2
	A_1 = 0.22 MICRONS
	A_2 = 0.15 MICRONS
SEE FIGURE 19	$N_1 = 2.5 \times 10^{17}$
	$N_2 = 2.5 \times 10^{17}$

CALCULATED NOISE FIGURE = 2.3 DB AT 32 GHz

Table 3. Calculated Parameters for FET Design

S Parameters (29 GHz)

$S_{11} = .75 \angle -70°$
$S_{12} = 1.06 \angle 79.8°$
$S_{21} = .086 \angle 79.7°$
$S_{22} = .73 \angle -45°$

Noise Parameters (29 GHz)

$F_{MIN} = 2.6$ dB
$R_n = 48$ ohms
$\Gamma_o = .64 \angle 43.9°$
$\Gamma_L = .67 \angle 51.1°$
$G_a = 5$ dB

Gain Parameters (29 GHz)

$K = 1.14$
$G_{MAX} = 8.63$ dB
$\Gamma_{ms} = .87 \angle 80°$
$\Gamma_{ml} = .87 \angle 57°$

Table 4a. S Parameters with No C_{dg} or Ls

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
21500.00	.95< -46	1.25< 116.0	.020< 120.2	.87< -28	1.95	-.03
23000.00	.94< -49	1.23< 111.8	.022< 118.2	.87< -30	1.80	.01
24500.00	.93< -52	1.21< 107.7	.025< 116.3	.87< -32	1.64	.05
26000.00	.93< -54	1.18< 103.7	.027< 114.3	.86< -34	1.47	.10
27500.00	.92< -57	1.16< 99.7	.030< 112.3	.86< -36	1.30	.15
29000.00	.91< -60	1.14< 95.8	.032< 110.2	.86< -38	1.11	.20
30500.00	.90< -63	1.11< 92.0	.035< 108.2	.85< -40	.92	.25
32000.00	.90< -65	1.09< 88.3	.037< 106.2	.85< -42	.73	.31
33500.00	.89< -68	1.06< 84.6	.040< 104.2	.85< -44	.53	.37

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

Table 4b. S Parameters with No C_{dg}, But with Ls

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
21500.00	.88< -45	1.24< 111.5	.040< 174.5	.84< -26	1.85	-.06
23000.00	.87< -48	1.22< 107.4	.047< 174.0	.84< -27	1.70	-.07
24500.00	.86< -50	1.20< 103.5	.055< 173.2	.84< -29	1.55	-.08
26000.00	.85< -53	1.18< 99.6	.063< 172.3	.83< -31	1.40	-.09
27500.00	.83< -56	1.15< 95.9	.073< 171.3	.83< -33	1.25	-.09
29000.00	.82< -59	1.13< 92.2	.083< 170.1	.83< -34	1.08	-.10
30500.00	.81< -61	1.11< 88.7	.094< 168.7	.83< -36	.92	-.10
32000.00	.80< -64	1.09< 85.2	.106< 167.3	.82< -38	.75	-.10
33500.00	.79< -67	1.07< 81.8	.119< 165.8	.82< -40	.57	-.10

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

Table 5. S Parameters for Complete Model, Including Ls and C_{dg}

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
21500.00	.82< -55	1.17< 99.9	.080< 68.9	.77< -35	1.39	.90
23000.00	.80< -58	1.15< 95.6	.081< 70.0	.76< -37	1.22	.96
24500.00	.79< -61	1.13< 91.4	.082< 71.7	.75< -39	1.05	1.01
26000.00	.77< -64	1.11< 87.4	.083< 73.9	.74< -41	.87	1.06
27500.00	.76< -67	1.08< 83.5	.084< 76.5	.74< -43	.69	1.11
29000.00	.75< -70	1.06< 79.8	.086< 79.7	.73< -45	.51	1.14
30500.00	.73< -73	1.04< 76.2	.088< 83.2	.72< -47	.33	1.17
32000.00	.72< -76	1.02< 72.8	.091< 87.0	.72< -49	.15	1.17
33500.00	.71< -79	1.00< 69.4	.095< 90.9	.71< -51	-.04	1.16

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

F MHZ	SOURCE REFL. COEFF. MAGN. <ANGLE	LOAD REFL. COEFF. MAGN. <ANGLE	GMAX DB
*500.0	WARNING: POTENTIALLY UNSTABLE CIRCUIT		
21500.0	.86< 67	.82< 52	11.67
*000.0	WARNING: POTENTIALLY UNSTABLE CIRCUIT		
23000.0	.91< 70	.89< 53	11.52
24500.0	.96< 73	.95< 54	10.69
26000.0	.91< 75	.90< 54	9.69
27500.0	.88< 78	.87< 55	9.09
29000.0	.87< 80	.86< 57	8.63
30500.0	.86< 83	.86< 58	8.27
32000.0	.86< 86	.86< 59	7.98
33500.0	.86< 88	.86< 61	7.76

FILE NAME• 'TRAINFO' • 'TRLINES' • 'LANGE' • 'NEW' OR 'QUIT'

III. REFERENCES

1. K. Kurokawa and W.O. Schlosser, "Quality Factor of Switching Diodes for Digital Modulation", Proc. IEEE, vol. 38, pp. 180-181, January 1970.

2. V. Sokolov, J. Geddes, A. Contolatis, P. Bauhahn and C. Chao, "A Ka-Band GaAs Monolithic Phase Shifter", IEEE Trans. Microwave Theory Tech., vol. MTT-31, December 1983.

3. H.A. Atwater and R.W. Sudbury, "Use of Switching Q in the Design of FET Microwave Switches", in MTT-S Int. Microwave Symp. Dig., pp. 370-372, June 1981.

4. W.V. McLevige and V. Sokolov, "Resonated GaAs FET Devices for Microwave Switching", IEEE Trans. Electron Devices, vol. ED-28, pp. 198-204, February 1981.

5. Y. Ayasli, A. Platzker, J. Vorhaus, and L.D. Reynolds, Jr., "A Monolithic Single-Chip X-Band Four-Bit Phase Shifter", IEEE Trans. Microwave Theory Tech. vol. MTT-30, pp. 2201-2206, December 1982.

6. R.A. Gaspari and H.H. Yee, "Microwave GaAs FET Switching", in 1978 IEEE Int. Microwave Symp. Dig., pp. 58-60.

7. C.A. Liechti, "Performance of Dual-Gate GaAs MESFETs as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators", IEEE Trans., Microwave

Theory and Tech., pp. 461-469, June 1975.

8. A.K. Wortman and E.E. Kohn, "A Monolithic Integrated Schottky Diode for Microwave Mixers", Solid State Electronics, 18, pp. 1095-1098, December 1975.

9. W. Kellner, et.al., "Design Considerations for Planar Schottky Barrier Diodes", Solid State Electronics, 23, pp. 9-15, January 1980.

10. N. Yokoyama, T. Oknishi, K. Odani, H. Onodera and M. Abe, "Ti/W Silicide Gate Technology For Self-Aligned GaAs MESFET VLSI's", Tech. Digest IEDM 80 (December 1981).

11. B.S. Hewitt, et.al., "Low-Noise GaAs MESFETs: Fabrication and Performance", Inst. Phys. Conf. Ser. No. 33a, pp. 246-254, 1977.

12. H. Fukui, "Optimal Noise Figure of Microwave GaAs MESFETs, "IEEE Trans. Elect. Dev., 26, pp. 1032-1037, July 1979.

13. C.A. Liechti, "Microwave Field-Effect Transistor - 1976", IEEE Trans. MTT, 24, pp. 279-300, June 1976.

14. R.A. Pucel, H.A. Haus, H. Statz, "Signal and Noise Properties of Gallium Arsenide Microwave Field-Effect Transistors", in Advances in electronics and Electron Physics, 38, p. 195, 1975.

15. P.G. Borden, "Substrate Conduction in GaAs MESFETs", Electronics Letter, 15, pp. 307-308, 1979.

16. L.F. Eastman and M.S. Shur, "Substrate Current in GaAs MESFETs", IEEE Trans. Electron Dev., 26, pp. 1359-1361, September 1979.

17. J.C. Voker, et.al., "Novel Microwave GaAs Field-Effect Transistor", Electronics Letter, 15, pp. 627-629, September 1979.

18. C.H. Oxley, et.al., "Q Band (26-40 GHz) GaAs FETs", 1981 IEDM Digest, pp. 680-683.

19. P.W. Chye and C. Huang, "Quarter Micron Low Noise GaAs FETs", IEEE Electron Device Letters, 13, pp. 401-403, December 1982.

20. C.H. Oxley, et.al., "Q Band (26-40 Ghz) GaAs FET Single Stage Amplifier", Electronics Letters, 18, pp. 260-262, March 18, 1982.

21. H. Fukui, "Design of Microwave GaAs MESFETs for Broad-Band Low-Noise Amplifier", IEEE Trans. MTT, 27, pp. 643-650, July 1979.

22. H. Fukui, Addendum to above, IEEE Trans. MTT, 29, October 1981.

23. W.A. Suter, "Feedback and Parasitic Effects on Noise", Microwave Journal, p. 123, February 1983.

24. H. Yamasaki and J.M. Schellenberg, "Design of Millimeter-Wave FETs", Proc. GaAs and Related Compounds, 1981, Olso, Japan.

The reverse of this page is blank.