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FINAL REPORT

AUTONOMOUS INTEGRATED RECEIVE SYSTEM (AIRS)
REQUIREMENTS DEFINITION

VOLUME III. PERFORMANCE AND SIMULATION

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MD 20771

TECHNICAL OFFICER: MR. TOM ROBERTSON

CONTRACT NO. NAS 5-26772

AUGUST 1984

LinCom Corporation
P.O. BOX 2793D LOS ANGELES, CALIFORNIA 90053

TR-0884-8211

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1.0 INTRODUCTION AND SUMMARY

The AIRS study consists of two phases performed over a period of two years. The first phase of this study was devoted to define the functional requirements of AIRS, to define the testing required to demonstrate its performance, to provide an assessment of the technology and cost involves in such an undertaking, and to prepare a specification based on the above findings. This phase of the AIRS study were documented in Vol. II and the accompanying functional specification of the final report.

The purpose of the Phase II study is to develop a computer model of the AIRS, as defined in the Phase I sutdy, to perform a computer simulation of the AIRS, and provide simulation results predicting the performance of the AIRS. The emerging TDAS requirements and techniques to enhance the AIRS capabilities were also incorporated into the AIRS baseline during this period. This volume of the final report serves to document the Phase II effort. The accompanying AIRS simulation software package has been installed at the Goddard CLASS computer. Instructions on using the simulation is contained in a CSS file called AIRS.

1.1 Organization and Summary

This volume is organized into 5 sections and 11 appendices. Section 2 discusses from a system operation point of view the autonomous and integrated aspects of the operation of the AIRS. The advantages of AIRS compared to the existing SSA receive chain equipment are highlighted. The three modes of AIRS operation are addressed in detail.

The configurations of the AIRS are defined as a function of the operating modes and the user signal characteristics in Section 3. Each AIRS configuration selection is made up of three components: the

hardware, the software algorithms and the parameters to be used by these algorithms. These components and the rules for their selections are treated in this section. Notice that the first two components are modeled in the AIRS simulation software. The final parameter selection process is to be accomplished via the simulation software.

A comparison between the AIRS and the wide dynamics demodulator (WDD) is provided in Section 4. They are compared in terms of their functional characteristics and implementation techniques. This serves to highlight some of the improvements that are designed into the AIRS. In addition, some unique features of AIRS are given.

The final section of this report is devoted to describing the organization of the AIRS analytical/simulation software. Since the algorithms developed in the software simulation can be transferred to the AIRS microprocessor with minor modifications, a strict Monte Carlo technique is adopted whenever possible. In the cases where the Monte Carlo technique is impractical and/or overly time consuming, the software is supplemented with analysis.

The modeling and analysis for simulating the performance of the PN subsystem is documented in detail in Appendix A and B. The acquisition performance is treated in Appendix A. The acquisition performance is determined based on the assumption that the code uncertainty region is uniformly distributed. In practice, a truncated 3-sigma Gaussian distribution is more appropriate since the actual received signal code epoch is more likely to be within the center of the predicted uncertainty region. If this is the case then the search should spend more time in the vicinity of the center of the uncertainty region. It is estimated that the acquisition time determined with the AIRS

simulation could be improved by a factor of 2 to 4. The analysis employed in Appendix A is not restricted to CCD matched filters. If a different implementation is used, e.g., using digital matched filter, the AIRS simulation is also appliable. However, when a digital matched filter implementation is used, the signal must first be sampled and hard-quantized. This introduces a 2 dB loss to the SNR. This factor must be accounted for when using the simulation.

The tracking performance of the PN subsystem is treated in Appendix B.

The frequency acquisition technique using a frequency-locked loop is documented in Appendix C.

The portion of the AIRS simulation software concerning the PN and the frequency acquisition system is documented in Appendix D. A user's manual and sample runs are also given.

The portion of the ARIS simulation regarding the phase-locked loop and the bit sync is documented in Appendix E. Sample runs are also given.

The rest of the Appendices are a collection of miscellaneous items. Appendix F shows how autonomous Doppler compensation can be implemented. Appendix G addresses the technology aspects of employing CCDs for PN acquisiton. Appendix H shows how the AIRS AGC functions and how a signal strength indicator, accurate to 0.2 dB, can be implemented. Appendix I shows that for all practical purposes, the Manchester symbol ambiguity can be resolved within 2000 symbols. Finally, an expression is given in Appendix K to assess the allowable rms phase jitter in order to maintain a mean slip time of over 90 minutes.

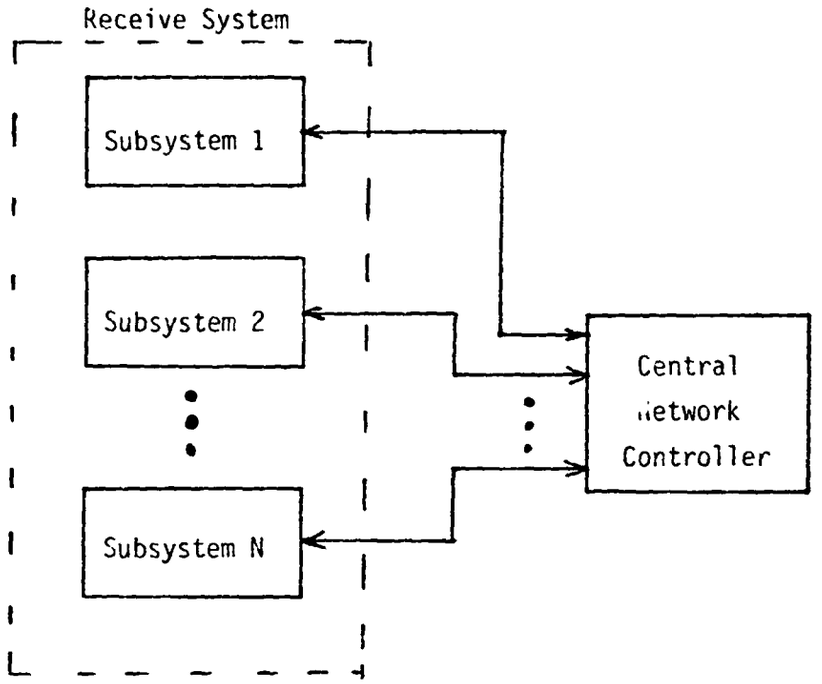
2.0 AUTONOMY AND INTEGRATED OPERATIONS FOR AIRS

This section discusses from a system operational point of view the autonomous and integrated aspects of the Automated Integrated Receiver AIRS (AIRS). The advantages of AIRS compared to the existing SSA receive chain equipment are highlighted. Finally, the three different modes of AIRS operations are discussed.

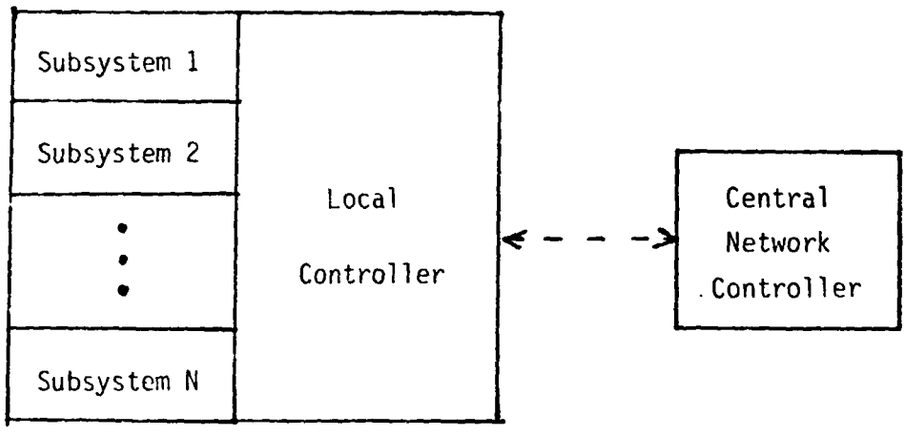
2.1 Introduction

The AIRS is designed to be a stand-alone receiver capable of autonomous, integrated operation for the S-band Single Access (SSA) return link of TDRSS. By autonomous operation, it is meant its capability to demodulate, detect and decode data, and to derive ranging and Doppler information from an IF input with a minimal dependence on an external executive computer such as the Automated Data Processor Equipment (ADPE) at White Sands Ground Terminal (WSGT). In order to achieve autonomous operation, the AIRS is capable of controlling its own receiver functions based on given a priori information as well as currently measured characteristics of the input signal. The AIRS is also an integrated receiver since the subsystems required for PN despreading, carrier and clock recovery, symbol detection and Viterbi decoding are designed, tailored, and interconnected to function as a single dedicated unit.

Figure 2.1 depicts the differences between the autonomous integrated approach and the conventional centralized approach to a receive system design. Notice that in the conventional approach the subsystems are controlled by a central network controller which is external to the receive system. There are no communications and interactions among the subsystems except for the required signal



(a) Conventional Approach



(b) Autonomous Integrated Approach

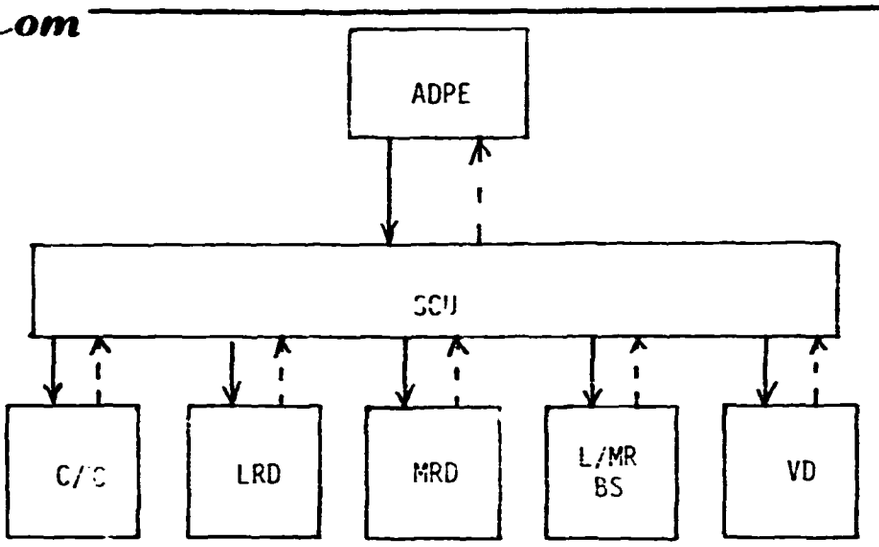
Figure 2.1. Comparison Between Conventional and AIRS Approach to Receive System Architecture.

interfaces. In the autonomous integrated approach, the receive system accepts setup commands from the network controller initially. After initial acquisition, the receive system is normally detached from the controller except for responses to an interrupt command. This is indicated by the dashed line. Notice that the subsystems are integral parts of the receive system and are interconnected among themselves through the local controller. As we shall see, this autonomous integrated structure provides several advantages over the conventional approach.

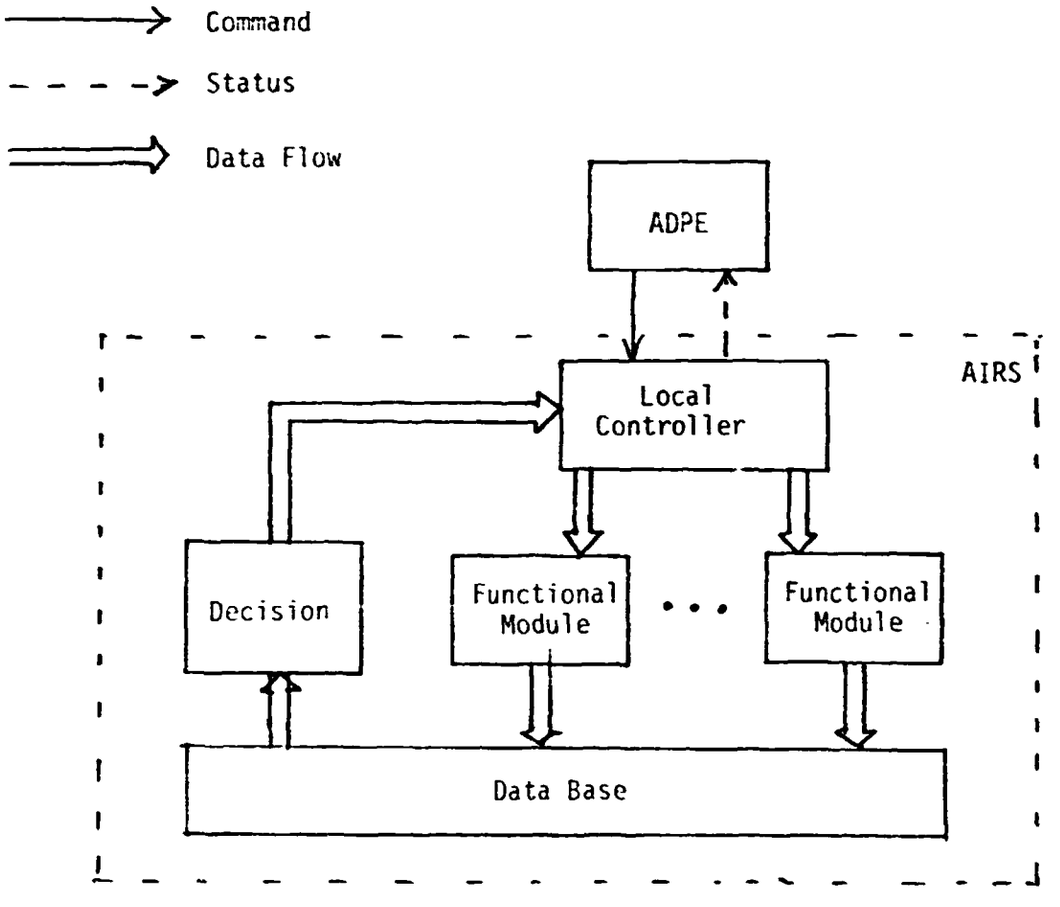
2.2 Advantages of the AIRS Concept

Figure 2.2 highlights the differences between AIRS and the corresponding portion of the current SSA Receive Chain. In the current implementation, the units, i.e., Down Converter/Doppler Correlator (C/C) Low Rate Demodulation (LRD), Medium Rate Demodulator (MRD), Low and Medium Rate Bit Synchronizers (L/MRBS) and the Viterbi Decoders (VD), are controlled directly by the ADPE through the Service Control Unit (SCU). The SCU merely acts as a common point of interface between the ADPE and the various units. There are two types of commands from the ADPE: static setup commands and dynamic Doppler commands. The one-time setup commands are used to configure the parameters of the various units. The dynamic commands are provided continuously throughout a mission and they are the carrier Doppler estimates (used by the C/C) and the PN code chip rate Doppler estimates (used by the LRD). The individual unit reports its status to ADPE through the SCU. The following features of the current system are worth noting:

- Doppler correction commands are required from the ADPE at all times for proper operation.



(a) Existing units in SSA receive chain



(b) AIRS

Figure 2.2.Architectural Comparison of AIRS with existing SSA Receive Chain Configuration

- There are no provisions for the ADPE to issue real-time changes to unit parameters to take advantage of the information provided by the status signals. The only ADPE reaction is to restart the system once an anomaly is detected.
- The individual units function independently of one other.

The AIRS also takes setup commands from and reports its status to ADPE as in the current implementation. However, the AIRS only uses the Doppler correction commands during acquisition. After acquisition, the AIRS generates its own Doppler estimates. Therefore, the interface between the ADPE and the AIRS can be removed after the link has been established except for configuration changes. During acquisition, the setup commands are similar to those issued by the ADPE. However, after acquisition, the AIRS can generate more accurate link characteristics by its own measurement than those provided by the a priori information. These measurements are fed to a decision algorithm (expert system) through a common data bus. The outcomes are used to instruct the local controller to modify the parameters of the functional modules to achieve the best desired performance. The key features of the AIRS are:

- Detached Operation from ADPE
- Real-Time Intelligent Operation
- Integrated Operation
- Self Diagnostics

In what follows, we shall address the advantages provided by the AIRS implementation.

2.2.1 Advantages of Autonomous Operation

There are four major areas where the AIRS autonomous operation is advantageous. These are:

- Reduced Dependence on ADPE
- Ease of Modification
- Real Time Operation
- Improved Performance

2.2.1.1 Reduced ADPE Dependence

Since the AIRS performs its own Doppler compensation once it has acquired, it can operate independent of the ADPE during the tracking operation. The ADPE can be freed to devote its attention to other processing needs of the ground station throughout the rest of the mission. Also, the receive chain operation will not be interrupted by possible disruptions in the ADPE. To accomodate emergency operations, the AIRS allows manual entry to simulate ADPE commands.

2.2.1.2 Ease of Modification

Currently, the setup commands from the ADPE contain both the data link characteristics (e.g., Data Group, Mode, expected signal power, data rates, etc.) as well as the settings for selectable unit parameters (e.g., search rate, IF bandwidths, loop bandwidths, etc.). These parameters are determined by the ADPE based on the estimated return link characteristics. A similar set of software for making that decision are incorporated into the AIRS control so that the only setup commands required from ADPE are those pertaining to data link characterization. This way, the AIRS configuration and parameters setup are completely independent of the ADPE. Any subsequent changes in the receiver structure as a result of new mission requirements or equipment modifications can be handled locally by the AIRS controller and will not impact the ADPE. In other words, future modifications on the AIRS will not alter the AIRS/ADPE protocol and interface. Presently, major ADPE

software revision will be required since the changes must be made compatible with other activities of the ADPE.

2.2.1.3 Real Time Operation

The ADPE setup commands are geared to achieving the "best" performance based on the a priori information on the user link characteristics scheduled for mission support. The receive system parameters are then frozen throughout the mission. However, after the receive system has acquired the user signal, the receive system itself is capable of generating better estimates on the user signal characteristics than those based on a priori information. The best set of receive system parameters may not necessarily be the same as one dictated by the ADPE. In what follows, we shall dwell on some examples to illustrate this point.

2.2.1.3.1 Signal Strength

The coherent AGC in the receive system is capable of providing an accurate measurement on the received signal strength. This information can be used to optimize the carrier and bit sync tracking bandwidths. For example, if the signal strength is higher than the a priori prediction, then the loop bandwidths can be opened up to allow for tracking errors due to phase noise and dynamics. Similarly, the bandwidths can be narrowed if the converse is true.

2.2.1.3.2 Wide Dynamics Operation

After acquisition, the receive system can measure the signal Doppler accurately. It does not have to rely on the ADPE for Doppler correction. This is particularly advantageous during a powered flight. Since the ADPE can only predict the burn occurrence to within ±9 secs, the Doppler correction provided to the SSAR chain can be off by

a frequency rate up to 765 Hz/sec for ±9 secs. The tracking loops in the current receive system must be able to track through this transient. Since the Doppler is internally compensated in the AIRS, the tracking loops will only see the frequency rate for a period of time proportional to the Doppler update rate which is on the order of a second or less. Since a tracking loop is more likely to slip and lose lock while operating under stress, the probability of loss of lock is proportional to the duration of the stress application. Therefore, the AIRS implementation is more tolerant to signal dynamics.

2.2.1.3.3 Reacquisition

Occasionally, the communication link breaks down due to an anamoly during a support mission. Up until the signal is lost, the tracking receiver has the most current estimate on the carrier frequency, PN chip rate, and PN epoch uncertainty. These uncertainties are much smaller than the initial uncertainty predictions given by the ADPE. The AIRS can therefore use this information to help reduce the uncertainty range to be searched during reacquisition. This way, the reacquisition time can be reduced. In the current system (except to some degree in the WDD), this information is ignored and there is no distinction between acquisition and reacquisition.

2.2.1.4 Performance Improvement

The ability to monitor the link conditions allows the AIRS to better match the receiver parameters with the incoming signal characteristics. This translates directly into BER, tracking and ranging performance improvements. The AIRS is also capable of resolving certain cases of I,Q channel ambiguities (e.g. when the data rates are close to each other) that the current system is not capable of doing.

The AIRS relies on its monitor signals to achieve this goal. However, these signals are either unavailable, inaccessible or impractical to be made available to the ADPE in the current system.

Through the use of optimal receiver algorithms, the threshold performance of the AIRS is greatly enhanced. Operationally, this means that the AIRS can be used to support degraded operation involving malfunctioning users.

2.2.2 Advantages of Integrated Operation

The AIRS subsystems are designed and interconnected to achieve the best receive system function as a single entity. This provides several advantages over the current system.

2.2.2.1 Reduced Hardware and Interface Complexity

Since the subsystems are not built as individual units, hardware that perform similar functions can be shared. For example, the analog-to-digital conversion function can be shared by both the carrier and the bit sync loops. Other obvious examples are power supplies and interface signal processors. In addition, since a single vendor is responsible for the AIRS, the interface requirements between the units (e.g. the LRD has to interface with the SCU and the L/MRBS) can be eliminated.

2.2.2.2 Ease of Maintenance and Self Diagnostic Capability

Reduced complexity translates directly into easier maintenance. In particular, because of the digital implementation approach chosen by the AIRS, maintenance is further simplified by reduced analog component counts (required only at the front end of the receive sysem before A/D conversion) and extensive use of digital components/numerical algorithms. Digital components eliminate the traditional analog problems associated with drifts, aging and temperature sensitivity which

requires periodic adjustments. In addition, the numerical algorithms are amendable to self diagnostic procedures which greatly simplify trouble-shooting. Because of the built-in intelligence of the AIRS, self diagnostics can be achieved in many levels. During operation, any anamoly that causes a signal dropout will initiate a self-diagnostic procedure to identify the origin of the failure mechanism, i.e., whether it was a result of the receiver failure or an anamoly in the link condition. The diagnostic procedure, whether during power-up or during operation, will be used to isolate fault to the board level.

2.2.2.3 Performance Improvements

Integrated operations mean that the AIRS subsystem functions are coupled together. This is most noticeable for the various tracking functions (i.e., code, carrier and bit sync loops). The AIRS employs a rather sophisticated data-aided loop (DAL) design for carrier tracking and bit sync. The advanages of a DAL implementation has been demonstrated to some extent by the WDD (for which a rather simple DAL implementation is employed). In particular, the inherent bit sync/data detector performance of the WDD has been demonstrated to be superior than the performance of the WDD used in conjunction with the L/MR bit sync. No doubt, the more sophisticated nature of the AIRS will further enhance this performance capability.

The DAL is also a better design in terms of the carrier tracking and threshold perfomance. The AIRS will have a lower threshold and smaller rms phase jitter for a given CNR input. The AIRS DAL also eliminates undesirable lock points on the S-curve. Thus, it is capable of differentiating between the I and Q channel for unbalanced QPSK signals. This eliminates certain I,Q channel ambiguities associated

with the current system. In addition, since the bit sync and carrier loop acquire simultaneously instead of sequentially, acquisition time is

ced.

The AIRS employs a Doppler compensation loop to minimize the loop stresses. The Doppler loop is coupled with the DAL and improves the tracking and threshold performance. Furthermore, the PN loop is aided by the DAL to further minimize the PN loop stress. This improves the ranging perfomance.

2.3 AIRS Operation Modes

The AIRS has three modes of operation. The two autonomous modes (Modes 1 and 2) are very similar except for the receiver configurations. The other mode, the test mode, is a mode where the receiver is operated manually by a keyboard/display via an external interface. The receiver parameter selections are menu-driven to allow friendly user interface. All three modes can be controlled by a local controller. Mode 1 and Mode 2 are normally controlled by a remote controller/computer such as the ADPE.

2.3.1 Mode 1 - Normal Mode

The flow diagram for the autonomous modes (Modes 1 and 2) of operation is shown in Figure 2.3. The AIRS accepts the setup commands from the ADPE. The setup commands define the user signal characteristics as shown in Figure 2.4. Based on these commands, the receiver will be configured and parameters will be selected by the AIRS control unit to best-match the data characteristics. The receiver configuration and parameters are distinct for Mode 1 and Mode 2. For Mode 1, the flow diagram for acquisition is shown in Figure 2.5. The various loops are configured to take advantage of all the information of

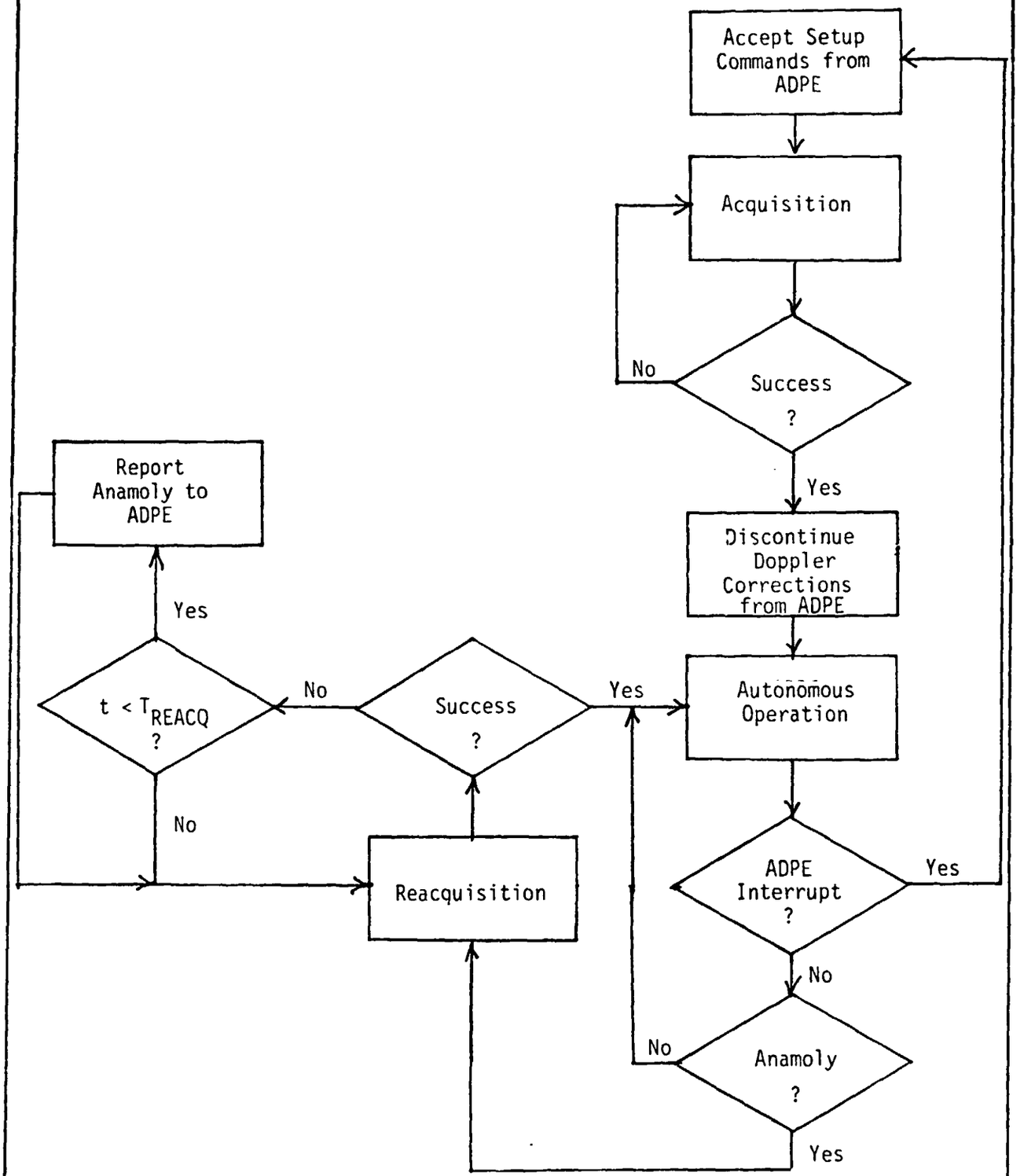


Figure 2.3. Flow Diagram for Autonomous Mode (Mode 1 & 2) Operations.

Mode Select (1, 2, or 3)

PN Code Tap Setting

I and Q Data Symbol Rate

I/Q Power Ratio

Code Search Direction

Epoch Delay

Search Range

Register A PN Code Kernal

Register B PN Code Kernal

DG-1/DG-2 Select

BPSK/QPSK Mode

Acquisition Start

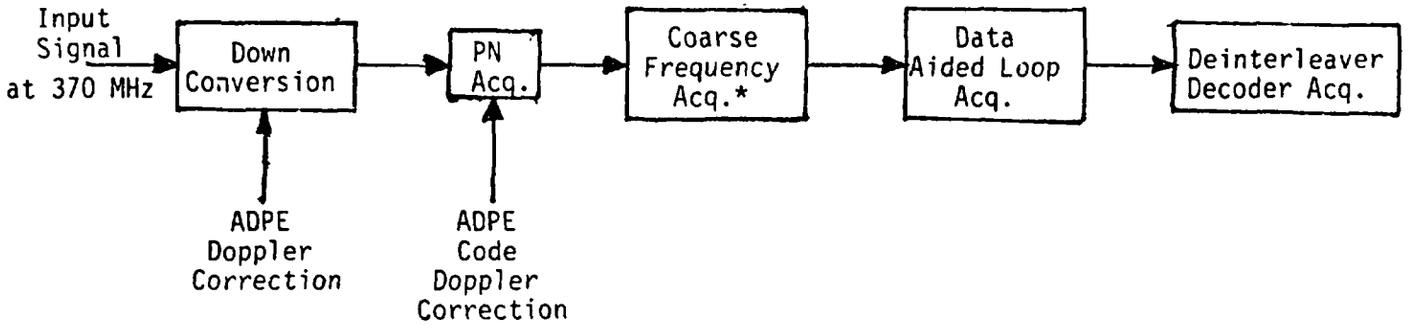
Code/Uncoded

Combined/Uncoded

Differential Format

EIRP

Figure 2.4. List of Setup Command Functions



*Use Frequency Tracking Loop to acquire carrier frequency (coarse acq.) and switch to DAL (fine acq.)

Figure 2.5. Mode 1 Acquisition [illegible]gram

the data characteristics of the incoming signal. For example, both the I and Q channel signals are processed for acquisition and tracking and the respective data rates are used to set the various bandpass filter bandwidths. (Currently, only the strong channel is used.) During acquisition, the ADPE also provides AIRS with the dyanmic commands which are the carrier Doppler and code Doppler corrections. Once AIRS has acquired, it signals ADPE to discontinue supporting the Doppler compensation. From this point, the AIRS is completely independent of the ADPE and operates functionally as shown in Figure 2.6. However, the ADPE can interrupt AIRS at any time to regain control the AIRS.

During autonomous oepration, the AIRS continually monitors for any system anamoly such as loss of lock. If such an anamoly occurs, the AIS enters a reacquisition mode. In this mode, the AIRS tries to reacquire the signal in the most efficient manner by using all the signal information mointored by the AIRS prior to the anamoly. If the reacquisition is successful, the AIRS resumes autonomous oepration. If the AIRS cannot acquire, after a preassigned amount of time determined by the search range uncertainties, the anamoly will be reported to ADPE for attention. The AIRS then continues to reacquire until the ADPE issues new setup command.

2.3.2 Mode 2 - Felxible Data Format Mode

The operational flow of this mode is very similar to mode 1 except for the receiver configurations during acquisition and tracking. The purpose of this mode is to allow the user to switch their baseband data charateristics (data rates, data formats) without having to reacquire the PN code and the carrier. To achieve this goal, the carrier loop and the bit sync must be decoupled. In addition, the AIRS cannot use the

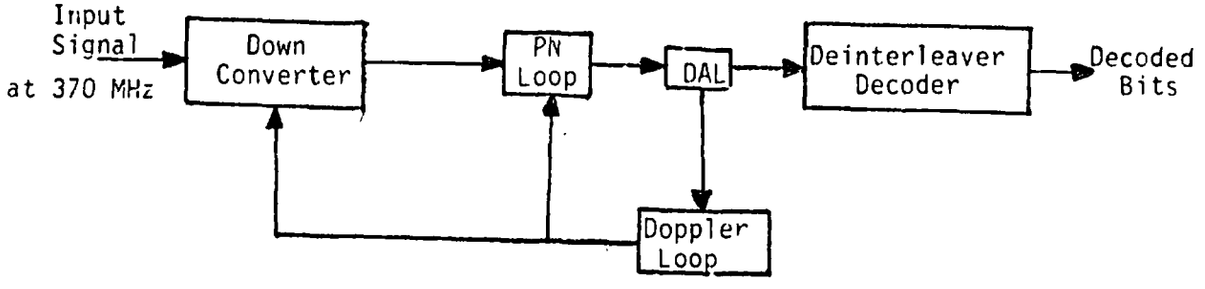


Figure 2.6. Function Diagram of AIRS during autonomous operation (Mode 1).

data rates information in the PN and the carrier loops. It can only assume that the highest data rate used is compatible with the user transmitter EIRP. Figure 2.7 shows the acquisition flow diagram for mode 2. Note that two separate bit syncs are used and they acquire independently. After acquisition the functional diagr. is shown in Figure 8. Note that in this case, the bit syncs can lose lock temporarily while the data rates are being switched. However, the PN and carrier loops will still be in lock. Therefore, no PN and carrier loop reacquisition are necessary.

2.3.3 Mode 3 - Test Mode (Manual Mode)

In the test mode, the receiver is configured via external interactive keyboard commands. The receiver parameters must also be selected externally. In this mode, the AIRS allows external access to various portions of the receiver. This also allows an operator to experimentally optimize the receiver performance by deviating from the autonomous control program of the receiver. This feature is helpful if the AIRS is to be further modified to accomodate new requirements after its development.

3.0 AIRS CONFIGURATIONS

Since the AIRS must accomodate a variety of data modulation schemes under three different modes of operation, it possesses a multitude of configurations. Surprisingly, the amount of hardware that needs to be reconfigured is relatively small. This can be attributed to the use of digital/microprocessor control techniques in the AIRS architecture. As will be demonstrated shortly, any change in data modulation can usually be accomodated via changing some nominal clock rates and parameters used in the software.

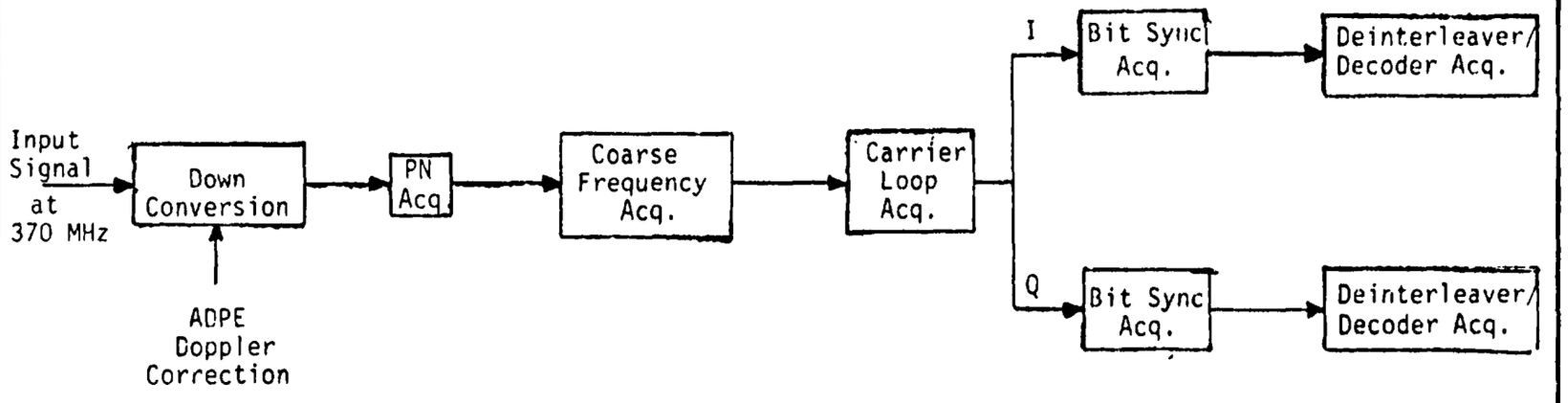


Figure 2.7. Mode 2 Acquisition Flow Diagram

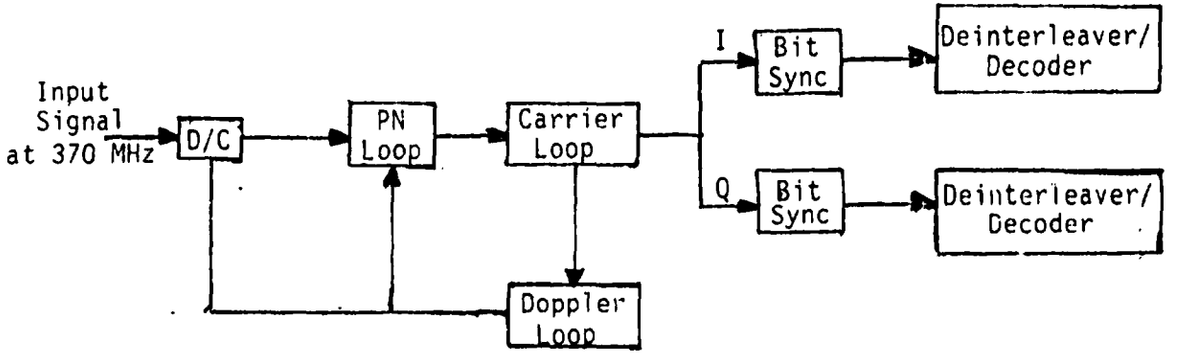


Figure 2.8. Functional Diagram of AIRS during Autonomous Operation (Mode 2)

Figure 3.1 is the functional block diagram of the AIRS. The received IF signal is split into two channels. These channels are first processed by the PN subsystems if they are spread. The I and Q channels are then coherently demodulated and A/D converted to digital samples. These samples, at a relatively high rate are processed in the digital signal processing (DSP) subsystem to generate the detected bits or symbols, carrier frequency and phase errors, bit sync timing errors, as well as other monitoring signals. The data rates of the errors and monitoring signals at the output of the DSP subsystem are typically reduced to a few kHz so that they can be processed by the succeeding microprocessor software. Based on these errors and monitoring signals, the software residing in the microprocessor then makes fine adjustment on the control and clock inputs to the A/D and DSP subsystem so as to maintain coherent demodulation and synchronous data detection. The exact control applied to these systems is a function of the modulation format and the operating mode selected.

Depending on the user data characteristics and the operating mode, the AIRS selects a particular configuration by arranging the hardware paths, the appropriate PSP blocks, the set of appropriate software algorithms, and a set of appropriate receiver parameters.

The user data characteristics are determined from the interface data supplied by the service control unit (SCU). Figure 3.2 shows the data characteristics that can be derived from the original SCU data. The effective C/N_0 can be estimated based on the minimum required E_b/N_0 and the data rate. The selection of the receiver mode (IRM) can be made via external switches or as a new item supplied by the SCU data.

The AIRS configuration table is shown in Figure 3.3. Depending on

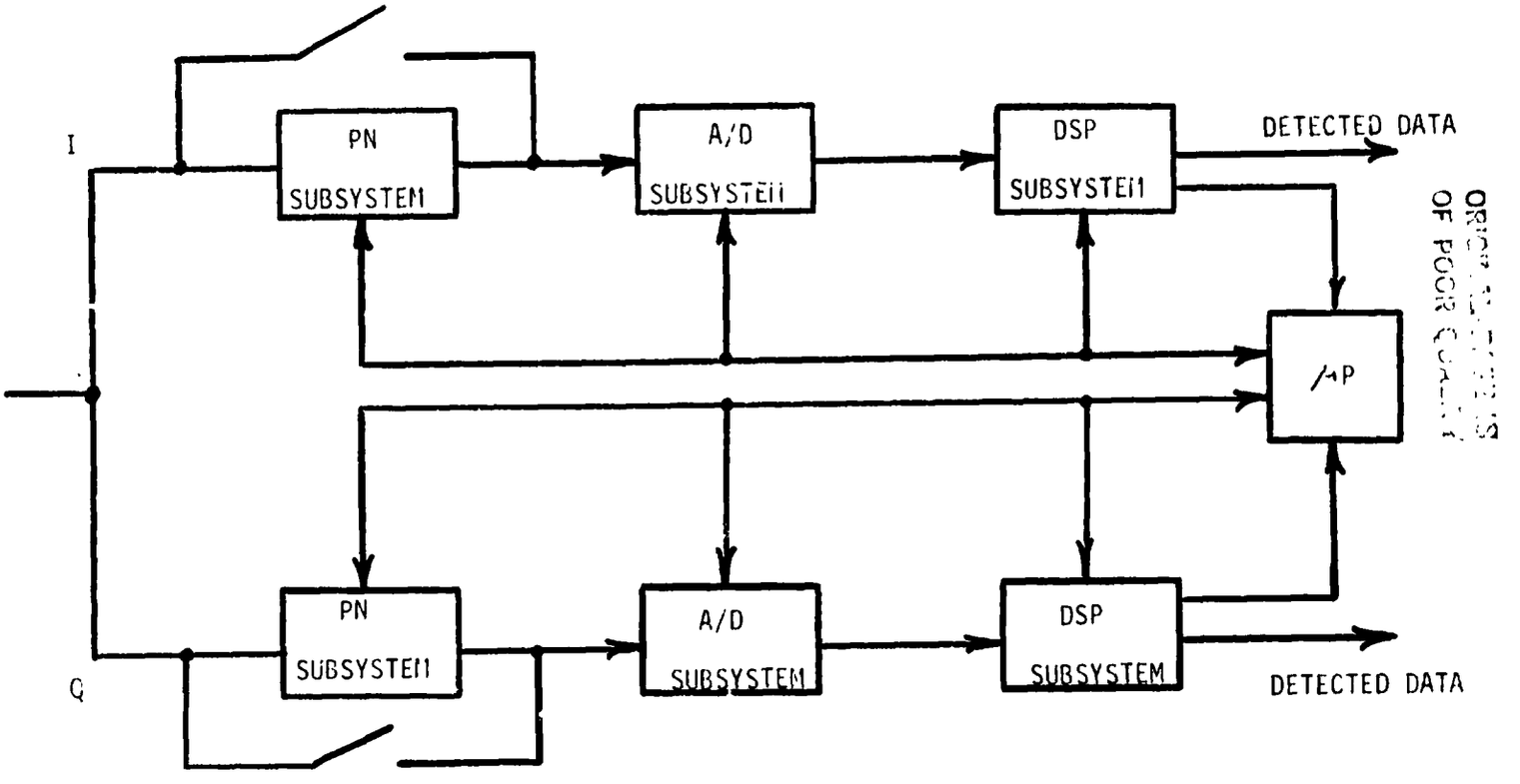


Figure 3.1. AIRS Functional Block Diagram.

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DATA CHARACTERISTICS

PN USE:
IPN/0 = I&Q (DG1-1,2)
1 = I ONLY (DG1-3)
2 = NONE (DG2)

SYMBOL FORMAT: (=BIT FORMAT IF UNCODED)
ISF/0 = BI-PHASE
1 = NRZ
2 = UNKNOWN

MODULATION FORMAT:
IMF/0 = BPSK (DG2)
1 = SQPSK (DG2)
2 = UQPSK (DG2)
3 = BPSK*2 (DG1)
4 = UNKNOWN (DG2)

CODE RATE:
ICR/0 = UNCODED
1 = RATE 1/2
2 = RATE 1/3
3 = UNKNOWN

RECEIVER MODE SELECTION:
IRM/0 = NORMAL MODE
1 = FLEXIBLE DATA FORMAT MODE
2 = TEST MODE

OTHER PARMETERS:
I/Q POWER RATIO
EFFECTIVE C/N_o
I BIT RATE
Q BIT RATE

DERIVED INFORMATION:
1. SYMBOL RATE = BIT RATE / CODE RATE
2. I CHANNEL EFFECTIVE C/N_o = EFFECTIVE C/N_o * IQPR/(1 + IQPR)
3. Q CHANNEL EFFECTIVE C/N_o = EFFECTIVE C/N_o / (1 + IQPR)
IQPR = I CHANNEL POWER / Q CHANNEL POWER

Figure 3.2. User Data Characteristics.

AIRS CONFIGURATIONS

IPN	PN CONFIGURATION
0	2-CHANNEL PN TRACK, STRONG CHANNEL ACQ
1	I-CHANNEL PN TRACK AND ACQ
2	E 'ASS PN SYSTEM

ISF	BIT SYNC CNOFIGURATION
0	BI-PHASE (NRZ @ 2*SYMBOL RATE)
1	NRZ
2	N/A

ISF	FLL CONFIGURATION
0	BI-PHASE (NRZ @ 2*SYMBOL RATE)
1	NRZ
2	BI-PHASE

IMF	FLL CONFIGURATION
0	IzQ-QzI
1	IzQ-QzI
2	IzQ-QzI
3	2 * (IzQ-QzI)
4	IzQ-QzI

IRM	IMF	PLL CONFIGURATION
0	0	DATA-AIDED 2-PHASE COSTAS
	1	DATA-AIDED 4-PHASE COSTAS
	2	DATA-AIDED 4-PHASE COSTAS
	3	2*DATA-AIDED 2-PHASE COSTAS
	4	N/A
1	0	N/A
	1	N/A
	2	N/A
	3	2*2-PHASE COSTAS
	4	4-PHASE COSTAS

Figure 3.3. AIRS Configuration Table.

the data characteristics represented in Figure 3.3 by the various values of the identifiers IPN, ISF, IMP, and IRM (see Figure 3.2 for what they represent), the AIRS uses different configurations for the PN subsystem, bit syncs, the frequency-locked loop (FLL) and the phase-locked loop (PLL).

3.1 Configuration Rules

Before describing in detail each of the subsystems and laying out all the different configurations, it is instructive to understand the basic rules being applied.

3.1.1 Normal Mode

In the normal mode of operation, all the necessary information on the data modulation format are known. The AIRS will take advantage of this knowledge to configure the receiver to exploit the modulation structure. The tracking loops, i.e., PN tracking loop, carrier recovery loop and bit sync will operate on both the I and Q channel in a coupled fashion. For example, in the DG-1 mode, there are two independent data channels. However, since they both have the same carrier, the AIRS carrier recovery loop processes the phase error samples from both channels. As another example, data-aided loops are used to obtain the optimum performance.

3.1.2 Flexible Data Format Mode

The flexible data format mode only affects the receiver configuration following PN despreading. Since the data modulation format cannot be assumed known at any given time, the carrier loops must be decoupled from the bit sync.

3.2 AIRS Subsystem Hardware

As shown in Figure 3.1, there are three distinct hardware

subsystems. They are the PN subsystem, the A/D subsystem and the DSP subsystem.

3.2.1 PN Subsystem

The PN subsystem is used for DG-1 signal when the input signal is spread. Initial acquisition is accomplished by using the CCD matched filters when the input data rate is less than 50 Ksps.* The CCD technique speeds up the acquisition process considerably at low data rates by providing a parallel processing capability. At higher data rate, because of the low number of PN chips to data bit ratios, the advantages of the CCD matched filter diminishes (see Appendix A). In addition, less than 1 sec acquisition time can be accomplished using conventional sequential detection schemes. Therefore the AIRS uses sequential detection for data rate higher than 50 Ksps. The use of sequential detection, however, does not involve additional hardware, since the correlators required for sequential detection are shared with the correlators required for tracking.

AIRS uses only one PN channel for acquisition, since there is no simple way to take advantage of the signal power provided by the other PN channel to aid acquisition, with the same level of complexity in hardware. In case of DG1 mode 1 or 2, the PN signal with the higher power is used. For DG-2, the PN subsystem is bypassed.

A dithered early-late gated loop structure is used for PN tracking. The dithered method minimizes the effects of hardware imbalances while providing a potential 3 dB improvement over the strict early-late gated loop. For DG1 mode 1 and 2, the dithering is done on

*When Manchester coding is used, 25 Ksps.

both the I and Q channel so that error signals from both channels can be used. This provides a potential 3 dB improvement over a scheme which tracks only one channel if both the I-Q channels have the same power. For DG1 mode 3 where only the I channel is spread, the dithered loop assumes the conventional structure. The details of the PN subsystem operation are described in Appendices A and B.

The CCD acquisition technique is inherently digital in nature so that the CCD acquisition unit interfaces with the AIRS microprocessor software directly. In order to tap the power of the AIRS software, the PN tracking loops and the portion of the PN acquisition system using sequential detection are implemented in a hybrid manner. The outputs of the correlators used in both systems are A/D converted. Loop filtering and sequential detection functions are then performed in software. Figure 3.4 shows the hardware arrangement for the tracking/sequential acquisition subsystem. The accumulator (ACM) is controlled by the dithering signal during tracking. For sequential acquisition, the ACM is controlled by the processor software. The digital data output to the AIRS processor will be on the order of 1 KHz or less.

3.2.2 A/D Subsystem

The A/D subsystem is shown in Figure 3.5. The synthesizer provides the local reference for coherent demodulation. The incoming data is filtered by the bandpass filter. The filter bandwidth is selected as a function of the incoming symbol rate. The bandwidth is selected so as to minimize the signal distortion on the filter output while maintaining the output signal-to-noise ratio to be as high as possible. The baseband signal at the mixer output is amplified to a suitable amplitude for A/D conversion by the gain control amplifier (GCA). The GCA serves

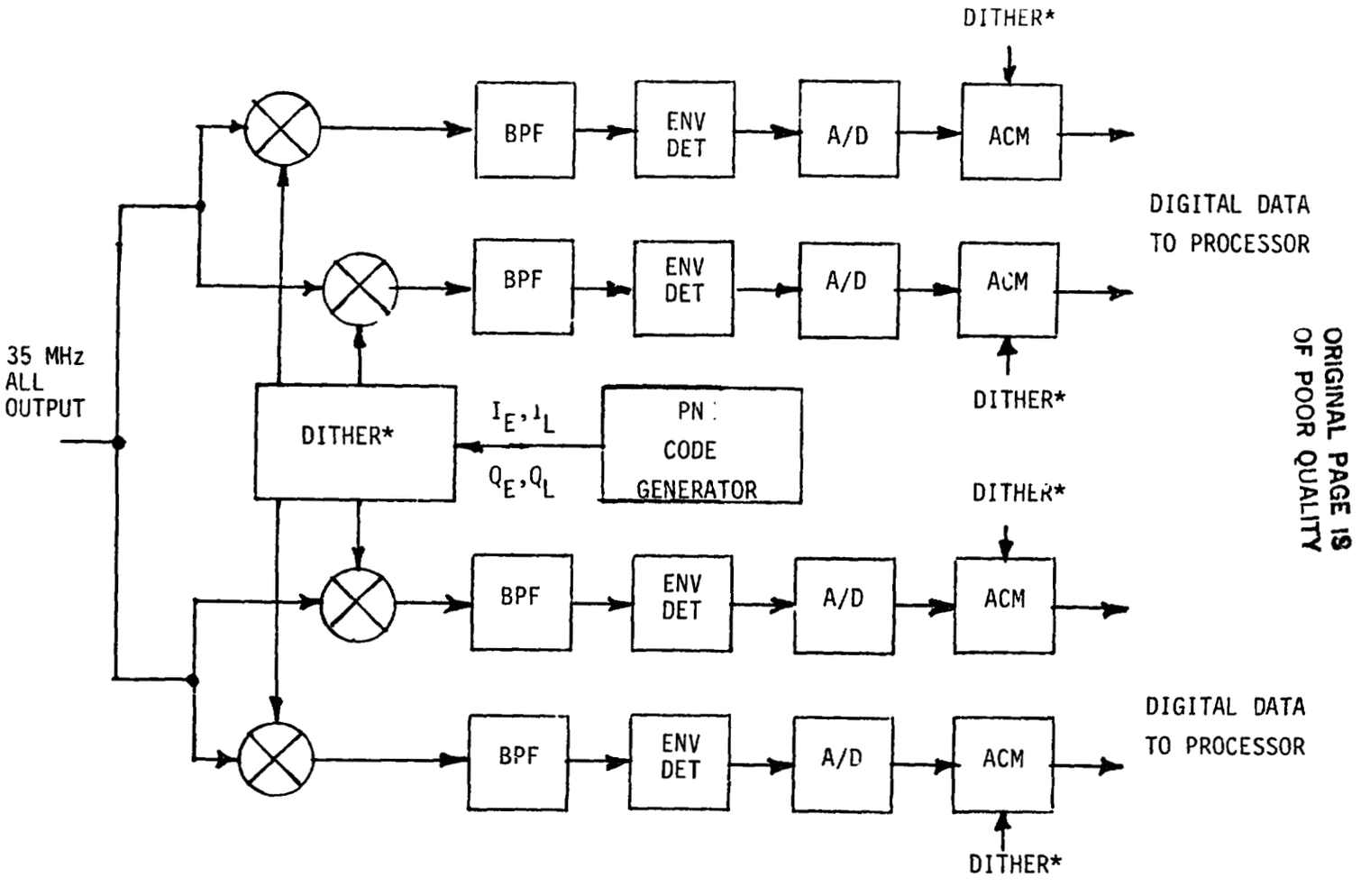


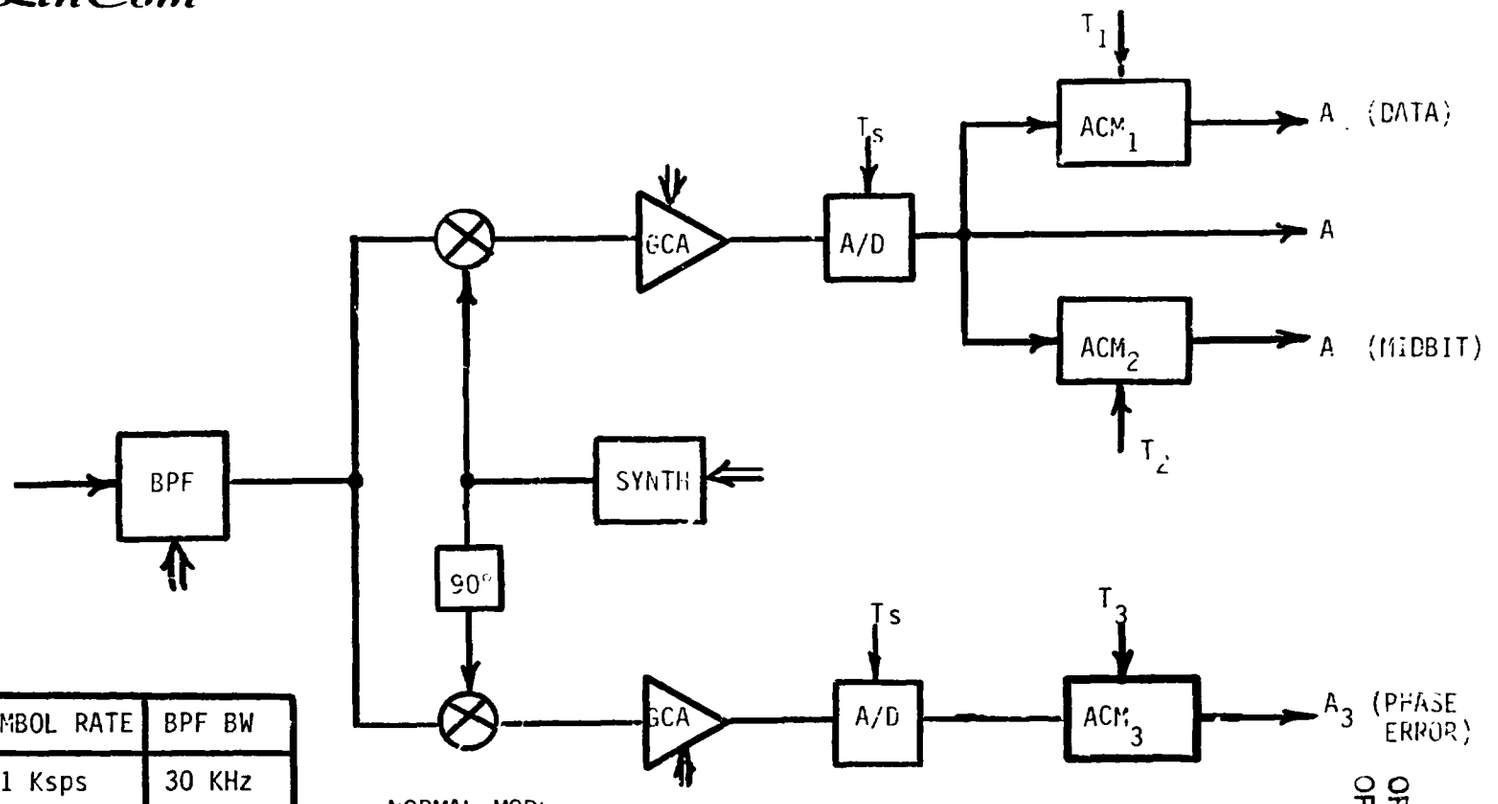
Fig. 3.4. PN Subsystem Hardware

to close the coherent AGC loop.

In the scheme depicted in Figure 3.5, two separate A/D converters are used to sample the inphase and quadrature channel. Another possibility is to use one A/D converter to sample directly at 4x the IF frequency of the incoming signal as done in the Wide Dynamics Demodulator (WDD). This eliminates the need for the two mixers. However, this technique is judged to be unsuitable for the AIRS application as discussed in Appendix I.

The output of the A/D is routed to two accumulators (ACM). ACM_1 (and ACM_3 in the lower branch) is the data accumulator because its dump clock T_1 is normally coherent with the symbol clock so that its output is an approximation to the optimum integrate and dump matched filter detector. Notice that clock for T_1 is higher than T_s. The midbit accumulator ACM_2 (ACM_4 in the lower branch) is normally dumped at the same rate at T_1, however, its phase differs from T_2 by half a cycle. Therefore the accumulator output is approximately the integral of the first half of a symbol and the last half of a previous symbol. This is illustrated in Figure 3.6. However, the clocks for T_1 and T_2 can be related in a different way for some configurations. The A/D samples are also available directly as A_1 (B_1).

In the normal mode of operation, the A/D sampling clock, at an integer multiple of the data rate, is derived from the bit sync clock. In the flexible data format mode operation the sampling rate is set to a rate determined solely by the highest data rate that the signal power can support. This is done becasue the actual data rate can vary without the knowledge of AIRS. Tying up the sampling clock with the data rate does not provide any advantage.



SYMBOL RATE	BPF BW
1 Ksps	30 KHz
5 Ksps	150 KHz
50 Ksps	1.5 MHz
100 Ksps	Bypass

- NORMAL MODE
  - A/D SAMPLING IS TIED TO BIT SYNC
- FLEXIBLE DATA MODE
  - A/D SAMPLING IS NOT RELATED TO BIT SYNC

Figure 3.5. A/D Subsystem.

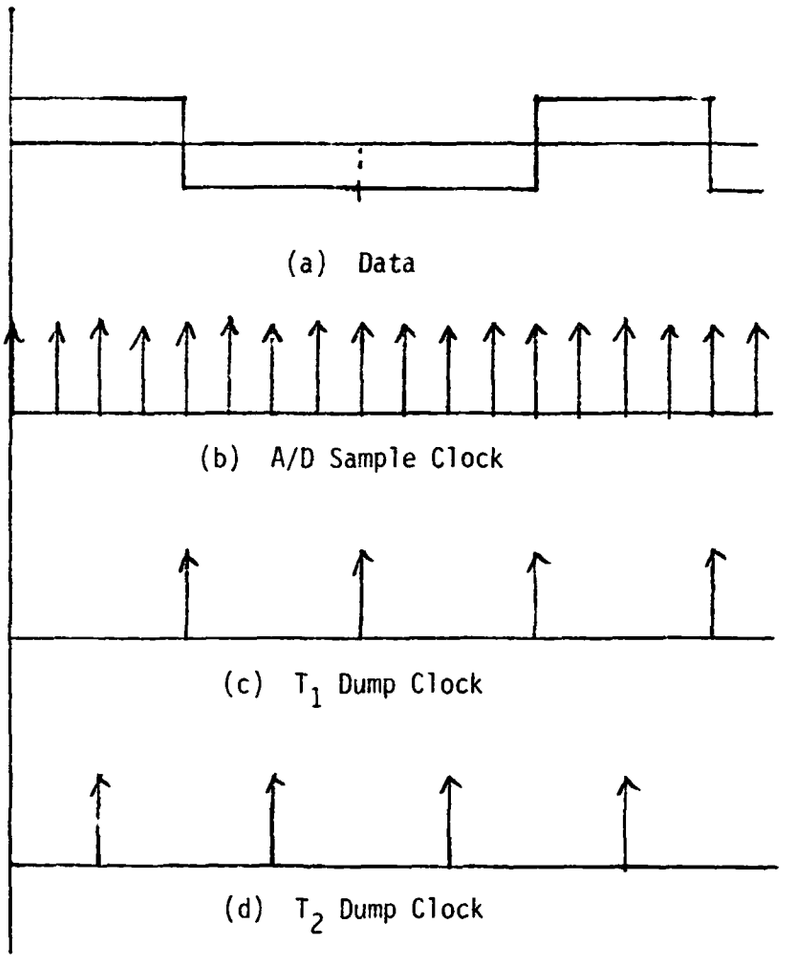


Fig. 3.6. Typical Timing Relationships. (The dump clock transfers the ACM content and resets the ACM for the next summation.)

3.2.3 DSP Subsystem

The digital samples from the A/D subsystem must be further processed before they can be used as inputs to the microprocessor software. The DSP subsystem consists of several blocks, each of which performs a distinct function as shown in Figure 3.7. Depending on the receiver configuration, appropriate outputs of the DSP subsystem are routed to the software. Notice that in the flexible data format mode, there is a separate DSP block for bit sync and for carrier recovery. In the normal mode, the DAL DSP block is used.

3.2.3.1 Frequency Error Signal Generator

The frequency error signal generator serves as the frequency error detector for the frequency-locked loop (FLL) and its implementation is shown in Figure 3.8. The dump rates for T_1 and T_3 is equal to M x of the symbol rate where M is an integer between 5 and 15. The sampling rate is nominally set at 32 times the symbol rate until it reaches the sampling speed limit. At that point, it reduces to the largest integer multiple of the symbol rate that does not exceed the sampling speed of the A/D converter.

The accumulator serves to filter as well as to slow down the data rate of the FLL error signal to match that of the software. Since the FLL bandwidth will be less than 10 Hz, the ACM can be dumped at a rate less than 1 KHz.

Also shown is the signal to be processed by the software for lock indication. The lock indicator signal is proportional to cos $\Delta\omega T_1$ while the frequency error is proportional to sin $\Delta\omega T_1$ when the FLL has acquired lock. Since $\Delta\omega T_1$ is small compared to 1 radian by design during tracking, a comparison between the two signals can be used to

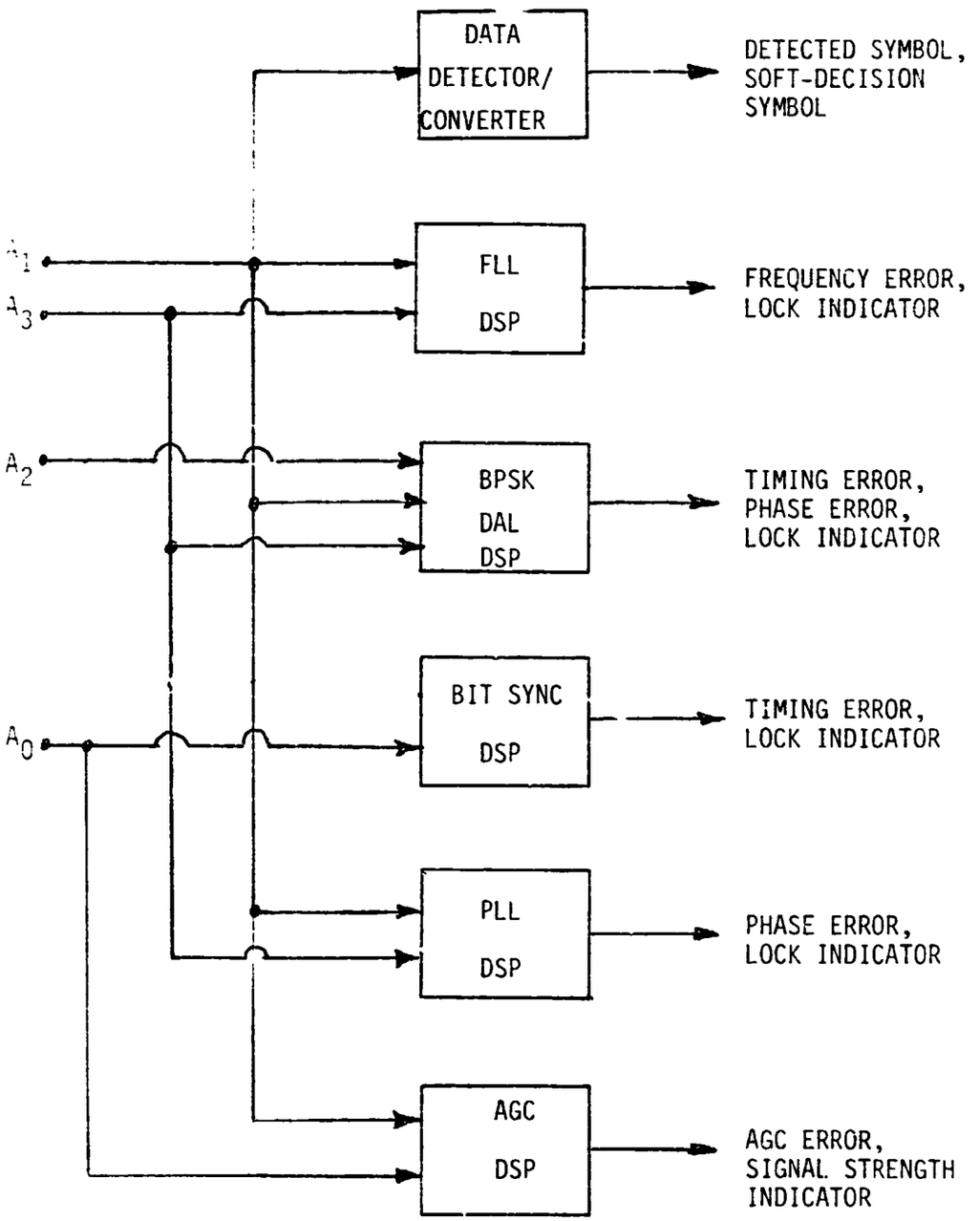
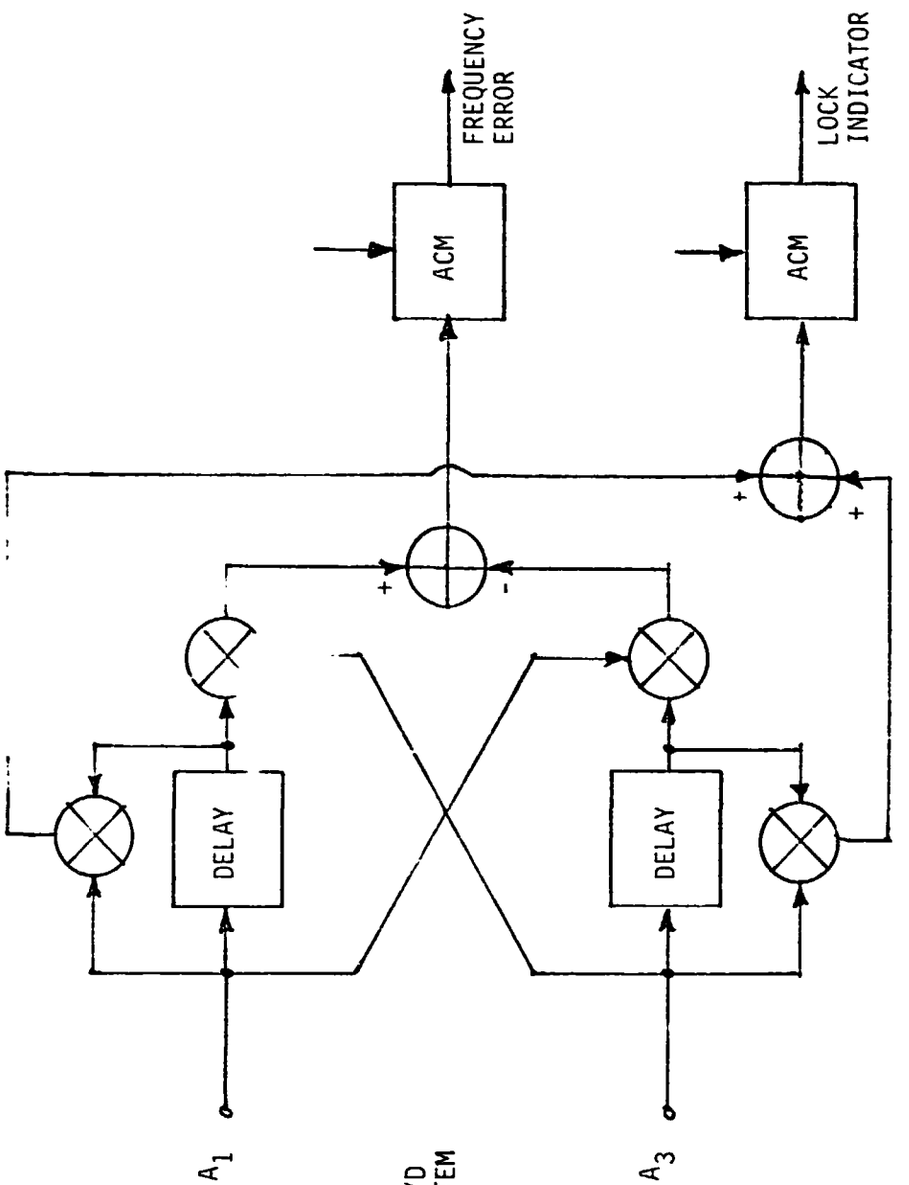


Fig. 3.7. DSP Subsystem.



o ACM DUMP RATE

$T_1 = T_3 = (\text{Symbol Rate}/M)^{-1}$

Fig. 3.8. FLL DSP.

indicate lock.

3.2.3.2 Data-Aided 2-Phase Costas Loop DSP

Figure 3.9 shows the DSP block required for generating the DAL errors. Notice that T_1, T_2 and T_3 are all derived from the bit sync clock. T_1 and T_2 are the same and T_3 is offset from them by half a symbol. The errors are output at a rate of roughly 10 x the loop bandwidths. The lock indicators consists of filtered versions of A_1, A_2, and A_3. When the system is locked, $A_1 \approx 0$, $A_2 \approx |\cos \phi|$, and $A_3 \approx |\sin \phi|$. Bit sync lock can be indicated by comparing A_1 and A_2 while carrier lock can be indicated by comparing A_2 and A_3.

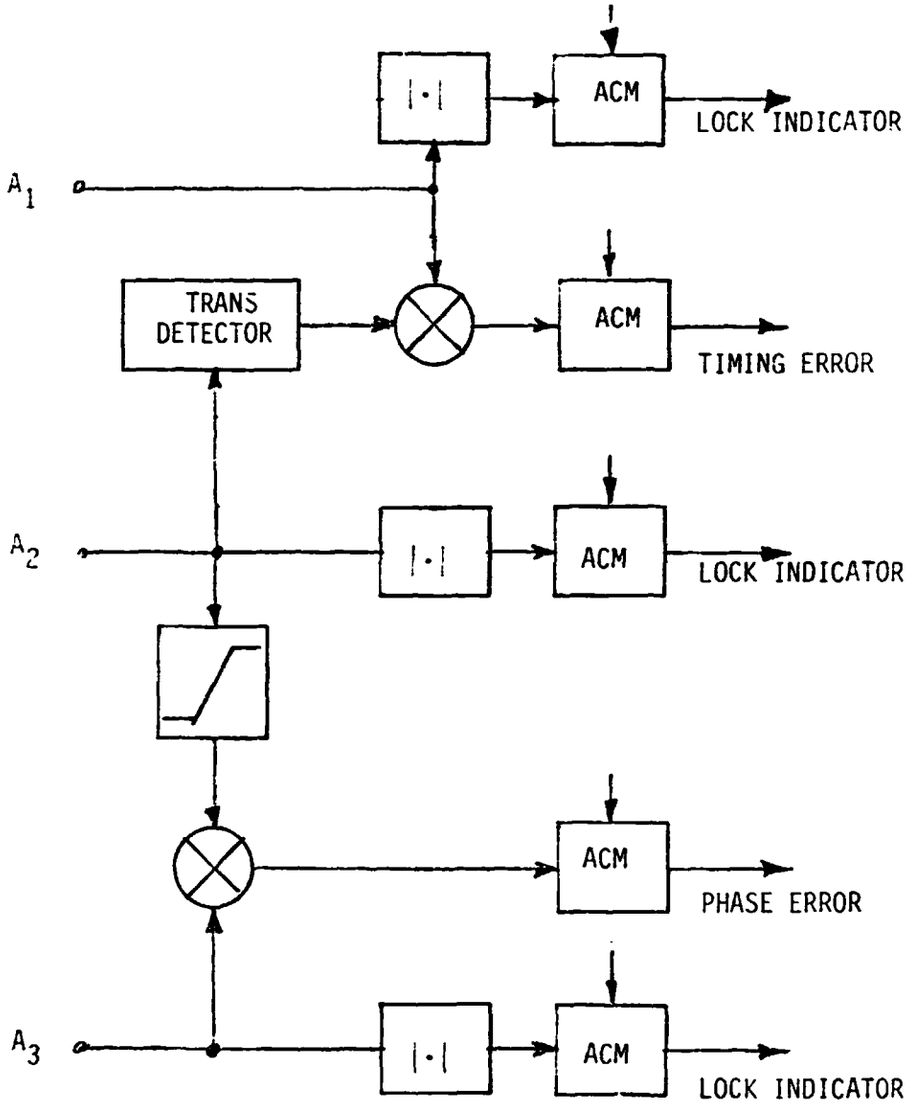
3.2.3.3 Data-Aided 4-Phase Costas Loop DSP

Data-aided 2-phase DSP from the I and Q channel are combined to form the 4-phase DSP as shown in Figure 3.10. For staggered QPSK the I and Q sampling clocks are the same and the dump clocks from the I channel is offset from those of the Q channel by half a symbol. For general unbalanced QPSK (UQPSK) operation, the sampling clocks and dump clocks for the I and Q channels are unrelated.

3.2.3.4 Flexible Data Format Mode PLL DSP

A novel approach is used for the flexible data format mode DSP for generating the phase error as shown in Figure 3.11. The A_0 and B_0 are dumped at 4 x the highest symbol rate allowed by the flexible data format mode. The (A_0,B_0) pair defines the phase angle of the signal vector. The ROM converts this phase angle to a phase error. The rate is slowed down by the output accumulator for the AIRS software.

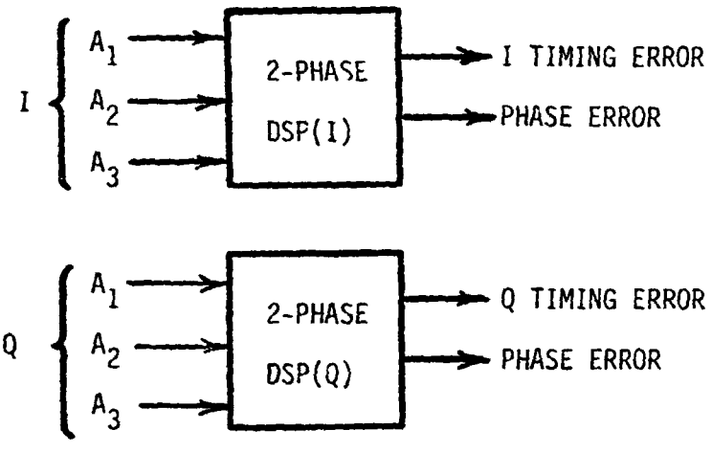
Figure 3.12 shows the required programming for the ROM. The phase angle θ, defined by $x = A_0$ and $y = B_0$ defines an address (x,y) of the



- ACM DUMP RATES
  - $T_3=T_1$ = (SYMBOL RATE)$^{-1}$
  - T_2 OFFSET BY HALF SYMBOL

Fig. 3.9. Data-Aided 2-Phase Costas DSP.

- DATA-AIDED 2-PHASE COSTAS LOOP DSP FROM I AND Q CHANNEL



- SQPSK
  - ACM DUMP RATES

    $T_1 = T_3 = (\text{Symbol Rate})^{-1}$

    T_2 Offset by Half Symbol

    I&Q Dump Clocks Staggered by Half Symbol

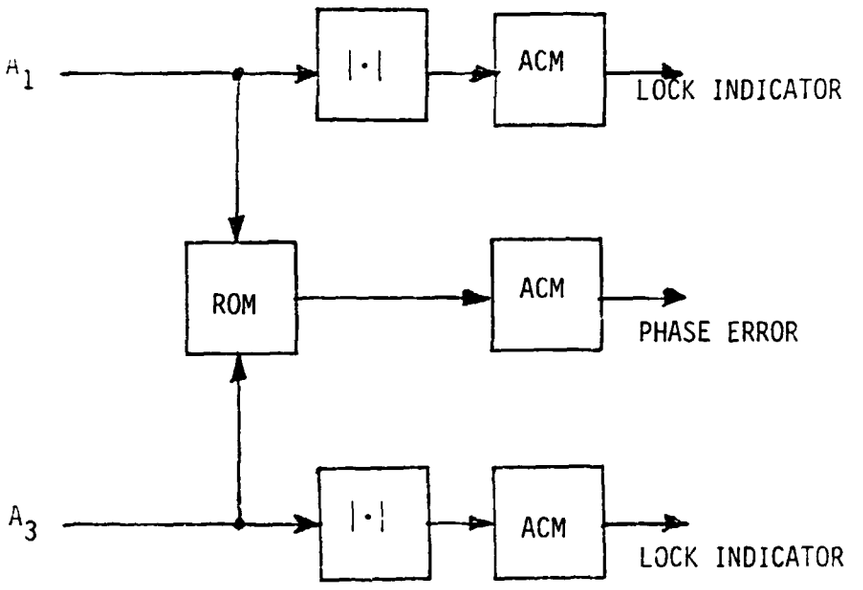
- UQPSK
  - ACM DUMP RATES

    $T_1 = T_3 = (\text{I or Q Symbol Rate})^{-1}$

    T_2 Offset by Half Symbol

    I&Q Dump Clocks Unrelated

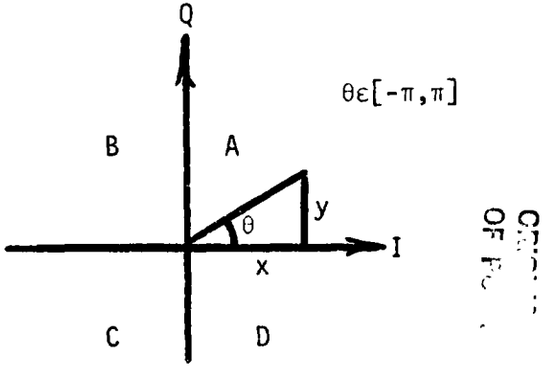
Fig. 3.10. Data-Aided 4-Phase Costas Loop DSP.



- ACM DUMP RATE
  - $T_1 = T_3 = (4 \times \text{Highest Symbol Rate})^{-1}$

Fig. 3.11. Flexible Data Format Mode PLL DSP.

MODULATION	θ IN QUADRANT			
	A	B	C	D
BPSK	θ	θ-π	θ+π	θ
QPSK	θ-π/4	θ-3π/4	θ+3π/4	θ+π/2
UQPSK	θ-Δ	θ-π+Δ	θ+π-Δ	θ+π



$\Delta = \frac{1}{2}\{45° + \tan^{-1}\frac{1}{2}\}$

$= 35.78°$

Figure 3.12. Selection of ROM.

ROM. The content of the ROM at that address is proportional to the entry in the table shown in the figure. For example, for BPSK modulation, the ROM content will be porportional to $\theta-\pi$ if θ is in quadrant B. In general, if the modulation is not specified, then BPSK must be assumed for DG1 and UPQSK must be assumed for UQPSK. It is interesting to note that Δ for UQPSK is selected as a compromise between a 1:1 and a 4:1 power split. When $\Delta = 45°$ this is optimal for balanced QPSK (1:1). When $\Delta = \tan^{-1}(1/2) = 26.6°$, this is optimal for (4:1) unbalanced QPSK. The penalty in not knowing the power split is an increase in jitter due to this 9° average offset.

The signal for lock indicator derived from A_1 is proportional to $|\cos \phi|$ where ϕ is the phase error. The signal derived from A_2 is proportional to $|\sin \phi|$. Lock indication can be obtained by comparing the two signals.

3.2.3.5 Flexible Data Format Mode Bit Sync DSP

In this mode, the bit sync must operate independent of the PLL as reflected in Figure 3.13. Notice that the samples A_1 come directly from the A/D converter. The integrate-and-dump is accomplished in this DSP blocks. The dump clocks are controlled by the bit sync synthesizer as done in a conventional DTTL. The detected data out of the full symbol ACM is also sent to the data detector DSP.

The full sybmol magnitude is much larger than the mid symbol magnitude when the bit sync has acquired. They can be used for lock indication.

3.2.3.6 AGC DSP

The processing block for AGC is shown in Figure 3.14. Every time the A/D sample registers an extreme value (e.g. 1 or 64 for a 6-bit A/D

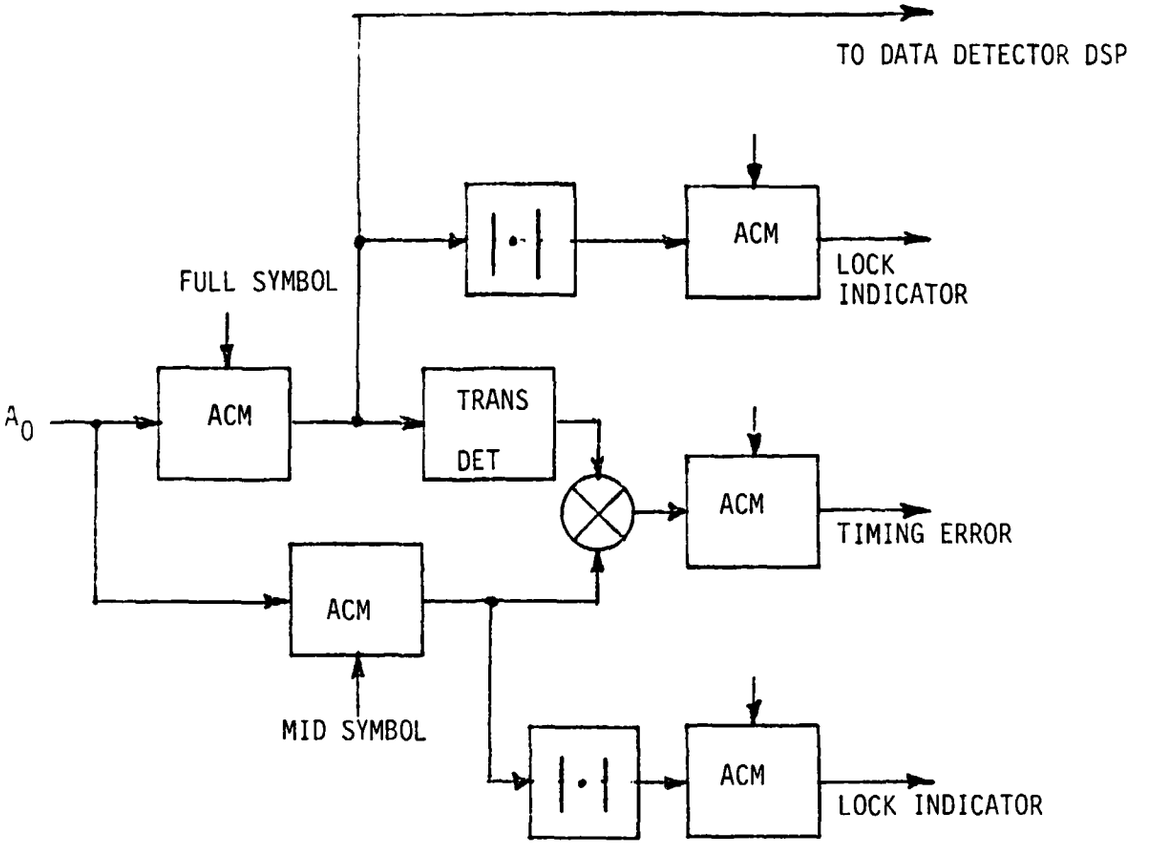


Fig. 3.13. Flexible Data Format Mode Bit Sync DSP.

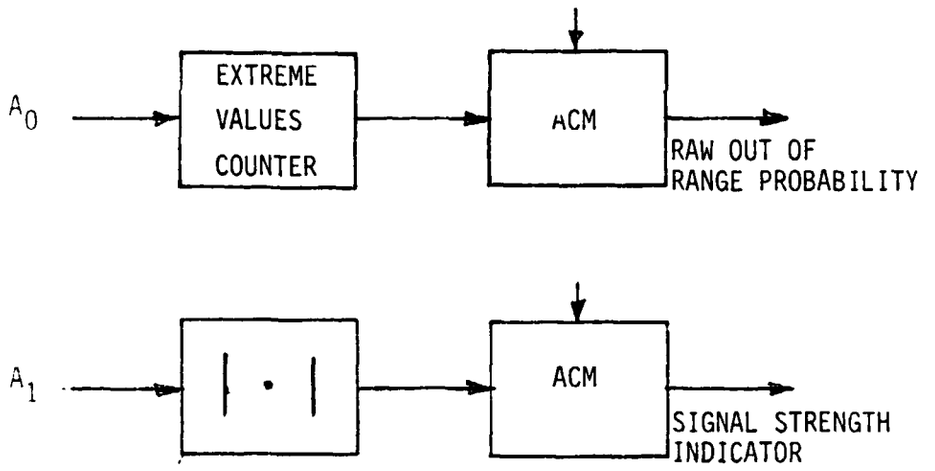


Fig. 3.14. AGC DSP.

converter), the counter outputs a one. This is accumulated for a number of samples so that when the ACM is dumped, its content is proportional to the out-of-range probability. The output rate to the software is approximately 10 x the AGC bandwidth.

The mean of $|A_1|$ is proportional to the signal amplitude and is used in the software that computes signal strength. The technique is explored in Appendix H.

3.2.3.7 Data Detector DSP

The purpose of the data detector DSP shown in Figure 3.15 is to provide soft (6 bit) and hard decision (1 or 0) detected symbols. In case of Manchester-coded symbols, the symbol is converted first to NRZ symbols. This conversion involves an ambiguity. The DSP block is capable of resolving this ambiguity. The technique used and analysis of its performance is documented in Appendix J.

3.3 Software Algorithms

There are four main functions of the microprocessor software. They are:

- Loop Filtering
- Synthesizer Control
- Monitor
- Logic

The first two functions are required to close the carrier loop and the bit sync. The third function is implemented to monitor the status of the receiver. The last function is used to configure the receiver, select the appropriate parameters and control the sequence of various operational procedures such as acquisition or reacquisition.

3.3.1 Loop Filtering

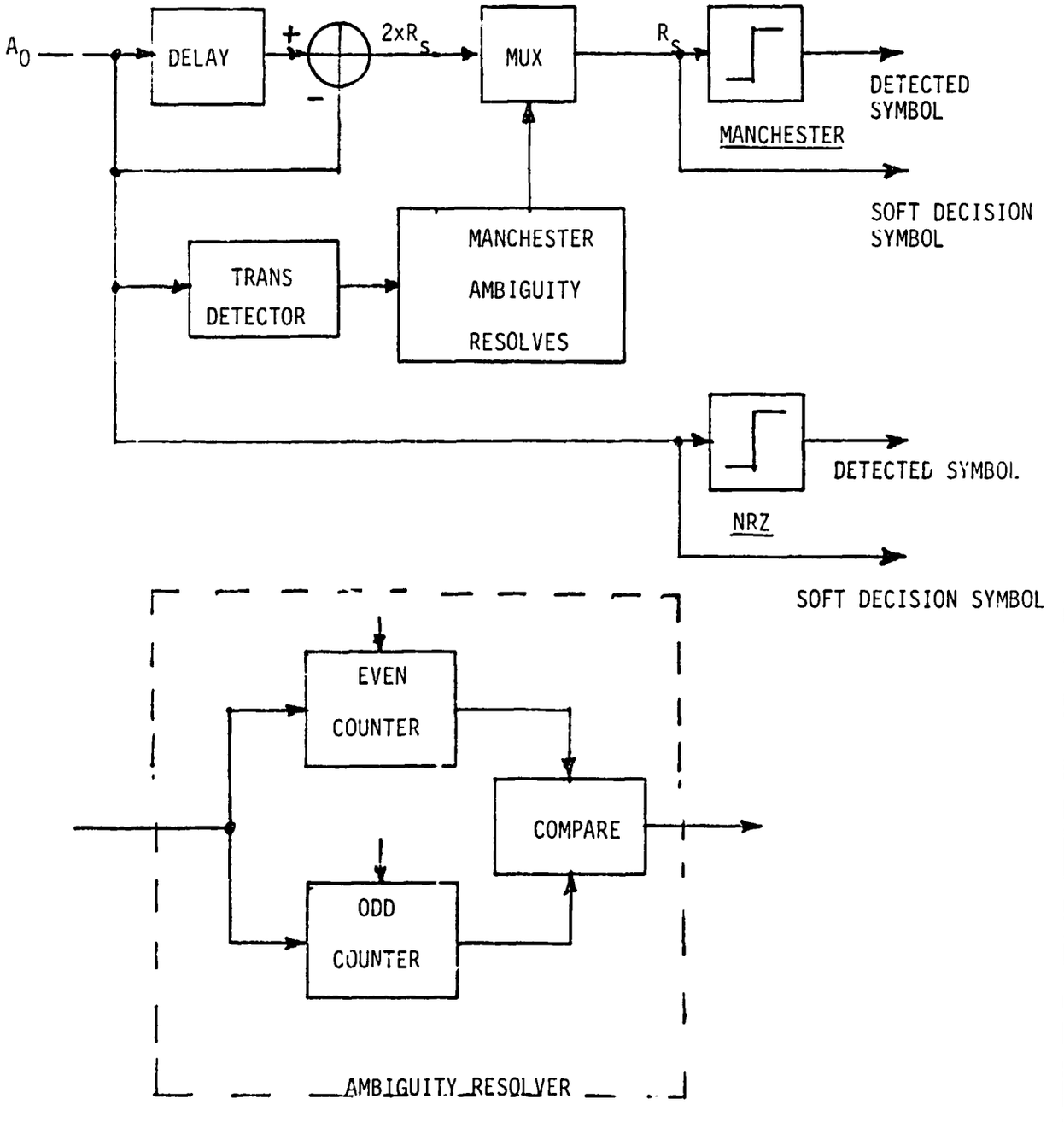


Fig. 3.15. Data Detector DSP.

The loop filtering algorithms takes an input digital sequence $\{x_k\}$ from the DSP subsystem and generates an output sequence by computing

$$y_k = ax_k + by_{k-1} + cy_{k-2}$$

The coefficients a, b, and c define the loop order (up to third order loop) and the loop noise bandwidth. The selection of these coefficients is done during the setup phase based on the given user characteristics. They are modified if a better user characterization can be obtained. e.g., after the receiver has acquired so that there is a better estimate on the signal level. These coefficients are also changed when, for example, the PLL switches to a third-order loop from a second-order loop after the initial acquisition. When the DSP loop error signal samples are available from both I&Q channels, they are weighted by the respective power split and combined before they are processed by the filtering algorithm. This is done for QPSK (DG-2) signals.

3.3.2 Synthesizer Control

The filtered output y_k is used to control the frequency (phase) of the appropriate synthesizers to close the carrier recovery and the bit sync loop. The filtered phase error controls the frequency of the local reference used to coherently demodulate the signal in the A/D subsystem. The filtered bit sync error is used to control the frequency of the bit sync synthesizer from which the T_s, T_1, T_2, and T_3 clocks in the A/D subsystem and other clocks in the DSP subsystem are generated.

3.3.3 Monitoring

Lock detector indicators and the signal strength indicator are lowpass filtered using a recursive difference equation similar to the loop filtering operation described above. The appropriate filtered signals are compared to verify lock (see Appendix K). The signal strength indicator samples are averaged and scaled properly to provide the signal strength estimate. These operations are performed continusouly as long as the AIRS is in operation.

3.3.4 Logic

The logic portion of the AIRS software is probably the most intricate of the software functions. It defines the acquisition, reacquisition, self-test and diagnostics sequence. It sets the receiver configuration (hardware, software and parameter selections) as a function of the set up commands. Currently, it is conceived to use a tree structure for the decision making. However, the AIRS concept is well adapted to be implemented as an expert system using artificial intelligence (AI) techniques.

3.4 Parameter Selection

The selection of the AIRS subsystem parameters such as carrier and bit sync loop bandwidths is based upon a tradeoff between a set of the drivers such as:

- Acquisition time
- Reacquisition time
- Mean slip time
- Phase noise
- Dynamics
- BER

The effects of these drivers have been considered in this report (see

Vol. 1, Appendices F,L). Fortunately, the AIRS has been designed so that most of these drivers can be accomodated in a very simple manner.

Typical carrier loop mechanizations require a compromise between the loop bandwidth for acquisition and tracking since the acquisition performance improves with a larger loop bandwidth while the tracking performance degrades. The AIRS gets around this problem by using a FLL to aid acquisition and a third-order loop to minimize the effect of the dynamics so that the PLL loop bandwidth can be designed based on mean slip time and phase noise alone.

In what follows, we consider various parameters and suggest values to be used for the key subsystems of the AIRS. If the operation of AIRS is compatible with the WDD, the system parameters will be selected on that basis. However, the AIRS simulation will be used as a tool to optimize these selections when the AIRS is ready for a final design.

3.4.1 Frequency-Locked Loop

The PLL is first-order since a first-order loop has the best acquisition performance for this application. In order to acquire the ±4.2 kHz frequency uncertainty within a short time (~ 1 sec) at the lowest acquisition signal level, a multiple bandwidth technique can be used. As an example, the FLL can initialize with a 6 Hz bandwidth, reduces to 3 Hz at the end of 0.2 sec and further reduces to .3 Hz at the end of 0.6 sec.

At higher signal levels, the loop bandwidth can be switched sooner. The actual switching time to achieve optimum performance can be determined by the AIRS simulation.

When the signal level is high (i.e., for symbol rate > 20 ksps), the use of FLL does not provide any advantage since a PLL can be

designed to acquire rapidly and without any possibility of false-locking to data side-bands. The situation is considered in the PLL discussion to follow.

3.4.2 PLL

The PLL is designed to first acquire phase with a second-order loop configuration and then to switch to a third-order loop for tracking. A selection of the bandwidth and loop order are shown in Table 3-1. The symbol rate is the sum of the I and Q channel. Notice that if the symbol rate is higher than 20 Ksps, a 5 kHz bandwidth loop is used to acquire frequency directly, without first aiding with a FLL. Again, the AIRS simulation can be used to optimize these parameters.

The selection of the lower limit of the PLL is based on satisfying the worst case tracking signal to noise level of C/N_0 = 28 dB-Hz. This will give a rms phase jitter of about 11° theoretically. This will also yield a slip time of about 90 minutes (see Appendix L). However, because of phase noise effects, the phase jitter will be slightly higher and the mean slip time will probably be on the order of 1 minute. Ideally, the phase jitter can be reduced by decreasing the loop bandwidth. In practice, oscillator phase noise of the system will begin to dominate at low loop bandwidths and introduce an additional component of the jitter which can make the total higher than the 11°.

In Table 3-1, notice that the loop bandwidth selection is determined by the symbol rate. This, of course, assumes that the signal level is barely meeting the BER requirement. In many cases, the transmitter will be transmitting more power than required for certain bit rates. In this case, the loop bandwidth can be modified to provide better performance. The AIRS will take advantage of the information

Table 3-1. AIRS Carrier Loop Bandwidth.

TRACKING

I&Q Symbol Rate (Ksps)*	Loop Order	Loop Bandwidth
SR < 1	Third	23 Hz
1 < SR < 18.3	Third	(.023) x SR
SR > 18.3	Third	420 Hz

ACQUISITION

I&Q Symbol Rate (Ksps)*	Loop Order	Loop Bandwidth
SR < 3	Second	90 Hz
3 < SR < 20	Second	(.029) x SR
SR > 20	Second	5 kHz

*NRZ only. Half for Manchester-coded symbol

provided by the signal strength estimator for this purpose.

3.4.3 Bit Sync

The bit sync bandwidths can be selected as follows:

Symbol Rate, $1/T_s$	$B_L T_s$ (%)
< 10 Ksps	1.5
10 - 250 Ksps	.78
0.25 - 1 Msps	.39
1 - 6 Msps	.2

4.0 AIRS AND WDD COMPARISON

To a certain degree, the wide dyanmics demodulator (WDD) is a predecessor of AIRS. This is exemplified by its digital implementation and its use of the data-aided loop for carrier and data clock recovery. In this section, the AIRS and WDD are compared in terms of their functional characteristics and implementation techniques. This serves to highlight some of the improvements that are designed into the AIRS. In addition, some unique features of AIRS are given.

4.1 Functional Characteristics Comparison

Figure 4.1 summarizes the differences between the AIRS and the WDD. The WDD is designed to replace the low rate demodulator (LRD) and therefore is basically a low data rate PN/BPSK demodulator. The bit sync and data detection capability is a byproduct of its data-aided carrier recovery loop. The AIRS, on the other hand, is a complete SSA return receive system that replaces the LRD, the medium rate demodulator (MRD), and the low and medium rate bit syncs (LRBS,MRBS). Therefore, it is a dual channel PN/BPSK and UQPSK demodulator and bit sync. It also interfaces directly with the Viterbi decoder (VD) to form an integrated receive system.

The WDD is chartered to provide wide dynamics operation. The technique employed is to use a third-order loop for carrier recovery. The AIRS also employs a third-order loop. In addition, it performs its own Doppler compensation, so that in a typical operational scenario, the Doppler rate uncertainty can be reduced significantly. This further enhances its dynamics handling capability.

The WDD reacquisition is basically the same as its acquisition except that the search range is reduced. The AIRS uses a multistep

WDD	AIRS
• REPLACES LRD • UP TO 300 Kbps	• REPLACES LRD, MRD, LRBS, MRBS • UP TO 3 Mbps
• WIDE DYNAMICS CAPABILITY	• IMPROVED WIDE DYNAMICS CAPABILITY
• REACQUISITION MODE • SINGLE STEP	• IMPROVED REACQUISITION • MULTISTEP
• ACQUISITION PERFORMANCE • 15 SEC AT THRESHOLDS	• IMPROVED ACQUISITION • 1 to 4 SECS
• FIXED LOOP BANDWIDTHS	• VARIABLE LOOP BANDWIDTHS

Figure 4.1. Functional Characteristics Comparison Between AIRS and WDD.

reacquisition strategy to adapt the searching algorithm to the diffusion of uncertainties as a function of the time from loss of lock.

The acquisition performance for the WDD is comparable to (slightly worse than) the LRD. The AIRS uses a parallel searching technique implemented with CCD to speed up the acquisition time at low signal levels.

Finally, the AIRS uses adaptive loop bandwidths to handle received signal level variations.

4.2 Implementation Techniques Comparison

A comparison of implementation techniques used by the AIRS and the WDD is shown in Table 4-1.

4.3 Unique AIRS Features

Features unique to AIRS are shown in Figure 4.2. These features are not found in the WDD.

WDD	AIRS
• PN ACQUISITION	• PN ACQUISITION
• SINGLE-CHANNEL SEARCH • SEQUENTIAL DETECTION REQUIRES AGC CAL • FALSE LOCK PROTECTION WITH VARIABLE THRESHOLD TECHNIQUE DEGRADES THRESHOLD PERFOMANCE	• MULTI-CHANNEL SEARCH • FOR 4-CHANNEL SEARCH ONLY; NOT REQUIRED WITH CCD IMPLEMENTATION • MULTI-CHANNEL OPERATIONS ALLOWS FALSE LOCK VERIFICATION AFTER CODE HIT
• PN TRACKING	• PN TRACKING
• ONLY ONE CHANNEL IS TRACKED • MODIFIED E/L DESPREADER • FIXED BANDWIDTH	• UP TO TWO CHANNELS ARE TRACKED (3 dB IMPROVEMENT) • DOUBLE TAU-DITHERED LOOP • VARIABLE BANDWIDTH
• CARRIER ACQUISITION • ONE CHANNEL • SWEEP ACQUISITION REQUIRES FALSE LOCK REJECTION ALGORITHM THAT CAN BE TIME CONSUMING	• CARRIER ACQUISITION • BOTH CHANNELS • FLL IMPLEMENTATION CANNOT FALSE LOCK
• CARRIER TRACKING	• CARRIER TRACKING
• ONE CHANNEL • SECOND/THIRD ORDER LOOP • FIXED BANDWIDTH	• BOTH CHANNELS • SECOND/THIRD ORDER LOOP AND DOPPLER COMPENSATION • VARIABLE BANDWIDTH
• IF SAMPLING AT 5 MHz	• BASEBAND SAMPLING
• REACQUISITION (ONE STEP)	• REACQUISITION (MULTISTEP)
• FREEZES PN LOOP AND PERFORMS CARRIER REACQ	• DISTINGUISHES BETWEEN PN, CARRIER AND BIT SYNC LOSS OF LOCK COMBINATIONS • WAIT, MINISEARCH & COLD START

Table 4.1. Implementation Comparison of WDD and AIRS.

- INTEGRATED DEMOD/BIT SYNC/DECODER OPERATION
- AUTONOMOUS STAND ALONE OPERATION
- PROVISION FOR RFI MITIGATION
- DOPPLER COMPENSATION
- AUTONOMOUS (NORMAL)/FLEXIBLE DATA/TEST MODE
- I/Q CHANNEL AMBIGUITY RESOLUTION
- VARIABLE LOOP BANDWIDTHS ALLOWS REAL TIME PHASE NOISE/ THERMAL NOISE TRADEOFFS

Figure 4.2. Unique AIRS Features.

5.0 AIRS ANALYTICAL/SIMULATION SOFTWARE

The primary purpose of the AIRS simulation software is to provide a computer emulation of the AIRS hardware and the AIRS software algorithms. The simulation is a tool for checking out and verifying the soundness of the technique used to implement the AIRS, and for exposing bugs and problems in the early stage of the design. The software tool is also used to evaluate and predict the performance of various AIRS subsystems. Finally, the software tool can be used to select the various system parameters whenever a tradeoff exists.

Since the algorithms developed in the software simulation can be transferred to the AIRS microprocessor software with minor modifications (perhaps to accomodate the microprocessor computation cycles), a strict Monte Carlo technique is adopted whenever possible. In the cases where the Monte Carlo technique is impractical and/or overly time consuming, the software is supplemented with analysis.

Figure 5.1 shows a typical application of the AIRS software. In this case, the simulation is used to optimize a design parameter.

5.1 AIRS Simulation Software Structure

The AIRS simulation software package is designed to evaluate the performance of the AIRS in terms of acquisition, tracking, BER and reacquisition. The software is organized into the following modules:

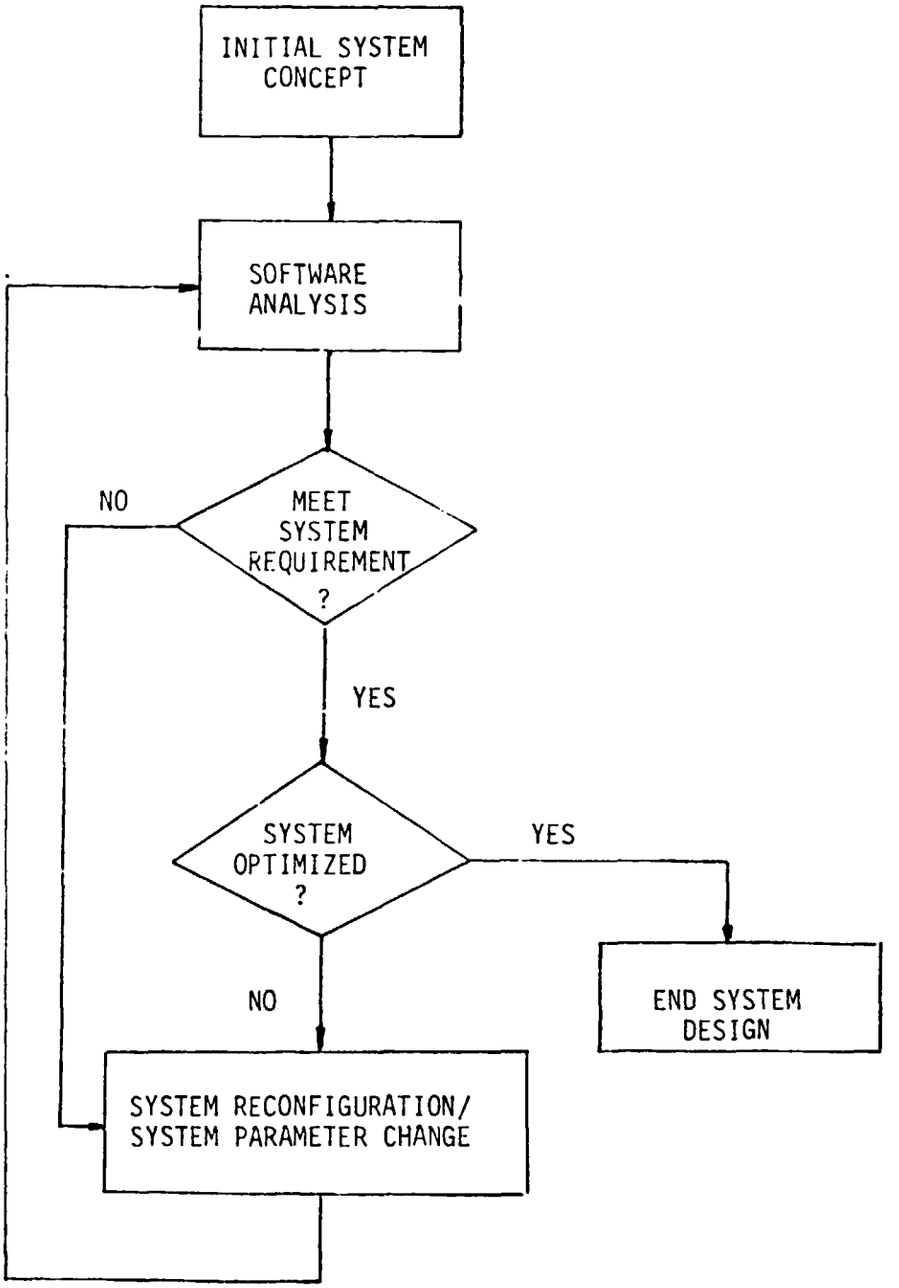
a. Interface module

b. Configuration module

c. Performance module

The interface module is used to translate the output of a CLASS execution module, whose purpose is to define the link conditions and user characteristics such as data group and modes, into a form usable by

Figure 5.1. DESIGN PROCEDURE BY USING SOFTWARE ANALYSIS TOOL



the succeeding configuration module. The configuration module is used to define the setup of the AIRS as a function of the link and user data characteristics, under the criterions established by the selected mode of receiver operation. Finally, the performance module computes and displays the various desired performance measures.

5.1.1 Interface Module

The pertinent output from the CLASS module defines the data characteristics for the I and Q components as well as the received effective C/N_0. The interface module translates the CLASS output into an explicit description of the I and Q channels. They describe:

a. Data format (NRZ/bi-phase)

b. Data rate

c. Code rate

d. PN spreading

e. BPSK/QPSK

f. Power ratio

g. Effective C/N_0

A summary of the I and Q channel characteristics are displayed as part of the interface module output.

5.1.2 Configuration Module

The configuration module takes the output of the interface module, and based on the selected mode of receiver operation, configure the AIRS signal porcessing architecture. The output of the module is a summary of the AIRS configuration for:

a. PN acquisition

b. PN tracking

c. Frequency acquisition

d. Carrier tracking

e. Bit sync

as well as the associated subsystem parameters.

5.1.3 Performance Module

The performance module is a collection of software packages that are used to predict ARIS subsystem performance. The module uses a combination of analysis and Monte Carlo simulation as shown in Figure 5.2 The performance packages that are analytical in nature are:

a. PN acquisition package

b. PN tracking package

c. BER package

d. Decoder package

the performance packages that are Monte Carlo in nature are:

a. Frequency acquisition package

b. Carrier tracking package

c. Bit sync tracking package

d. Carrier/bit sync tracking package

These packages can be used to support four main executive programs that determine AIRS sytem acquisition, reacquisition, tracking, and BER performance. The interconnections between the modules and the main programs are shown in Figure 5.3. The packages all employ a user-friendly interactive approach to help the user define the pertinent subsystem parameters.

5.1.3.1 Analytical Packages

5.1.3.1.1 PN Acquisition Package

The PN acquisition package determines both the mean time to acquire and the time to acquire with a probability for three PN acauisition

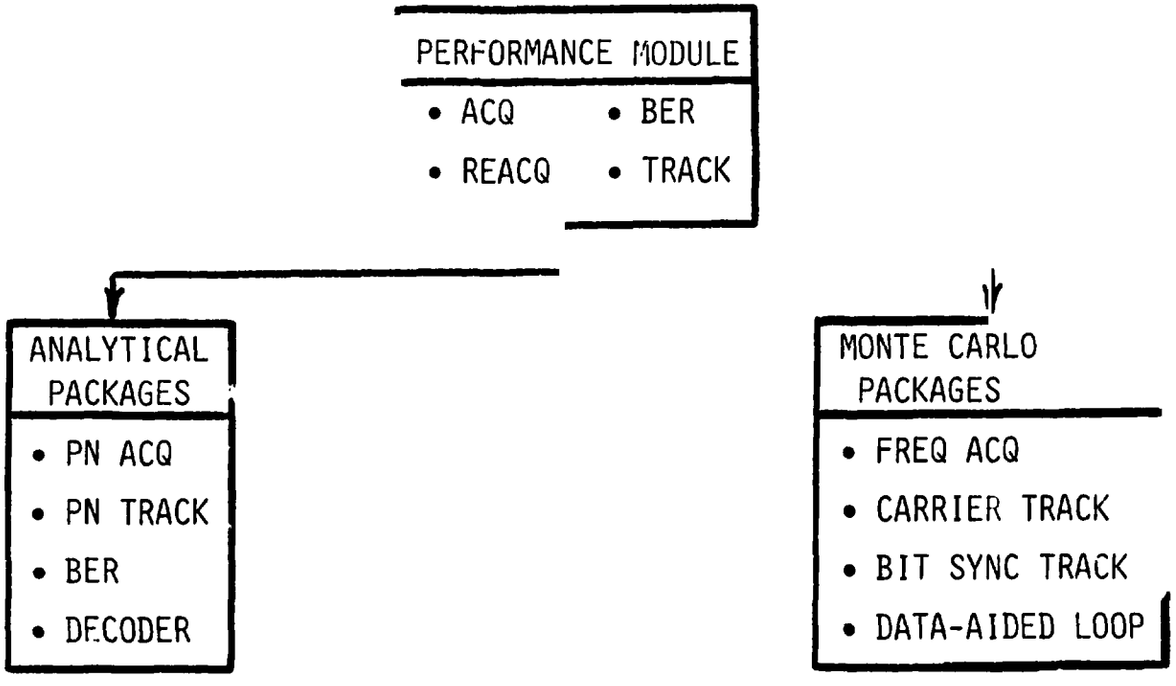


Figure 5.2. Performance Module.

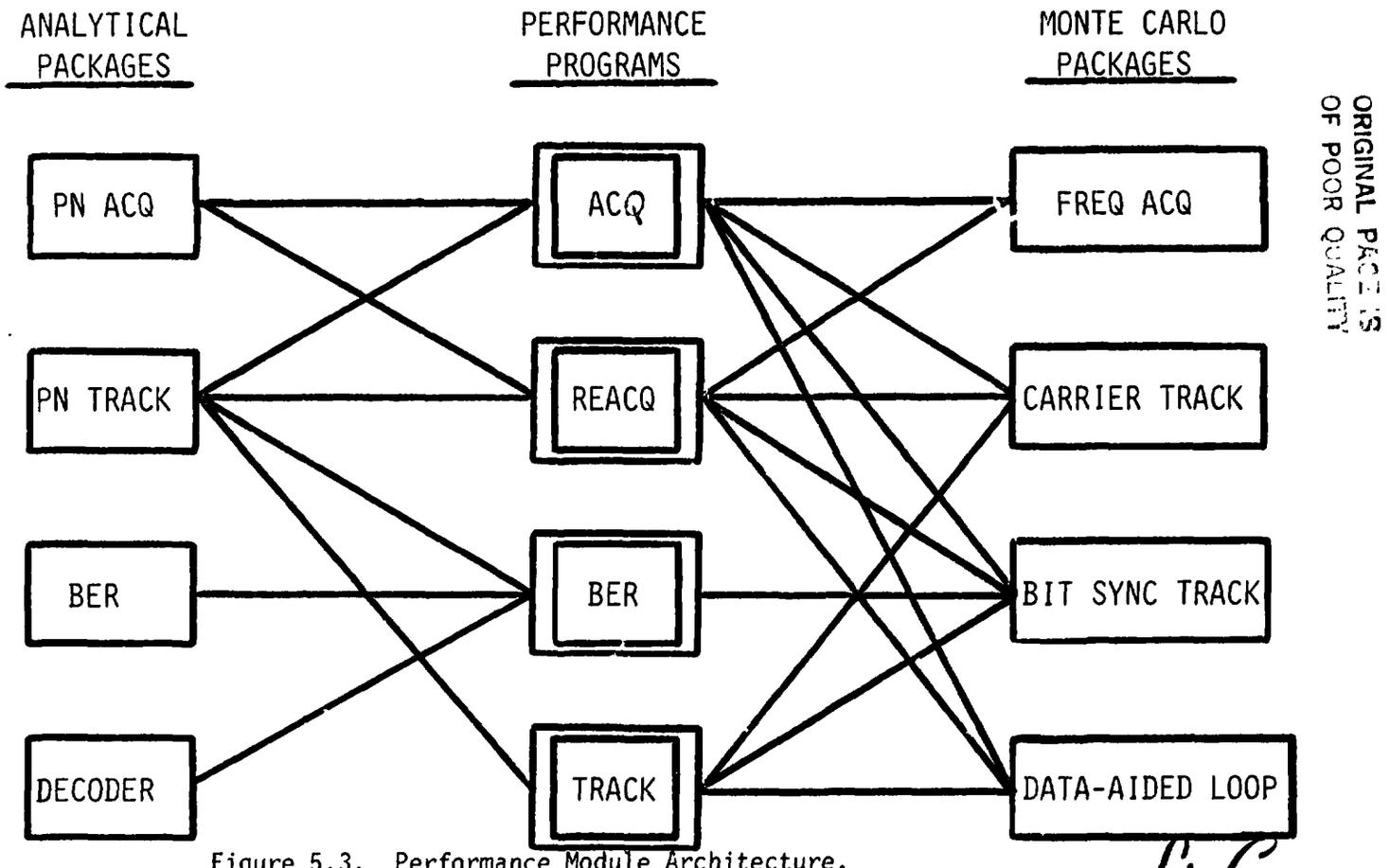


Figure 5.3. Performance Module Architecture.

schemes. Two schemes are based on using CCD PNMFs and one scheme is based on multi-channel sequential search.

5.1.3.1.2 PN Tracking Package

This package determines the initial pull-in, tracking, and slip performance of the configured subsystem. The output performance measures are: pull-in time, rms PN chip jitter, and mean time to lose lock.

5.1.3.1.3 BER Package

This package determines the bit error rate (BER) for uncoded data or the symbol error rate (SER) for coded data. For coded data the BER package also computes the probability mass at each quantization level. There are two portions of the package. The first one deals with the transient BER, i.e., during acquisition and high dynamics operation. For the transient BER computation, the effects of the mean carrier phase error are incorporated. The second portion deals with steady state operation. For the steady state BER computation, the effects of phase jitter and timing jitter are considered.

5.1.3.1.4 Decoder Package

This package computes the decoded BER for convolutionally encoded data. It is based on computing the computational cutoff rate of the quantized symbol.

5.1.3.2 Monte Carlo Packages

The main purpose of the Monte Carlo packages is to duplicate the AIRS hardware/software structure, so that it can be checked for potential problems. As such, the Monte Carlo packages should not be used for extensive performance predictions as the computational time will be prohibitively long.

5.1.3.2.1 Frequency Acquisition Package

This package duplicates the AIRS algorithms. The received signal is sampled and processed in the manner of a frequency-locked loop. The algorithm stops once the incoming signal carrier frequency can be matched to within 25 Hz. This is done by implementing a lock detector. The output of this package is the mean time to acquire frequency lock.

5.1.3.2.2 Carrier Tracking Package

This package is used in the Flexible Data Format mode in which the carrier loop and the bit sync loop must be decoupled. The output of this package is the mean time to acquire phase lock, the mean phase offset (which will be a function of time during transient), the rms phase jitter. The mean time to lose lock determination is partly analysis and partly simulation.

5.1.3.2.3 Bit Sync Tracking Package

This package is used in the Flexible Data Format mode in which the carrier loop and bit sync loop must be decoupled. The output of this package is the mean time to acquire timing, the mean timing error, the rms time jitter, and the mean time to lose lock. The mean time to lose lock determination is partly analysis and partly simulation.

5.1.3.2.4 Carrier/Bit Sync Tracking Package

This package is used during normal operation in which a data aided tracking loop configuration is used. In this case, the bit sync and the carrier loop acquires simultaneously. The output is the mean phase and lock acquisition time, the mean phase and clock error, the rms phase and clock error, and the mean time to lose carrier and bit sy[illegible] lock. The mean time to lose lock determination is a combination o[illegible]'ysis and

Monte Carlo simulation.

5.2 An Application Example

Figuare 5.4 shows an application example of using the AIRS software to determine system acquisition time. Notice that the analytical portion of the software computes the time spent during code search, code loop acquisition, and Viterbi decoder node sync. The time spent during frequency, phase and bit sync acquisition are determined via Monte Carlo simulation.

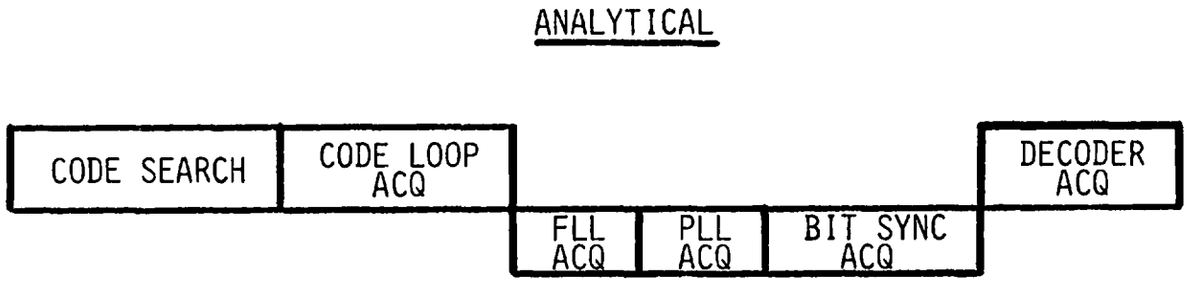


Figure 5.4. AIRS Acquisition Time.

APPENDIX A

RAPID PN ACQUISITION SCHEMES FOR AIRS: TECHNIQUE, ANALYSIS AND PERFORMANCE SIMULATION

This appendix is a revised and updated version of an earlier technical report, TR-0484-8211, prepared by Y. T. Su and C. M. Chie under this contract.

LinCom

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LinCom

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1. Introduction and Summary

1.1 Introduction and Objective

An Autonomous Integrated Receive System (AIRS) has been proposed by LinCom to improve the current Tracking and Data Relay Satellite System (TDRSS), and to use as a receiving system for the future Tracking and Data Acquisition System (TDAS). The object of this study is to examine in depth three possible code acquisition subsystems for the AIRS, namely,

- serial search using charged-coupled device (CCD) pseudonoise matched filter (PNMF)
- parallel search using PNMF
- four-channel parallel search using sequential detection,

and to develope a software analysis tool for predicting the performances of these systems.

The software package is to have many useful features, for example, it can

- generate the operation characteristics for different detector configurations, parameterized by SNR and integration time
- produce sensitivity curves (or data), e.g., detection (false alarm) probability vs. threshold, noise power, SNR, etc.
- evaluate the system performance (with given design parameters) under different SNR environments
- optimize system parameters.

1.2 Organization of the Report

This report is organized as follows.

Section 2 defines the general PN acquisition problem and classifies search algorithms. Section 3 describes and motivates the three schemes to be investigated. Section 4 identifies assumptions needed for

analysis and summarizes performances of various systems. Conclusions and some suggestions for further studies are contained in Section 4. Appendices A to G detail the performance analysis and software applications.

An executive summary is contained below in section 1.3.

1.3 Executive Summary of Progress and Results

We have developed analytical models for the three acquisition subsystems mentioned in Section 1.1. Complete performance measures, e.g., mean acquisition time, time for 90% acquisition, and a corresponding software package (as one part of the AIRS demonstration program) which contains the features listed in Section 1.1 are obtained. In the course of analyzing system performance, we have developed analytical expressions, both exact and approximation. For detection and false alarm probabilities of each detector structure involved. Efficient numerical algorithms for computations are also found. To assess, according to merit, the three candidate systems, numerical optimizations have been performed. As expected, the CCD receivers outperform the sequential detection method. For the two receivers using CCD PNMF, the serial search is superior to the parallel search though this advantage dwindles as the reference C/N_0 increases.

The AIRS' current acquisition requirements are summarized in Table 1-1. This study has found that these requirements can all be met by both CCD systems without difficulty, as exemplified in Table 1-2. This table is evaluated with the following parameters:

Code Epoch Timing Uncertainty	±1900 chips
Reference C/N_0 for One Channel	36.5 dB-Hz
Number of Doppler Bins	3

Table 1-1. Acquisition Time vs. C/N_0 and Mode Requirements for the AIRS

ACQUISITION TIMES FOR 90% ACQUISITION

C/N_0 dB-Hz	5 SECONDS	15 SECONDS	45 SECONDS
39.5	N/A	DG-1 Modes 1, 2A, 3 DG-2 Modes 2A, 3	DG-1 Mode 2B DG-2 Mode 2B
49.5	DG-1 Modes 1, 2A, 3	DG-1 Mode 2B	N/A

Table 1-2. Acquisition Performance for Algorithms Using CCD PNMF

Algorithm	Parallel Search	Serial Search
Acquisition Time (sec.)	3.95	3.89
Acquisition Probability	0.914	0.925
Number of CCD PNMF's Per Channel	8	8
Length of a PNMF (cells)	255	255
Required Memory Size (bits) for Noncoherent Integration	2^{10} (~ 8K)	2^{10} (~ 8K)

Sampling Loss	2.5 dB
Doppler Loss	0.4 dB
Data Transition Loss	0.2 dB
PN Code Rate	3M chips/sec
IF Bandwidth	6 MHz
CCD Transport (Sampling) Clock Rate	6 MHz

The inclusion of the 4-channel sequential detection method serves to illustrate the superiority of the CCD receivers. For example, with the same set of parameters shown above, the minimum mean acquisition times (in sec) for the CCD receivers are 2.47 (serial) and 3.95 (parallel) respectively while that for 4-channel sequential detection is at least 6.65. Noted that the minimum mean acquisition times for the CCD receivers are different from the acquisition times in Table 1-2. The reason is that the data obtained in Table 1-2 is based upon the criterion of minimizing the time required for 90% acquisition.

The above numerical results are shown in part to highlight the versatility of the software analysis tool developed by this study. Not only the goals set up in Sec. 1.1 are accomplished but several more functions are added. Among these additions are the capabilities to:

- Obtain the optimal system parameters under the criterion of either minimizing the mean acquisition time or the time for 90% acquisition.
- Estimate the correlation loss due to pre-despreading filtering.
- Help to decide between performance and complexity (i.e., number of channels, length of CCD PNMF's, bin width, and bit numbers).

Details can be found in Appendix G.

2. Background

The PN acquisition problem can be defined as to find a pair of Doppler and code phase estimate $(\hat{\omega}_d, \hat{\tau})$ for the incoming waveform:

$$r(t) = \sqrt{2S}\, d(t)\, P_n(t-\tau) \cos[(\omega_c+\omega_d)t+\phi] + n(t) \qquad (2\text{-}1)$$

such that

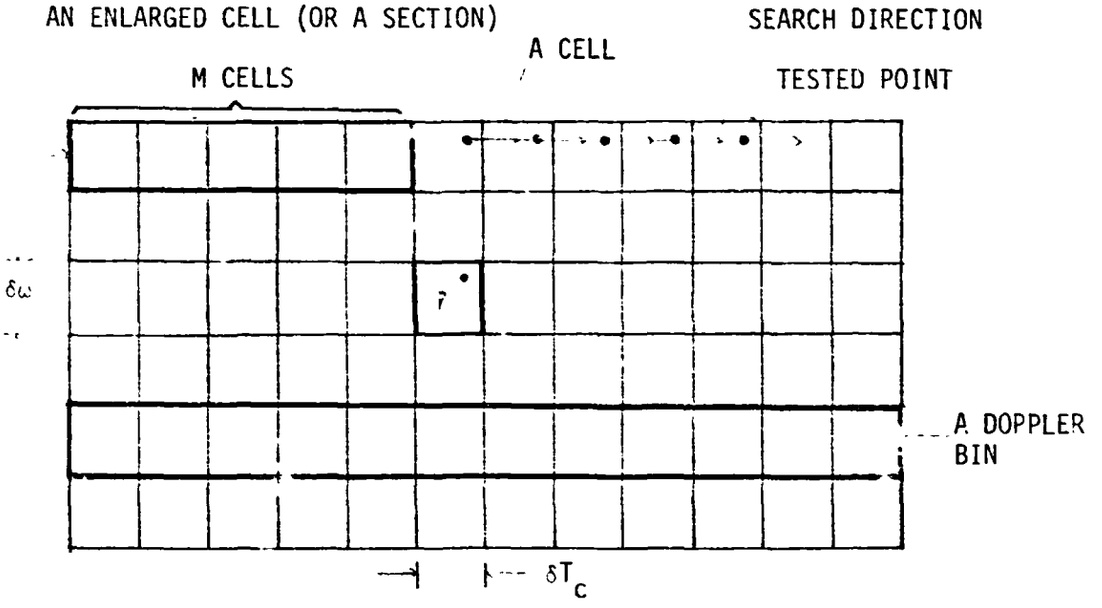
$$|\omega_d - \hat{\omega}_d| < \delta\omega, \qquad (2\text{-}2a)$$

$$\text{and } |\tau - \hat{\tau}| < \delta T_c. \qquad (2\text{-}2b)$$

In the above expression, $P_n(t-\tau)$ is the received PN code with rate T_c^{-1}, delayed by τ with respect to an arbitrary time reference, $d(t)$ is the data modulation, $n(t)$ is additive white Gaussian noise with a one-sided power spectral density N_0. S, ω_c and ϕ are the carrier's power, frequency and phase respectively and ω_d is the Doppler frequency. The requirement of simultaneous Doppler estimate $\hat{\omega}_d$ is due to the fact that the Doppler offset must be small enough not to incur too much signal power degradation when correlation between received signal and local estimate is performed. Hence, the choice of $\delta\omega$ depends not only on the pull-in region of the carrier-phase tracking loop but on the Doppler loss tolerable in obtaining code phase estimate $\hat{\tau}$. The parameter δT_c, on the other hand, is typically chosen as T_c or a fraction of T_c, which is within the pull-in capacity of the code-tracking loop.

Consider the rectangular time-frequency uncertainty region shown in Fig. 2-1, where a small $\delta\omega \times \delta T_c$ rectangular is defined as a cell. The PN acquisition problem is now equivalent to find out which cell satisfies the condition (2-2). Here, there may be more than one such a cell because usually we test only one specific point within a cell; see

Fig. 2-1. A Time-Frequency Uncertainty Region.



also Fig. 2-1. Thus, acquisition algorithms are in fact searching strategies and can be classified into three categories: serial, parallel or compound search. This report discusses two algorithms which fall into the third category and will be called as SPS (serial-parallel-serial) and SSP (serial-serial-parallel) algorithms according to the way signal is processed. The compound nature of these algorithms, as we shall see, is due to the usage of the so-called CCD PN match filters (PNMF) [1] and the low chip-signal energy to noise power density ratio (E_c/N_0) environments. Algorithm similar to SPS has been discussed [2], though no rigorous definition and analysis are given. Pure serial or parallel search algorithms using either digital match filter [3] or SAW device [4] were also investigated recently.

3. Acquisition Algorithms Using CCD PNMF

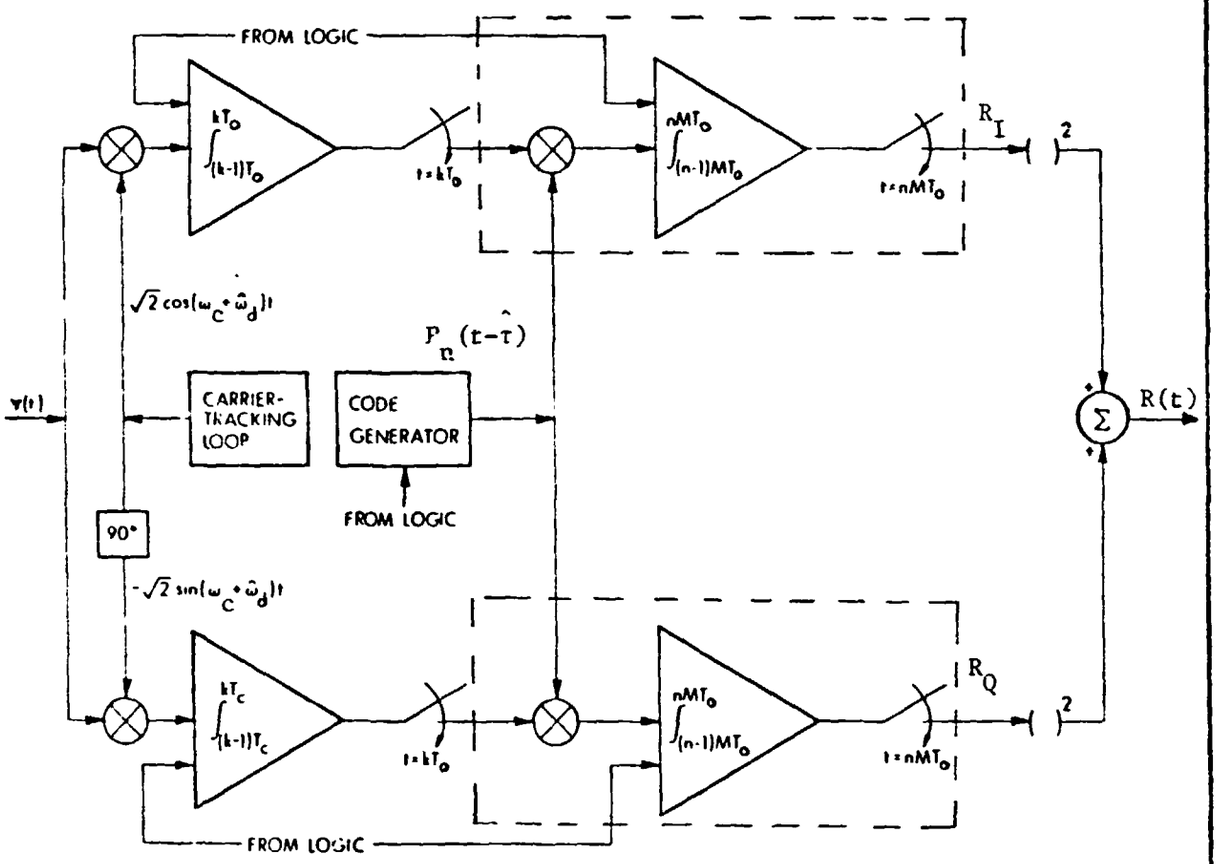
3.1 An Analytical Model for CCD Detector

An equivalent CCD detector is shown in Fig. 3-1. The received waveform, after frequency deconversion (mixing), is integrated for a fraction of the chip time and sampled at a rate $R_s=1/\delta T_c$ (integrate-and-dump) in both I and Q arms. The sampled baseband I & Q signals are then fed into an I/Q pair of CCD PNMF's (correlation), squared in each arm and finally added to yield a test statistic $R(nT_0)$ at time $t=nT_0$, where $T_0 \triangleq \delta T_c$.

Denote the sampled signals at the input of I and Q channel PNMF's by $\gamma_I(\kappa T_0)$ and $\gamma_Q(\kappa T_0)$ respectively. Then the outputs of I/Q PNMF's are

$$R_g(nT_0) = \sum_{\kappa=1}^{M} P_n(\kappa T_0)\, \gamma_g[(\kappa+n-M)T_0], \qquad M>n>M \qquad (3\text{-}1)$$

where g denotes I or Q (channel).



: CCD PNMF

$T_0 \triangleq \delta T_c$

Fig. 3-1. An Equivalent CCD I-Q Detector.

Obviously, with the capability of retaining thus reusing the received information, $\gamma(\kappa T_0)$'s, the CCD detector can produce the test statistics, $R(nT_0)$'s, at a rate M times faster than conventional analog I-Q detector. However, this improvement factor M can not be made arbitrary large due mainly to the presence of the data modulation d(t). On the other hand, in small E_c/N_0 situations, long correlation period is necessary to get a robust statistic. This dilemma can be solved by resorting to noncoherent integrations (NI). NI, or post-detection integration, is a technique borrowed from pulse radar detection theory [6] referring to the case in which phase coherence between consecutive pulses is not maintained. In our case, NI is equivalent to the following summation operation:

$$\sum_{i=1}^{N_I} R_i \tag{3-2}$$

where

$$R_i = R_I^2(i) + R_Q^2(i) \tag{3-3}$$

$$R_g(i) = \sum_{\kappa=1}^{M} P_n[(i-1)MT_0 + \kappa T_0]\, \gamma_g[(i-1)uT_0 + \kappa T_0]$$

$$\doteq \int_{(i-1)MT_0}^{iMT_0} P_n(t')\gamma_g(t' + (i-1)\Delta T_0)dt' \tag{3-4}$$

u is a constant larger than or equal to M and $\Delta T_0 = (u-M)T_0$.

3.2 Algorithm Using CCD PNMF

We are now in a position to define the SPS and SSP algorithms. Basically, they are all two-stage tests. The difference lies in the first stage test only. The second stage test, or the verification mode is used to reduce the false alarm rate so as to avoid a costly false

code tracking attempt (usually modeled as a penalty time [7]). A single-dwell test (SDT) will be used as the second stage test for both algorithms. As we shall see, the acquisition time is insensitive to that consumed by a properly designed SDT for the second stage.

(A) The SSP algorithm:

(A.0) Load the PNMF with M samples of $\gamma_g(t)$ (initialization).

(A.1) Fix a M-cell segment of the PN code for local reference.

(A.2) Let the incoming waveform samples run through the PNMF for MT_0 seconds and collect serially M test statistics R_{ij}, $(i-1)M + 1 \leq j \leq iM$, corresponding to a section of M cells (Fig. 2-1) in the uncertainty range. These numbers are stored in a first in first out (FIFO) register for further (noncoherent) addition; See Fig. 3.2.

(A.3) Repeat (A.1) & (A.2) for N_I mutually disjoint segments of the local PN code. The test statistics corresponding to the same code phase are added (i.e. NI) and at the end of the N_I^{th} iteration, only the largest* and its phase are kept in two registers.

(A.4) Repeat the process (A.1)-(A.3) for all (disjoint) sections (or bins) in the uncertainty range.

(A.5) The code phase with the largest test statistic is to be tested by the second stage test and will be used as our estimate $\hat{\tau}$ (see eq. (1-2)) for further code phase tracking if passes; otherwise, go back to (A.0) and start all over.

The SSP algorithm is based on the maximum likelihood estimate principle

*Here, the largest is chosen from the M cells in the section under consideration and the previous largest one.

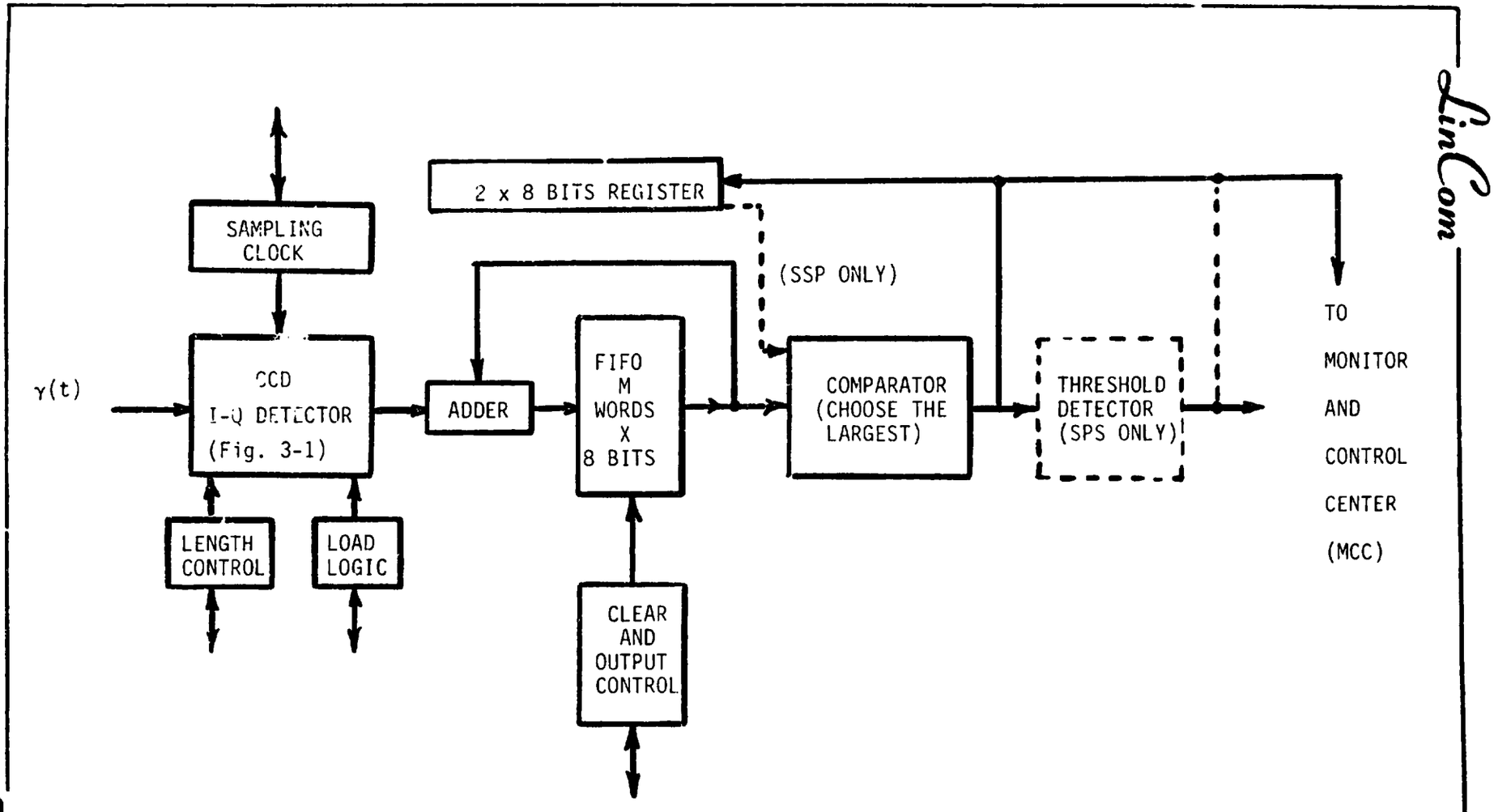


Fig. 3-2. Rapid PN Acquisition Systems Using CCD PNMF; ↕ Denotes Command From MCC.

to use the code phase which yields the highest correlation value. Such an algorithm is optimal in the sense of minimizing the error probability [8]. Nevertheless, our criterion is to minimize the mean acquisition instead and hence the cost is time not error rate though they are related. The second algorithm, taking the above fact into consideration, is essentially the same as the well-known serial search algorithms [7] with enlarged cells, where an enlarged cell is what we call a section (bin) in (A.2) above, i.e., M consecutive cells; see also Fig. 2-1. Therefore,

(B) The SPS algorithm (Fig. 3.2):

(B.0) = (A.0)

(B.1) = (A.1)

(B.2) = (A.2)

(B.3) Repeat (B.1) and (B.2) for N_I iterations. If the largest test statistic is larger than a threshold then go to the 2nd stage test, otherwise go to the next section and repeat this process (B.1) to (B.3).

The purpose of this algorithm is to shorten the time needed to go to the second stage if the resulting statistics of a certain section indicate strongly that a good estimate is obtained.

3.3 Four-Channel Parallel Search Using Sequential Detection

This approach divides the uncertainty range into four equal length regions. Each region is searched by one channel. Once coarse synchronization is declared in one of the four channels the other three sequential detectors will stop searching and the system then enters the code tracking mode. Theoretically, the acquisition time will be reduced to only a quarter of that of a single channel case, assuming very low

false alarm rate, since the H_1-cell exists in only one region. Thus it suffices to analyze the one-channel sequential detection. An analytical model of the sequential detection used for PN acquisition is depicted in Fig. 3.3. The product of the local code and the incoming waveform is fitered by a bandpass filter which is wide enough to accomodate the data modulation and the Doppler uncertainty. A sequence of independent and identical distributed (i.i.d.) observations are then obtained by sampling the envelope detector output at a rate = $1/2B_{IF}$ where B_{IF} is the bandwidth of the BPF. These observations, R_i, are further modified by first multiplied by a and then subtracted by b, where a,b are constants depending on E_c/N_0. The cumulated sum of modified observations

$$X_i \triangleq aR_i - b \ ,$$

i.e.,

$$S_k = \sum_{i=1}^{K} X_i \ ,$$

are fed into the decision logic. There are two decision logics that can be simply implemented. The first one, denoted by $S_1(A,B)$, uses the decision rule:

	$> A$	stop sampling and decide that H_1 is true (D_1)
S_k	$\varepsilon(A,B)$	continue by taking another sample (D)
	$< B$	stop sampling and decide that H_0 is true (D_0)

while the second one, denoted by $S_2(B,N_t)$, uses the following rule:

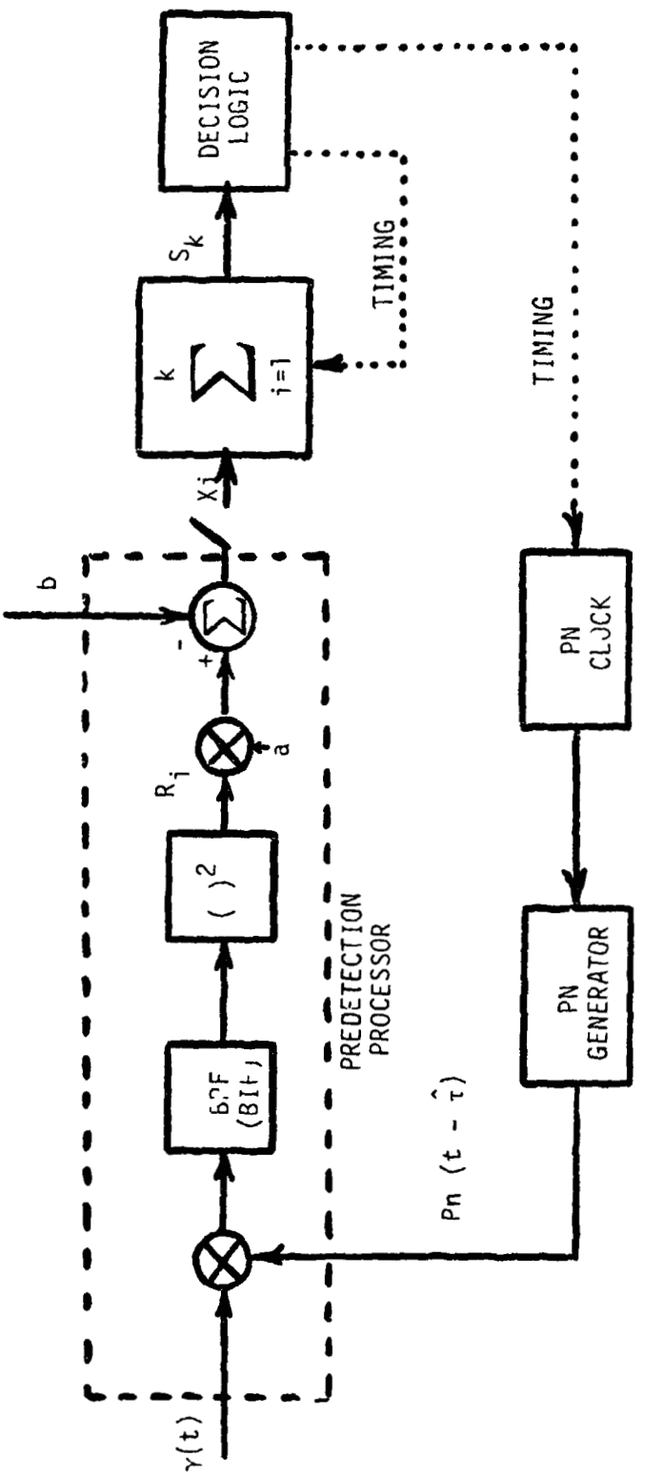


Fig. 3-3. Analytical Model for a PN Acquisition System with Sequential Detection.

$S_k > B$	for all $1 \leq k \leq N_t$	D_1
$S_k \leq B$	for any $1 \leq k \leq N_t$	D_0
otherwise		D

$S_2(B,N_t)$ is usually a preferable choice because:

(1) The truncation time is needed to set an upper bound for the per cell dwell time so as not to reduce the Doppler range over which a coarse synchronization can be detected.

(2) The acquisition time is insensitive to the dwell time spent in H_1-cells. After all, the number of H_0-cells is hundreds or thousands times as large as that of H_1-cells.

Except for the mean dwell time in a H_1-cell, the two tests are practically the same as far as the performance is concerned.

4. Performance Analysis and Numerical Results

4. Summary of Performance Results

In Appendix A, we show that the test statistics $R(nT_0)$ produced serially by the CCD correlator are independent if $\delta = 1$ and exhibit only very small correlations among neighboring $R(nT_0)$'s if $\delta < 1$. Furthermore, if we define a H_1-cell as one which satisfies (2-2) and a H_0-cell which does not, H_1, the hypothesis that the present cell under examination is a H_1-cell and H_0 its complement hypothesis. Then, as mentioned in the beginning section, there are more than one H_1-cell in most cases. Moreover, the number of H_0-cells is much larger than that of H_1-cells. To facilitate our analysis, we shall make the following assumptions: (1) all test statistics are independent no matter what δ is. (2) there is one and only one H_1-cell in the uncertainty region, (3)

the code self noise* is negligible, and (4) M(in chips) >> 1.

Under these assumptions, it can then be shown (Appendix B and D) that the detection and false alarm probabilities, P_{D_1}, P_{FA_1}, for the first stage test are

$$P_{D_1} \doteq \int_{\gamma}^{\infty} P(y|H_1)dy \qquad \text{(4-1a)}$$

(for SPS)

$$P_{FA_1} \doteq \frac{M}{\delta} \int_{\gamma}^{\infty} P(y|H_0)dy \qquad \text{(4-1b)}$$

and

$$P_{D_1} \doteq \int_{0}^{\infty} P(y|H_1)\left[\int_{0}^{y} P(x|H_0)dx\right]^{C_0}dy \qquad \text{(4-2a)}$$

(for SSP)

$$P_{FA_1} = 1 - P_{D_1} \qquad \text{(4-2b)}$$

respectively,

$$P(y|H_1) = \left(\frac{y}{N\beta}\right)^{N-1/2} e^{-(y+N\beta)} I_{N-1}(2\sqrt{N\beta y}) , \qquad \text{(4-3a)}$$

where

$$P(y|H_0) = \frac{y^{N-1}}{(N-1)!} e^{-y} \qquad \text{(4-3b)}$$

N = the number of noncoherent integrations,

$\beta = E_c/N_0$,

$I_{N-1}(\cdot)$ = modified Bessel function of order N-1,

C_0 = the nubmer of H_0-cells.

Detailed analyses and computational algorithms pertaining to P_{D_1} and P_{FA_1} are to be found in Appendix B and D. As for the 2nd stage test, Appendix C contains the derivation of the operation characteristic, P_{D_2}

vs. P_{FA_2}. The mean acquisition times for both algorithms are (see Appendix F)

$$\bar{T}_{ACQ} = \tau_D + (\frac{1}{P_D} - \frac{1}{2})(\tau_{D_1} + P_{FA_1}\tau_{D_2} + P_{FA}\cdot T_p \cdot T_c)N_d N_t, \text{ (SPS)} \quad (4\text{-}4)$$

and

$$\bar{T}_{ACQ} = \tau_D + P_D^{-1}[N(C_{N_0}+1) + \tau_{D_2}P_{FA_1}/T_c + P_{FA}\cdot T_p]T_c, \text{ (SSP)} \quad (4\text{-}5)$$

where

$P_D = P_{D_1} \cdot P_{D_2}$,

$P_{FA} = P_{FA_1} \cdot P_{FA_2}$,

$\tau_D = MT_c$,

$\tau_{D_1} = N\tau_D$,

- = dwell time for the second stage est,

T_p = Penalty time (in chips),

N_D = number of Doppler bins,

N_t = number of time bins.

The analysis details of the sequential detection method are contained in Appendix E.

4.2 Numerical Results

Based upon the above analysis, the numerical behaviors of both CCD algorithms are demonstrated in Fig. 4-1 through Fig. 4-5. An empirical optimization rule is adopted: P_{FA} must be small enough to offset T_p. According to this rule, we set $P_{FA} = 10^{-5}$ such that $(P_{FA} \cdot T_p)T_c$ is of the order of msec even with T_p as large as 10^8. The other system parameters: P_{D_1}, P_{D_2}, P_{FA_1}, τ_{D_1}, τ_{D_2}, unless specified, are chosen to minimize $\bar{T}_{ACQ}$.

Fig. 4-1 shows the SSP performance as a function of N_- and M

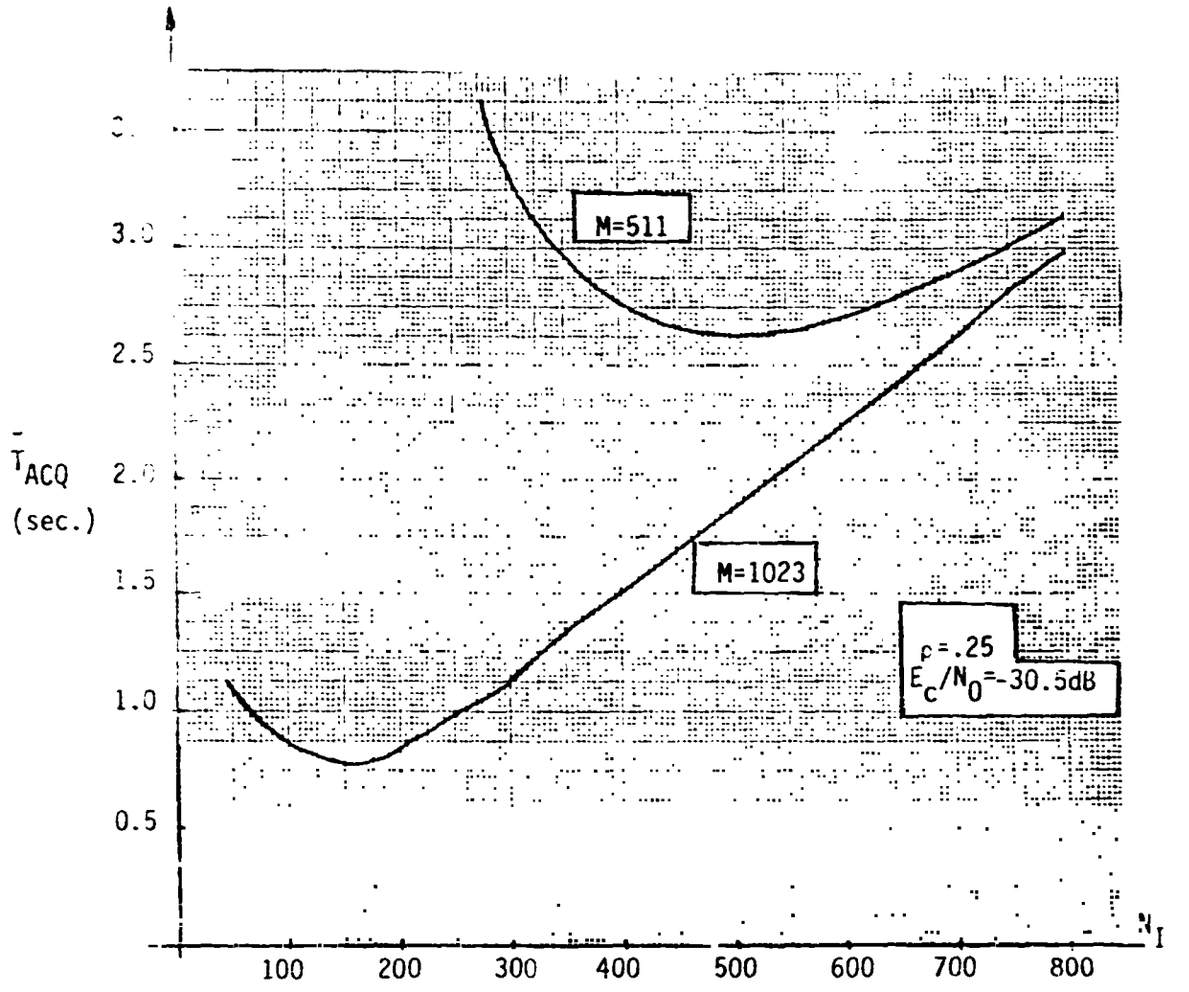


Figure 4 - 1. Mean Acquisition Time for SSP As a Function of N_I.

(chips) when E_c/N_0 = -30.5 dB, $\delta T_c = .5T_c$ and $p \triangleq |\tau-\hat{\tau}|/T_c = .25$. An optimal N_I do exist for each parameter set. The accumulated acquisition probability $F_{ACQ}(t)$ is shown in Fig. 4-2, where we use the formula:

$$F_{ACQ}(t) \triangleq Pr[T_{ACQ}<t]$$

$$= \sum_{n=1}^{[t/T_A]} (1-P_D)^{n-1}P_D, \qquad (4\text{-}6)$$

where

$$T_A \triangleq [N(C_0+1) + \frac{\tau_{D_2}}{T_c} P_{FA_1} + P_{FA}\cdot T_p]T_c, \qquad (4\text{-}7)$$

[x] = the largest integer less than x.

Comparisons can be made: between the best case (p=0) and the worst caes (p=.25), among different M (coherent integration period). The choice of M's is of course dependent on the data rate.

Performances for the SSP and SPS algorithms as a function of E_c/N_0 and N_I are described in Fig. 4-3 and 4-4, which exhibit the importance of a judicious choice of N_I as the E_c/N_0 varies. This is because N_I has put an inherent lower bound on the time required to make a decision (see the flat portions of the curves corresponding to different N_I's in Fig. 4-3 and 4-4).

Comparison between the SPS and SSP algorithms is made in Fig. 4-5 where N_I has been optimized. It can be seen that the SPS algorithm is superior to the SSP algorithm though this superiority is dwindled as E_c/N_0 gets higher. The SSP algorithm, however, is less sensitive to the variation of E_c/N_0 owing to the fact that a threshold for the first stage test is not necessary; see Fig. 4-7 and Fig. 4-8.

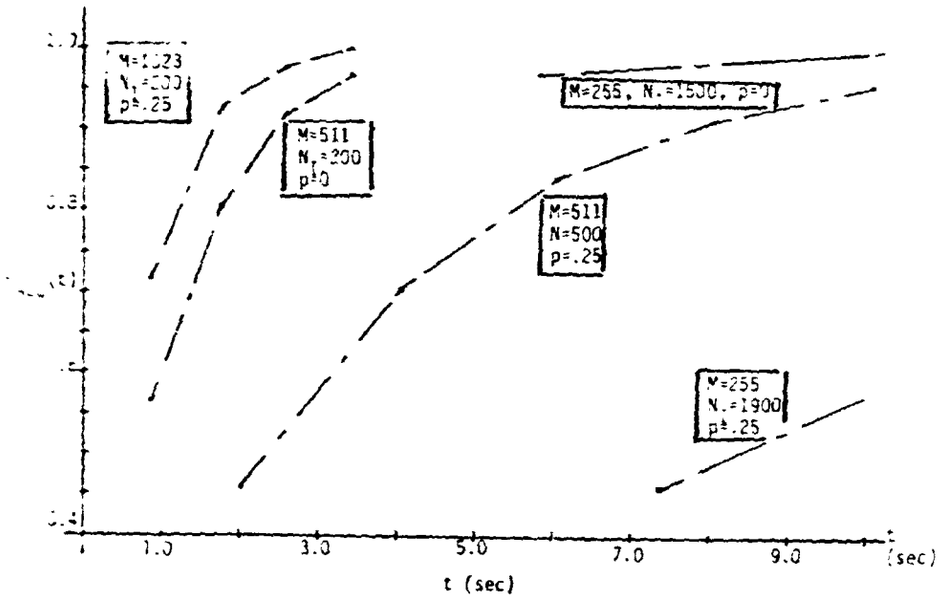


Fig. 4-2. Distribution of Acquisition Time for the SPP Algorithm.

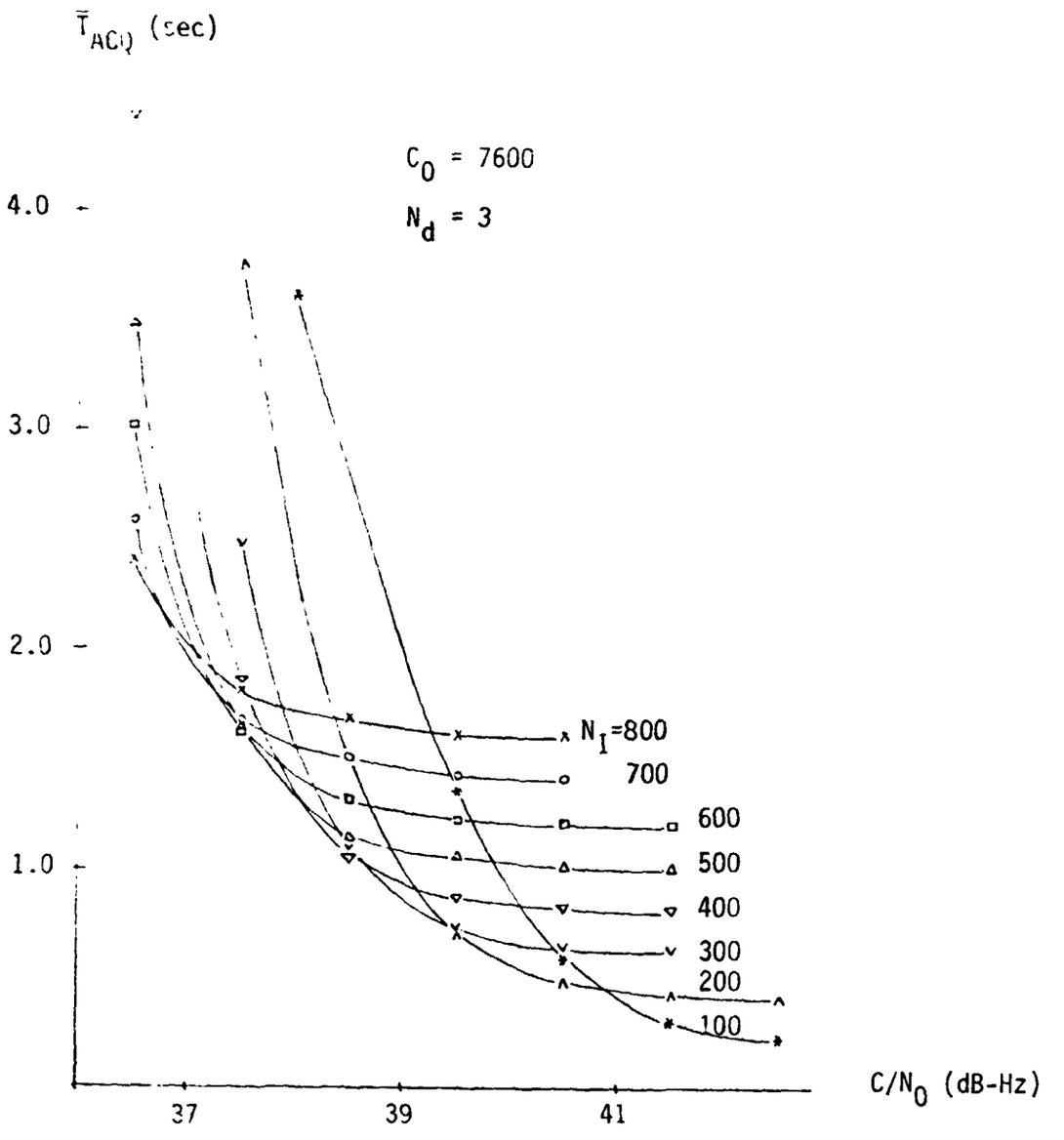


Fig. 4-3. Performance of the SPS Algorithm with Different N_I's.

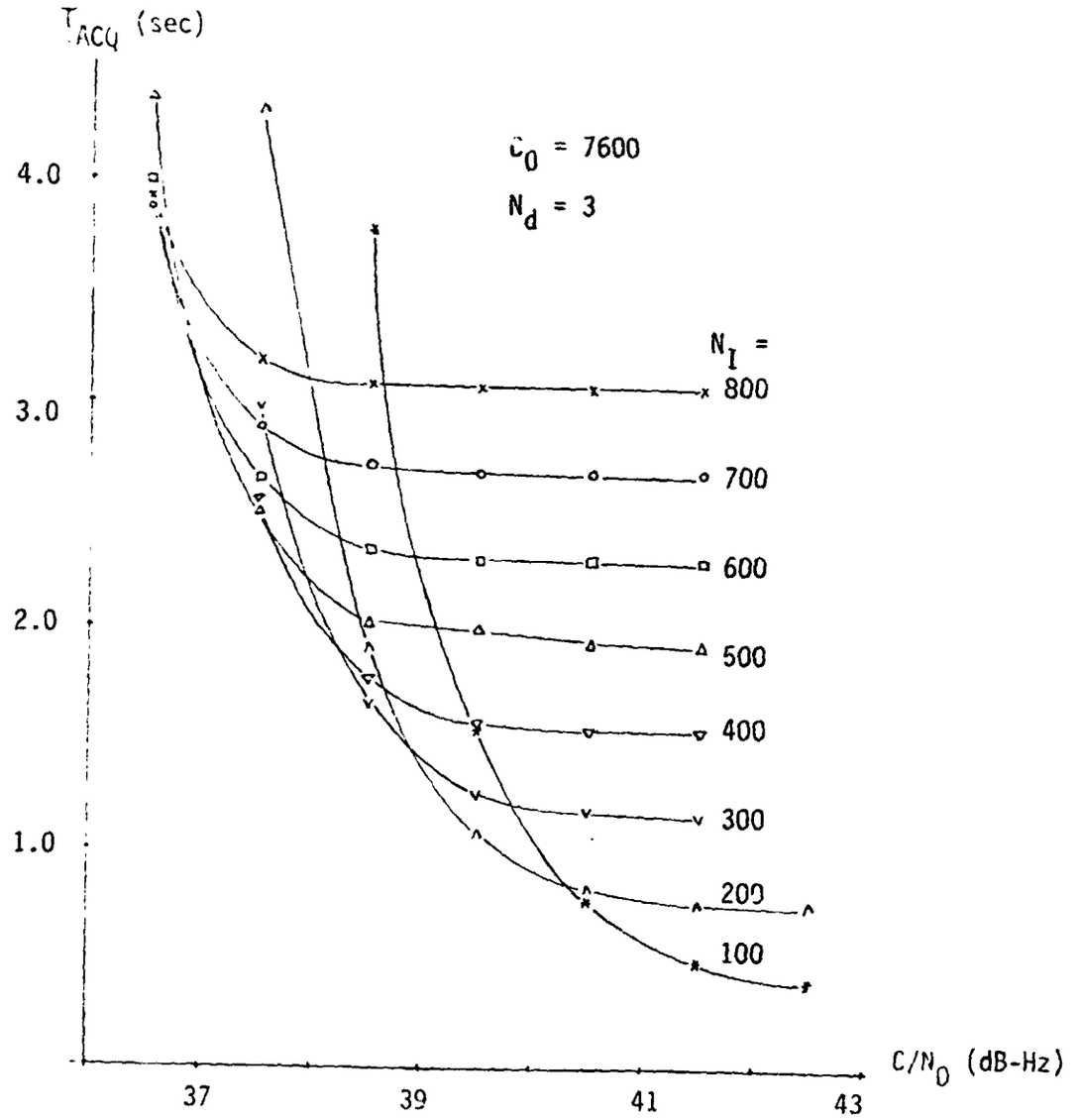


Figure 4-4. Performance of the SSP Algorithm with Different N_I's.

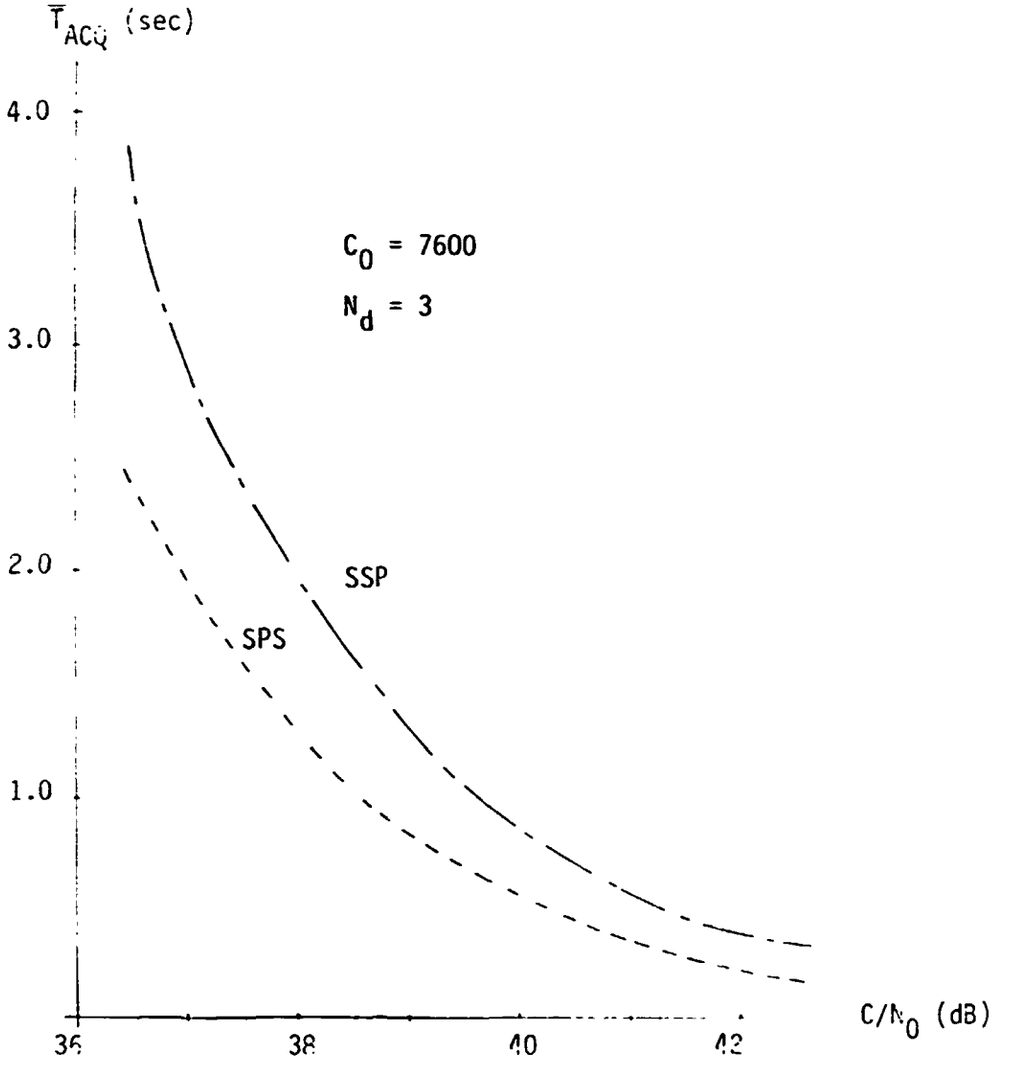
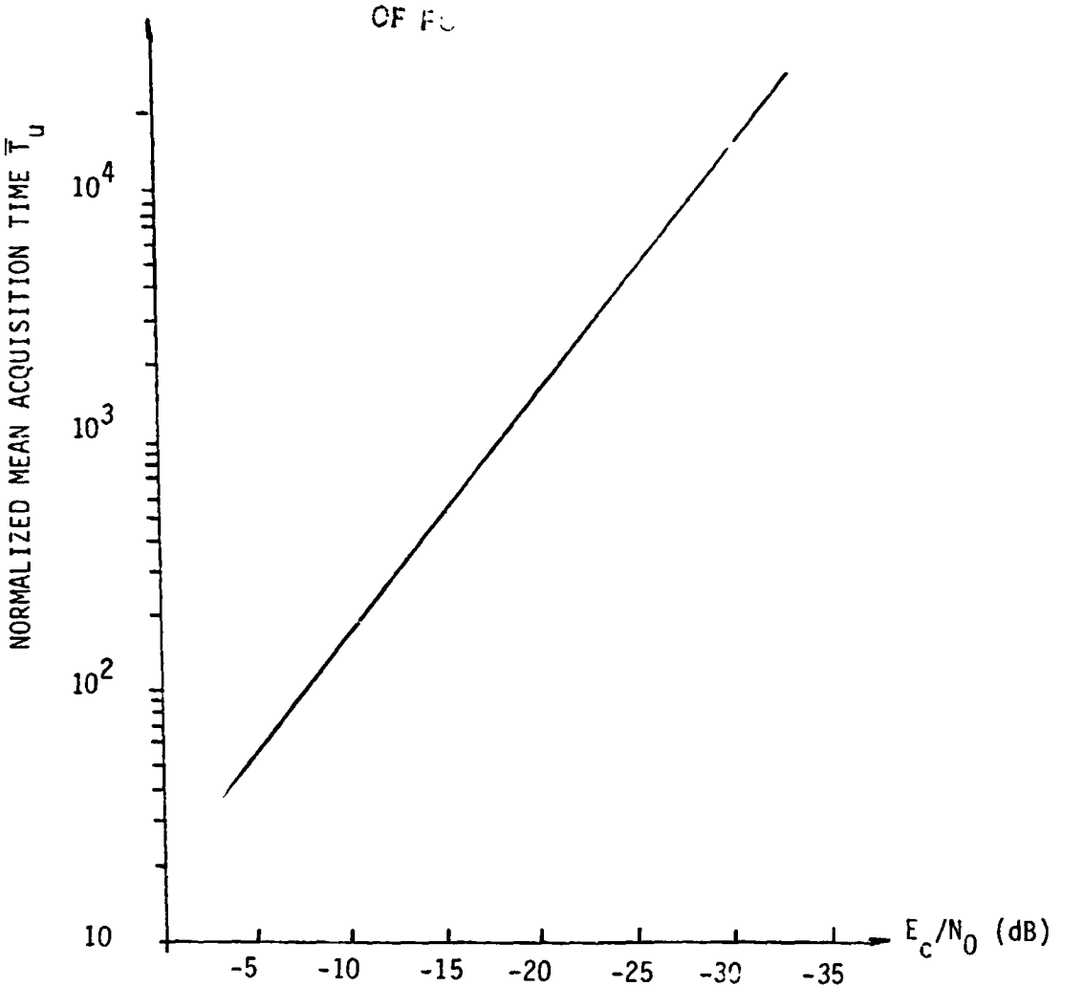


Fig. 4-5. Performance of the Optimal SSP and SPS Systems.

Fig. 4-6. Acquisition Performance With Single Channel Sequential Detection, Worst Case p = .5, $\delta T_c = T_c$.



The relative insensitivity of τ_{D_2} to $\overline{T}_{ACQ}$ can be found in Table 4-1 to 4-3 for both algorithms, where t(0.9) is defined as the time required to acquire with probability 0.9. Note that this number for the SPS is an upperbound; see Appendix F.

The above numerical results are computed with the following parameters:

N_d (Doppler bin)	3
$1+C_0$ (cells per Doppler bin)	7600
δT_c (step size)	0.5 chip
Sampling loss	2.5 dB (p=.25)
Doppler loss	0.4 dB
Data transition loss	0.2 dB
Code chip rate	3 MHz
M	512 (chips)
IF bandpass filter bandwidth	6 MHz
Processing gain	30 dB

Evidently, even with C/N_0 = 36.5 dB-Hz (only one channel is used), i.e., E_c/N_0 = -31.9 dB (sampling loss excluded), we still can acquire within 4 sec with a probability equal to 0.9. The AIRS' acquisition requirement thus can be met without difficulty. For comparison purposes we include here the best sequential test performance (Fig. 4-6). The normalized mean acquisition in Fig. 4-6 can be converted into $\overline{T}_{ACQ}$ in seconds via

$$\overline{T}_{ACQ}(\text{sec}) = \overline{T}_u(1+C_0)T_c. \qquad (4\text{-}8)$$

5. Conclusion and Further Studies

The main results achieved by this study can be summarized as

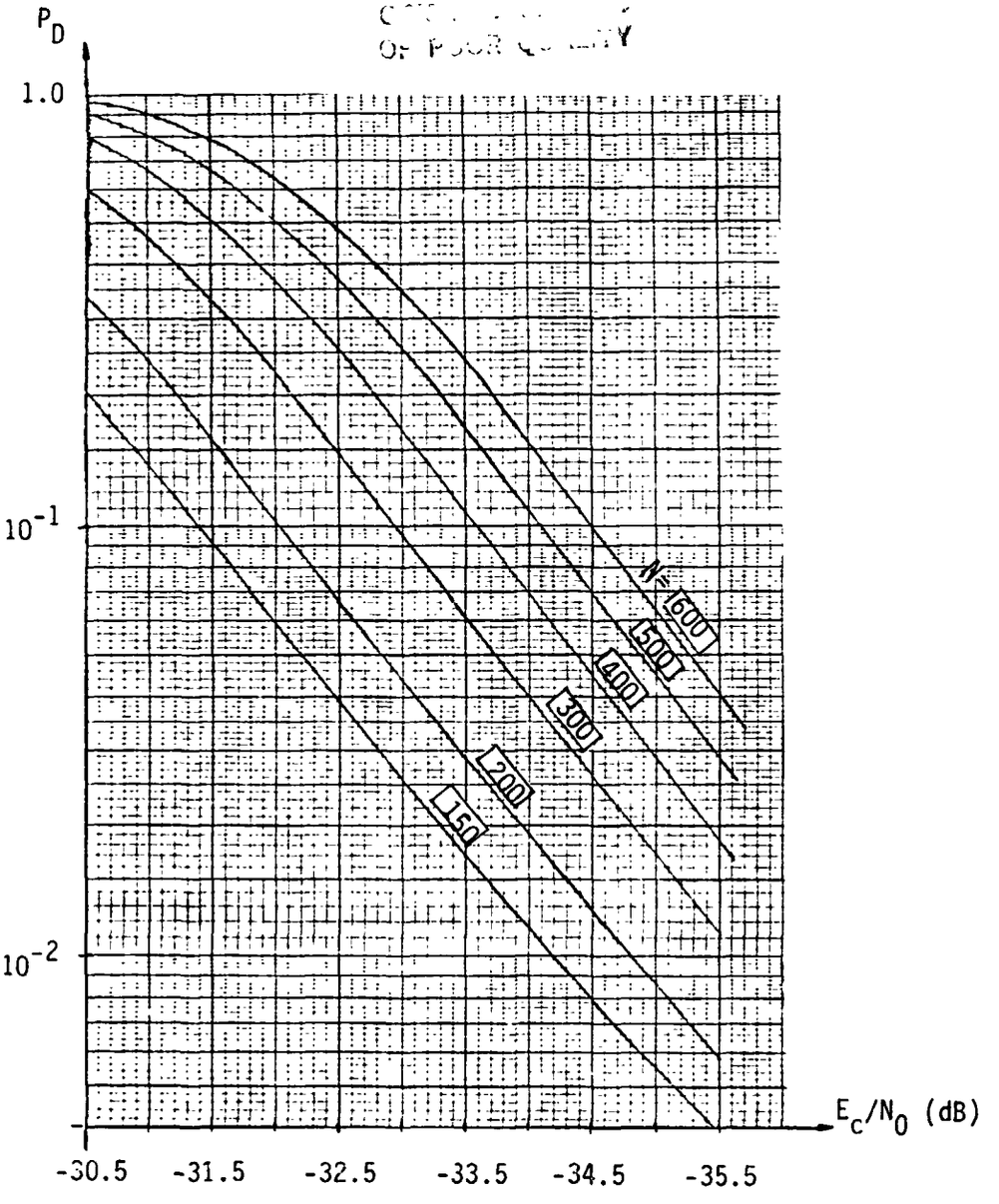


Fig. 4-7. Operation Characteristic of the SSP First Stage Test.

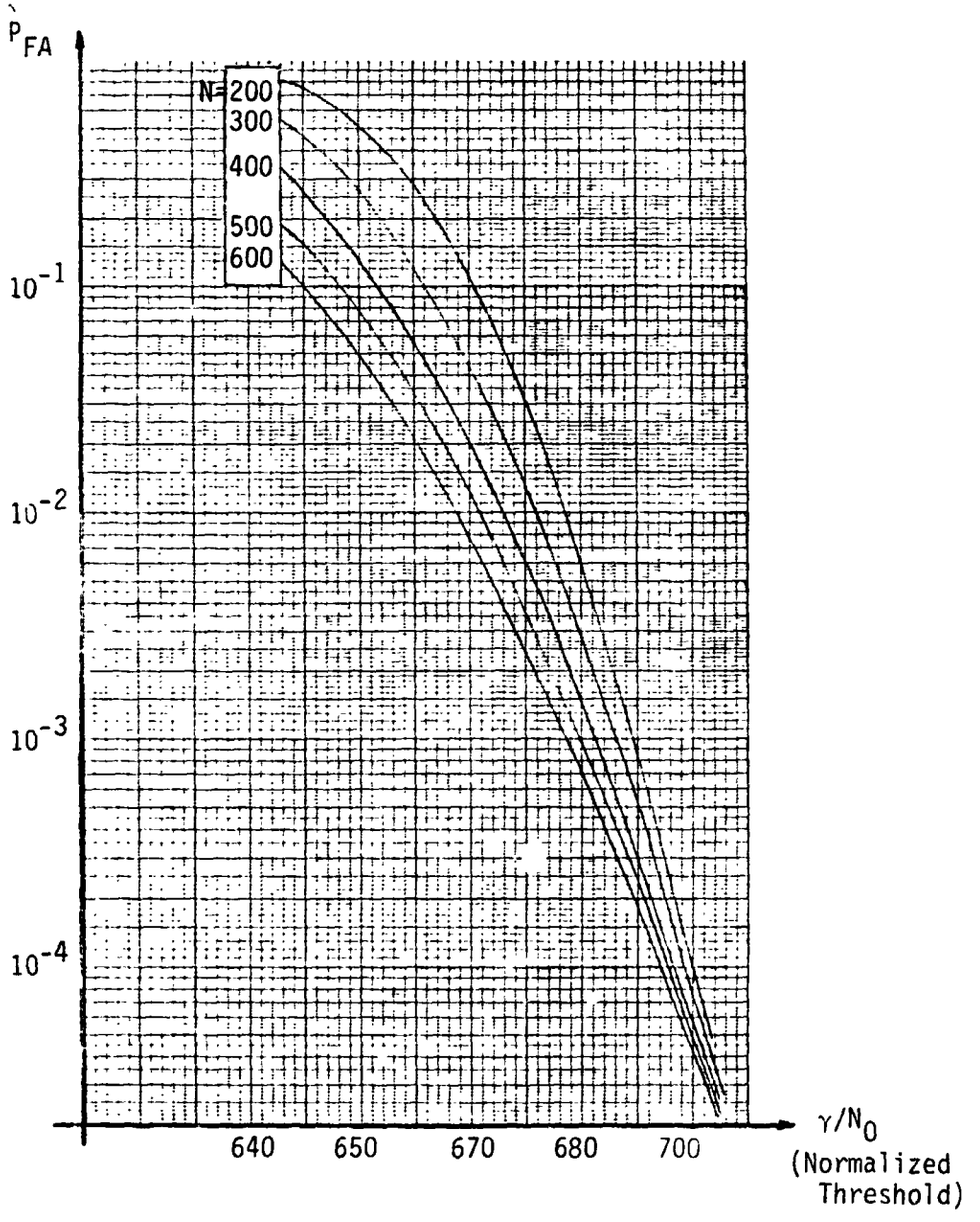


Fig. 4-8a. Operation Characteristic of tne SPS First Stage Test.

E_c/N_0= -35.52 dB

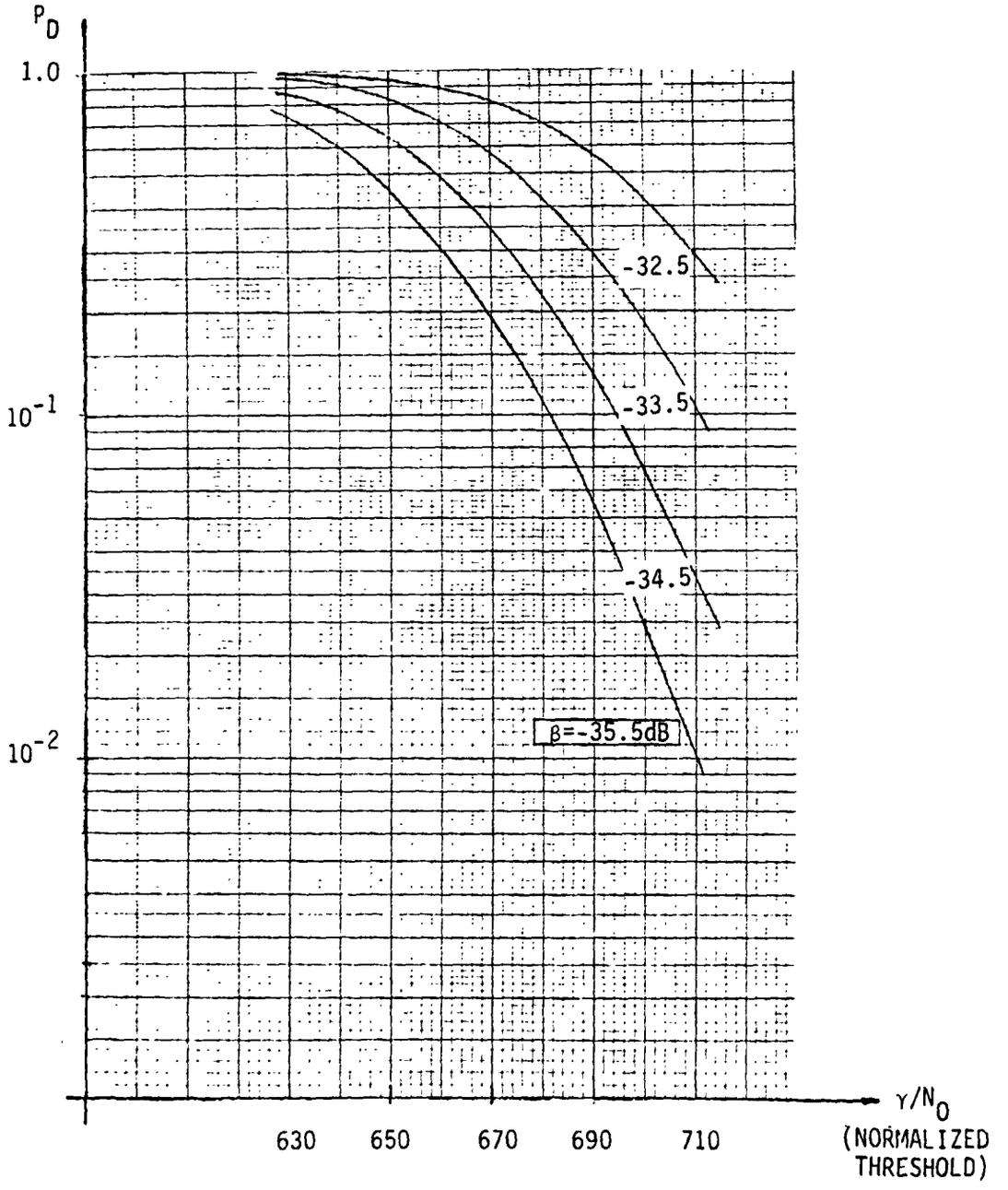


Fig. 4-8b. Operation Characteristic of the SPS First Stage Test.

Table 4-1.* System Performance Parameeers for the SPS.

C/N_0 (dB-Hz)	36.5	37.5	38.5	39.5	40.5
$\bar{T}_{ACQ}$ (sec)	2.58	1.65	1.05	0.722	.494
τ_{D_2} (sec)	1.4(-1)	9.2(-2)	6.2(-2)	4.2(-2)	3.53(-2)
N_I	700	500	400	300	200
P_{D_1}	.743	.794	.908	.948	.960
P_{FA_1}	3.64(-2)	2.94(-2)	3.23(-2)	2.78(-2)	4.85(-2)
P_{D_2}	.990	.991	.992	.993	.990

Table 4-2.* System Performance Parameters for the SSP.

C/N_0 (dB-Hz)	36.5	37.5	38.5	39.5	40.5
$\bar{T}_{ACQ}$(sec)	3.88	2.53	1.65	1.09	.737
τ_{D_2} (sec)	8.3(-2)	5.9(-2)	3.9(-2)	2.6(-2)	2.33(-2)
N_I	700	500	300	200	150
P_{D_1}	.712	.778	.719	.728	.811
P_{FA_1}	.288	.221	.281	.272	.189
P_{D_2}	.995	.995	.995	.994	.993

*R_c = 3 MHz, M = 512 (chips), BW_{IF} = 6 MHz, processing gain = 30 dB.

Table 4-3.* Performance Parameters for the SPS and SSP Algorithms when C/N_0 = 36.5 dB-Hz.

Algorithm	SSP	SPS
$\bar{T}_{ACQ}$ (sec)	4.27	2.56
τ_{D_2} (sec.)	1.0[illegible]-1)	1.67(-1)
N_I	1000	950
t(0.9) (sec.)	3.91	3.89
P_D	.915	.927
P_{FA_1}	8.19(-2)	4.90(-2)

follows.

(I) Precise definitions of two algorithms for code acquisition subsystems using matched filter type correlators.

(II) Rigorous performance analysis for both algorithms. This analysis can be easily applied to other algorithms, e.g., the fast local code algorithm described below or, the sequential test algorithm discussed in Appendix E.

(III) The addition of the second stage test. The improvement due to this addition is similar to that obtained by a two dwell system over a single dwell system.

(IV) Numerical optimizations have been carried out for both algorithms.

(V) Sensitivities of both algorithms are examined and performance comparisons are made.

(VI) Development of a software analysis tool (Appendix G) with versatile capabilities.

We have investigated thus far the behaviors of the SSP and SPS algorithms in the region which features low E_c/N_0, long code period and large or medium uncertainty ranges. This condition, i.e., the parameters chosen in Sec. 4, corresponds to the worst condition the AIRS is supposed to operate. Evidently, from a worst case consideration the SPS algorithm is a preferrable choice.

As to the hardware aspect, it appears that a dual 256-tap CCD correlator will be aviiable this summer from Fairchild and Ford. The device is based on a mask developed by S. C. Munroe of the MIT Lincoln Laboratory [10]. It appears to be directly compatible with the AIRS acquisition requirements. Becasue of the size of the bulky substrate

required, SAW correlators are deemed to be unsuitable for the AIRS application [11].

An improvement on the acquisition subsystem performance presented in Sec. 4 can be achieved by minor modification on our CCD algorithms. The modifications are made in (A.1) and (A.2) (i.e., (B.1) and (B.2)) [9]. Instead of fixed local code reference segment during every coherent integration period, we let the local code run at a rate N+1 times faster than the sampling rate. Hence, before a new sample entering the PNMF, N test statistics are produced. The N+1-th one is discarded because of the concurrent shift of the sampled signal and the local code. Judging from eq. (4-4), (4-5) and Tables (4-1), (4-2), $\overline{T}_{ACQ}$ can be reduced by as much as N times so long as $\tau_{D_1}/N >> \max(\tau_D, P_{FA_1} \cdot \tau_{D_2})$. The achievable local code rate $(N+1)/\delta T_c$ is of course another technology issue. It appears now, for a sampling rate $1/\delta T_c$ = 6M chips/sec, not much room (i.e., N) left to be improved.

Recently, two systems similar to the SSP scheme have been reported. The CCD receiver described in [5] used a quantized NI method: every coherent integration output becomes either 1 or 0, depending on whether it passes a threshold or not. The other one proposed by Holm [7] used 64 bits digital correlators built by TRW along with the fast local code algorithm mentioned before. Because of the digital correlators, hard-limiting on the received waveform is necessary. Both systems are built to operate in a small uncertainty region and high (relatively) E_c/N_0 environment. We hope that the performance evaluations of these two systems can be accomplished in the future so that we can make assertions on the losses incurred by quantizations.

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APPENDIX A

AUTOCORRELATION FUNCTION OF THE CCD CORRELATOR OUTPUT

We want to show, in this appendix, that the output samples of the CCD correlator are (almost) uncorrelated and independent if they are samples corresponding to the code phases in the H_0 region.

Because of the nonlinear operation in both I and Q channels, the uncorrelatedness of the u_0 samples is difficult to prove directly from the statistic of R(t), the correlator output. However, if we can show that samples before the square-law device in both channels are independent then this independence can be carried over to the output, since the squaring operation is memoryless.

For analytical simplicity, we shall assume that (1)* there is no data modulation and (2) the sampling value at $t = nT_0$, $T_0 = T_c/\bar{m}$, $\bar{m} = 1$ or 2. Then the output of the I-channel PNMF is

$$R_I(nT_0) = \cos(\Delta\omega nT_0+\phi) \sum_{k=1}^{M} \{P_n(kT_0)[\sqrt{S}P_n((n-M+k)T_0+\tau) + n((n-M+k)T_0+\tau)]\Delta T_0\} \qquad (A.1)$$

where $|\tau| > T_c$, $n > M$, S is the signal power and ΔT_0 is a constant related to T_0.

From assumption (2) and the uncorrelatedness between $P_n(kT_0)$'s and $n(kT_0)$'s, we have

*As a matter of fact, this assumption is redundant unless $|\tau| < T_c$, because a binary random data modulation sequence will not alter the statistic of R_I or R_Q if $|\tau| \geq T_c$; see also (A.4).

$$E\{R_I(nT_0)R_I(mT_0)|\phi\}$$

$$= \cos(\Delta\omega nT_0+\phi)\cos(\Delta\omega mT_0+\phi)\Delta T_0\{\sum_k\sum_\ell SE[P_n(kT_0)P_n(\ell T_0)P_n((n-M+k)T_0+\tau)$$

$$\cdot P_n((m-M+\ell)T_0+\tau)]$$

$$+\sum_k\sum_\ell E[P_n(kT_0)P_n(\ell T_0)]E[n((n-M+k)T_0+\tau)n((m-M+\ell)T_0+\tau)]\}$$

$$\triangleq \cos(\Delta\omega nT_0+\phi)\cos(\Delta\omega mT_0+\phi)R_I(n,m) \qquad (A.2)$$

Hence,

$$E\{R_I(nT_0)R_I(mT_0)\} = \frac{1}{2}\cos[\Delta\omega(n-m)T_0]R_I(n,m) \qquad (A.3)$$

Observing that

$$E\{n[(n-M+k)T_0+\tau]n[(m-M+\ell)T_0+\tau]\}$$

$$= \delta_{n+k,m+\ell} = \begin{cases} 1 & \text{if } n+k = m+\ell \\ 0 & \text{otherwise} \end{cases} \qquad (A.4)$$

and

$$E[P_n(kT_0)P_n(\ell T_0)] \doteq 0 \quad \text{if } |k-\ell| > \bar{m} \qquad (A.5)$$

we then conclude that the second double summation in the bracket becomes zero if $|n-m| > \bar{m}$.

In case that the PN sequence $\{P_n(t)\}$ can be modeled as a random

binary (±1) sequence, i.e., $MT_c \ll L(\text{Period of } \{P_n(t)\})$, then a similar conclusion for the first double summation can be reached. Furthermore, in the low E_c/N_0 enviroment, this term is negligible even if $|n-m| < \bar{m}$. Looking back at (A.1), we can see that $R_I(nT_0)$ is actually a linear combination of Gaussian R.V.'s and is itself a Gaussian R.V. Independence of $R_I(nT_0)$ follows from the uncorrelatedness. As mentioned before, $R_I^2(nT_0)$ are then independent, so are $R_Q^2(nT_0)$. The independence between I and Q channel is generally valid, so is that of $R_I^2(nT_0) + R_Q^2(nT_0) \triangleq R(nT_0)$.

Notice that there still exists some "residual" correlations among $\bar{m}$ consecutive samples if $\bar{m} > 1$, this residual correlation will be reduced by a factor of N, after N noncoherent integrations, where $N \gg 1$ in all cases of interest. Therefore, for practicl purposes, we can neglect the correlations among these $\bar{m}$ (usually, $\bar{m}=2$) consecutive samples.

APPENDIX B

STATISTICS OF THE FIRST STAGE TEST

We shall derive the detection (P_{D_1}) and false alarm (P_{FA_1}) probabilities for the 1-st stage test of the SPS scheme, those of the SSP search will be discussed in Appendix D. Because

$$S_j = \sum_{i=1}^{N_I} R_{ij} \tag{B.1}$$

where R_{ij} is the sampled value obtained from the i-th coherent integration at the j-th cell, the statistics of R_{ij} under both H_0 and H_1 must be obtained first.

Fig. B.1 shows an equivalent coherent integration circuit, where R_I and R_Q can be written as

$$R_I(MT_c) = \bar{x}(MT_c) \cos \phi + [\tilde{x}(MT_c) \cos \phi + N'(MT_c)] \tag{B.2a}$$

and

$$R_Q(MT_c) = \bar{x}(MT_c) \sin \phi + [\tilde{x}(MT_c) \sin \phi + N'(MT_c)] \tag{B.2b}$$

where

$$\tilde{x}(t) \triangleq x(t) - E[x(t)] \triangleq x(t) - \bar{x}(t) \tag{B.3a}$$

$$x(t) \triangleq (\sqrt{S}T_c)^{-1} \int_0^{MT_c} PN(t+sT_c)PN(t+\hat{s}T_c)dt \tag{B.3b}$$

and $N'(MT_c)$, $N'(MT_c)$ are i.i.d. Gaussian R.V.'s with zero mean and variance $\frac{M}{2}\frac{E_c}{N_0}$ (note we have a normalization factor $1/\sqrt{S}T_c$ in both correlators).

At low E_c/N_0, the fluctuation part of x(t) is negligible, so for a fix ϕ both R_I and R_Q can be regarded as sum of a constant (possibly

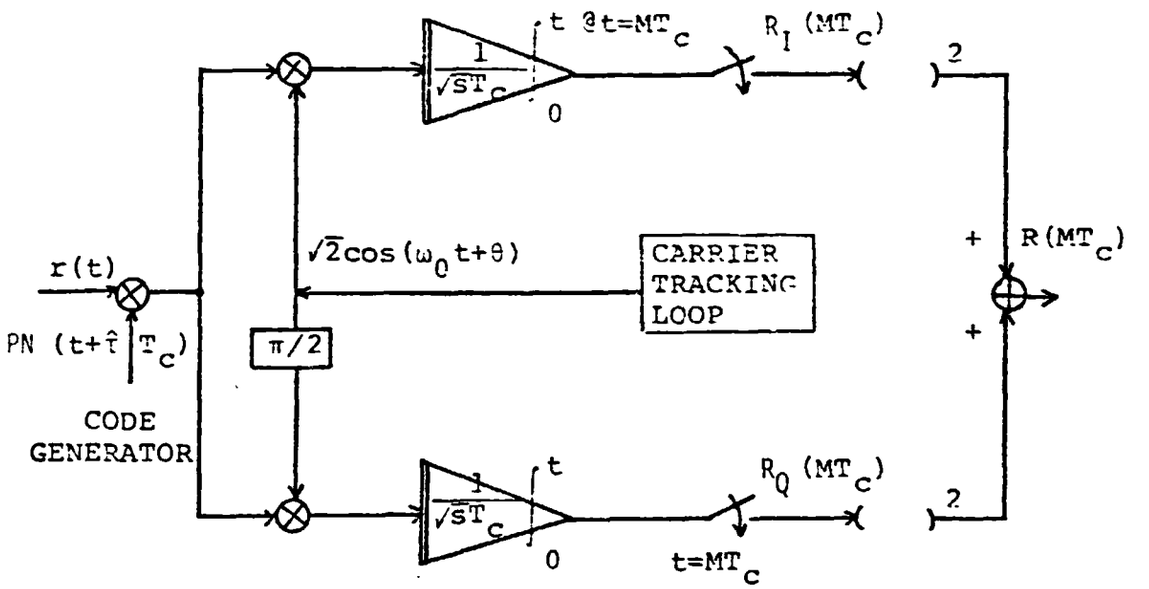

Fig. B.1. An Equivalent Coherent I-Q System.

zero) and a Gaussian R.V. With this assumption, the density functions of $R^2(t)$ under both hypothesis are well-known, i.e., they are [1]

$$P(R(t)|H_1) = (2\sigma^2)^{-1} \exp - \frac{R(t)+m^2}{2\sigma^2} I_0\left(\frac{m}{\sigma^2} R(t)\right) \tag{B.4a}$$

and

$$P(R(t)|H_0) = (2\sigma^2)^{-1} \exp - \frac{R(t)}{2\sigma^2} \tag{B.4b}$$

where

$$\sigma^2 = \frac{1}{2} (E_b/N_0)^{-1}\left(\frac{t}{T_c}\right) \tag{B.5a}$$

$$m = (1-|p|)t/T_c \tag{B.5b}$$

and

$$p = s - \hat{s} \tag{B.5c}$$

Define

$$R(MT_c)/2\sigma^2 \triangleq Z \tag{B.6}$$

$$\frac{m^2}{2\sigma^2}\bigg|_{t=MT_c} = (1-|P|)^2\left(\frac{E_c}{N_0}\right)M \triangleq \beta \tag{B.7}$$

then (B.4a) and (B.4b) becomes

$$P(Z|H_1) = e^{-(Z+\beta)} I_0(2\sqrt{\beta Z}) \tag{B.8a}$$

$$P(Z|H_0) = e^{-Z} \tag{B.8b}$$

It is now straightforward to obtain* [2]

*$P(y|H_0)$ is a version of Chi-square density function of 2N degree freedom and $P(y|H_1)$ is the so-called noncentral Chi-square density with noncentrality parameter β and 2N degree of freedom.

$$P(y|H_0) = \frac{y^{N-1}}{(N-1)!} e^{-y} \qquad \text{(B.9a)}$$

and

$$P(y|H_1) = \left(\frac{y}{N\beta}\right)^{N-1/2} e^{-(y+N\beta)} I_{N-1}(2\sqrt{Ny\beta}) \ , \qquad \text{(B.9b)}$$

where

$$y \triangleq S_j/2\sigma^2 \ ,$$

$$N = N_I \ .$$

P_{D_1} is then equal to

$$P_{D_1} = \int_{\gamma}^{\infty} \left(\frac{y}{N\beta}\right)^{N-1/2} e^{-(y+N\beta)} I_{N-1}(2\sqrt{Ny\beta})dy$$

$$\triangleq Q_N(\beta,\gamma) \qquad \text{(Generalized Q Function).} \qquad \text{(B.10)}$$

Two possible false alarm probabilities must be distinguished:

$$P_{F,1} \triangleq \Pr[\text{a false alarm occurs}|\hat{H}_1] \qquad \text{(B-11a)}$$

$$P_{F,0} \triangleq \Pr[\text{a false alarm occurs}|\hat{H}_0] \qquad \text{(B-11b)}$$

where

$\hat{H}_1 \triangleq$ one and only one samples in the section (M chips) under examination belongs to H_0 region,

and

$\hat{H}_0 \triangleq$ the whole section under examination belong to H_0 region.

It is clear that

$$P_{F,1} = \left(\frac{M}{SS} - 1\right) \hat{P}_{FA} \cdot P_f \tag{B.12a}$$

$$P_{F,0} = \frac{M}{SS} \hat{P}_{FA} \tag{B.12b}$$

where

$$P_f = P_r\{\text{sample value } y \text{ is the largest } | y > \text{threshold}, y \in H_0\},$$

and

$$\hat{P}_{FA} = \int_{\gamma}^{\infty} \frac{y^{N-1}}{\Gamma(N)} e^{-y} dy$$

$$\triangleq 1 - P(N,\gamma)$$

$$= \left(1 + \gamma + \frac{\gamma^2}{2!} + \ldots + \frac{\gamma^{N-1}}{(N-1)!}\right) e^{-\gamma} \tag{B.13}$$

Eq. (B.10) and (B.13) are special cases of Eq. (D.2b) and (D.2a) of Appendix D where computational aspect is discussed. However, (B.10) or (B.13) is much easier to evaluate, for example, Parl [3] has a very stable recursive method for computing $Q_N(\beta,\gamma)$.

A simple lower bound for $P_{F,1}$ is

$$P_{F,1} > \left(\frac{M}{SS} - 1\right) \hat{P}_{FA} .$$

For large M, this becomes

$$P_{F,1} > \frac{M}{SS} \hat{P}_{FA} = P_{F,0} \tag{B.14}$$

Hence setting

$$P_{FA_1} = P_{F,0} = P_{F,1}$$

the resulting system performance, i.e., $\overline{T}_{acq}$, will be an upper bound. Finally, we like to mention that P_{D_1} in (B.10) is actually an upper bound also. The "real" P_{D_1} is

$$P_{D_1} = Q_N(\beta,\gamma)(1 - P_{F,1}) \tag{B.15}$$

However, $P_{F,1} << 1$ is oftentime the case of interest, thus

$$P_{D_1} \doteq Q_N(\beta,\gamma).$$

For large N and small β, P_{FA_1} and P_{D_1} are related by [4]

$$\sqrt{N(1+2\beta)}\phi^{-1}(P_{D_1}) \tilde{=} \sqrt{N}\phi^{-1}(P_{FA_1}) - N\beta \tag{B.16}$$

where $\phi^{-1}(\cdot)$ is the inverse complement error function. This relatin is obtained from Gaussian approximations of $P(y|H_0)$ and $P(y|H_1)$. Hence a rough estimate of required N is

$$\sqrt{N} \approx \beta^{-1}[\phi^{-1}(P_{FA_1}) - \sqrt{1+2\beta}\ \phi^{-1}(P_{D_1})] \tag{B.17}$$

provided

$$\phi^{-1}(P_{FA_1}) < \sqrt{1+2\beta\phi}^{-1}(P_{D_1}) \ .$$

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APPENDIX C

ON THE DERIVATION OF THE RECEIVER OPERATING CHARACTERISTIC (ROC) OF THE SECOND STAGE TEST

Consider the test shown in Fig. C.1, where we define

$$y(MT_c) = \int_0^{MT_c} x^2(t)dt \ , \tag{C.1}$$

and $x^2(t)$ has a bandwidth of W_{BP}, the bandwidth of the BPF before the squaring device.

If $\frac{1}{MT_c} << W_{BP}$, i.e., $W_{BP}MT_c >> 1$ then $x^2(t)$ can be modeled as wideband process. Thus under H_0, it can be easily shown [1] that

$$E[x^2(t)|H_0] = N_0W_{BP}$$

$$\triangleq m_0 \tag{C.2a}$$

and

$$Var[x^2(t)|H_0] = (N_0W_{BP})^2$$

$$\triangleq \sigma_0^2 \ . \tag{C.2b}$$

Hence

$$E[y(MT_c)|H_0] = \int_0^{MT_c} E[x^2(t)]dt = (N_0W_{BP})MT_c \tag{C.3a}$$

$$Var[y(MT_c)|H_0] = N_0^2W_{BP}MT_c \ . \tag{C.3b}$$

Under H_1, the mean and variance of y can be obtained in three steps.

First, by [2] the power spectral density function of $\hat{x}(t)$* (see

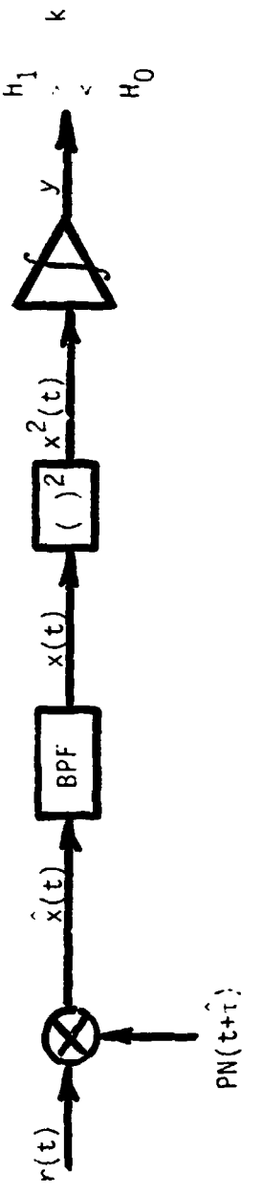

Fig. C.1. A Single Dwell-Time Detector for the Second Stage Test.

Fig. C.1) is

$$\hat{x}(f) = \left(1-|P|\,\frac{L+1}{L}\right)^2 \delta(f) + \frac{L+1}{L}\,p^2 \sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \mathrm{sinc}^2(\pi mp)\,\delta\left(f+\frac{m}{T_c}\right)$$

$$+ \frac{L+1}{L^2}\,p^2 \sum_{\substack{-\infty \\ m\neq 0}}^{\infty} \mathrm{sinc}^2(\pi mp/L)\,\delta\left(f+\frac{m}{LT_c}\right) \qquad |P| < 1 \qquad (C.4)$$

where sinc x = sin x/x.

Secondly, assuming $W_{BP} = 2/T_b = 2R_b$ and $L \gg 1$ then

$$x(f) \doteq s(1-|P|)^2 S(f) \qquad (\text{PSD of } x^2(t)) \qquad (C.5)$$

Finally, we have

$$E[y(MT_c)|H_1] = [S(1-|P|)^2 + N_0 W_{BP}]MT_c \triangleq m_1 \qquad (C.6)$$

$$\mathrm{Var}[y(MT_c)|H_1] = [2S(1-|P|)^2 + N_0 W_{BP}]N_0 MT_c \triangleq \sigma_1^2 \qquad (C.7)$$

A Gaussian approximation via a central-limit theorem type argument ($W_{BP}MT_c \gg 1$) then yields

*In the absence of noise.

$$P_{D_2} = \text{erfc}\left\{ \frac{\sigma_0 \, \text{erfc}^{-1}(P_{FA_2}) + m_0 - m_1}{\sigma_1} \right\}$$

$$= \text{erfc}\left\{ \frac{\text{erfc}^{-1}(P_{FA_2}) - 2\frac{E_c}{N_0}(1-|\rho|)^2\sqrt{MT_c}}{\sqrt{(\frac{E_c}{N_0})n(1-|\rho|)^2 + 1}} \right\} \quad \text{(C.8a)}$$

where

$$n \triangleq \frac{T_b}{T_c} . \quad \text{(C.8b)}$$

In the above discussion, we have assumed that the second stage test (verification mode) use a circuit like that shown in Fig. C.1 which may be taken from one arm of the tracking loop. On the other hand, we can utilize the first stage test circuit for the verification mode; in that case, the ROC is the same as eq. (B.10) and (B.13) derived in Appendix B.

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APPENDIX D

ON THE COMPUTATION OF P_{FA_1} (AND P_{D_1})

D.1 General Discussions

From Appendix B, we know that the summation of N noncoherent integrations has the following two different distributions:

$$P(y|H_0) = \frac{y^{N-1}}{(N-1)!} e^{-y} \tag{D.1a}$$

and

$$P(y|H_1) = \left(\frac{y}{N\beta}\right)^{N-1/2} e^{-(y+N\beta)} I_{N-1}(2\sqrt{Ny\beta}) \tag{D.1b}$$

where

$$\beta = M(1-|\rho|)^2 \frac{E_c}{N_0}, \tag{D.1c}$$

and $I_{N-1}(x)$ is the modified Bessel function of order N-1. Since all y correspond to code epoch in H_0 region are independent (Appendix A), we have, for the SSP algorithm,

$$\begin{aligned} P_{FA} &\triangleq \Pr\{\text{one of } y \text{ in } H_0 \text{ region has the maximum value}\} \\ &= C_0 \int_0^\infty P(y|H_0)\left\{\left[\int_0^y P(x|H_1)dx\right]\left[\int_0^y P(x|H_0)dx\right]^{C_0-1}\right\}dy \\ &\triangleq C_N \int_0^\infty P(y|H_0)F(y|H_1)F^{C_0-1}(y|H_0)dy \end{aligned} \tag{D.2a}$$

or, equivalently,

$$P_{FA} = 1 - P_D$$

$$= 1 - \Pr\{\text{the y from } H_1 \text{ region has the maximum value}\}$$

$$= 1 - \int_0^\infty P(y|H_1)\left[\int_0^y P(x|H_0)dx\right]^{C_0}dy$$

$$= \int_0^\infty P(y|H_1)[1 - F^{C_0}(y|H_0)]dy \qquad \text{(D.2b)}$$

where

$$C_0 \triangleq C-1 \ . \qquad \text{(D.2c)}$$

The above equation was shown by Lindsey [8] to have the following expansion:

$$P_{FA} = \frac{1}{C} \sum_{n=2}^{C} (-1)^n \binom{C}{n} \exp\left[-\frac{(n-1)n\beta}{n}\right] \sum_{k=0}^{(n-1)(N-1)} \alpha_{k,n}\, k!\, L_k^{(N-1)}\left(-\frac{N\beta}{n}\right) n^{-(N+k-1)} \qquad \text{(D.3)}$$

where $L_k^{(N-1)}(-y)$ is the k-th generalized Laguerre polynomial of order N-1, and $\alpha_{k,n}$ is the k-th coefficient of x^k in the expansion

$$\left(\sum_{m=0}^{C_0} \frac{x^m}{m!}\right)^n = \sum_{k=0}^{nC_0} \alpha_{k,n} x^k \ .$$

It is well known that $L_k^{(N-1)}(-y)$ can be computed by [4, Ch. 22]

$$L_0^{(N-1)}(-y) = 1$$

$$L_1^{(N-1)}(-y) = y + N$$

$$\vdots$$

$$L_k^{(N-1)}(-y) = \frac{1}{k}(y+N+2k-2)L_{k-1}^{(N-1)}(-y) \qquad \text{(D.4)}$$

$$+ \quad (N+k-2)L_{k-2}^{(N-1)}(-y).$$

With the initial condition:

$$\alpha_{0,n} = 1 \qquad , \quad 1 \leq n \leq C_N$$

$$\alpha_{k,1} = 1/k! \qquad , \quad 0 \leq k \leq N-1 \qquad \text{(D.5a)}$$

$\alpha_{k,n}$ can be obtained via the recursion

$$\alpha_{k,n} = \sum_{i=0}^{\min(k,L-1)} \frac{\alpha_{k-i,n-1}}{i!} . \qquad \text{(D.5b)}$$

For the special case $C_0 = 1$, (D.2b) can be expressed by [1]

$$P_{FA} = \frac{e^{-N\beta/2}}{2} \sum_{i=0}^{(N-1)} \left\{ \frac{(\frac{N\beta}{2})^i}{i!(N+i-1)!} \sum_{k=i}^{N-1} \frac{(N+k-1)!}{(k-i)!2^{N+k-1}} \right\} \qquad \text{(D.6)}$$

Unfortunately, both (D.3) and (D.6) become useless when N or C_N is very large. For large N and C=2, Marcum [1] derives the following Gram-Charlier series expansion for P_{FA}:

$$P_{FA}(2) = \frac{1}{2}[1-\phi^{-1}(T)] + C_3\phi^{(2)}(T) - C_4\phi^{(3)}(T) - C_6\phi^{(5)}(T)... \qquad \text{(D.7)}$$

where

$$T \triangleq \beta \sqrt{\frac{N}{2(1+\beta)}} \quad , \tag{D.8a}$$

$$C_3 = -\frac{\beta}{2\sqrt{2N}\,(1+\beta)^{3/2}} \quad , \tag{D.8b}$$

$$C_4 = \frac{1+2\beta}{8N(1+\beta)^2} \quad , \tag{D.8c}$$

$$C_6 = \frac{\beta^2}{16N(1+\beta)^3} \quad , \tag{D.8d}$$

$$\phi(y) = \frac{1}{\sqrt{2\pi}} e^{-y^2/2} \quad , \tag{D.8e}$$

$\phi^{(i)}(y)$ denotes the i-th derivative w.r.t. y and

$$\phi^{-1}(y) \triangleq \frac{1}{\sqrt{2\pi}} \int_{-y}^{y} e^{-a^2/2} da \quad . \tag{D.8f}$$

Using the union bound along with (D.7), then

$$P_{FA} \leq C_0 P_{FA(2)} \tag{D.9}$$

In case of large C_0, more terms on the Gram-Charlier series may be needed in order that (D.9) can render useful results.

D.2 Numerical Algorithm

We now proceed to describe a direct numerical evaluation algorithm for P_{FA} by use of (D.2b).

First let us define $\hat{F}(y) \triangleq 1 - F^{C_0}(y|H_0)$. Since $\hat{F}(y)$ is a monotone decreasing function of y for any fix N and C_0, it is easy to see

$$P_{FA} = \int_0^{\infty} P(y|H_1)\hat{F}(y)dy$$

$$= \int_0^{\alpha} P(y|H_1)\hat{F}(y)dy + R(\alpha) \qquad (D.10)$$

where

$$R(\alpha) = \int_{\alpha}^{\infty} P(y|H_1)\hat{F}(y)dy$$

$$< \hat{F}(\alpha) \int_{\alpha}^{\infty} P(y|H_1)dy$$

$$< \hat{F}(\alpha) \; . \qquad (D.11)$$

P_{FA} can thus be obtained by evaluating the 1-st term on the right hand side of (D.10) with a truncation error less than $\hat{F}(\alpha)$.

To have an accurate calculation of the integral

$$\int_0^{\alpha} P(y|H_1)\hat{F}(y)dy \qquad (D.12)$$

one has to have algorithms to render precise values of $P(y|H_1)$ and $\hat{F}(y)$ in the first place. $P(y|H_1)$ can be obtained from standard routine [3] with minor modifications to avoid overfloating or underfloating problems. F(y) will be evaluated by the following algorithm* suggested by Chie [2].

Let K_0 be the integer such that

*Simple closed form approximations valid in some region can be found, for example in [4], or [7].

$$\frac{x^{k_0}}{k_0!} = \max_{1\le i\le N-1} \left\{\frac{x^i}{i!}\right\}, \qquad x > 0$$

then

$$k_0 = [x] \triangleq \text{decimal part of } x \qquad \text{if } N-1 > x$$

$$= N-1 \qquad \text{if } N-1 < x .$$

Let $[10^{-z},10^{z}]$ be the range of real numbers the available computer can handle, then

$$F(y|H_0) = 1 - e_{N-1}(y)e^{-y} \tag{D.13}$$

where

$$e_{N-1}(y)e^{-y} = \left(\sum_{k=1}^{N-1} \frac{y^k}{k!}\right)e^{-y}$$

$$< (N-1)\frac{y^{k_0}}{k_0!}\, e^{-y} < 1 \tag{D.14}$$

Hence if

$$(N-1)\frac{y^{k_0}}{k_0!}\, e^{-y} < 10^{-z}$$

then

$$F(y|H_0) \doteq 1 .$$

Assuming $(N-1)y^{K_0}e^{-y}/K_0! > 10^{-z}$ henceforth, we shall describe the algorithm for two distinct cases.

Case I. $N-1 < x$

1) Let $$t_1 = \frac{y^{N-1}}{(N-1)!}\, e^{-y}$$

$$t_i = \frac{y^{N-i}}{(N-i)!}\, e^{-y}$$

2) Compute

$$S_k = \sum_{i=1}^{k} t_i$$

until

$$(N-1-k)t_{k+1}/S_k < 10^{-E} \text{ or } K = N-1,$$

where E is a predetermined positive integer.

3) Let $\hat{K}$ be the largest integer which statisfies the above condition and set $F(y|H_0) \triangleq 1-S_{\hat{k}}$. The resulting truncation error will be less than $10^{-E}[1-F(y|H_0)]$.

Case II. $N-1 > x$

Let

$$t_1 \triangleq \frac{y^{k_0}}{k_0!} e^{-y}$$

$$t_i \triangleq \frac{y^{k_0-i}}{(k_0-i)!} e^{-y}$$

2) Compute

$$S_k = \sum_{i=1}^{K} t_i$$

until

$$(K_0-K)t_{K+1}/S_K < 10^{-E_1}$$

or

$$K_0 < K$$

3) Let $\hat{K}$ be the largest integer which satisfies the above condition and let

$$t_{\hat{K}+i} = \frac{x^{K_0+i}}{(K_0+i)!} e^{-y}$$

4) Compute

$$S_\ell = \sum_{i=1}^{\ell} t_i = S_{\hat{K}} + \sum_{i=1}^{\ell-\hat{K}} t_{\hat{K}+i}$$

until

$$[N-1-\ell-(K_0-\hat{K})]t_{\ell+1}/S_\ell < 10^{-E_2}$$

or

$$N-1-K_0 < (\ell-\hat{K})$$

The resulting truncation error, after setting $F(y|H_0) = 1-S_{\hat{\ell}}$, where $\hat{\ell}$ is defined similar to $\hat{K}$, will be less than

$$(10^{-E_1}+10^{-E_2})S_{\hat{\ell}} .$$

Observing that $\hat{F}(y)$ behaves like a step function (see Fig. D.1), we further split (D.12) into two integrals:

$$\int_0^{\alpha_1} P(y|H_1)\hat{F}(y)dy + \int_{\alpha_1}^{\alpha} P(y|H_1)\hat{F}(y)dy \qquad (D.15)$$

where α_2 is the smaller one between $\hat{F}(\alpha_2) = 0.9$ and $\alpha_2 = N(1+\beta)$. Each integral will in turn be calculated according to an adaptive Gaussian quadratic rule [2].

D.3 Gaussian Approximation

Note that both $P(y|H_0)$ and $P(y|H_1)$ converge to a Gaussian density as $N \to \infty$ (see also Fig. D.1). This fact suggests that we substitute the following approximations

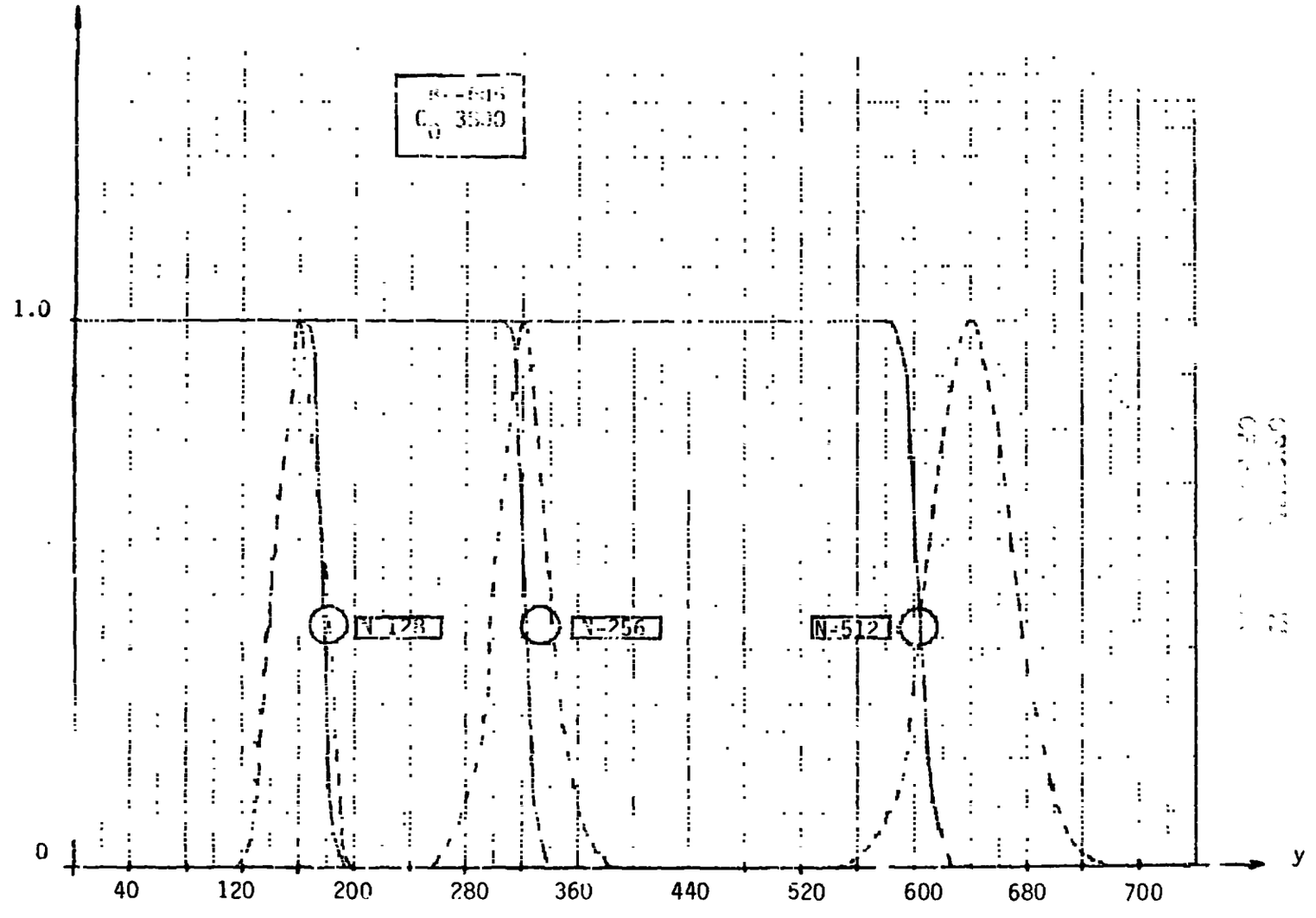

Figure D.1. Behavior of $\hat{F}(y)$ and $P(y|H_1)$.

___ For $\hat{F}(y)$

--- For $P(y|H_1)$ (normalized w.r.t. Peak Vlaue of $P(y|H_1)$

$$P(y|H_0) \doteq \frac{1}{\sqrt{2\pi}\sigma_0} \exp - (y-m_0)^2/2\sigma_0^2 \qquad \text{(D.16a)}$$

$$P(y|H_1) \doteq \frac{1}{\sqrt{2\pi}\sigma_1} - \exp - (y-m_1)^2/2\sigma_1^2 \qquad \text{(D.16b)}$$

with

$$\begin{aligned} m_1 &= N(1+\beta) \\ m_0 &= N \\ \sigma_1^2 &= N(1+2\beta) \\ \sigma_0^2 &= N \ , \end{aligned} \qquad \text{(D.16c)}$$

into (D.2b) and change the low limits to $-\infty$ to get

$$P_{FA} = 1 - \frac{1}{\sqrt{2\pi}\hat{\sigma}} \int_0^{\infty} [e^{-\frac{(u+\hat{m})^2}{2\hat{\sigma}^2}} \phi^{C_0}(-u) + e^{-\frac{(u-\hat{m})^2}{2\hat{\sigma}^2}} \phi^{C_0}(u)]du \qquad \text{(D.17)}$$

where

$$\hat{\sigma} \triangleq \sigma_1/\sigma_0 = (1+2\beta)^{1/2}$$

$$\hat{m} \triangleq \frac{m_1-m_0}{\sigma_0} = \sqrt{N}\beta$$

$$\phi(u) \triangleq \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{u} e^{-t^2/2}dt \ . \qquad \text{(D.18)}$$

For $C_0 = 1$, (D.17) becomes

$$P_{FA} = \phi\left(\frac{\hat{m}}{\hat{\sigma}}\right) - \frac{e^{-\hat{m}^2/2\hat{\sigma}^2}}{\sqrt{\pi/2}\,\hat{\sigma}} \int_0^{\infty} \phi(u) e^{-u^2/2\hat{\sigma}^2} \sinh\left(\frac{\hat{m}}{\hat{\sigma}^2} u\right)du \qquad \text{(D.19)}$$

The Gaussian approximations (D.17) and (D.19) are compared with direct computation described before. Some selected numerical results are shown in Table D.1a-D.1c.

Finally, if we substitute the power series

$$\phi(u) = \frac{1}{2} + \frac{e^{-u^2/2}}{\sqrt{2\pi}} \sum_{n=0}^{\infty} P(n)u^{2n+1} \tag{D.20}$$

$$P(n) \triangleq [1\cdot 3\cdot 5 \ \ldots \ (2n+1)]^{-1} \tag{D.21}$$

into (3.19), we find, after some manipulations,

$$P_{FA} = \frac{1}{2} - \frac{1}{2\pi\hat{\sigma}} \exp\left[-\left(\frac{\hat{m}^2}{2\hat{\sigma}^2} - \frac{c^2\hat{\sigma}^2}{8\hat{m}}\right)\right]$$

$$\cdot \sum_{n=0}^{\infty} \overline{P}(n)\left[D_{-(2n+1)}\left(\frac{\hat{m}/\hat{\sigma}^2}{\sqrt{2C}}\right) - D_{-(2n+1)}\left(-\frac{\hat{m}/\hat{\sigma}^2}{\sqrt{2C}}\right)\right] \tag{D.22}$$

where

$$\overline{P}(n) = 4n!/C^{n+1} \tag{D.23}$$

$$C = \frac{1}{2} + \frac{1}{2\hat{\sigma}^2}$$

and

$$D_{-n}(y) \triangleq \frac{e^{-y^2/4}}{\Gamma(n)} \int_0^{\infty} e^{-yt-\frac{t^2}{2}} t^{n-1} dt \tag{D.24}$$

is the Parabolic Cylinder Function. Unfortunately, this series expansion cannot tell us the behavior of the P_{FA} explicitly.

Table D.1. Gaussian Approximation, $P_{FA}(G)$, for False Alarm Probability, $P_{FA}(E)$. (a) $C_{N_0} = 10^{\hat{}}$ ^{N} = 512. (b) $C_{N_0} = 10^3$, β = -6 dB. (c) N = 256, β = -6 dB

Table D.1a.

β (dB)	-6	-5	-4
$P_{FA}(G)$	2.82(-2)	1.69(-3)	1.95(-5)
$P_{FA}(E)$	3.50(-2)	1.98(-3)	1.75(-5)

Table D.1b.

N	32	64	128	256	512
$P_{FA}(G)$	.924	.833	.62?	.270	.028
$P_{FA}(E)$	.958	.891	.70?	.329	.035

Table D.1c.

C_{N_0}	1	10^3	$4x10^3$
$P_{FA}(G)$	.533(-2)	.270	.376
$P_{FA}(E)$	.511(-2)	.330	.460

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APPENDIX E

ON THE PERFORMANCE OF $S_1(A,B)$ AND $S_2(a,b,B_0,N_t)$

E.1 Performance of $S_1(A,B)$

Let $\{X_n, n=1,2,3,\ldots\}$ be a sequence of i.i.d. R.V.'s. Define $S_k \triangleq \sum_{n=0}^{k} X_n$, where $X_0 = x_0$ with probability one, and $t \triangleq \inf\{k: S_k \notin (A,B)\}$, where $A > 0 \geq B$. If $f(x|H_i)$ is the common probability density function of X_n, $n > 0$ given that the hypothesis H_i holds, then

$$P_i(x_0) \triangleq \Pr[X_0=x_0, S_t \epsilon d_i] \qquad x_0 \epsilon (A,B)$$

$$= \Pr[X_0=x_0, S_1 \epsilon d_i] + \int_B^A P_i(z) f(z-x_0|H_i)dz$$

$$\triangleq \pi_i(x_0) + \int_B^A P_i(z) f(z-x_0|H_i)dz \qquad (E.1)$$

where

$$d_1 \triangleq \{x: x > A\} \qquad (E.2a)$$

$$d_0 \triangleq \{x: x < B\} \qquad (E.2b)$$

Similarly, if we define

$$E_i(x_0) = E\{t|X_0=x_0, S_t \epsilon d_i\} \qquad (E.3)$$

then

$$E_i(x_0) = 1 + \int_B^A E_i(z) f(z-x_0|H_i)dz \qquad (E.4)$$

Eq. (E.1) and (E.4)* were given by Anscombe [1] and Kemperman [2]. Two similar equations were obtained by Albert [3] for analyzing the so-called generalized sequential test. Kendall [4] then applied Albert's work to the special case where

$$X_i = aR_i - b \ , \tag{E.5}$$

and

$$f(x|H_0) = \frac{1}{a} e^{-(x+b/a)} \qquad x > -b \tag{E.6a}$$

$$f(x|H_1) = \frac{1}{a} \exp-(\frac{x+b}{a} +\beta) I_0(2\sqrt{\frac{\beta}{a}(x+b)}) \qquad x > -b \tag{E.6b}$$

The first set of integral equations, i.e.,

$$P_0(x_0) = \exp - \frac{1}{a}(A-x_0+b) + \int_{\max(x_0-b,B)}^{A} a^{-1} P_0(y) e^{-(y+b-x_0/a)} dy$$

$$B < x_0 < A \tag{E.7}$$

and

$$E_0(x_0) = 1 + \frac{1}{a} \int_{\max(x_0-b,B)}^{A} E_0(y) e^{-(y-x_0+b/a)} dy$$

$$B < x_0 < A \tag{E.8}$$

were solved by Kendall [4], while the set corresponding to the H_1 case has eluded all effort to derive a closed form solution. Nevertheless,

*Both belong to the class of Fredholm equations of the 2nd kind.

for the case we are interested in, i.e., $P_{FA} \triangleq P_0(0) \ll P_D \triangleq P_1(0)$, or, $A \gg |B|$, the so-called Wald's approximations are valid because of the fact that $B < 0 < E(X_i) \ll A$. Now, let us look at the solutions of (E.7) and (E.8) first. They are

$$P_{FA} = P_0(0)$$

$$= \frac{G[-DB;Db]}{G[D(A-B+b);Db]} e^{-\alpha D(A+b)} \tag{E.9}$$

$$\bar{T}_0 \triangleq E_0(0)$$

$$= e^{-\alpha DB} H[-DB;Db] + P_0(0)\{1-e^{\alpha D(A-B+b)} H[D(A-B+b);Db]\}, \quad B<0<A \tag{E.10}$$

where

$$G(x;c) \triangleq 1 + \sum_{j=1}^{n} \frac{(jc-x)^j}{j!} \quad c \leq nc \leq x \leq (n+1)c \tag{E.11}$$

$$H(x;c) \triangleq (n+1)e^{-\alpha x} - \sum_{j=1}^{n} \sum_{i=0}^{j-1} \frac{(jc-x)^i}{i!\alpha^{j-i}} \quad c \leq nc \leq x \leq (n+1)c \tag{E.12}$$

and

$$\alpha \triangleq e^{b/a} = a^{-1}D \tag{E.13}$$

The above formulae become useless when $(A-B)/b \gg 1$. Good approximations utilizing Laplace transformation method were also derived by Kendall [Appendix,4]. After some rearrangements of Kendall's approximation formula, we reach the following numerically stable

equations:

$$P_{FA} = \frac{(\alpha Db-1)e^{DB(\gamma-\alpha)}-(1-\gamma Db)}{(\alpha Db-1)e^{D(h+b)(\alpha-\gamma)}-(1-\gamma Db)} \tag{E.14}$$

$$\bar{T}_0 = (\alpha Db-1)^{-1}\left[\frac{(\alpha Db)^2}{2(\alpha Db-1)} - 1 - \alpha DB\right] - \frac{e^{-DB(\alpha-\gamma)}}{(\alpha-\gamma)(1-\gamma Db)}$$

$$+ P_{FA}\left\{1 - \left[\frac{\alpha D(h+b)+(\alpha Db)^2/2(\alpha Db-1)-1}{\alpha Db-1} - \frac{\gamma e^{D(\alpha-\gamma)(h+b)}}{(1-\gamma Db)(\alpha-\gamma)}\right]\right\} \tag{E.15}$$

where α,γ are two real roots of $S = e^{SDb}$, $\gamma < e < \alpha$, and $h \triangleq A-B$.

Eqs. (E.14) and (E.15) have a truncation error less than $10^{-(3+[A-B/b])}$, $[x]$ being the integer part of x. Hence (E.9) and (E.10) will be used if $[\frac{A-B}{b}] < N$, where N! is the largest real number which computer can handle, otherwise use (E.14) and (E.15).

On the other hand, $P_D \triangleq P_1(0)$ can be obtained through the two-step algorithm:

(1) Solve the transcendental equation

$$E[e^{-X\omega}] = 1 \tag{E.16}$$

(2) Substitute the nonzero root* ω_1 of (E.16) into

$$P_D = \frac{1-e^{\omega_1 B}}{e^{\omega_1 A} - e^{\omega_1 B}} \tag{E.17}$$

Finally, $\bar{T}_1 \triangleq E_1(0)$ is to be computed by the use of Wald identity:

*The existence and uniqueness of such a ω_1 was proved by Wald [5].

$$E_1(0) = E(X_t)/E(X_1). \tag{E.18}$$

E.2 Performance of $S_2(a,b,B_0,N_t)$

Let

$$S_{k,\ell} = \sum_{i=1}^{k} \hat{R}_{i\ell} \tag{E.19}$$

$$\hat{R}_{i\ell} = aR_{i\ell}^2 - b \qquad \text{if } S_{k-1,\ell} > B_0$$

$$= -\infty \qquad \text{otherwise} \tag{E.20}$$

where $a > 0$, $b > 0$, $B_0 < 0$ and $R_{i\ell}^2$ is defined in (B.1).

Test $S_2(a,b,B_0,N_t)$ is defined by the decision rule:

$$\begin{aligned} D_0&: \quad \text{if } S_{k,\ell} \leq B_0 \qquad \forall\ 1 \leq \ell \leq M \\ D_{1,m}&: \quad \text{if } S_{k,m} > B_0 \qquad \forall\ 1 \leq k \leq N_t, \\ &\quad \text{and } S_{N_t,m} = \max_{\ell}\{S_{N_t,\ell}\} \\ \overline{D}&: \quad \text{otherwise} \end{aligned} \tag{D.21}$$

where

$D_0 \triangleq$ accept $\hat{H}_0$ (see Appendix B), stop testing the present section and go to the next section.

$D_{1,m} \triangleq$ reject $\hat{H}_0$, go to the second stage test.

$\overline{D} \triangleq$ continue by taking another set of samples.

In other words, $S_2(a,b,B_0,N_t)$ is a modified version of the so-called variable dwell-time (VDT) system analyzed in [6], the modification being that D_0 is not made until all $S_{k,\ell}$ have crossed the boundary B_0 and $D_{1,m}$ is made at N_t-th noncoherent integrations by choosing the maximum one.

Conceivably, the improvement made by this test will not be so impressive as that by the VDS over the fix dwell-time system. This is evident from Table E.1 shown below. Other sequential procedures using CCD PNMF's are considered to be inferior to S_2 since each trajectroy $S_{k,\ell}$ is independent of one another, no conclusion as to the categorization ($\hat{H}_1$ or $\hat{H}_0$) of one trajectory can be drawn from the behavior of a group of different trajectories (or a single one).

Table E.1.

		Detection Probability	False-Alarm Probability	Mean Dwell-Time
Fix Dwell-Time (FDT)	M=1	P_D	P_{FA}	$\bar{T}_D$
	M=m	P_D	mP_{FA}	$\bar{T}_D$
VDT	M=1	P_D	P_{FA}	$\bar{T}_{D_V} < \bar{T}_D$
S_2	M=m	P_D	mP_{FA}	$< \bar{T}_{D_V}$

The mean dwell time can be computed by modifying Wald's approximation as described in [6], or, if an exact answer is preferable, use the recursive algorithm in [7].

Let n be the random stopping time at which D_0 is reached and $F(n|H_i)$ be the distribution function of n under H_i, given that M being equal to one. After obtaining $F(n|H_i)$ from [6] or [7], we set*

$$P_D \doteq [1-F(N_t|H_1)] \tag{E.22}$$

$$P_{FA} \doteq (M-1)[1-F(N_t|H_0)] \tag{E.23}$$

*Assuming $P_{FA} << P_D$.

$$E[n|H_0] = \sum_{n=1}^{N_t} n[F^M(n|H_0)-F^M(n-1|H_0)]. \qquad (E.24)$$

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APPENDIX F

DERIVATIONS OF THE MEAN ACQUISITION TIME ($\overline{T}_{ACQ}$) AND THE DISTRIBUTION FUNCTION OF THE ACQUISITION TIME

The mean acquisition time for the SPS algorithm is straightforward. After the initialization period which takes MT_c sec the acquisition process behaves like that of a two-dwell system with enlarged cells (bins). Hence

$$\overline{T}_{ACQ} = \tau_d + \left(\frac{1}{P_D} - \frac{1}{2}\right)(\tau_{D_1} + P_{FA_1}\tau_{D_2} + P_{FA}\cdot T_p T_c) N_d N_t \qquad \text{(F-1)}$$

where

$\tau_D = MT_c$,

$\tau_{D_1} = N\tau_D$ = dwell time for the first stage test,

τ_{D_2} = dwell time for the 2nd stage test,

$T_p T_c$ = penalty time,

$P_d = P_{D_1}\cdot P_{D_2}$,

$P_{FA} = P_{FA_1}\cdot P_{FA_2}$,

$N_d \cdot N_t$ = total number of bins in the uncertainty region

= (number of Doppler bins) $\cdot$ (number of time bins).

Eq. (F-1) is actually an upper bound only since $1 + C_0$ is not always equal to an integer multiple of M. In other words, one of the N_t time bins must have less than M cells. Thus $\tau_{D_1} N_d N_t$ can be reduced to $(1+C_0)NT_c$.

An exact analysis expression for $F(T_{ACQ})$ cannot be found. However, if $P_{FA_1} \ll 1$, $P_{FA_1}\tau_{D_2} \ll \tau_{D_1}$, then the distribution function for single-

dwell system derived by DiCarlo and Weber can be used as an upper bound.

For the SSP case,

$$\overline{T}_{ACQ} = \tau_D + \sum_{n=1}^{\infty} \sum_{k=1}^{n} [nT_A+(n-k)\overline{T}_p]\Pr\{\text{correct detection at the } n\text{-th try, } (n-k) \text{ false alarms}\}$$

$$= \sum_{n=1}^{\infty} \sum_{k=1}^{n} [nT_A+(n-k)\overline{T}_p](1-P_D-P_{FA})^{k-1}P_{FA}^{(n-k)}P_D$$

where

$$T_A = \tau_D + (C_{N_0}+1)NT_c + \tau_{D_2}, \qquad \overline{T}_c = \overline{\tau}_p T_c . \tag{F-2}$$

After simplification, we obtain

$$\overline{T}_{ACQ} = P_D^{-1}\left\{ \frac{T_A}{u-v}\left[\frac{u}{(1-u)^2} - \frac{v}{(1-v)^2} \right] - \frac{T_p}{u-v}\frac{u}{1-u} + \frac{T_p}{v}\frac{u}{1-u} \right\},$$

where

$u = P_{FA}$,

$v = 1 - P_D - P_{FA}$.

If $P_{FA} \ll P_D$, then

$$\overline{T}_{ACQ} \doteq \frac{T_A}{P_D} + \tau_D \tag{F-3}$$

which is eq. (4-5) in the main text.

The distribution, ignoring the very small probability mass affected by P_{FA}, is

$$F(T_{ACQ}) = \sum_{n=1}^{[\frac{T'_{ACQ}}{T_A}]} (1-P_D)^{n-1} P_D \ , \qquad \text{(F-4)}$$

where

$T'_{ACQ} = T_{ACQ} - \tau_D$,

$[x] \triangleq$ integer part of x.

(4-6) of the main text is then obtained by neglecting τ_D ($\ll T_A$).

APPENDIX G

AN ADAPTIVE PN ACQUISITION SYSTEM

The advantages of using CCD PN matched filters (PNMS) have been demonstrated in great detail [1]. It was shown that the presence of data modulation put a limit on the coherent integration period, M. According to Grieco [5] the expected data transition loss (DTL), L, is given by

$$L = \begin{cases} 1-M/4G_p & \text{(NRZ encoding)} \\ 1-3M/4G_p & \text{(Manchester encoding)} \end{cases} \qquad (1)$$

where

$$G_p = \frac{\text{code chip rate}}{\text{data rate}} > M \ .$$

Thus the TDRSS SSA service, having a large data rate operation range (0.1-300 Kb/sec), calls for an adaptive coherent integration length.

Using the SPS algorithm, PN code can be acquired within 2.6 seconds with a probability of .92 [1]. The design system parameters for the above data are as follows.

N_d (Doppler bin)	3
C_0+1 (cells per Doppler bin)	7600
δT_c (step size)	0.5
Sampling Loss (dB)	2.5
Doppler Loss (dB)	0.4

Data Transition Loss (dB)	0.2
Code Rate	3 Mchips/sec
M (chips)	512

From (1), a 0.2 dB data transition loss is resulted from a data rate of 1.05 Kb/sec.

The RCA TC 1235A CCD correlator designed by Munroe of Lincoln Laboratory [2] has a programmable length of 64, 128 and 256 (chips). Two such correlators in tandem will allow a programmable length of 64n, $1 \leq n \leq 8$. For a code rate of 3 Mchips/sec, we propose that the break points be at data rate = $3 \times 10^3/64n$ Kb/sec. In other words, the correspondence between data rates and coherent correlation lengths is as shown in the following table.

M (chips)	512	448	384	320	256	192	128	64
Data Rate* (Kb/sec)	5.9	6.7	7.8	9.4	11.7	15.7	23.4	50.0

*one channel

These break points allow at most one possible data transition during a coherent integration period and the resulting system performance will not be worse than the design point, i.e., 90% acquisition time $\leq$ 2.6 seconds. To show the latter claim, let us consider the worst case when the data transition occurs at the middle of a coherent integration period. Since the statistics under H_0 is not altered by the presence of

data modulation we shall consider only the detection probability. For the above worst case, there is at most a 3 dB loss if we assume equally likely ±1 data modulation. Because then, there is one data transition for every two periods and whenever there is a data transition at the middle of that period the test statistic produced at the end of that period will be no worse than zero which accounts for the 3 dB loss. Hence, for example, when M switches from 512 to 448 at 5.9 Kb/sec a 3 dB worst data transition loss plus a 0.58 dB processing gain loss can be well compensated by a 7.5 dB C/N_0 increase due to the data rate increase (from 1.05 K to 5.9K). With the same M, the DTL increase due to data rate increase can also be made up for by C/N_0 incrase; see eq. (1). Other cases can be checked similarly.

For data rate greater than 50 Kb/sec, we have to switch to 4-channel sequential detector which can be easily configured with devices borrowed from code tracking loop (a 2-channel double dither loop). Based on the numerical results presented in [3], we find, after necessary conversions, that the mean acquisition at 50 Kb/sec is less than 1.2 sec for the 4-channel sequential detector. The 90% acquisition time is expected to be less than 2.6 sec then. Two facts support the above estimation: (1) distribution of acquisition time for serial search algorithms can be well-approximated by that of a Gaussian random variable if $C_0 >> 1$ [4], (2) mean and variance of the acquisition time can be minimized by the same set of parameters [3].

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APPENDIX B

PN CODE TRACKING LOOP

B.1 Introduction

Code tracking is the second step of a two-step code synchronization procedure. It will be initialized right after code acquisition or coarse synchronization has been achieved to further reduce the code epoch offset between the received code and the incoming code and maintain this state for as long as possible.

Several different types of code tracking loops have been investigated in the literature, and two of them, namely, the delay-locked loop (DLL) [1-2] and the tau-dither loop (TDL) [3], are widely used and thoroughly analyzed. Both of these configurations can be operated in a coherent or noncoherent mode. For our application, PN acquisition and tracking must be performed prior to carrier synchronization, and hence noncoherent tracking is of interest.

One disadvantage of the DLL is the difficulty to maintain a close match between its two envelope detectors. Gain imbalance problem which results in tracking error can be eliminated by applying the TDL. On the other hand, the TDL suffers an approximate 3 dB loss in noise performance [3] due to the time-sharing of the early and late gates. Recently, Hopkins [4] proposed a new phase detector configuration called double-dither loop (DLL) which combines the desirable features of the DLL and TDL, i.e., the 3 dB dithering loss is recovered with no gain imbalance effects. By modifying Hopkins' DLL the AIRS'code tracking subsystem employs a 2-channel DLL (2-DDL) in order to:

- eliminate gain imbalance problem of the DLL

- pick up 3 dB dithering loss of the TDL
- utilize the weak (I) channel signal energy not used by the one-channel DDL.

B.2 Analytical Model and Timing Diagram for the 2-DDL

The 2-DDL is illustrated in Fig. B.1. I_E (I_L) and Q_E (Q_L) denote the advanced (delayed) versions of the local I and Q channel PN codes respectively. The timing diagram of the dithering signals, S_1 to S_8 is illustrated in Fig. B.2 where G_I and G_Q denote the I channel and Q channel gains. Notice that at any given time if the input signal r(t) is cross-correlated with advanced (early) and delayed (late) versions of the local I channel PN code in the upper channel then in the lower channel it is cross-correlated with those of the Q channel PN code and vice versa. The dithering gain signals, S_4, S_8 and sign signals, S_3, S_7 are designed in such a way that proper gain and sign are assigned to the outputs of envelope detectors and a proper control signal is formed at any time. Related system parameters and definitions are listed in Table B.1.

Following are assumptions made in the subsequent analysis of the 2-DDL:

(1) B_L (loop bandwidth) $<<$ $1/T_c$ (chip rate), i.e., code self noise can be neglected

(2) B_L $<<$ $1/T_b$ (bit rate) i.e., modulation self noise [ ] can be neglected

(3) $1/T_d$ (dithering rate) $<<$ $2/T_b$ ($\approx$ bandwidth of the BPF).

(4) Long PN code

(5) Zero code Doppler

(6) The time offset between early and late codes is one chip time.

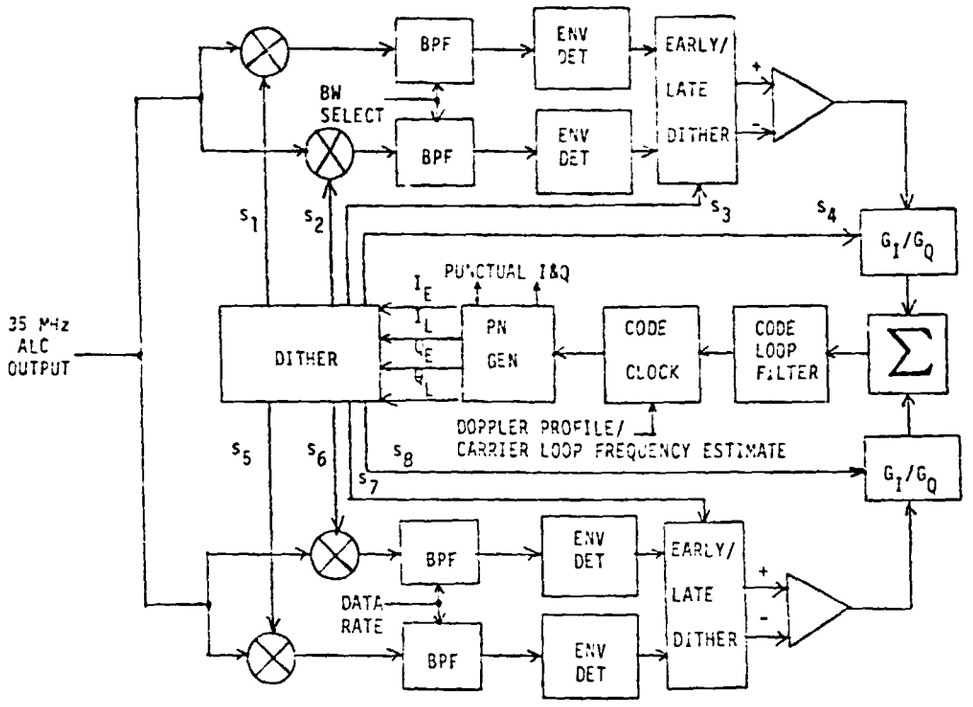

Fig. B.1. Analytical Model for the 2-Channel Double Dither Loop (2-DDL).

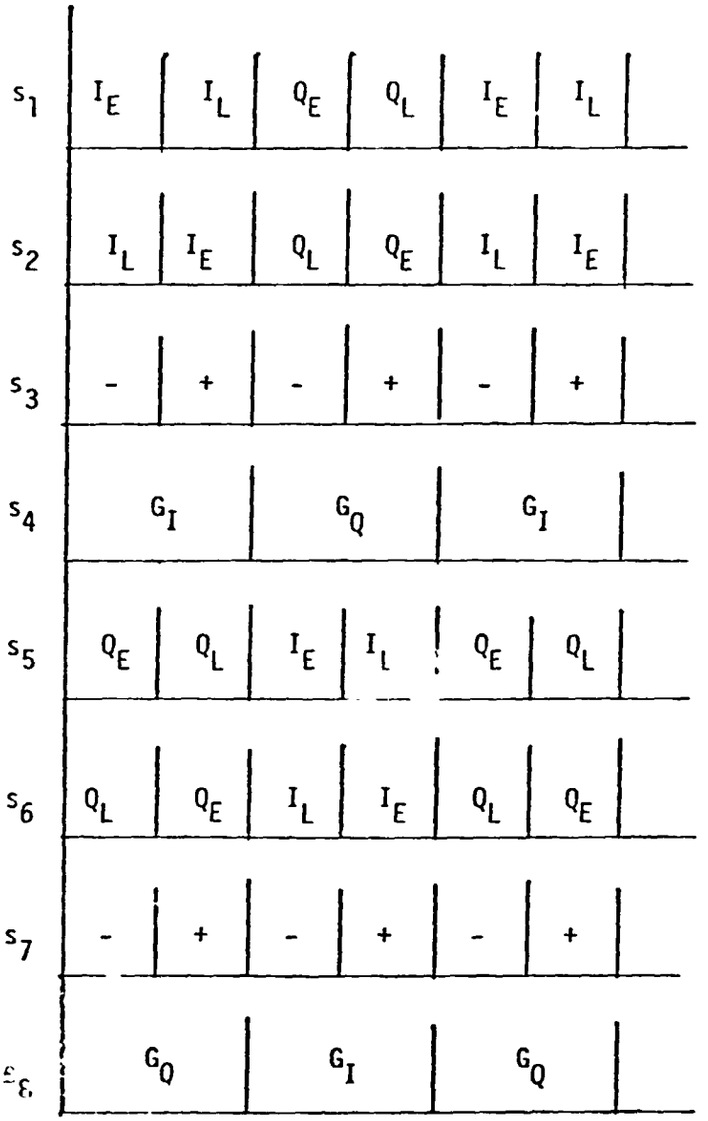

Fig. B.2. Timing Diagram for 2-DDL.

Table B.1. System Parameters and Definitions.

• CODE RATE	$1/T_c$
• DATA RATE	$1/T_b$ $(=R_b)$
• INPUT SIGNAL-TO-NOISE RATIO	$E_b/N_0 = ST_b/N_0$
• EARLY-LATE GATING	$\Delta = T_c/2$ (Half a Chip)
• LOOP BANDWIDTH	B_L
• Q:I POWER RATIO	G
• DITHERING RATE	$1/T_d$
• CORRELATION LOSS	C_L
• CODE PHASE JITTER	σ
• MEAN SLIP TIME	$\bar{T}_L$
• NORMALIZED MEAN SLIP TIME	$\log_{10}(2B_L\bar{T}_L)$

The 2-DDL of Fig. B.1 can be modeled as that shown in Figs. B.3 and B.4, given the above assumptions and following a similar argument of Hopkins [4]. The corresponding dither signals which select appropriate outputs sequentially are shown in Fig. B.5.

B.3 Code Phase Jitter Analysis

In Fig. B.4, W_i is the two-sided bandwidth of the bandpass filter of the i^{th} bandpass detector BPD_i) and B_i is that of the low pass filter of BPD_i. A correlator through which the received signal is cross-correlated with PN sequence $A_B, A_B \in \{I_E, I_L, Q_E, Q_L\}$, and four parallel G-again BPD's in cascade is called a A_B-G detector (Fig. B.4). Let us denote the signal and noise components of the output of BPD_i in a A_B-G detector as $G \cdot y_{A_B,i}$ and $G \cdot n_{A_B,i}$ respectively. Then it can be shown [4] that

$$y_{A_B,i} = k_i n_i (1+\rho_{A_B,i}) + \nu_i \qquad (B.1)$$

$$E(n_{A_B,i}) = 0 \qquad (B.2)$$

$$\sigma^2_{A_B,i} = Var(n_{A_B,i})$$

$$= k_i^2 n_i^2 \left(\frac{2B_i}{W_i}\right)(1+2\rho_{A_B,i}) \qquad (B.3)$$

where

all $n_{A_B,i}$ are independent of each other

k_i = gain constant of BPD_i

ν_i = dc offset of BPD_i

$n_i = N_0 W_i$

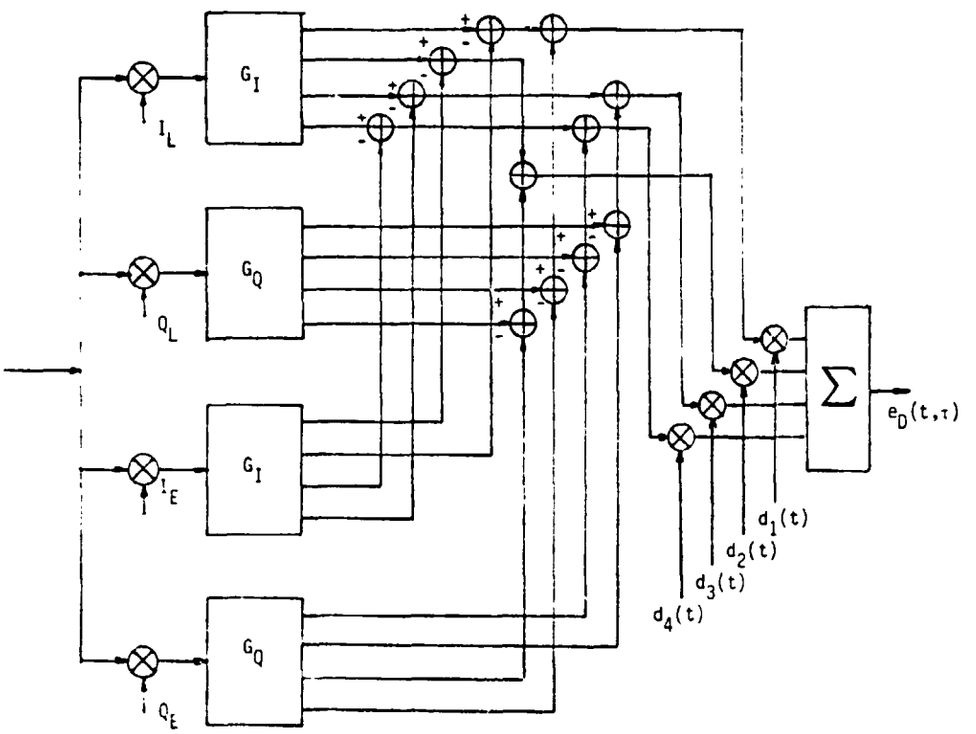

Fig. B.3. An Equivalent Analytic Model for the 2-DDL.

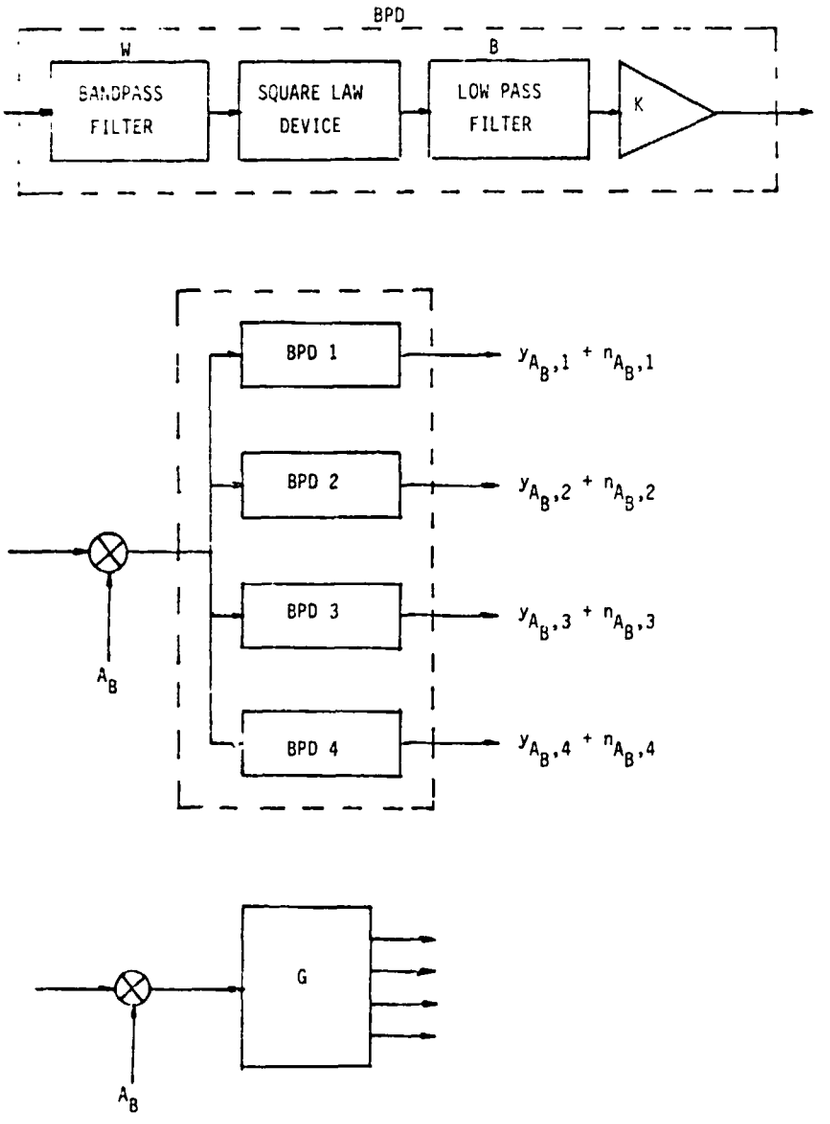

Fig. B.4. Analytical Model for an A_B-G Detector.

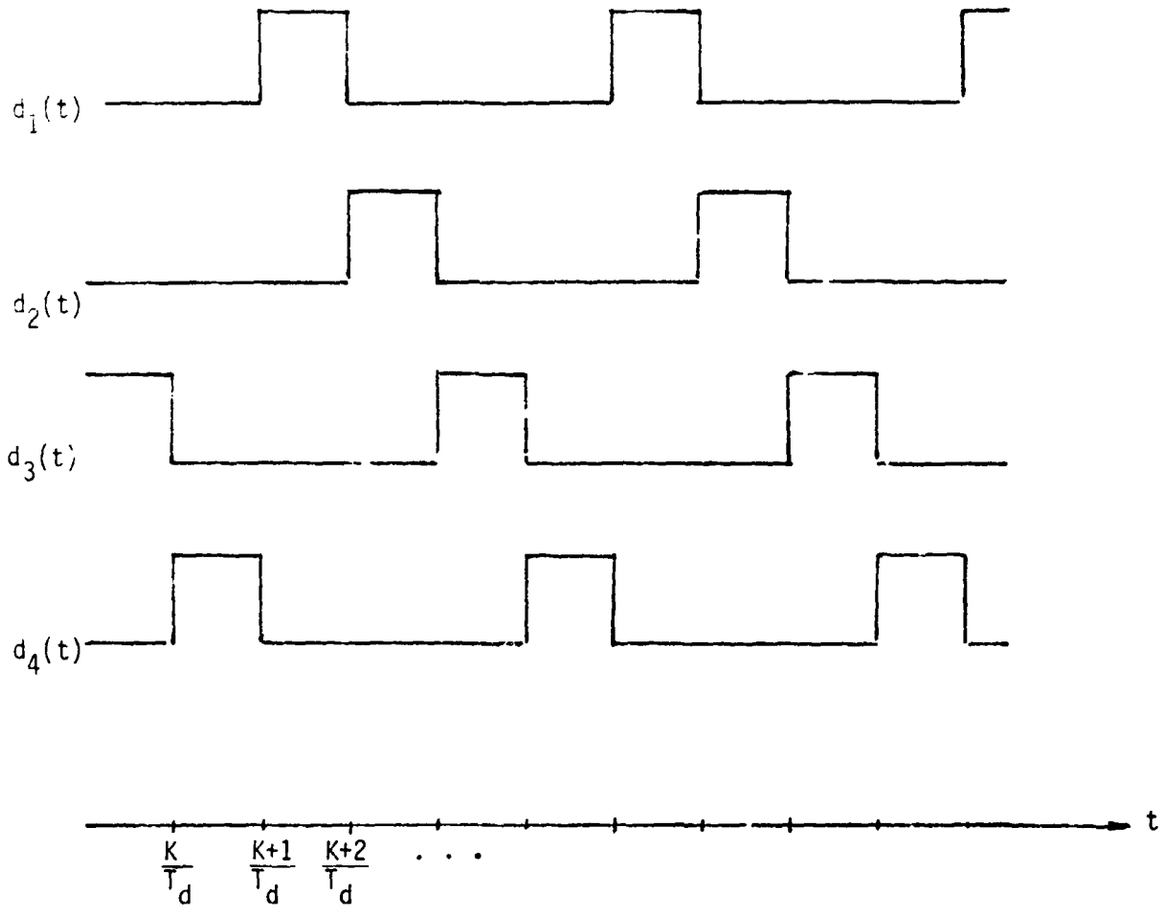

Fig. B .5. Timing Diagram for the Dithering Signals.

$$\rho_{A_B,i} = \frac{ST_i}{N_0} R_c^2(\tau + \frac{T_c}{2}) \text{ if } A_B = I_E \text{ or } Q_E$$

$$= \frac{ST_i}{N_0} R_c^2(\tau - \frac{T_c}{2}) \text{ if } A_B = I_L \text{ or } Q_L \qquad \text{(B.4)}$$

s is the total signal power

$T_i = 1/W_i$

and

$$R_c(\tau \pm \frac{T_c}{2}) = E[PN(t)PN(t+\tau \pm \frac{T_c}{2})] . \qquad \text{(B.5)}$$

The output of the 2-DLL phase detector, omitting time and delay arguments, is

$$\begin{aligned} e_D = {} & d_1\{G_I[y_{I_L,1} - y_{I_E,2}] + G_Q[y_{Q_I,3} - y_{Q_E,4}]\} \\ & + d_2\{G_I[y_{I_L,2} - y_{I_E,1}] + G_Q[y_{Q_L,4} - y_{Q_E,3}]\} \\ & + d_3\{G_I[y_{I_L,3} - y_{I_E,4}] + G_Q[y_{Q_L,1} - y_{Q_E,2}]\} \\ & + d_4\{G_I[y_{I_L,4} - y_{I_E,3}] + G_Q[y_{Q_L,2} - y_{Q_E,1}]\} + n(t) \end{aligned} \qquad \text{(B.6)}$$

where n(t) is the totality of all noise terms. The phase discriminator characteristic (PDC) is defined as the expectation of $e_D(t,\tau)$, which is denoted $D(\tau)$, i.e.,

$$D(\tau) = E(e_D) . \qquad \text{(B.7)}$$

By the independence of $\{n_{A_B,i}\}$, eq. (B.1), (B.2), (B.4), and the

equation $E(d_i) = 1/4$, we obtain

$$D(\tau) = \frac{S}{4}(k_1+k_2+k_3+k_4)(G_I+G_Q)[R_c^2(\tau - \frac{T_c}{2})-R_c^2(\tau + \frac{T_c}{2})] \quad . \quad (B.8)$$

average of the phase detector output is in proportion to the mean of all four gain constants.

The normalized PDC or normalized S-curve $g(\tau)$ is obtained

$$g(\tau) = \frac{D(\tau)}{D'(0)}$$

$$= 2[R_c^2(\tau - \frac{T_c}{2})-R_c^2(\tau + \frac{T_c}{2})] \qquad (B.9)$$

which is shown in Fig. B.6.

The variance of e_D can be derived from (B.1) to (B.4) and the identities:

$$E(d_i) = 1/4$$

$$E(d_i^2) = 1/4$$

$$E(n_{A_B,i}, n_{C_D,i}) = 0 \quad , \quad \text{if } A_B \neq C_D$$

$$\sigma^2_{I_E,i} = \sigma^2_{Q_E,i}$$

$$\sigma^2_{I_L,i} = \sigma^2_{Q_L,i}$$

It is found that

$$\mathrm{Var}(e_D) = \frac{(G_I^2+G_Q^2)}{4} \sum_{i=1}^{N} (\sigma^2_{I_E,i}+\sigma^2_{I_L,i})] - 3E^2(e_D) \qquad (B.10)$$

To assess the performance of the 2-DDL and to compare with other tracking loops, the following balanced conditions are assumed:

$$\nu_i = 0$$
$$k_i = k$$
$$W_i = W$$
$$B_i = B \text{ , for all } i$$
$$\tau = 0$$

Under these conditions $E(e_D) = 0$, all $\sigma^2_{I_E,i}$ and $\sigma^2_{I_L,i}$ are equal, $R_c(\tau - \frac{T_c}{2}) = R_c(\tau + \frac{T_c}{2}) = 1/2$, and (B.10) becomes

$$\mathrm{Var}(e_D) = 4k^2N_0^2BW(1 + \frac{S}{2N_0W})(G_I^2+G^2_Q) \qquad (B.11)$$

Normalizing $\mathrm{Var}(e_D)$ with respect to $D'(0)$ as in the case of $E(e_D)$ yields

$$\sigma_D^2 \triangleq \frac{\mathrm{Var}(e_D)}{[D'(0)]^2}$$
$$= \frac{(G_I^2+G_Q^2)}{(G_I+G_Q)^2} \mathrm{SNR}_0^{-1} [\frac{1}{2} + \mathrm{SNR}_I^{-1}] \qquad (B.12)$$

where

$$\mathrm{SNR}_I = \frac{S}{N_0W}$$

$$\mathrm{SNR}_0 = \frac{S}{N_0B}$$

Substituting $G = G_Q/G_I$ into (B.12) gives

$$\sigma_D^2 = \frac{1+G}{(1+G)^2} (SNR_0)^{-1} [\frac{1}{2} + \frac{1}{SNR_I}] \qquad (B.13)$$

It was shown [4] that the code phase jitter can be determined by replacing 2B with the equivalent noise bandwidth of the loop B_L, if $B_L < 2B$. Hence the normalized phase jitter is

$$\sigma_{2\text{-DDL}}^2 = \frac{1+G}{(1+G)^2} (SNR_L)^{-1} [\frac{1}{2} + (SNR_I)^{-1}] \qquad (B.14)$$

where

$$SNR_L = \frac{2S}{N_0 B_L} \qquad (B.15a)$$

and

$$SNR_I = \frac{S}{N_0 W} \qquad (B.15b)$$

For comparison, we list the normalized phase jitters for TDL and DDL below, assuming only the stronger channel signal is tracked.

$$\sigma_{TDL}^2 = (G \cdot SNR_L)^{-1} [.905 + (.453 - \frac{1}{5T_D W}) (G \cdot SNR_I)^{-1}] \qquad (B.16)$$

$$\sigma_{DDL}^2 = (G \cdot SNR_L)^{-1} [.5 + (G \cdot SNR_I)]^{-1}. \qquad (B.17)$$

When G = 1, it is noticed that

$$\sigma_{2\text{-DDL}}^2 = \frac{1}{2} \sigma_{DDL}^2 \approx \frac{1}{4} \sigma_{TDL}^2 .$$

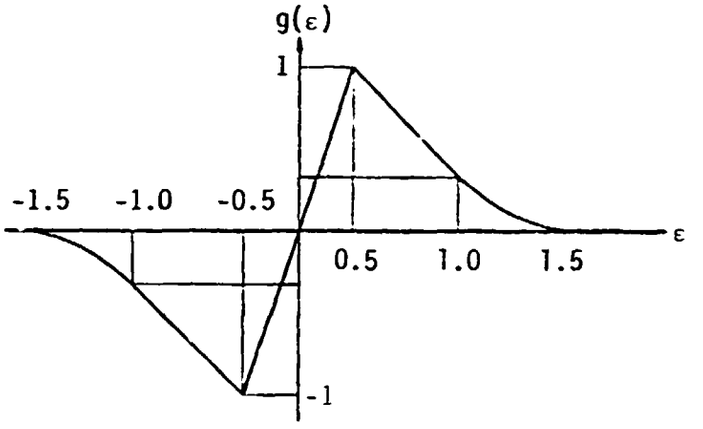

Fig. B.6. Normalized Phase Discriminator Characteristic (PDC) for 2-DDL.

For high input SNR, the improvement for the 2-DDL over TDL is about 3 dB in terms of required SNR. Fig. B.7 and Fig. B.8 show the normalized phase jitters for three different loops in low SNR and higher SNR environments respectively.

B.4 Mean Time to Lose Lock

Given an initial code offset τ_0, the time to lose lock T_L for a code tracking loop is defined as

$$T_L = \inf_{t>0} \{t: D(\tau)=0, \tau=\tau_0 \text{ at } t=0\} \qquad \text{(B.18a)}$$

The mean time to lose lock $\overline{T}_L$ is then given by

$$\overline{T}_L = E(T_L \mid \tau=\tau_0 \text{ at } t=0) \ . \qquad \text{(B.18b)}$$

Evaluation of $\overline{T}_L$ requires nonlinear analysis of the tracking system, and, for a first order loop, a general expression was obtained [5] in terms of a double integral for arbitrary phase detector configurations. In case $\tau_0=0$ and the phase detector is characterized by (B.9), the double integral can be simplified into a product of two single integrals [6]. Since $|\tau_0| < .25$ and in general τ_0 is close to zero for our system, it is appropriate for use to use the result of [6] as an approximation. The expression for $\overline{T}_L$ in this case is

$$\overline{T}_L = \frac{1}{4\sigma^2(2B_L)} \{\int_0^{3/2} e^{-[G(\varepsilon)/\sigma^2]} d\varepsilon\}\{\int_0^{3/2} e^{[G(\varepsilon')/\sigma^2]} d\varepsilon'\} \qquad \text{(B.19)}$$

where

$$G(\varepsilon) = \int^{\varepsilon} g(\tau)d\tau \ ,$$

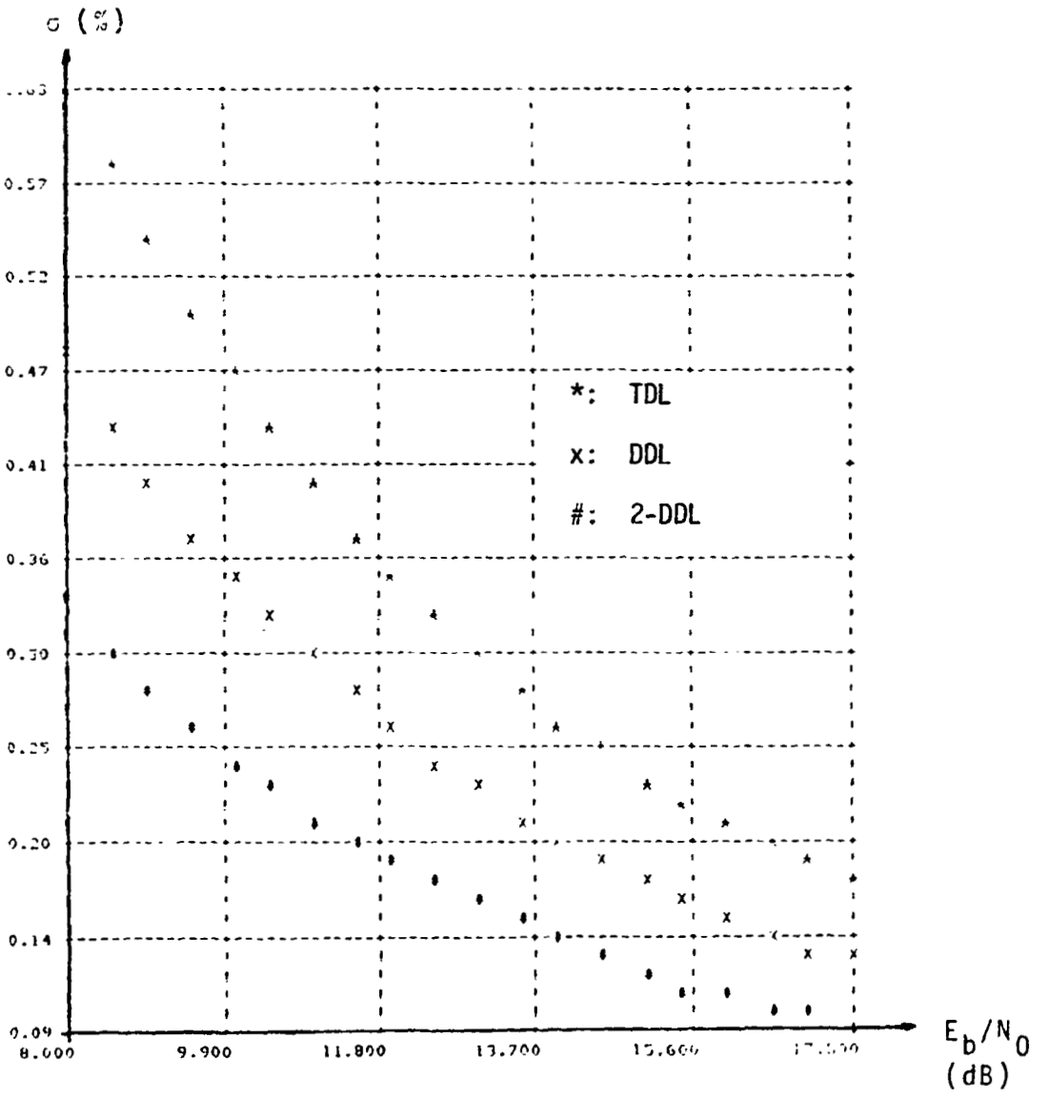

Fig. B.7. Code Phase Jitter for Various Loops; G=1.0, B_L=.5 Hz.

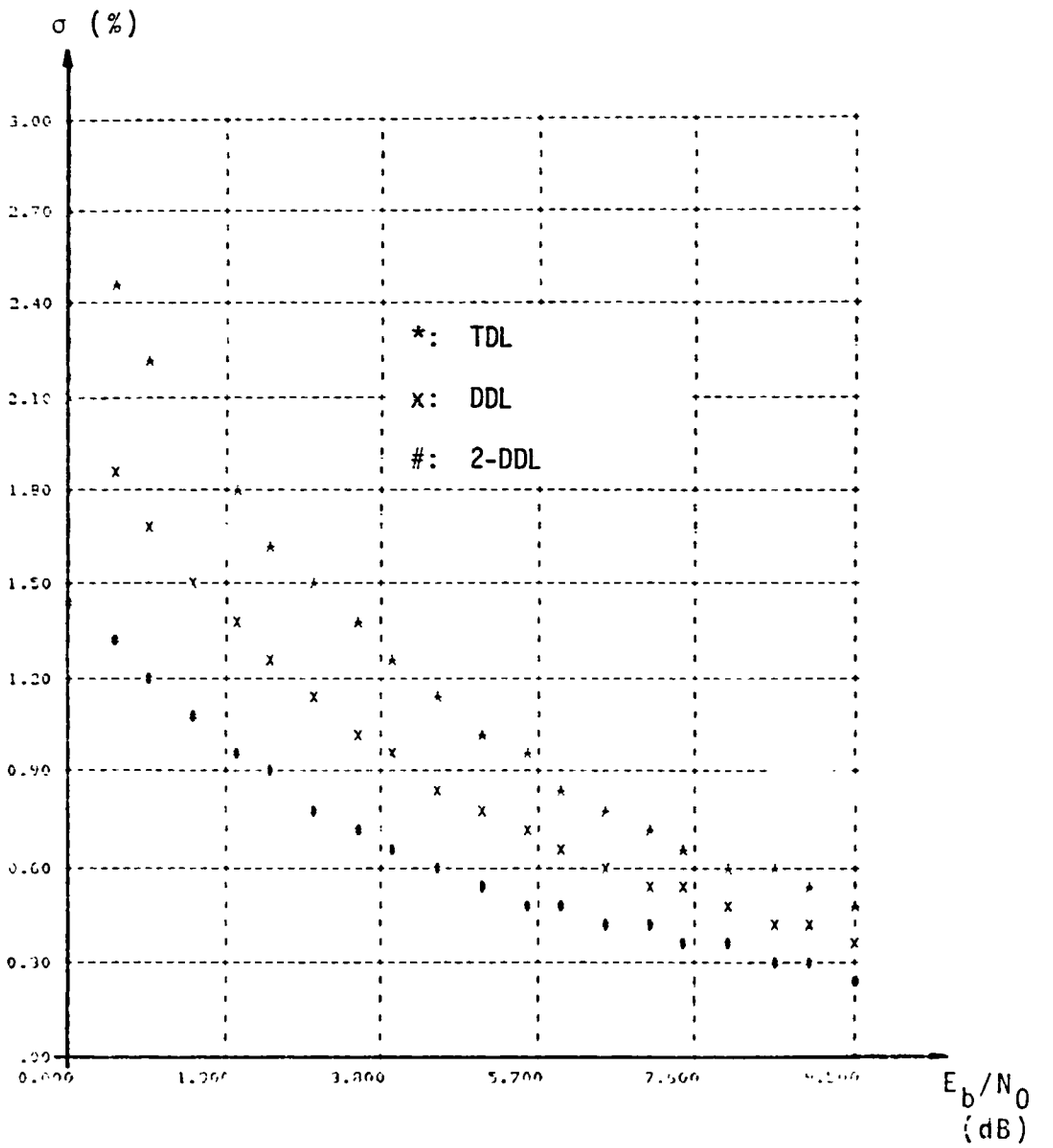

Fig. B.8. Code Phase Jitter for Various Loops; G=1, B_L=.5 Hz.

$g(\varepsilon)$ is the normalized phase discriminator characteristic (PDC) shown in Fig. B.6 and σ^2 is the code phase jitter. The value 3/2 is derived from the fact that the late and early version of the local PN code is offset by one chip time.

For an arbitrary initial condition τ_0, it can be shown that

$$\overline{T}_L\Big|_{\tau_0} = \overline{T}_L\Big|_{\tau_0=0} + \frac{1}{2\sigma^2}\int_{-3/2}^{3/2} e^{-G(\varepsilon)/\sigma^2}\int_0^{|\tau_0|} e^{G(\varepsilon')/\sigma^2} d\varepsilon' d\varepsilon \quad \text{(B.20)}$$

The normalized mean time to lose lock, $\log_{10}(2B_L\overline{T}_L)$, as a function of phase jitter σ is plotted in Fig. B.9 and B.10 for selected values of σ.

B.5 Pull-In Time and Lock Detector

B.5.1 Pull-In Time

The noiseless pull-in behaviors for various types of PDC have been studied by Spilker [1], Gill [2] and Nielson [7]. In the presence of noise, the pull-in time defined by

$$T_p = \inf_{t>0}\{t: |\tau| < \tau_p;\ \tau=\tau_0 \text{ at } t=0\} \quad \text{(B.21)}$$

is a random variable, and so it is only meaningful to look at the expectation of T_p:

$$\overline{T}_p = E(T_p \,|\, \tau=\tau_0 \text{ at } t=0)\ . \quad \text{(B.22)}$$

However, such an expectation does not exist because there is a nonzero probability that $T_p = \infty$. The reason is as follows.

The noise performance of the normalized code phase error $\varepsilon(t) \triangleq \frac{\tau(t)}{T_c}$ is governed by the differential equation:

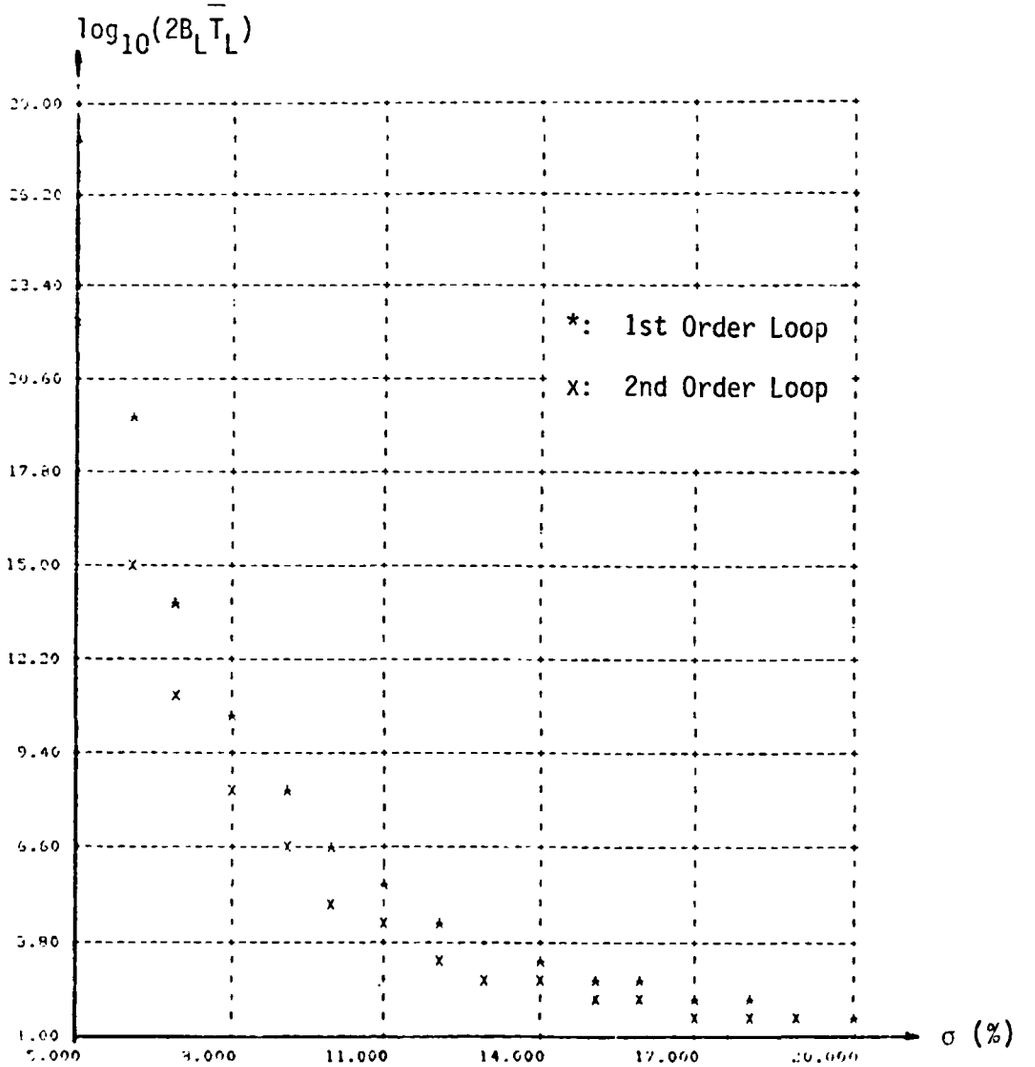

Fig. B.9. Normalized Mean Slip Time vs Phase Jitter.

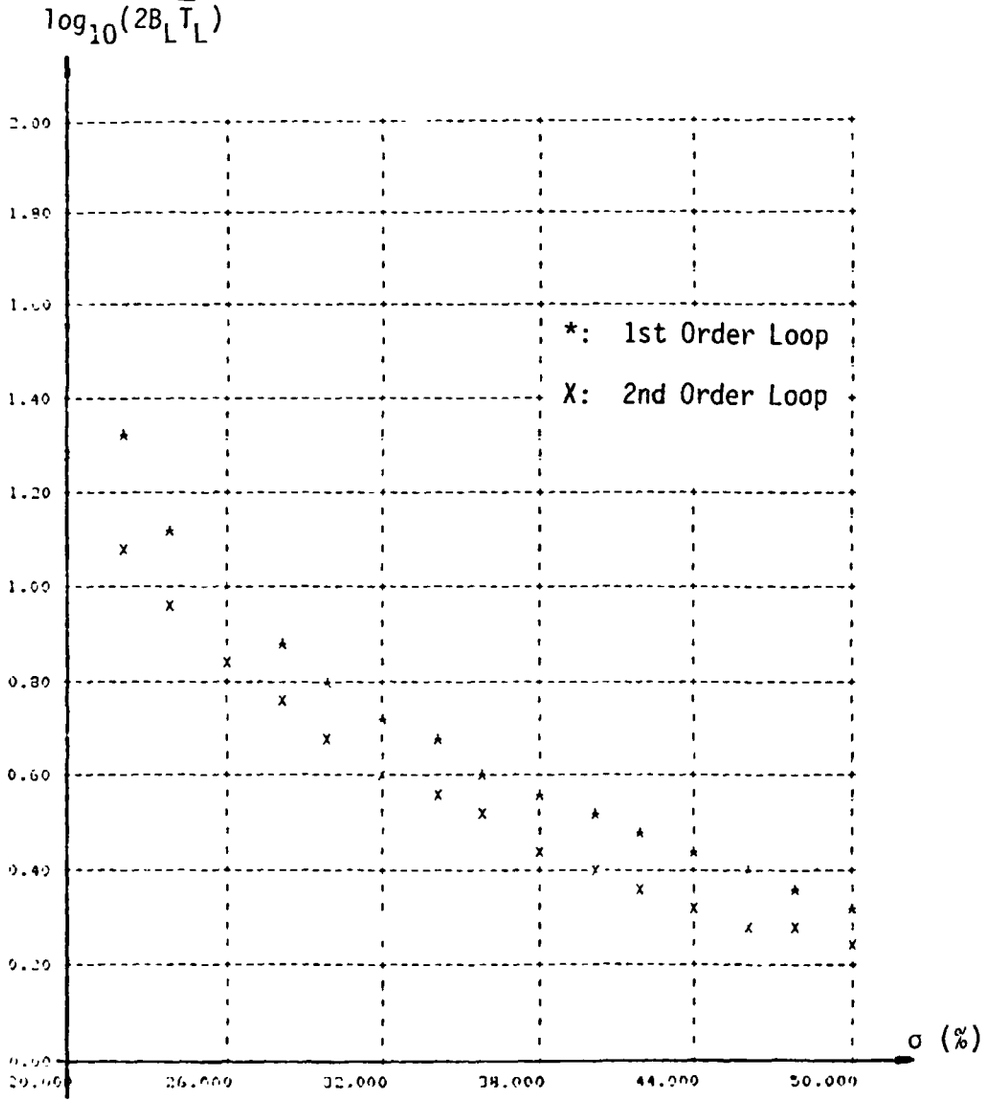

Fig. B.10. Normalized Mean Slip Time vs Phase Jitter.

$$d\varepsilon = -4B_L g(\varepsilon)dt + \sqrt{8B_L \sigma^2}\, dW_0 \qquad (B.23)$$

where $\int dW_0$ is a standard Wiener process and σ^2 is the phase jitter. In deriving (B.23), we have made the assumption that the noise component out of the phase detector, n(t) of (B.6), is white Gaussian noise.

For small ε, $g(\varepsilon) \approx \varepsilon$. Substituting $g(\varepsilon)$ by ε in (B.23) yields

$$d\varepsilon = -4B_L \varepsilon\, dt + \sqrt{8B_L \sigma^2}\, dW_0 \qquad (B.24)$$

which shows that $\{\varepsilon(t)\}$ is an Ornstein-Uhlenbeck (O-U) process The O-U process of (B.24) has a transition density function [8]

$$P(t,x,y) = \phi\left(\frac{\alpha_0^2}{2\alpha_0}\left(1-e^{-2\alpha_0 t}\right), x e^{-\alpha_0 t}, y\right) \qquad (B.25a)$$

where

$$\phi(t,x,y) = \frac{1}{\sqrt{2\pi t}} e^{-(y-x)^2/2t} \qquad (B.25b)$$

$$\alpha_0 = 4B_L$$

$$\sigma_0 = (8B_L)^{1/2}\sigma .$$

Eq. (B.25a) tells us that there is a nonzero probability from $\varepsilon = x = \tau_0$ to y = 3/2 even with a PDC $g(\varepsilon) = \varepsilon$. However we have to be reminded of the fact that at $\varepsilon = 3/2$, $g(\varepsilon) = 0$, and so there is a nonzero probability that ε will remain to be larger than 3/2 forever.

In order to assess the noise pull-in performance with a suitable criterion we neglect the probability that $|\varepsilon| > 1/2$ and apply the

approximation (B.24) for $\{\varepsilon(t),\ 0<t<T\}$, where T is a reasonably large number, say 10 seconds. That is, $\overline{T}_p$ is now defined by

$$\overline{T}_p = \int_0^T tP(t,x,y)dt \ . \qquad (B.26)$$

B.5.2 Lock Detector

The lock detector structure of the code tracking subsystem is shown in Fig. B.11 which is the same as that of a post-detection integrator used in the PN acquisition subsystem. The operation characteristic of such a detector has been derived in Sec. 2, which we now rewrite in eq. (B.27)

$$P_D = \operatorname{erfc}\left\{ \frac{\operatorname{erfc}^{-1}(P_{FA}) - 2\frac{E_c}{N_0}(1-|\varepsilon|)^2\sqrt{M}}{\sqrt{G_p\frac{E_c}{N_0}(1-|\varepsilon|)^2 + 1}} \right\} \qquad (B.27)$$

where P_{FA} = design false alarm probability

$$\frac{E_c}{N_0} = \frac{E_b}{N_0}\frac{T_c}{T_b} = \frac{E_b/N_0}{G_p}$$

$G_p = T_b/T_c \triangleq$ processing gain

M = integration time (chips) .

Eq. (B.27) is plotted in Fig. B.12 for $P_{FA} = 10^{-8}$, E_c/N_0 = -32 dB, $1/T_c$ = 3 M chips/sec and $\varepsilon = 1/4$. Note $P_D = .99$ can be achieved within .085 sec with the above specified worst case.

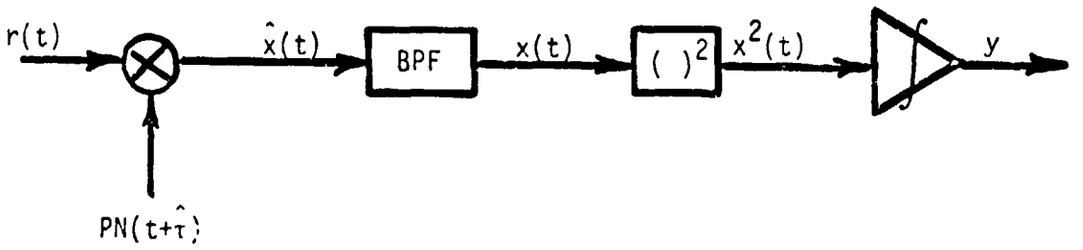

Fig. B.11. Lock Detector for the 2-DDL.

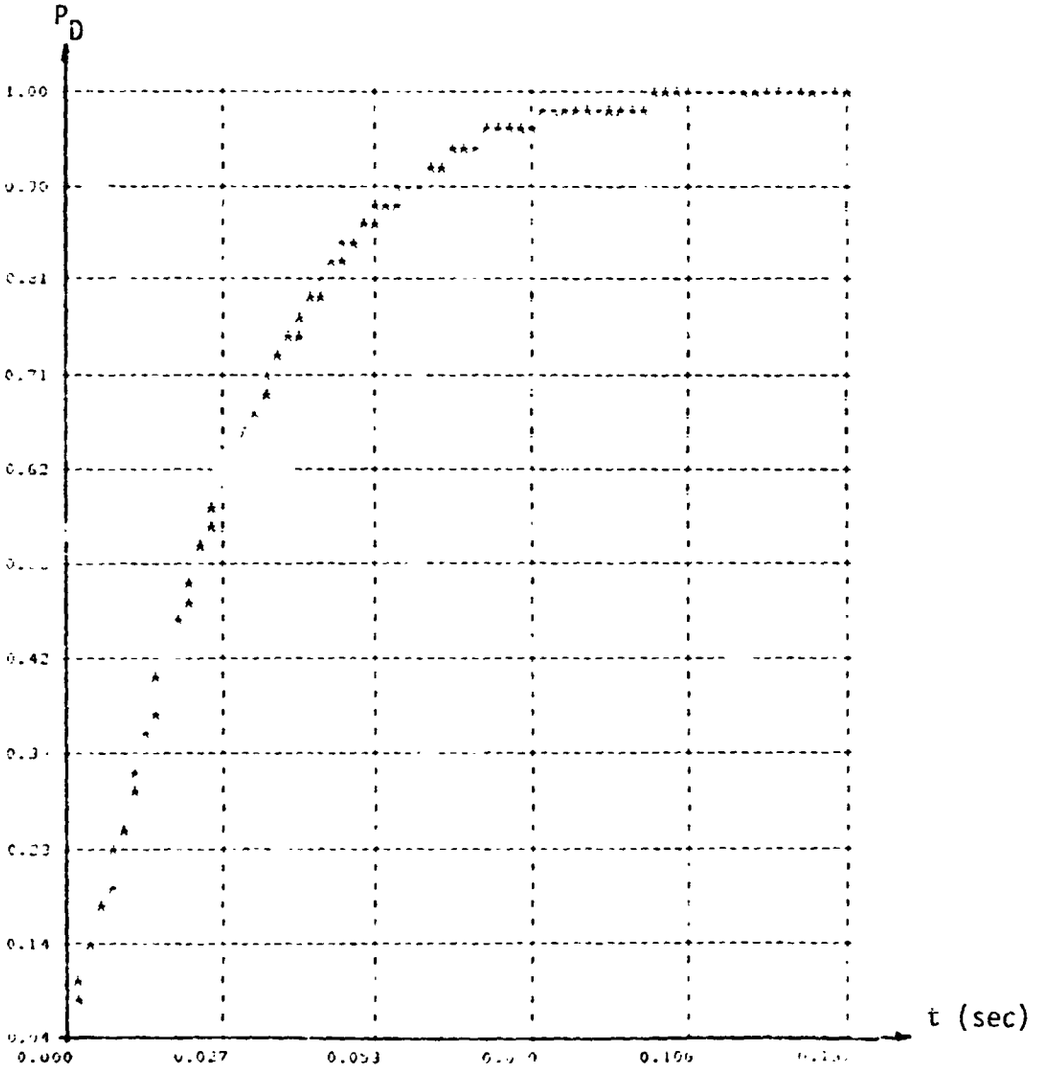

Fig. B.12. Detector Operation Characteristic for Lock Detector Shown in Fig. B.11.

B.6 Bandlimiting Effects of Pre-Despreading Filter and Bandpass Arm Filters

B.6.1 Correlation Loss Due to RF Filtering

The model under consideration is illustrated in Fig. B.13 where

$$r(t) = \sqrt{2S}\, PN(t-\tau)d(t)\cos(\omega_0 t+\phi) + n(t)$$

$$= \text{received waveform}$$

$H(\omega)$ = the transfer function of the RF bandpass filter which is centered at ω_0.

$\hat{r}(t) = \sqrt{2S}\, PN(t-\hat{\tau})\cos(\omega_0 t+\hat{\phi})$

= local estimate

$\tilde{r}(t)$ = the filtered version of $r(t)$.

Let the truncation function $\lceil T \rceil(t)$ be defined by

$$\lceil T \rceil(t) = \begin{cases} 1 & |t| < T \\ 0 & \text{otherwise} \end{cases}$$

and the cross correlation function between $\tilde{r}(t)\lceil T \rceil(t)$ and $\hat{r}(t)\lceil T_1 \rceil(t)$ by

$$R(\delta,\psi) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} E[\tilde{r}(t)\hat{r}(t)\lceil T \rceil(t)]dt$$

where

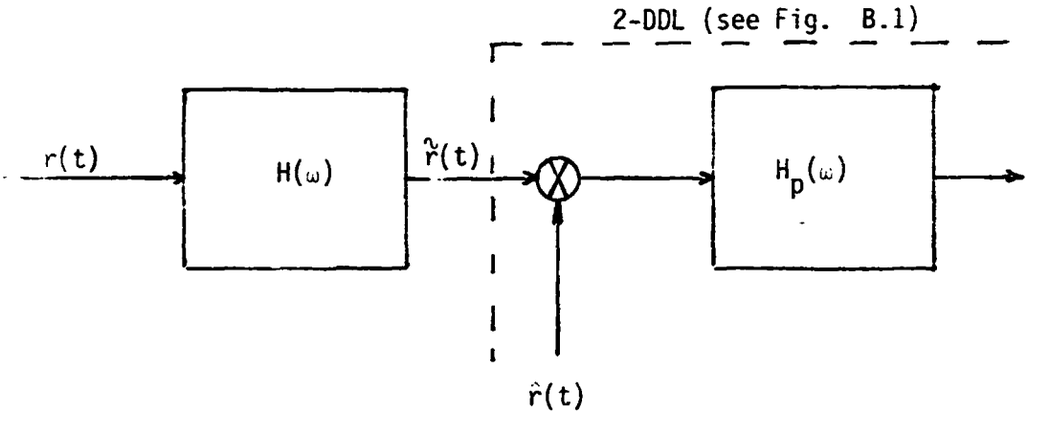

Fig. B.13. RF Predespreading Filter Model.

$$\delta = \tau - \hat{\tau}$$

$$\psi = \phi - \hat{\phi} .$$

Then it can be shown [10] that

$$R(0,0) = \frac{\sqrt{S}}{2\pi} \int_{-\pi\beta}^{\pi\beta} T_c \, \mathrm{sinc}^2(\omega T_c/2) d\omega$$

if

$$H(\omega-\omega_0) = \begin{cases} e^{-i\omega\alpha} , & |\omega| < \pi\beta \\ 0 , & \text{otherwise} \end{cases}$$

In case the $H(\omega-\omega_0)$ has a nonlinear phase $\phi(\omega)$ instead of constant phase α, then

$$R(0,0) \approx \frac{\sqrt{S}T_c}{2} \int_{-\pi\beta}^{\pi\beta} \mathrm{sinc}^2(\omega T_c/2) \cos \tilde{\alpha}\omega^3 d\omega$$

where

$$\tilde{\alpha} = \frac{1}{6} \frac{d^3\phi(\omega)}{d\omega^3} \bigg|_{\omega=0}$$

The number $R^2(0,0)$ corresponds to a signal energy degradation in the best case where $\delta = \psi = 0$ and hence is called correlation loss. This correlation loss, as a function of bandwidth-time product is depicted in Fig. B.14 for the case $\alpha = 0$. For further details see [9,10].

B.6.2 Bandlimiting Effect in Tracking Loops

The bandlimiting effect due to bandpass arm filters in the tracking loop is most easily accounted for by a signal energy degradation $\mathcal{D}$ defined as

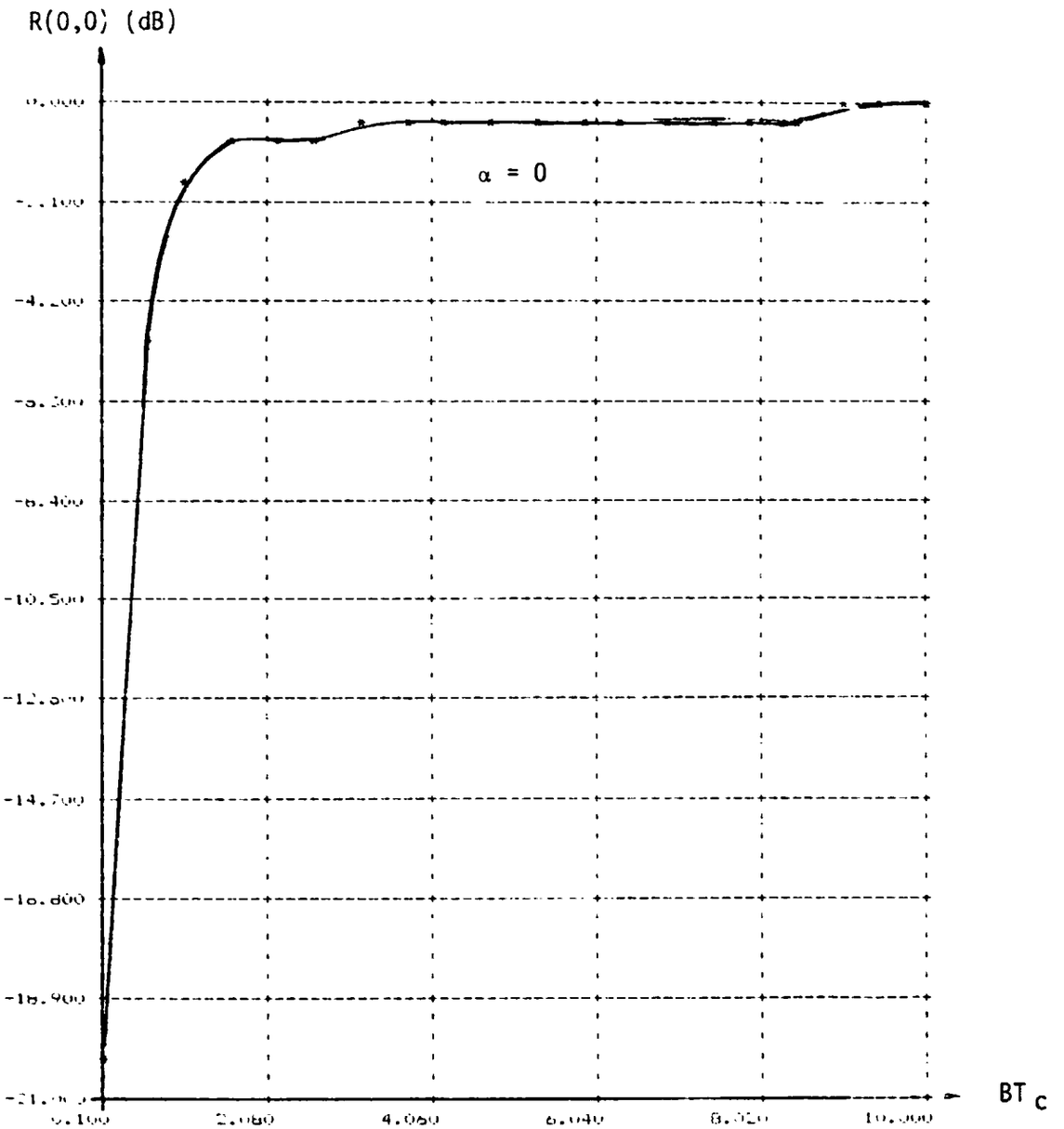

Fig. B.14. Correlation Loss Due to Prefiltering.

$$\sigma^2 = E[(\tilde{d}(t))^2]$$

where

$\tilde{d}(t)$ = filtered version of $d(t)$.

It was shown [6] that σ^2 can be expressed in the following way:

$$\sigma^2 = \frac{\int_{-\infty}^{\infty} S_d(f)|H_p(f)|^2 df}{\int_{-\infty}^{\infty} S_d(f) df}$$

$H_p(f)$ = the transfer function of the BPF

$S_d(f)$ = the spectral density of $d(t)$.

Simon [11] has examined the bandlimiting effects of the BPF for both DLL and TDL. For TDL, he found the optimal B_i/R_b, in the sense of minimizing jitter, lie between 2.5 and 3.0 for $0 \leq E_b/N_0 \leq 14$ (dB) and $B_i T_d = 4$.

As for the choice of T_d, Hartmann [3] suggested that $B_i/4 < 1/T_d < B_i/2$, since, as mentioned before, the dithering rate $1/T_d$ must be chosen small enough for the dithered signal to be passed by the IF BPF and, on the other hand, be large enough such that the sinusoidal component at $1/2T_d$ be out of the mainlobe of the loop filter.

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APPENDIX C

FREQUENCY ACQUISITION

C.1 Introduction

The implementation and performance of the frequency acquisition subsystem are described in this Appendix. Supporting software and its set up can be found in the next two appendices.

A carrier tracking loop does not acquire when the initial frequency error is comparable to the loop bandwidth. It is thus necessary to align the received and local carrier frequencies to within the loop bandwidth such that IF/or baseband process can take place. To avoid false lock in conventional frequency searching scheme and to make a rapid pull-in from a large initial frequency error possible we adopt a digital automatic frequency control (AFC) loop modified from Cahn's composite AFC/Costas loop [1]. The remainder of this appendix includes:

- Analytic model and description of the AFC loop
- Discriminator characteristics and pull-in range
- Simulation model
- Performance analysis
- Performance results
- Lock detector and its performance
- Modification for DG-1

C.2 Analytic Model and Description of the AFC Loop

The AFC loop or frequency acquisition loop (FAL) for the AMS has the configuration of Fig. C.1. The frequency synthesizer output is assumed to be of the form

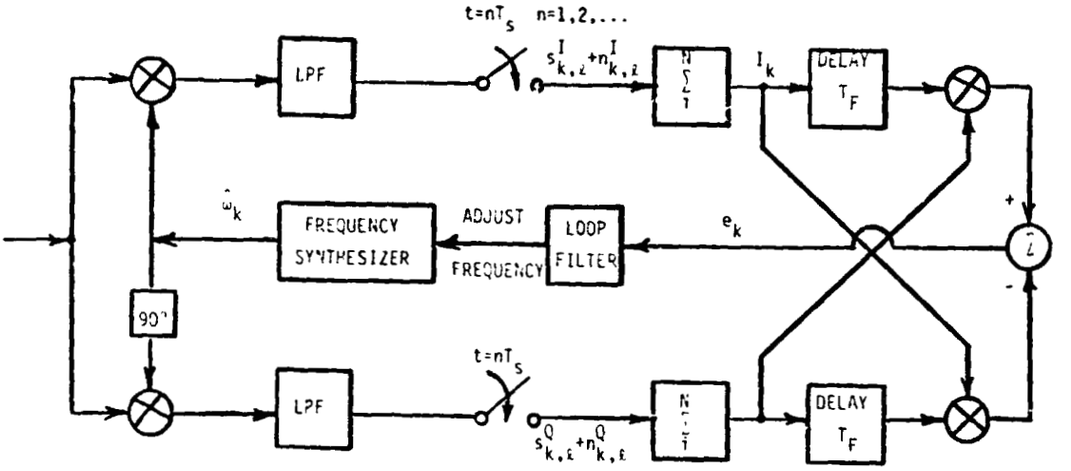

Fig. C.1. Frequency Acquisition Loop (FAL) Configuration.

$$\cos \omega_k \hat{t}.$$

The combination of mixer and low pass filter (LPF) serves as a frequency difference detector (FDD) which results in baseband outputs of

$$I(t) = d_I(t) \cos[\Delta\omega t+\phi(t)] - \sqrt{G}d_Q(t) \sin[\Delta\omega t+\phi(t)] + n_I(t) \quad (C.1a)$$

$$Q(t) = d_I(t)\sin[\Delta\omega t+\phi(t)] + \sqrt{G}d_Q(t)\cos[\Delta\omega t+\phi(t)] + n_Q(t), \quad (C.1b)$$

where $d_I(t)$, $d_Q(t)$ are the $\pm\sqrt{2S'}$ valued data stream, assuming filtered by the FDD without distortion, of I and Q channels respectively, S' is the I channel signal power, $\Delta\omega$ is the frequency difference between the received and local carrier, G is the Q:I power ratio, and $n_I(t)$,$n_Q(t)$ are independent narrow band Gaussian process with one-sided power spectral density N_0.

The sampling and summation combination is the digital realization of an integrate-and-dump (I/D) filter. The relationship among the sampling rate ($1/T_s$), the bit rate ($1/T_b$), the number of samples for each update (N) and the number of updates per bit time (M) can be summarized in the equation

$$\frac{1}{T_s} = \frac{MN}{T_b} \quad (C.2)$$

The control signal, e_k, which is proportional to frequency error is derived by

$$e_k = I_{k-1}Q_k - I_kQ_{k-1} \qquad (C.3)$$

where I_k, Q_k are the outputs of the digital I/D filters at time $t = kT_F = k(T_b/M)$. The control signal, after being filtered by the loop filter, will produce a signal to adjust the local frequency synthesizer.

C.3 Discriminator Characteristics and Pull-In Range

The generation of the control signal (C.3) is motivated by the fact that an unnormalized frequency discriminator can be formed by [2]

$$\dot{\theta} = I\frac{dQ}{dt} - Q\frac{dI}{dt} \qquad (C.4)$$

Approximating the time derivatives by finite differences over a time delay T_F, we have

$$\dot{\theta} = I(t-T_F)Q(t) - I(t)Q(t-T_F) \qquad (C.5)$$

For I(t),Q(t) the same as those in (C.1a) and (C.1b), ignoring noise and data modulation, we find

$$\dot{\theta} = 2(1+G)S' \sin(\Delta\omega T_F) \triangleq 2S[\sin(\Delta\omega T_F)]$$

Since the I/D filter has a transfer function as

$$H(\omega) = \text{sinc}\left(\frac{\omega T_F}{2}\right) \qquad (C.6)$$

where

$$\text{sinc}(x) = \frac{\sin x}{x} ,$$

it can be easily shown that the FAL discriminator characteristic (DC), which is defined as the mean of the control signal, is

$$D(\Delta\omega) = 2S \, \text{sinc}^2\left(\frac{\Delta\omega T_F}{2}\right) \sin(\Delta\omega T_F) . \qquad (C.7)$$

$D(\Delta\omega)$ will be normalized with respect to $D'(0)$ henceforth.

Eq. (C.7) is shown in Fig. C.2, from which we see that the DC is negligibly small when $\left|\frac{\Delta\omega T_F}{2\pi}\right| > 2.0$; see also Fig. C.6. The arrows on the curve indicate direction of frequency error variation with time in a noiseless environment. It is clear that the noiseless pull-in range is

$$\left|\Delta\omega T_F\right| < \pi$$

or (C.8)

$$\left|\Delta f T_F\right| < 1/2$$

where $\Delta f = \Delta\omega/2\pi$.

In the presence of thermal noise, the pull-in range is of course expected to be narrower and dependent on actual input signal to noise ratio (SNR_I). Fig. C.4, C.5, C.6 are three typical frequency error trajectories for $\Delta f T_F$ = .42, .525 and 1.05, respectively.

C.4 Simulation Model

According to the analytical block diagram shown in Fig. C.1 we set up the following simulation model for the AFC loop; the corresponding system parameters and their definitions are summarized in Table C.1.

$$I_k = \frac{1}{N} \sum_{\ell=1}^{N} (s^I_{k,\ell} + n^I_{k,\ell}) = \left(\frac{1}{N} \sum_{\ell=1}^{N} s^I_{k,\ell}\right) + n^I_k$$

$$\triangleq s^I_k + n^I_k \qquad (C.9a)$$

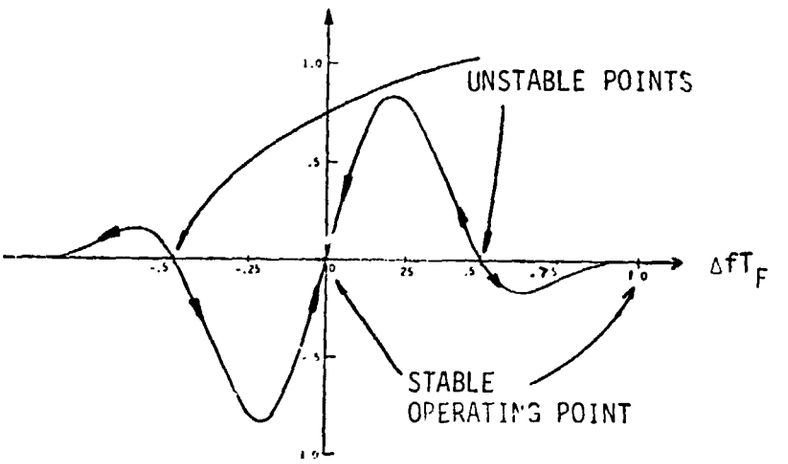

Fig. C.2. Phase Discriminator Characteristic for FAL ($D(\Delta fT_F)/D'(0)$).

Table C.1. FAL System Parameters and Definitions.

Bit Signal to Noise Ratio	$E_b/N_0 = ST_b/N_0$
Bit Rate	$1/T_b$ (R_b)
Q:I Power Ratio	G $(1 \leq G \leq 4)$
Sampling Rate	$1/T_s$
Loop Bandwidth	B_L
Accumulation Number for the I/D Filter	N
Update Speed	T_F (T_b/M)
Control Signal at $t = kT_F$	e_k
Output of the I/D Filter	I_k (I-channel)
at $t = kT_F$	Q_k (Q-channel)
Signal Component of $I_k(Q_k)$	$S^I_{k,\ell}$ $(S^Q_{k,\ell})$
at $t = (k-1)T_F+(\ell-1)T_s$	
Noise Component of $I_k(Q_k)$	$n^I_k(n^Q_k)$
Original Frequency (Phase) Offset	$\Delta\omega_0$ (θ_0)
Frequency Error at $t = kT_F$	$\Delta\omega_k$ (ϕ_k)

$$Q_k = \frac{1}{N}\sum_{\ell=1}^{N}(s^Q_{k,\ell}+n^Q_{k,\ell}) = (\frac{1}{N}\sum_{\ell=1}^{N} s^Q_{k,\ell}) + n^Q_k$$

$$\triangleq s^Q_k + n^Q_k \qquad \text{(C.9b)}$$

$$s^I_{k,\ell} = G_I d_{I_k}\cos[\phi_k+\Delta\omega_k(\ell-1)T_s]-G_Q d_{Q_k}\sin[\phi_k+\Delta\omega_k(\ell-1)T_s] \qquad \text{(C.10a)}$$

$$s^Q_{k,\ell} = G_I d_{I_k}\sin[\phi_k+\Delta\omega_k(\ell-1)T_s]+G_Q d_{Q_k}\cos[\phi_k+\Delta\omega_k(\ell-1)T_s] \qquad \text{(C.10b)}$$

where n^I_k, n^Q_k are i.i.d. Gaussian random variables with variance $N_0/(2sT_F)$, $G^*_I = 1/\sqrt{1+G}$ and $G^*_Q = \sqrt{G/1+G}$. The difference equations governing the control signal e_k, the local frequency and phase estimates $\hat{\omega}_k, \hat{\theta}_k$ and the state variables, I_k, θ_k and $\Delta\omega_k$, for a first order FAL are

$$e_k = I_{k-1}Q_k - I_kQ_{k-1} \qquad \text{(C.13)}$$

$$\hat{\omega}_{k+1} = \hat{\omega}_k + \gamma e_k \qquad \text{(C.14)}$$

$$\hat{\theta}_{k+1} = \hat{\theta}_k + \hat{\omega}_k T_F \qquad \text{(C.15)}$$

$$\Delta\omega_{k+1} = \Delta\omega_0 - \hat{\omega}_{k+1} \qquad \text{(C.16)}$$

$$\phi_{k+1} = \theta_{k+1} - \hat{\theta}_{k+1} \qquad \text{(C.17)}$$

$$\theta_{k+1} = \Delta\omega_0(k+1)T_F + \theta_0 \,. \qquad \text{(C.18)}$$

C.5 Performance Analysis

C.5.1 Frequency Jitter: Steady State Analysis

From (C.14) and (C.16), we obtain

*Note the G_I and G_Q defined here are square roots of those defined in Appendix B.

$$\Delta\omega_{k+1} = \Delta\omega_k - \gamma e_k$$

$$= \Delta\omega_k - \gamma E(e_k) - \gamma[e_k - E(e_k)] \qquad (C.19)$$

For BPSK signaling, (C.19) becomes

$$\Delta\omega_{k+1} = \Delta\omega_k - \gamma D(\Delta\omega_k) + \bar{n}_k \qquad (C.20)$$

where

$$\bar{n}_k = -\gamma[e_k - E(e_k)]$$

$$= -\gamma[(n^I_{k-1}n^Q_k - n^I_k n^Q_{k-1}) + (s^I_{k-1}n^Q_k + n^I_{k-1}s^Q_k - s^I_k n^Q_{k-1} - n^I_k s^Q_{k-1})]$$

$$= -\gamma[(\text{noise} \times \text{noise}) + (\text{signal} \times \text{noise})] \qquad (C.21)$$

Assuming $\Delta\omega_k T_F << 1$, i.e., $D(\Delta\omega_k) \approx \Delta\omega T_F$, we obtain

$$\Delta\omega_{k+1} = \Delta\omega_k(1-\gamma T_F) + \bar{n}_k.$$

Letting $a = 1-\gamma T_F < 1$, the above equation becomes

$$\Delta\omega_{k+1} = a\Delta\omega_k + \bar{n}_k \qquad (C.22)$$

Before we can proceed, a few observations and assumptions are needed. First, we notice that

$$E(\bar{n}_k) = 0 \qquad (C.23a)$$

$$\mathrm{Var}(\tilde{n}_k) = E(\tilde{n}_k^2) = 2\gamma^2\left[\left(\frac{N_0}{2sT_F}\right)^2 + \frac{N_0}{2sT_F}\right] \qquad \text{(C.23b)}$$

and

$$E(\tilde{n}_i\tilde{n}_j) = 0 \qquad \text{if } i \neq j \qquad \text{(C.23c)}$$

Hence $\{\tilde{n}_k\}$ is a sequence of uncorrelated and identical distributed random variables. Moreover, $\Delta\omega_k$ and $\tilde{n}_k$ are independent because of the independence between $\Delta\omega_0$, the initial frequency error, and $\tilde{n}_0$. Next, we observe that

$$E(\Delta\omega_k) = E(a^k\Delta\omega_0 + a^{k-1}\tilde{n}_0 + a^{k-2}\tilde{n}_1 + \ldots + \tilde{n}_{k-1})$$

$$= a^k\Delta\omega_0$$

and

$$E[(\Delta\omega_k)^2] = a^2E[(\Delta\omega_{k-1})^2] + 2aE(\Delta\omega_{k-1}\tilde{n}_{k-1}) + E(\tilde{n}_{k-1}^2)$$

$$= a^{2k}(\Delta\omega_0)^2 + E(\tilde{n}_{k-1}^2)\,\frac{1-a^{2k}}{1-a^2}\,.$$

The second equation has used two observations mentioned above, i.e.,

$$E(\Delta\omega_{k-1}\tilde{n}_{k-1}) = E(\Delta\omega_{k-1})E(\tilde{n}_{k-1}) = 0 \quad \forall K$$

and

$$E(\tilde{n}_1^2) = E(\tilde{n}_2^2) = \ldots = E(\tilde{n}_{k-1}^2)\,.$$

Now, if $K \gg 1$ such that $a^k \approx 0$ then

$$E(\Delta\omega_k) = 0,$$

$$E[(\Delta\omega_k)^2] = \frac{E(\tilde{n}_{k-1}^2)}{1-a^2}, \qquad \text{(C.24)}$$

and the autocorrelation function is found to be

$$E(\Delta\omega_i \Delta\omega_j) = a^{\ell} E(\Delta\omega_j^2)$$

$$= \frac{a^{\ell} E(\tilde{n}_{j-1}^2)}{1-a^2}, \qquad i = j+\ell. \qquad \text{(C.25)}$$

As has been expected, $\Delta\omega_k$ is asymptotically independent of $\Delta\omega_0$, and $\Delta\omega_i$ and $\Delta\omega_j$ are uncorrelated if $|i-j| = \ell \gg 1$. We shall establish (C.24) by another approach through which our simulation result on frequency jitter is to be justified. Let us form a new sequence $\{\Delta\omega_k'\}$ from the sequence $\{\Delta\omega_k\}$ by the sampling rule:

$$\Delta\omega_k' = \Delta\omega_i \qquad \text{(C.26)}$$

$$i = kj + k_0$$

where n and k_0 is such that

$E(\Delta\omega_i \Delta\omega_{i+j}) / \sqrt{E(\Delta\omega_i^2) E(\Delta\omega_{i+1}^2)} \approx 0$ and $a^{k_0} \approx 0$.

For analytical simplicity, we assume $\{\tilde{n}_k\}$ are Gaussian so that the uncorrelatedness of $\{\tilde{n}_k\}$ makes them i.i.d. The difference equation governing the new sequence $\{\Delta\omega_k'\}$ is similar to (C.22):

$$\Delta\omega_{k+1}' = a' \Delta\omega_k' + \tilde{n}_k' \qquad \text{(C.27)}$$

where $a' = a^j$ and

$$\tilde{n}'_k = a^{j-1}\tilde{n}_{kj} + a^{j-2}\tilde{n}_{kj-1} + \ldots + a\tilde{n}_{(k+1)j-2} + \tilde{n}_{(k+1)j-1}$$

It is clear that $\Delta\omega'_k$ and $\tilde{n}'_k$ are independent and $\tilde{n}'_k$ are i.i.d. Gaussian with mean zero and variance equal to $\frac{1-a'^2}{1-a^2}\,\mathrm{Var}(\tilde{n}_k)$. The uncorrelated sequence $\{\Delta\omega'_k\}$, being driven by a white Gaussian sequence, is itself white Gaussian. This and the choice of k_0 ($a^{k_0} \neq 0$) imply that $\{\Delta\omega'_k\}$ is a stationary white Gaussian process.

Since $\Delta\omega'_k$ has finite mean, by the strong ergodic theorem [3], the sample mean

$$\frac{1}{N}\sum_{K=i+1}^{N+i} \Delta\omega'_k \triangleq m_N \qquad \text{(C.28a)}$$

converges to the $E(\Delta\omega'_k)$ with probability one. Furthermore, if $\{\tilde{n}'_k\}$ is ergodic itself, then the sample variance

$$(N-1)^{-1}\left(\sum_{K=1}^{N} (\Delta\omega'_k)^2 - NM_N^2\right) \triangleq S_N \qquad \text{(C.28b)}$$

converges to $\mathrm{Var}[\Delta\omega'_k]$ with probability one [3]. In summary, if $\{\tilde{n}'_k\}$ is an ergodic, stationary, white Gaussian sequence then the sample mean and variance will converge to the assemble mean and variance with probability one. This will be our underlying assumption about $\{\tilde{n}'_k\}$ in the subsequent discussions. Summarizing $\Delta\omega'_k$ from 1 to N and dividing by N, we obtain, from (C.27),

$$\frac{1}{N}\sum_{K=1}^{N} \Delta\omega'_{k+1} = \frac{a'}{N}\sum_{K=1}^{N} \Delta\omega'_k + \frac{1}{N}\sum_{K=1}^{N} \tilde{n}'_k \,.$$

For N >> 1 and stationary $\{\Delta\omega'_k\}$,

$$\sum_{K=1}^{N} \Delta\omega'_{k+1} \approx \sum_{K=1}^{N} \Delta\omega'_k ,$$

hence

$$m_N(1-a) \approx \frac{1}{N} \sum_{K=1}^{N} \tilde{n}'_k . \qquad (C.29)$$

Now, substituting the identity

$$\sum_{K=1}^{N} \Delta\omega'^2_{k+1} = a'^2 \sum_{K=1}^{N} \Delta\omega'^2_k + 2a' \sum_{K=1}^{N} \Delta\omega'_k \tilde{n}'_k + \sum_{K=1}^{N} \tilde{n}'^2_k$$

and (C.29) into (C.28b), we find

$$(N-1)s_N \doteq (1-a'^2)^{-1}\left[\sum_{K=1}^{N} \tilde{n}'^2_k + 2a' \sum_{K=1}^{N} \Delta\omega'_k \tilde{n}'_k - \frac{1}{N(1-a')^2}\left(\sum_{K=1}^{N} \tilde{n}'_k\right)^2\right].$$

Denoting the frequency jitter by $\sigma^2_{\Delta F}$, we have

$$\sigma^2_{\Delta F} = \lim_{N\to\infty} \frac{s_N}{4\pi^2}$$

$$= \frac{1}{4\pi^2(1-a'^2)} \lim_{N\to\infty} \left[\frac{1}{N-1} \sum_{K=1}^{N} \tilde{n}'^2_k + \frac{2a'}{N-1} \sum_{K=1}^{N} \Delta\omega'_k \tilde{n}'_k - \frac{1}{(1-a')^2} \frac{\left(\sum \tilde{n}'_k\right)^2}{N(N-1)}\right]$$

By ergodicity, and independence of $\Delta\omega'_k$ and $\tilde{n}'_k$, it is easy to show that

$$\lim_{N\to\infty} \frac{1}{N-1} \sum_{K=1}^{N} \tilde{n}'^2_k = \mathrm{Var}(\tilde{n}'_k)$$

$$\lim_{N\to\infty} \frac{\left(\sum \tilde{n}'_k\right)^2}{N(N-1)} = \lim_{N\to\infty} \frac{N-1}{N} \left(\frac{\sum \tilde{n}'_k}{N}\right)^2 = 0$$

$$\lim_{N\to\infty} \frac{\sum \Delta\omega_k' \tilde{n}_k'}{N-1} = 0$$

and so

$$\sigma_{\Delta F}^2 = \frac{\mathrm{Var}(\tilde{n}_k')}{4\pi^2(1-a'^2)} \qquad \text{(C.30a)}$$

$$= \frac{\mathrm{Var}(\tilde{n}_k)}{4\pi^2(1-a^2)}$$

$$= \frac{\gamma^2}{4\pi^2(2\gamma T_F - \gamma^2 T_F^2)} \left[\frac{1}{2(\mathrm{SNR}_I)^2} + \frac{1}{\mathrm{SNR}_I} \right]$$

$$= \frac{\gamma}{4\pi^2 T_F(2-\gamma T_F)} \left[.5(\mathrm{SNR}_I^{-2}) + \mathrm{SNR}_I^{-1} \right]$$

where

$$\mathrm{SNR}_I \triangleq \frac{ST_F}{N_0} \ , \qquad \text{(C.30b)}$$

$$B_F \triangleq 1/T_F \ .$$

If $\gamma T_F \ll 1$ then

$$\sigma_{\Delta F}^2 = \frac{\gamma B_F}{8\pi^2} \left[\frac{1}{\mathrm{SNR}_I} + \frac{1}{2(\mathrm{SNR}_I)^2} \right] \qquad \text{(C.31)}$$

From the simulation efficiency viewpoint, however, (C.26) is not a good sequence to work with, especially when $a \approx 1$, i.e., $B_L T_F \ll 1$. We

would rather use the sequence $\{D_k\}$ given by

$$D_k = \Delta\omega_i - a\Delta\omega_{i-1} = n_{i-1}$$

$$i = k + K_0, \quad k \geq 1$$

It can be easily proved that

$$E(D_i D_j) = 0 \quad \text{if } i \neq j$$

and

$$E(D_i^2) = E(\tilde{n}_{i+k_0}^2) = Var(\tilde{n}_{i+k_0}) .$$

Hence $\sigma_{\Delta F}^2$ can be obtained by first computing the sample variance of the white Gaussian sequence $\{D_k\}$ and then dividing it by $4\pi^2(1-a^2)$. For other modulation format, $\sigma_{\Delta F}^2$ can be derived accordingly by substituting the corresponding $D(\Delta\omega_k)$ and $Var(\tilde{n}_k)$ into (C.28). We have found, however, that they are all equal except for SPQSK which renders

$$\sigma_{\Delta F}^2 = \frac{\gamma B_F}{8\pi^2} \left[\frac{1}{\alpha_1 (SNR_I)} + \frac{1}{2(\alpha_2 SNR_I)^2} \right] \qquad (C.32)$$

where α_1 and α_2 are functions of $M(=T_f/T_b)$ and $N(=T_s/T_F)$. When both M and N are large, say ≥ 10, then $\alpha_1 \approx \alpha_2 \approx 1$.

So far, we have assumed a NRZ signal format and ignored the data transition loss caused by a reverse of the control signal at the bit junction whenever a data transition occurred. It can be shown that the average loss for a BPSK/NRZ signal is .75/M and $3(1+G^2)/16M$ for UQPSK/NRZ. Because the Manchester coding guarantees a sign transition

during a bit time the average loss for BPSK is 3/2M and and $3(1+2G^2)/8M$ for UQPSK. It is the consideration of such a data transition loss whence a median (≥ 5) or large M requirement is derived. A more accurate estimation of $\sigma^2_{\Delta F}$ should replace SNR_I defined in (C.28b) by $SNR_I' \triangleq D_0 SNR_I$, where D_0 is the data transition loss described above.

C.5.2 Acquisition Time: Transient State Analysis

C.5.2.1 Noiseless Behavior

The noiseless acquisition time, T_{AQF}, is defined here as

$$T_{AQF} = \inf_{t>0} \{t: \Delta\omega_t = 0\} , \qquad (C.33)$$

i.e., the first time the frequency error becomes zero.

There will be no attempt to address the nonlinear FAL analysis here. Throughout this subsection discussions are restricted to the linear operating region of a FAL, that is, $\Delta\omega_0$ is always assumed to be such that $\Delta\omega_0 T_F < 1/6$. In this region, the continuous-time version of the FAL shown in C.1 can be equivalently modeled as that illustrated in Fig. C.3. For a first order loop,

$$F(s) = \frac{1}{sT_I} .$$

Hence the closed-loop transfer function becomes

$$H(s) = \frac{K_r K_0 F(s)}{1+K_r K_0 F(s)}$$

$$= \frac{1}{1+(T_I/K_r K_0)s} \qquad (C.34a)$$

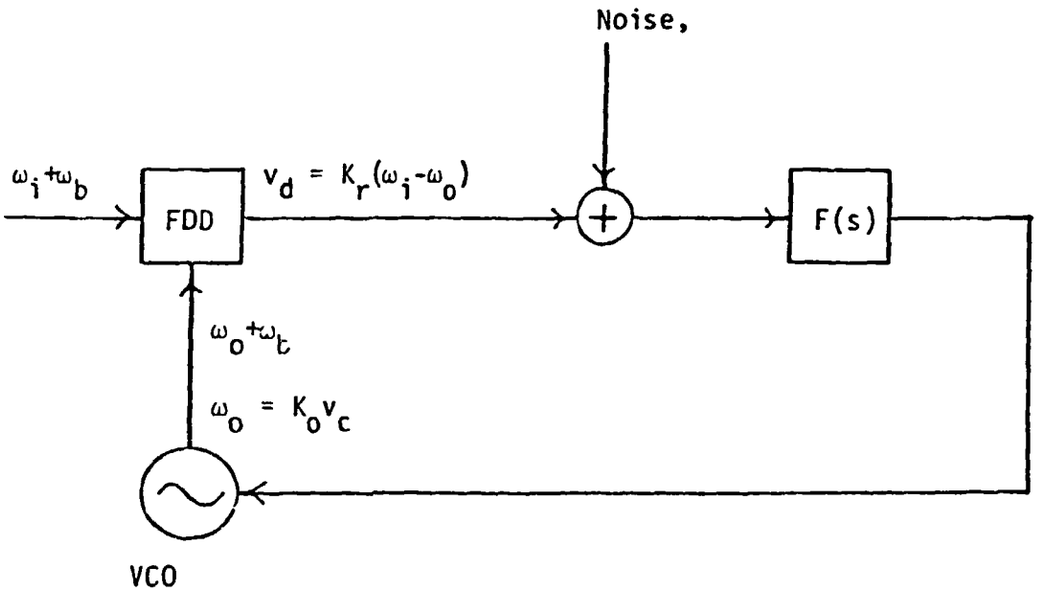

Fig. C.3. An Equivalent Continuous-Time Model for the FAL of Fig. .1.

Compared with (C.22), we obtain

$$T_I = 1$$

$$K_r = a$$

and

$$K_0 = \gamma .$$

Defining the loop time constant as

$$T_L = T_I/K_r K_0 = 1/a\gamma \qquad \text{(C.34b)}$$

and taking the inverse Laplace Transform of (C.34a), we obtain

$$\Delta\omega_t \triangleq \mathcal{L}^{-1}(H(s)) = \Delta\omega_0 e^{-t/T_L} \qquad \text{(C.35)}$$

Therefore T_{AQF} can be estimated via

$$t = T_L \ln \frac{\Delta\omega_0}{\Delta\omega_t} \qquad \text{(C.36)}$$

so long as $\Delta\omega_0 \cdot \Delta\omega_t > 0$.

C.5.2.2 Noise Performance

Eq. (C.33) is used to define the so-called noiseless acquisition time because the behavior of $\{\Delta\omega_k, k=0,1,\ldots\}$ in a noiseless environment, being well-approximated by the deterministic equation, (C.35), of its continuous-time version, is a deterministic and decreasing function of k. As a noise performance measure, (C.35) is of course not appropriate any more, due to frequency jitter. Hence, we define the δ-P frequency acquisition time as

$$T_{AQF}(\delta,P) = \inf_{t>0} \{|\Delta\omega_t| < \delta \text{ with probability } P\} \qquad (C.37a)$$

Usually, $\delta << \Delta\omega_0$ and δT_F is in the linear region of $D(\Delta\omega)$, so Gaussian assumption is valid and (C.40a) is equivalent to

$$T_{AQF}(\delta,P) = \inf_{t>0} \{|\Delta f_t| < \delta,\ \text{erfc}(\frac{\delta}{\sigma_{\Delta F}}) < \frac{1-P}{2}\} \qquad (C.37b)$$

Even with the assumption of 100% acquisition probability, $T_{AQF}(\delta,P)$ does not necessarily exit, due to the fact that the inequality

$$\text{erfc}(\frac{\delta}{\sigma_{\Delta F}}) < \frac{1-P}{2} \qquad (C.38)$$

cannot always be satisfied. A more feasible performance measure is the mean acquisition time, $\overline{T}_{AQF} = E[T_{AQF}(\delta,P)]$, given (C.38) and 100% acquisition probability. An approximation of $\overline{T}_{AQF}$ is dericed as follows.

In the presence of noise, we have

$$d(\Delta\omega_t) = -\gamma D(\Delta\omega_t)dt + \gamma\, \tilde{n}(t)dt\ ,$$

and in the linear region of $D(\Delta\omega_t)$ it becomes

$$d(\Delta\omega_t) = -\gamma T_F \Delta\omega_t dt + \gamma\, \tilde{n}(t)dt$$

where

$$\Delta\omega_t\Big|_{t=kT_F} = \Delta\omega_k$$

and

$$\tilde{n}(t)\Big|_{t=kT_F} = \tilde{n}_k \gamma^{-1}$$

If we assume $\tilde{n}(t)$ is an additive white Gaussian noise with a one-sided power spectral density $\tilde{N}_0$, where

$$\tilde{N}_0 = \frac{2\mathrm{Var}(\tilde{n}_k)}{\gamma^2 B_F} = 4T_F\left[\left(\frac{N_0}{2s\tilde{T}_F}\right)^2 + \frac{N_0}{2sT_F}\right]$$

then $\{\Delta\omega_t, t>0\}$ becomes the well-known Ornstein-Uhlenbeck process [4] which is also an approximation used to compute the mean pull-in time for the PN code tracking loop discussed in Section Y. The mean acquisition time, assuming a 100% pull-in probability, is thus to be evaluated by

$$\bar{T}_{AQF} = \int_0^{\infty} tP(t,\Delta\omega_0,0)dt \approx \int_0^{T} tP(t,\Delta\omega_0,0)dt \qquad (C.39)$$

where

T is a large number

$$P(t,\Delta\omega_0,y) = \phi\left(\frac{\sigma^2}{2\alpha}(1-e^{-2\alpha t}), \Delta\omega_0 e^{-\alpha t}, y\right),$$

$$\phi(t,x,y) = \frac{1}{\sqrt{2\pi t}} e^{-(y-x)^2/2t},$$

$$\sigma = \gamma\sqrt{\frac{\tilde{N}_0}{2}},$$

and

$$\alpha = \gamma T_F .$$

Eq. (C.39) is in fact a conditional mean only. The 'real' $\bar{T}_{AQF}$ does not

exist, followed by a similar argument given in Sec. C.5.1. In case of SQPSK, $\tilde{N}_0$ is replaced by

$$\tilde{N}_0 = 2T_F \left[\frac{1}{\alpha_1(SNR_i)} + \frac{1}{2(\alpha_2 SNR_I)^2} \right] . \qquad (C.40)$$

This complete our linear analysis of the FAL for DG2.

C.6 Performance Results

C.6.1 Simulation and The etical Predition

Judging from (C.29), frequency jitter is controlled by the triple (γ, B_F, SNR_I) or equivalently by $(B_L, T_F, E_b/N_0, M)$ since

$$\gamma = 4B_L ,$$
$$B_F = 1/T_F , \qquad (C.41)$$
$$SNR_I = \frac{ST_b}{N_0}\frac{T_F}{T_b} = \frac{E_b}{N_0}\left(\frac{1}{M}\right) . \qquad (C.42)$$

The above fact suggests that a small B_L and a large T_F (small M) be used. On the other hand, a larger T_F implies a smaller pull-in range and a small B_L will delay the acquisition time; see eq. (C.8) and (C.35). One solution to this dilemma is to apply a multiple-stage strategy. More specifically, (B_L, T_F) will not remain constant but will vary with time, of course, we would like to have a large B_L and small T_F initially, and B_L (T_F) be switched to smaller (larger) values at some predetermined time. Such a multiple loop bandwidth and update speed system allows us to enjoy the advantages of both fast pull-in time and small frequency jitter in a wide dynamic range environment. Befo giving our design proposal based on our worst-case assumption for DG-2 we like to go through a verification-by-simulation test on the analysis

given in the above two subsections.

To begin with, let us demonstrate three typical frequency error ($\Delta\omega_t$) trajectories in Fig. C.4, C.5 and C.6 for $\Delta f_0 T_F$ = .42, .525 and 1.05 respectively. Notice that each trajectory converges to a stable operating point according to the directions of arrows shown in Fig. C.2. Nevertheless, this is not to say that given an initial operating point the dynamic behavior of $\Delta\omega_t$ will follow Fig. C.2 and converge to a predetermined stable operating point with probability one. Shown in Fig. C.7 is another trajectory for $\Delta f_0 T_f$ = .525, which turns out to be a successful pull-in. These all have been predicted by eq. (C.37a) which tells us that the trajectory of $\Delta\omega_t$ is drifted by a time-varying force $-\gamma D(\Delta\omega_t)$ and, at the same time, perturbed by the variance term $\gamma\tilde{n}(t)$.

Roughly speaking, whenever the drift is overcome by the variance, which occurs with a nonzero probability in the presence of $\tilde{n}(t)$, the trajectory will not follow the phase diagram shown in Fig. C.2 anymore. Simulation results show that successful pull-in can be achieved with high probabilities for $E_b/N_0 \geq 8$ dB at $1/T_b$ = 1 KHz if

$$|\Delta f_0 T_F| < 1/4 \qquad \text{(C.43)}$$

which is larger than the linear region of $D(\Delta\omega)$.

As mentioned before, both frequency jitter and acquisition time are in proportion to B_L. Fig. C.8 is the sample variance trajectory computed from Fig. C.4b. The horizontal straight line is the frequency jitter estimated by (C.31). The simulation result is very close to the theoretical computation. By eq. (C.34b) and (C.35), it is predicted that at $t = T_L$, the frequency error will be reduced to e^{-4} of the

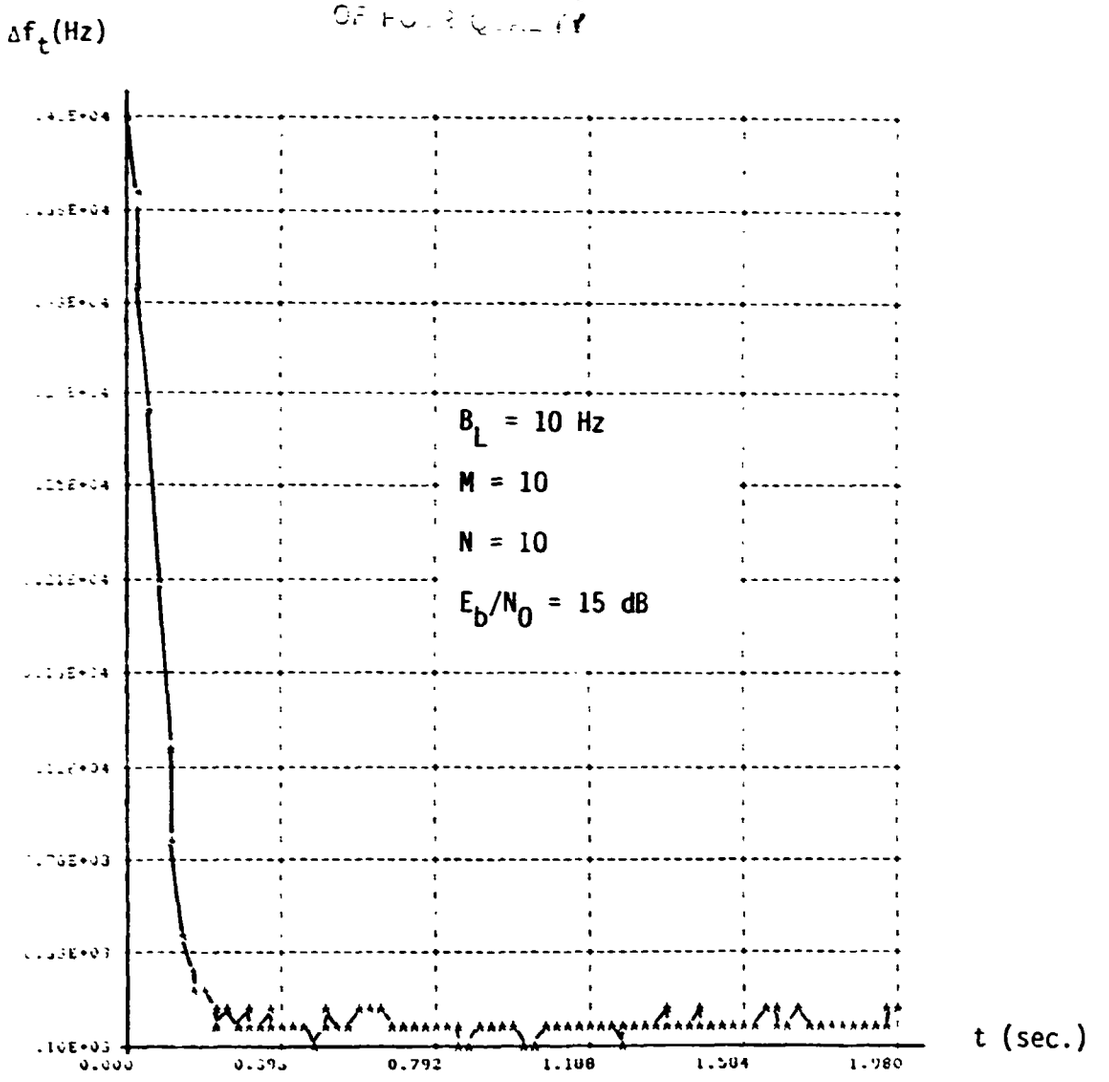

Fig. C.4a. A Sample Trajectory of $\{\Delta\omega_t\}$; Δf_0 = 4.2 KHz, $\Delta f_0 T_F$ = 4.2, E_b/N_0 = 15 dB.

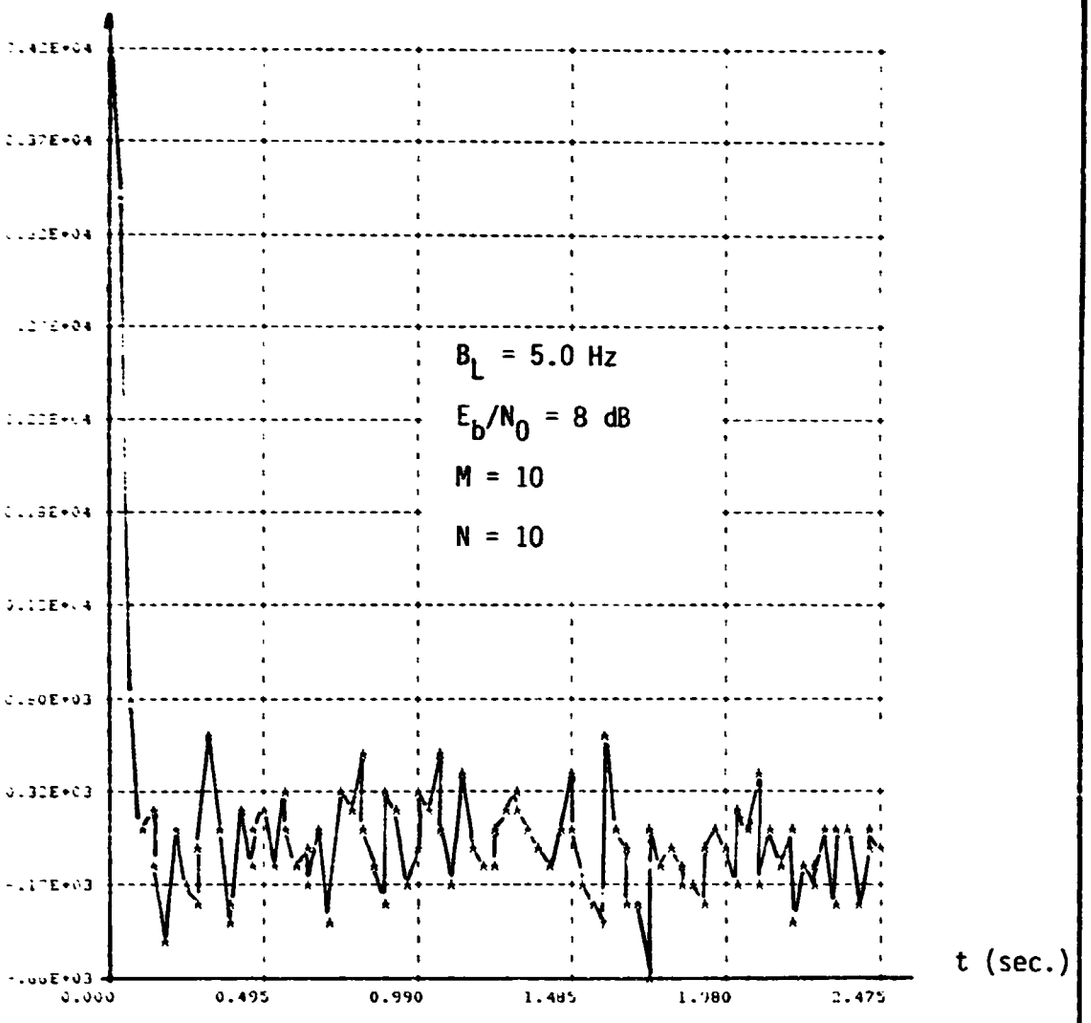

Fig. C .4b. Another Sample Trajectory of $\{\Delta\omega_t\}$ when $\Delta f_0 T_F$ = .42.

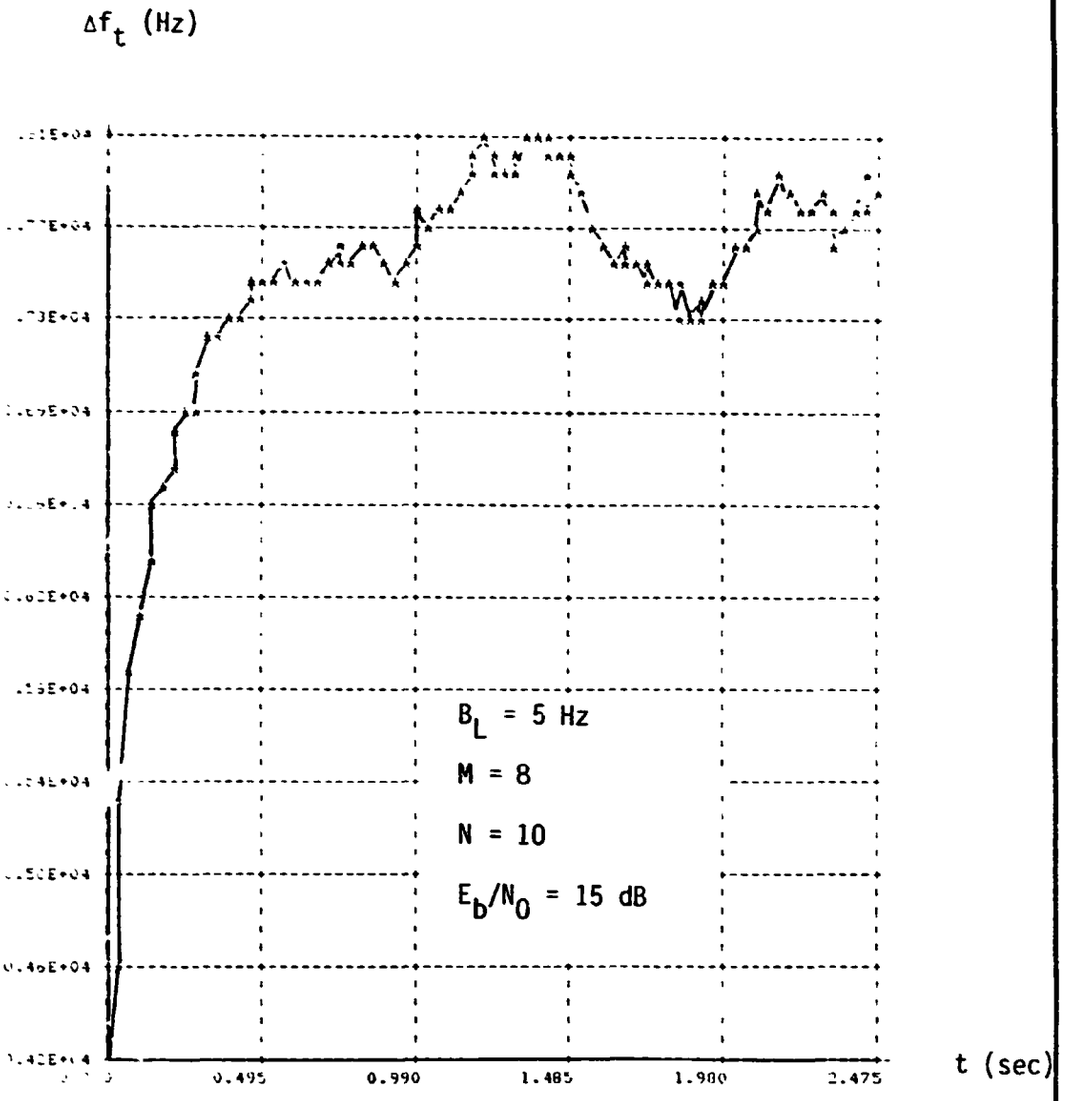

Fig. C.5. A Simple Trajectory of $\{\Delta\omega_t\}$ When $|\Delta f_0 T_F| = .525$.

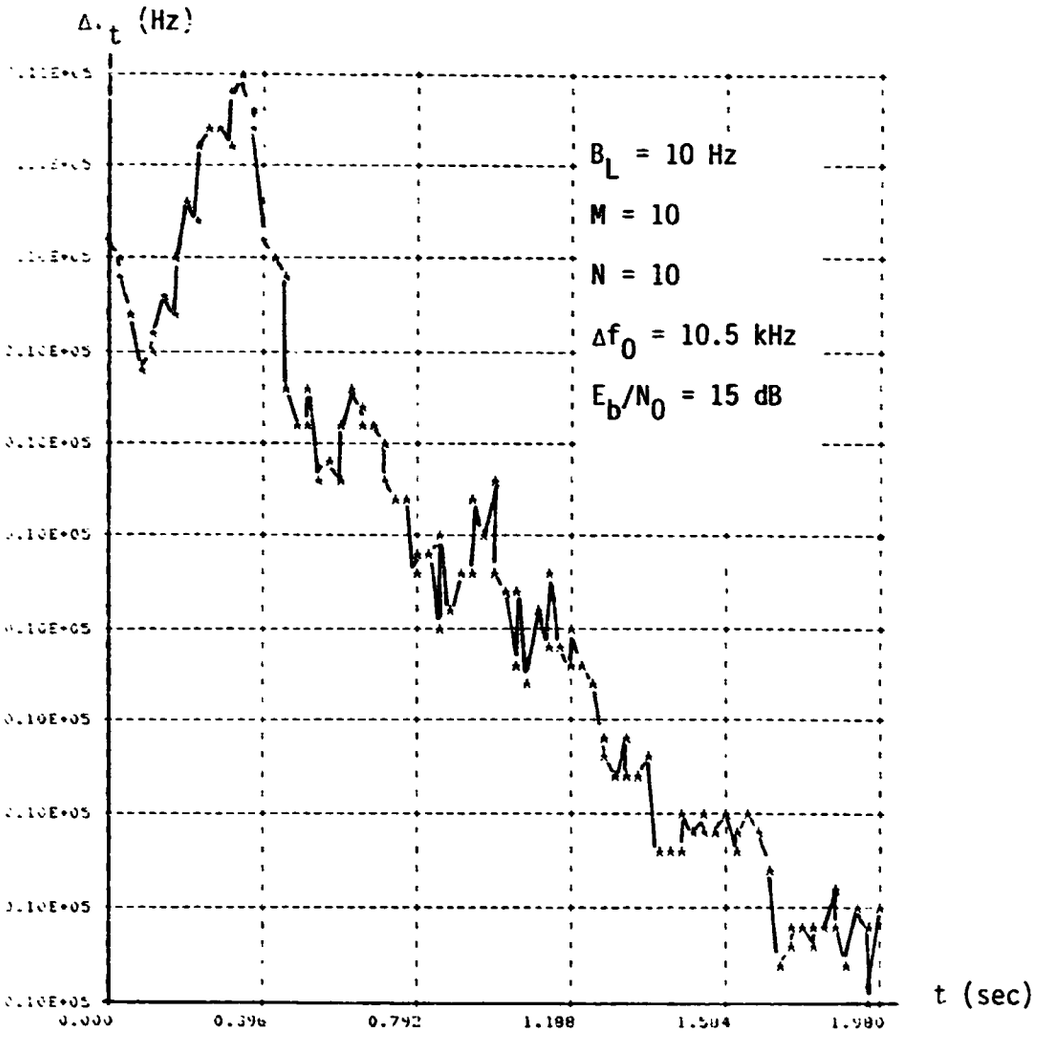

Fig. C.6. A Sample Trajectory of $\{\Delta\omega_t\}$ When $\Delta f_0 T_F = 1.05$.

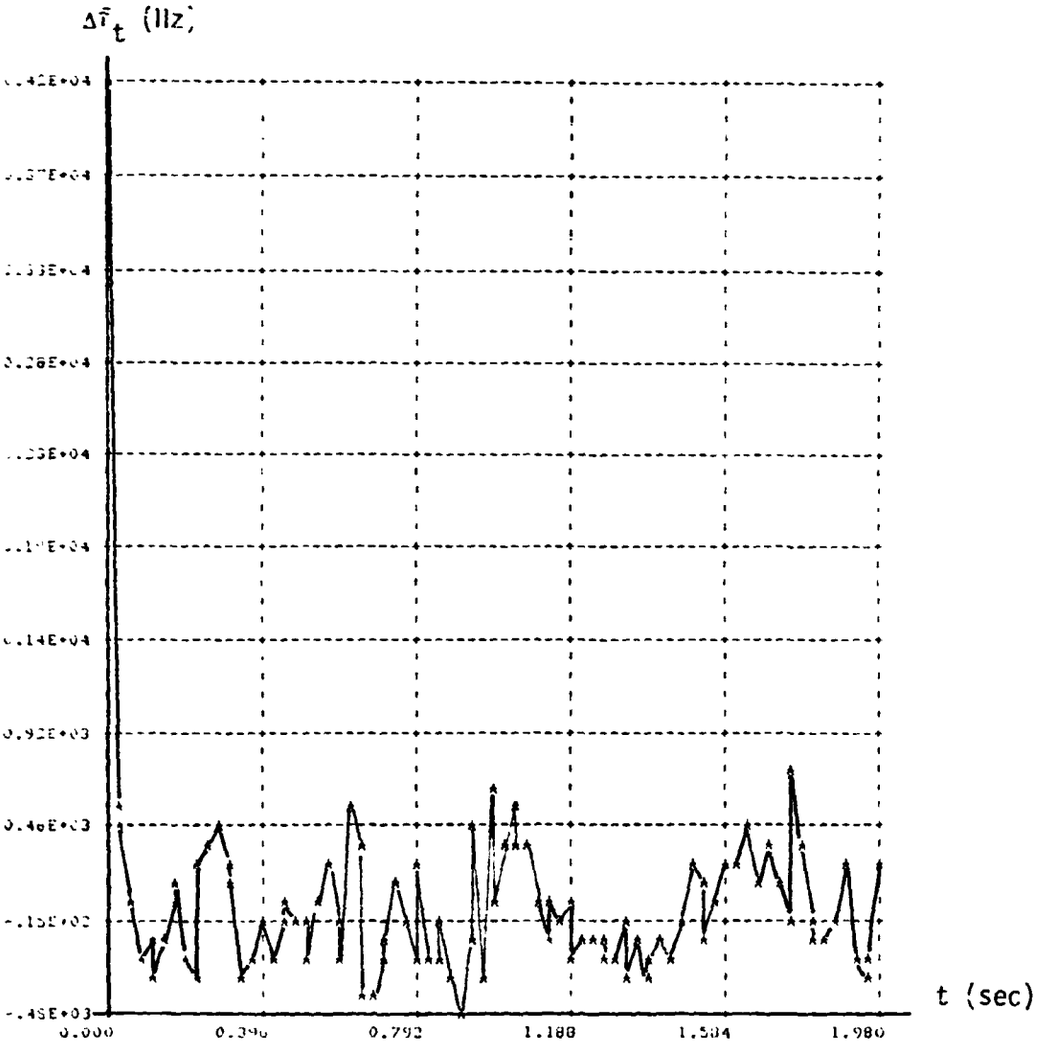

Fig. C.7. A Successful Pull-In Trajectory of $\{\Delta\omega_t\}$ When $\Delta f_0 T_R = .525$.

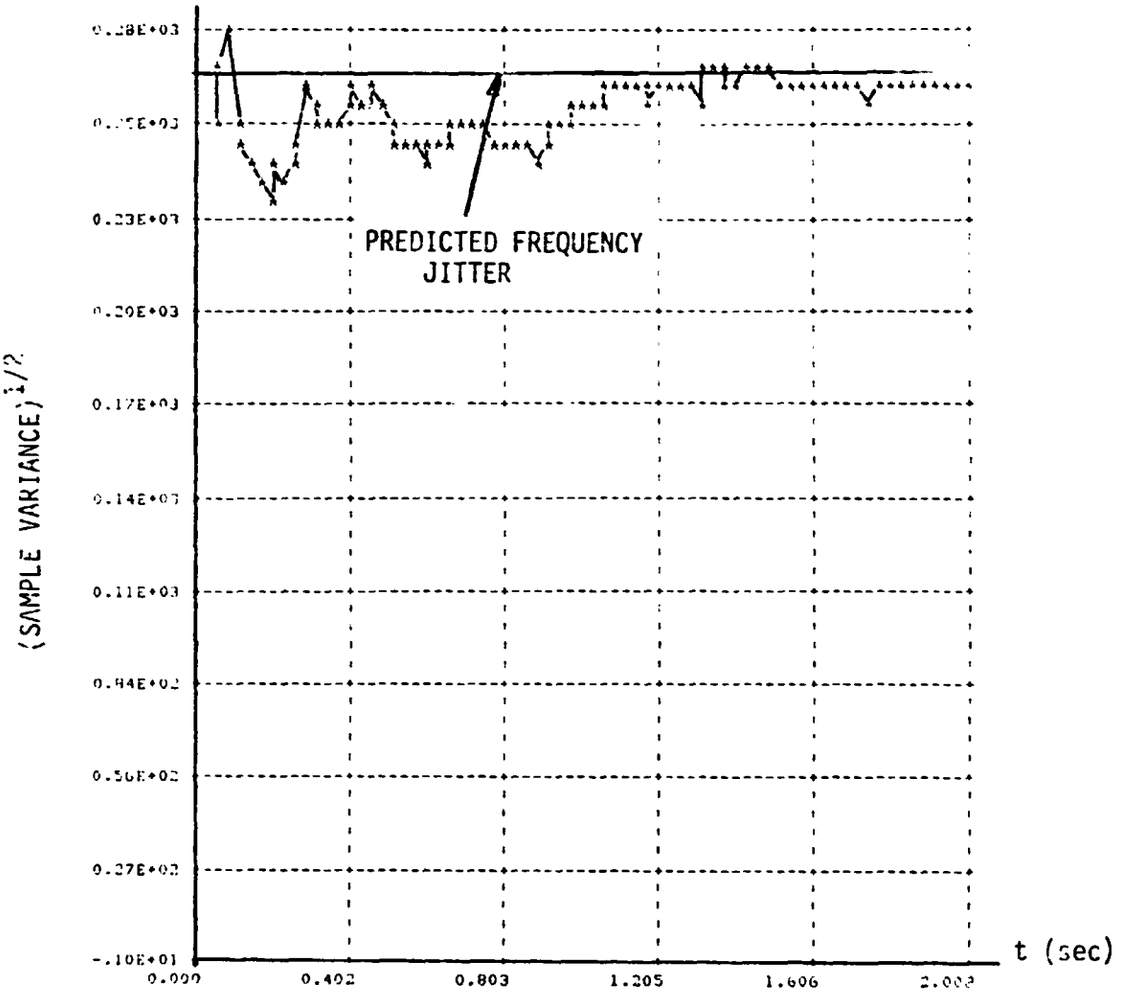

Fig. C.8. Sample Deviation Trajectory Computed From Fig. .4b.

original frequency offset $\Delta\omega_0$. Fig. C.9 and C.10 exhibit two different cases: in Fig. C.9, $\Delta f_0 T_F = .42$ while in Fig. C.10 $\Delta f_0 T_F = .042$. Obviously, the prediction based on (C.35) is too optimistic for the former but quite accurate for the latter. The reason for the discrepancy in Fig. C.9 is simple: the operating point for the former is in the nonlinear part of $D(\Delta\omega)$ and the derivation of eq. (C.35) assumes a linear $D(\Delta\omega)$, which implies a much larger $D(\Delta\omega)$ at $\Delta f_0 T_F = .42$, and zero noise.

C.6.2 Design Procedure for DG-2

Our design proposal is based on the assumption that the available E_b/N_0 at $1/T_b = 1$ KHz is at least 8 dB and the largest frequency uncertainty is ±4.2 KHz. In order to operate in this worst-case condition, T_F must be such that $|T_F \Delta f_0| < .25$, which implies

$$T_F < 6.0 \times 10^{-5} \text{ (sec)}$$

or (C.44)

$$M > 4|\Delta f_0| T_b \approx 17$$

Our second requirement is that noiseless $\Delta\omega$ be reduced to within ±25 Hz in 0.2 second. From (C.36), the loop time constant is

$$T_L = t\left(\ln \frac{\Delta\omega_0}{\Delta\omega_t}\right)^{-1}.$$

Since $T_L = 1/4B_L$ the required loop bandwidth is given by

$$B_L = (4t)^{-1} \ln\left(\frac{\Delta\omega_0}{\Delta\omega_t}\right). \quad (C.45)$$

Substituting $t = 0.2$, $\Delta\omega_0 = 4200$ and $\Delta\omega_t = 25$ into (C.45), we obtain

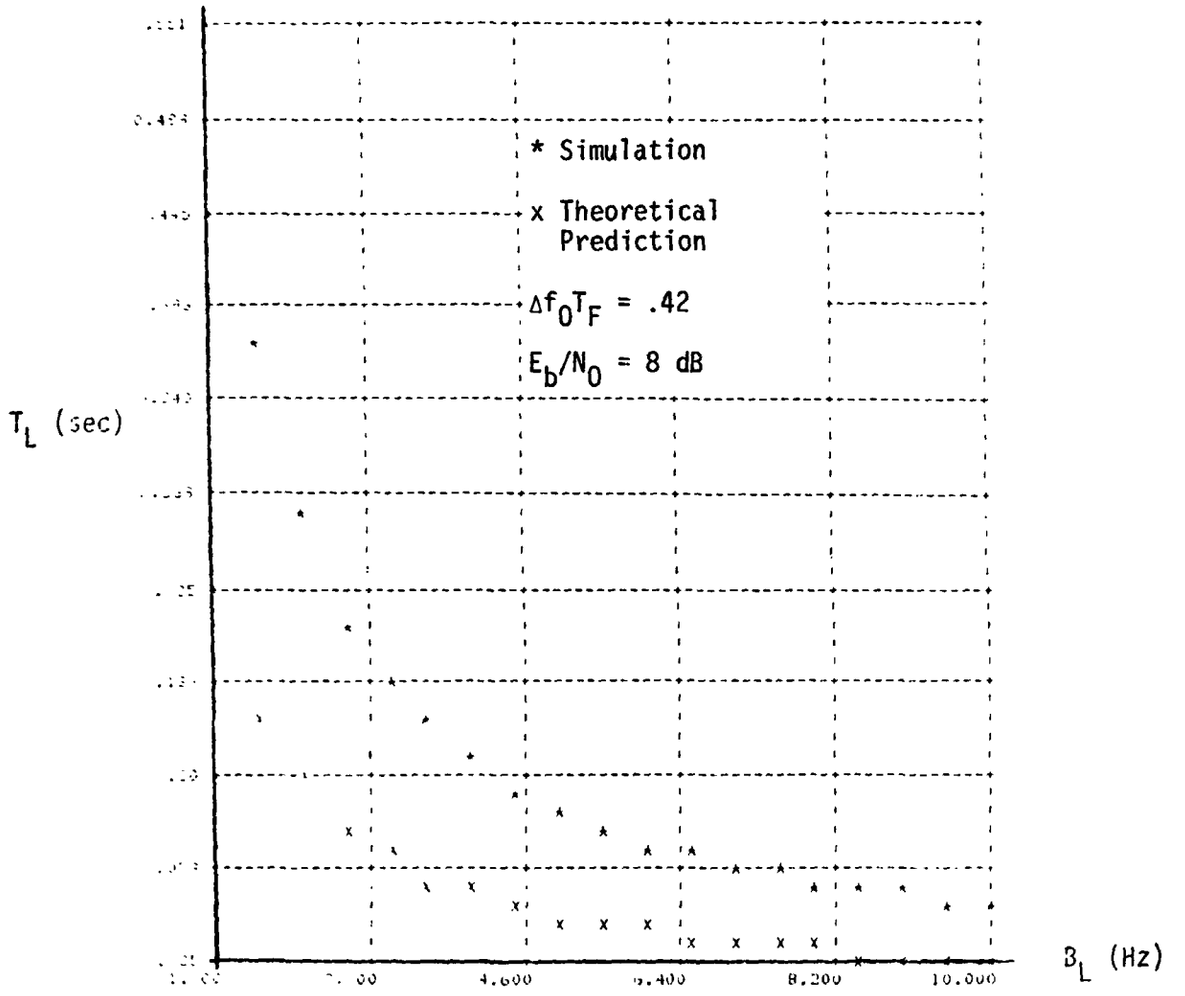

Fig. C.9. Loop Time Constant (T_L) as a Function of B_L.

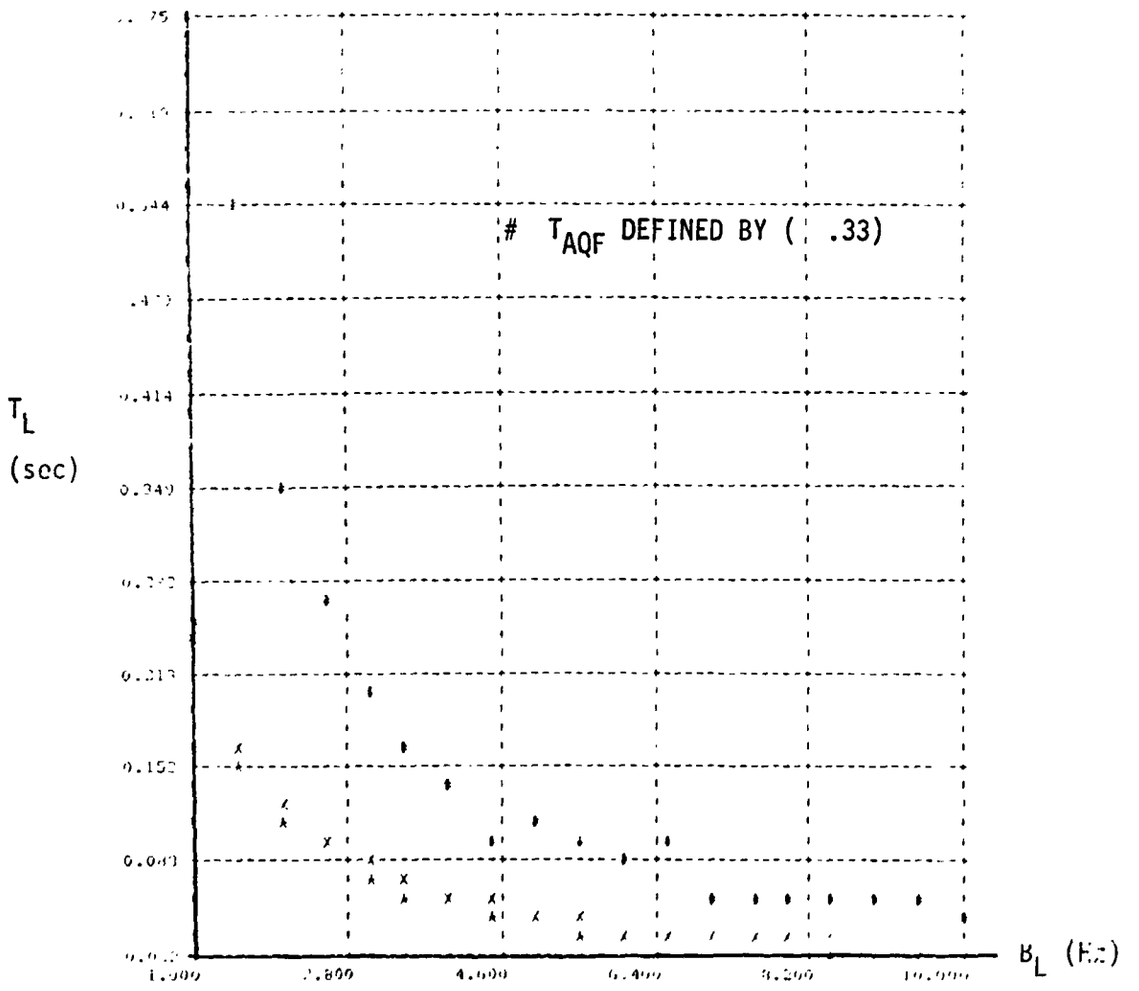

Fig. C.10. Simulation (*) and Theoretical Prediction (x) of T_L at E_b/N_0 = 8 dB.

$$B_L \approx 6.4 \text{ (Hz)} .$$

The third design criterion is to have a frequency jitter less than 10 Hz. By (C.31) this requirement is translated into

$$B_L = \frac{2(\pi\sigma_{\Delta F})^2 T_F}{[(SNR_I')^{-1}+(2SNR_I'^2)^{-1}]} . \qquad (C.46)$$

If M = 20 then we require

$$B_L \approx .012 \text{ (Hz)}$$

and if M=5 then $B_L \approx .36$ (Hz).

With B_L = 6.4 Hz, M = 17 the frequency jitter is about 186 Hz according to (C.31). Assuming 100% pull-in probability and a Gaussian distribution of Δf at t = 0.2 sec, the above jitter implies then that $|\Delta f| < 211$ Hz (one σ point) with probability 0.68 and $|\Delta f| < 30$ Hz with probability 0.02 only. An equivalent statement is that $|\Delta f|$ will remain large for a very long time; see Fig. C.11 and C.12. To get rid of this undesirable phenomena at least one intermediate stage is needed. If M and B_L in this stage is such that the worst Δf, assuming to be the 3σ point 583 Hz at t = 0.2 second, be reduced to 5 Hz (noiseless) when t = 0.6 second. Again by (C.36) we obtain

$$B_L = 2.974 \text{ (Hz)}.$$

Using M = 5, $\sigma_{\Delta F}$ is found to be 28 Hz.

In addition to the above three considerations, the accumulation

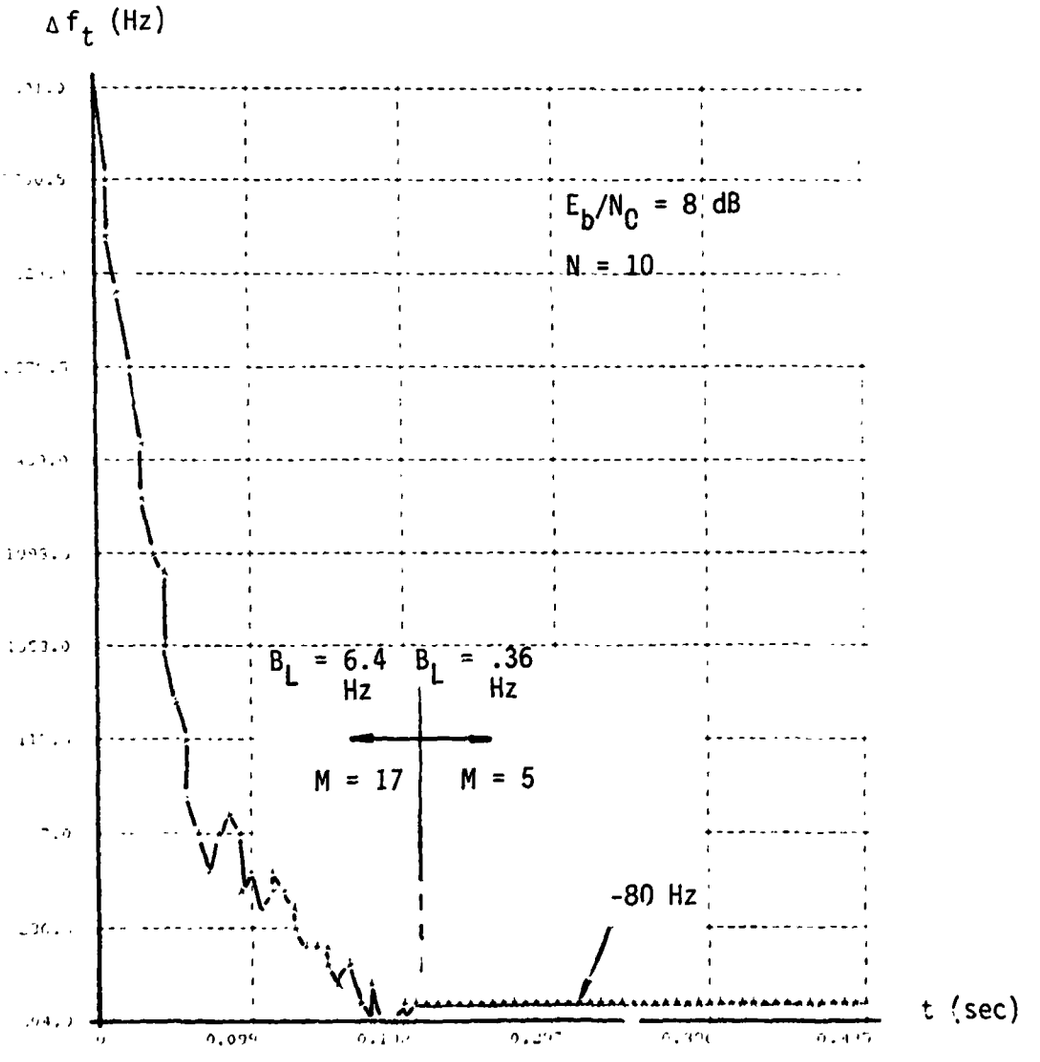

Fig. C.11. A Sample Frequency Error Trajectory for a 2-Stage FAL.

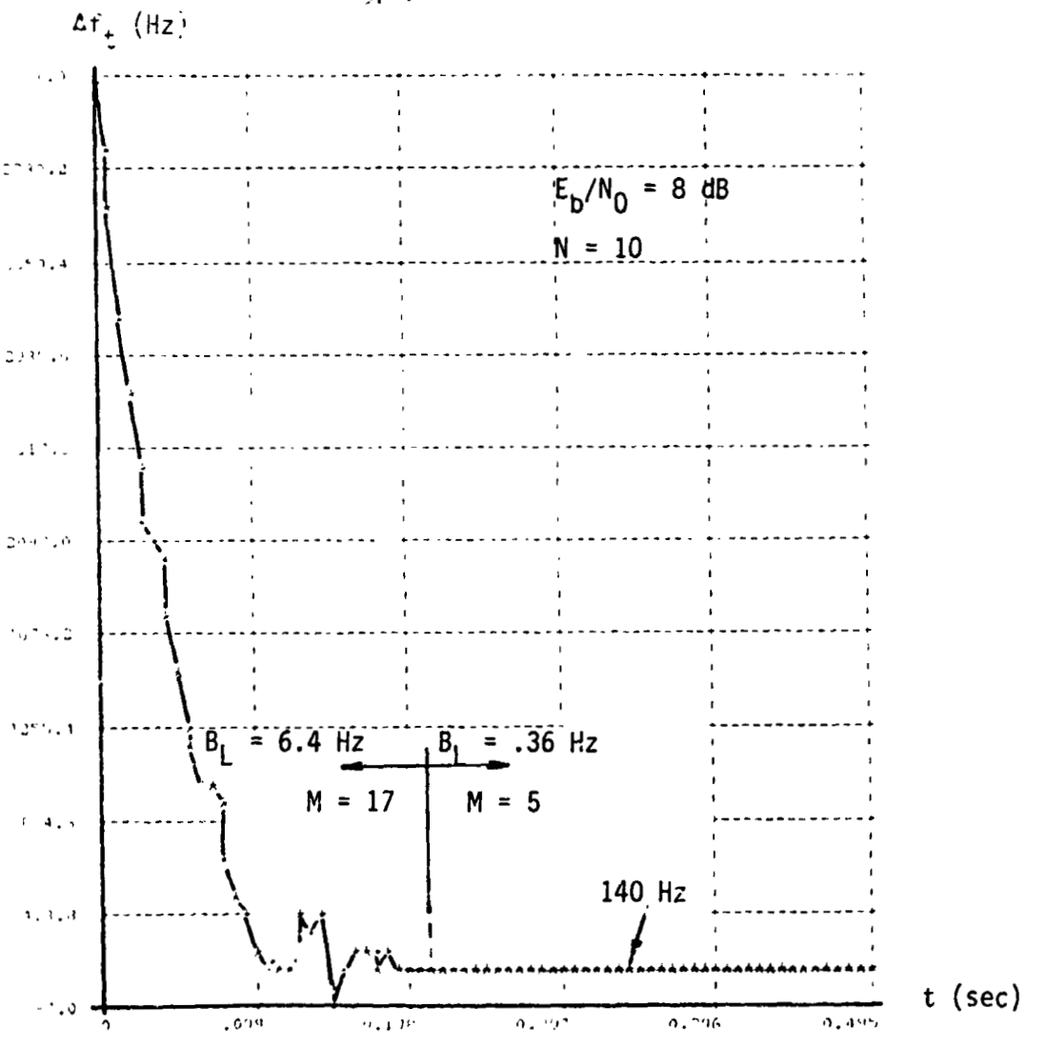

Fig. C.12. Another Sample Trajectory of Δf_t for a 2-Stage FAL.

number N must be large enough so that (1) the loss due to the data transition is negligible, and (2) the digital implementation of the I/D filter has a performance close to an ideal analog I/D low-pass filter. For this, we demand that

$$N > 10.$$

The above seemingly ad hoc design approach can be stated in a more systematic way, i.e., as a mathematic programming problem, as follows.

(1) Given T_b (R_b), E_b/N_0 and Δf_0

$\Rightarrow$ decide initial stage M via

$$M > 4|\Delta f_0|T_b. \tag{C.44}$$

(2) Given $\sigma^2_{\Delta F}$

$\Rightarrow$ decide final stage B_L and M by

$$B_L = \frac{2(\pi\sigma_{\Delta F})^2 T_F}{[(SNR_I)^{-1}+(2SNR^2)^{-1}]} \tag{C.46}$$

and

$$SNR_I = (\frac{E_b}{N_0})/M .$$

(3) Given the number of intermediate stages, N_s

$\Rightarrow$ decide the corresponding B_L and M such that $T_{AQF}(\delta,P)$ defined by (C.37b) is minimized.

Our approach for solving (3, described above is mathematically

unsound and clearly incomplete. An estimate using Gaussian and 100% acquisition assumption shows $|\Delta f| < 46$ Hz with probability .9 at t = 0.6 sec. However, simulation results (Fig. C.13-14) are better than what has been predicted perhaps because of the discrete nature of the AGC loop.

For high E_b/N_0, two-stage loop is often good enough and the design procedure can be summarized as that in Table C.2.

C.7 Lock Detector and Its Performance

Lock detector (LD) is an auxiliary circuit used to provide a recognition signal when the frequency error is reduced to a preset level. Conventional LD algorithms for Costas or squaring loops do not work for FAL because of either large pre-sampling bandwidth (hence $I_k^2+Q_k^2$ fails) or inappropriate indication signal (since $I_k^2-Q_k^2 \alpha \cos \phi_k$).

A good LD for FAL has to take into account the fact that the AGC may not be able to respond appropriately when the frequency error is large. So the design philosophy is to avoid comparing with a signal-power-dependent threshold. This consideration lead to the following LD algorithm: Define

$$C_k \triangleq I_k I_{k-1} + Q_k Q_{k-1} \tag{C.47}$$

Accumulate $|C_k|$ and $|e_k|$ for M_0 times, i.e.,

$$X_1 \triangleq \sum_{k=k_0+1}^{k_0+M_0} |C_k'| \tag{C.48a}$$

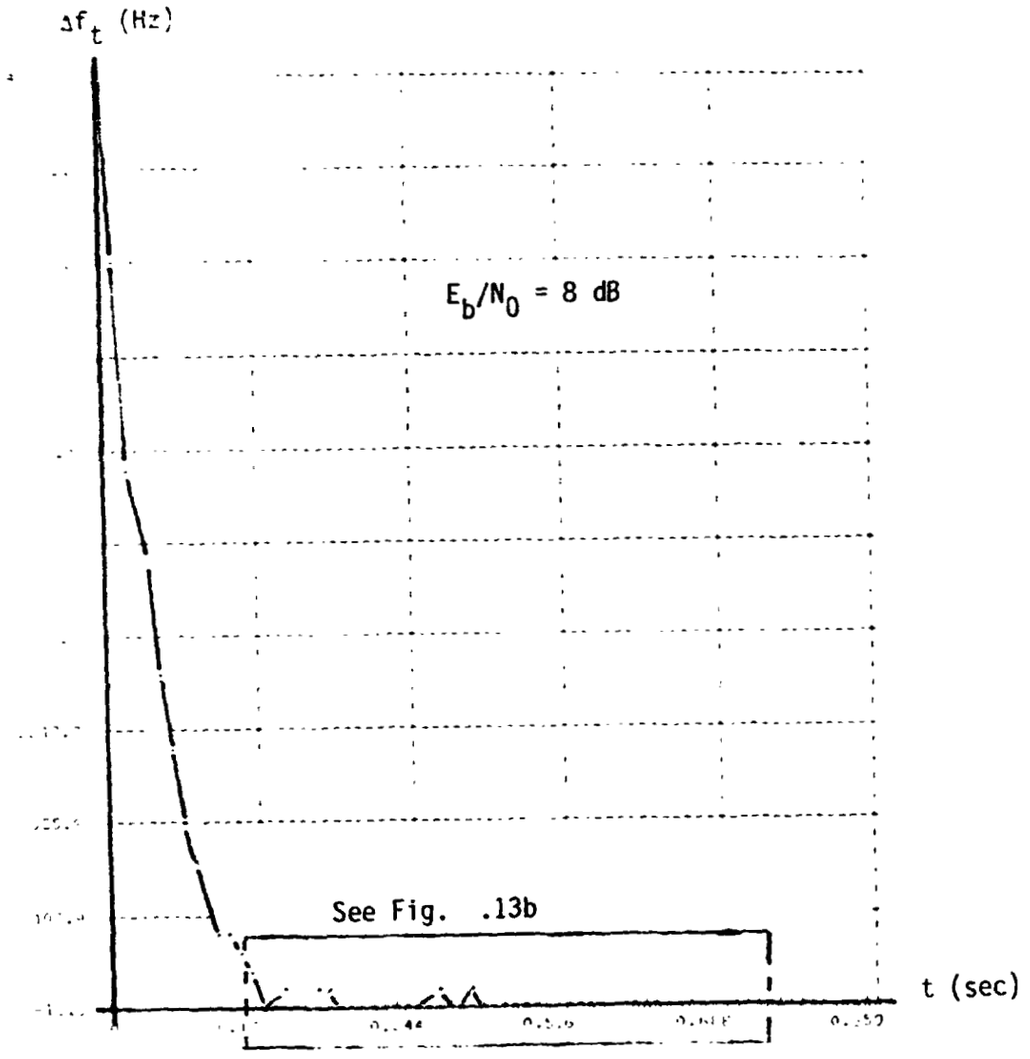

Fig.C.13a. A Sample Trajectory of Δf for a 3-Stage FAL.

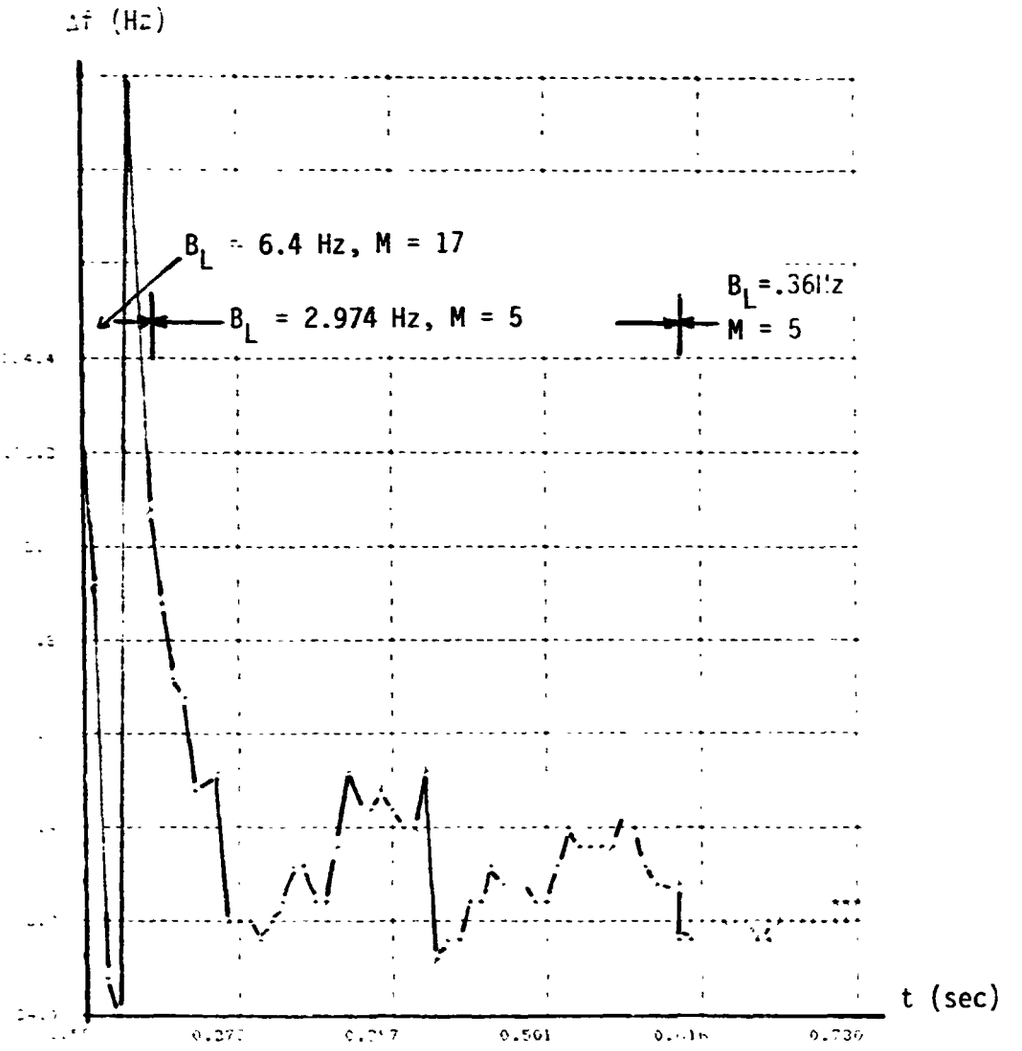

Fig. C.13b. The Enlarged Part of ▭ in Fig. C.13a.

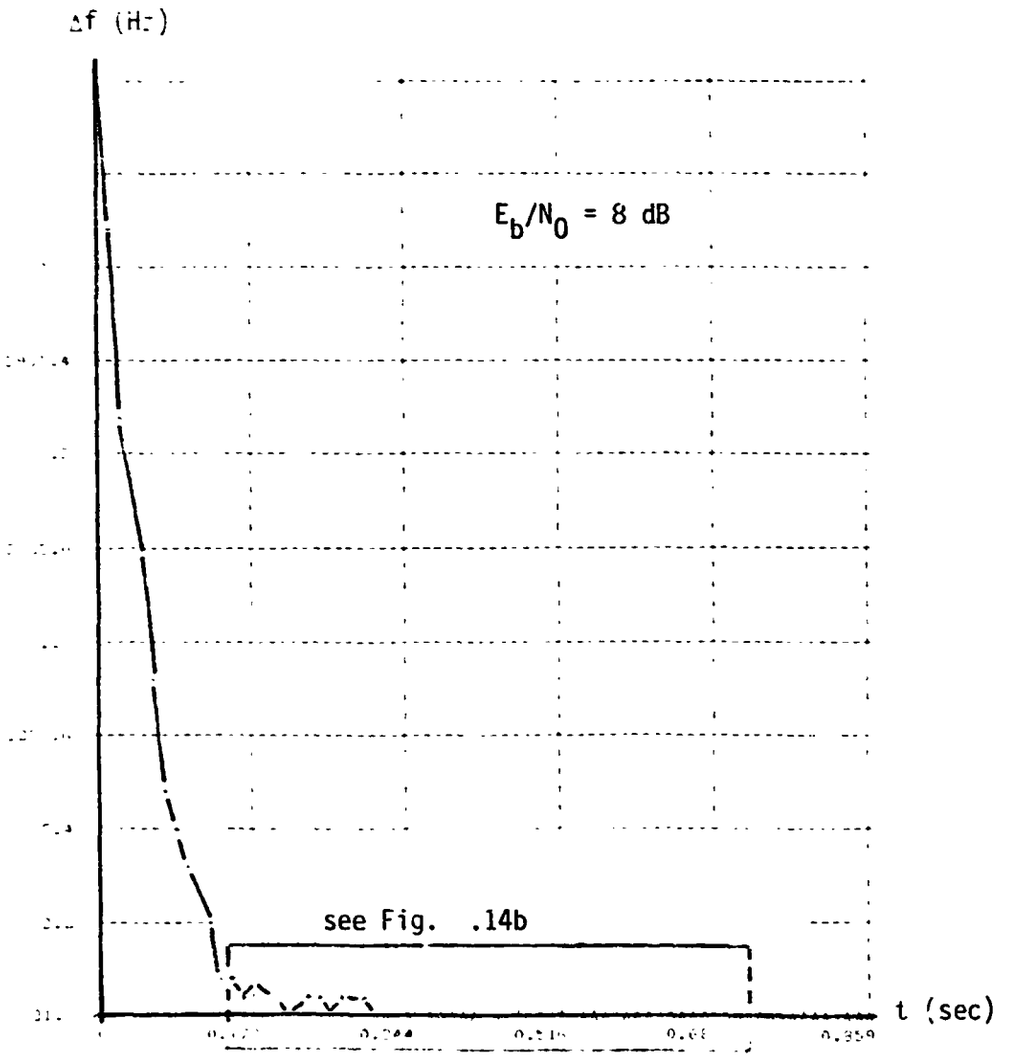

Fig. C .14a. A Sample Trajectory of Δf for a 3-Stage FAL.

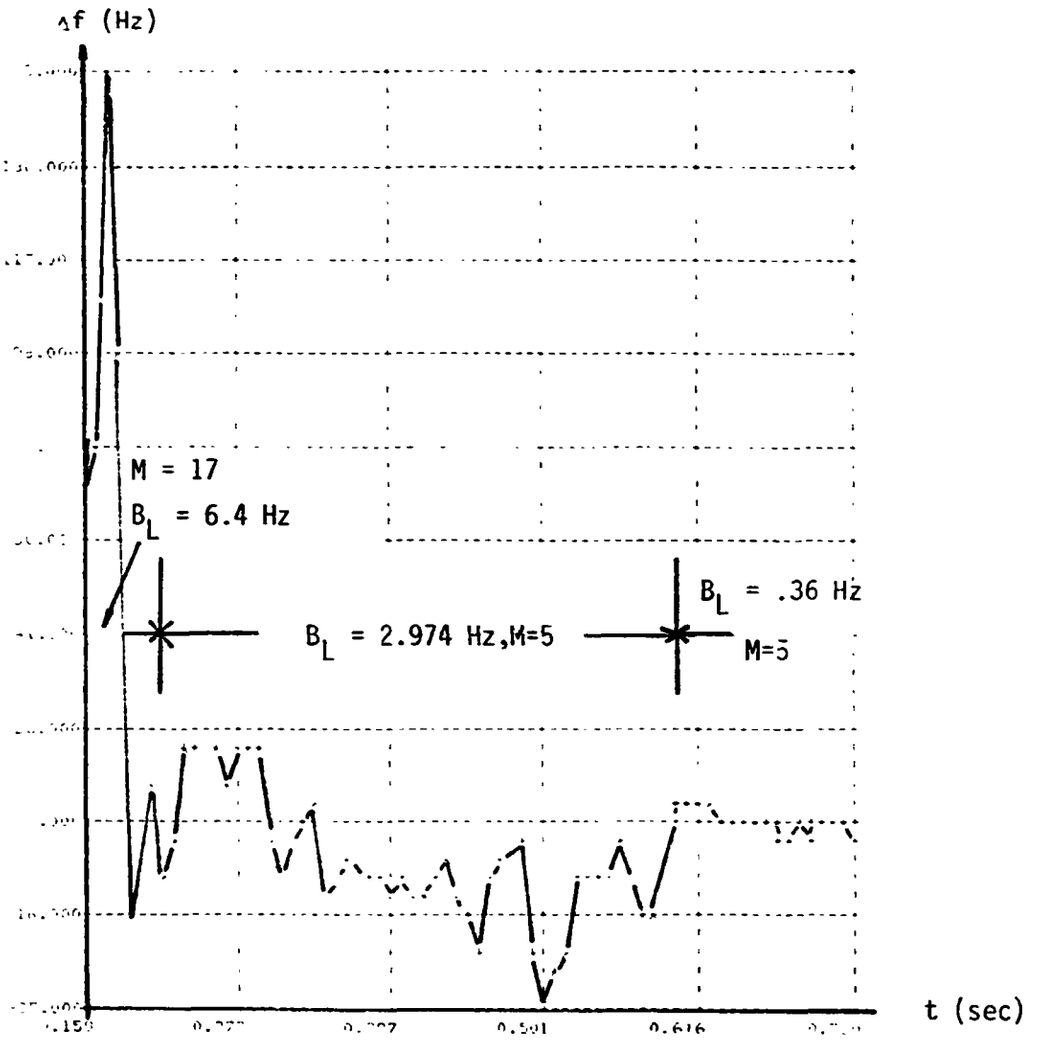

Fig. C.14b. The Enlarged Part of ▭ in Fig. C.14a.

Table C.2. FAL (2-stage) Design Procedure for High E_b/N_0.

SYSTEM PARAMETER	DETERMINED BY	RELATED DESIGN PARAMETER
First Stage T_F (M)	$T_F < \frac{1}{4\lvert\Delta f_0\rvert}$,	$\lvert\Delta f_0\rvert$ = Pull-In Range in Hz
	$M > 4\lvert\Delta f_0\rvert/R_b$	
	$M \geq 5$	Data Transition Loss
First Stage B_L	$B_L = (4t)^{-1} \ln \frac{\Delta\omega_0}{\Delta\omega_t}$	t = Noiseless Pull-In Time (sec.)
		$\Delta\omega_t$ = Pull-In State = Design Frequency Error at t
Second Stage $T_F(M)$ and B_L	$B_L = \frac{2(\pi\sigma_{\Delta F})^2 T_F}{[(SNR_I')^{-1}+2(SNR_I')^{-2}]}$	$\sigma_{\Delta F}$ = Frequency Jitter (Hz)
	$SRN_I' = \frac{E_b}{N_0}(M)^{-1}D_0$	$\frac{E_b}{N_0}$ = Bit Signal-to-Noise Ratio
Accumulation Number N	≥ 10	D_0 = Data Transition Loss

$$X_0 \triangleq \sum_{k=k_0+1}^{k_0+M_0} |e_k'| \,. \qquad \text{(C.48b)}$$

Then declare acquisiition if

$$X_1 > X_0 \,.$$

In (C.48), k_0 is chosen to be large enough that e_k' and C_k' are in steady state. The relation between (C_k', e_k') and (C_k, e_k) is the same as that between $\Delta\omega_k'$ and $\Delta\omega_k$; see eq. (C.26). It can be shown that

$$E(C_k) = 2S\ \mathrm{sinc}^2\left(\frac{\Delta\omega T_F}{2}\right)\cos(\Delta\omega_k T_F). \qquad \text{(C.49)}$$

Thus for $\Delta\omega T_F \ll 1$,

$$E(C_k) \doteq 2S \cos \Delta\omega_k T_F$$

Let C_k be written as

$$C_k = E(C_k|\Delta\omega_k) + [C_k - E(C_{1k}|\Delta\omega_k)]$$

$$\triangleq \bar{C}_k + \tilde{C}_k.$$

It can be shown that $\bar{C}_k$ and $\tilde{C}_k$ are uncorrelated and so

$$E(C_k) = E(\bar{C}_k) + E(\tilde{C}_k)$$

$$= E(\bar{C}_k)$$

$$= \frac{2}{\sqrt{2\pi}\sigma_{\Delta F}} \int_0^\infty E(C_k|\Delta f) e^{-\Delta f^2/2\sigma_{\Delta F}^2} d(\Delta f);$$

moreover,

$$E(C_k^2) = E(\bar{C}_k^2) + E(\tilde{C}_k^2)$$

$$= \frac{2}{\sqrt{2\pi}\sigma_{\Delta F}} \int_0^\infty E^2(C_k|\Delta f) e^{-\Delta f^2/2\sigma_{\Delta F}^2} d(\Delta f) + \beta_v \left(\frac{B_F}{B_L} - 2\right)$$

$$\triangleq \sigma_1 \qquad \text{(C.50)}$$

where

$$\beta_v \triangleq 2\left(\frac{\pi\sigma_{\Delta F}}{B_F}\right)^2.$$

and $E(C_k|\Delta f)$ is given by (C.49); replacing $\Delta\omega$ by $2\pi\Delta f$ and x by 1. We notice in steady state $|\Delta f T_F| \ll 1$; thus $\bar{C}_k \approx 1$ and $|\bar{C}_k| \approx 1$. This can be justified as follows.

The assumption that $|\Delta f T_F| \ll 1$ in steady state with a high probability is derived from the small frequency jitter and large B_F (small T_F) assumptions. Under these conditions, i.e., $\sigma_{\Delta F}^2/B_F \ll 1$, $B_F \ll 1$,

$$E(\bar{C}_k^2) \approx \sqrt{\frac{2}{\pi\sigma_{\Delta F}^2}} \int_0^\infty \cos^2(2\pi\Delta f T_F) e^{-\Delta f^2/2\sigma_{\Delta F}^2} d(\Delta f)$$

$$= \frac{1}{2}\left(1 + e^{-4\beta_v}\right)$$

$$\approx 1$$

and $\beta_v << 1$, $\beta_v \beta_F << 1$, The right hand side of (C.52) is apparently dominated by the first term, $E(\bar{C}_k^2)$; so $C_k \approx \bar{C}_k$ and

$$E(|C_k|) \approx E(|\bar{C}_k|)$$

$$\approx \sqrt{\frac{2}{\pi\sigma_{\Delta F}^2}} \int_0^\infty \cos(2\pi\Delta f T_F) e^{-\Delta f^2/2\sigma_{\Delta F}^2} d(\Delta f)$$

$$= e^{-\beta_v}$$

$$\approx 1.$$

As for e_k, the same assumption leads to

$$e_k \approx 2\pi T_F \Delta f + \tilde{e}_k \qquad (C.51)$$

where $\tilde{e}_k$ is defined in a way similar to $\tilde{C}_k$. Based on (C.7) and the fact that Δf being a Gaussian variable, e_k written as

$$e_k = \bar{e}_k + \tilde{e}_k$$

has a mean $E(e_k)$

$$E(e_k) = E(\bar{e}_k) + E(\tilde{e}_k) = 0$$

and variance $Var(e_k)$

$$Var(e_k) = E(\bar{e}_k^2) + E(\tilde{e}_k^2)$$

$$= \sqrt{\frac{2}{\pi\sigma^2_{\Delta F}}} \int_0^\infty E^2(e_k|\Delta f) e^{-\Delta f^2/2\sigma^2_{\Delta F}} d(\Delta f) + \beta_v(\frac{B_F}{B_L} -)$$

$$\triangleq \sigma_0^2 \qquad (x.52)$$

Hence

$$E(|e_k|) = \int_{-\infty}^{0} \frac{-x}{\sqrt{2\pi}\,\sigma_0} e^{-x^2/2\sigma^2_0} dx + \int_0^\infty \frac{x}{\sqrt{2\pi}\sigma_0} e^{-x^2/2\sigma_0^2} dx$$

$$= \sqrt{\frac{2\sigma_0^2}{\pi}} \triangleq \mu_0 \qquad (C.53a)$$

and

$$Var(|e_k|) = \sigma_0^2 - \frac{2}{\pi}\sigma_0^2 = (1 - \frac{2}{\pi})\sigma_0^2 \triangleq \hat{\sigma}_0^2 \qquad (C.53b)$$

Notice that by taking absolute value of e_k, the variance is reduced by a factor of $(1-2/\pi)^{-1} \approx 2.75$, $Var(e_k)$ is of the order of $(ST_F/N_0)^{-1}$ while $Var(|e_k|) = 0((\frac{2.75ST_F}{N_0})^{-1})$. Similar reduction between $Var(C_k)$ and $Var(|C_k|)$ is also obtained. Define

$$\mu_1 \triangleq E(|\overline{C}_k|)$$

$$= \frac{2}{\sqrt{\pi\sigma^2_{\Delta F}}} \int_0^\infty \text{sinc}^2(\pi\Delta f T_F)\cos(2\pi\Delta f T_F) e^{-\Delta f^2/2\sigma^2_{\Delta F}} d(\Delta f) \qquad (C.54a)$$

then

$$\hat{\sigma}_1^2 = \sigma_1^2 - \mu_1^2 .$$

For $M_0 >> 1$, x_1 and x_0 can be approximated by Gaussian random variables, using a central limit theorem type argument, with means $M_0\mu_1$, $M_0\mu_0$ and variances $M_0\sigma_1^2$, $M_0\sigma_0^2$ respectively.

The detection probability of the LD is then given by

$$P_{D_L} = Pr\{x_1 > x_0\}$$

$$= Pr\{x_1 - x_0 > 0\}$$

$$= \text{erfc}\left(\frac{\mu_0 - \mu_1}{\sqrt{(\hat{\sigma}_1^2 + \hat{\sigma}_0^2)/M_0}}\right)$$

$$> 1/2 \qquad \text{(C.55)}$$

The inequality, $P_{D_L} > 1/2$ is derived from the fact that $\mu_1 > \mu_0$ which is obvious from observing (C.53a) and (C.54a). Of course, P_{D_L} is still a function of SNR_I, though a very insensitive one (Fig. C.15), but the AGC sensitivity problem has been eliminated.

C.8 Modification for DG-1

C.8.1 Modification in Loop Structure

PN sequences are used in DG-1. In the receiver, code synchronization must be established before frequency acquisition subsystem is initialized. For mode 1 and 2, the I and Q channel modulating PN sequences are derived from the same generator but the Q channel sequence is offset by x + 1/2 chips relative to the I channel sequence where $x \geq 20{,}000$. It is appropriate to model them as two independent PN sequences as far as performance is concerned since $T_F/T_c << 20{,}000$ in all practical cases. To utilize signal energies from both independent channels, like the 2-DDL case we 'enhance' the FAL of Fig.

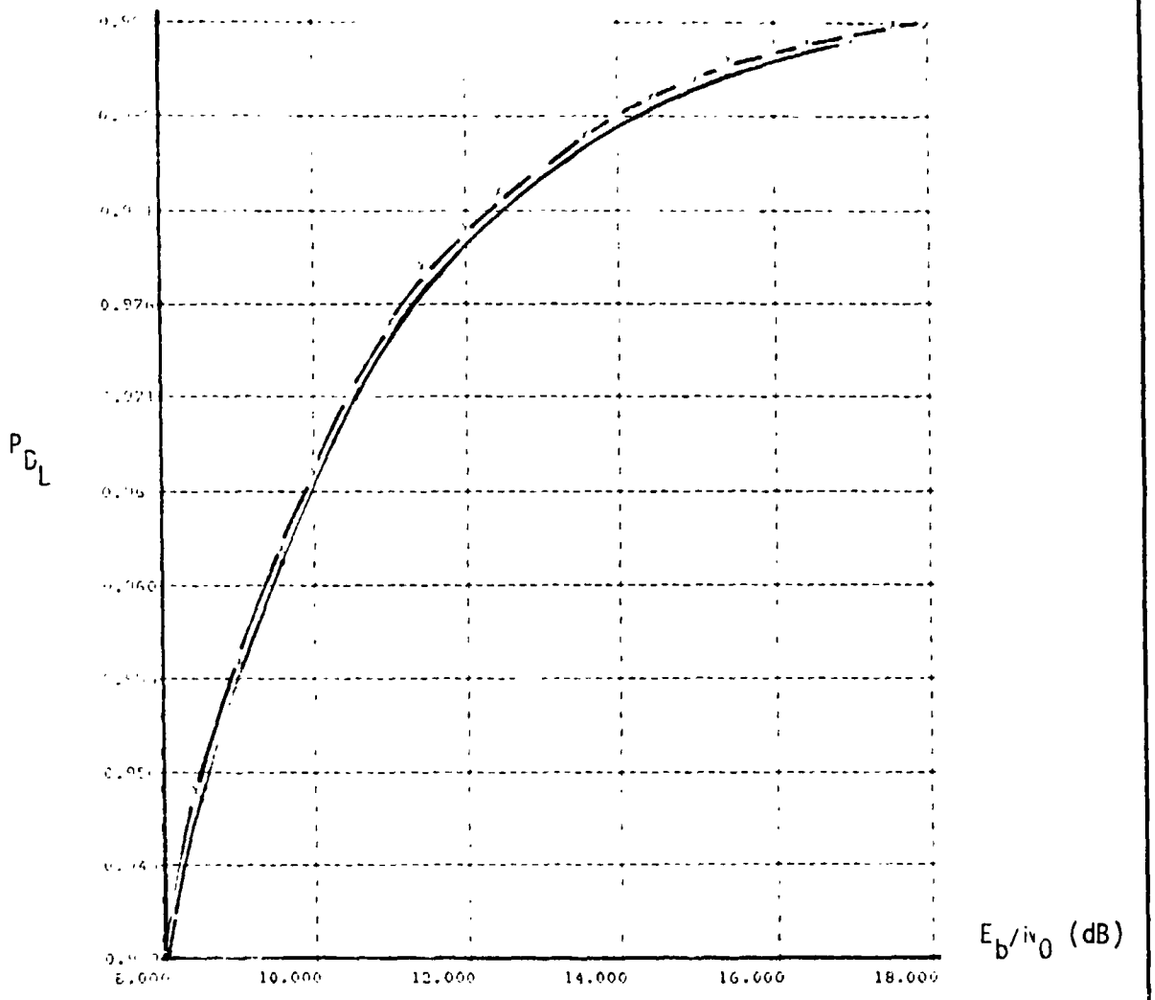

Fig. C.15. Lock Detector Detection Probability for DG-1, Mode 1 (——) and DG-2 (—x—).

C.1 to that of Fig. C.16. Statistically, the control signal from the upper pair of channels is the same as that from the lower ones, except for a scale factor. It is thus proper enough to discuss the upper half only. Unless otherwise specified, it is henceforth understood that the signal and noise under consideration are from the upper (I) channels. To simplify our notation, the argument for distinguishing upper and lower channels will be suppressed if there is no danger of confusion. For this 2-channel FAL, (C.10a) and (C.10b) should be modified to become

$$S^I_{k,\ell} = G_I d_{I_k} \cos[\phi_k + \Delta\omega_k(\ell-1)T_s] + \hat{n}^I_{k,\ell}$$

$$\triangleq \hat{S}^I_{k,\ell} + \hat{n}^I_{k,\ell} \qquad \text{(C.56a)}$$

$$S^Q_{k,\ell} = G_I d_{I_k} \sin[\phi_k + \Delta\omega_k(\ell-1)T_s] + \hat{n}^Q_{k,\ell}$$

$$\triangleq \hat{S}^Q_{k,\ell} + \hat{n}^Q_{k,\ell} \qquad \text{(C.56b)}$$

where

$$\hat{n}^I_{k,\ell} = -n_{PN} G_Q \sin[\phi_k + \Delta\omega_k(\ell-1)T_s]$$

$$n_{k,\ell} = n_{PN} G_Q \cos[\phi_k + \Delta\omega_k(\ell-1)T_s]$$

$$n_{PN} = \frac{1}{T_s}\int_0^{T_s} d(t)PN_1(t)PN_2(t)dt \doteq \frac{1}{T_s}\int_0^{T_s} dPN_1(t)PN_2(t)dt$$

(mode 1 and 2 or mode 3, Bi-ϕ) (C.57a)

$$= \frac{1}{T_s}\int_0^{T_s} d(t)PN_1(t)dt \doteq \frac{1}{T_s}\int_0^{T_s} dPN_1(t)dt \quad \text{(mode 3,NRZ)}$$

(C.57b)

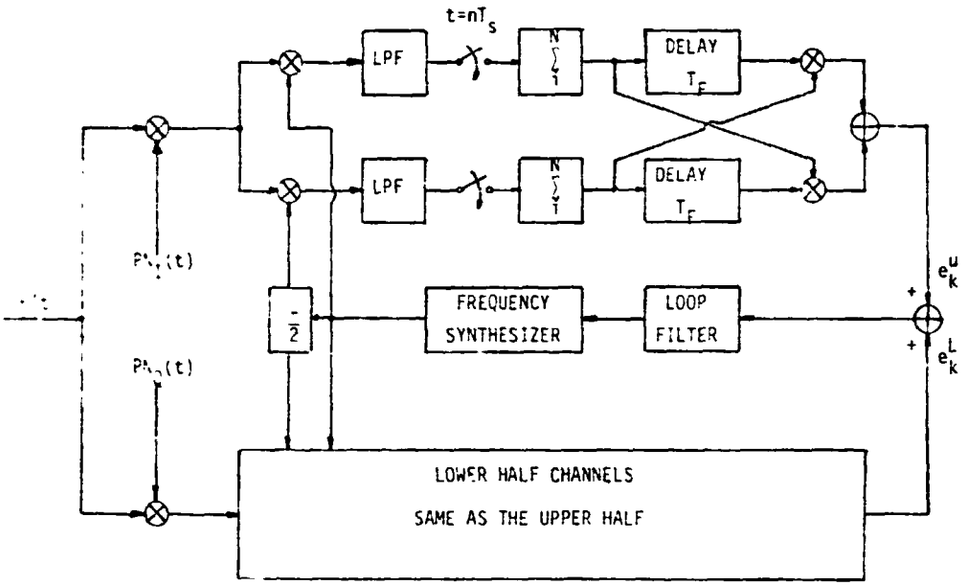

Fig. C.16. Analytic Model for the Double Frequency Acquisition Loop (DFAL) Used in DG-1.

d(t) is a ±1 valued data stream, d is a ±1 binominal random variable, and $PN_1(t)$, $PN_2(t+\frac{T_c}{2})$ are two independent PN sequences offset by half a chip time (T_c).

C.8.2 Noise Model for DG-1

Mathematically, eq. (C.57a) and(C.57b) are equivalent to

$$n_{PN} = \frac{1}{L} \sum_{i=1}^{2T_s/T_c} \frac{b_i}{2} \qquad \text{(C.58a)}$$

$$= \frac{1}{L} \sum_{i=1}^{T_s/T_c} b_i \qquad \text{(C.58b)}$$

where b_i are independent equally likely ±1 valued binominal random variables and $T_s/T_c \triangleq L$ is assumed to be an integer. We can rewirte (C.9a) and (C.9b) for DG-1 as

$$I_k = \frac{1}{N} \sum_{\ell=1}^{N} (\hat{S}^I_{k,\ell} + \hat{n}^I_{k,\ell} + n^I_{k,\ell})$$

$$\triangleq S^I_k + \frac{1}{N} \sum_{\ell=1}^{N} (\hat{n}^I_{k,\ell} + n^I_{k,\ell})$$

$$\triangleq S^I_k + n^I_k \qquad \text{(C.59a)}$$

and

$$Q_k = \frac{1}{N} \left(\sum_{\ell=1}^{N} \hat{S}^Q_{k,\ell} \right) + \frac{1}{N} \sum_{\ell=1}^{N} (\hat{n}^Q_{k,\ell} + n^Q_{k,\ell})$$

$$\triangleq S^Q_k + n^Q_k \qquad \text{(C.59b)}$$

It is well known that n_{PN} approaches to a Gaussian variable as T_s/T_c goes to infinite. For finite T_s/T_c, it can be shown [Appendix I, 5] that the rms approximation error e, defined by

$$e^2 = \sum_{k=0}^{L} [P_b(k)-P_g(k)]^2$$

where

$$P_b(k) \triangleq Pr(n_{PN}=K) = \binom{L}{\frac{K+L}{2}} 2^{-L}, \quad -L \leq K \leq L$$

$$P_g(k) \triangleq \frac{1}{2}\left[\text{erf}\left(\frac{K+\frac{1}{2}}{\sqrt{2}L}\right) - \text{erf}\left(\frac{K-\frac{1}{2}}{\sqrt{2}L}\right)\right]$$

is less than 3% if $L \geq 12$ for mode 3 or if $L \geq 6$ for mode 1 and 2. Based upon this, n_k^I and n_k^Q will be approximated by two independent zero mean Gaussian variables with variance equal to

$$\text{Var}(n_k^I) = \begin{cases} \frac{1}{2}\left(\frac{1}{2L'(1+G)} + \frac{N_0}{ST_F}\right) & \text{(mode 3,NRZ)} \\ \frac{1}{2}\left(\frac{1}{4L'(1+G)} + \frac{N_0}{ST_F}\right) & \text{(otherwise)} \end{cases} \qquad \text{(C.60a)}$$

and

$$\text{Var}(n_k^Q) = \text{Var}(n_k^I) \qquad \text{(C.60b)}$$

if

$$L' = ML \begin{cases} \geq 6 & \text{(mode 1 and 2 or, mode 3, Bi-}\phi\text{)} \\ \geq 12 & \text{(mode 3,NRZ)} \end{cases} \qquad \text{(C.70)}$$

C.8.3 Frequency Jitter

Forming the control signal e_k by adding the error signals from the

upper channels e_k^u and that from the lower ones e_k^L, i.e.,

$$e_k = e_k^u + e_k^L ,$$

the frequency jitter is found to be

$$\sigma_{\Delta F}^2 = \frac{\gamma B_F}{8\pi^2} \left\{ \frac{1}{2} \left[\frac{1+G^2}{a_0^2 L'^2 (1+G)^2} + \frac{1}{L'(SNR_I)} + \frac{1}{(SNR_I)^2} \right] + \frac{1+G^2}{a_0 L'(1+G)^2} + \frac{1}{(SNR)_I} \right\} \qquad (C.71)$$

where

$a_0 = 4$ for mode 1 and 2 or, mode 3 with Bi-ϕ

$\quad\;\; 2$ for mode 3, NRZ.

For $L' \gg 1$,

$$\sigma_{\Delta F}^2 = \frac{\gamma B_F}{8\pi^2} \left[\frac{1}{2(SNR_I)^2} + \frac{1}{SNR_I} \right] . \qquad (C.72)$$

If T_c^{-1} = 3 M bits/sec, M = 20, $1/T_B$ = 1 k bits/sec, then $L' = 1.5 \times 10^2$, and if M=5, $L' = 6.0 \times 10^2$.

In both cases, $L' \gg 1$ and $1/L' \ll 1/SNR_I$ so the design parameters in C.6.2 remains good for DG-1 if the design criterions are the same; see Fig. C.17 for a comparison. Suppose only the lower channels, i.e., the stronger Q channel signal is tracked, then (C.71) becomes

$$\sigma_{\Delta F}^2 = \frac{\gamma B_F}{8\pi^2} \left\{ 2^{-1} \left[\frac{1}{a_0 L'} + \frac{1+G}{G(SNR_I)} \right]^2 + \frac{1}{a_0 L'} + \frac{1+G}{G(SNR_I)} \right\}. \qquad (C.73)$$

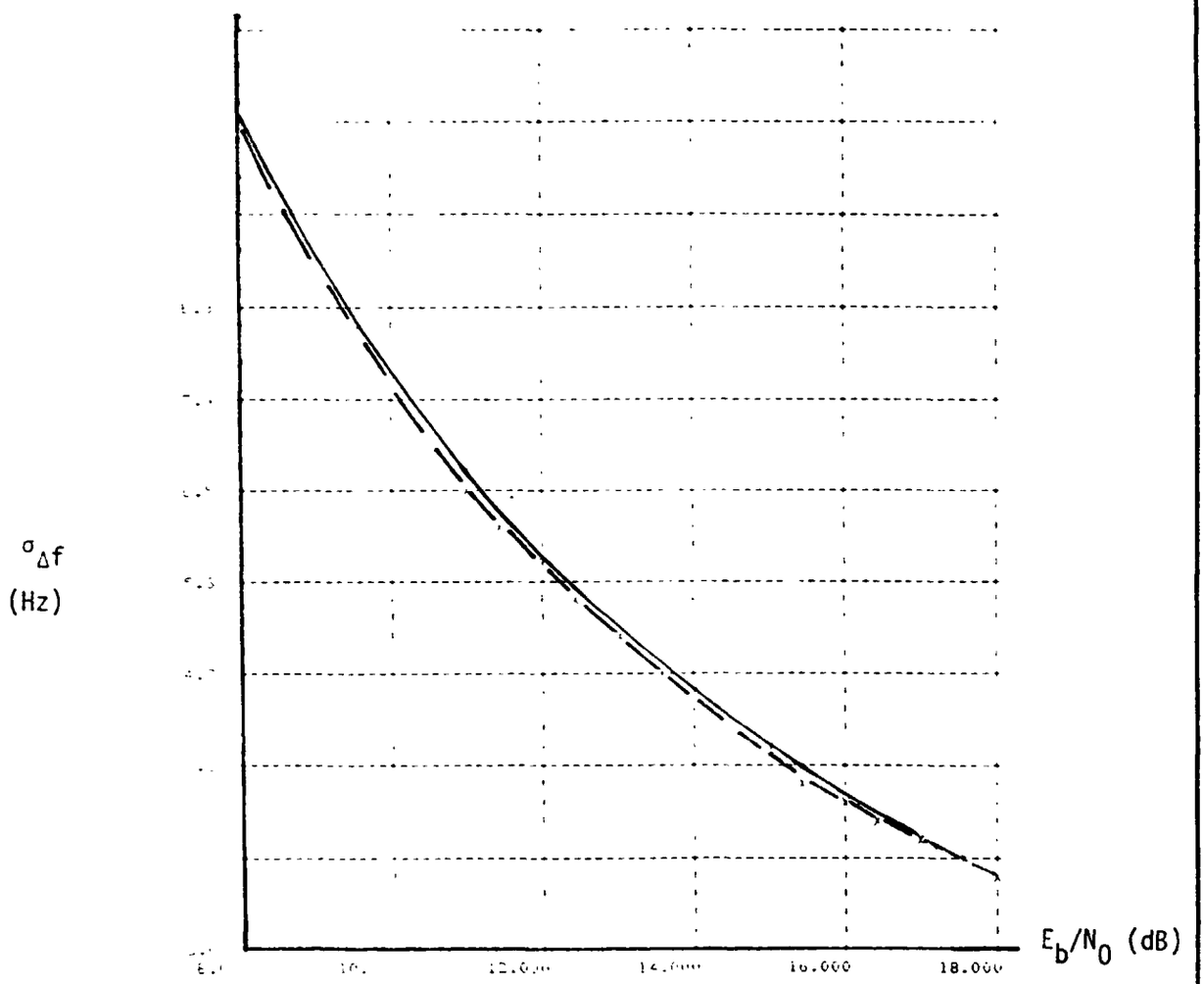

Fig. C.17. Frequency Jitter for DG-1, Mode 1 (——) and DG-2 (—x—).

For large L'

$$\sigma^2_{\Delta F} = \frac{\gamma B_F}{8\pi^2}\left[\frac{1}{2(SNR_I^Q)^2} + \frac{1}{SNR_I^Q}\right] \qquad (C.74)$$

where

$$SNR_I^Q = (SNR_I) \cdot \frac{G}{1+G} .$$

REFERENCES

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[3] Karlin, S. and Taylor, H. M., A First Course in Stochastic Processes, Academic Press, Inc., New York, 1975.

[4] Uhlenbeck, G. E. and Ornstein, L. S., "On the Theory of the Brownian Motion," Physical Review, Vol. 36, July 1930.

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APPENDIX D

INTRODUCTION TO THE APPLICATION OF AIRS DEMONSTRATION PROGRAM (APD)

D.1 Purpose

The AIRS demonstration program (APD) described herein is a FORTRAN language software package capable of analyzing and simulating the performance of various subsystems of the AIRS. It is an interactive software package developed by LinCom for NASA/Goddard Space Flight Center to run on the Perkin-Elmer computer, and will be used as a software analysis tool for the AIRS. This appendix and the one following discuss the organization and applications of the APD. Definitions of input and output parameters are documented, and, for explanatory purposes, a sample run is included at the end.

D.2 APD Design Philosophy and Architecture

The functional guidelines which were followed in the course of designing, developing the APD are stated below:

(1) APD will allow a great deal of flexibility for any system change and expansion.

(2) It will serve as a engineering analysis tool in both system design stage and system operation stage.

(3) It should be easy to understand, use and maintain.

(4) The outputs should contain all the information necessary for system performance assessments.

(5) The powerful capability of the existing software package-CLASS should be utilized.

(6) The computation time should be kept as a minimum.

As a consequence of the above requirements, the APD is organized in a logical and structural modular form as shown in Fig. D.1, basic

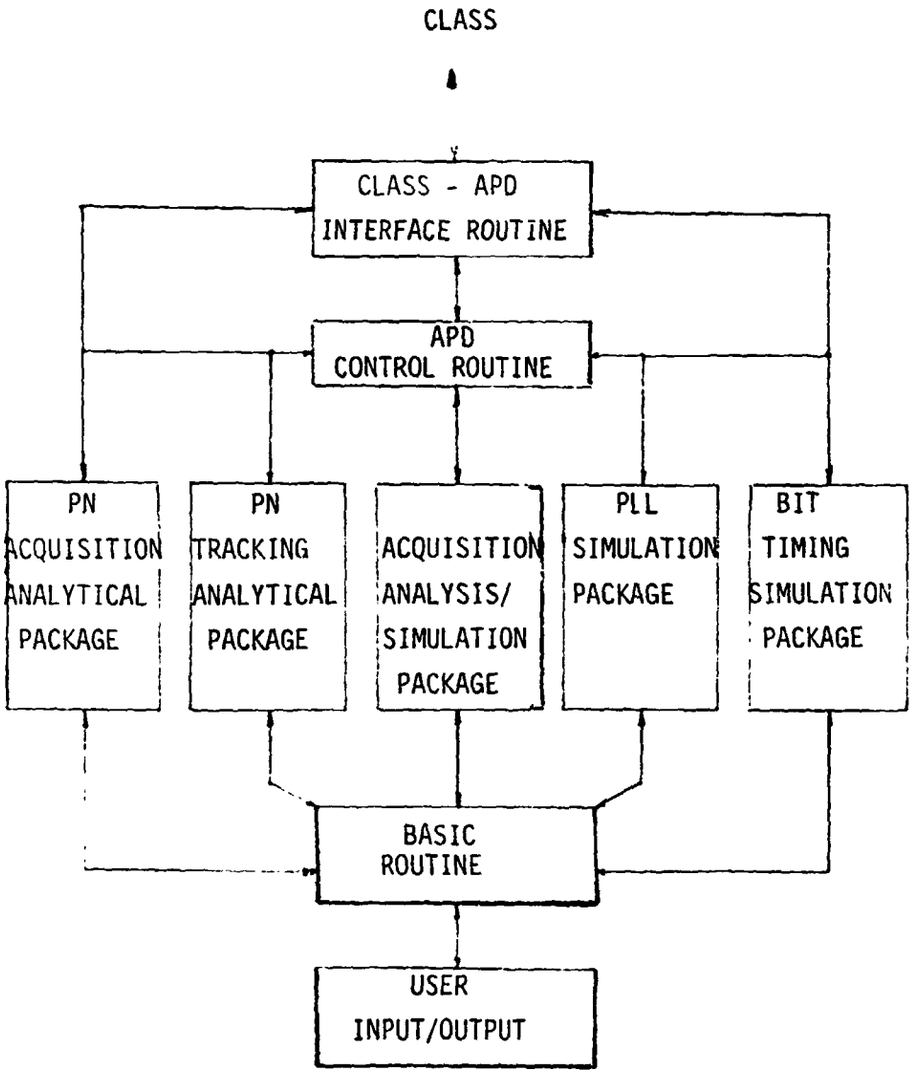

Figure D.1. Current Architecture of the AIRS Demonstration Program (ADP).

routines referring to those used in more than one configurations within one subsystem and/or in several subsystems. Detailed architectures for the PN acquisition system are shown in Fig. D.2 and Fig. D.3. The PLL and bit sync simulation package are discussed in Appendix E.

In order that the PAD be able to communicate with and thus utilize the CLASS an interface routine is included.

D.3 Properties and Parameters

D.3.1 The Acquisition Subsystem

There are fourteen system parameters of the Acquisition Subsystem to ve specified:

(1) C/N_0 (dB-Hz)

(2) Data format (NRZ or bi-phase)

(3) Data rate (kHz)

(4) Code rate (M chips/sec)

(5) I and Q channel power ratio G, $0 < G < 1$

(6) Designed false alarm rate

(7) Search step size (chip)

(8) Doppler loss (dB)

(9) Data Transition loss (dB)

(10) Number of Doppler bins

(11) Number of chips per Doppler bin

(12) Length of the CCD PNMF (chips)

(13) Number of the noncoherent integrations (1st stage)

(14) Integration time (K chips) fo the 2nd stage test, three options to be chosen from:

(1) Receiver configuration (SSP or SPS)

(2) Optimization with respect to parameter 13 above

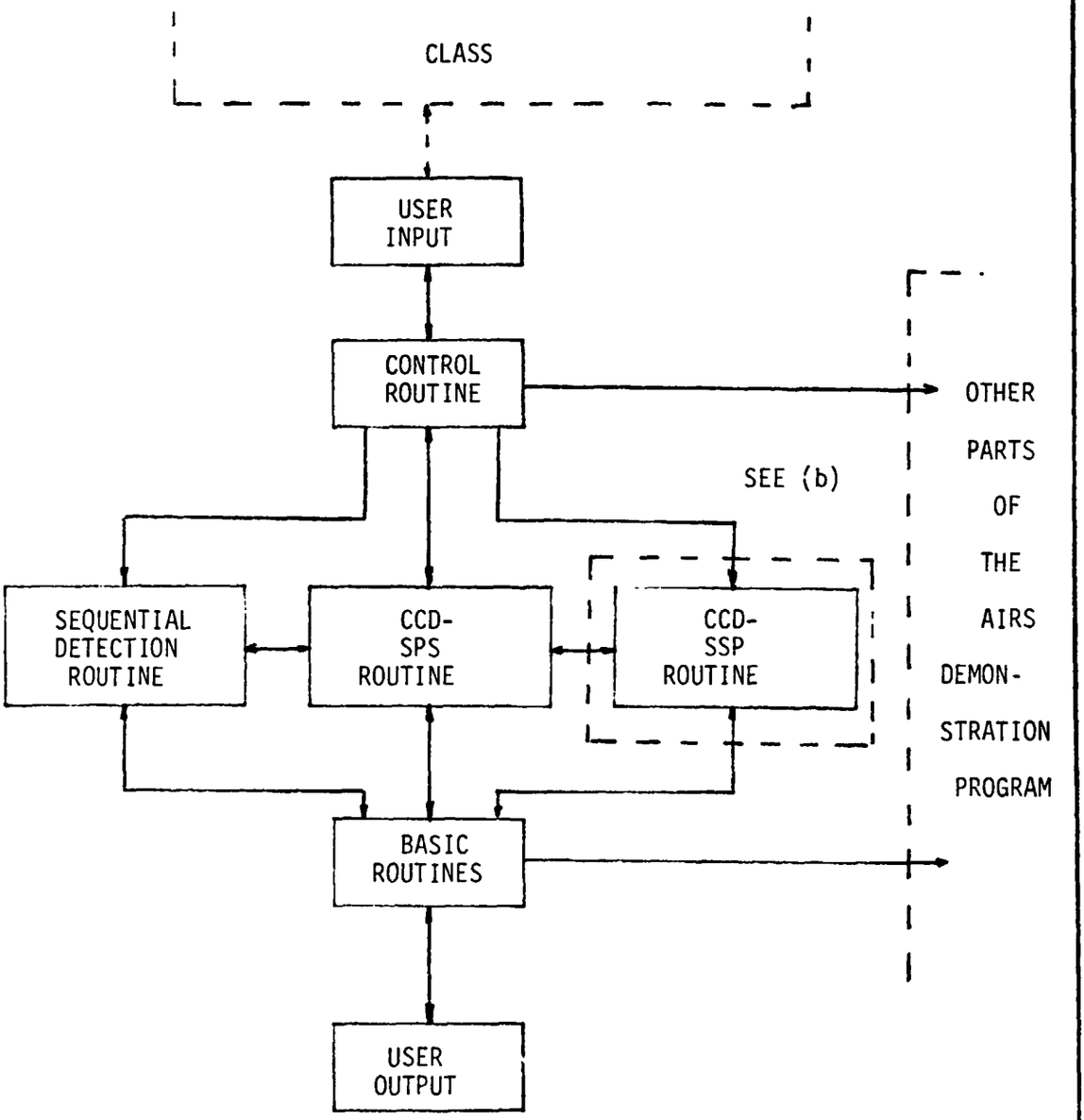

Fig. D.2. Current Software Architecture.

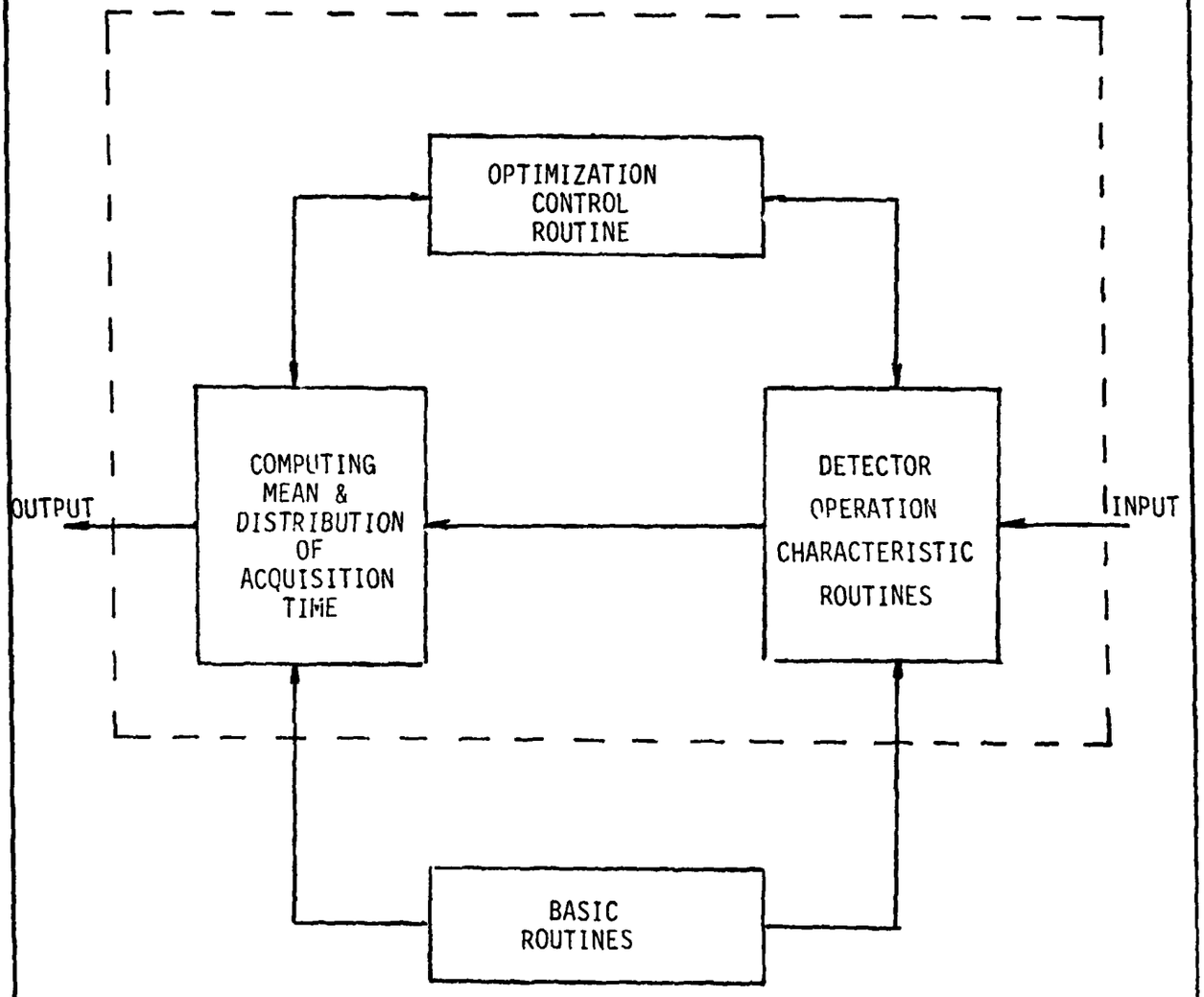

Fig. D.3. Current Software Architecture

(3) Performance criterion - minimizing the mean acquisition time or, minimizing the time for 90% acquisition probability.

Note that the minimization is carried out by choosing the optimal detection (& false alarm) probabilities of both stages. For the second criterion, a 90% detection probability per cell is assumed. Besides the evaluation of the acquisition time the APD also offer operation characteristic analysis for various detector structures.

D.3.2 Code Tracking Subsystem

Though a 2-DDL is proposed and found to be superior to other existing code tracking loops, the performances of DDL and TDL are also presented. The effects of the pre-despreading RF filtering and IF filtering in both I & Q arms of the tracking loop are considered and modeled as signal energy degradations. Lock detector is part of the code tracking system and its performance evaluation is included in the task of APD. System parameters pertaining to the code tracking are summarized as follows.

(1)-(6): same as (1)-(5) & (7) of the acquisition subsystem.

(7) Loop bandwidth (Hz)

(8) Cut-off frequency (normalized by data rate) of the arm BPF

(9) Chip time - bandwidth product of the RF filter

(10) Phase nonlinearity of the RF filter

(11) Designed false alarm rate for the lock detector (LD)

(12) Integration time (chips) for LD.

Two options do exist, namely,

(1) Loop configuration (2-DDL, DDL or TDL)

(2) Choice of the IF filter (ideal BPF or 3-pole Butterworth).

Code phase jitter, normalized mean slip time and mean pull-in time for the 2nd order loop are calculated, where a 2 dB degradation from the 1st order loop in jitter square is added to the 2nd order loop. One-delta loops, i.e., one chip delay between early and late gates, and zero original code phase offset are assumed in all computations.

D.3.3 The Frequency Acquisition Subsystem

A digital 2-channel, multiple-stage, 1st order automatic frequency loop is investigated. The maximum number of stages in a AGC loop is limited to be three. Besides (1)-(3) and (5) in D.3.1, there are eleven parameters to be determined, namely,

(5) Original frequency error (Hz)

(6) Number of samples per update (N)

(7) Number of upoates per bit time for the 1st, 2nd & 3rd stage

(8) Loop bandwidth (Hz) for the 1st, 2nd & 3rd stages

(9) Switch time (sec) from the 1st (2nd) to the 2nd (3rd) stage

(10) Seed (a double-precision real) for random number generator.

To control the frequency error trajectory to be plotted, three parameters are added:

(11) Number of points (at most 100) in a curve

(12) Sampling interval, i.e., number of updates between 2 points

(13) Plot-starting time (sec).

By using proper values in (11)-(13), we can examine closely both "global" and "local" behaviors of the frequency acquisition process. Parameter (10) is used to generate different and independent trajectories by entering different values.

D.4 Accessing and Running APD

To access the APD simply type the system command

*RERUNRFI/G AIRS

and APD will respond with a series of options-and-parameters sections to guide the user, in a page by page procedure to obtain the numerical results he or she needs. To terminal APD, a user needs only to choose the "ENDING (APD, OR PN ACQUISITION, etc.) ANALYSIS" command in the control routine. The application of the APD in designing an optimal system f . s a standard recursive process as shown in Fig. D.4. All the related system parameters are determined in at most three sections, where each section is designed in such a way that it will fit one screen. T facilitate the usage of APD, all system parameters are defaulted to some values and users can have options to change or not change any of them for their design purpose. For a better understanding of the APD we include below a sample run of it.

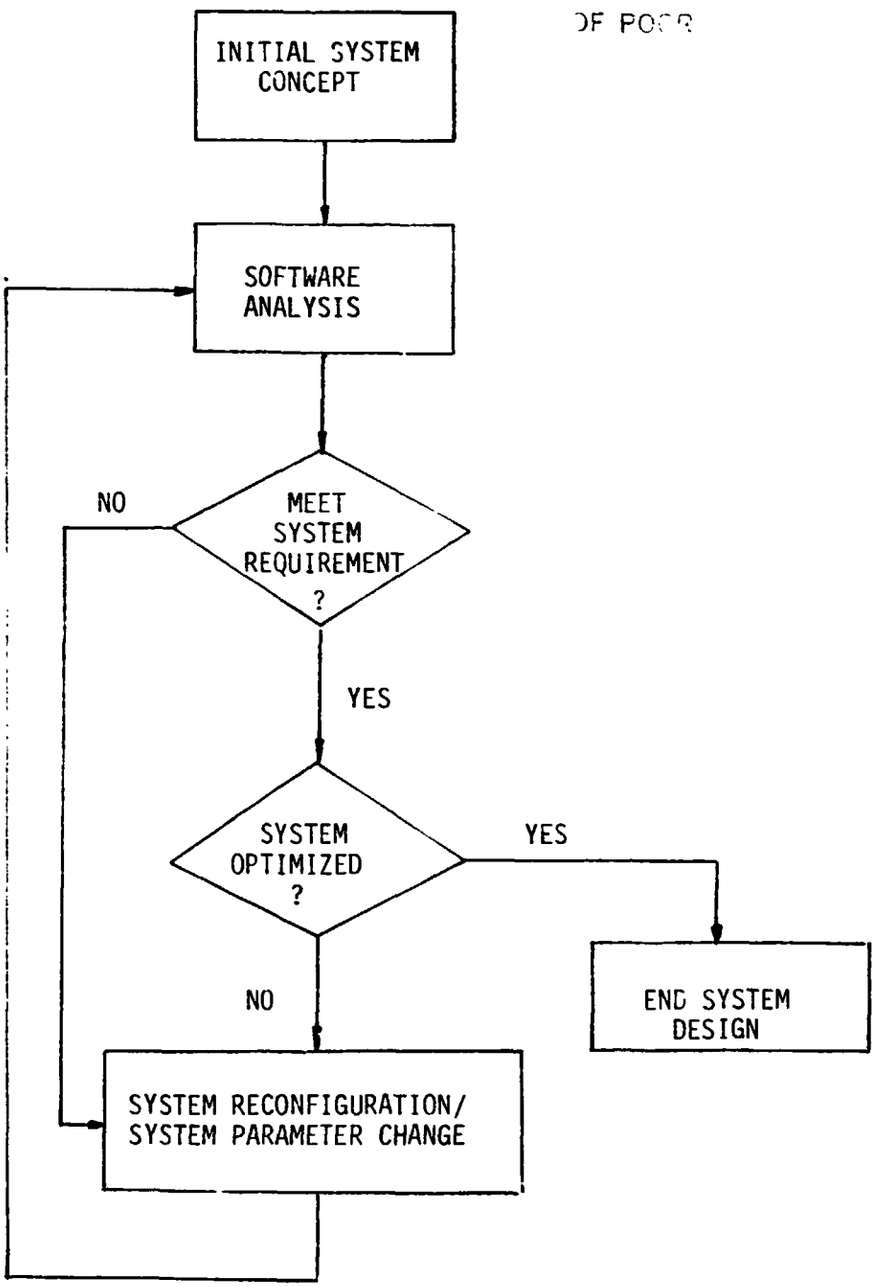

Fig. D.4. Design Procedure by Using SAT

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```
AIRS DEMONSTRATION PROGRAM
(ADP)

VERSION 1.0

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THE CURRENT DATA CHARACTERISTICS ARE :

1.  PN USE =  0
    0 => I&Q (DG1-1,2)
    1 => I ONLY (DG1-3)
    2 => NONE (DG2)
2.  SYMBOL FORMAT(OR BIT FORMAT IF UNCODED) =  1
    0 => BI-PHASE
    1 => NRZ
    2 => UNKNOWN
3.  MODULATION FORMAT =  3
    0 => BPSK (DG2)
    1 => SQPSK (DG2)
    2 => 8PSK*2 (DG1)
    4 => UNKNOWN (DG2)
4.  CODE RATE =  1
    0 => UNCODED
    1 => RATE 1/2
    2 => RATE 1/3
    3 => UNKNOWN
6.  I BIT RATE(KHZ) =     1
7.  Q BIT RATE(KHZ) =     1
8.  Q/I POWER RATIO (BETWEEN 1 & 4) =   4
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
? 1
ENTER NEW VALUE FOR PARAMETER  1
? 1
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
? 0
THE CURRENT DATA CHARACTERISTICS ARE :
```

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```
1.  PN USE =  1
    0 => I&Q (DG1-1,2)
    1 => I ONLY (DG1-3)
    2 => NONE (DG2)
*.  SYMBOL FORMAT(OR BIT FORMAT IF UNCODED) =  1
    0 => BI-PHASE
    1 => NRZ
    2 => UNKNOWN
3.  MODULATION FORMAT =  3
    0 => BPSK (DG2)
    1 => SQPSK (DG2)
    3 => BPSK*2 (DG1)
    4 => UNKNOWN (DG2)
4.  CODE RATE =  1
    0 => UNCODED
    1 => RATE 1/2
    2 => RATE 1/3



    3 => UNKNOWN
5.  I BIT RATE(KHZ) =     1
6.  Q BIT RATE(KHZ) =     1
7.  Q/I POWER RATIO (BETWEEN 1 & 4) =   4

ENTER 1 FOR PN ACQUISITION SUBSYSTEM ANALYSIS
      2 FOR PN TRACKING SUBSYSTEM ANALYSIS
      3 FOR FREQUENCY ACQUISITION LOOP ANALYSIS & SIMULATIONS(A&S)
      4 FOR BIT SYNC A&S
      5 FOR PLL A&S

:1
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ACQUISITION SUBSYSTEM ANALYSIS

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```
ENTER 1 FOR ACQUISITION TIME EVALUATION
      2 FOR RCVR. OPERATION CHARACTERISTIC INVESTIGATION

?1
THE FOLLOWING IS A LIST OF PARAMETERS TO BE DETERMINED
1.  INPUT C/NO(DB) =   36.5
4.  PN CODE RATE(M-CHIPS/SEC.) = 3.00
5. ACQUISITION ALGORITHM = 2
      1 => SPS(SERIAL SEARCH)
      2  => SSP(PARALLEL SEARCH)
6.  DESIGN FALSE ALARM RATE = 0.10D-04
7.  SEARCH STEP SIZE(CHIP) = .50
8.  DOPPLER LOSS(DB) = .40
9.  DATA TRANSMISSION LOSS(DB) = .20
10. # OF DOPPLER BINS = 3
11. # OF CHIPS PER DOPPLER BIN = .38D+04
16. # OF NONCOH. INTEG. FOR THE CCD DETECTOR =  500
17. LENGTH OF CCD PNMF(CHIPS) =  511
18. INTEGRATION TIME(K-CHIPS) FOR THE 2ND STAGE TEST =  100.
19. AUTO-OPTIMIZATION ON THE 2ND STAGE TEST = 2
      1  =>  YES
      2  =>  NO
20. PERFORMANCE CRITERION = 1
      1  =>  MIN. THE MEAN ACQUSITION TIME
      2  =>  MIN. THE TIME FOR 90% ACQUISITION
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
?18
ENTER NEW VALUE FOR PARAMETER 18
?450
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
?19
ENTER NEW VALUE FOR PARAMETER 19
?1
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
?16
ENTER NEW VALUE FOR PARAMETER 16
?400
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
?0
```

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THE CURRENT ACQ. SUBSYSTEM PARAMETERS ARE :

```
 1.  INPUT S/NO(DB) =   36.5
 2.  PN CODE RATE(M-CHIPS/SEC.) = 3.00
 3. ACQUISITION ALGORITHM = 2
       1 => SPS(SERIAL SE ARCH)
       3  => SSP(PARALLEL SEARCH)
 4.  DESIGN FALSE ALARM RATE = 0.10D-04
 5.  SEARCH STEP SIZE(CHIP) = .50
 6.  DOPPLER LOSS(DB) = .40
 7.  DATA TRANSMISSION LOSS(DB) = .20
 8. # OF DOPPLER BINS = 3
 9. # OF CHIPS PER DOPPLER BIN = .38D+04
10. # OF NONCOH. INTEG. FOR THE CCD DETECTOR =  600
11. LENGTH OF CCD PNMF(CHIPS) =  511
12. INTEGRATION TIME(K-CHIPS) FOR THE 2ND STAGE TEST =  450.
13. AUTO-OPTIMIZATION ON THE 2ND STAGE TEST = 1
       1  =>  YES
       2  =>  NO
20. PERFORMANCE CRITERION = 1
       1  =>  MIN. THE MEAN ACQUSITION TIME
       2  =>  MIN. THE TIME FOR 90% ACQUISITION
ENTER 1 FOR PRINTING OUT RESULTING PERFORMANCE
      2 FOR TABULATED PERFORMANCE VS. PARAMETER
>1
```

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PERFORMANCE WITH THE ABOVE SPECIFICATION CAN BE SUMMARIZED

AS FOLLOWS.

```
 PD =  0.59529D+00  WHEN T  = 0.24308D+01 SEC.
 PD =  0.83621D+00  WHEN T  = 0.48615D+01 SEC.
 PD =  0.93371D+00  WHEN T  = 0.72922D+01 SEC.
 PD =  0.97317D+00  WHEN T  = 0.97228D+01 SEC.
 PD =  0.98914D+00  WHEN T  = 0.12154D+02 SEC.
 PD =  0.99561D+00  WHEN T  = 0.14584D+02 SEC.
 PD =  0.99822D+00  WHEN T  = 0.17015D+02 SEC.
 PD =  0.99928D+00  WHEN T  = 0.19446D+02 SEC.
 PD =  0.99971D+00  WHEN T  = 0.21876D+02 SEC.
 PD =  0.99988D+00  WHEN T  = 0.24307D+02 SEC.
 PD =  0.99995D+00  WHEN T  = 0.26738D+02 SEC.
 PD =  0.99998D+00  WHEN T  = 0.29168D+02 SEC.
 PD =  0.99999D+00  WHEN T  = 0.31599D+02 SEC.
 PD =  0.10000D+01  WHEN T  = 0.34030D+02 SEC.
 PD =  0.10000D+01  WHEN T  = 0.36460D+02 SEC.
MEAN ACQ. TIME= 0.40834D+01 SEC.
DETEC. PROB.= 0.59529D+00
DWELL TIME ON THE 2ND STAGE TEST= 0.15067D+00 SEC.
FALSE-ALARM PROB.(1ST STAGE)= 0.40470D+00
FALSE-ALARM PROB.(2ND STAGE)= 0.24709D-04
FALSE-ALARM PROB.= 0.10000D-04
DETEC. PROB.(1ST STAGE)= 0.59529D+00
DETEC. PROB.(2ND STAGE)= 0.10000D+01
```

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```
ENTER 1 FOR ENDING ANALYSIS, 2 FOR CONTINUATION


?

*****************************************************************

THE CURRENT DATA CHARACTERISTICS ARE :



1.  PN USE =  1
    0 => BOTH (DG1-1,2)
    1 => 1 ONLY (DG1-3)
    2 => NONE (DG2)
2.  SYMBOL FORMAT(OR BIT FORMAT IF UNCODED) =  1
    0 => BI-PHASE
    1 => NRZ
    2 => UNKNOWN
3.  MODULATION FORMAT =  3
    0 => BPSK (DG2)
    1 => SQPSK (DG2)
    3 => APSK*2 (DG1)
    4 => UNKNOWN (DG2)
4.  CODE RATE =  1
    0 => UNCODED
    1 => RATE 1/2
    2 => RATE 1/3
    3 => UNKNOWN
5.  I BIT RATE(KHZ) =     1
6.  Q BIT RATE(KHZ) =     1
8.  Q/I POWER RATIO (BETWEEN 1 & 4) =   4
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
?

ENTER 1 FOR PN ACQUISITION SUBSYSTEM ANALYSIS
      2 FOR PN TRACKING SUBSYSTEM ANALYSIS
      3 FOR FREQUENCY ACQUISITION LOOP ANALYSIS & SIMULATIONS(A&S)
      4 FOR BIT SYNC A&S
      5 FOR PLL A&S

?2
```

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```
PN TRACKING SUBSYSTEM ANALYSIS

THE FOLLOWING IS A LIST OF PARAMETERS TO BE DETERMINED
1.  INPUT C/NO(DB) =   36.5
2.  DATA FORMAT (1 FOR NRZ, 2 FOR BI-PHASE) = 1
3.  DATA RATE(KHZ) = 1.00
4.  PN CODE RATE(M-CHIPS/SEC.) = 3.00
5.  SEARCH STEP SIZE(CHIP) = .50
6.  LOOP BANDWIDTH(HZ) =  0.5
7.  CHOICE OF LOOPS(# OF CHANNELS) = 4
      1 => TAU-DITHER LOOP
      2 => DOUBLE &DITHER LOOP(DDL)
      4 => 2-CHANNEL DDL
17. CHOICE OF BPF = 2
      1 => IDEAL BPF
      2 =>  3-POLE BUTTERWORTH
28. CUT-OFF FREQ.(DIVIDED BY DATA RATE) OF THE BPF = 2.0
29. FREQ.(DOPPLER) OFFSET(HZ) =  0.0
31. PHASE NONLINEARITY OF THE PRE-DESPREADING FILTER = 0.10
32. TIME(CODE CHIP)-BW(PREDESPEADING FILTER) PRODUCT =  2.0
33. INTEGRATION TIME(CHIPS) FOR LD = 0.100D+06
34. DESIGNED FALSE ALARM RATE FOR LD = 0.100D-07
41. I:Q POWER RATIO (G,0<G<=1) = 0.250
ENTER THE PARAMETER NUMBER TO BE REDEFINED
ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE



ENTER 1 FOR PRINTING OUT RESULTING PERFORMANCE
      2 FOR TABULATED PERFORMANCE VS. PARAMETER
1

PERFORMANCE WITH THE ABOVE SPECIFICATION CAN BE SUMMARIZED
AS FOLLOWS
SIGNAL DEGRADATION DUE TO BPF = -0.94 DB
CORELATION LOSS = -1.37 DB


CODE PHASE JITTER(%) = 1.069  & 1.199 (2ND ORDER LOOP)
NORMALIZED MEAN SLIP TIME = 0.340D+02 & 0.340D+02 (2ND ORDER
MEAN PULL-IN TIME = 0.983D-01 & 0.111D+00 (2ND ORDER LOOP)
DETECTION PROBABILITY FOR LD = 0.973E+00
```

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```
 ENTER 1 FOR ENDING ANALYSIS, 2 FOR CONTINUATION

>2

 ************************************************************************

 THE CURRENT DATA CHARACTERISTICS ARE :

 1.  PN USE =  1
     0 => I&Q (DG1-1,2)
     1 => I ONLY (DG1-3)
     2 => NONE (DG2)
 2.  SYMBOL FORMAT(OR BIT FORMAT IF UNCODED) =  1
     0 => BI-PHASE
     1 => NRZ
     2 => UNKNOWN
 3.  MODULATION FORMAT =  3
     0 => BPSK (DG2)
     1 => SQPSK (DG2)
     3 => BPSK*2 (DG1)
     4 => UNKNOWN (DG2)
 4.  CODE RATE =  1
     0 => UNCODED
     1 => RATE 1/2
     2 => RATE 1/3
     3 => UNKNOWN
 6.  I BIT RATE(KHZ) =      1
 7.  Q BIT RATE(KHZ) =      1
 8.  Q/I POWER RATIO (BETWEEN 1 & 4) =    4
 ENTER THE PARAMETER NUMBER TO BE REDEFINED
 ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
>0

 ENTER 1 FOR PN ACQUISITION SUBSYSTEM ANALYSIS
       2 FOR PN TRACKING SUBSYSTEM ANALYSIS
       3 FOR FREQUENCY ACQUISITION LOOP ANALYSIS & SIMULATIONS(A&S)
       4 FOR BIT SYNC A&S
       5 FOR PLL A&S

>3
```

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```
FREQUENCY ACQUISITION LOOP ANALYSIS


THE FOLLOWING IS A LIST OF PARAMETERS TO BE DETERMINED
 1.  INPUT C/NO(DB) =   36.5
 70. FREQUENCY ERROR (HZ) = 0.420D+04
 71. # OF SAMPLES PER UPDATE =  10
 72. # OF UPDATE / BIT TIME(1ST STAGE) =  17
 73. LOOP BW (HZ,1ST STAGE) =  6.400
 74. # OF UPDATES /BIT TIME(2ND STAGE) =   5
 75. LOOP BW(HZ) FOR THE 2ND(INTERMIDIATE) STAGE =  2.974
     (SET TO 0 IF ONLY 2 STAGES ARE USED)
 76. SWITCH TIME(SEC.) FROM 1ST TO 2ND STAGE = 0.200
 77. # OF UPDATE / BIT TIME FOR THE FINAL(3RD) STAGE =   5
     (SET TO 0 IF ONE-STAGE FAL IS USED)
 78. LOOP BW(HZ) FOR THE 3RD STAGE =  0.360
     (SET TO  0 IF ONLY ONE STAGE IS USED)
 79. SWITCH TIME(SEC.) FROM 2ND TO FINAL STAGE =  0.600
 80. # OF POINTS(< 100) IN A CURVE =  50.
 81. SAMPLING INTERVAL(# OF UPDATES BETWEEN TWO POINTS) =  100.
 82. START-PLOTTING TIME(SEC.) =  0.000
 83. SEED FOR RANDOM GENERATOR(1.D3<  <1.D16) =  0.371D+11
 ENTER THE PARAMETER NUMBER TO BE REDEFINED
 ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
>1
 ENTER NEW VALUE FOR PARAMETER  1
>38.
 ENTER THE PARAMETER NUMBER TO BE REDEFINED
 ENTER 0 IF NO PARAMETER CHANGE IS TO BE MADE
>0
```

```
   THE CURRENT FAL. SUBSYSTEM PARAMETERS ARE :

 1.   INPUT C/NO(DB) =    38.0
 70.  FREQUENCY ERROR (HZ) = 0.420D+04
 71.  # OF SAMPLES PER UPDATE =   10
 72.  # OF UPDATE / BIT TIME(1ST STAGE) =   17
 73.  LOOP BW (HZ,1ST STAGE) =   6.400
 74.  # OF UPDATES /BIT TIME(2ND STAGE) =    5
 75.  LOOP BW(HZ) FOR THE 2ND(INTERMIDIATE) STAGE =   2.974
      (SET TO 0 IF ONLY 2 STAGES ARE USED)
 76.  SWITCH TIME(SEC.) FROM 1ST TO 2ND STAGE = 0.200
 77.  # OF UPDATE / BIT TIME FOR THE FINAL(3RD) STAGE =  5
      (SET TO 0 IF ONE-STAGE FAL IS USED)
 78.  LOOP BW(HZ) FOR THE 3RD STAGE =   0.360
      (SET TO  0 IF ONLY ONE STAGE IS USED)
 79.  SWITCH TIME(SEC.) FROM 2ND TO FINAL STAGE =   0.600
 80.  # OF POINTS(< 100) IN A CURVE =   50.
 81.  SAMPLING INTERVAL(# OF UPDATES BETWEEN TWO POINTS) =   100.
 82.  START-PLOTTING TIME(SEC.) =   0.000
 83.  SEED FOR RANDOM GENERATOR(1.D3<  <1.D16) =   0.371D+11
 ENTER 1 FOR PRINTING OUT RESULTING PERFORMANCE
       2 FOR TABULATED PERFORMANCE VS. PARAMETER
?1

 SIMULATION RESULTS WITH THE ABOVE SPECIFICATION CAN BE SUMMARIZED
 AS FOLLOWS.
```

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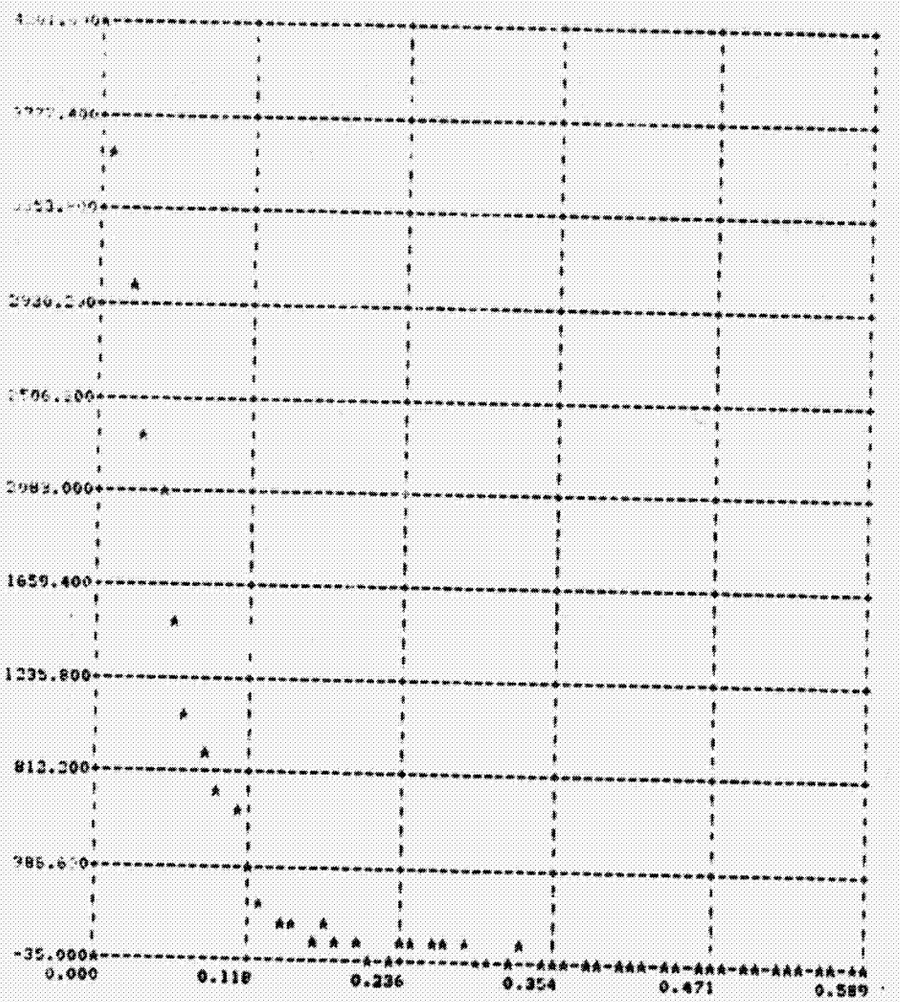
FREQUENCY ERROR TRAJECTORY (SIMULATION):



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```
 ADD. TIME = 0.0505
 FREQ. JITTER(MODE 2,NRZ) = 0.115E+03 ;(OTHERWISE) = 0.115E+03
 DETECTION PROB. FOR LD. = 0.949E+00(MODE 2,NRZ) & 0.949E+00


 ***************************************************************

 ENTER 1 FOR ENDING ANALYSIS, 2 FOR CONTINUATION

>1
 END OF FREQUENCY ACQUISITION JDP ANALYSIS


 ***************************************************************

 ENTER 1 FOR END OF ADP
       2 FOR CONTINUATION
>1


 END OF ADP
IT'S BEEN NICE WORKING WITH YOU...
```

APPENDIX E

DATA-AIDED LOOP SIMULATION

E.1 Simulation Software Organization

The data-aided loop simulation software is organized into eight main subroutines as shown in Figure E.1. These subroutines are modified slightly to accomodate different types of modulations. The main program handles the input question and answer session whose purpose is to define the simulation parameters. The main program also controls the flow of the program execution. The main loop in Figure E.1 starts with SAMPLE, which generates noise-corrupted signal samples. The sampling instants are determined by the timing error of the loop at that point in time. The phase error of the loop is used to rotate these samples. The number of samples generated correspond to a symbol time. The data symbol as well as the noise samples are generated using pseudo random techniques. Therefore, the DAL is a strict Monte Carlo simulation.

The generated samples are processed by DSP to detect the symbol and to generate the dynamic bit sync error and the dynamic carrier recovery loop error. The dynamic errors are filtered by FIL to control the carrier and bit synth synthesizers modeled by SYNTH. The SYNTH routine computes the current phase estimate and the sampling clock estimate. These estimates are used in the DOPPLR routine, which models the Doppler profile, to generate the phase and timing error for the next call of SAMPLE. This completes a simulation cycle.

The five routines SAMPLE, DSP, FIL, SYNTH and DOPPLR are designed to duplicate the AIRS functions on a one-to-one basis. Hence, the software can be used to realistically model the AIRS operation and

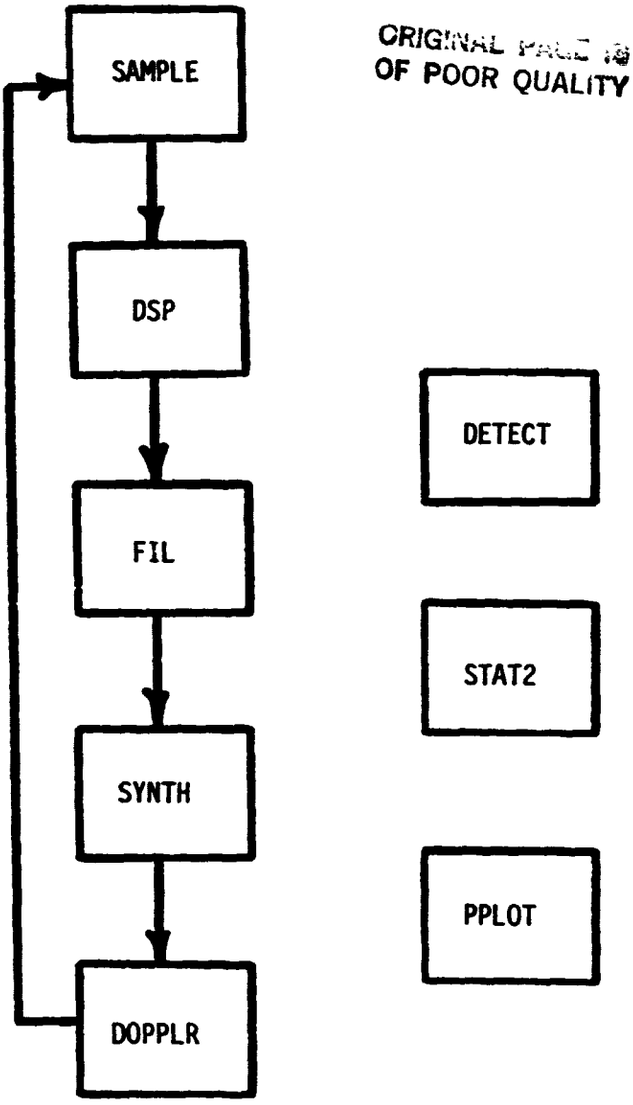


Figure E.1. Simulation Flow Diagram.

predict its performance.

Aside from these routines, there are three additional ones that are used to perform housekeeping functions. Subroutine DETECT keeps track of the SNR estimate and the BER. STAT2 keeps track of the means and variances of the phase and timing jitter. Finally, PPLOT plots the timing and phase error transients during acquisition.

E.2 Sampled Signal Model

The incoming signal is represented by

$$s(t) = \sqrt{2P_1}\, d_1(t) \cos \omega_0 t + \sqrt{2P_2}\, d_2(t) \sin \omega_0 t$$

where $d_1(t)$ and $d_2(t)$ represent unity amplitude (± 1) baseband symbol sequences with data rates $1/T_1$ and $1/T_2(t)$ respectively. This discussion assumes that NRZ formats are being used and can be easily modified for Manchester format. The received signal is a noise-corrupted version of s(t) given by

$$r(t) = s(t) + n(t)$$

where n(t) is an additive white Gaussian noise (AWGN) with one-sided spectral density N_0 watts/Hz. Figure E.2 shows the front end processing of the AIRS receiver used to convert the received signal to digital samples. The received signal is first converted to its I,Q baseband components via the coherent demodulation process. The phase tracking error of the local carrier recovery is modeled by the phase error ϕ. The I-Q baseband components, ignoring the double frequency terms, is given by

$$r_I(t) = \sqrt{P_1}\, d_1(t) \cos \phi + \sqrt{P_2}\, d_2(t) \sin \phi + n_I(t)$$

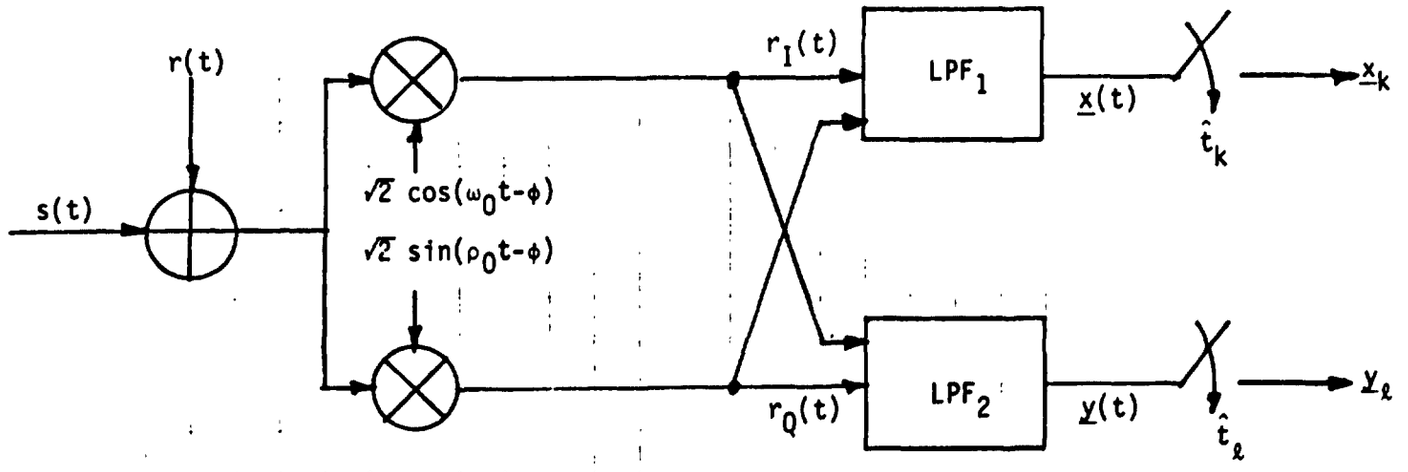
$$r_Q(t) = -\sqrt{P_1}\, d_1(t) \sin \phi + \sqrt{P_2}\, d_2(t) \cos \phi + n_Q(t)$$

where $n_I(t)$ and $n_Q(t)$ are independent baseband AWGN processes with one-sided spectral density N_0 watt/Hz. The baseband processes are lowpass filtered and sampled according to the local clocks $\hat{t}_k$ and $\hat{t}_\ell$. The nominal clock rates of $\hat{t}_k$ and $\hat{t}_\ell$ are integer multiples of the bit rate given by N_1/T_1 and N_2/T_2.

In Figure E.2, the vectors $\underline{x}(t)$ and $\underline{y}(t)$ denote the two components of the lowpass filter outputs for $r_I(t)$ and $r_Q(t)$. Similarly each of the vector samples $\underline{x}_y$ and $\underline{y}_k$ has 2 components.

For convenience, the lowpass filter is modeled in the simulation by a moving window integrator as shown in Figure E.3. The gain in front of the integrator is selected so that the signal samples $\underline{x}_k$ are nominally of unity amplitude level. The lowpass filter for $r_Q(t)$ is analogous. When the bit sync is perfect, the local sampling clock coincides with the transmit data clock (defined by the transition insta··) every N_1 samples. If there is a bit sync error $\varepsilon = t-\hat{t}$, then some the samples will not be of unity amplitude as shown in the last example in Figure E.3. In this example, the local clock leads the transmit clock so that $\varepsilon < 0$.

The components of the vector samples $\underline{x}_k$ and $\underline{y}_\ell$ are given by



$$s(t) = \sqrt{2P_1}\, d_1(t) \cos \omega_0 t + \sqrt{2P_2}\, d_2(t) \sin \omega_0 t$$

$$r_I(t) = \sqrt{P_1}\, d_1(t) \cos \phi + \sqrt{P_2}\, d_2(t) \sin \phi + n_I(t)$$

$$r_Q(t) = -\sqrt{P_1}\, d_1(t) \sin \phi + \sqrt{P_2}\, d_2(t) \cos \phi + n_Q(t)$$

Figure E.2. Signal Model.

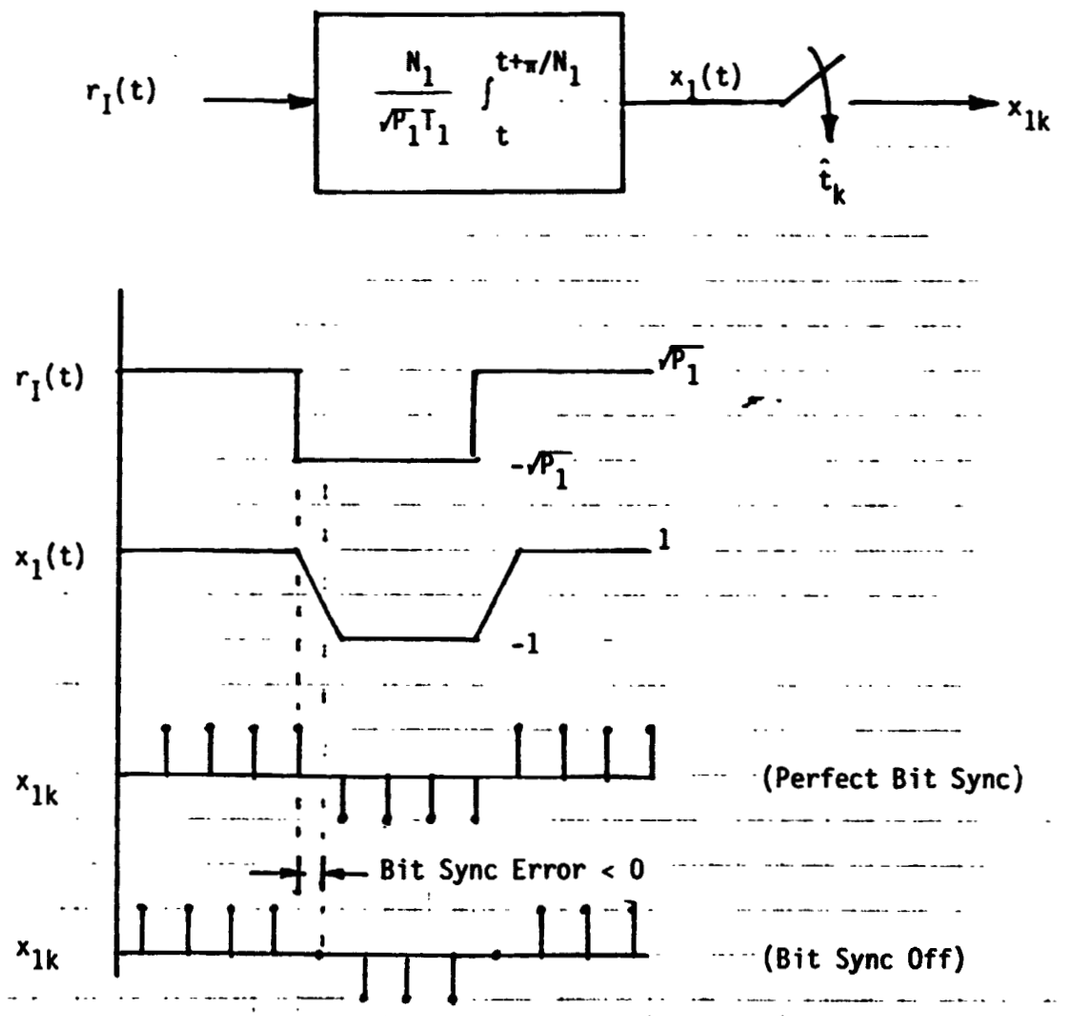


Figure E.3. Sampling Model. (N_1=4, ϕ=0, n(t)=0)

$$x_{1k} = \tilde{d}_{1k} \cos\phi + \sqrt{P_2/P_1}\,\tilde{d}_{2k} \sin\phi + \tilde{n}_{Ik}$$

$$x_{2k} = -\tilde{d}_{1k} \sin\phi + \sqrt{P_2/P_1}\,\tilde{d}_{2k} \cos\phi + \tilde{n}_{Qk}$$

$$y_{1\ell} = -\sqrt{P_1/P_2}\,\bar{d}_{1\ell} \sin\phi + \bar{d}_{2\ell} \cos\phi + \bar{n}_{Q\ell}$$

$$y_{2\ell} = \sqrt{P_1/P_2}\,\bar{d}_{1\ell} \cos\phi + \bar{d}_{2\ell} \sin\phi + \bar{n}_{I\ell}$$

where

$$\tilde{d}_{ik} = \frac{N_1}{T_1} \int_{\hat{t}_k}^{\hat{t}_k+N_1/T_1} d_i(t)dt$$

$$\bar{d}_{i\ell} = \frac{N_2}{T_2} \int_{\hat{t}_\ell}^{\hat{t}_\ell+N_2/T_2} d_i(t)dt$$

for i=1,2. The noise samples are Gaussian with zero means and variances given by

$$E[\tilde{n}_{Ik}^2] = E[\tilde{n}_{Qk}^2] = (N_1/2)(P_1T_1/N_0)^{-1}$$

$$E[\bar{n}_{Q\ell}^2] = E[\bar{n}_{I\ell}^2] = (N_2/2)(P_2T_2/N_0)^{-1}$$

The sample pair $(\tilde{n}_{Ik},\tilde{n}_{Qk})$ is independent as well as $(\bar{n}_{Q\ell},\bar{n}_{I\ell})$. The sample pairs $(\tilde{n}_{Ik},\bar{n}_{I\ell})$ and $(\tilde{n}_{Qk},\bar{n}_{Q\ell})$ are correlated. Notice that the samples for the filtered data waveforms are normalized to unity as shown in Figure E.3.

E.3 Loop Parameters

In the DAL simulation, the loops are characterized by its order and

its one-sided loop noise bandwidth. In a digital receiver, the loop action can be described by a difference equation*

$$\phi_{k+1} = \phi_k - F(z)e_k \qquad \text{(E-1)}$$

Presently, we have ignored the Doppler offset as it has no bearing on the loop bandwidth characterization. In this equation, F(z) describes the action of the loop filter and is given in z-operator form as

$$F(z) = G_1 + \frac{G_2}{1-z^{-1}} + \frac{G_3}{(1-z^{-1})^2}$$

For a first-order loop, $G_2 = G_3 = 0$. For a second-order loop, $G_3 = 0$. A third-order loop has all nonzero gains. In the simulation, the filtering is performed in the subroutine FIL. The error e_k is generated in the subroutine DSP and is normalized so that $E[e_k] \sim \phi_k$ while tracking.

To determine the loop bandwidth, noticed that (E-1) approximated by a differential equation

$$\dot{\phi} = -(G_1/T + G_2/T^2 s + G_3/T^3 s^2)\phi \qquad \text{(E-2)}$$

where T is the time between update of the loop phase error, typically equal to a symbol time, and the correspondence $(1-z^{-1}) = sT$ is used. The loop bandwidth for the analog loop described by (E-2) is well known and is summarized in Table E-I. Loop bandwidths used in the simulation

*We concentrate presently on the carrier-recovery loop. The bit sync will be treated later on.

Table E.1. Filter Parameters in Terms of One-Sided Loop Noise Bandwidth B_L. (For a Second-Order Loop, the Damping Ratio $\zeta = 0.707$ is Used. For a Third-Order Loop, the Wiener Optimum Filter is Used.)

LOOP-ORDER	FILTER PARAMETERS
1	$G_1 = 4B_LT$
2	$G_1 = \frac{8}{3} B_LT$ $G_2 = \frac{1}{2} (\frac{8}{3} B_LT)^2$
3	$G_1 = \frac{4}{3} B_LT$ $G_2 = (\frac{4}{3} B_LT)^2$ $G_3 = \frac{1}{2} (\frac{4}{3} B_LT)^2$

is defined in this manner.

For the bit sync, the determination of the noise-bandwidth is similar except that (E-1) is replaced by the difference equation governing the normalized timing error samples

$$\lambda_{k+1} = \lambda_k - F(z)e_k \qquad \text{(E-3)}$$

The DSP routine normalizes e_k so that $E[e_k] = \lambda_k$ for small λ_k. This is defined for 50% transition density with NRZ data.

E.4 Effect of Data Modulation

For a single channel operation, i.e., data appearing only on the I or Q channel, the determination of equation (E-1) is trivial. In that case, T is either the symbol time for NRZ data or half the symbol time for Manchester-coded data. For DG2, the situation is a little complicated. If the data rates are equal and coherent, then T is the symbol time and e_k is the average of the error signal provided by the I and Q channel. For unequal data rates, the loop error signals are produced at irregular intervals. Figure E.4 illustrates this point. The DAL processes the error signal samples as they become available. Therefore, instead of (E-1) we have two simultaneous difference equations, namely,

$$\phi_{k+1} = \phi_k - F(z)e_{Ik} \qquad \text{(E-4a)}$$

$$\phi_{\ell+1} = \phi_\ell - F(z)e_{Q\ell} \qquad \text{(E-4b)}$$

where k and ℓ denotes the indexes of two different sequences of epochs in time. According to the optimum MAP estimation, the ratio of

Figure E.4 . Carrier Recovery Loop Error Signal Samples (I Channel to Q Channel Data Rate Ratio is 4:3).

$E[e_{Ik}]/E[e_{Qk}]$ must be equal to P_I/P_Q = I:Q channel power ratio. The subroutine DSP is set up to normalized e_{Ik} and e_{QK} so that $E[e_{Ik}] \sim \phi_k/[1+(P_Q/P_I)(R_Q/R_I)]$ and $E[e_{Q\ell}] \sim (P_Q/P_I)\,\phi_\ell/[1+(P_Q/P_I)(R_Q/R_I)]$ for small small errors. (We use R_Q/R_I to denote the symbol rate ratio of Q to I channel.)

We can combine (E-4b) with (E-4a) by increasing the update rate of (E-4b). Then since in one I-symbol time T, there are only R_Q/R_I parts of error signal on the average from the Q channel, we have, approximately,

$$\phi_{k+1} = \phi_k - F(z)\left[e_{Ik} + \frac{R_Q}{R_I}\, e_{Q\ell}\right] \qquad \text{(E-5)}$$

It is easy to check that the average value of the bracketed term in (E-5) is proportional to ϕ. Hence, we can use Table I to determine the loop parameters.

E.5 Sample Runs

Figures E.5 shows a typical run using the command RUN BPSK.

```
ENTER EB/N0(DB),SAMPLE/BIT,DATA RATE(BPS)
)5,8,2192
ENTER DOPPLER(HZ), DOPPLER RATE(HZ/S)
)0,765
ENTER LOOP ORDER AND BW FOR PLL
)3,70
ENTER LOOP ORDER AND BW FOR BIT SYNC
)2,34
OPTION: ENTER 1(ACQ), 2(TRACK), OR 3(BOTH)
)1
ENTER #ACQ SAMPLES((=100), INC STEP(BIT), #TRIALS
)100,3,10
ENTER 0(RANDOM DATA),1(SQ),2(ALL1),3(ALL0)
)0
ENTER INIT TIMING, PHASE ERROR(BIT,DEG), SEED
)0,0,9
```

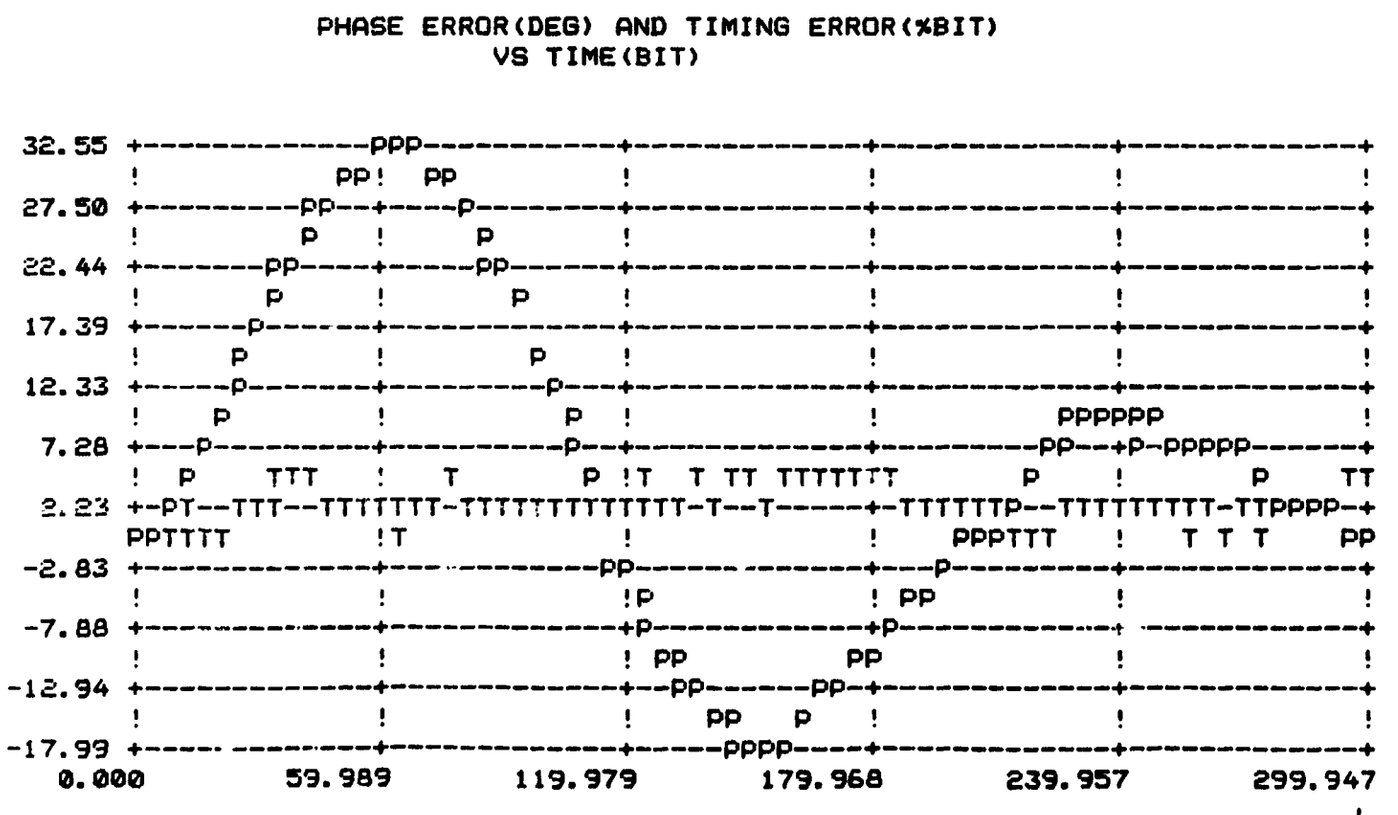


Figure E.5. A Typical Run by Using RUN BPSK.

APPENDIX F

AIRS AUTONOMOUS DOPPLER COMPENSATION

Summary

Techniques for autonomous Doppler compensation for AIRS are proposed and their performance are evaluated. A first-order compensation technique is shown to be capable of reducing the maximum Doppler offset error to less than 800 H_z during a powerflight if the Doppler compensation is applied once every second. The duration of maximum Doppler rate is also reduced from 9 sec to 1 sec. The performance can be further improved by reducing the time between Doppler compensations, T_D. An approximate relation is that the duration of maximum Doppler rate is T_D, and the maximum Doppler error is the amount of Doppler accumulated over T_D due to the Doppler rate.

1.0 Introduction

Figure 1 shows a functional diagram for the AIRS Doppler compensation scheme. During acquisition the ADPE Doppler predictions are used to control the downconverter synthesizer frequency, nominally at 335 MH_z. After the AIRS has acquired and the carrier recovery loop is in lock, the AIRS takes over the Doppler compensation. The AIRS accomplishes this as follows. First of all, the frequency of the recovered carrier is generated by the AIRS tracking unit. This recovered carrier frequency, nominally at 35 MH_z, is known. The actual

Doppler on the received SSA signal is the difference between the sum of the recovered carrier frequency and the frequency setting of the downconverter frequency synthesizer at the particular time instant, and the nominal frequency at 370 MH_z. This Doppler frequency is sampled periodically and the samples are used by the AIRS to extrapolate the Doppler frequency to the next sample point. The AIRS then uses this to control the downconverter synthesizer until the next sample is obtained. This function is performed by the downconverter synthesizer control unit and Figure 2 illustrates this technique.

2.0 Extrapolation Techniques

The problem of performing AIRS compensation can simply be stated as follows. Given a measured Doppler profile $f(t)$ between 0 and t, what is the best way to extrapolate, i.e., determine an estimate $\hat{f}(t+\tau)$ for $f(t+\tau)$ at a later time $t+\tau$? Because of practical constraints, we only wish to measure the Doppler and perform extrapolation at regular time intervals separated by T_D secs. The problem then reduces to: given f_0, f_1, ..., f_k where f_k is $f(kT_D)$, how can one predict f_{k+1}?

2.1 First and Second Order Extrapolation

In what follows, we consider two ways to perform extrapolation. The first method is exact if the Doppler profile is linear but there is a constant error if the profile is quadratic. The second method is exact if the profile is quadratic but there is a constant error term if this profile is cubic. In either case, the constant error term is proportional to T_D, the interval between Doppler measurement updates.

2.1.1 First-Order Extrapolation

The first order extrapolation is given by

$$\hat{f}_{k+1} = 2f_k - f_{k-1} \qquad (1)$$

The associated error is

$$e_{k+1} = f_{k+1} - \hat{f}_{k+1} = f_{k+1} - 2f_k - f_{k-1} \qquad (2)$$

Note that the error term (2) is the second increment of the Doppler profile. Note also that two measured Doppler samples are needed for the extrapolation.

2.1.2 Second-Order Extrapolation

The second-order extrapolation is given by

$$\hat{f}_{k+1} = 3f_k - 3f_{k-1} + f_{k-2} \qquad (3)$$

and the associated error is

$$e_{k+1} = f_{k+1} - 3f_k + 3f_{k-1} - f_{k-2} \qquad (4)$$

Notice that the error term is the third increment of the Doppler profile and three measurements are needed for the extrapolation.

3.0 Performance Examples

To see how the extrapolation techniques perform, we select an

example from the WDD dynamics profile used to test the cycle slipping performance during an uncompensated powered flight. This is shown in Figure 3 where a 765 H_z/S Doppler rate (AIRS spec maximum) is applied at t=4 secs. Since the ADPE may be off by 9 secs, the current system Doppler error associated with the ADPE controlled downconversion is the difference shown. Figure 4 shows the extrapolated Doppler used by the AIRS downconverter when the first and second order extrapolation techniques are used. For simplicity, the frequency of the downconverter is linearly interpolated between Doppler updates (2 seconds in this case). The Doppler seen by the AIRS carrier tracking unit is the difference between the actual profile and the downconverter frequency profile and is shown in Figure 5. Note the marked improvement.

The doppler compensation error can be further reduced by decreasing T_D. Figure 6 shows that the peak error is roughly linearly proportional to the Doppler update period T_D.

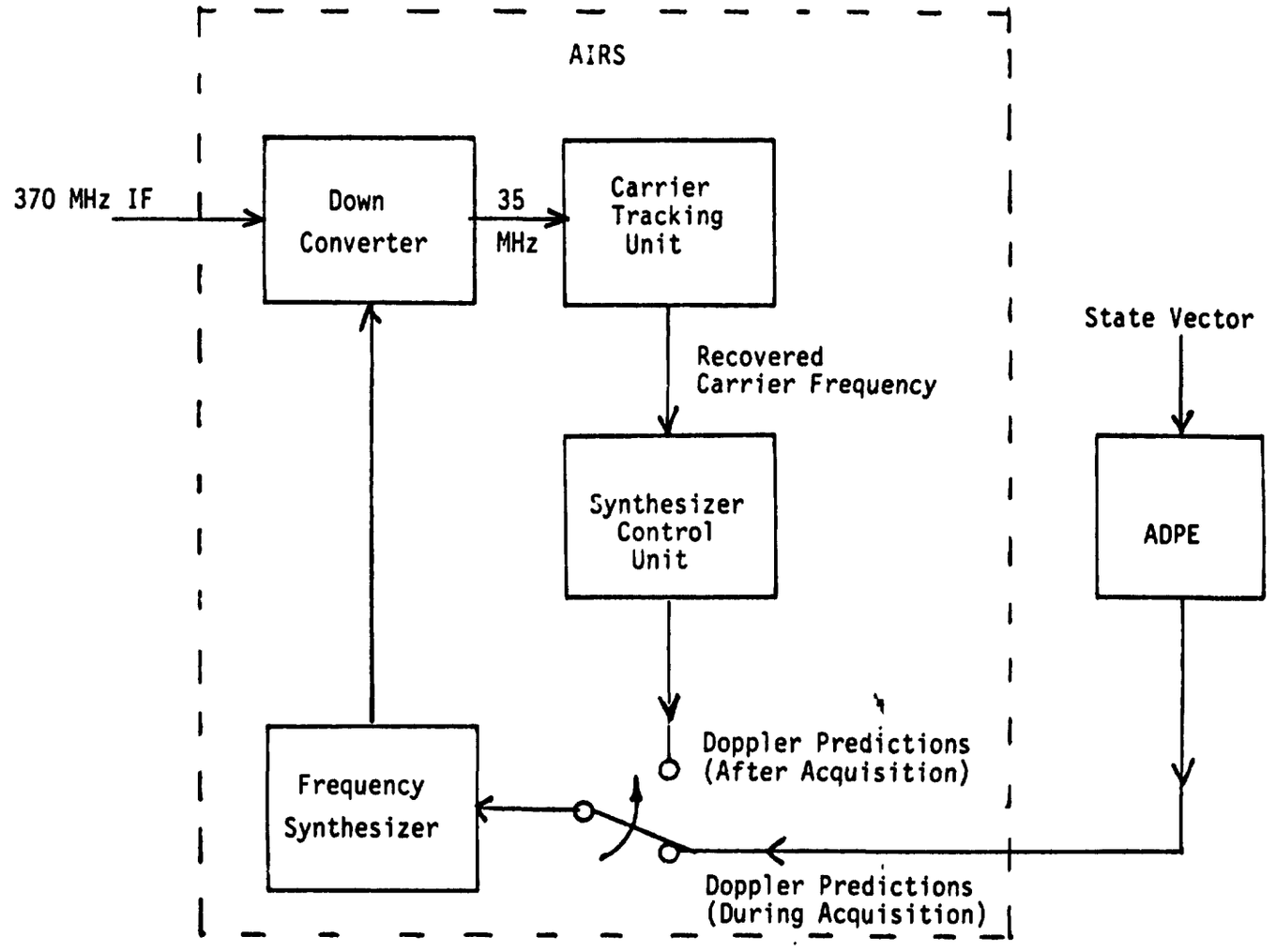


Figure 1. Functional Diagram for the AIRS Autonomous Doppler Compensation Scheme

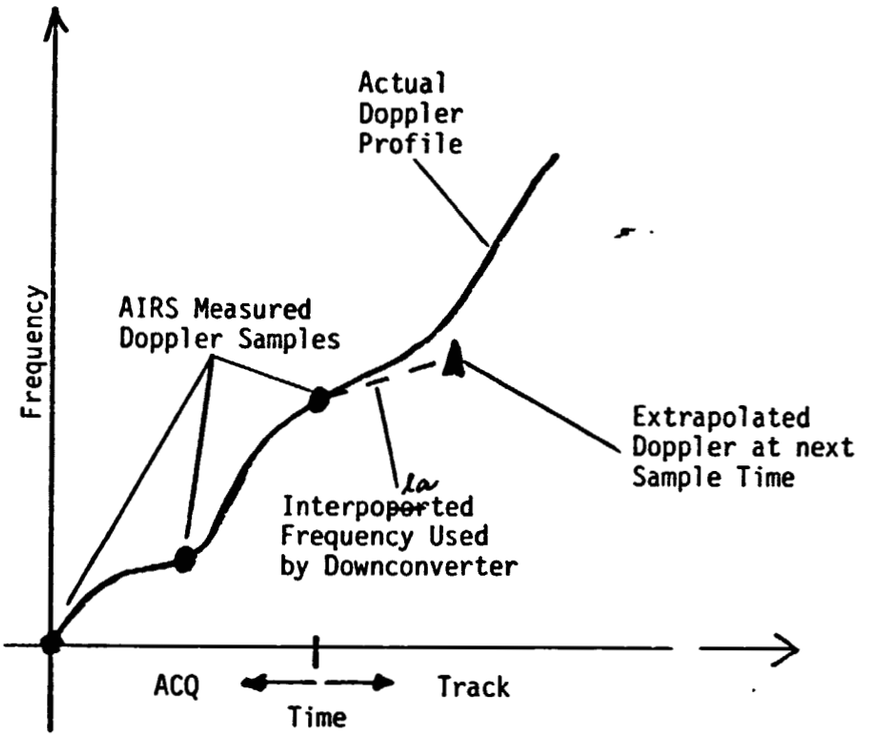


Figure 2. Computation of Downconverter Frequency.

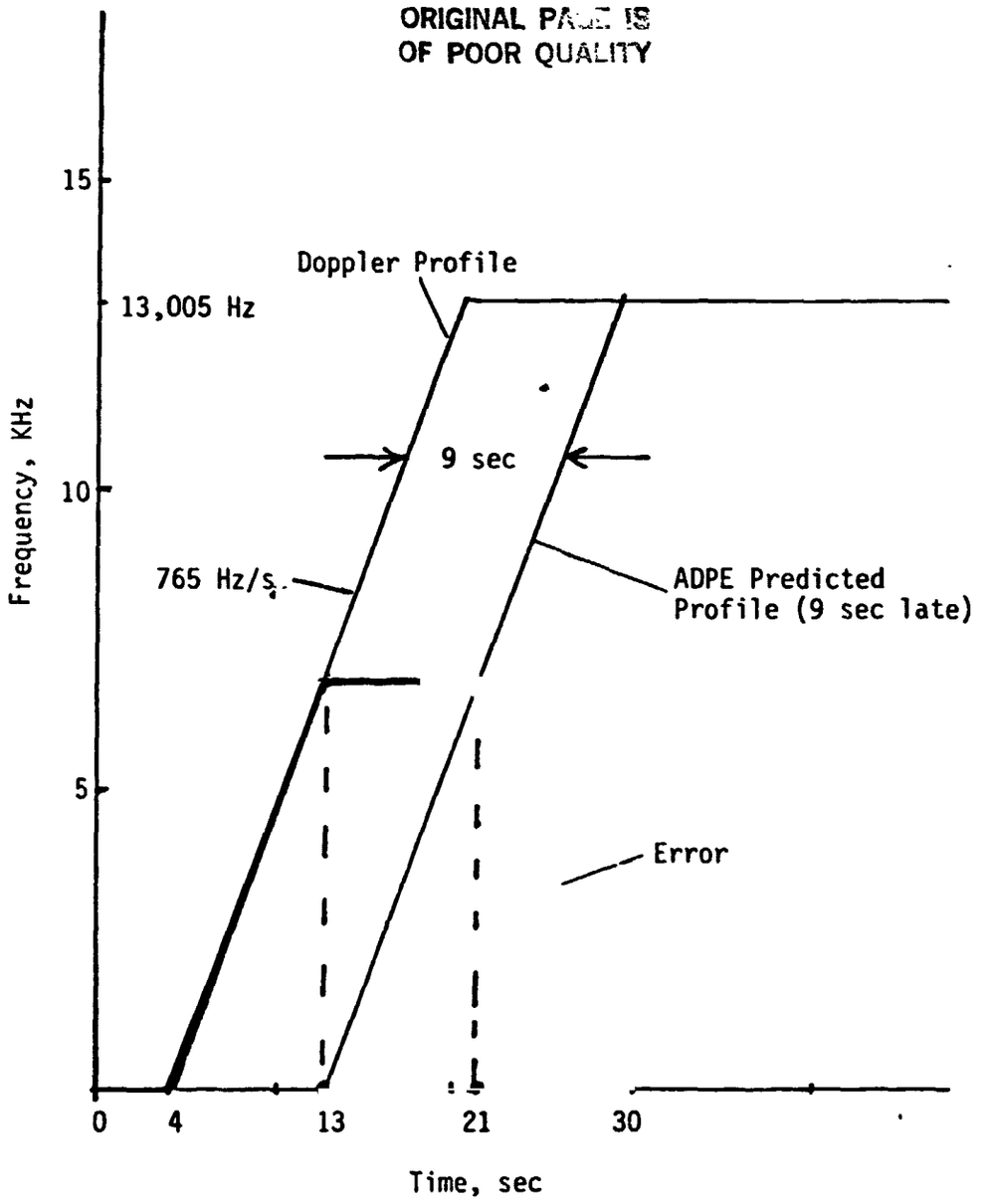


Figure 3. Doppler Profile and Associated ADPE Prediction Error

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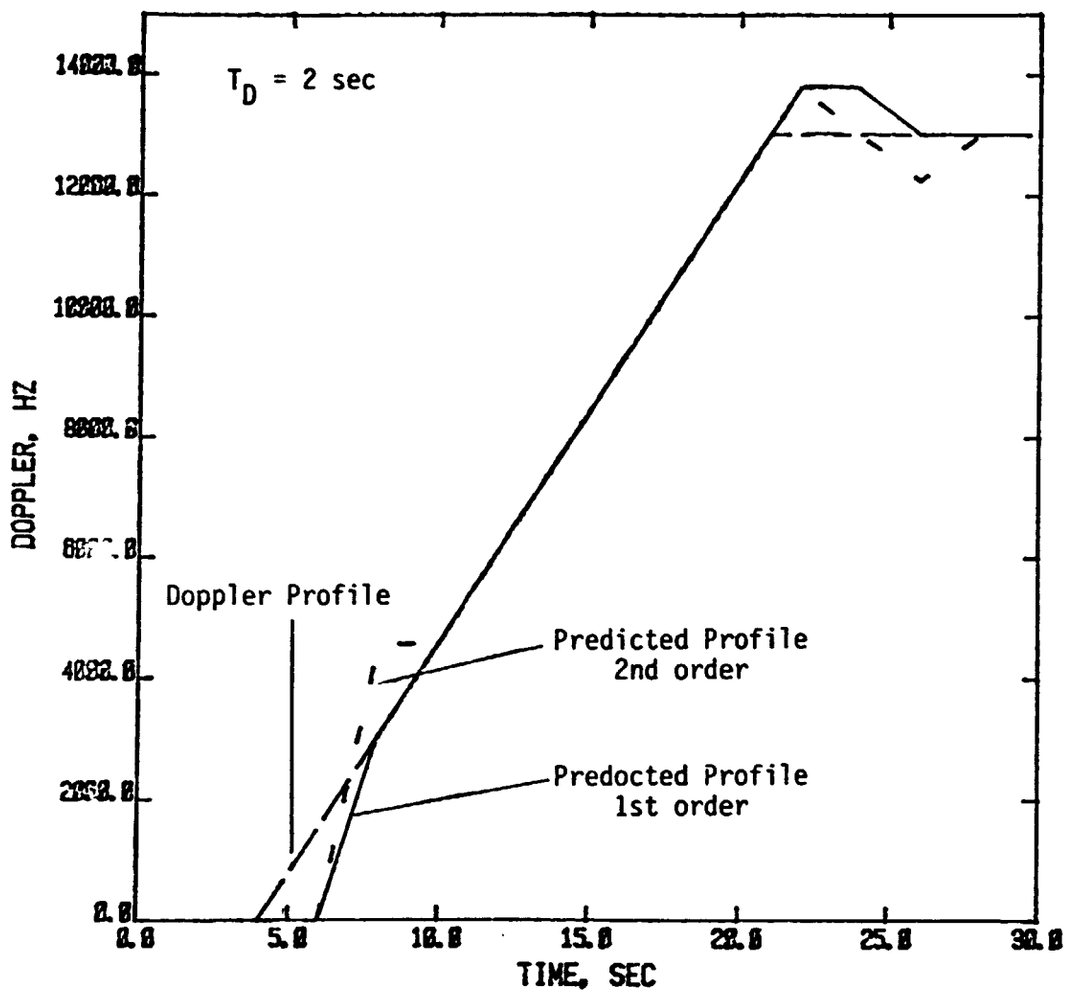

Figure 4. Extrapolated Doppler

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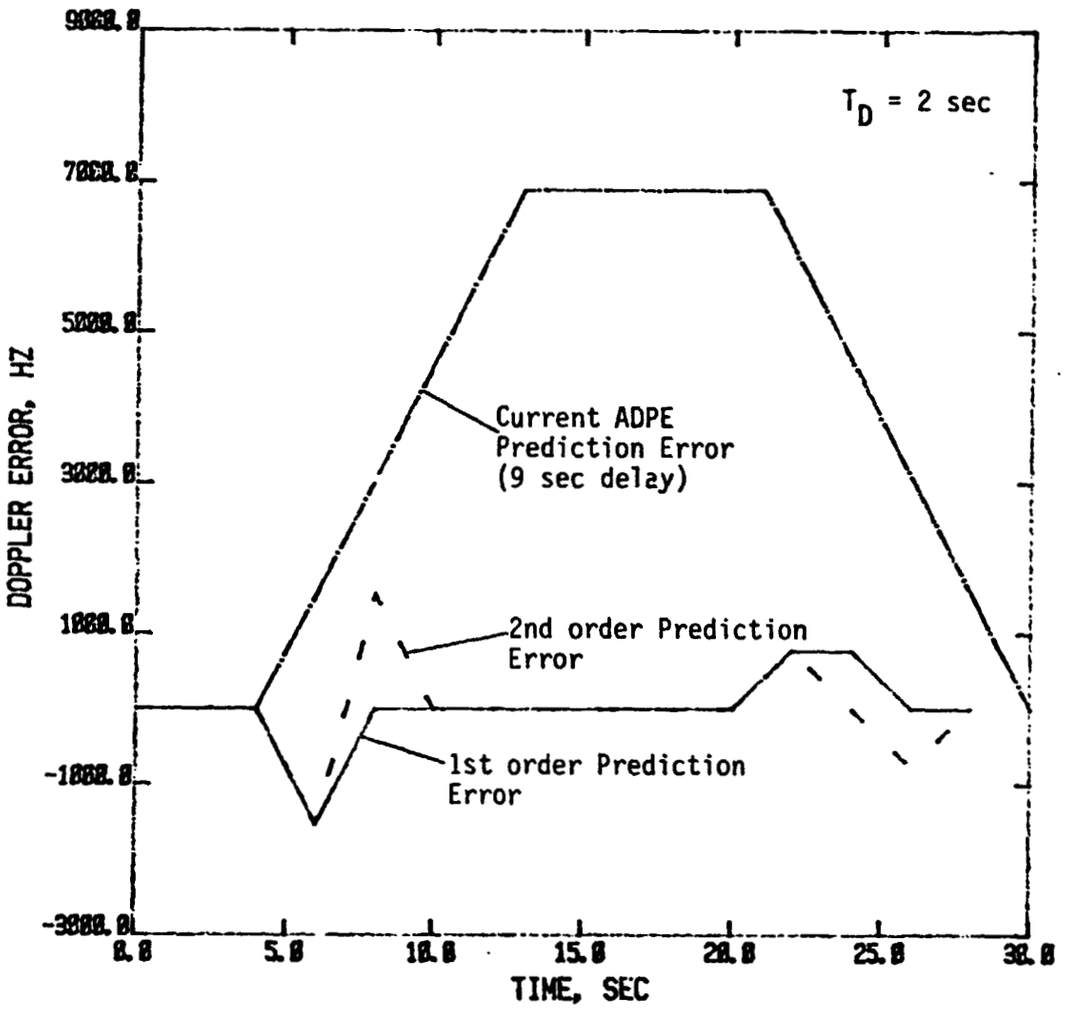

Figure 5. Comparison between ADPE and AIRS Doppler Compensation.

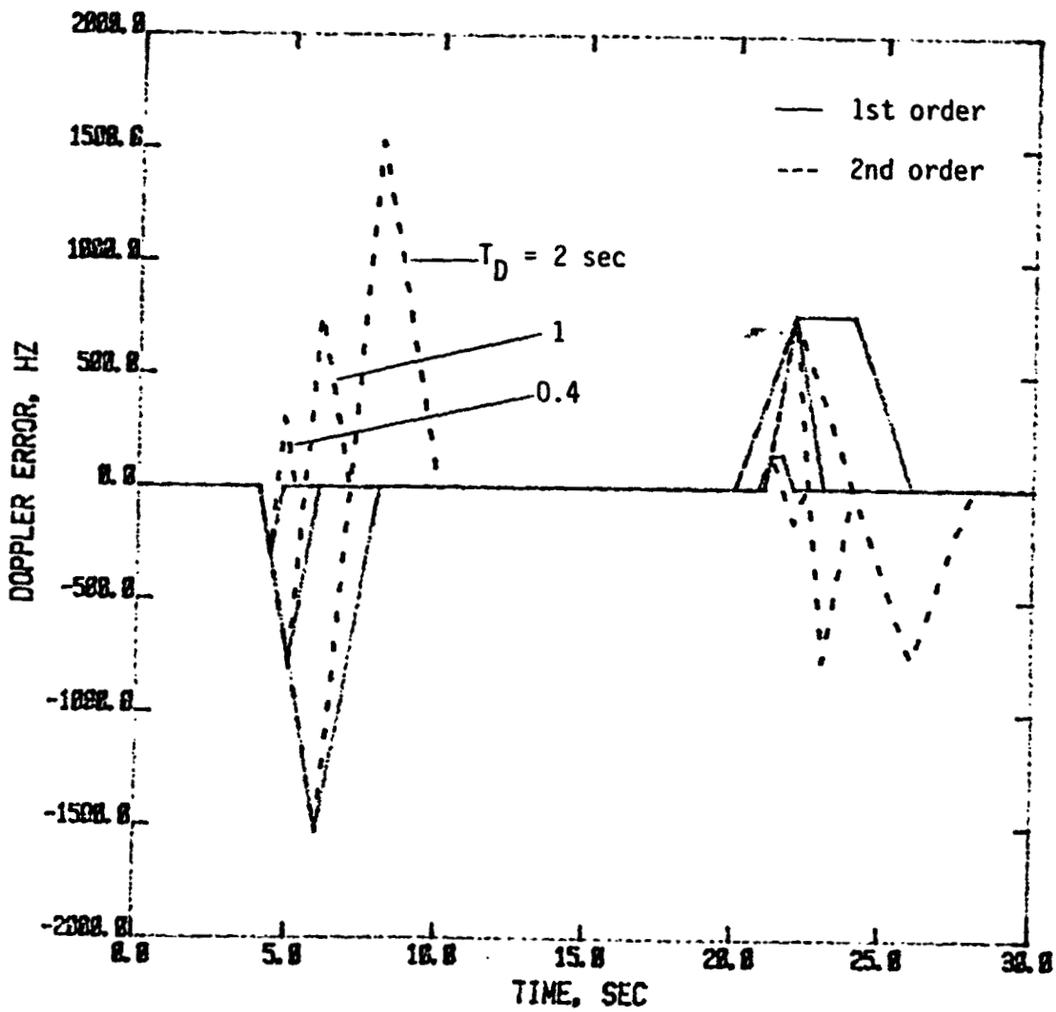

Figure 6. Doppler Compensation error as a function of T_D.

APPENDIX G

TECHNOLOGY ISSUES INVOLVING CCD AND SAW DEVICES FOR AIRS

SUMMARY

It appears that a dual 256-tap CCD correlator will be available next summer from Fairchild and Ford. The device is based on a mask developed by S. C. Munroe of the MIT Lincoln Laboratory. The device appears to be directly compatible with the AIRS acquisition requirements. Because of the size of the bulky substrate required, SAW correlators are deemed to be unsuitable for the AIRS application.

CCD Devices

The attached paper describes work performed by MIT Lincoln Laboratory on the development of a 256-tap CCD correlator prior to 1982. Subsequently, they have developed a mask for an improved version of the TC1235A device to be transferred to Fairchild [Contact: David Wen (415) 858-6166] and to Ford Aero [Contact: John Roschen (714) 720-6151] for commercial (military?) production. The device should be available by next summer.

The new chip has an area of 50,000 mil^2 and is based on 4 μm technology. A lot of the external functions shown in Figure 3 of the paper will be incorporated into the new chip. The new chip will be a dual correlator accepting both the I and Q signals and can correlate 256 samples (512 I&Q) simultaneously. The inputs to the new chip are the

reference PN code, the associated clock and a latch signal. The reference PN code is clocked sequentially into the chip and the latch signal controls the timing which determines when the PN chips will be loaded in parallel to form the fixed binary weights for the correlation. While the correlator chip is performing the correlation, it can accept the next set of sequential PN code reference input. Since the latching of code weights takes place within 400 ns, there is no problem in updating different sections of the PN codes in sequence. This simplifies the hardware requirements since we do not need another device for setting up the next set of weights. The output of the chip interfaces directly with an A/D converter.

For the AIRS application, it is anticipated that up to 1,000 PN chips will need to be correlated. This means that 8 of these devices must be used in parallel, each matched to an appropriate portion (128 chips at 2 taps/chip) of the total section of 1,000 chip code. Since the A/D operates at a relatively slow speed of 3 MHz, accumulating the 8 outputs does not appear to be a major hardware problem.

SAW Devices

A programmable SAW tapped delay line consists of a single piezoelectric substrate with an interdigital transducer at one end which launches a SAW toward an array of interdigital tap transducers. Each tap transducer is wire bonded to a substrate containing integrated circuit switching chips which combine the taps with their respective polarities chosen to match a selected code sequence. Typically the SAW travels at a velocity of 3×10^5 cm/sec which corresponds to a delay of 3.3 μs per cm of substrate. Correlating a 512-chip sequence for the 3 Mcps TDRSS chip rate (171 μs) requires a 52 cm length of substrate.

This size is difficult to grow and handle. Even though several substrates can be cascaded to shorten the individual substrate lengths, the SAW implementation will be bulky and awkward in terms of size. Therefore, it appears that the SAW tapped delay lines are not suitable for the AIRS application.

MilCom '82

UNCLASSIFIED

THE USE OF CCD CORRELATORS IN THE SEEK COMM SPREAD SPECTRUM RECEIVERS† (U)

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(617) - 862 - 5500 x 3245
M.I.T. Lincoln Laboratory
P.O. Box 73
Lexington, Massachusetts 02173

(U) ABSTRACT

(U) The SEEK COMM radio uses a pair of Charge-Coupled Device (CCD) correlators to detect the dehopped, pseudo-noise modulated signals in each of three receiver channels. Developed jointly by M.I.T. Lincoln Laboratory and RCA, the TC1235A analog-binary correlator had specification goals which were strongly driven by SEEK COMM system requirements. With minor exceptions our experience with the device performance, interface requirements, and the total analog-binary correlator board have been very favorable. In terms of performance and practicality the TC1235A is a major advance over earlier correlators. The correlator boards have been designed to permit plug-in replacement of the CCD correlators with a single, one-time gain trim. To date, however, not one TC1235A has been replaced due to failure. The minor deficiencies in the device have been sufficiently characterized, and are well enough understood, to be either minimized or eliminated in the next generation chip.

(U) INTRODUCTION

(U) CCD correlators were chosen and developed for use in the SEEK COMM receivers primarily because of the advantage analog-binary correlators have over all digital correlators in a jamming environment. Rather than dwell on device design and development, which have been covered previously, [1,2,3], the emphasis here will be on CCD correlator system requirements and device performance, interface requirements, board level performance, and experience gained.

(U) SYSTEM REQUIREMENTS AND DEVICE PERFORMANCE

(U) The design of the SEEK COMM receivers placed a number of requirements on the correlators. Many of these specifications were translated directly into design goals for the RCA TC1235A CCD correlator. Table 1 summarizes both the system requirements and the actual device performance. The following comments apply to that table.

TABLE 1
(U) CCD CORRELATOR SPECIFICATIONS

System Requirements	TC1235A Performance
Device Length: 512, 256 points; programmable	512, 256, 128
CCD Clock Rate (> 2X chipping rate): 8 MHz	> 10 MHz
Program (Reference) Register Load Rate: 8 MHz	> 10 MHz
Reference Latch Update Time: <<3 μs (symbol length)	≈ 5 μs
Dynamic Range*: > 40 dB (full length mode)	> 50 dB
Signal-to-Noise Ratio: > 35 dB	> 35 dB
Distortion: "Low"	≈ 1%
Code Insensitivity (to code balance, distribution)	No code-dependent bias, some devices sensitive to distribution of 1's and 0's.
Device Interchangeability	Yes - with one-time gain trim.
Low Power Dissipation: < 2W	900 mW
Reasonable off-chip support circuitry	Yes

*Dynamic range defined as $20 \log_{10} \frac{\text{Signal input at max. output}}{\text{Signal input at min. detectable output}}$

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(3) The need to minimize intermodulation between signal and jammer ...e the distortion specification.

(C) The code-insensitivity issue has two aspects. The first is the sensitivity of the correlator to imbalances in the numbers of 1's and 0's in the reference code[1]. In the TC1235A this problem has been designed out[3]. The second aspect is sensitivity to the distribution of 1's and 0's in the reference code. The source of this subtle and unexpected problem, which reached unacceptable levels in only a few correlators while in the full-length mode, was traced to differences between the first and second halves of the devices. These nonuniformities can occur because the chip is folded at midpoint and mask registration errors parallel to the CCD channel affect the first and second halves differentially. By eliminating several extremely asymmetrical codes and including the correlator in an auto-zero loop the problem has been bypassed in the SEEK COMM radio. With the understanding of the mechanism gained from the TC1235A it should be possible to reduce code sensitivity to negligible levels in the next generation CCD correlators.

(U) Figure 1 is an oscillogram showing correlator performance while single sampling a $3V_{p-p}$, 8 MHz, 255-bit, cyclic M-sequence. As expected, a single correlation spike occurs every 32 μs. While there is some nonuniformity superimposed upon the constant clock feedthrough in the baseline, its value is consistent with the device being mismatched to the cyclic code by 1 bit (256 vs 255 bits). In terms of peak-to-sidelobe ratio, therefore, the TC1235A approaches the theoretical value for cyclic M-sequences.

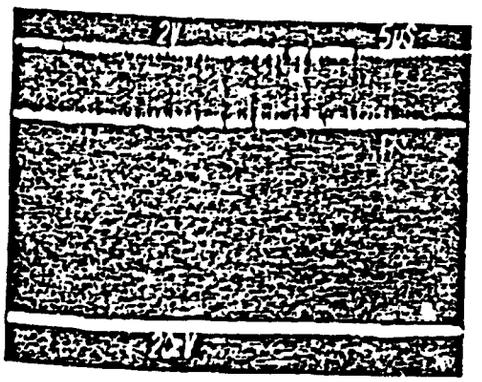

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Fig. 1. (U) TC1235A CCD correlator.

(U) Figure 2 is a photomicrograph of the TC1235A mounted and bonded in a 64-pin ceramic DIP. As can be seen not all pins are used, and some of the bonded pins are redundant. The chip is folded at the midpoint, thereby producing mirror image symmetry about a central horizontal axis. Although the chip is large it was fabricated with 8 μm design rules. If fabricated with today's 4 μm rules the area would more than halve, making it comparable in area to a 64 Kbit DRAM. Design changes contemplated in some circuits for the next generation will shrink size, power, and pin count still further while enhancing performance.

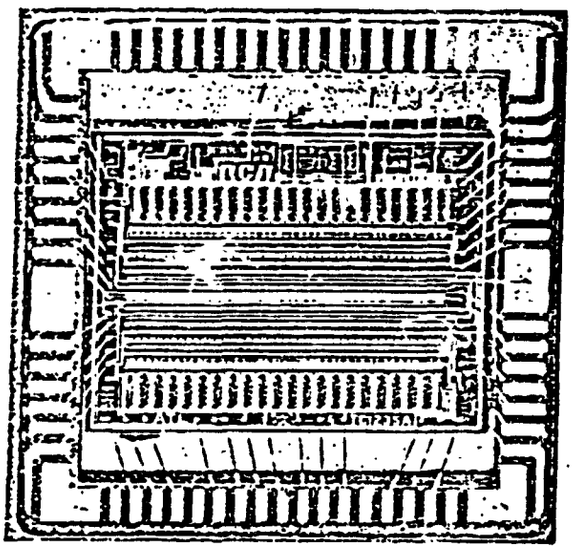

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Fig. 2. (U) TC1235A CCD correlator chip.

(U) SEEK COMM A/D SLICE

(U) The analog-binary correlator board in the SEEK COMM radio is often referred to as the A/D slice because all signals routed to the board are analog, while all those leaving are digital. Figure 3 is a block diagram of the slice. Due to the I and Q nature of the signals two correlators are required per receiver channel. For diagnostic reasons analog switches have been placed before the correlators so that a test input can be routed to either or both devices. This feature facilitates rapid isolation of faults.

(U) The CCD off-chip support circuitry consists of the following. A single $20V_{p-p}$ CCD shift register transfer clock and $8V_{p-p}$ input sampling (strobe) pulse are generated in one circuit. The load logic circuitry controls loading of the reference code and updating of the latches. The on-chip program

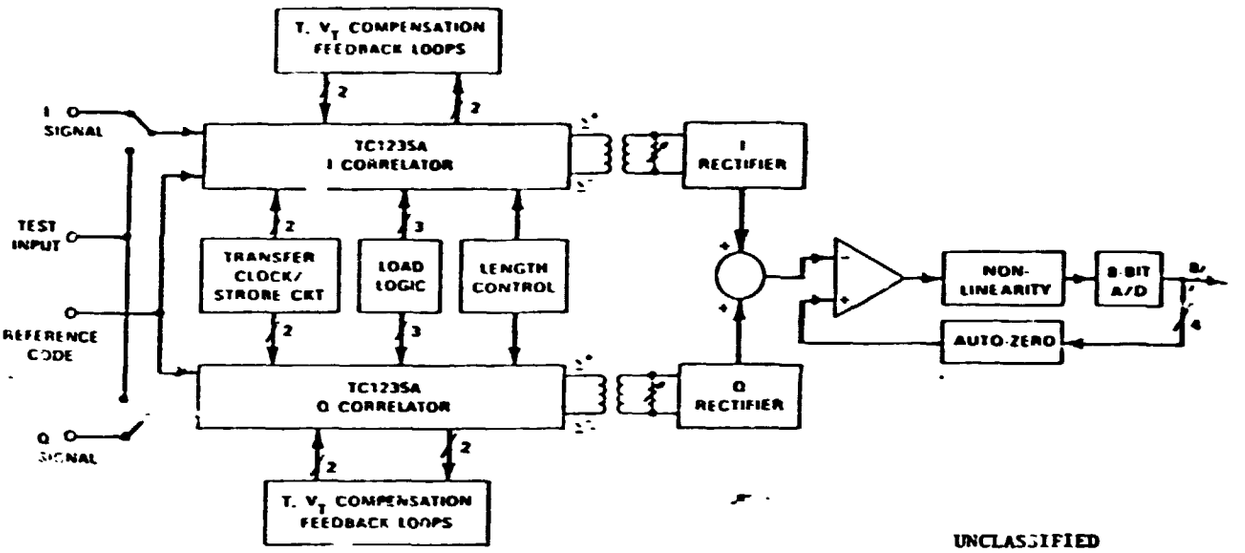

Fig. 3. (U) TC1235A analog-binary correlator board block diagram.

register clock driver is used here, and both the input reference code and clock input to the on-chip driver are TTL compatible. Length control switches enable the correlator to be either 512 or 256 stages long for sync or data modes, respectively. A very important support circuit consists of two feedback loops per correlator which completely stabilize the devices against threshold voltage and temperature variations. These compensation loops enable plug in replacement of the correlators with only a one-time gain trim performed during board calibration. If an emitter resistor can be justified to stabilize a single bipolar transistor against wide variations in β then surely a dual op amp and a few passive components can be justified to stabilize an IC with nearly 10,000 transistors and many orders of magnitude more signal processing capability. Incorporation of this automatic compensation circuitry, which consumes little power or area, was a major step toward the goal of a "tweakless" A/D slice. When the CCD correlators are in production status, so that the fabrication conditions are more uniform, the ±10% maximum gain variations seen now should be reduced considerably. Once the maximum correlator gain variations are less than about ±5% then even the one-time gain trim can be eliminated, therby resulting in a completely adjustment-free board.

(U) The post correlator processing circuitry begins with the transformers, which provide scaling and level shifting of the differential correlator outputs with high common mode rejection. Gain adjustment is effected by trimming potentiometers on the secondaries of the transformers. Fast, precision rectifiers convert the bipolar differential inputs into easily summed unipolar current source outputs. The combined currents are fed to a fast op amp for voltage conversion and scaling, with the result routed to an 8-bit flash A/D converter after modification by a nonlinearity. The purpose of the nonlinearity is to expand the low signal end (by 2X) and compress the high end (by 2X), thereby achieving 9-bit resolution. Finally, an auto-zero loop forces the A/D output to be a digital zero for the zero analog signal condition. Our experience has been that an auto-zero loop would be necessary even if the correlators were perfect because of the temperature-dependent input offsets of both the fast op amp and the A/D converter. However, the auto-zero loop could be simpler, and the function implemented less frequently, if the correlators were outside the loop. By reducing the sensitivity of the next generation of CCD correlators to asymmetrical codes it should be possible to do this.

(U) Figure 4 is a photograph of the SEEK COMM analog-binary correlator board. In the upper left corner are the I,Q, and test inputs, together with two analog switch IC's. The two CCD correlators are in the upper right quadrant. Nearby are the feedback compensation loops, length, and program register control circuits. In the lower center is the transfer and strobe clock circuitry. The A/D converter and support circuitry is in the lower left hand corner, while the digital timing chain is in the lower right. For convenience the rectifiers, fast op amp, nonlinearity, and auto-zero circuitry have been placed on a daughter board mounted behind the correlators.

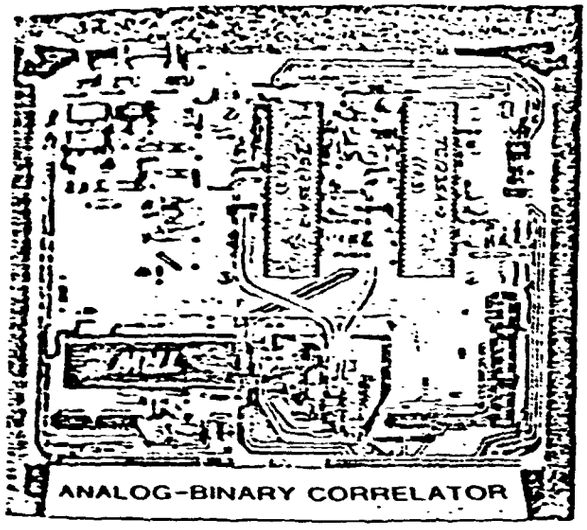

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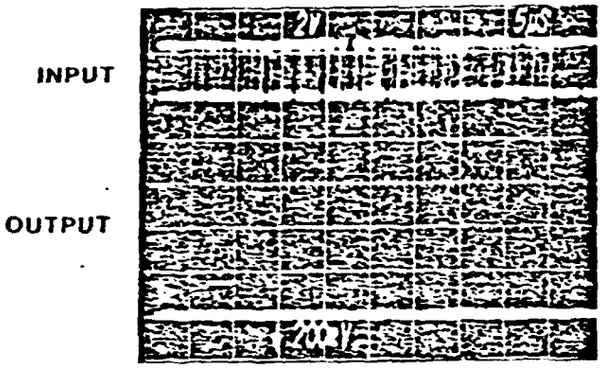
Fig. 4. (U) TC1235A analog-binary correlator board.



ANALOG-BINARY CORRELATOR BOARD

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Fig. 5. (U) TC1235A analor-binary board.

(U) The A/D alice boards are completely interchangeable, and dissipate about 12W typical. With the exception of power and dynamic range the specifications for the board are almost identical to those listed in Table 1 for the TC1235A itself. The worst case dynamic range measured for some boards is about 35 dB, down from about 50 dB minimum for the device alone tested with cyclic M-sequences. The typical dynamic range is about 40 dB, with highs near 50 dB. One factor contributing to the dynamic range reduction on the board is the more severe test conditions of aperiodic codes which are not M-sequences. This situation illuminates defects such as sensitivity to asymmetrical codes. Another factor is imperfections in the post correlator processing circuitry. In any case, elimination of several extremely asymmetrical codes rendered board-level performance more than adequate for the radio.
(U) Both board and CCD correlator reliability have been excellent. Figure 5 is an oscillogram showing board performance after conversion of the digital output to analog form by a D/A converter. If compared with Fig. 1, which shows performance for one correlator alone, it is clear that other than a scale change the only significant difference in the waveforms is the increased nonuniformity in the baseline of the board output. This increase is due primarily to the intentional nonlinearity on the board which amplifies low level signals by a factor of two.

(U) SUMMARY

(U) The TC1235A is an analog-binary CCD correlator developed jointly by RCA and MIT Lincoln Laboratory for use in the SEEK COMM receivers. It is a third generation device which exhibits a quantum leap in performance over earlier correlators. When used with proper support circuitry the TC1235A displays reliability and capability more than adequate for use in spread spectrum receivers. Its few flaws, which are relatively minor, have been characterized and are understood well enough to be significantly reduced or eliminated in the next generation.

(U) REFERENCES

[1]. S. C. Munroe, "The Code-Dependent Bias Problem in Programmable CCD Correlators," Presented at the IEEE Circuits and Systems Society CCD Signal Processing Workshop, NY (May 1978).

[2]. D. A. Gandolfo et al, "Analog-Binary CCD Correlator: A VLSI Signal Processor," IEEE JSSC, Vol. SC-14, No. 2 (April 1979).

[3]. S. C. Munroe, "Programmable Zero-Bias Floating Gate Tapping Method and Apparatus," U.S. Patent No. 4,298,953, Issued 3 November 1981.

APPENDIX H

OPTIMAL GAIN CONTROL FOR ADC

H.1 Introduction

Gain control is required to match the dynamic range of the input signal and the analog-to-digital converter (ADC) to minimize distortions introduced by the A/D system. Here, a techniuqe for generating the required feedback to adjust this gain is described. The technique also provides a way to estimate the received signal level.

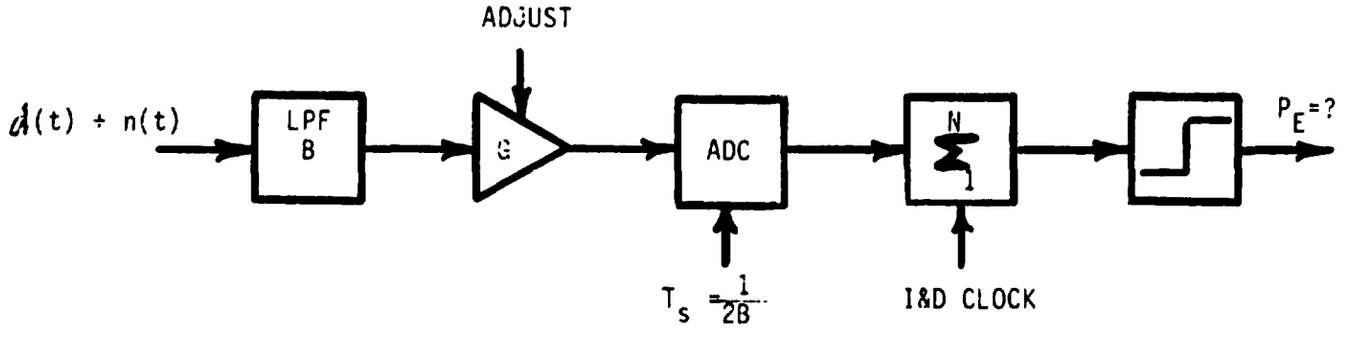
H.2 System Model

Figure H.1a shows a system model for analysis. The incoming signal is modeled by

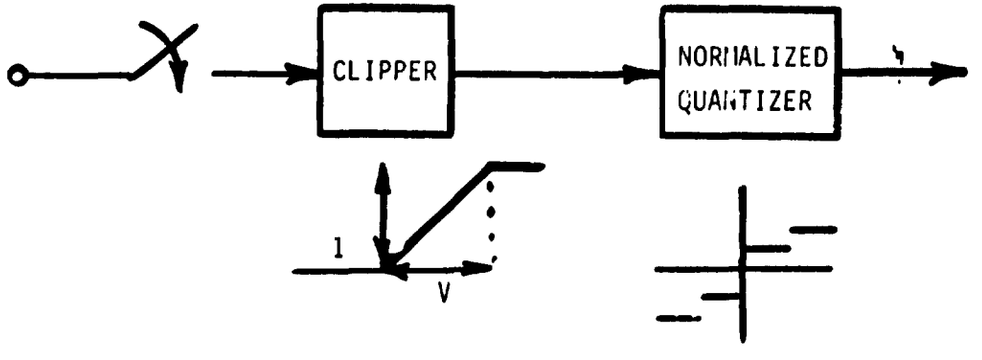
$$s(t) = d(t) + n(t)$$

where d(t) is a $\pm\sqrt{S}$ NRZ waveform with bit time T and n(t) is white with density $N_0/2$. The purpose of the low pass filter is for antialiasing and is assumed to be ideal with bandwidth B Hz. It is also assumed that BT >> 1 so that the signal is undistorted at the filter output. The gain in front of the ADC is adjusted so as to minimize the probability of error at the output of the digital integrate and dump (summer).

Figure H.1b shows the model used for the ADC. The output of the gain controlled amplifier is sampled and then clipped to the range of (-V/2,V/2) where V is the dynamic range of the ADC. The clipped signals is then quantized to 2^n levels where n is the number of bits used by the ADC. The normalized converter characteristics is



(a) SYSTEM MODEL



(b) ADC MODEL

Figure H.1. Analysis Model.

$$Q(y) = \begin{cases} 2^{n-1}+k & \text{for } (k-1)\Delta < y < k\Delta \\ & k=1,\ldots,2^{n-1} \\ 2^{n-1}-k+1 & \text{for } k\Delta < y < (k-1)\Delta \end{cases}$$

where $\Delta = 2^{-n}$ is the normalized quantization step size of the ADC.

Assuming the I&D clock for the summer is coherent with the data transition, i.e., perfect bit sync available, the input for each I&D period is a sequence of signal samples of the same sign. Without loss of generality we assume that a $+\sqrt{S}$ signal is sent. Then, the input to the clipper is a Gaussian sample with mean = $G\sqrt{S}$ and variance $G^2\sigma^2 = G^2N_0B$. The probability of the sample x_k at each of the levels of the ADC output can be computed easily. In particular, the probability of assuming the lowest (1) P_L, the highest (2^n) level P_H, and the sum of the two, P_{out} are of interest as we shall see shortly. They are given by

$$P_H = \frac{1}{2}\,\mathrm{erfc}[(\tfrac{1}{2}-\Delta)/\gamma-1]\sqrt{\rho}$$

$$P_L = \frac{1}{2}\,\mathrm{erfc}[(\tfrac{1}{2}-\Delta)/\gamma+1]\sqrt{\rho}$$

$$P_{out} = P_H + P_L$$

where $\gamma = G\sqrt{S}/V$, $\rho = S/2\sigma^2$ and $\mathrm{erfc}(x) = \sqrt{2/\pi}\int_x^\infty e^{-x^2}dx$. After computing the probability of each ADC output levels, the probability distribution of the summer output can be easily determined, for example see [1]. The probability of making an error, i.e. P_E can then be obtained.

H.3 Dependence of P_E on A/D System Parameters

The resultant probability of error is a function of the ADC input signal-to-noise ratio, the integration length N, the number of bits n used, and the setting of the gain G. Figures H.2-H.5 show the performance of the digital I&D system compared to an ideal analog I&D system. The degradation, in terms of signal-to-noise ratio loss at a fixed E_b/N_0, is plotted vs the normalized gain γ/ρ as a function of different combinations of E_b/N_0, n and N.

In a practical system implementation, one must somehow use information from the ADC outputs to adjust the gain G. The last set of curves in Figures H.2-H.5 unfortunately are related to the system parameters in a complicated way so that they can be of limited use for error signal generation. Intuitively, it is reasonable to assume that the ADC outputs, regardless of the A/D parameters, must be "statistically preserving" of its samples, in order to optimize the system performance. Figure H.6 shows the performance degradation of the digital I&D system in a form motivated by this intuitive reasonin The degradation is plotted against the out of range probability P_{out} for a variety of input signal conditions and integration length with n fixed at 6 bits. From this figure, it is obvious that if P_{out} is restricted to $2^{-5} = 1/32$ or less, the degradation is less than 0.02 dB. The approach suggested by Figure H.6 to adjust for optimal gain is to keep track of the occurrences of the highest and lowest samples and adjust the gain G so that $P_{out} = 1/32$.

H.4 Analysis of Proposed AGC/Signal Strength Indicator

Figure H.7 shows the out of range probability as a function of the normalized gain $\gamma/\sqrt{\rho} = \frac{G}{V}\sqrt{2}\,\sigma$ with varying system parameters E_b/N_0, N

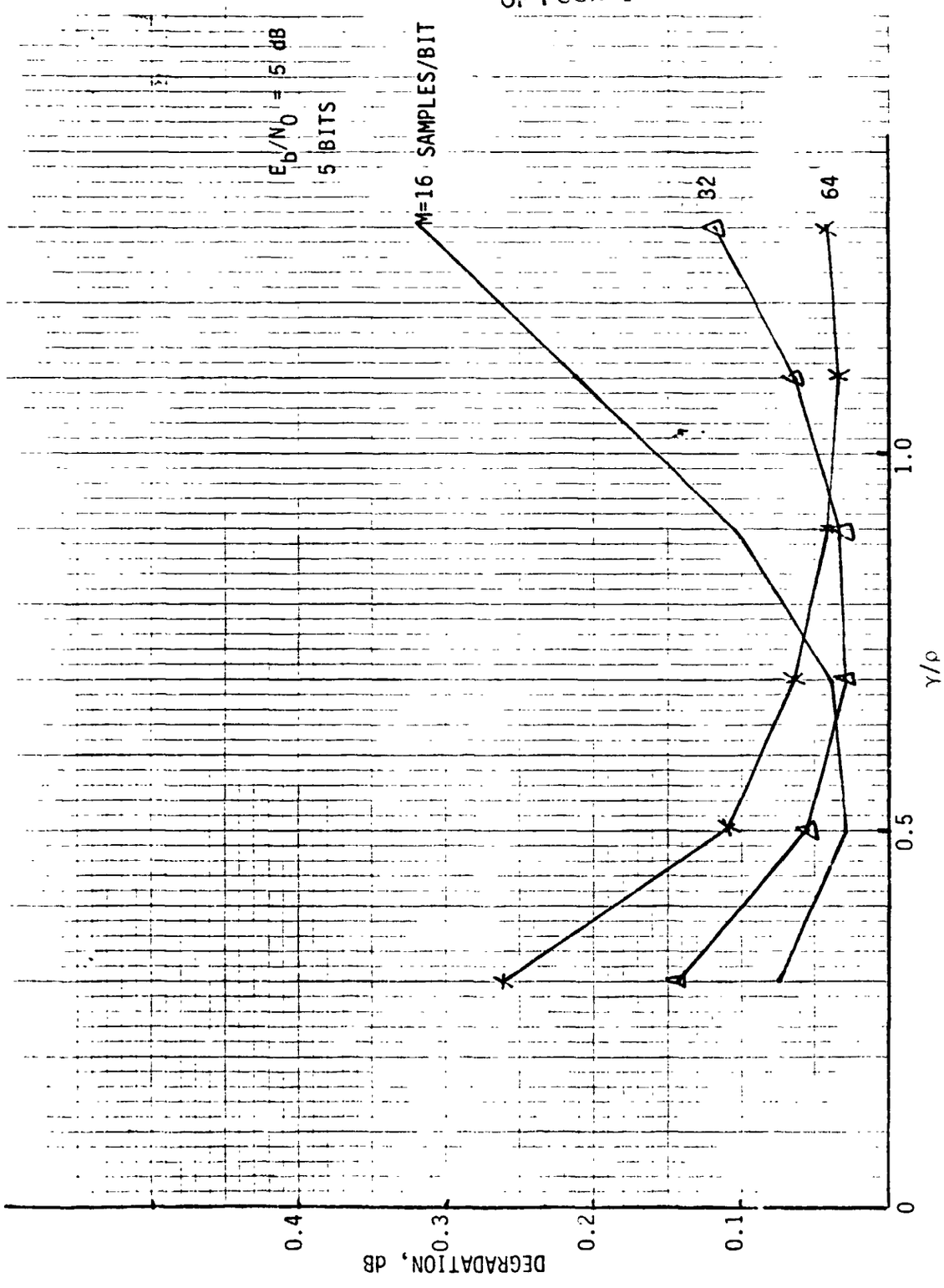


Figure H.2. Digital Integrate-and-Dump ADC Loading Sensitivity.

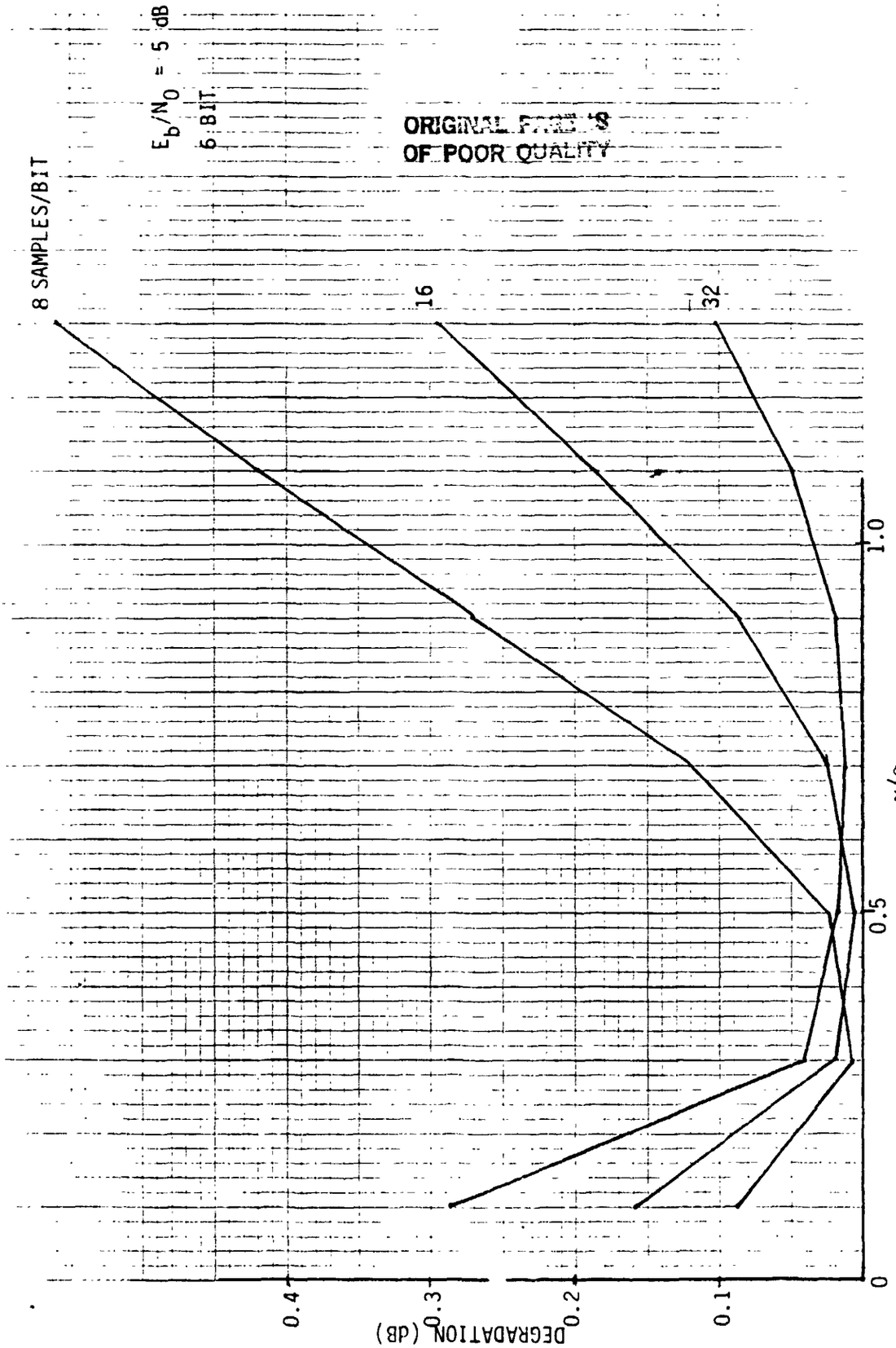


Figure H.3. Digital Integrate-and-Dump ADC Loading Sensitivity.

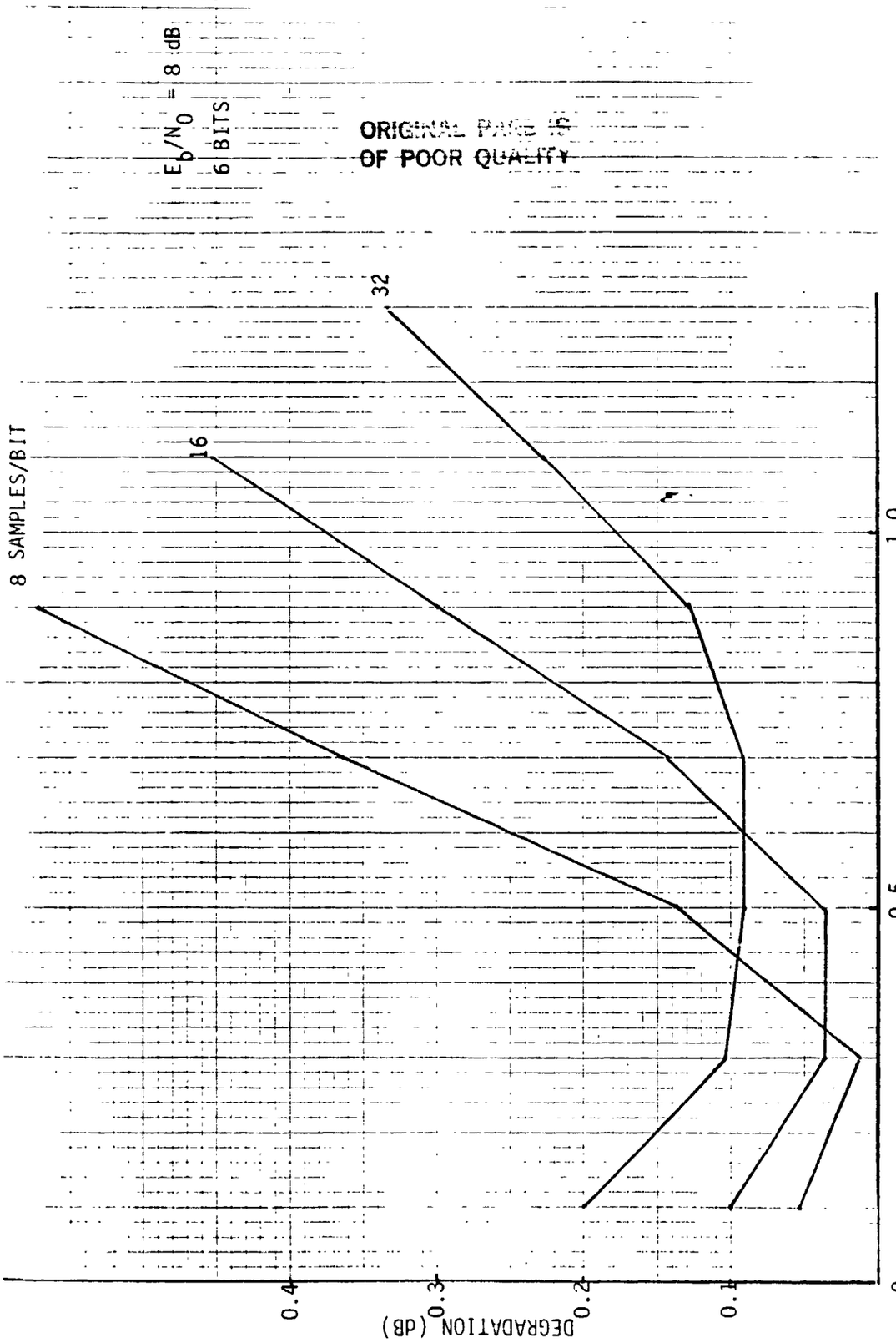


Figure H.4. A Digital Integrate-and-Dump ADC Loading Sensitivity.

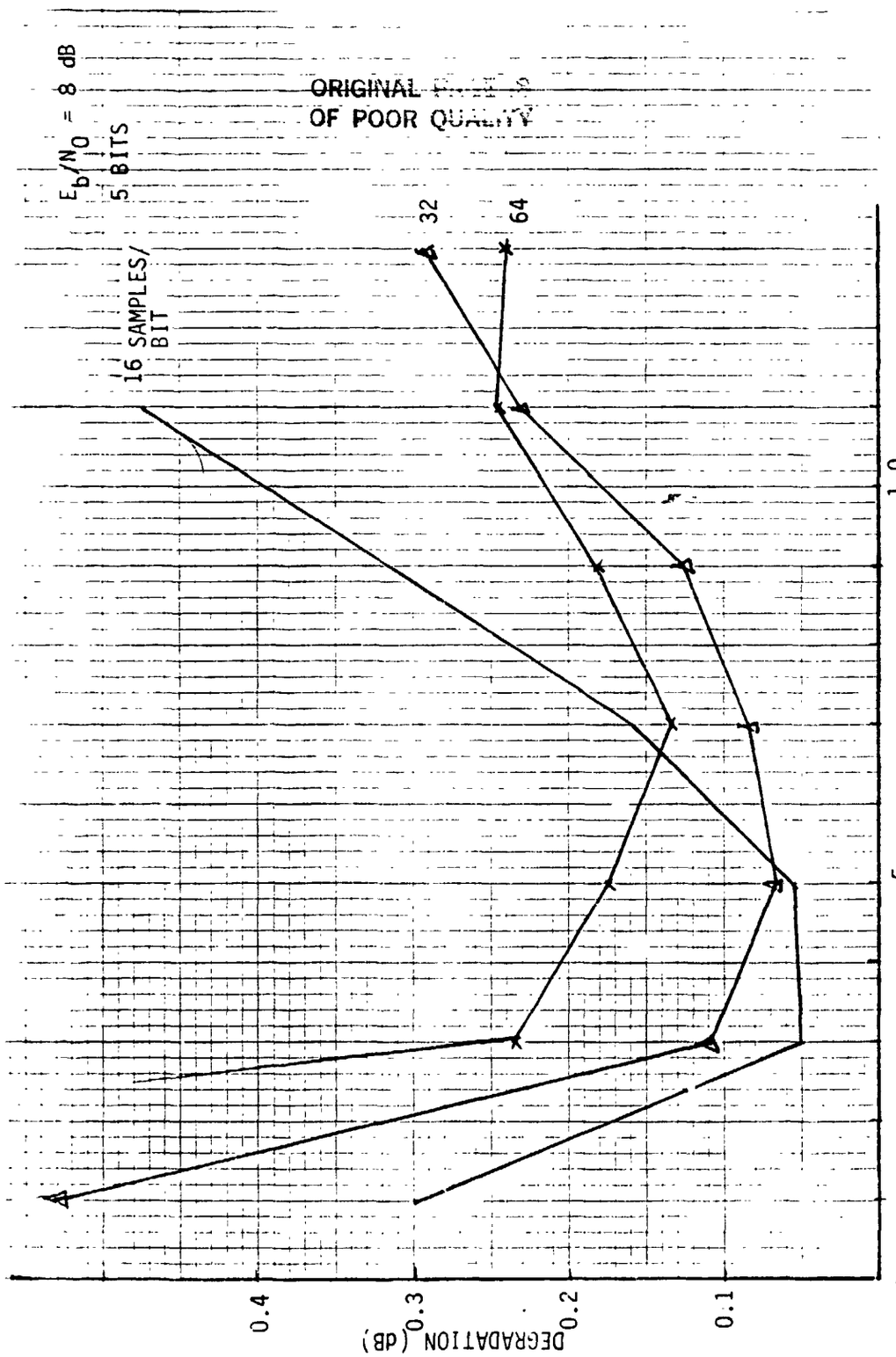


Figure H.5. Digital Integrate-and-Dump ADC Loading Sensitivity.

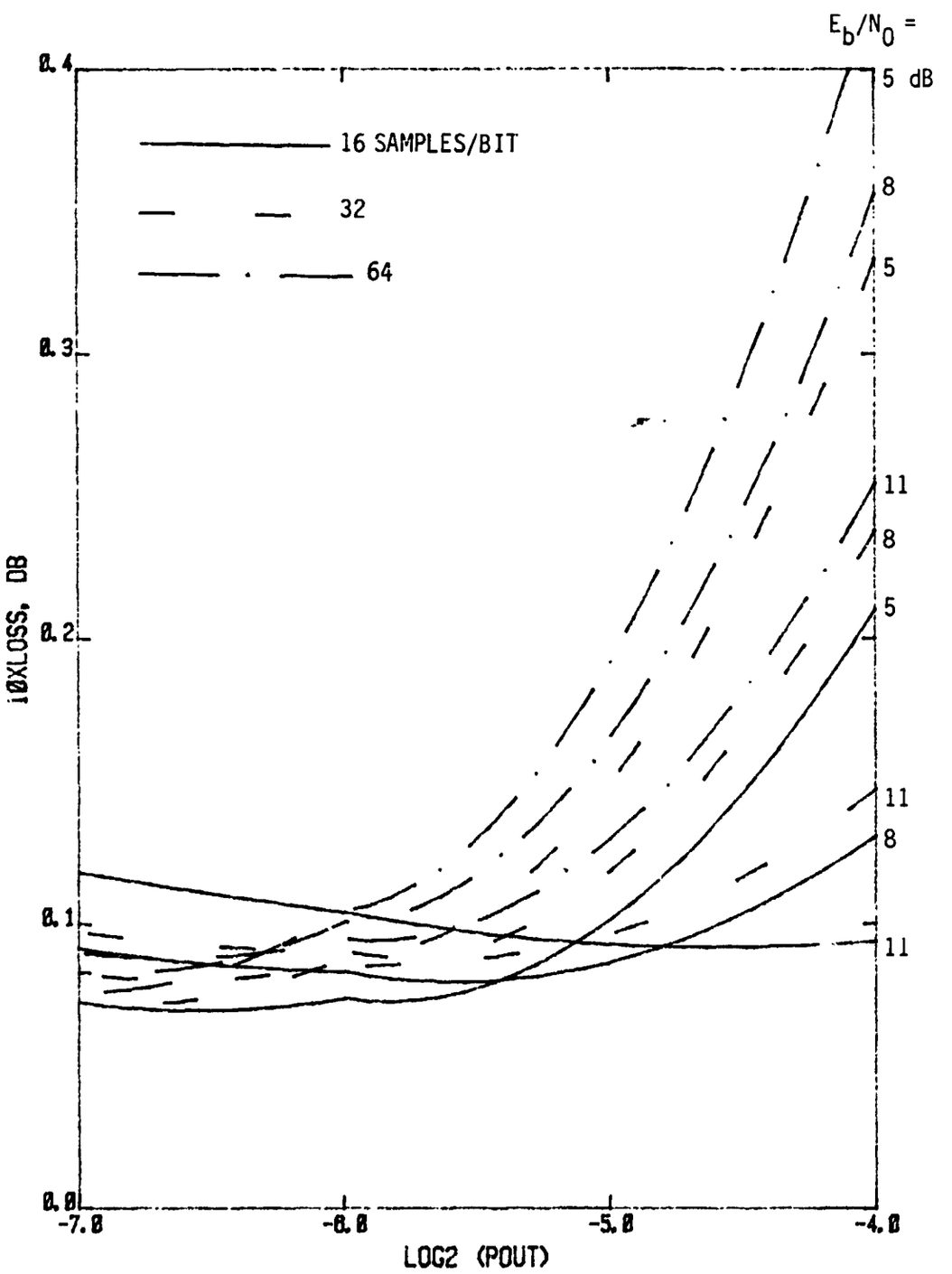


Figure H.6. SNR Degradation vs P_{out}.

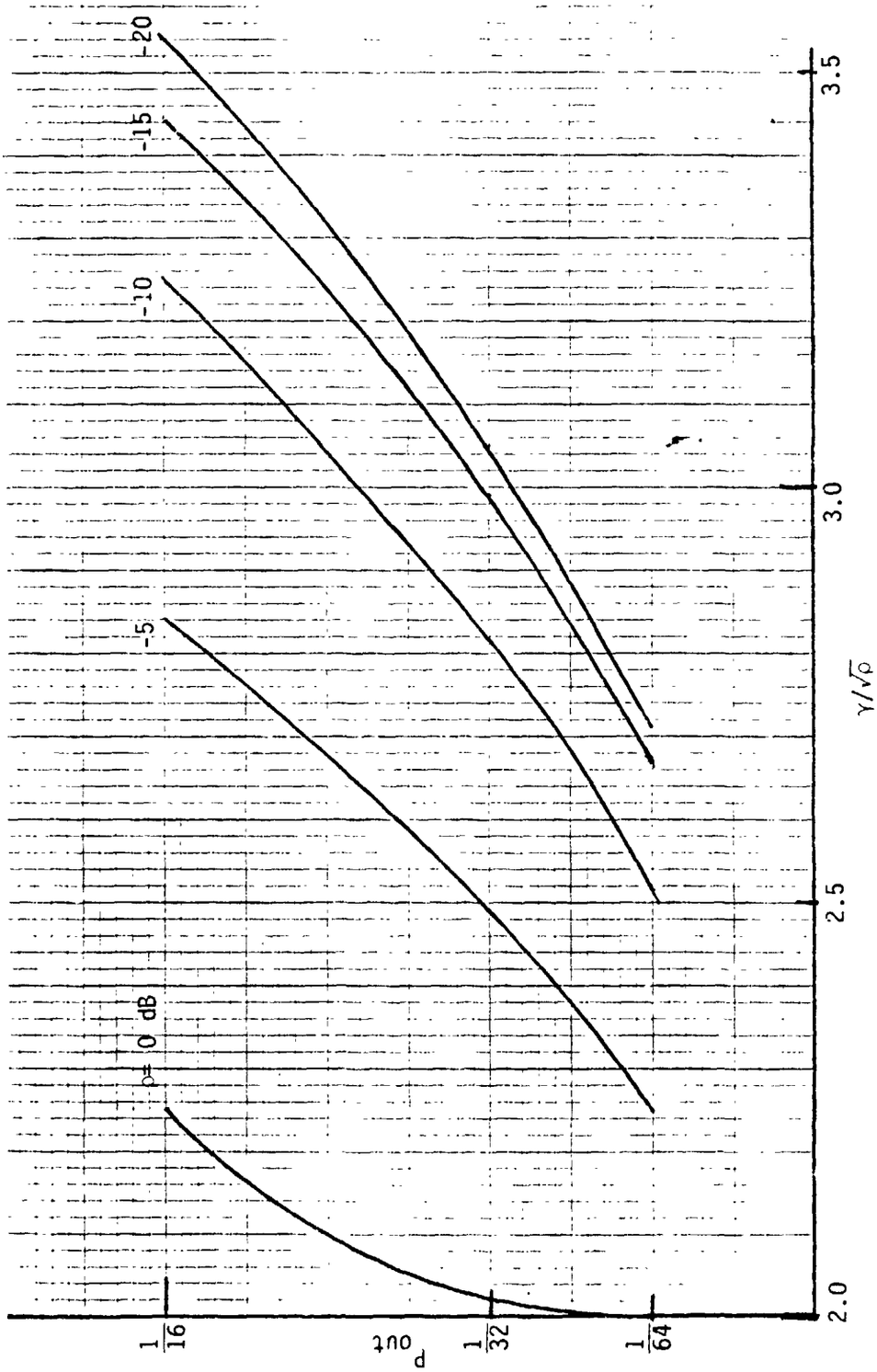


Figure H.7. P_{out} vs Normalized Gain.

and n. It can be observed that P_{out} can serve as an error feedback to adjust the gain. For a fixed P_{out} and system parameters, it is shown in Figure H.8 that the mean output of the ADC m is a good estimate of signal $\gamma = G\sqrt{S}/V$. If one measures the mean output of the A/D, then one can estimate the input signal amplitude $\sqrt{S}$ via

$$\sqrt{S} = \frac{V}{G} \cdot m$$

Since V is a known hardware parameter and G is the steady state gain of the AGC system. Figure H.9 shows the algorithms required to implement this AGC/signal strength indicator system.

Reference

[1] C. M. Chie, "Performance Analysis of Digital Integrate-and-Dump Filters," IEEE Trans. Comm. Tech. Aug. 1982, pp. 1979-1983.

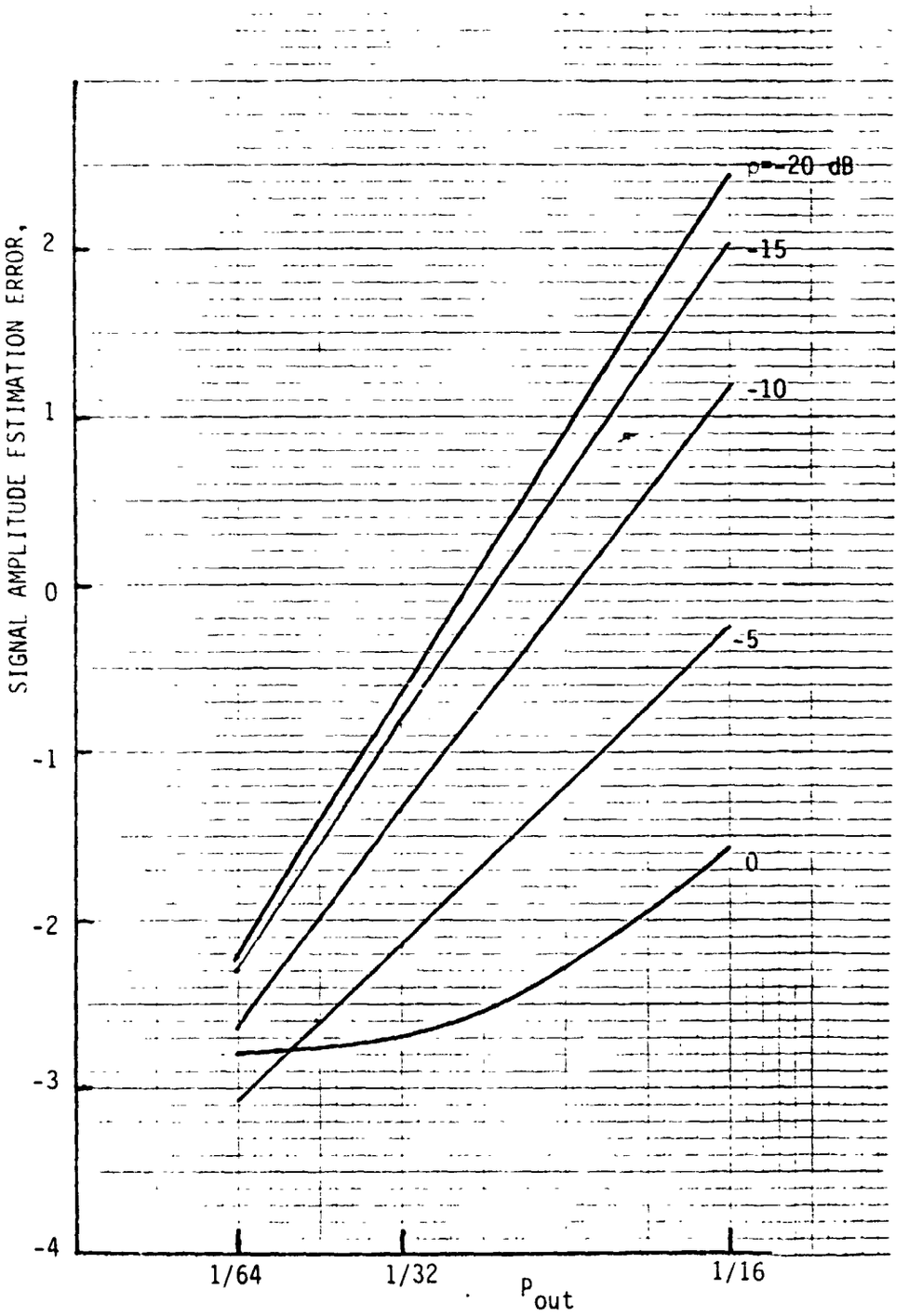


Figure H.8. Signal Amplitude Estimation Error.

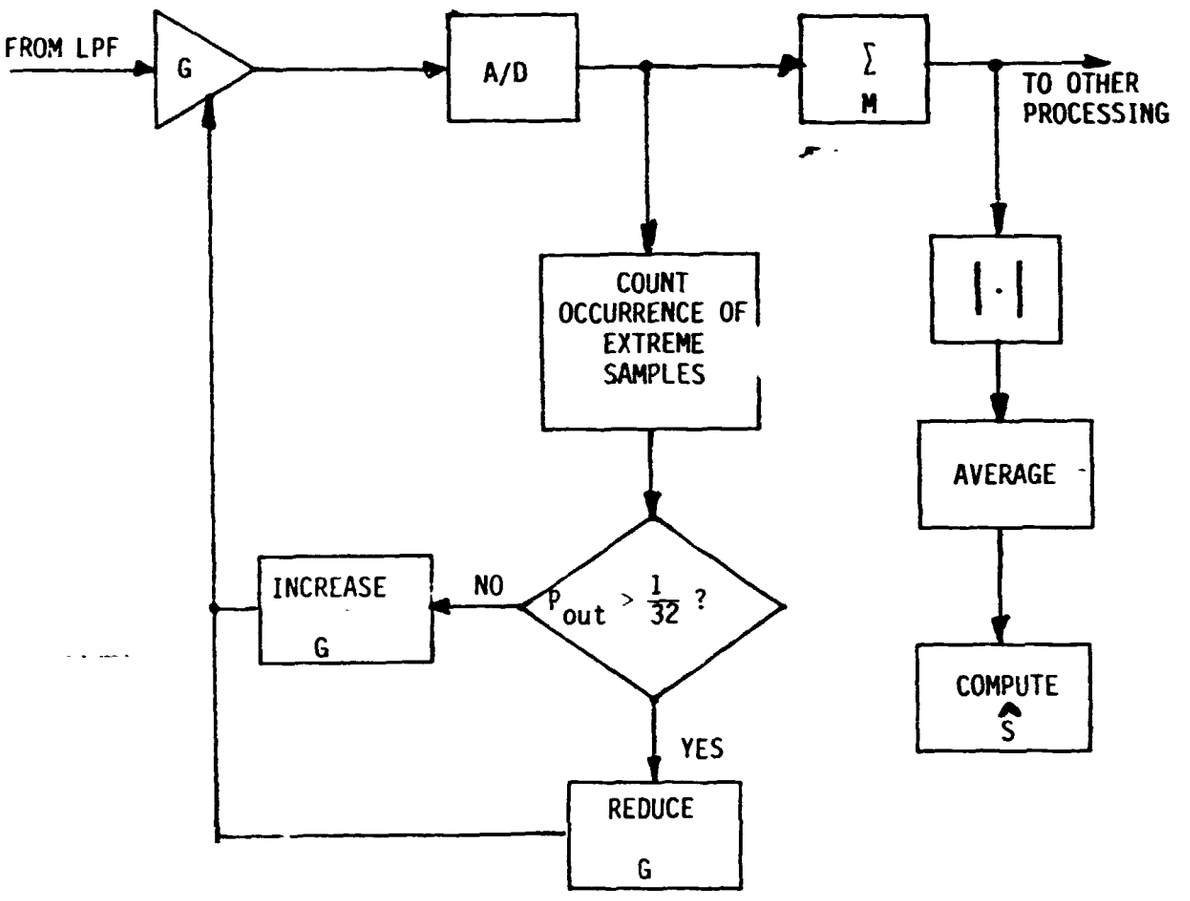


Figure H.9. AGC and Signal Strength Indicator Algorithm.

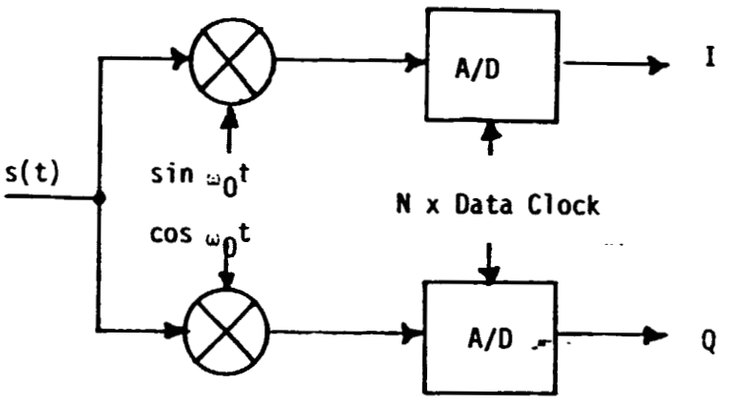
APPENDIX I

BASEBAND VS IF I-Q SAMPLING

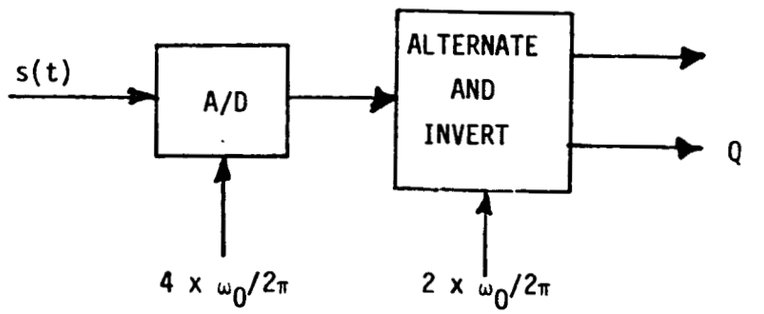
Figure I.1 shows two approaches to obtain inphase and quadrature (I&Q) samples of an IF signal $s(t) = \sqrt{2P}\, a(t) \sin \omega_0 t$. The first approach is straightforward, it uses two A/D converters to sample the demodulated baseband outputs after the mixing operation. The second approach samples at 4 x the IF frequency and yields 2 pairs of I-Q samples every IF cycle as shown in the example in Figure I.2. Notice that the I and Q samples have to be inverted alternatively because of the sign change of the IF carrier every half a cycle.

Obviously, the IF approach saves hardware, namely, 2 mixers and 1 A/D converters. However, there are disadvantages. First of all, the sampling speed is currently a technology constraint. Given a fixed sampling speed the baseband technique offers two times more samples, hence two times more resolution in time. Secondly, in the IF sampling scheme, the samples must be taken precisely at multiples of $\pi/2$ of the IF carrier. However, for data detection purpose, the system performance can be enhanced if the samples are taken coherent with the data clock as done in the baseband scheme. This advantage becomes more apparent as the number of samples/symbol decreases.

Let us consider an example. A state-of-the-art commercial flash A/D converter has a conversion speed of about 60 MHz. For 6 Msps operation there are 10 samples/symbol. With the I-Q sampling, there are only 5 samples per channel. Even if the bit sync can operate perfectly, the inherent time quantization error has a peak-to-peak value of 1/5 = 20% since the sampling instants are forced to be coherent with the IF

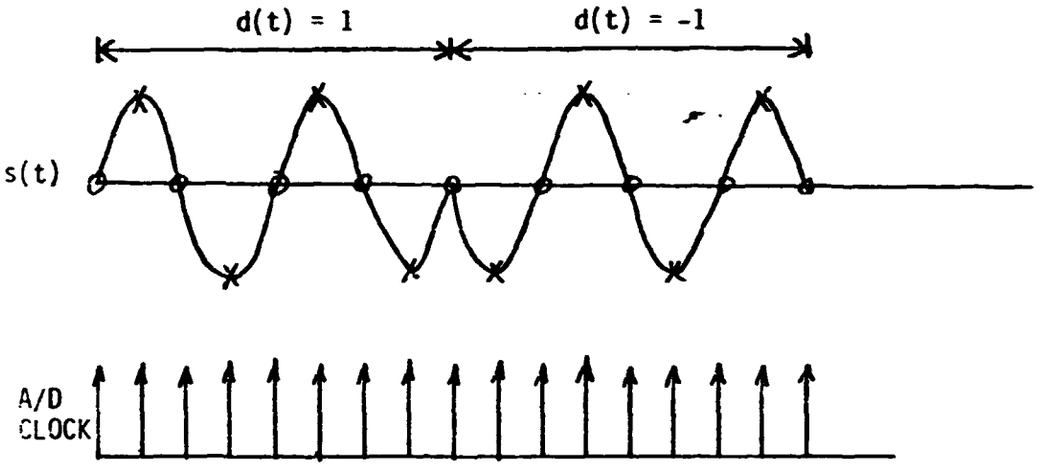


(a) Baseband I-Q Sampling



(b) IF I-Q Sampling

Figure I.1. I-Q Sampling ($s(t) = \sqrt{2P}\, d(t) \sin \omega_0 t$).



o = I-Samples

x = Q-Samples

Figure I.2 IF I-Q Sampling.

carrier instead of the bit sync. This also affects the integrate-and-dump detector performance. On the other hand, since the sampling clocks in the baseband technique are controlled and adjusted* by the bit syncs, the quantization error can be made to be very small.

Of course, at low data rate where there are many samples/symbol, the IF technique becomes attractive.

*To the resolution of the synthesizer providing the clock, which can be made very fine.

APPENDIX J

MANCHESTER SYMBOL AMBIGUITY RESOLUTION

When the baseband data is Manchester-coded, there is a need to resolve the ambiguity associated with the symbol alignment. Figure J.1 illustrates this problem. Depending on the bit alignment, the symbol stream can be interpreted either as all ones or zeros in this example. If the data symbols are correctly aligned, there is always a transition in the middle of the symbol. If the data symbol is purely random, then the occurrence of a transition in the middle of the misalignment symbol is only 50%.

By keeping track of the number of transitions using the two different symbol alignments, one can resolve this ambiguity statistically. Let us assume that we keep track of $M = 2^N$ symbols and see which symbol alignment yields the most mid-symbol transitions. Let p_c be the probability of error in making a correct decision on the half symbol so that

$$p_c = \frac{1}{2} \operatorname{erfc} \sqrt{\frac{1}{2} E_s/N_0}$$

A transition is declared if the first half of the detected symbol is different from the second half. Given that the correct symbol alignment is used, we can easily determine the following probabilities

$$p_1 = (1-p_c)^2 + p_c^2$$

$$q_1 = 1-p_1$$

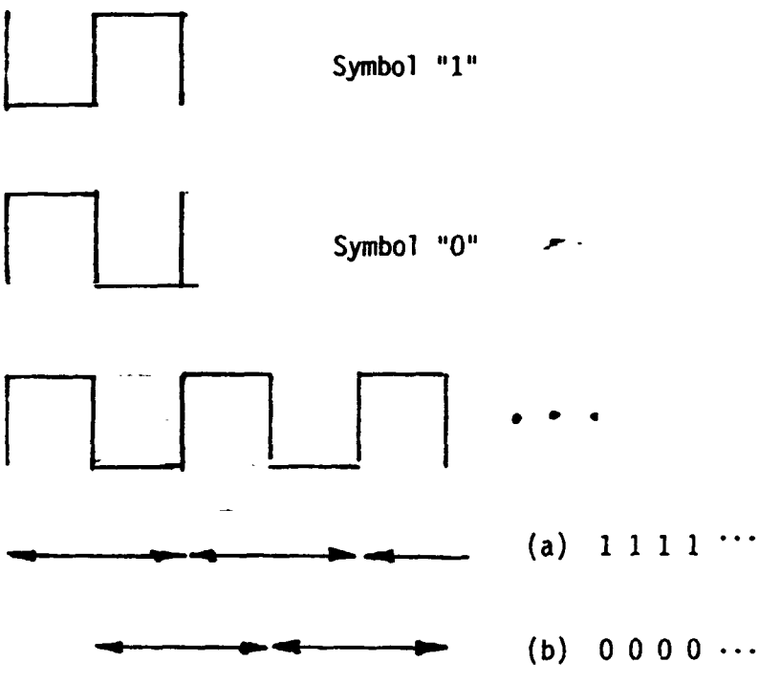


Figure J.1. Manchester Symbol Ambiguity

of detecting the transition (p_1) and not detecting the transition (q_1) at the middle of the symbol. The probability of detecting a transition at the wrong symbol alignment is

$$p_2 = p_T p_1 + (1-p_T)q_1$$

where p_T is the probability of having a transition. Notice that p_T is related to the data transition density of the symbol pattern, p_t via $p_T = 1-p_t$. We also use $q_2 = 1-p_2$ to denote the probability of not detecting a transition.

After observing for $M = 2^N$ symbols, the probability distribution of the number of observed transitions k, at the correct alignment is

$$P_1(k) = \binom{M}{k} p_1^k q_1^{M-k}$$

And for the incorrect alignment,

$$P_2(\ell) = \binom{M}{\ell} p_2^{\ell} q_2^{M-\ell}$$

The probability of picking the incorrect alignment based on the number of observed transition in both cases is the error of the ambiguity resolution process and is given by

$$P_E = \text{Prob}(k \leq \ell)$$

$$= \sum_{\ell=1}^{M} \sum_{k=1}^{\ell} P_1(k) P_2(\ell)$$

Figure J.2 shows the probability of incorrectly aligning the Manchester symbol. This is computed for the worst case data transition density p_t = 0.125 per the TDRSS requirement. As an example, for a worst case E_b/N_0 = 5 dB, P_c < 0.05 so that the ambiguity can be resolved with an error probability less than 10^{-9} if 1,000 bits are used.

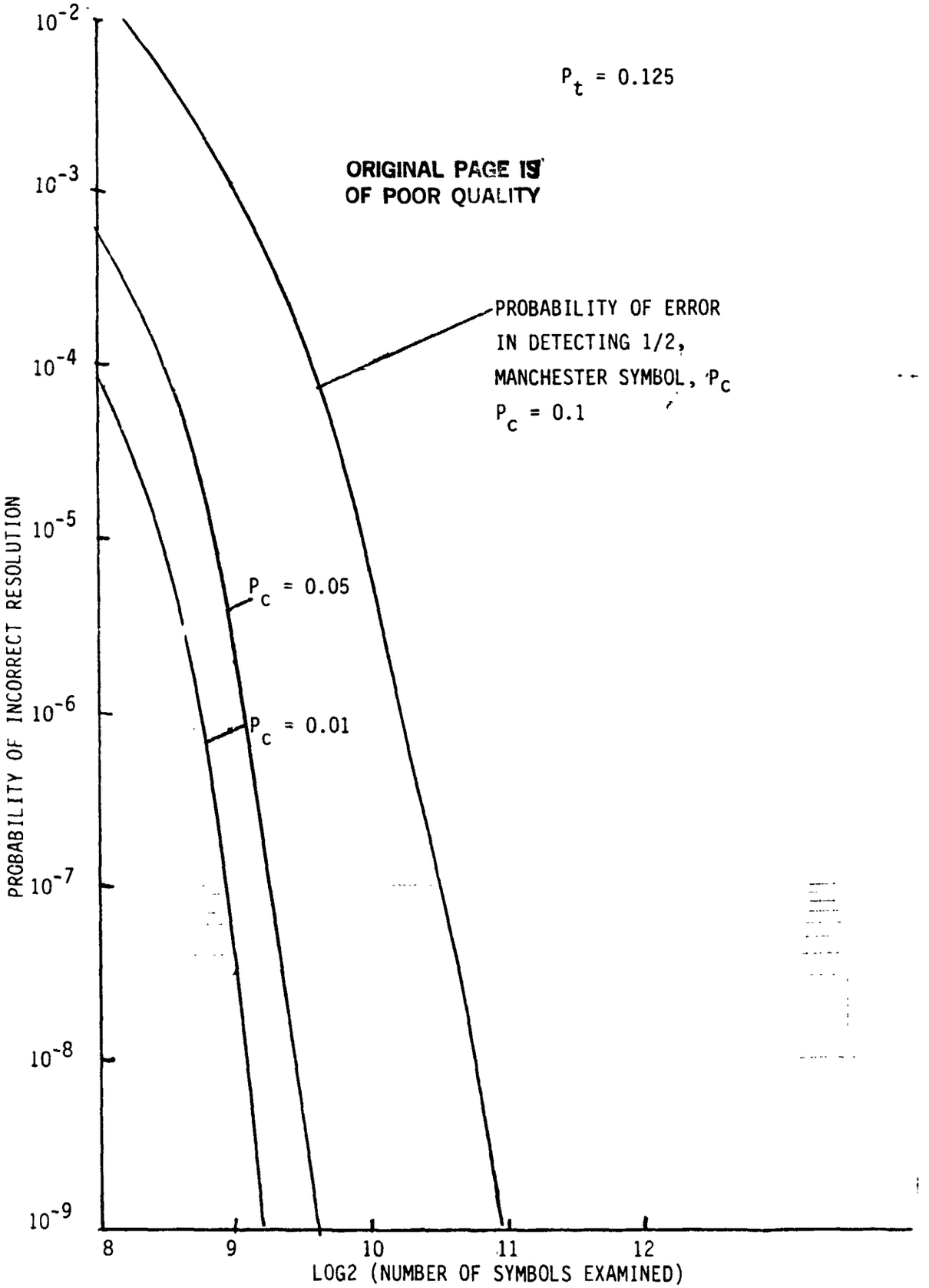


Figure J.2. Manchester Symbol Ambiguity Resolution Performance.

APPENDIX K

LOCK INDICATION

Since the AIRS operation requires switching to different configurations at various stages of the receiver operation, means must be provided to monitor and verify whether what stage is the receiver operating at. This is the task of the lock indicators. In AIRS, lock indication is derived from comparing two signals, (selected to be insensitive to other system conditions), of which one signal will be high relative to the other when the system under consideraiton is in lock, and vice versa. This avoids, for example, the need to establish a fixed absolute voltage reference, which may be difficult to maintain during acquisition.

As an example, the lock indicator for the carrier loop is obtained by comparing the in-phase output (proportional to $|\cos \phi|$) and the quadrature output (proportional to $|\sin \phi|$) of the A/D subsystem. Since the gain of the receiver is identical for both signals, the relative magnitude of the two signals is independent of the receiver power level or whether the AIRS is in the acquisition or the tracking mode.

Figure K.1 shows the signals to be compared for lock indication. The signals used for the FLL is proportional to $|\sin \Delta\omega T_F|$ and $|\cos \Delta\omega T_F|$ where T_F is the update speed. Before the FLL acquires, both signals are of comparable value. After the AIRS has acquired, $|\sin \Delta\omega T_F|$ is very small compared to $|\cos \Delta\omega T_F|$.

For the bit sync, the signals are comparable if the bit sync is not locked. Once locked, the full-bit ACM output is much larger than the mid-bit output.

LOOP TYPE	COMPARISON FILTERED* SIGNALS
CARRIER LOOP	$\|\cos \phi\|$ vs $\|\sin \phi\|$
FREQUENCY LOCK LOOP	$\|I_k Q_{k-1} - Q_k I_{k-1}\|$ vs $\|I_k I_{k-1} + Q_k Q_{k-1}\|$
BIT SYNC	|FULL-BIT ACM| vs |MID-BIT ACM|
AGC**	MEASURED vs DESIGNED OUT OF RANGE PROBABILITY

*Means accumulated M times.

**Really a fixed threshold scheme; however, P_{out} is not a function of input conditions.

Figure K.1. Lock Indicator Signals for AIRS Subsystems.

The lock indicator signal for the AGC is a little different. The signal measures the probability that a A/D sample is out of range. If the AGC is set incorrectly, then this probabil. y will be different from the design value (e.g. 1/32). If the gain is too high then the probability will be greater than 1/32, and vice versa. When the system is in lock, then the measured value will be within a prescribed range around the design probability.

Analysis

The performance of these lock indicators can best be determined via analysis than via a Monte Carlo simulation since the latter is very time consuming in the range of interest. The analysis is not difficult and is straightforward. Figure K.2 shows the analytical approach applicable to AIRS. These procedures can be followed during the final design phase of the AIRS. Because M is usually large, the law of large number applies and $\sum |A|$ and $\sum |B|$ can be replaced by Gaussian random variables. In that case, the analysis can be simplified further. As a matter of fact, standard results can be used and are found in radar literature under the topic of noncoherent integration.

1. IF UNLOCK, $E|A| \approx E|B|$

   IF LOCK, $E|A| >> E|B|$

2. DETERMINE PDF OF $|A|, |B|$

3. ACCUMULATE $|A|$ AND $|B|$ M TIMES, DETERMINE PDF

4. COMPARE $\sum |A| / \sum |B|$ WITH THRESHOLD, DETERMINE P_{FA} AND P_D

5. REPEAT 3 AND 4 UNTIL SATISFIED

Figure K.2. Analytical Approach to Lock Indicator Design.

APPENDIX L

MEAN SLIP TIME

The mean time to first slip τ for a CW PLL is given by [1] the approximation

$$\tau = \frac{\pi e^{2\alpha \cos \phi_{ss} + 2\beta\phi_{ss}}}{4B_L \cos \phi_{ss} \cosh \pi\beta}$$

where α = linearized loop signal-to-noise ratio, ϕ_{ss} is the steady state phase error, and $\beta = \alpha \sin \phi_{ss}$. If we approximate the BPSK and QPSK loop S-curves by sin 2ϕ and sin 4ϕ respectively, then with a simple substicution, the mean time to first slip can be shown to be

$$\tau = \frac{\pi e^{\frac{2\alpha}{2} \cos N\phi_{ss} + \frac{2\beta}{N} N\phi_{ss}}}{4B_L (\cos N\phi_{ss}) \cosh \pi\beta/N}$$

where $\beta = \frac{\alpha}{N} \sin N\phi_{ss}$ and N = 2 (BPSK) or 4 (QPSK). For simplicity we can assume that ϕ_{ss} is zero since it is negligible with a third-order loop for the TDRSS Doppler profile. It is instructive to express α in terms of the steady state rms phase jitter σ_ϕ^2. Then we have an approximate formula for the mean time to first slip

$$\tau = \frac{\pi}{4B_L} e^{2/N^2 \sigma_\phi^2}$$

where N is the number of phases in the modulation scheme and σ_ϕ^2 is in radians.

As an example, let B_L = 50 Hz. Then to achieve a 90 minute mean time to first slip, we require

$$N^2 \sigma_\phi^2 < 2/\ln(4B_L \tau/\pi)$$

or $\sigma_\phi < 22.7^0/N$. Hence BPSK requires $\sigma_\phi < 11.3^0$ and QPSK requires $\sigma_\phi < 5.7^0$ to meet the slip time requirement.

Reference

[1] C. M. Chie, "New Results on Mean Time-to-First-Slip for a First-Order Loop," submitted to IEEE Trans. Comm., 1984.