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5101-247
Flat-Plate
Solar Array Project

DOE/JPL-1012-98
Distribution Category UC-63b

Proceedings of the Flat-Plate Solar Array Project Research Forum on The Design of Flat-Plate Photovoltaic Arrays for Central Stations

(December 5, 6, 7, 8, 1983, at Sacramento, California)

Prepared for
U.S. Department of Energy
Through an Agreement with
National Aeronautics and Space Administration
by
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

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The JPL Flat-Plate Solar Array Project is sponsored by the U.S. Department of Energy and is part of the Photovoltaic Energy Systems Program to initiate a major effort toward the development of cost-competitive solar arrays.

This publication reports on work done under NASA Task RE-152, Amendment 66, DOE / NASA IAA No. DE-AI01-76ET20356.

ABSTRACT

The Flat-Plate Solar Array Project, managed by the Jet Propulsion Laboratory for the U.S. Department of Energy, has focused on advancing technologies relevant to the design and construction of megawatt-level central-station systems. Photovoltaic modules and arrays for flat-plate central-station or other large-scale electric power production facilities require the establishment of a technical base that resolves design issues and results in practical and cost-effective configurations.

The Central Station Research Forum addressed design, qualification and maintenance issues related to central-station arrays derived from the engineering and operating experiences of early applications and parallel laboratory research activities. Technical issues were examined from the viewpoint of the utility engineer, architect-engineer and laboratory researcher. The forum included presentations on optimum source-circuit designs, module insulation design for high system voltages, array safety, structural interface design, measurements and array operation and maintenance.

The Research Forum focused on current capabilities as well as design difficulties requiring additional technological thrusts and/or continued research emphasis. Session topic summaries highlighting major points during group discussions, identifying promising technical approaches or areas of future research, are presented.

FOREWORD

The Jet Propulsion Laboratory's Flat-Plate Solar Array Project (FSA), funded by the U.S. Department of Energy (DOE) as part of the National Photovoltaics Program, provides the focus for research on flat-plate photovoltaic arrays.

Establishment of the technology base for flat-plate central station arrays continues as a major thrust of the national program and has recently increased in importance with the construction of several megawatt-level central-station systems. These systems, funded both by private enterprise and by federal grants, have highlighted the capabilities and deficiencies of current array technologies. In parallel, ongoing research has made substantial progress in resolving some of the technical issues related to central-station arrays.

The purpose of the FSA Research Forum on the Design of Flat-Plate Photovoltaic Arrays for Central Stations was to bring forth the design, construction and initial operating experience from early applications together with the latest results of laboratory research activities. A key objective is the sharing of technical experience, including identification of promising technical approaches, remaining problem areas, and needed research.

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David H. Otth	Co-Chairman
Russell S. Sugimura	Co-Chairman
Mary Phillips	Research Forum Coordinator
David Tustin	Audio & Graphics Coordinator

DESIGN OF FLAT-PLATE PHOTOVOLTAIC ARRAYS FOR CENTRAL STATIONS RESEARCH FORUM

December 5-8, 1983

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SESSION I

SOURCE-CIRCUIT DESIGN ISSUES

R.R. Addiss, Chairman

OMIT TO P.7

SESSION I

SOURCE-CIRCUIT DESIGN ISSUES

Chairman: R.R. Addiss, Jr., Solar Power Corp.

SUMMARY

The issues addressed can be divided roughly into three categories: maximizing fault tolerance, maximizing power output, and minimizing cost. Factors affecting fault tolerance are: type of cell or module failures, hot-spot heating, and use of by-pass diodes. Factors affecting power output include mismatch and shadowing losses. And finally, the current and voltage levels of the source circuit affect the balance of system (BOS) costs.

In the first paper, R.G. Ross, Jr., of the Jet Propulsion Laboratory (JPL) reviewed past work in many of these areas. Concentrating on fault tolerance, his analysis shows that paralleling cell strings within a series block will actually decrease fault tolerance unless a very large number (at least eight, but preferably many more) are paralleled, but that a single series string has the greatest fault tolerance. The number of cells in series within the block should be minimized (more frequent cross ties and bypass diodes). Fewer than four or five should be avoided only if shorted cells can be a significant failure mode.

From his work on the SMUD verification array, which contains multiparallel cells, C.C. Gonzalez of JPL discovered a new mode of hot-spot heating not encountered in single series strings. Because the effective shunt resistance of cells tends to be low, the cells can pass currents under reverse bias that significantly exceed their short-circuit current, provided the current source is available. In a single series string of cells, only the short-circuit current of a single cell is available, but with multiparallel cell strings, the current generated by the several paralleled cells is available to feed a single cell. In effect, the cell having the lowest shunt resistance will hog most of the current. Gonzalez reported finding hot-spot temperatures 25°C to 50°C higher than those attainable in single series strings when the array under test was subjected to worst-case shadowing. The problem is alleviated by using fewer cross ties. Gonzalez says "more than three cells per cross tie" are needed. But how many more? Some work to better define these conditions would be most useful. Until then, by taking these results in conjunction with Ross's work, one can be reasonably confident that somewhere between five and 10 cells per cross tie will not be too far from optimum.

J.P. Rumburg of ARCO Solar Industries described the extensive program at ARCO Solar Industries to investigate hot-spot heating in complex series-parallel arrays. Included in a detailed statistical characterization of cells, characterization of shadow configurations, and the development and validation of analytical models. Most important will be the results of empirical tests to be performed on utility-scale panel configurations. Publication of their findings will be a valuable contribution to the industry.

N.F. Shepard, Jr., outlined the general rules for the design and selection of bypass diodes. After reviewing the functions the diodes perform, he clearly defined the boundary between the module designer's concerns and those of the array designer. The module designer must deal only with the diode requirements at the submodule level, i.e., when two or more diodes per module are required. He must use only p-n junction diodes, to ensure that any diodes the array designer may incorporate at the module level will turn on first. The array designer's responsibilities begin at the module level, so he is free to choose the diodes that best meet his requirements for the particular series-parallel arrangement he has designed. Shepard also presented the design data needed by a module designer who wants to incorporate chip diodes mounted on heat-spreader plates directly into the module laminate. He also proposed a means by which an array designer might incorporate a diode within a harness connector, and pointed out its advantages (e.g., no arcing upon disconnect) and limitations (e.g., 25-A maximum current).

The dependence of mismatch loss on the allowed variations of the different cell (module) parameters and the different cell (module) interconnect schemes has not yet been studied sufficiently to give any clear understanding of how much power loss is likely to result from any particular source-circuit design. T.J. Lambarski of BDM Corp. reviewed the limited number of studies that have been done. With only one exception, all of these are based on computer modeling analyses in which only one or a very few of the possibly significant parameters were allowed to vary. (Part of the problem in getting a complete understanding is the large number of parameters that influence the results significantly.) All address photocurrent variations, and generally agree that 1% to 2% mismatch loss is achievable with good module matching, but mismatch loss may increase up to 7% (or higher) with poor module matching. (What constitutes "good" and "poor" matching may vary somewhat with the model used.) In the one detailed experimental study of the 100-kW Beverly PRDA system, where modules were initially matched in 5% bins of shot-circuit current, the mismatch loss was found to be 1 1/2% as configures with five modules in parallel. Reconfiguring the system to single module strings reduced mismatch loss to under 1%. Thus, both experimental and theoretical studies show that $\simeq$ 1% mismatch loss is achievable. But it is not clear how to guarantee this, nor whether it is compatible with the optimum fault-tolerant designs or with the characteristic parameters of non-sheet-silicon technologies.

R. Spencer of Acurex Corp. addressed the still more difficult problem of minimizing mismatch loss in arrays containing a mix of modules from different manufacturers. If the system is large enough to have several inverters, then arranging for one inverter per manufacturer not only will reduce mismatch loss, but also will eliminate some constraints on module specifications (e.g., operating voltage). If not, then additional constraints must be imposed on the module specs, but Spencer warned against over-specifying the module to the extent that the manufacturer is not free to produce a cost-effective design. A primary rule (which should be self-evident) is: never mix hardware from different manufacturers in the same source circuit.

In the final paper of this session, G.T. Noel of Battelle's Columbus Laboratories presented the results of his study of the dependence of BOS costs

on source-circuit current and voltage levels. Three voltage levels (400 V; ± 400 V; ± 1000 V) and four current levels (15, 30, 45, and 60 A) were addressed. At all voltage levels, the lowest current (15 A) had significantly higher costs than any of the higher current levels. Also, the highest voltage (± 1000 V) had significantly higher costs than either of the lower voltages except at the highest current level (60 A), where the costs become almost independent of voltage level. The generally higher costs of the highest-voltage systems result from the higher insulation levels required for the bypass diodes and interconnect wiring (cable insulation), and the cost of existing high-voltage disconnect switches. Noel believed that the latter could be overcome if hardware development could be stimulated.

Reviewing the present status of source-circuit design, the requirements for fault tolerance appear to be reasonably well defined, although refinements of the analyses are always welcome. Based on performance alone, a single series string of cells is preferred, but cost-related factors (number of bypass diodes; minimizing self-shadowing losses) may dictate paralleling of cells. In that case, the maximum number in parallel that can be accommodated should be used to approach the performance of a single series string. Designs that result in the lowest BOS cost appear to be compatible with the fault-tolerant designs. But we are not sure that this is also true for low mismatch loss. We are not yet able to predict mismatch loss with much confidence. This subject clearly requires more study. Still more important is the need to verify the analytical results experimentally, on installed systems. In this regard it is disappointing to see large systems being installed that do not take full advantage of the analytical results presently available.

SOURCE-CIRCUIT DESIGN OVERVIEW

R.G. Ross, Jr.
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The source circuit is the fundamental electrical building block of a large central-station array; it consists of a series-parallel network of solar cells that develops full system voltage. The array field is generally made up of a large number of parallel source circuits.

Source-circuit electrical configuration is driven by a number of design considerations, which must be considered simultaneously. Examples include:

(1) Providing fault tolerance against open-circuit cell failures.

(2) Providing fault tolerance against short-circuit cell failures.

(3) Minimizing the (mismatch) power loss due to cell and module electrical performance variation.

(4) Providing fault tolerance to hot-spot heating due to local shadowing and circuit failures.

(5) Minimizing the power loss associated with expected (e.g., morning and afternoon) shadowing.

(6) Being consistent with efficient module cell layout (module series-paralleling).

(7) Being consistent with effective panel and array layout.

(8) Minimizing intermodule and array wiring complexity and cost.

(9) Accommodating fault diagnosis measurements and replacement of failed modules.

Of the above considerations, let us consider two key ones in detail: array fault tolerance and hot-spot heating endurance.

Array Fault Tolerance

Central-station photovoltaic arrays require large numbers of series solar cells to achieve system operating voltages between 700 and 1500 volts. Without circuit redundancy elements, such as series-paralleling and bypass diodes, high-voltage arrays would be highly sensitive to typical open-circuit cell failures, which average around one per 10,000 per year. Design techniques have been developed to allow selection of appropriate levels of circuit redundancy and to predict the degree of expected plant power degradation

versus circuit configuration (References 1 and 2). Economic considerations generally require that power degradation be maintained below 0.2% per year, i.e., 1% in five years. As indicated in the accompanying table, this can be achieved by dividing each source circuit into 100 to 200 series blocks with bypass diodes around each. Although the number of parallel cell strings is not critical, optimal fault tolerance is achieved with single-string or highly paralleled (eight or more cells in parallel) source circuits. Excessive cross-tying (more frequently than every five cells) is discouraged because of increased sensitivity (decreased tolerance) to the presence of short-circuited solar cells.

Hot-spot Heating

Hot-spot heating occurs when a solar cell is forced to pass a current greater than its short-circuit current. This circumstance typically arises in a localized region of the array when the short-circuit current level of the region is reduced below that of the surrounding array due to partial shadowing, local soiling, or cell breakage.

The resulting heating level is proportional to the reverse voltage developed across the affected region and to the current passing through it. As a result, worst-case heating generally occurs under conditions of partial shadowing when irradiance (current) levels are high. The most effective means of controlling hot-spot heating levels is to limit the maximum reverse voltage by means of bypass diodes connected in parallel around the solar cells. With a bypass diode present, the maximum reverse voltage is limited to the output voltage of the bypassed cells.

The choice of number of bypassed cells per diode is made to limit maximum module heating levels to below around 120°C. At temperatures higher than this the module polymeric encapsulant degrades rapidly. Most module designs require bypass diodes every 10 to 20 series solar cells.

References

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2. Flat-Plate Photovoltaic Module and Array Circuit Design Optimization Workshop Proceedings, JPL Internal Document No. 5101-170, Jet Propulsion Laboratory, Pasadena, California, May 19-20, 1980.

SOURCE-CIRCUIT DESIGN OVERVIEW

JET PROPULSION LABORATORY

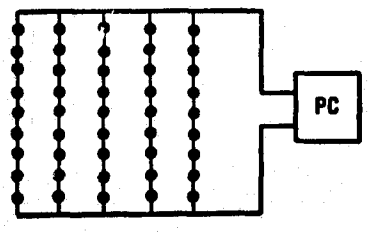
R.G. Ross, Jr.

Source-Circuit Design Requirements

- **Series cells to achieve system operating voltage**
- **Minimize losses due to cell performance variation**
  - **Open-circuit cells**
  - **Short-circuit cells**
  - **Mismatched cells**
- **Protect modules from hot-spot heating damage**
- **Minimize power loss due to shadowing**
- **Minimize intermodule and field wiring costs**
- **Minimize maintenance costs**
  - **Fault identification and location**
  - **Repair and replacement**

Effect of Cell Failures on Array Degradation

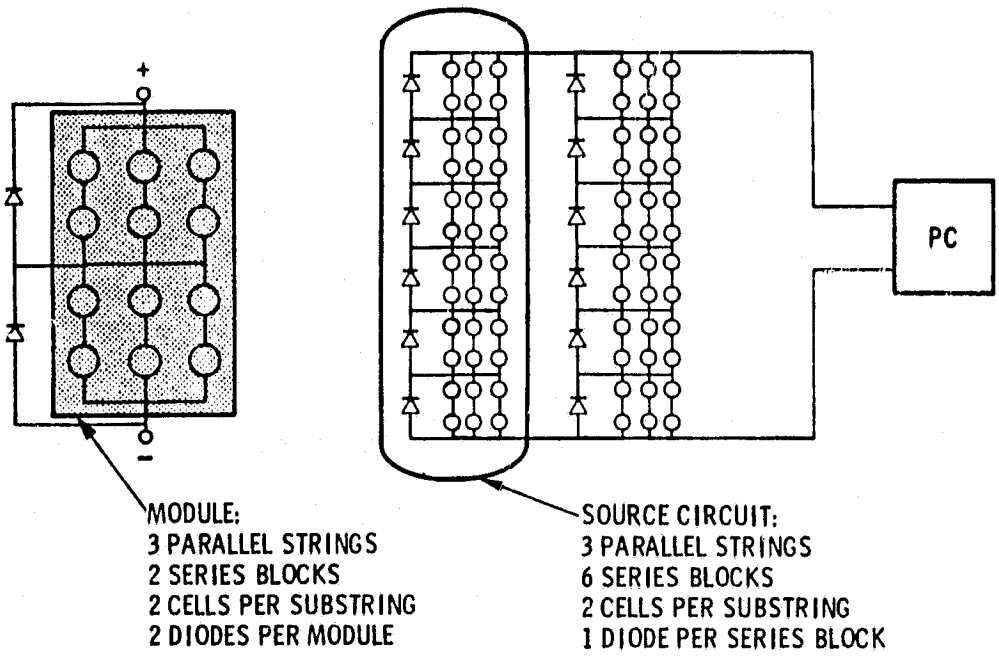
(NO CIRCUIT REDUNDANCY)
(CELL FAILURE RATE R = 0.0001/YEAR)



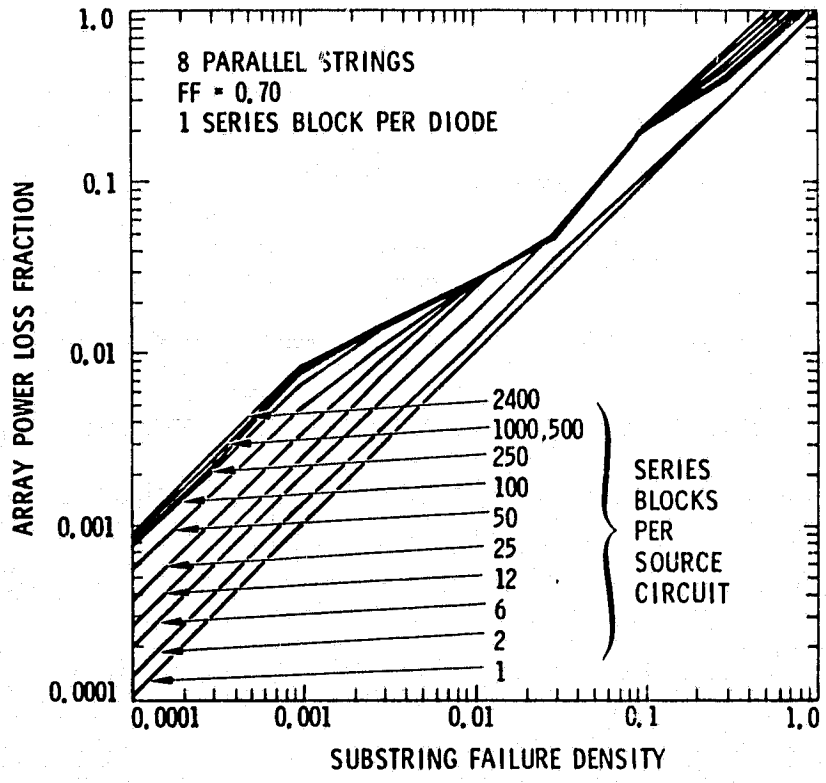
ARRAY VOLTAGE	SERIES CELLS (S)	POWER LOSS AT 5 YEARS
15	36	1.8%
150	360	16.5%
1500	3600	83.5%

POWER LOSS = 1 - [1- (YEARS X R)]^S

Series-Parallel Nomenclature



Array Power Loss vs Substring Failure Density

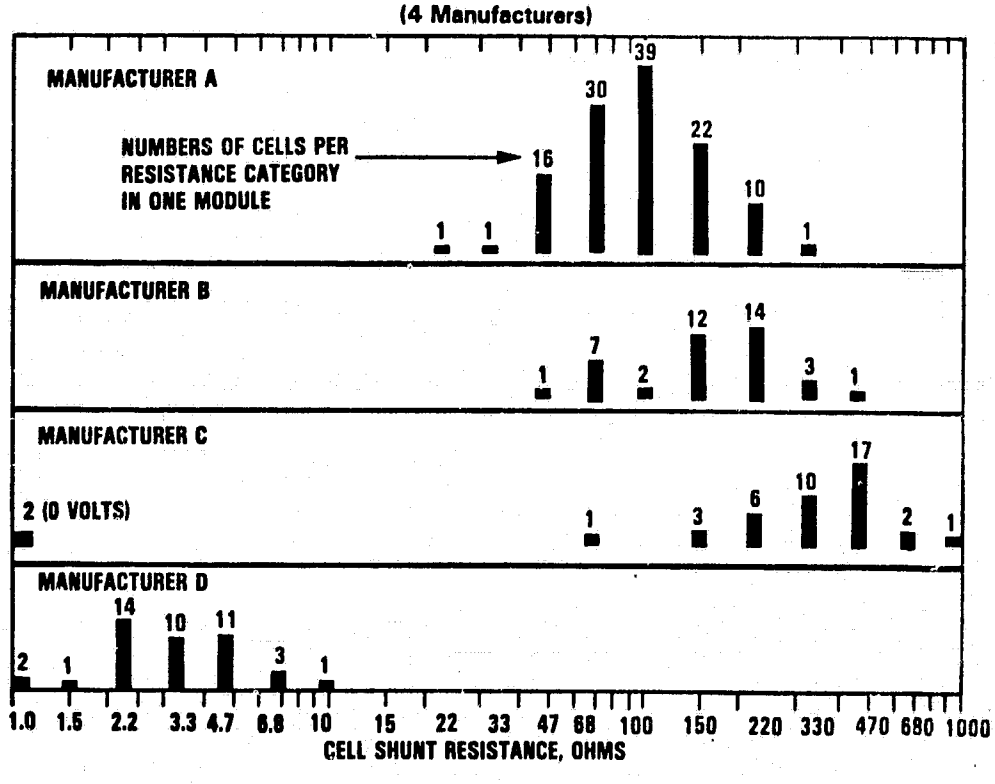


Fraction of Power Loss After 5 Years vs Circuit Redundancy

- 450-Volt Source Circuit
- One Diode Per Series Block
- Cell Failure Rate = 0.0001

CELLS PER SUBSTRING	SERIES BLOCKS	CELLS IN PARALLEL				
		1	4	8	16	
1000	1	0.390	0.390	0.390	0.390	UNACCEPTABLE HOT-SPOT HEATING
50	20	0.023	0.110	0.048	0.032	
20	50	0.011	0.050	0.025	0.015	
10	100	0.005	0.022	0.013	0.008	OPTIMUM DESIGN REGION
5	200	0.003	0.010	0.007	0.004	
2	500	0.001	0.004	0.003	0.002	SENSITIVE TO SHORTED CELLS

Typical Cell Shunt Resistances



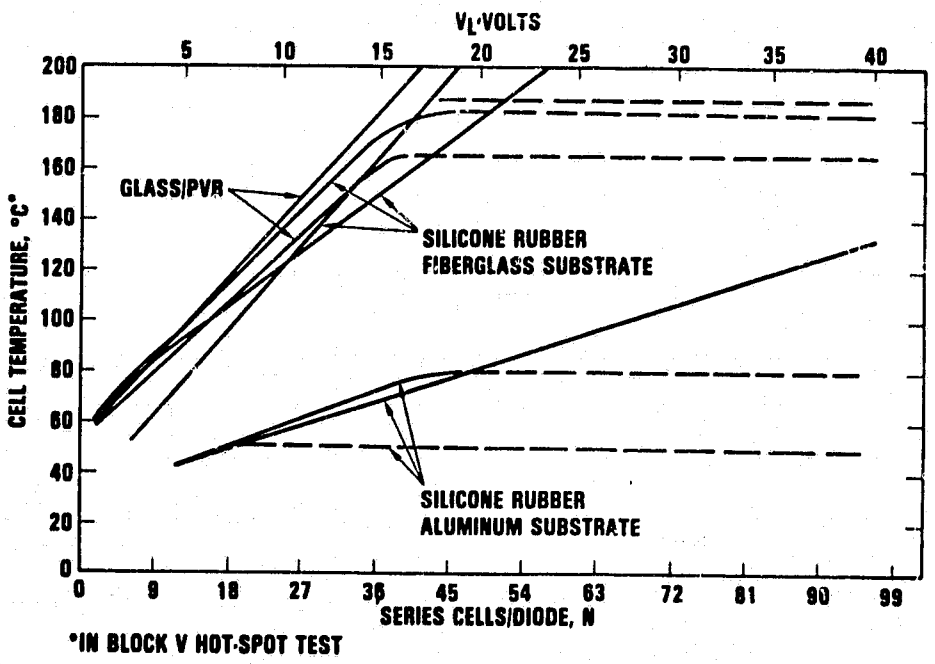
Observed Module Response vs Cell Temperature

MODULE ENCAPSULANT	CELL HOT-SPOT TEMPERATURE °C 100 120 140 160 180
SILICONE RUBBER WITH HEAT RESISTANT SUBSTRATE	CELL BREAKDOWN; CELL BREAKDOWN; CRACKED CELL
GLASS SUPERSTRATE WITH PVB	ONSET OF CARBONATION; CARBONATION OVER HALF OF CELL; ENCAPSULANT DISCOLORED AND SMOKING
ENCAPSULANT WITH OUTGASSING PROBLEM	MULTIPLE CELL CRACKS AND ENCAPSULANT DELAMINATION; ONE CELL SURVIVED TO 180°C BEFORE CRACKING AND SHORTING

CONCLUSION:

- **Hot-spot temperatures should be kept below approximately 120°C**

Measured Hot-Spot Temperature vs Number of Series Cells per Diode



*IN BLOCK V HOT-SPOT TEST

Source-Circuit Conclusions

- **Array fault tolerance requires source circuits with $\gtrsim$100 series blocks (with diodes) and with single, or 8 or more, cells in parallel**

- **Hot-spot protection suggests bypass diodes every 10 to 20 series cells**

D2

N84 32685

SOURCE-CIRCUIT DESIGN WITH MULTIPLE PHOTOVOLTAIC MANUFACTURERS

Robert Spencer
Acurex Corp.
Mountain View, California

This presentation covers the problems associated with source circuit design for use in PV hardware of different manufacturers or processes. The solutions presented for these problems are those developed for the second MW of the Sacramento Municipal Utility District (SMUD) project. Panels from up to four manufacturers will be used to produce 1.2 MW dc.

Sources of Interactive Problems

The basis of problems arising from several PV types in an array field is the varying performance of dissimilar materials. If two products could be perfectly matched at some set of conditions, they may demonstrate mismatch at changed insolation, temperature, or irradiance spectrum. Different reverse characteristics may lead to severe hot-spot problems. In addition, differences in module dimension or interconnection topology cause increased balance-of-system (BOS) complexity and cost. Finally, manufacturing uncertainties can produce products different from the manufacturer's intentions.

Potential Approaches

No single manufacturer or technology controls the PV market, nor does any have the capacity to support it unilaterally. Therefore, approaches that allow for the differences in products while minimizing standardization requirements must be evaluated. Some standards must, however, be generated to enable systems designers to use available equipment. Three options are feasible for array fields with multiple vendors. In no case may different hardware be mixed within a source circuit. Hence, the options are one inverter PV manufacturer, one dc regulator manufacturer, or a single inverter and increased standardization.

Design Impact

For all of these approaches, standardized physical and electrical interfaces are required to allow standard BOS design. This can be accomplished at the panel level, which leaves quite a bit of flexibility for the module dimensions. At present, and with current array field sizing, it is not cost-effective to use multiple converters or regulators. Therefore, the field voltage will be the same for all source circuit designs. Since a small variability exists in the number of panels in each source circuit, standard panel voltages must be adopted. For the SMUD design, there are eight standard voltages. The maximum mismatch power losses thus total less than 2% and may be improved as the vendors are selected.

SOURCE-CIRCUIT DESIGN WITH MULTIPLE PHOTOVOLTAIC MANUFACTURERS

ACUREX CORP.

Robert Spencer

System Design Constraints

MAXIMUM ANNUAL ENERGY AND CAPACITY FOR INSTALLED COST

ONE MECHANICAL DESIGN PER FIELD

ONE VOLTAGE AT A TIME PER INVERTER

LOW ENOUGH VOLTAGE TO MINIMIZE GROUND FAULTS

ADEQUATE PARALLELING TO YIELD HIGH RELIABILITY

LOW LOSSES - MISMATCH/RESISTIVE/SOILING

DON'T BUY "SPECIALS"

Hardware Differences

PHYSICAL

- DIMENSIONS
- WEIGHT
- TOLERANCES
- MOUNTING INTERFACE
- STRENGTH; IMPACT & WIND LOAD

ELECTRICAL

- CURRENT
- VOLTAGE
- SERIES RESISTANCE
- SPECTRAL RESPONSE
- SERIES/PARALLEL CONFIGURATION
- TEMPERATURE COEFFICIENTS

Problem Areas

MECHANICAL

IF THE SYSTEM OWNER BUYS PV MODULES, HE WILL DESIGN A DIFFERENT SUPPORT STRUCTURE FOR EACH MANUFACTURER.

- NO LEARNING CURVE/MASS PRODUCTION BENEFITS ON BOS COST
- MORE CONTRACTOR COST FOR INSTALLATION
- MORE COST FOR SPARES

IF THE SYSTEM OWNER BUYS PANELS WITH STANDARD DIMENSIONS, HE MUST AVOID OVER-CONSTRAINT OF THE MANUFACTURER.

- MAXIMUM LENGTH, WIDTH AND WEIGHT
- STANDARD MOUNTING INTERFACE
- STANDARD LOADING REQUIREMENTS
- CORROSION PROTECTION

IN DEFINING A STANDARD, ASSESS IT'S APPLICABILITY TO OTHER SYSTEM DESIGNS

ELECTRICAL

STANDARD CAN'T CONSTRAIN:

- EFFICIENCY
- THERMAL PERFORMANCE
- SPECTRAL RESPONSE
- SERIES RESISTANCE

STANDARD SHOULD CONSTRAIN:

VOLTAGE - AT PCU BUS	- LIMIT THE NUMBER OF PCU's
SERIES/PARALLEL CONFIGURATION	- MAINTAIN RELIABILITY
SHADOWING WITHSTAND	- HOT SPOT HEATING
VOLTAGE ISOLATION	- GROUND FAULT

STANDARD MUST ADDRESS:

- MODULE/PANEL SORTING
- MISMATCH AND RESISTIVE LOSSES ON PANEL
- GROUNDING
- MAINTENANCE
- MISMATCH AND RESISTIVE LOSSES OFF PANEL

Design Limitations: Small Systems

EFFICIENCY DIFFERENCES NECESSITATE SEGREGATION OF MANUFACTURER'S EQUIPMENT INTO DIFFERENT SOURCE CIRCUITS

IF DIFFERENT MANUFACTUERS ARE FED INTO THE SAME INVERTER MISMATCH WILL RESULT DUE TO:

VOLTAGE MISMATCH (ALL CIRCUITS WORK OFF PEAK POWER)
TEMPERATURE VARIATION
INSOLATION AND SPECTRAL VARIATION

LOWER POWER OUTPUT CAUSES INCREASED BOS COST

DIFFERENT SPECTRAL RESPONSE MAY AFFECT SYSTEM VALUE TO OWNER

- DIFFERENT ANNUAL ENERGY EFFICIENCY
- DIFFERENT CAPACITY ON PEAK

Design Limitations: Large Systems

ONE PCU PER MANUFACTURER

NO NEED FOR VOLTAGE STANDARD

MISMATCH LOSSES REDUCED

MUST STILL EVALUATE BASED ON:

- PANEL POWER
- SPECTRAL RESPONSE
- RELIABILITY

HOT-SPOT HEATING IN CENTRAL-STATION ARRAYS

C.C. Gonzalez
Jet Propulsion Laboratory
Pasadena, CA 91109

Hot-spot heating has been examined extensively in the past, and the Jet Propulsion Laboratory has developed a laboratory test to determine module hot-spot susceptibility. A test cell is driven into a back-bias voltage equivalent to the maximum-power voltage of the total number of series cells per bypass diode. The test current is equivalent to the maximum-power current of a single cell. The effective shadow level, and consequently the test current, are controlled by the cell illumination level. However, the test in its current configuration is based on the assumption that no current imbalance will result from parallel cell strings. A central-station application, such as the Sacramento Municipal Utility District (SMUD) Project, contains large numbers of modules connected in parallel; in addition, the modules contain parallel strings.

Hot-spot tests performed on the SMUD verification array have shown that current imbalance occurs, resulting in significant hot-spot heating. One cause of current imbalance is differences in the average shunt resistances of parallel cell strings due to cell shunt-resistance variations. Because the impact of statistical averaging is reduced, differences in string shunt resistances increase as the number of cells per substring is reduced (the frequency of cross ties is increased). Bypass diodes at a frequency of two modules per diode are currently being used on the SMUD array because of potential hot-spot problems.

In-depth hot-spot tests were performed on the SMUD verification array with bypass diodes. The tests had several objectives: a comparison of hot-spot temperatures achieved under field conditions with those obtained with the present laboratory hot-spot test using similar modules, an assessment of current imbalance versus cross-tie frequency, and an assessment of different shadow patterns and shadow densities. Instrumented modules were used to vary the number of cross ties and to measure the test-cell current and back-bias voltage. The widths, lengths, and densities of the shadows were varied to maximize the back-bias voltage at maximum power current. An infrared camera was used to indicate the existence of hot spots and estimate temperature increases in conjunction with thermocouples.

The results of these hot-spot tests indicate a sensitivity of back-bias heating to the shadow size (amount of cell coverage) and density. Partial cell coverage and diffuse shadows produce the greatest heating for high-shunt-resistance cells such as those in the SMUD modules; however, low-shunt-resistance cells (<5 ohms) achieve the greatest heating with full coverage. The test shadow producing the greatest hot-spot heating was a long thin diffuse shadow stretching across the panel but covering only a portion of each cell. Total cell coverage by hard shadows produced negligible heating anywhere in the panel containing shadowed cells.

The tests demonstrated that current imbalance and intensified hot-spot heating occur in some cases when the number of cells per substring is decreased to three or fewer (the standard SMUD modules have three cells per substring). The results also indicate that, when current imbalances exist, worst-case field hot-spot temperatures are as much as 50°C higher than those obtained in the laboratory hot-spot test (200°C versus 150°C). Under less severe circumstances there was as much as a 25°C difference in some cases.

The results of the hot-spot tests lead to the following conclusions: (1) The shadow condition with the highest probability of occurrence that can also lead to potentially severe hot-spot heating is a broad shadow covering several cells in a number of strings but having a protuberance that partially covers some parallel cells. This conclusion follows from the types of shadows that produced severe heating in the tests, combined with the fact that a broad shadow with a protuberance has a higher occurrence probability than a long thin shadow like the one in the test. (2) The use of frequent cross ties aggravates shunt resistance mismatch in parallel cell strings, leading to current imbalance and severe hot-spot heating during back-biasing. (3) The existing laboratory hot-spot test greatly underpredicts hot-spot temperatures in multiparallel cell strings due to current imbalance with frequent cross ties, and (to a much lesser degree) due to hot cells adjacent to the test cell. The laboratory test assumes single strings and does not account for parallel shadowed cells. (4) Finally, there is a need to modify the Block V hot-spot test to account for current imbalance with multiparallel cell strings.

HOT-SPOT HEATING IN CENTRAL-STATION ARRAYS

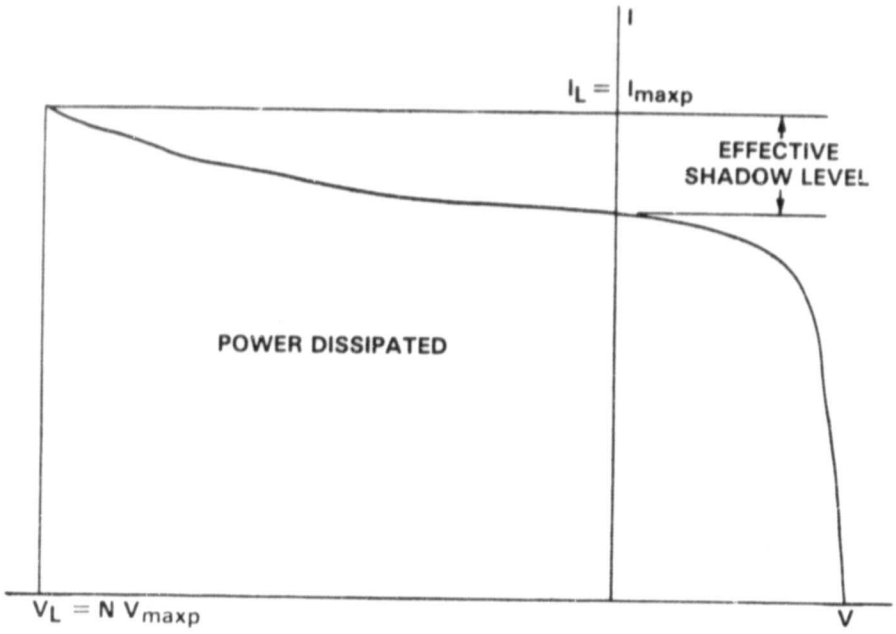
JET PROPULSION LABORATORY

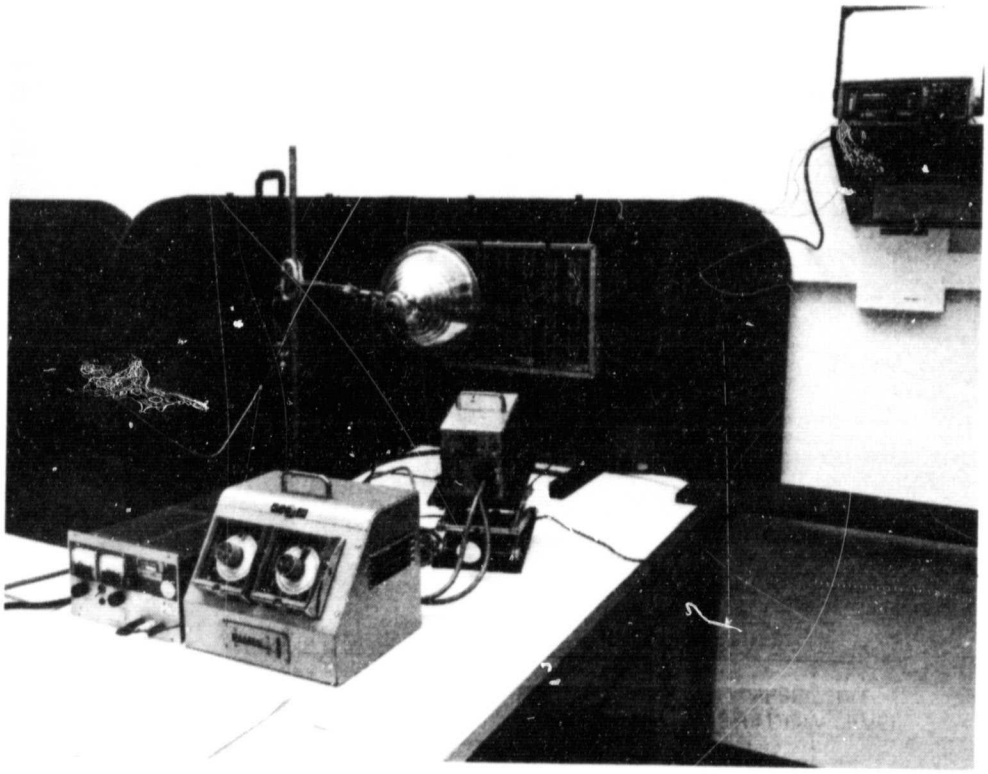
C.C. Gonzalez

Hot-Spot Test

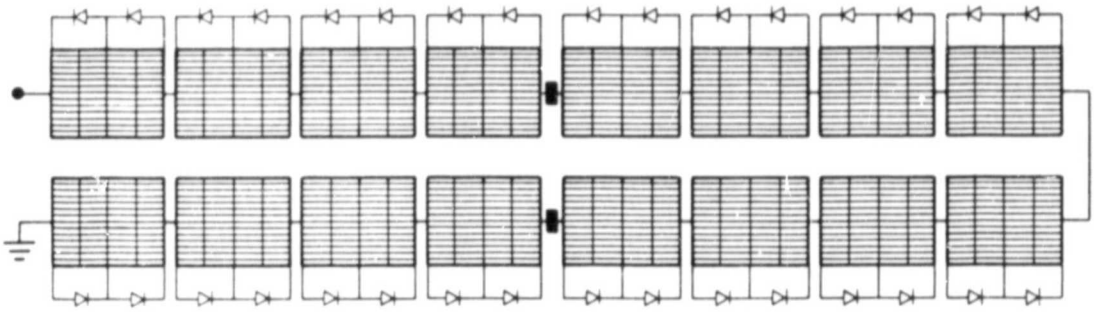
- **Laboratory test developed to determine hot-spot susceptibility of modules**
  - **Key features:**
    - **Test parameters**
      - **Applied test current equivalent to cell max-power current; however, I_{SC} is used for low-shunt-resistant cells**
      - **Simulates shadow level leading to maximum back-bias voltage at max-power current**
      - **Applied back-bias voltage determined by bypass diode frequency**
    - **Test conditions**
      - **Thermal boundary conditions for 100 mW/cm^2, 40°C ambient**
      - **100 hours test duration**
  - **Key assumption**
    - **No current imbalance resulting from multiparallel cell strings**

Hot-Spot Test: Test Parameters

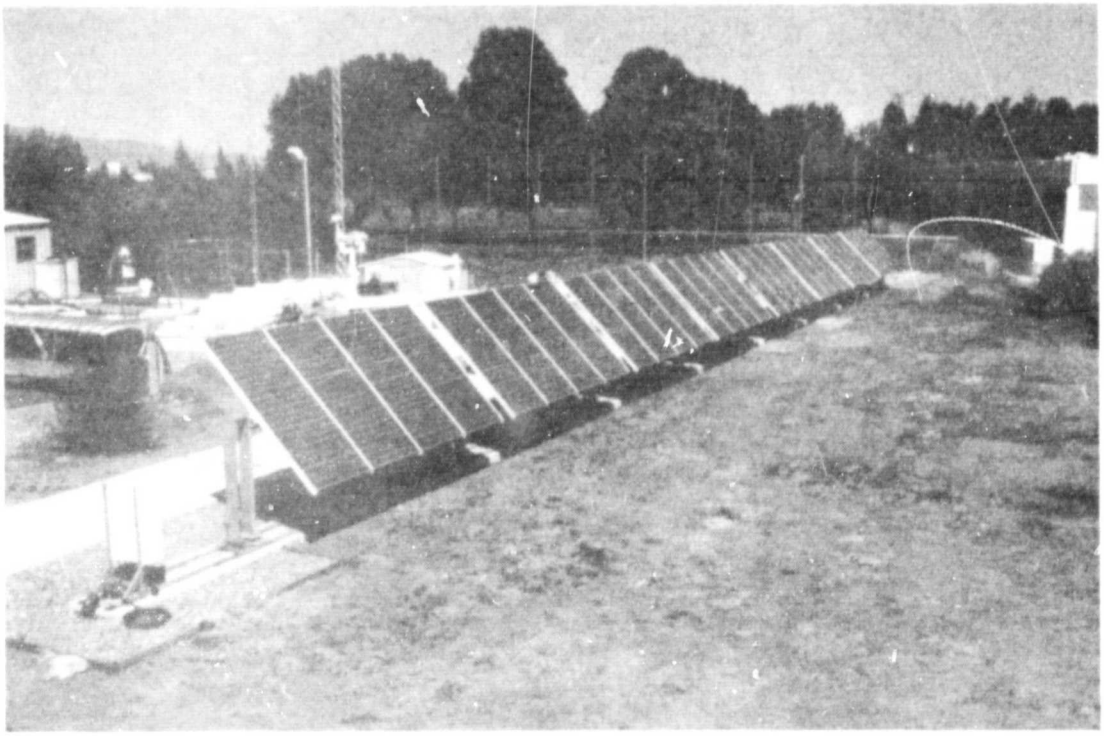




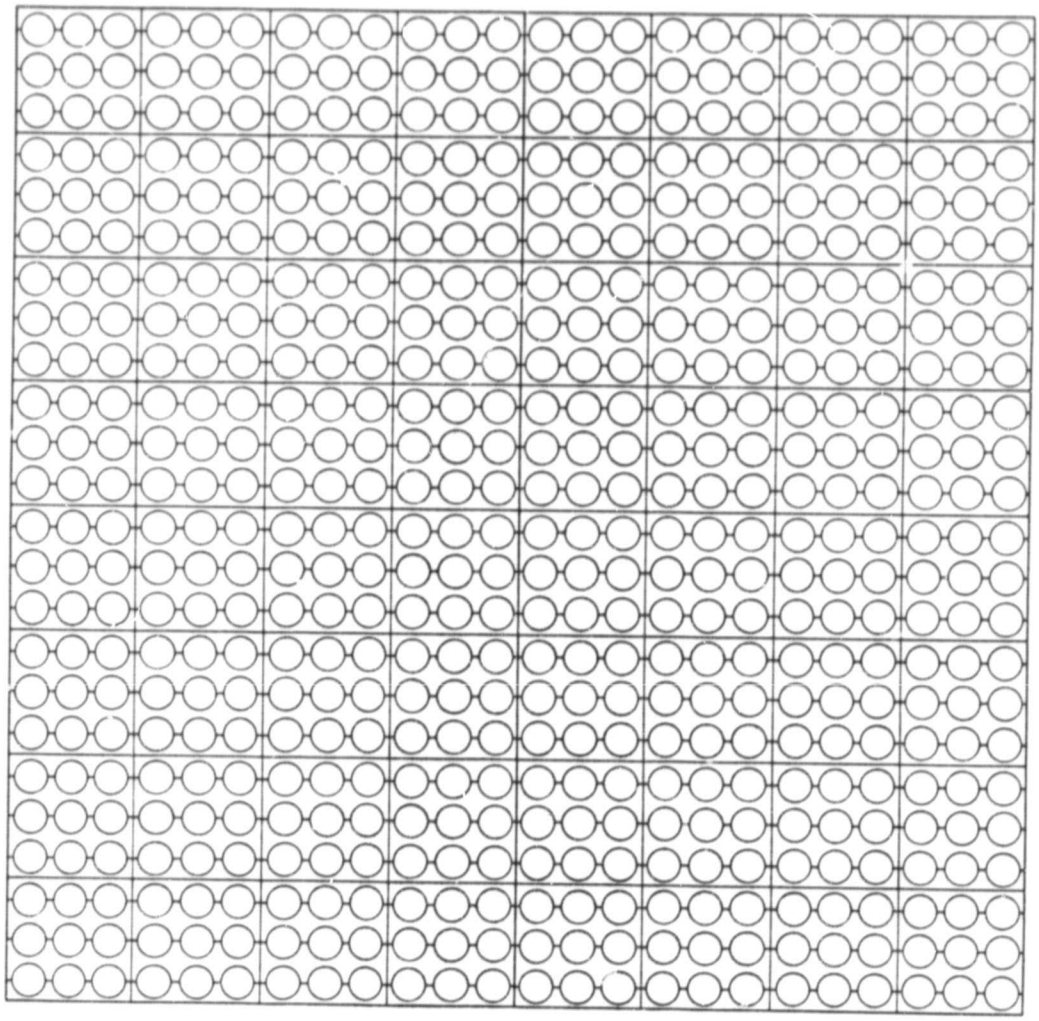
SMUD Source-Circuit Electrical Configuration

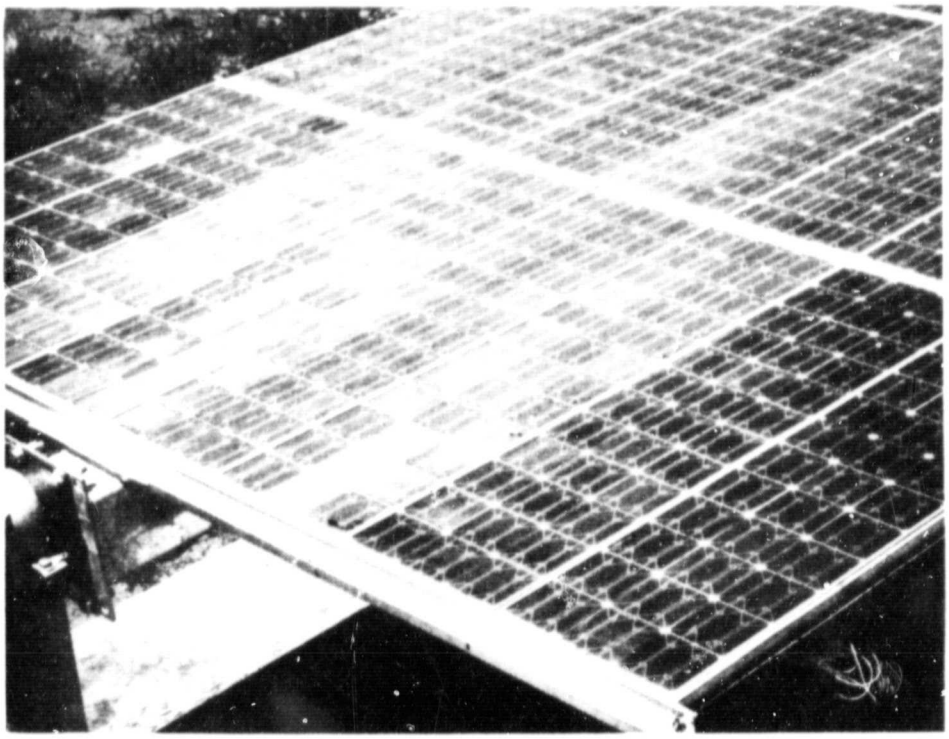


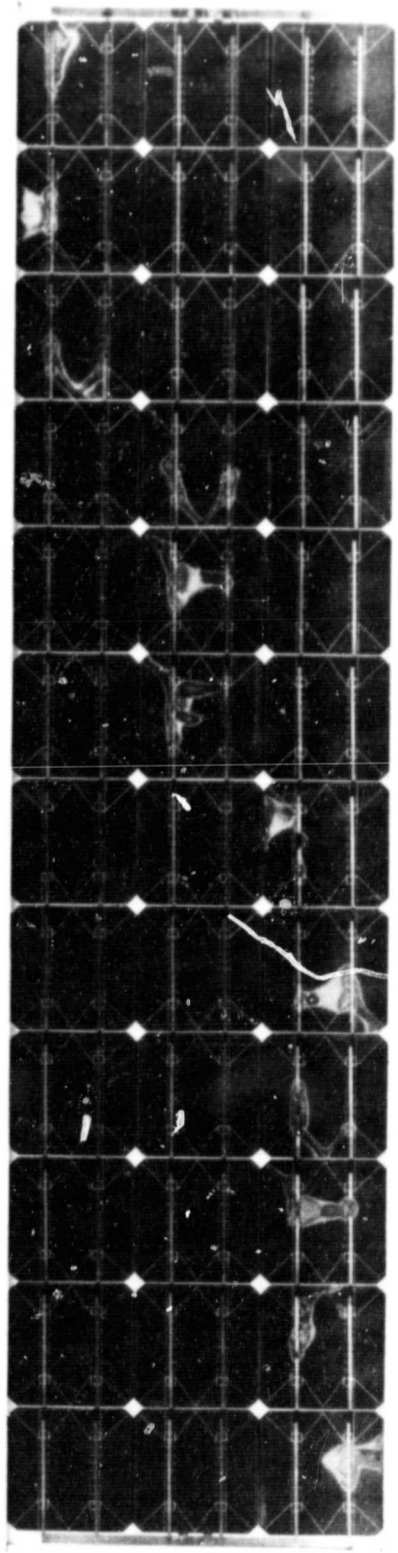
Source Circuit: 2 arrays
16 panels
64 series blocks (modules)
24 cells in parallel
12 cells per substring
Approx. 21 kW at STC
Approx. 56 A

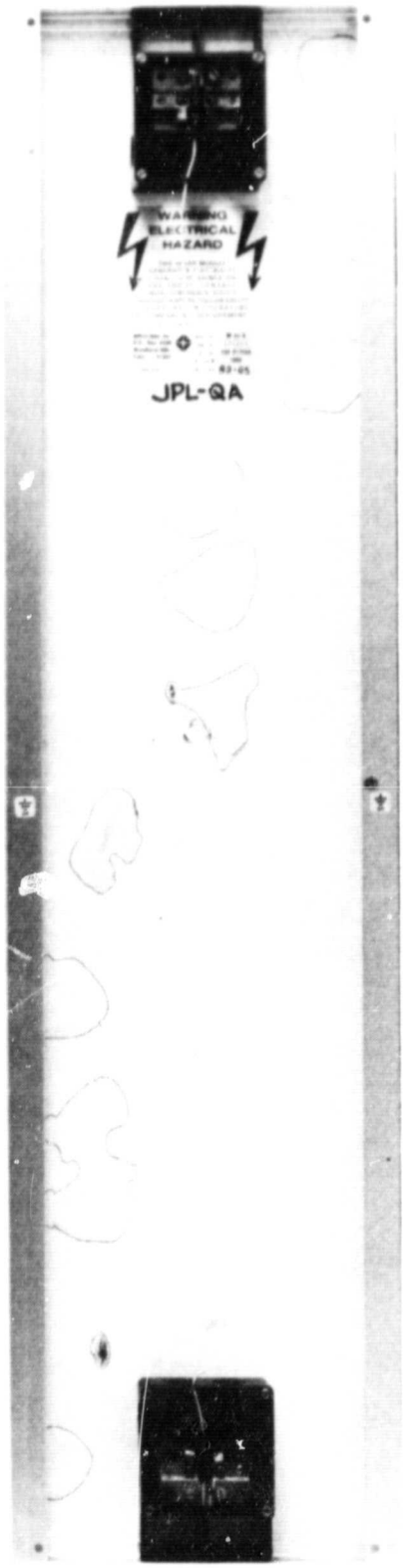


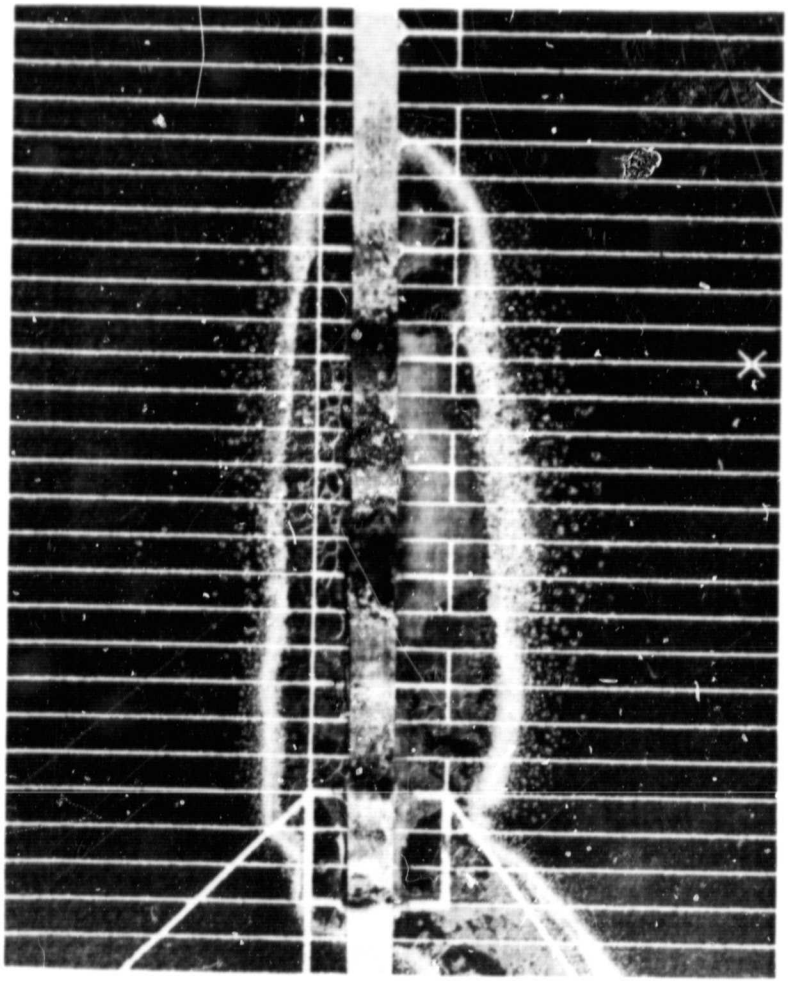
SMUD Module and Panel Configuration







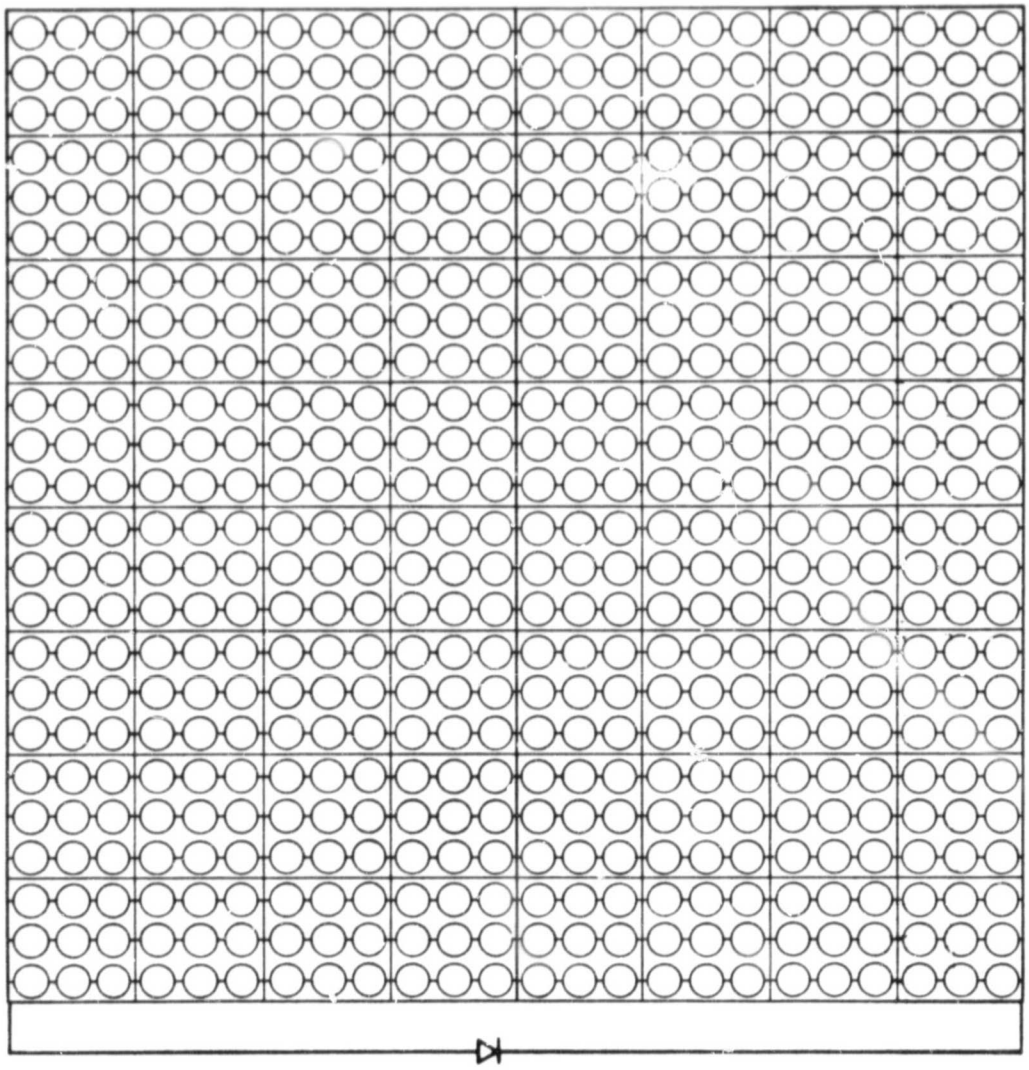




Findings From Preliminary SMUD Verification Array Tests (Without Bypass Diodes)

- Extreme current imbalance and hot-spot heating with shorted source circuit and shadowed panel
  - Heating localized in cell path with lowest shunt resistance
  - Failure level temperatures ($>200°C$) in approximately 7 seconds
- Conclusion: Bypass diodes required to protect against transient (short-term) shorting

SMUD Module and Panel Configuration With Bypass Diode

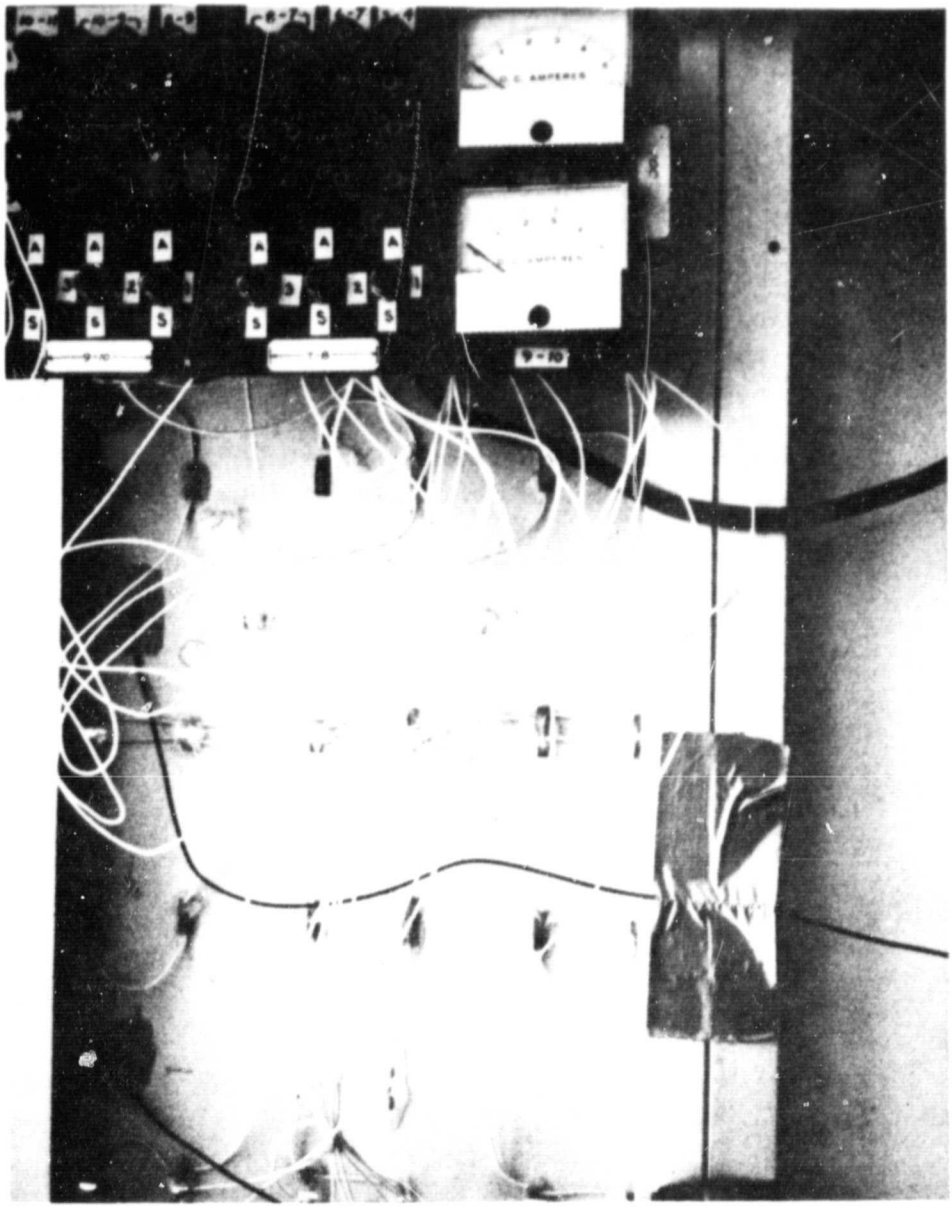


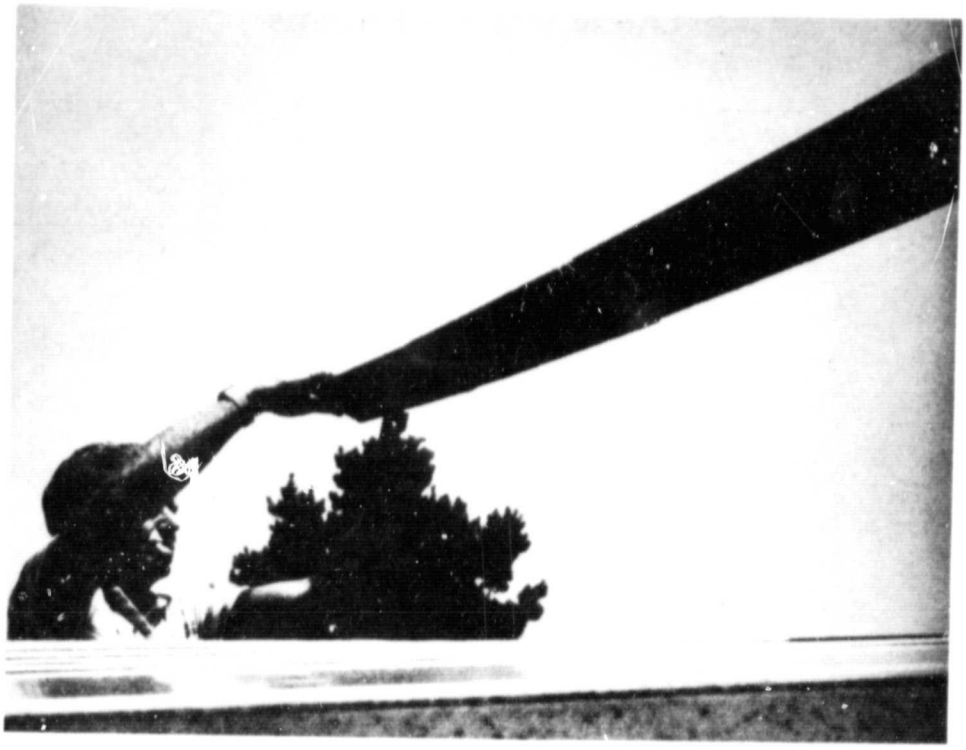
Test Objectives (With Bypass Diodes)

- **Compare hot-spot temperatures achieved under field conditions with those obtained from present laboratory hot-spot tests**
- **Assess extent of current imbalance versus cross-tie frequency**
- **Assess effects of different shadow patterns and shadow densities**

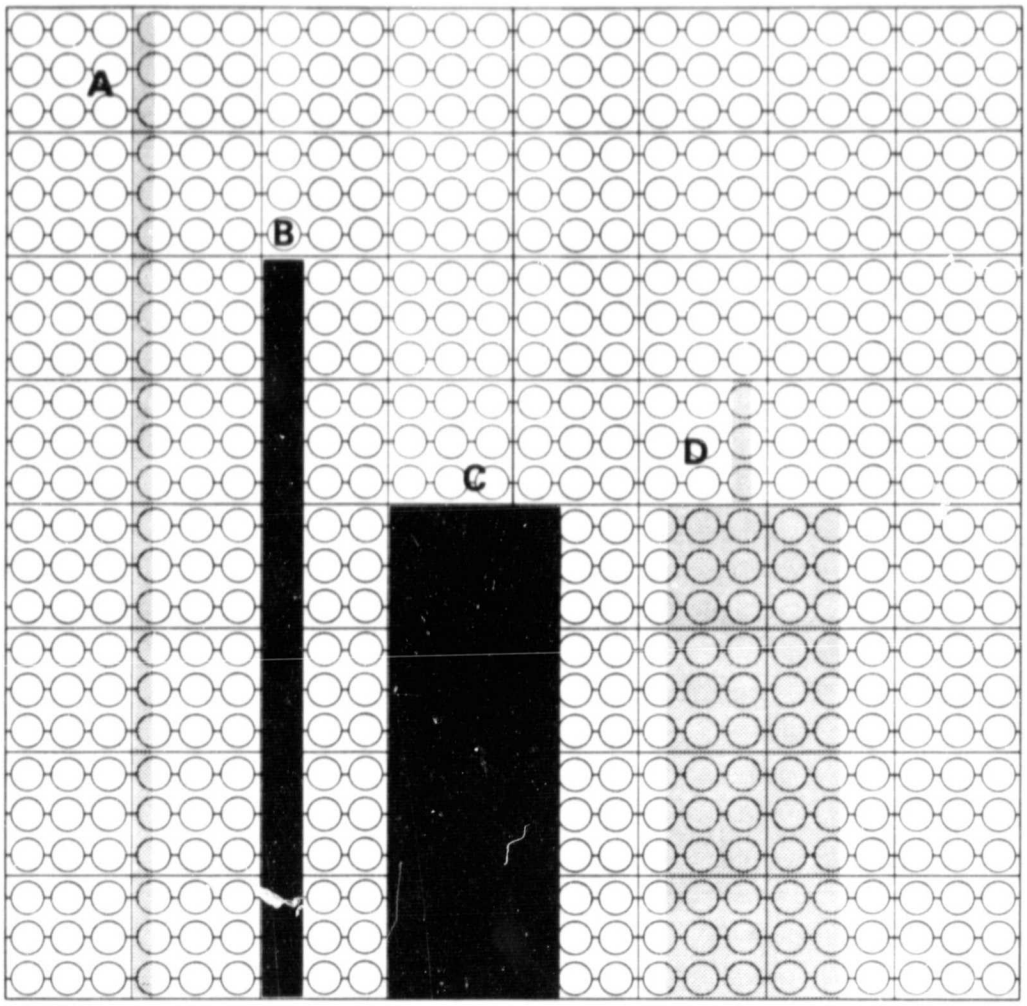
Test Procedure

- Hot-spot tests performed with bypass diodes around every two modules
  - Use of instrumented modules to:
    - Vary number of cross ties
    - Measure cell current and back-bias voltage
  - Varied width, length, and density of shadow to maximize back-bias voltage at max-power current (actual point of maximum power dissipation occurs at diode turn-on)
  - Use of IR camera to indicate existance of hot spots and estimate temperature increases in conjunction with thermocouples





Array Shadow Patterns



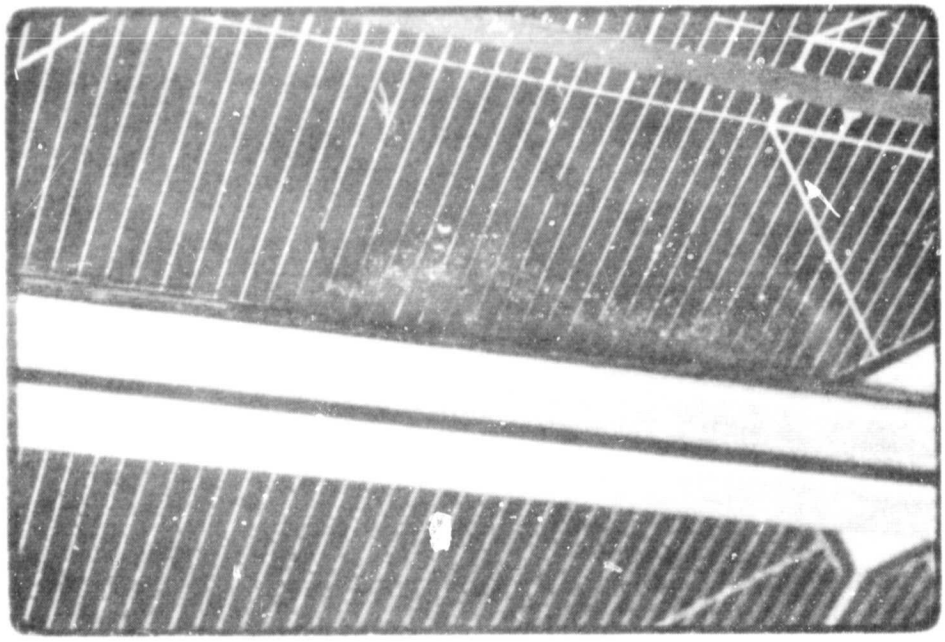
A Partial cell coverage by diffuse shadow

B,C Full coverage of one cell or more by hard shadow

D Full coverage combined with partial cell coverage with a diffuse shadow

Test Observations

- Sensitivity to shadow size (amount of cell coverage) and density
  - Partial cell coverage and diffuse shadows such as A and D produce greatest heating for high-shunt-resistance cells; changes to full cell coverage for low shunt resistance ($\approx 5\ \Omega$)
  - Hot spots occur in shadowed area
  - Total cell coverage by hard shadows such as B and C produce negligible heating
- Occurrence of current imbalance and severe hot-spot heating noted with three or fewer cells per substring
- Hot-spot temperatures in field were in general greater than in laboratory
  - Differences about 10-50°C
  - Upper limit values: 200°C versus 150°C



Conclusions

- Use of frequent cross ties aggravates shunt resistance mismatch in parallel cell strings, leading to current imbalance and severe hot-spot heating during back-biasing

- Existing single-string laboratory hot-spot test underpredicts hot-spot temperatures in multiparallel cell strings due to:

    - Current imbalance with frequent cross ties

    - Adjacent hot cells resulting from shadows covering numerous parallel cell strings

- Need to modify BLock V hot-spot test to account for current imbalance with multiparallel cell strings

HOT-SPOT INVESTIGATIONS OF UTILITY SCALE PANEL CONFIGURATIONS

J.C. ARNETT, R.B. DALLY, J.P. RUMBURG
ARCO SOLAR INDUSTRIES
WOODLAND HILLS, CALIFORNIA

INTRODUCTION

The study described herein is part of an ongoing program at ARCO Solar to understand the causes of array faults and mitigate their effects. These studies are currently concentrating on the panel proposed by ARCO for the 900 kw second phase of the SMUD project. The panel is designed for hot spot tolerance without compromising efficiency under normal operating conditions. Series/paralleling internal to each module improves tolerance in the power quadrant to cell short or open circuits.

Analytical methods have been developed for predicting "worst case" shade patterns and calculating the resultant cell temperature. Experiments conducted on a prototype panel at the Chatsworth test facility support the analytical calculations.

DESCRIPTION OF THE PROPOSED PANEL AND MODULE

The M52-L module ARCO Solar has proposed for the 900 kw second phase of the SMUD project, contains 36 square, CZ silicon cells in a 12 series by three parallel arrangement. The cells are "type A" characterized by high shunt resistance in the range of 10 to 100 ohms.

An array of nine parallel by four series modules make up each panel. The maximum reverse voltage across a damaged or shaded cell is limited to about seven volts by four bypass diodes which protect each panel.

DETERMINING WORST CASE SHADING

Type A cells become hottest when a parallel row of cells are partially shaded. This shade pattern causes current redistribution to the cells with the lowest shunt resistance. The maximum reverse voltage across an individual cell, however, is still limited by the voltage across the other (n-1) cells in the series block.

A shaded or broken cell becomes hottest when it loads the remaining (n-1) cells in the series string at their maximum power point. For type A cells, the critical level of shading which yields this condition is a function only of the shunt resistance (R_{sh}) and the number of series cells per diode (n). An attached figure illustrates this phenomena and defines the equation to determine the critical shade level. For the M52 module, the shade level varies from 9% for a cell with 100 ohms of shunt resistance, to 30% for a cell with 10 ohms of shunt resistance. This agrees with results obtained during the short term hot spot test performed on a verification panel at ARCO Solar, where it was found

that an opaque shadow a quarter cell wide (25% shading) produced the highest cell temperatures. By contrast, a series shadow does not yield as high temperatures because the back bias power dissipation is shared among a number of cells.

DETERMINING THE TEMPERATURE OF A BACK-BIASED CELL

Temperature of a reverse biased cell is determined from a plot similar to that used to define NOCT. Cell minus ambient temperature is plotted against power dissipation density. At high power levels, the curve begins to flatten out, as expected, due to the intrinsic nature of radiative heat transfer. Note that a simple extrapolation of the NOCT line will yield erroneous results at high power levels.

During the short term hot spot test at ARCO, insolation was 100.4 mw/cm^2, and ambient temperature was 20.2°C. Power dissipation density due to inpinging solar radiation and reverse bias power consumption caused by the 25% cell shadow was 220 mw/cm^2. An attached figure shows a predicted temperature rise of 72°C above ambient, or a cell temperature of 92.2°C. The actual measured cell temperature was 91°C. The verification panel passed this test without sustaining electrical or mechanical degradation.

While this plot predicts the temperature rise for a uniformly heated cell, an IR camera revealed that temperature is not uniform over the surface of the cell. In no case however, was the temperature of a localized hot spot more than 7°C above the average.

MODULE INTERNAL SERIES/PARALLELING

Worst case cell heating can only occur when a series block is at short circuit. It is important to realize that a short circuit condition occurs infrequently, and a module should be tolerant to array faults while in the normal operating mode. Series/paralleling internal to the module increases fault tolerance in the power producing quadrant. Attached figures show the effects of cell shadowing, and cell open circuits on the power produced by a module at standard test conditions (T_{cell}=25°C, INS=1000 W/m^2, and V_{mod}=5.78 volts). For faulted modules, a substantial increase in module power is realized by providing alternate current paths, i.e. series/paralleling.

CONCLUSIONS

Panel and module design for utility scale systems should consider the effect of array fault energy loss in the forward quadrant under normal operating conditions as well as the hot spot heating of cells that operate in the reverse quadrant.

Although some 21,000 modules will be included in SMUD PV2, the effects of cell shading can be ascertained by consideration of a series block of nine parallel modules. Worst case cell heating can occur only when the series block is at short circuit, and in no case will the reverse voltage across a single cell be greater than the voltage produced by the other cells in the string.

During the short term hot spot test at ARCO, cell temperatures reached a maximum of 91°C, and the verification panel sustained no electrical or mechanical degradation. Long term hot spot testing is currently underway with no ill effects.

Future plans include a random and periodic sampling of cells to map the statistical distribution of shunt resistance, determination of temperature and irradiance level effects on shunt resistance, and the addition to PVSYS, the ARCO Solar simulation routine, of a program for determining energy loss due to cell shadowing for various shadow configurations, densities, and frequency of occurrence.

HOT-SPOT INVESTIGATIONS OF UTILITY-SCALE PANEL CONFIGURATIONS

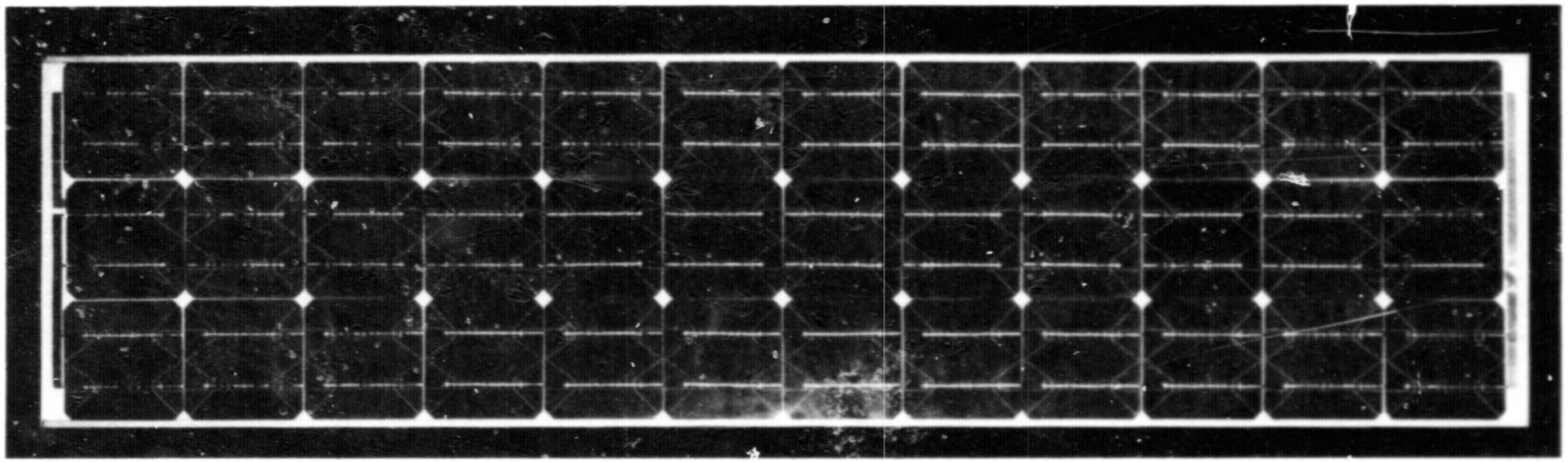
ARCO SOLAR INDUSTRIES

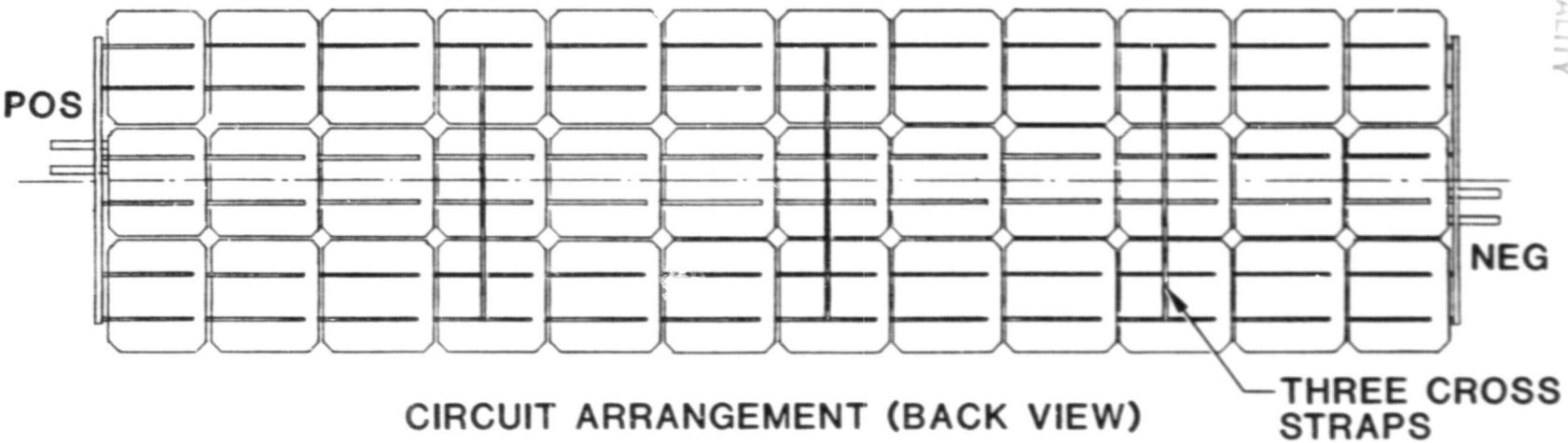
J. C. Arnett
R.B. Dally
J. P. Rumburg

Hot-Spot Investigation Approach

- CELL CHARACTERIZATION
- SHADOW
- ANALYTICAL PREDICTIONS
- FIELD TESTING
- DESIGN CRITERIA

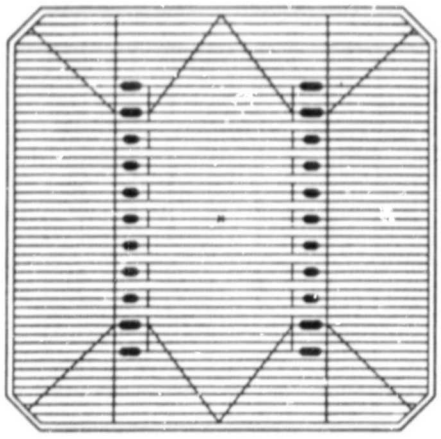
ARCO Solar M52-L Module





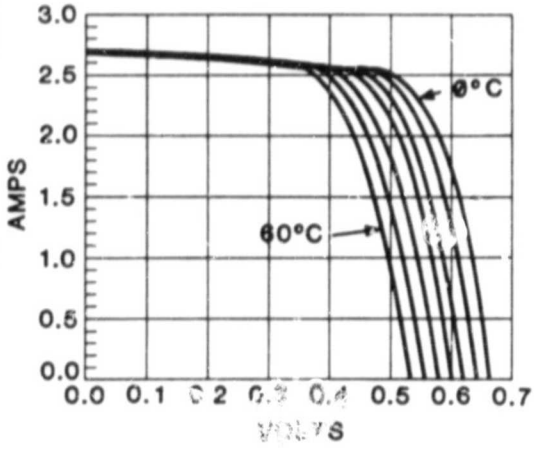
CIRCUIT ARRANGEMENT (BACK VIEW)

ARCO Solar PV Cell



CELL AREA = 93.3 CM^2

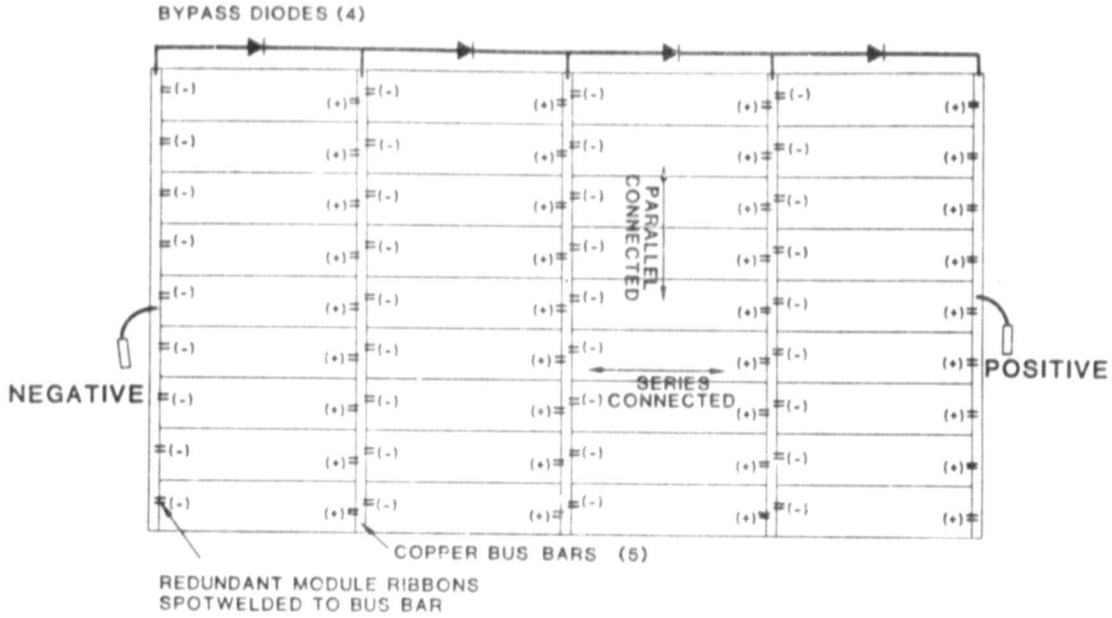
SHUNT RESISTANCE,
R_{SH} = 10–100 Ω



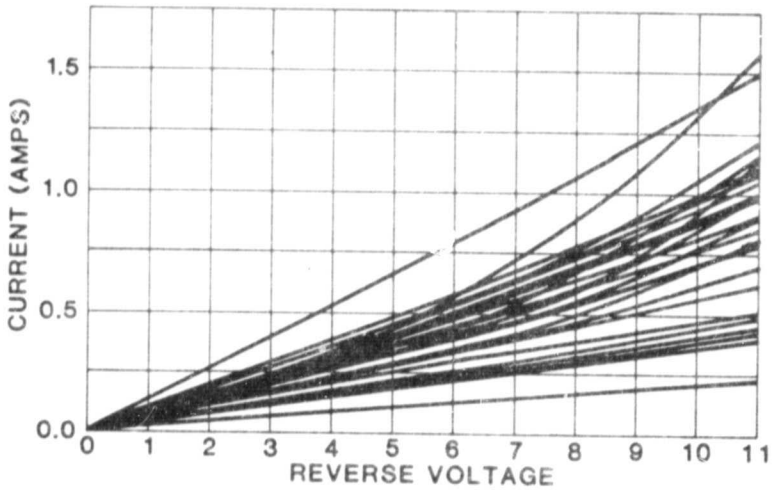
SQUARE CELL
CHARACTERISTICS AT STC

I_{SC} = 2.70 AMPS
V_{OC} = 0.60 VOLTS
I_{MP} = 2.48 AMPS
P_{MAX} = 1.19 WATTS @ 0.48 VOLTS

SMUD PV2 Panel Electrical Configuration



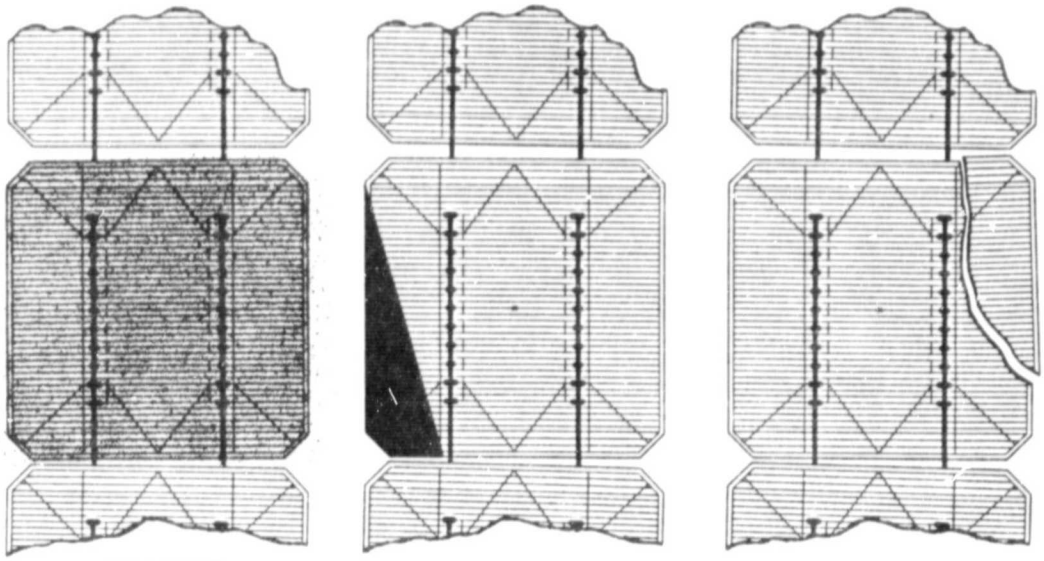
Reverse I-V for ARCO Cells



"TYPE A" CELLS

R_{SHUNT} = 10–100 Ω

Conditions That Result in Cell Back Bias

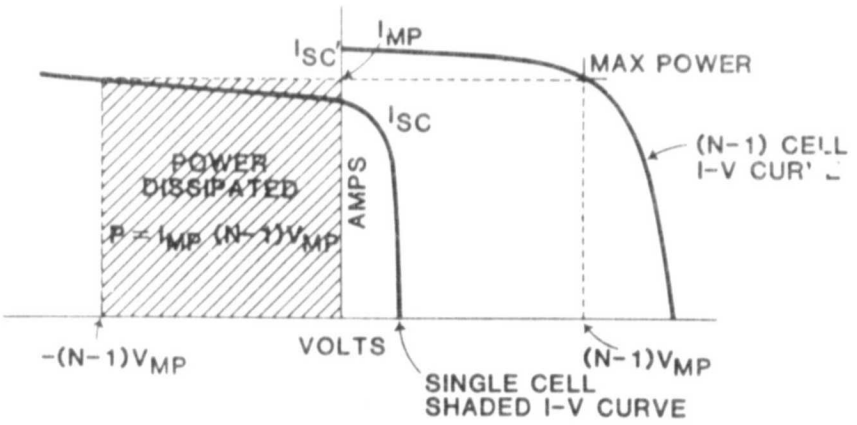


LOSS OF LIGHT FROM UNIFORM SOFT SHADOW OVER ENTIRE SURFACE

OPAQUE "HARD" SHADOW

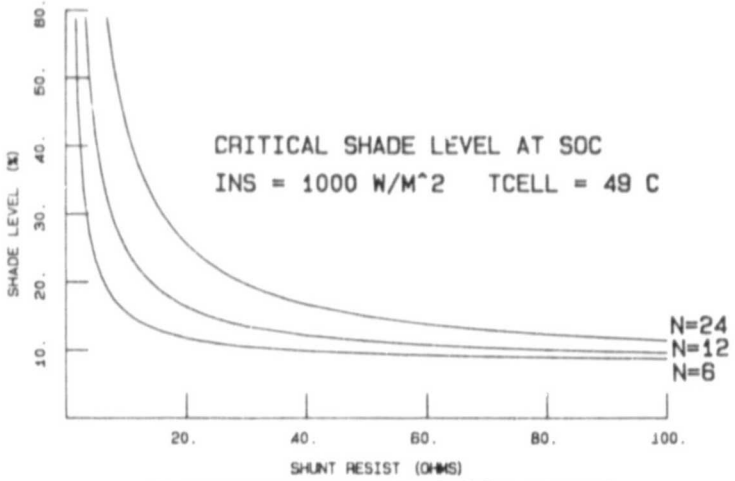
LOSS OF ACTIVE AREA DUE TO CELL CRACK

Worst-Case Cell Heating in a String of N Cells



- SHADED CELL LOADS THE OTHER CELLS AT THEIR MAX POWER POINT
- CRITICAL SHADE LEVEL EQUAL TO $1 - \frac{I_{SC}'}{I_{SC}}$
- CRITICAL SHADE LEVEL IS A FUNCTION OF R_{SH} AND N
- FUNCTION WHICH DEFINES CRITICAL SHADE LEVEL: $1 - \left[\frac{I_{MP} - \frac{(N-1)V_{MP}}{R_{SH}}}{I_{SC}}\right]$

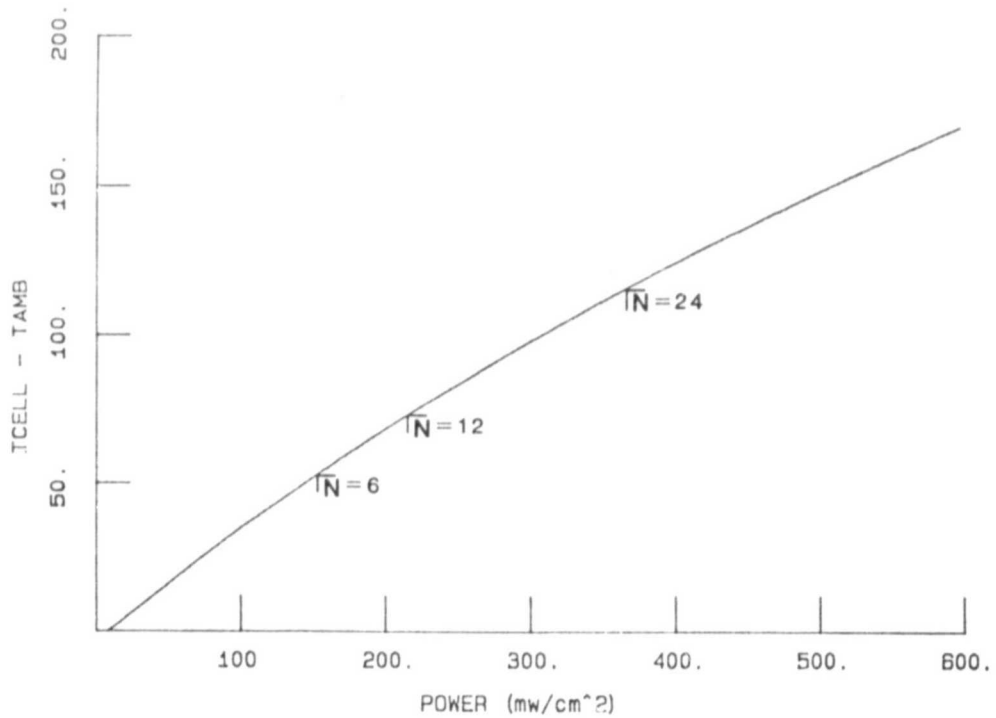
Critical Shade Level Operating Conditions



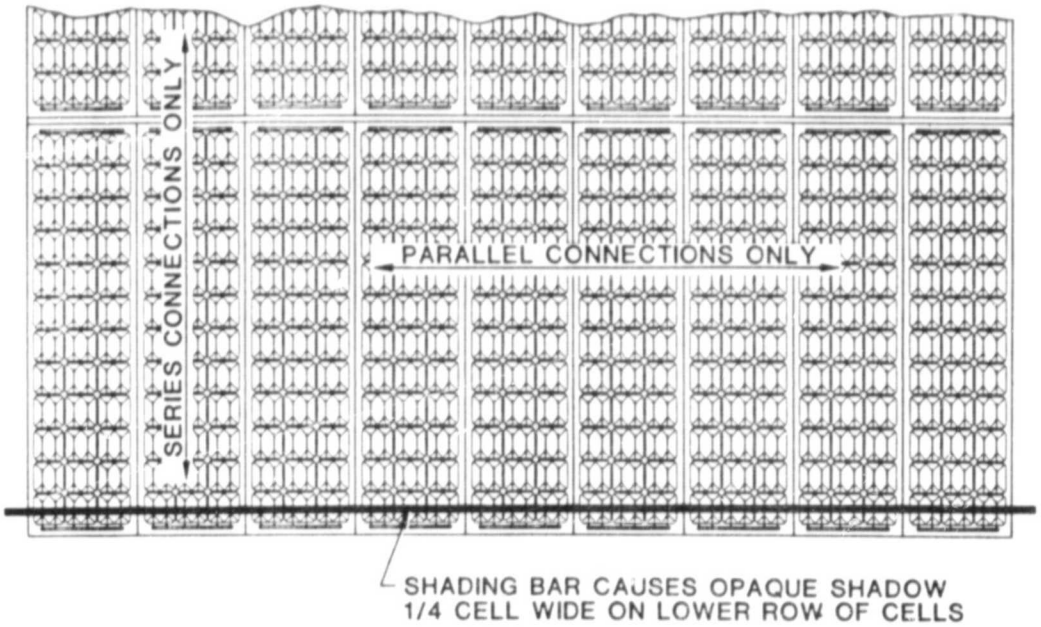
STANDARD OPERATING CONDITIONS

I_{NS}	= 1000W/M^2	I_{MP}	= 2.53 AMPS
T_{CELL}	= 49° C	P_{MAX}	= 1.06 WATTS @ 0.42 VOLTS
		I_{SC}	= 2.75 AMPS

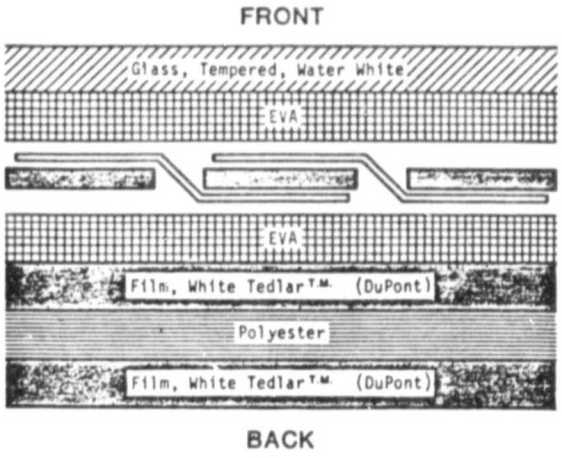
Cell Temperature vs Power Dissipation (M52-L)



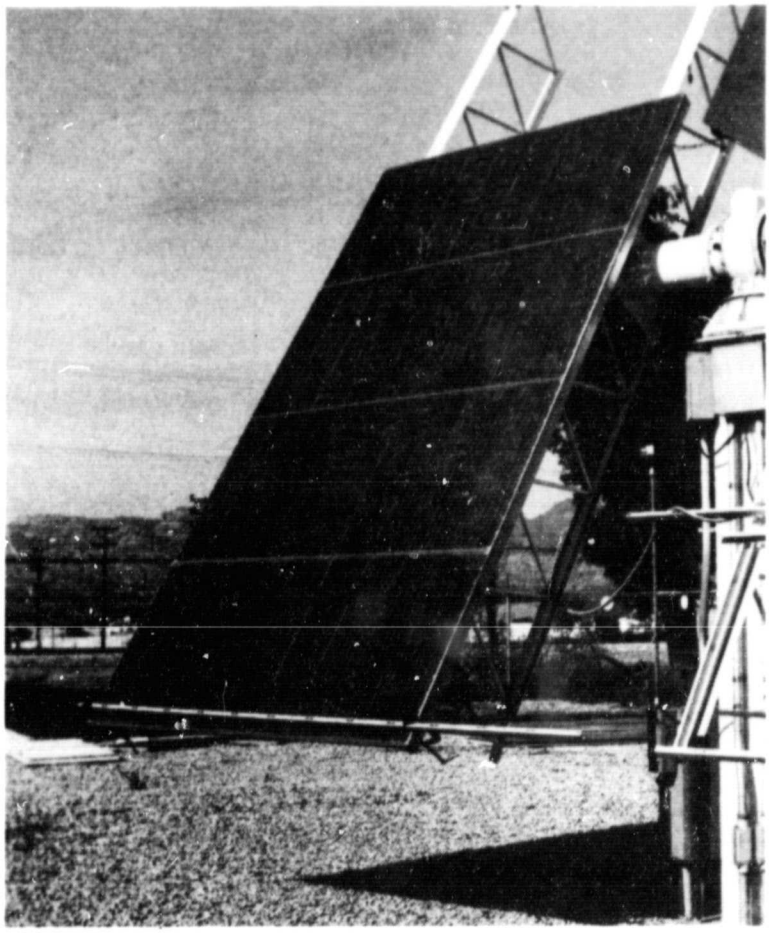
Worst-Case Shading



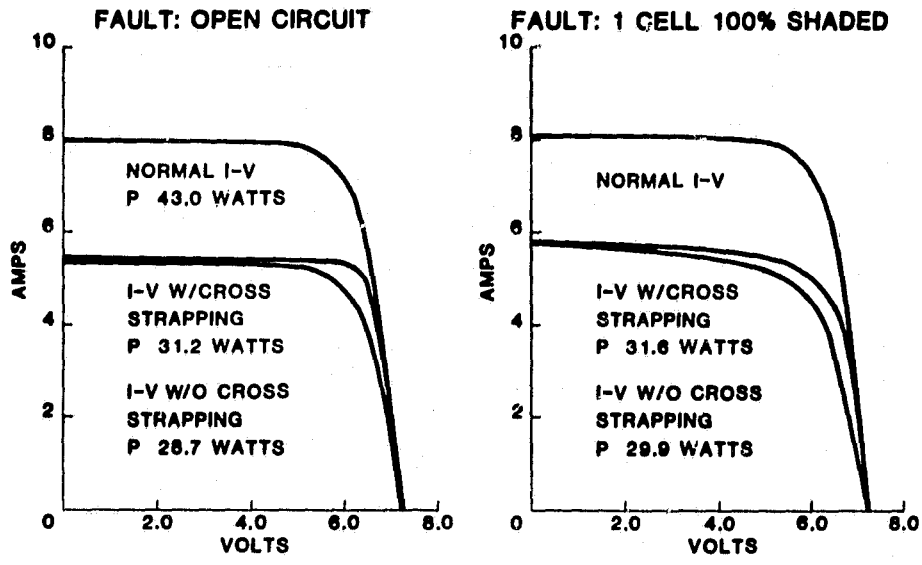
M52 Module Laminate Cross Section



SMUD PV2 Prototype Panel During Hot-Spot Testing:
Shading Bar Covers 25% of Bottom Row of Cells



Effect of Cell Faults in the Power Quadrant



Future Work

- STATISTICAL BASE OF CELL CHARACTERISTICS
- SHADOW GEOMETRY AND DENSITY
- FREQUENCY OF SHADOW OCCURENCE
- REASSESSMENT OF DESIGN CRITERIA

DESIGN AND SELECTION OF BYPASS DIODES

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Why Use Bypass Diodes?

Bypass diodes are often required to limit to potential for reverse voltage "hot-spot" heating in high voltage arrays or in arrays that undergo periodic operation near the short-circuit point. In addition, when properly applied, bypass diodes can minimize the effect of shadowing and various internal module failures on the array energy output.

As highlighted in Figure 2, the decision to package a bypass diode as an integral part of a photovoltaic module, whether externally or internally-mounted, should be made by the module designer based on requirements related exclusively to the ability of the module to survive anticipated use conditions, including "hot-spot" heating exposure. With this objective in mind and with the additional requirement to design a module with the electrical and geometric properties appropriate to a specific application, the module designer is free to use bypass diodes in any of the arrangements depicted in Figure 2. If the circuit layout is such as to provide adequate "hot-spot" heating immunity without the use of bypass diodes, this option becomes a valid design approach. The incorporation of a single bypass diode across the module terminals is not regarded as a reasonable action by the module designer since its use does not enhance the ability of that module to survive the "hot-spot" heating exposure and complicates the array circuit design by introducing problems of current sharing among individual module diodes if the array designer wishes to employ a parallel-connected group of modules as a circuit element. Depending on the module circuit configuration, it may be necessary to employ multiple bypass diodes as part of the module design to ensure satisfactory "hot-spot" performance. In such cases, where the requirement for multiple bypass diodes would require the repeated penetration of the module encapsulant for connections to externally-mounted diodes, it would seem logical to mount the diodes as an integral part of the encapsulation system.

The array designer should use bypass diodes to maximize the array energy output over the operational lifetime of the system in the face of shadowing and various internal module failures. In addition, the array designer may use bypass diodes to enhance the safety of the system by eliminating the potential for arcing when a module is removed from an illuminated circuit. Figure 3 illustrates the options available to an array designer in a circuit arrangement consisting of a parallel-connection of series strings. An implementation that uses no bypass diodes in the array circuit is not considered to be an appropriate solution when the objectives of the array design can be better achieved by one of the other arrangements shown. If the selected module design contains multiple internal diodes, the array designer may simply elect to series-connect these modules with no additional diodes.

For an arrangement of series-connected parallel groups, as illustrated in Figure 4, one bypass diode can be employed for each parallel-connected group. If the individual modules contain multiple internal bypass diodes, it will be necessary to install one large diode to ensure that the bypass current passes through the external circuit.

Internally-Encapsulated Bypass Diodes

Unpackaged diode cells of the type shown in Figure 5 can be soldered to appropriately-sized heat spreader plates and encapsulated within the module laminate as illustrated in Figure 6. The dissipation of the heat generated within the small diode chip when conducting the bypass current represents the most difficult design problem involved with the integration of these chips within the module encapsulant. It is also essential that the thickness of the package to be laminated along with the solar cell circuit be kept as small as possible to assure conformance of the rear cover sheet with the minimum use of encapsulant material. These requirements combine to dictate that the diode chip be mounted to a thin heat spreader plate which is fabricated from a material of high thermal conductivity. In this way, it is possible to maintain an acceptably low junction temperature by transferring the heat from this small source through the fin created by the plate and on out into the adjacent solar cell circuit elements where it can be ultimately rejected to the surroundings by radiation and convection. The size of the heat spreader plate required to produce the specified temperature level within the laminate will depend on the diode heat generation as well as on the insolation level, ambient temperature, wind speed and details of the module mounting arrangement. The most logical mounting location for this plate is directly behind the solar cell circuit where the required fin area can be encapsulated without increasing the exposed module area. This mounting arrangement will generally require that the heat spreader plate be electrically insulated from the rear sides of the solar cell circuit, since the plate size and/or mounting location may require the plate to stradle cells of different potentials within the circuit. Similarly, it will be necessary to insulate the anode lead from the rear side of the solar cell circuit. A silicone foam tape thermal barrier layer is applied around the diode cell to prevent the ethylene vinyl acetate encapsulant from contacting the diode body which will be somewhat hotter than the adjacent heat spreader plate. This foam tape barrier, which is configured in two layers to completely surround the diode cell, also functions to ease the conformance of the rear cover sheet during module lamination in that no abrupt changes in thickness are encountered as the rear cover sheet is forced down by the laminator diaphragm.

The size and thickness of the cathode heat spreader plate is dependent on the diode heat dissipation requirement as shown in Figure 7. Experiments performed on encapsulated module segments containing diodes mounted to copper heat spreader plates of various sizes have produced the results given on the left hand graph of this figure. These tests were performed under room ambient conditions with the modules mounted face-up on a horizontal surface of two inch thick styrofoam insulation to virtually eliminate heat rejection from the rear side. The externally supplied bypass current was varied to produce a range of diode heat dissipations. These experimental data, relating the temperature difference between the heat spreader near the diode body and the surrounding solar cells to both the heat spreader size and diode dissipation,

can be used to define a recommended heat spreader size for a required level of bypass diode heat dissipation. This recommended relationship is given on the right hand graph of Figure 7 for environmental conditions which include an ambient temperature of 40°C with an insolation of 1.0 kW/m^2 and no heat rejection from the module rear surface. Thus, the heat spreader plate dictated by this relationship can be regarded as being conservatively-sized for almost any U.S. location. The reader is cautioned against extrapolating this relationship much beyond the 15 watt dissipation level since it is apparent that the slope of the curve at this point is increasing at a rapid rate. In fact, it is obvious that at some point, which is not much greater than 15 watts, it will become impractical to consider this approach as a valid method for dissipating the localized diode heat, since the ultimate heat transfer at an acceptably-low temperature difference is limited by the available planar surface area of the module top face.

The FOB factory cost of the bypass diode/heat spreader assembly, sized for three different current ratings, was analyzed with the results as summarized in Figure 8. In each case, the heat spreader plate area has been determined from the experimentally-derived relationship discussed above. The results of this analysis, as displayed on the right hand graph of the figure, are expressed as the cost of the bypass diode/heat spreader assembly per m^2 of module area as a function of both the annual production rate and the bypass diode rating. It is apparent from these results that the cost of the diode/heat spreader assembly per unit of module area can be decreased by increasing both the current rating and the producton rate for the unit. For a given annual production rate, an increase in diode assembly current rating will reduce the cost per unit area for providing the bypass function, but this benefit is of rapidly diminishing value as this rating approaches 18 amperes (or 15 watts of diode dissipation).

Externally-Mounted Diodes

Current practice for bypass diode mounting uses standard packaged diodes in module-mounted plastic enclosures. Significant technical advantages, relative to the standard diode package, can accrue through the use of a mounted diode cell as illustrated in Figure 9. The overall thermal resistance between the diode junction and a point immediately on the isothermal heat sink side of the grease joint interface between this heat sink and a beryllia (BeO) disk ($R_{\theta js}$) is shown to vary with disk diameter (D) and thickness (t_B) and diode cell diameter (d). For 20 watts of diode dissipation, the total cost, which includes the diode cell, heat sink and BeO insulating disk, is minimized by the use of a BeO disk with a diameter of 0.625 inches and a thickness in the range of 0.093 to 0.150 inches.

A diode cell/heat spreader of this configuration can be packaged within a harness-mounted enclosure as shown in Figure 10. When this enclosure is mated with the module-mounted receptacle, the module becomes the support for the enclosure and the restraint for the harness.

Reliability Considerations

Photovoltaic module bypass diodes operate in a manner which is characterized by the periodic application of a relatively low reverse voltage.

This reverse voltage will generally be less than 15 vdc and will be applied as 12 hours "ON" followed by 12 hours "OFF". Since there will be negligible diode power dissipation during this period, the diode temperature will approximate the solar cell temperature. This temperature will approach the ambient temperature during nighttime or "OFF" periods and will be elevated above the ambient temperature during daylight periods by an amount which varies with the solar intensity and wind speed and direction. Occasionally, the bypass diodes may be required to conduct current in the forward direction at a level which varies with insolation level and circuit loading conditions.

The predominant failure mechanisms found in semiconductor services are related to junction temperature and fit the Arrhenius model as shown in Figure 11 for a typical rectifying diode. The criteria for failure are also consistent with this application and generally include a low threshold of leakage current (10 to 500 μA) at a specified reverse voltage as well as a small change in the forward voltage drop (10 to 100 mV) at a specified forward current. No failure rate data is available for the operation of power diodes in the continuous dc reverse voltage blocking mode which is typical of the normal bypass diode operating condition. There is a general agreement among experts in this field that the continuous dc reverse voltage operation will tend to increase the leakage current with time compared to a normal ac rectifying application. However, the failure limit for reverse voltage leakage current in a photovoltaic module bypass application can be many orders of magnitude higher than that for the power rectifier and still operate satisfactorily.

Notwithstanding the obvious shortcomings in the available failure rate data as it might be applicable to the bypass diode operating conditions, it is possible to draw certain conclusions based upon rectifying diode data. For the photovoltaic module bypass application, the diode reliability will be almost exclusively determined by the reverse bias operating conditions since the exposure time under these conditions is many orders of magnitude larger than the expected exposure to a forward conducting operating condition. Fortunately, the average junction temperature under these reverse bias operating conditions is relatively low; with 45°C being the maximum expected average temperature for a U.S. site location. Also, the magnitude of the reverse voltage is a small fraction of the lowest available rated value for PN junction devices. These two factors combine to yield a low failure rate for this diode application based on the available data.

Conclusions

The conclusions highlighted in Figure 12 clearly differentiate between the motives of the module designer and the motives of the array designer. In any consideration of bypass diodes, it is important to first establish the objectives for the intended application.

DESIGN AND SELECTION OF BYPASS DIODES

GENERAL ELECTRIC CO.

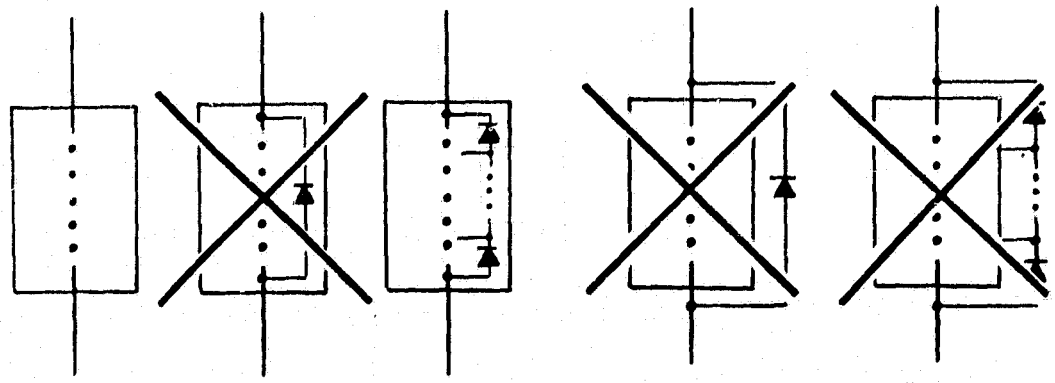
Neal F. Shepard, Jr.

Why Use Bypass Diodes?

- PROVIDES A PARALLEL PATH FOR CURRENT AROUND CIRCUIT ELEMENTS SO THAT
  - SOURCE CIRCUIT I_{sc} IS NOT LIMITED BY A REDUCTION IN THE I_{sc} CAPABILITY OF ELEMENTS WITHIN THE BYPASSED GROUP
  - REMOVAL OF A MODULE FROM AN ILLUMINATED ARRAY DOES NOT CREATE AN ARC
- LIMITS THE REVERSE VOLTAGE THAT CAN BE DEVELOPED ACROSS THE BYPASSED GROUP TO THE FORWARD VOLTAGE DROP OF THE CONDUCTING BYPASS DIODE

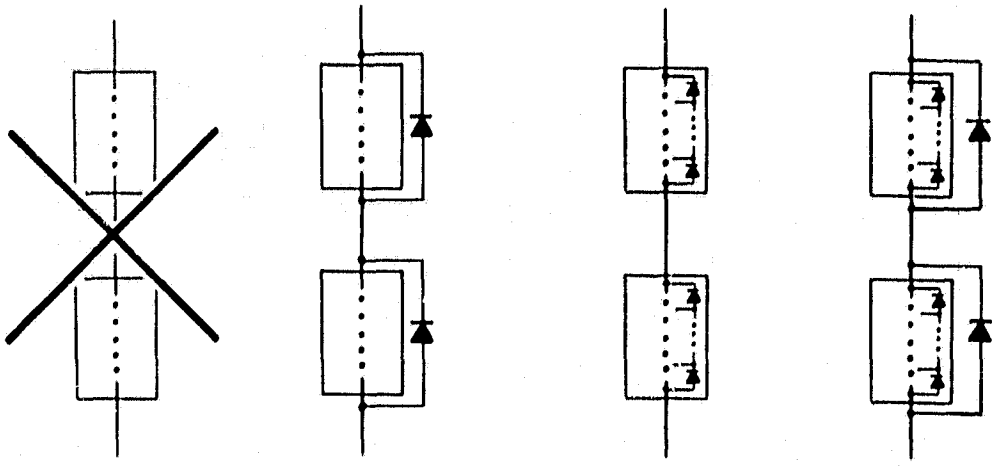
The Module Designer's Bypass Diode Options

REASON FOR DIODE USE - MAXIMIZE PROBABILITY OF SURVIVING ANTICIPATED USE CONDITIONS



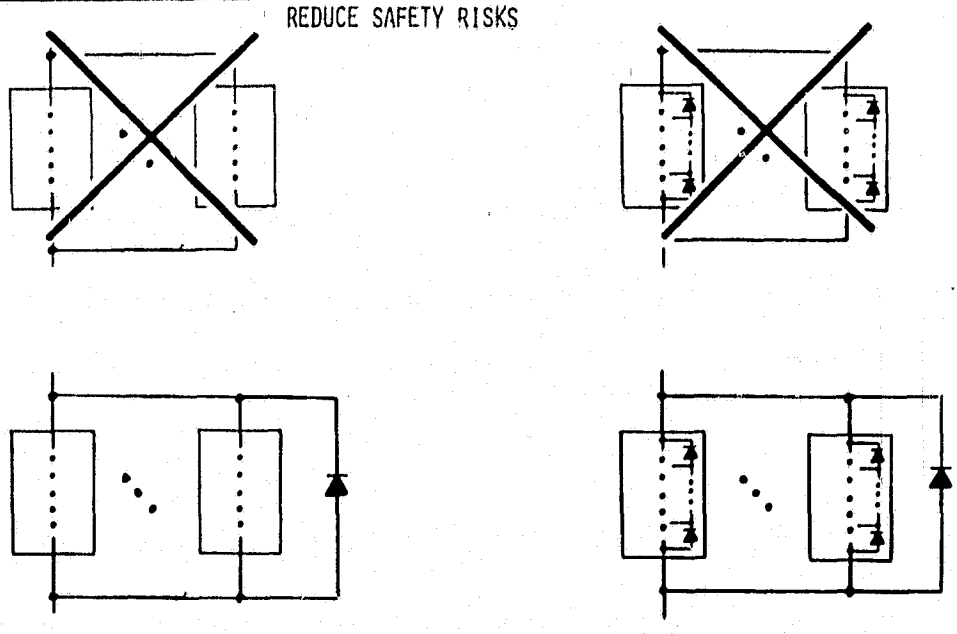
The Array Designer's Bypass Diode Options for Parallel-Connected Series Strings

REASONS FOR DIODE USE - MAXIMIZE ARRAY ENERGY OUTPUT OVER LIFE, REDUCE SAFETY RISKS

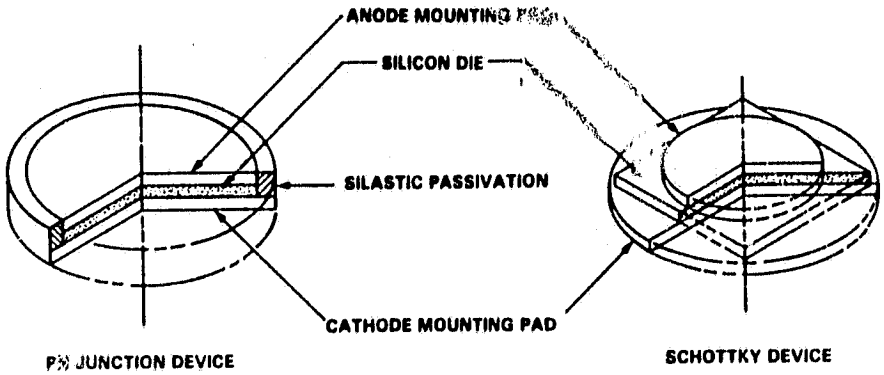


The Array Designer's Bypass Diode Options for Series-Connected Parallel Groups

REASONS FOR DIODE USE - MAXIMIZE ARRAY ENERGY OUTPUT OVER LIFE, REDUCE SAFETY RISKS

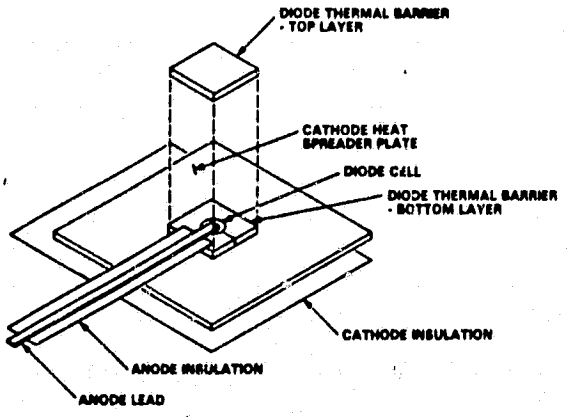


Diode Cell Packaging Configurations

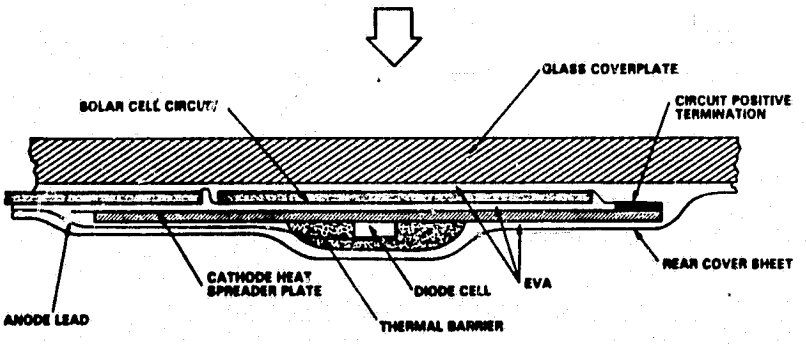


SUPPLIERS:	SEMICON GENERAL INSTRUMENTS	SEMICON INTERNATIONAL RECTIFIER M/ACON MOTOROLA TRW UNITRODE VARO

Encapsulated Bypass Diodes: Packaging Concept

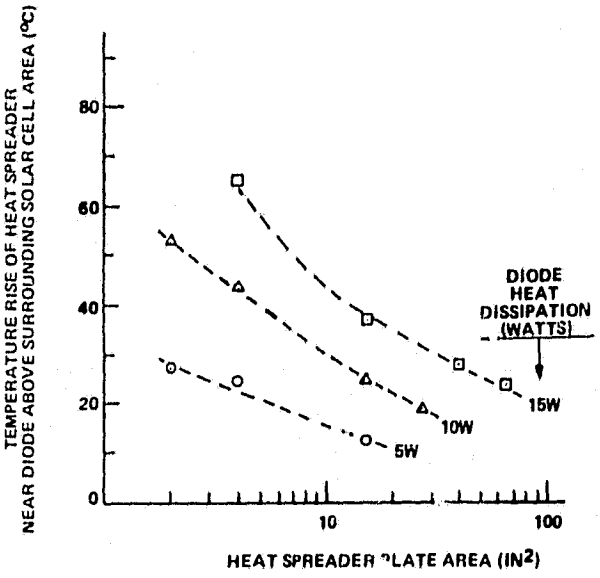


- ENVIRONMENTALLY AND ELECTRICALLY ISOLATED FROM SURROUNDINGS
- NO EXPOSED CONDUCTIVE SURFACES
- NEGLIGIBLE INCREASE IN ENCAPSULANT VOLUME

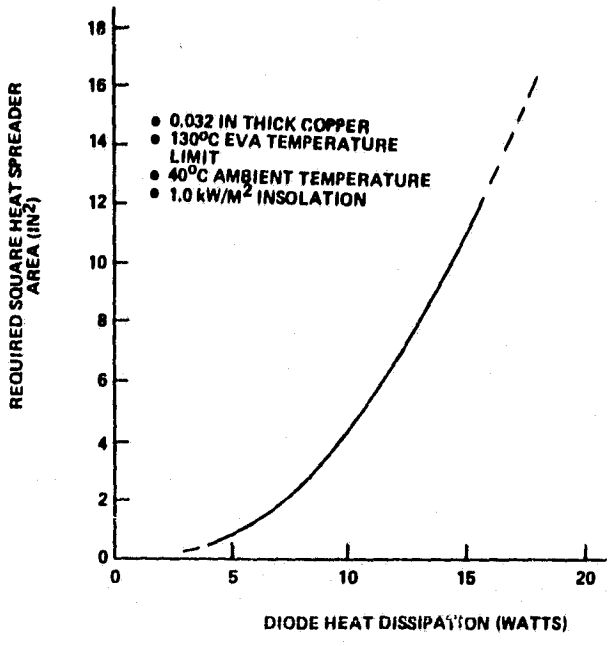


Encapsulated Bypass Diodes: Thermal Capability

EXPERIMENTAL RESULTS



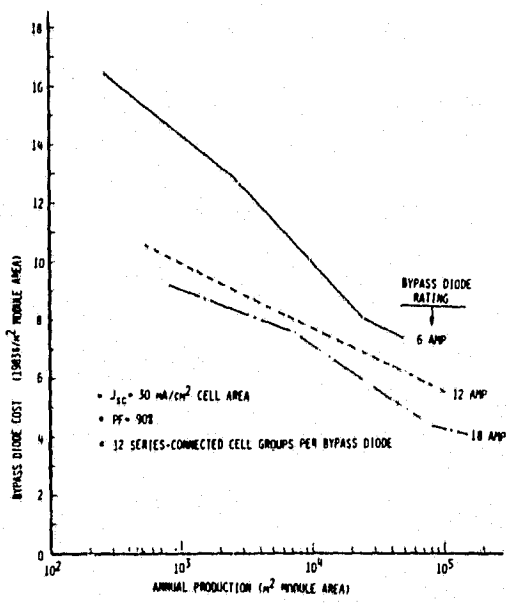
RECOMMENDED HEAT SPREADER SIZE



Encapsulated Bypass Diodes: Cost Analysis

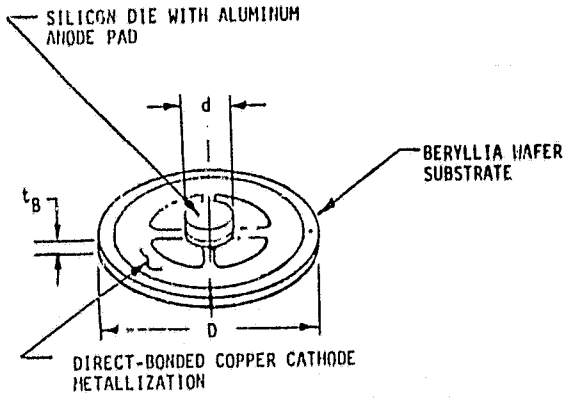
DESIGN PARAMETERS

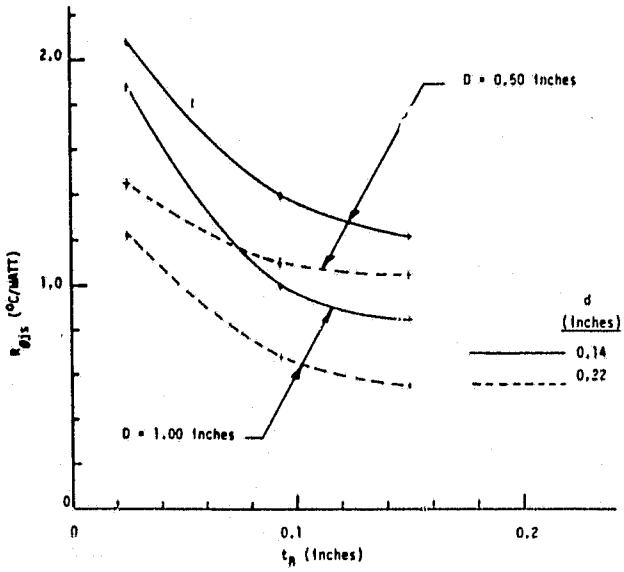
Rated Bypass Current (Amperes)	Diode Cell Manufacturer/Rating	0.032" Thick Square Copper Heat Spreader Plate Size (Inches)	Copper Anode Lead	
			Thickness (Inches)	Width (Inches)
6	Semicon/20 Amp	0.90	0.005	0.120
12	Semicon/40 Amp	2.10	0.007	0.170
18	Semicon/50 Amp	3.30	0.010	0.180



ESTIMATED FOB FACTORY PRICE

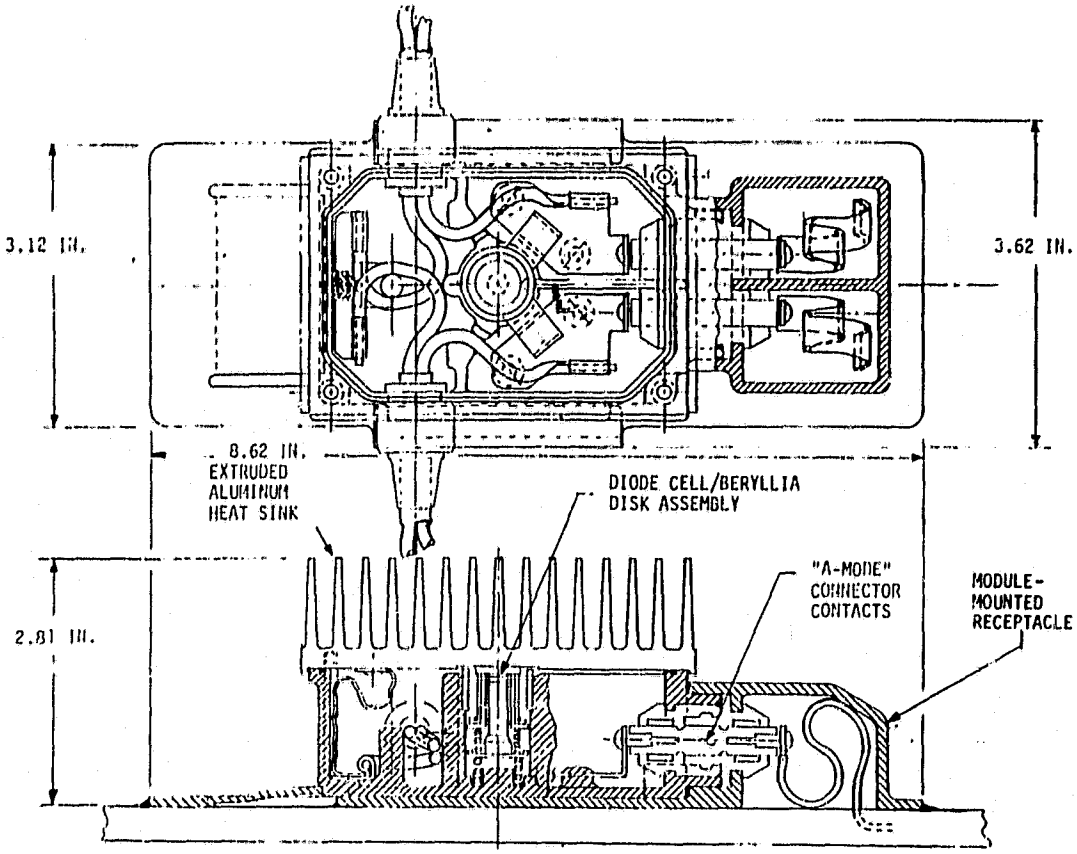
Externally Mounted Diodes: Diode Cell Mounting Approach





- REDUCES JUNCTION-TO-SINK THERMAL RESISTANCE
- ELIMINATES STUD PACKAGE AND ASSOCIATED MOUNTING HARDWARE
- REDUCES THERMAL STRESSES IN SOLDER JOINT BETWEEN SILICON DIE AND HEAT SPREADER
- ASSURES ADEQUATE DIELECTRIC STRENGTH (3000 v MAY BE REQUIRED FOR CENTRAL STATION APPLICATIONS)

Externally Mounted Diodes: Harness Connector Packaging



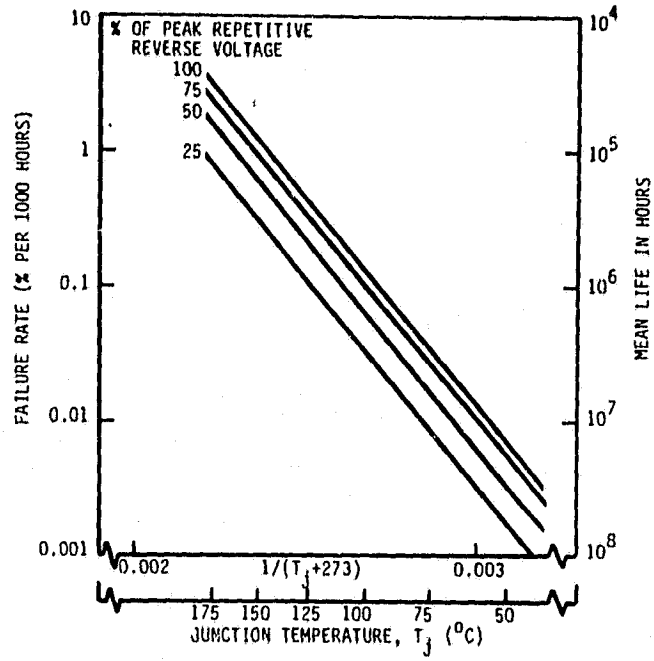
Bypass Diode Reliability Considerations

OPERATING CONDITIONS:

- PROLONGED OPERATION WITH THE PERIODIC APPLICATION OF A LOW REVERSE VOLTAGE
- OCCASIONAL OPERATION IN A FORWARD CONDUCTION MODE

DESIGNING FOR HIGH RELIABILITY

- DERATE REVERSE VOLTAGE
- LIMIT JUNCTION TEMPERATURE TO 125°C UNDER WORST CASE FORWARD CONDUCTION CONDITIONS
  - MAXIMUM AMBIENT TEMPERATURE
  - MAXIMUM INSOLATION



FAILURE RATE FOR A TYPICAL RECTIFYING DIODE

Conclusions

- IF THE MODULE DESIGN DICTATES MULTIPLE BYPASS DIODES, THE MODULE DESIGNER SHOULD
  - USE AN INTERNALLY-ENCAPSULATED PACKAGING APPROACH WITH PN JUNCTION DIODE CELLS
- FOR PARALLEL-CONNECTED SERIES STRING APPLICATIONS, THE ARRAY DESIGNER SHOULD
  - USE UNPACKAGED DIODE CELLS MOUNTED TO BeO HEAT SPREADERS
  - PACKAGE THE BYPASS DIODE INTEGRAL WITH THE MODULE CONNECT-MEANS ON THE HARNESS SIDE OF THE MODULE CONNECTOR INTERFACE
  - LIMIT SOURCE CIRCUIT CURRENT TO 25 AMPERES
- FOR SERIES-CONNECTED PARALLEL GROUP APPLICATIONS, THE ARRAY DESIGNER SHOULD
  - USE A SINGLE DIODE FOR EACH PARALLEL GROUP
  - PACKAGE THE BYPASS DIODE IN A SEPARATE STRUCTURE-MOUNTED ENCLOSURE
  - LIMIT SOURCE CIRCUIT CURRENT TO ? AMPERES

N84 32689

A REVIEW AND SUMMARY OF CELL AND MODULE MISMATCH LOSSES FROM THEORETICAL AND EXPERIMENTAL STUDIES

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Albuquerque, NM 87106

INTRODUCTION

This paper attempts to consolidate the work performed to date on power loss due to PV cell and module parameter mismatch. The losses result from the fact that current-voltage (I-V) characteristics of cells (and consequently, of modules) vary over a manufactured lot. Therefore, the peak power and the peak power I-V point vary from cell to cell. Cells connected in series or parallel are constrained to operate at the same current or voltage; therefore, most cells will not be operating at their peak power points. The largest parameter variation occurs in the cell photocurrent generation; therefore, the most significant loss occurs in series connections since all cells are essentially limited by the lowest photocurrent. As a result, most theoretical studies have addressed only photocurrent variation effects, considering shunt and series resistance, ideality factor and saturation current to be comparatively insignificant. Experimental studies, on the other hand, must be carefully configured to eliminate experimental errors. Only one experimental study could be identified which was specifically configured to study mismatch loss effects. This was the Beverly High School PRDA Study (1). Other experimental results consist of estimates based on limited data not taken from specially configured tests.

REVIEW OF STUDIES

A computer study was performed by JPL (2) in which typical stepped, truncated, photocurrent distributions were postulated and assigned to cells by a Monte Carlo method. To form modules cells were combined in series by adding voltages along constant current lines and in parallel by similarly adding currents. Details and results of the study are shown in the accompanying viewgraphs. A total of less than 200 cells were used for each case. The principal conclusion was that mismatch loss in a module or small number of modules is not significant (<1.25%) if cells are sorted into bins so that photocurrent variations are no greater than $\pm$10%. Also, mismatch losses can be reduced by paralleling strings and reducing the length of series strings. The study did not address other parameter variations. In addition, the cell I-V curves generated by photocurrent perturbations all have the same V_{OC}. The study does not claim to assess array level mismatch loss. A study performed by Bucciarelli (3), which consisted of developing simplified equations based on the JPL results, will not be discussed here.

BDM performed a computer study using the El Paso Electric PRDA for modeling (4). The PV-TAP computer code was used with Gaussian distributions on photocurrent. Details and results of this study are also contained in the viewgraphs. An Ebers-Moll single exponential model was used which will vary V_{OC} logarithmically with photocurrent. Other parameter variations were not

considered. The results may be somewhat conservative because the distributions were not truncated. Since 6480 cells (representing a third of the total array) were simulated, there may have been an average of about one cell in each 9-module string with a photocurrent outside the 3-sigma limits. It was assumed that initial cell photocurrent distribution was ±10% in a manufactured lot, but that photocurrents would vary after encapsulation and installation due to reflectivity changes, spectral mismatch and initial exposure changes. Final photocurrent distributions could be increased to ±15% or ±17.5%. If cells were initially sorted into ±2.5% bins, these bins would spread corresponding to ±7.5% or ±10%. Three application cases considered were: random utilization of cells with no binning; sorting of cells into bins for modules but no module matching; and matching of modules in strings by bin number. For random useage, mismatch losses were 9.5 - 11.2%; with sorting and matching, however, losses were reduced to 4.5 - 6.1%.

Based on the differences in modeling techniques and the size of the array, the BDM study would be expected to produce higher losses. If the "random useage" case is compared with the second JPL distribution, the BDM results are about twice as high. The many differences, however, make detailed comparisons impossible. In the actual PRDA array, cell binning was used and modules were matched in a string. The array is currently producing power about 6% lower than would be expected based on a sample of module I-V curves taken onsite 2 years ago. However, measurements taken over a period of time indicate that more than half of this may be due to degradation effects. It should also be noted that this array operates at fixed voltage which might increase mismatch losses and that some of the modules are operating at 2-3V below the nominal module operating voltage.

Another mismatch loss study (5) was performed by BDM with the use of PV-TAP. Residential and central station modules and array were developed from advanced PV technology cells. The modeling techniques were the same as in the previous study. Results are shown in the accompanying viewgraphs. In this study, technology applications were rank ordered by expected tolerance to mismatch losses based on number of cells in series, number of parallel strings in module, fill factor and paralleling at the cell level. The many minor differences between the arrays overrode these factors to some extent for the 10 and 20% photocurrent variation cases but for the 50% case, the results lined up as expected. The one exception is the GaAs P2S6 case, the only example of paralleling at the cell level, which produced the lowest losses. Analyzing the El Paso Electric Study results in a similar manner and overlaying the results produces good agreement.

The most detailed experimental study which could be identified was performed on the Beverly High School PRDA (1). In this array, five modules are paralleled before seriesing to obtain string voltage. Operating voltages in the array were measured for a sample of modules; then, modules were disconnected to obtain I-V curves to assess power loss. Total power loss of 1.4% was reported, of which about half was due to subarray paralleling. Effects of module paralleling were also assessed. It was concluded that in current matched modules, voltage variations became significant and resulted in mismatch loss when modules are paralleled. The results should be considered valid only for this array. Use of modules with smaller series strings (5V modules) might produce different results. The implication, however, is that modules connected in parallel should be matched by voltage rather than

current. This may be difficult to implement, however, due to manufacturers' module testing techniques which determine power at a fixed voltage.

Other less rigorous experimental results are also summarized in the viewgraphs. Results are estimates based on array power compared with manufacturers' I-V curves or on expected effectiveness of module matching techniques (Hughes).

A recent paper from Belgium (9) reported at the Fifth European Communities PV Conference recommends storing both the peak power voltage and current of modules on files for computer matching of modules, by voltage for parallel connection of modules, and by group currents for series connection of groups. Only an abstract is available at this time which claims that mismatch losses can be kept to about 1%. Actual array losses were not given.

Conclusions are summarized in the final viewgraphs. One of the principal differences between the theoretical studies and experimental results is that the former is based on cell variations while the latter is based on module variations. Cell binning, however, is a prerequisite for low array mismatch losses. It appears that array mismatch losses can be kept to about 1-2% but there is a lack of definitive experimental results. The desirability of voltage matching for parallel connections is not certain. The other conclusions outline some continuing concerns and the need for continued attention to mismatch loss effects in future systems.

I would like to acknowledge helpful discussions with the following persons: R. Addis, Solar Power; J. Castle and G. Naff, Hughes; M. Fuentes and H. Post, Sandia; C. Gonzales and R. Ross, JPL; G. Noel, Battelle; V. Risser, NMSEI.

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A REVIEW AND SUMMARY OF CELL AND MODULE MISMATCH LOSSES FROM THEORETICAL AND EXPERIMENTAL STUDIES

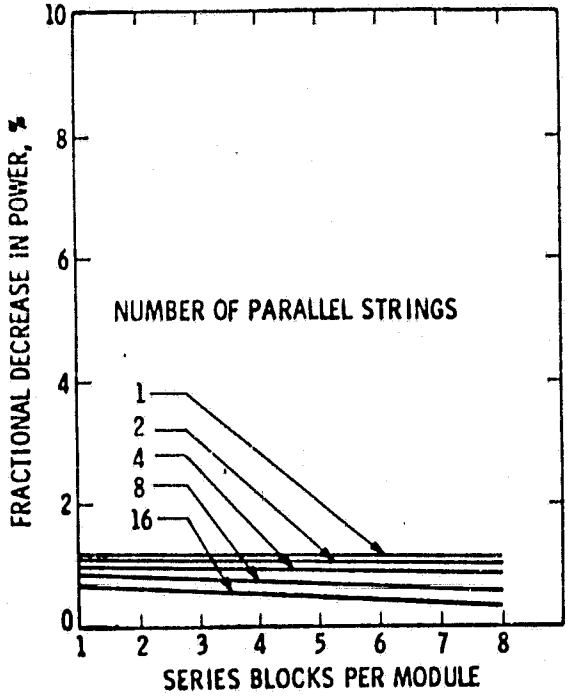
THE BDM CORP.

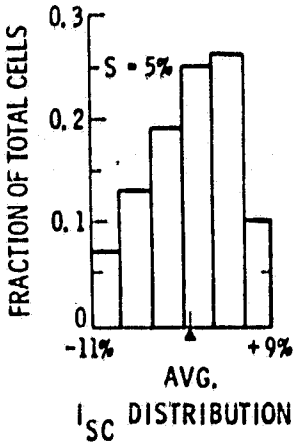
Timothy J. Lambarski

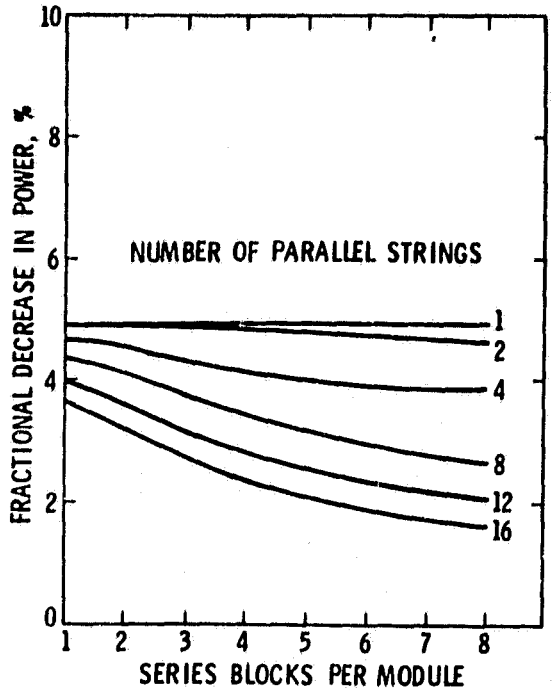
JPL Study Assumptions and Modeling

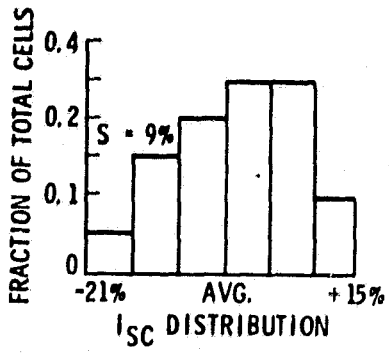
- PURPOSE — TO ASSESS CELL MISMATCH LOSSES IN MODULES
- I_{PH} VARIATIONS ONLY, TRUNCATED DISTRIBUTIONS
- CELL FILL FACTOR = 0.70
- CELL I-V CURVES OBTAINED FROM PERTURBATIONS ABOUT THE AVERAGE
- CELLS COMBINED BY ADDING POINTS ON CURVES
- NUMBER OF CELLS — LESS THAN 200

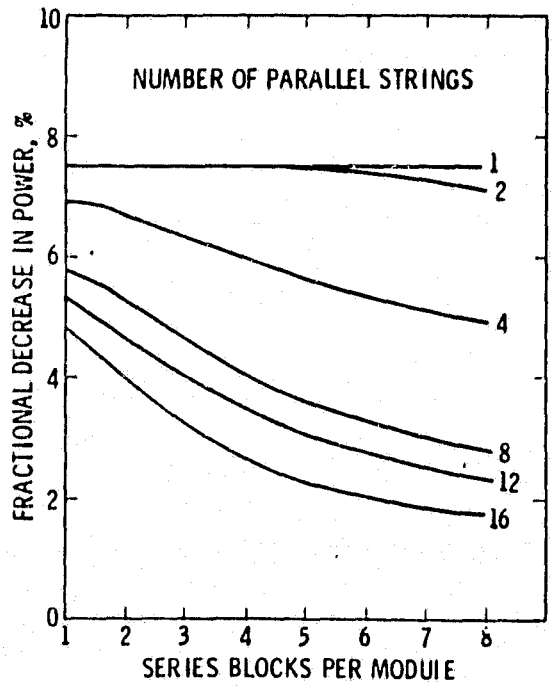
Module Mismatch vs Cell I_{sc} Distribution and Module Series-Parallelling

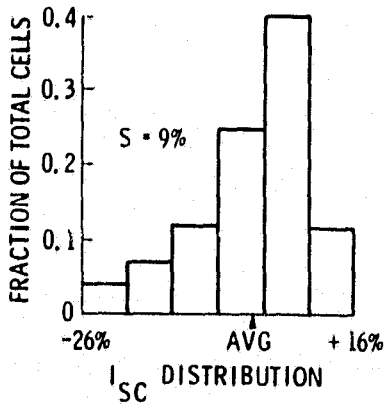












JPL Study Conclusions

- **MISMATCH LOSSES INSIGNIFICANT (c. 1.25%) FOR CELL PHOTOCURRENT VARIATIONS $< \pm 10\%$**

- **MISMATCH LOSSES FOR LARGER CELL PHOTOCURRENT VARIATIONS CAN BE REDUCED TO 2-4% RANGE BY PARALLELING STRINGS AND REDUCING LENGTH OF SERIES STRINGS**

EL Paso Electric PRDA Theoretical Study Assumptions and Modeling

- I_{PH} VARIATIONS ONLY, GAUSSIAN DISTRIBUTIONS
- CELL FILL FACTOR = 0.70 (SOLAR POWER CELLS)
- PV-TAP COMPUTER CODE WITH EXPONENTIAL CELL MODEL
- 18 CELLS IN BYPASS GROUP; 2 SERIES GROUPS IN MODULE
- 9 MODULES IN SERIES STRING; 20 STRINGS
- 1) RANDOM UTILIZATION OF CELLS
  2) CELL SORTING IN MODULES, NO MODULE MATCHING
  3) CELL SORTING IN MODULES, MODULE MATCHING IN STRING

Bin Distributions

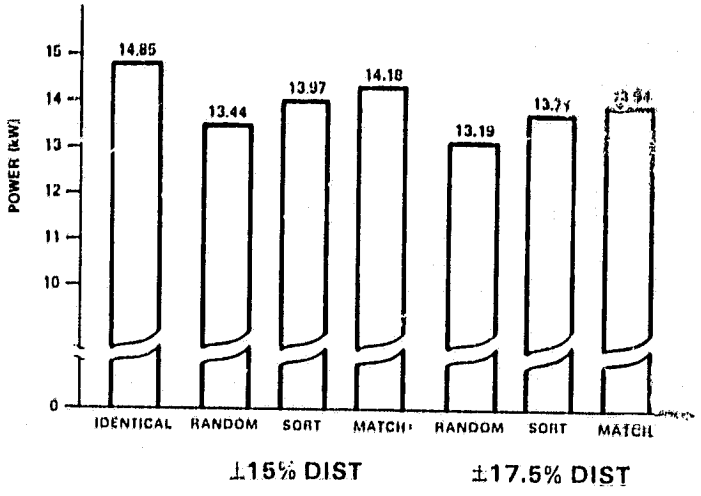
BIN NO.	ORIGINAL ±2.5% BINS*	±7.5% DISTRIBUTION*	±10% DISTRIBUTION*
1	1.8 - 1.9 AMPS	1.7 – 2.0 AMPS	1.65 – 2.05 AMPS
2	1.9 - 2.0 AMPS	1.8 - 2.1 AMPS	1.75 - 2.15 AMPS
3	2.0 - 2.1 AMPS	1.9 - 2.2 AMPS	1.85 - 2.25 AMPS
4	2.1 - 2.2 AMPS	2.0 - 2.3 AMPS	1.95 - 2.35 AMPS
OVERALL DISTRIBUTIONS	±10%	±15%	±17.5%

*BIN DISTRIBUTIONS ARE ONLY APPROXIMATE AND ARE BASED ON 2 AMPS FOR SIMPLICITY

Matrix of Analyses

RUN NO.	CONDITIONS	DISTRIBUTION	
		RUN A	RUN B
1.	ALL CELLS IN ARRAY IDENTICAL	NONE	N/A
2.	RANDOM I_{SC} VARIATION IN ARRAY	±15%	±17.5%
3.	I_{SC} VARIATION IN MODULE DUE TO BINNING	±7.5%	±10%
	MODULES IN STRING SELECTED RANDOMLY	4 BINS/STRING	4 BINS/STRING
4.	I_{SC} VARIATION IN MODULE DUE TO BINNING	±7.5%	±10%
	MODULES IN STRINGS SELECTED BY BIN	1 BIN/STRING	1 BIN/STRING
	STRINGS IN ARRAY SELECTED RANDOMLY	4 BINS/ARRAY	4 BINS/ARRAY

Power Produced by Each Case



Results Expressed in Terms of Percent Reductions From the Ideal Case

RUN NO.	POWER (kW)	% REDUCTIONS
1	14.85	9.5% → 5% SAVING
2A	13.44	
3A	13.97	5.93%
4A	14.18	4.51%
1	14.85	11.2% → 5.1% SAVING
2B	13.19	
3B	13.71	7.7%
4B	13.94	6.1%

Comparison With JPL Study

- GAUSSIAN VERSUS TRUNCATED STEPPED DISTRIBUTION
  - — POSSIBILITY OF LOWER CELLS
- ARRAY VERSUS MODULE
  - — LONGER STRINGS
  - — MORE CELLS
  - — POSSIBILITY OF LOWER CELLS
- EXPONENTIAL EQUATIONS MAY PRODUCE LARGER VOLTAGE VARIATIONS
- BDM "RANDOM USE" CASE SHOULD PRODUCE HIGHER LOSSES THAN JPL SECOND DISTRIBUTION CASE (9.5% VERSUS 5%)

El Paso Electric PRDA Experimental Results

- SOLAR POWER MODULES, MODULE MATCHING IN STRING
- EXPECTED POWER BASED ON MODULE MEASUREMENTS: 16.5 kW
- EXPERIMENTAL NORMALIZED POWER: 15.5 kW
  - — REGRESSION TECHNIQUE BASED ON MEASUREMENTS OVER PERIOD OF TIME
- TOTAL LOSSES: 6%, MODULE DEGRADATION MAY ACCOUNT FOR MORE THAN HALF
- ARRAY OPERATES AT FIXED VOLTAGE BELOW PEAK VOLTAGE
- SEVERAL MODULES OPERATING 2-3 V BELOW NOMINAL OPERATING VOLTAGE

Advanced PV Systems Theoretical Study
Assumptions and Modeling

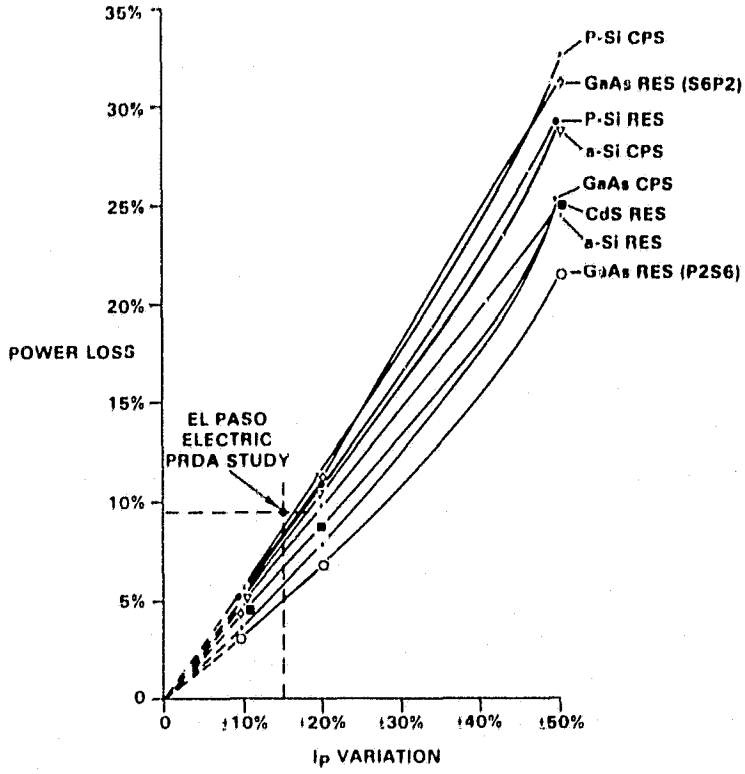
- EXTRAPOLATED EFFICIENCY CELLS FROM ADVANCED PV TECHNOLOGIES
- I_{PH} VARIATIONS ONLY, GAUSSIAN DISTRIBUTIONS
- PV-TAP COMPUTER CODE WITH EXPONENTIAL CELL MODEL
- RANDOM UTILIZATION OF CELLS
- RESIDENTIAL — 200 V STRINGS
  CENTRAL STATION — 1000 V STRINGS

Assessment of Factors Affecting Photocurrent Variation Responses

	POLY-SILICON		A-SILICON		$CdS/CuInSe_2$	GaAs			EL PASO ELECTRIC STUDY
VALUE/RANKING	RES	CPS	RES	CPS	RES	RES (S6P2)	RES (P2S6)	CPS	
BYPASS GROUP SIZE	10/4*	10/4	7/3	7/3	10/4	6/2	6/2	4/1	18/5
PARALLELING IN MODULE	4/2	3/3	10/1	2/4	4/2	2/4	2/4	2/4	1/5
FILL FACTOR	0.77/3	0.77/3	0.69/2	0.69/2	0.65/1	0.82/4	0.82/4	0.77/3	0.70/2
PARALLELING CELL	NO/2	NO/2	NO/2	NO/2	NO/2	NO/2	YES/1	NO/2	NO/2
TOTAL WEIGHT	11	12	8	11	9	12	11	10	14

*WITHIN A CATEGORY, TECHNOLOGIES ARE RANK ORDERED ACCORDING TO TOLERANCE TO PHOTOCURRENT VARIATIONS, THEREFORE, 1 REPRESENTS THE HIGHEST TOLERANCE

Power Loss Due to I_P Variation



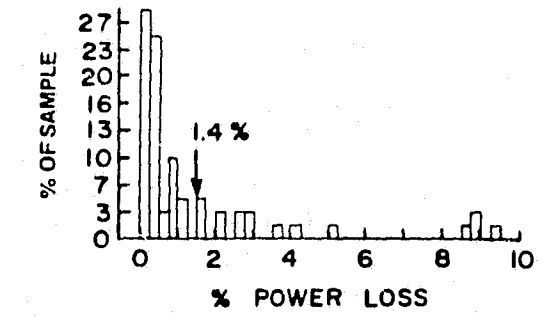
Arrangements of Applications by Decreasing Power Loss

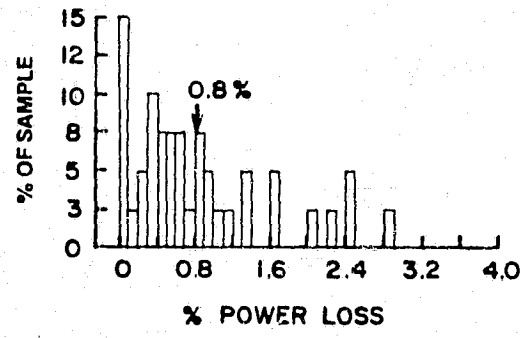
PHOTOCURRENT VARIATION	+10%		+20%		+50%	
APPLICATION	POLY-Si CPS	-5.5 -12	POLY-Si CPS	-11.4-12	POLY-Si CPS	-32.5-12
-- POWER LOSS (%)	POLY-Si RES	-5.39-11	GaAs RES (S6P2)	-11.4-12	GaAs RES (S6P2)	-31.3-12
— WEIGHT	A-Si CPS	-5.13-11	POLY-Si RES	-10.9-11	POLY-Si RES	-29.5-11
	A-Si RES	-4.93-8	A-Si CPS	-10.4-11	A-Si CPS	-29.2-11
	GaAs RES (S6P2)	-4.41-12	A-Si RES	-10.0-8	GaAs CPS	-25.6-10
	CdS RES	-4.33-9	CdS RES	-8.9-9	CdS RES	-25.2-9
	GaAs CPS	-3.68-10	GaAs CPS	-7.8-10	A-Si RES	-25.0-8
	GaAs RES (P2S6)	-3.08-11	GaAs RES (P2S6)	-6.9-11	GaAs RES (P2S6)	-21.4-11

Beverly High School PRDA Experimental Study

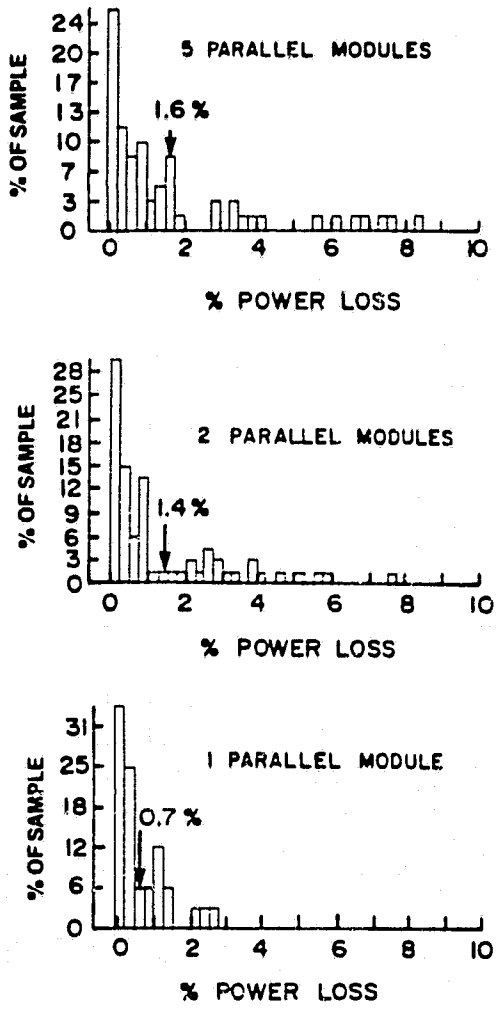
- SOLAR POWER MODULES (36 SERIES CELLS IN 2 BYPASS GROUPS)
- FIVE PARALLEL MODULES BY 16 GROUPS IN SERIES IN SUBARRAY
- MODULE MATCHING IN SUBARRAY ON ±2.5% I_{SC}
- MEASURED PARALLEL GROUP VOLTAGE
- DISCONNECTED MODULE AND MEASURED POWER AT V_{OP} AND PEAK
- 60 MODULES OUT OF 3200 FOR TOTAL MISMATCH
- 64 MODULES IN TWO SUBARRAYS FOR EFFECTS OF PARALLELING STUDY

Distribution of Total Array and Subarray Paralleling Losses

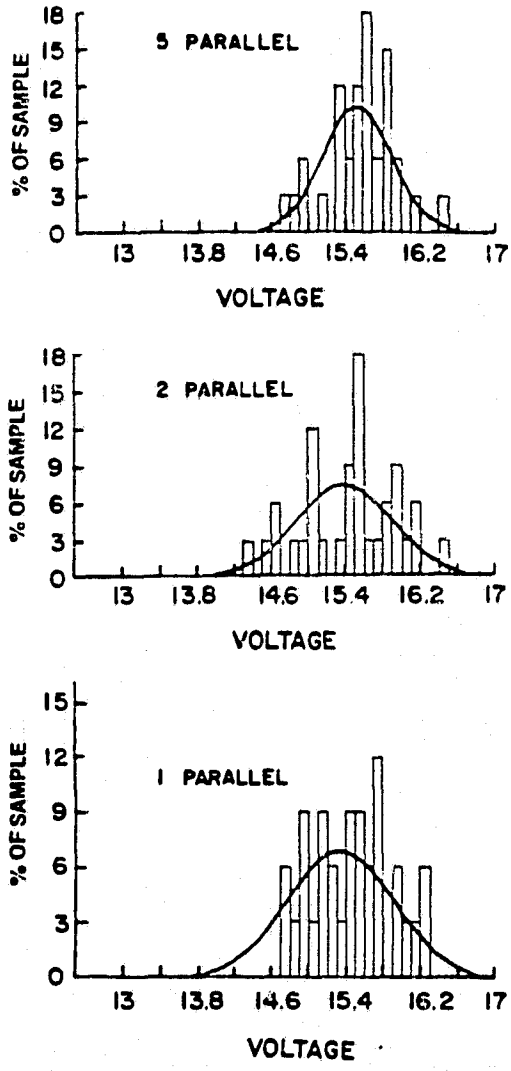




Distribution of Power Loss vs Degree of Paralleling



Distribution of Operating Voltage vs Degree of Paralleling



Conclusions From Beverly PRDA Study

- ARRAY LOSSES LIMITED TO 1.4% BY MODULE MATCHING
- SUBARRAY MISMATCH LOSSES MAY ACCOUNT FOR HALF OF THIS
- PARALLELING MODULES NOT RECOMMENDED FOR I_{SC} MATCHED MODULES DUE TO VOLTAGE MISMATCH EFFECTS
- JPL AND BDM STUDIES ASSESSED I_{PH} VARIATION ONLY
  - V_{MP} VARIED ONLY INDIRECTLY DUE TO ΔI_{PH}
- RESULTS MAY BE DEPENDENT ON LENGTH OF SERIES STRING IN MODULE

BDM Southwest RES Prototype Experimental Results

- MOTOROLA MODULE (33 SERIES CELLS)
- 13 SERIES MODULES BY 9 PARALLEL STRINGS
- ESTIMATES FROM STRING DATA COMPARED WITH MANUFACTURER'S MODULE I-V CURVES
- ΔP = APPROX. ±5%
- MISMATCH LOSS = 2-3.5%

Battelle 30 kW Array at Sandia: Experimental Results

- SOLEC MODULES (11 SERIES CELLS x 6 PARALLEL STRINGS)
- TWO PARALLEL MODULES
- MODULE FF = 0.70, $\Delta P_M < \pm 10\%$
- NO MODULE MATCHING
- 5-7% MISMATCH LOSSES
- WIRING LOSSES < 1%

Hughes 30 kW Array at Sandia: Experimental Results

- SOLAREX MODULES (12 SERIES CELLS x 6 PARALLEL STRINGS)
- NO MODULE PARALLELING
- MODULE FF = 0.65 — 0.68
- MODULE MATCHING IN STRING TO 0.25A I_{MP} (2%)
- WORST CASE ESTIMATES
  - — STRING LOSSES < 1%
  - — TOTAL ARRAY LOSSES < 2%

Mismatch Loss Minimization in PV Pilot Projects (Reported at 5th European Communities PV Conference)

- MODULES CLASSIFIED BY PEAK POWER CURRENT AND VOLTAGE
- STORED ON COMPUTER FILE
- MODULES IN PARALLEL MATCHED BY VOLTAGE
- PARALLEL GROUPS IN SERIES MATCHED BY CURRENT
- SIMULATION INDICATES LOSSES CAN BE KEPT TO ABOUT 1%

Summary and Conclusions

- ARRAY LOSSES SHOULD BE BASED ON MODULE NOT CELL VARIATIONS
- CELL BINNING IS PREREQUISITE FOR LOW ARRAY MISMATCH LOSSES
- LOSSES MAY BE 4-7% WITHOUT MODULE MATCHING
- LOSSES MAY BE 1-2% WITH MODULE MATCHING
- LACK OF DETAILED EXPERIMENTAL ASSESSMENTS
- VOLTAGE MATCHING MAY BE BENEFICIAL WHEN PARALLELING MODULES
- FIXED VOLTAGE OPERATION MAY INCREASE MISMATCH LOSS AND DEGRADATION
- HIGHER FILL FACTORS, LONGER SERIES STRINGS PRODUCE HIGHER LOSSES
- LOSSES MAY BE MORE SIGNIFICANT FOR ADVANCED TECHNOLOGIES
  - — MONOLITHIC DEPOSITION = LARGER VARIATIONS
  - — PIN-HOLE SHORTS MAY PRECLUDE CELL PARALLELING
  - — HIGH CURRENT RATIOS
- MISMATCH LOSSES AT OTHER THAN STANDARD CONDITIONS NOT KNOWN
- EFFECTS OF INITIAL MISMATCH ON DEGRADATION LOSSES NOT KNOWN
- FAILURE OF MANY ARRAYS TO ACHIEVE EXPECTED POWER NOT FULLY UNDERSTOOD

D7

SOURCE CIRCUIT DESIGN CONSIDERATIONS

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The cost of several circuit configurations for large (5MW) array fields have been investigated with the objective of assessing the relative costs of high and low voltage configurations. The three source circuit NOC voltages included in the evaluations were 400V (ungrounded), 800V (±400V center grounded), and 2000V (±1000V center grounded). Four source circuit configurations were considered for each of the three NOC voltages. These configurations correspond to source circuit currents of 15, 30, 45, and 60 amperes, respectively. Conceptual layouts for 5MW building blocks for each of the above configurations were developed. These designs were optimized to minimize BOS electrical and structural costs. Only the BOS electrical costs were evaluated in detail. The designs were broken down into the following elements for costing:

- Basic Source Circuit - intermodule wiring, bypass diodes and associated hardware, source circuit to J-Box wiring, etc.
- J-Box - blocking diodes, varistors, heat sinks, housing, etc.
- Disconnects - source circuit disconnects, fuses, housing, etc.
- Bus Cabling - J-Box to PCU interface wiring, trenching, etc.
- Interface - bus bar, group disconnects, fuses, etc.
- Fault Detection - shunts, signal wire, electronics, alarm, etc.

Specific manufacturers hardware was identified for all cost elements and sub-elements and high volume cost estimates were obtained either by direct quotation or by projection when direct quotations could not be obtained. All costs are based on currently available hardware and the use of accepted design guidelines and rules.

A summary of the results of the cost calculations is given in the attached table. The costs are given in dollars-per-watt for each of the cost elements. The major conclusions from the analysis are:

- High-voltage, low-current source circuits do not appear economical.

- At higher currents the cost of high-voltage and low-voltage circuits begin to approach each other.

- There appears to be no significant near-term cost advantage in the use of high-voltage source circuit designs.

- Developmental work/manufacturer stimulation is necessary to provide lower-cost, high-voltage hardware appropriate to high-voltage photovoltaic array designs.

SOURCE-CIRCUIT DESIGN CONSIDERATIONS

BATTELLE'S COLUMBUS LABORATORIES

G.T. Noel

Cost Element Contributions

COST ELEMENT CONTRIBUTIONS IN DOLLARS/WATT (10% EFFICIENCY)
FOR 5MW BUILDING BLOCK DESIGNS - 400V, 800V, AND 2000V SOURCE CIRCUITS

	400V UNGROUNDED				±400V CENTER GROUNDED				±1000V CENTER GROUNDED			
	15A	30A	45A	60A	15A	30A	45A	60A	15A	30A	45A	60A
Source Circuit Cost	0.21	0.12	0.22	0.24	0.21	0.12	0.21	0.24	0.67	0.35	0.30	0.24
J-Box Cost	0.07	0.04	0.03	0.02	0.05	0.03	0.02	0.01	0.03	0.02	0.01	0.01
Bus Cabling Cost	0.07	0.04	0.03	0.02	0.06	0.03	0.03	0.02	0.02	0.01	0.01	0.01
Interface Cost	0.05	0.04	0.03	0.03	0.03	0.02	0.02	0.01	0.01	0.01	0.01	0.01
Disconnect Cost	NA*	NA*	NA*	NA*	0.12	0.06	0.04	0.03	0.34	0.17	0.11	0.08
Fault Detection Cost	0.11	0.06	0.04	0.03	0.06	0.03	0.02	0.01	0.02	0.01	0.01	0.01
TOTAL	0.51	0.30	0.35	0.34	0.53	0.29	0.34	0.32	1.09	0.57	0.45	0.36

(*) Disconnect cost included in J-Box cost for 400V ungrounded source circuits

Objective

ASSESS ARRAY FIELD ELECTRICAL BOS COST DIFFERENCES FOR ALTERNATIVE SOURCE CIRCUIT DESIGNS IN CENTRAL STATION CONFIGURATIONS

Ground Rules

- ALL DESIGNS ANALYZED IN 5 MW BUILDING BLOCK CONFIGURATION
- ALL DESIGNS BASED ON 5 VOLT PV MODULES
- ALL COSTS BASED ON HIGH QUANTITY QUOTES FOR CURRENTLY AVAILABLE HARDWARE
- ALL DESIGNS USE ONE BYPASS DIODE PER SERIES BLOCK

Major Cost Elements of the Analysis

- SOURCE CIRCUIT COSTS
- J - BOX COSTS
- BUS CABLING COSTS
- INTERFACE COSTS
- CIRCUIT DISCONNECT COSTS
- FAULT DETECTION COSTS

Basic Source Circuit Subelements

- INTERMODULE WIRING
  - WIRE
  - INTERCONNECTS
  - LABOR
- BYPASS DIODES
  - DIODES
  - HEAT SINKS
  - HOUSING
  - INSTALLATION (LABOR)
- SOURCE CIRCUIT TO J-BOX WIRING

J-Box Subelements

- BLOCKING DIODES
- VARISTORS
- CENTER TAP GROUNDING (800V, 2000V)
- SHUNT
- DISCONNECT SWITCH (400V)

Bus Cabling Subelements

- CABLE (J-BOX TO INTERFACE)
- CABLE TRENCH
- LABOR

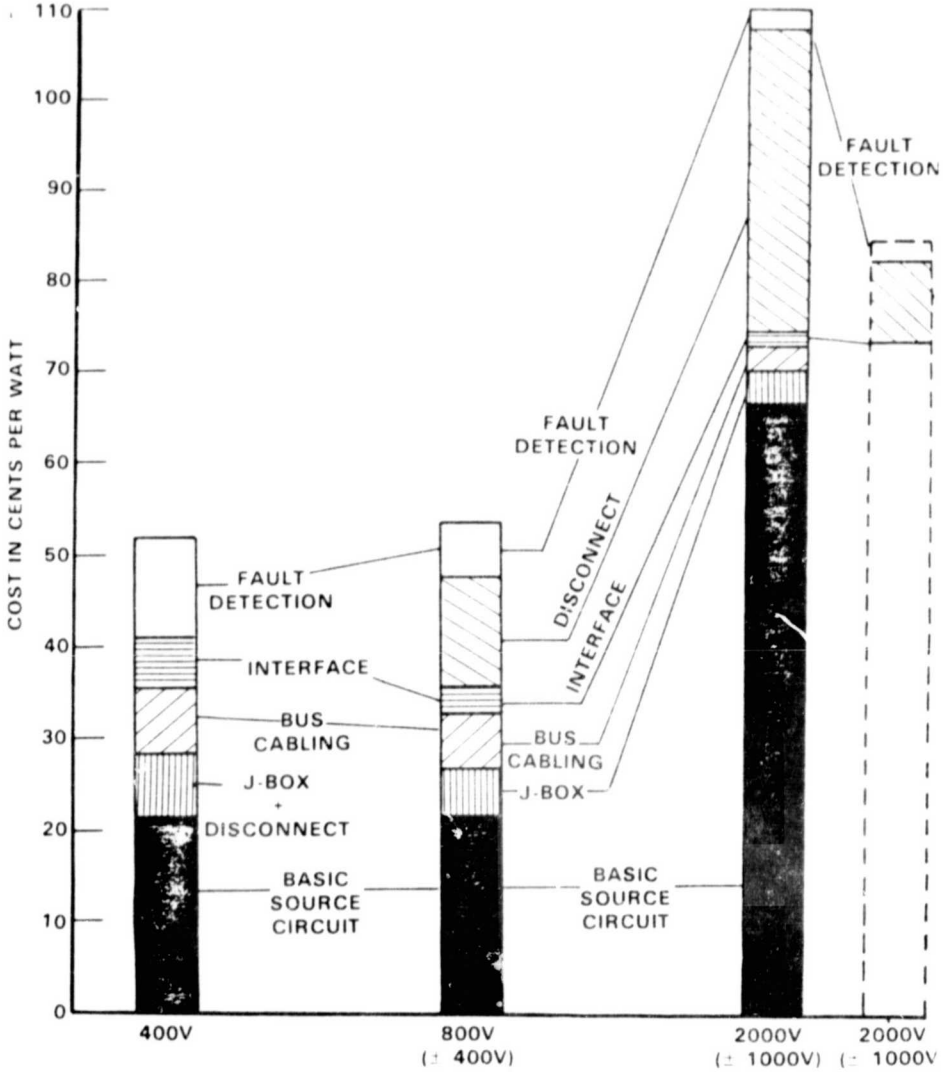
Disconnect Subelements

- DISCONNECT SWITCH
- HOUSING
- MOUNTING/INSTALLATION

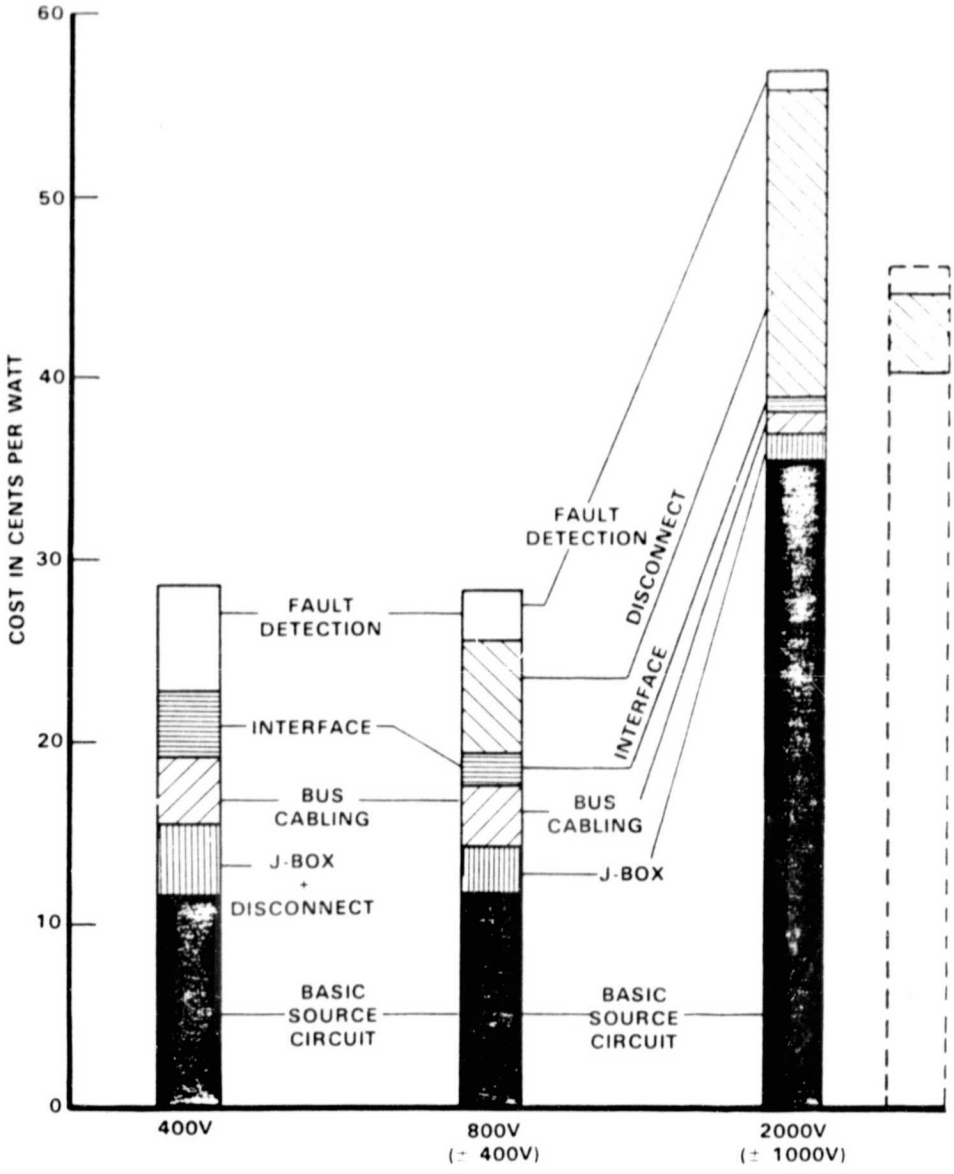
Fault Detection Subelements

- SIGNAL WIRE
- SENSING ELECTRONICS
- ALARM INDICATOR

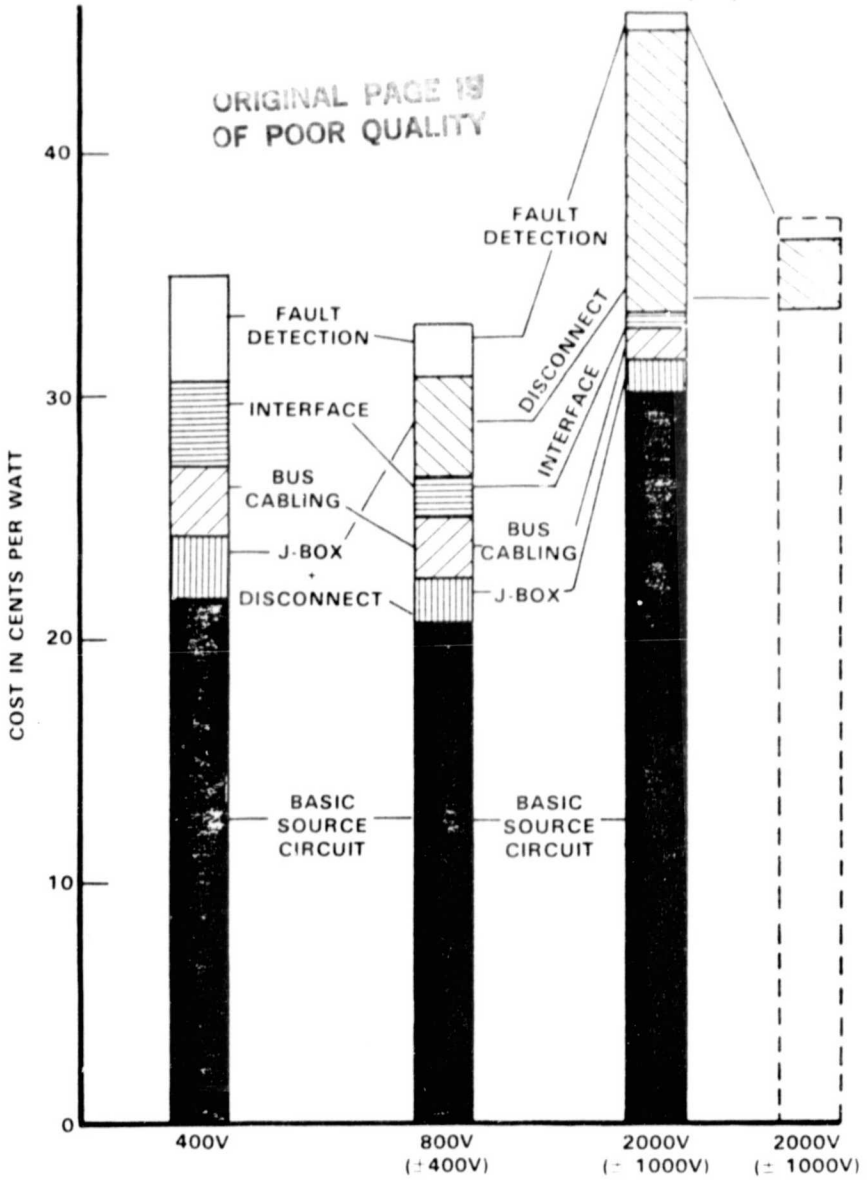
Cost Element Contributions vs Source Circuit Voltage: 15-Ampere Circuits



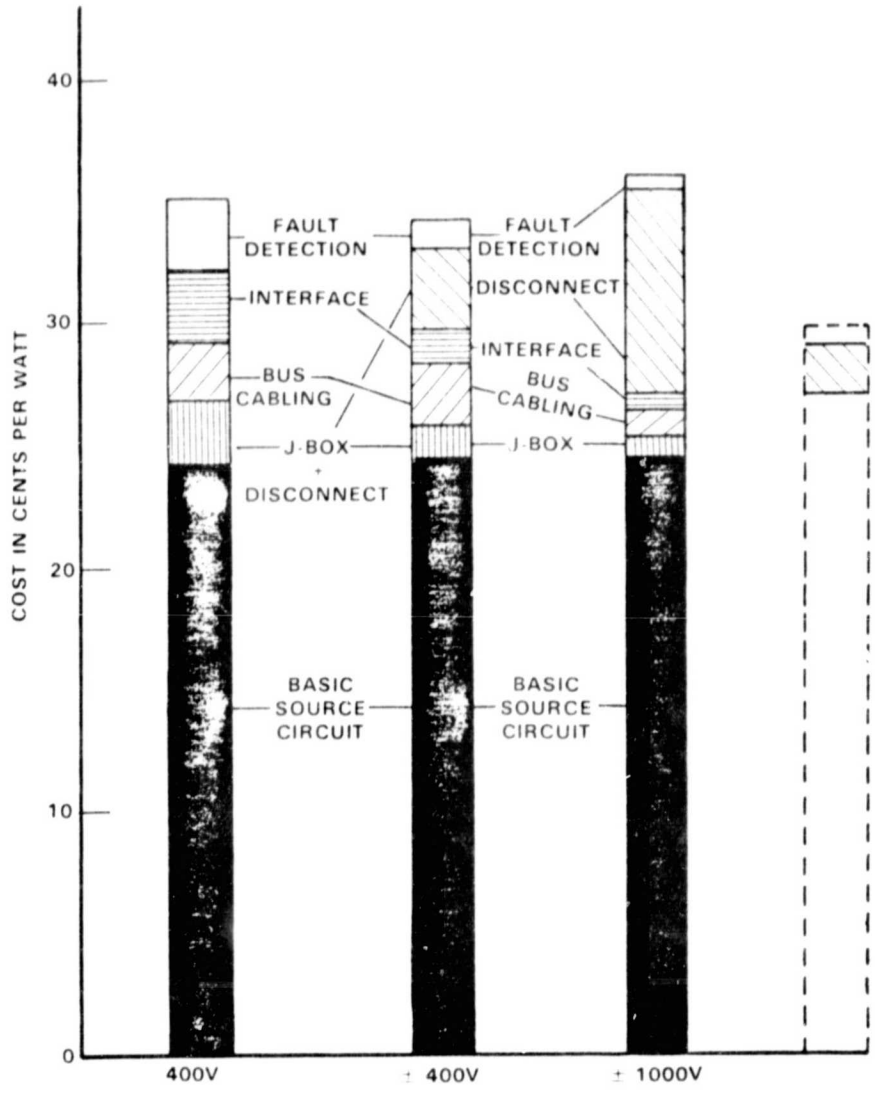
Cost Element Contributions vs Source Circuit Voltage: 30-Ampere Circuits



Relative Cost Element Contribution vs Source Circuit Voltage for 45-Ampere Source Circuits



Relative Cost Element Contribution vs Source Circuit Voltage for 60-Ampere Source Circuits



Conclusions

- HIGH VOLTAGE LOW-CURRENT CIRCUITS NOT ECONOMICAL
- AT HIGHER CURRENTS HIGH AND LOW VOLTAGE CIRCUIT COSTS APPROACH EACH OTHER
- HIGH VOLTAGE CIRCUITS NOT LIKELY TO OFFER NEAR TERM ADVANTAGE
- DEVELOPMENTAL WORK/MANUFACTURER STIMULATION NEEDED TO DEVELOP LOW-COST HIGH VOLTAGE HARDWARE

SESSION II

INSULATION DESIGN FOR HIGH SYSTEM VOLTAGE

J.C. Arnett, Chairman

COMMIT TO P.95

SESSION II

INSULATION DESIGN FOR HIGH SYSTEM VOLTAGES

Chairman: J.C. Arnett, ARCO Solar Industries

SUMMARY

The second session of the Forum undertook a review and discussion of recent experience and progress in the area of high-voltage design for insulating materials and configurations in large-area arrays. The focus on this subject is considered to be appropriate and timely in light of the trend toward selection of higher system operating voltages in large grid-connected systems.

Historically, in considering high-voltage design for PV, it is clear that during the early stages of the National PV Program (Blocks I and II), the use of a 500-volt hi-pot was adequate for evaluation of modules designed for the stand-alone, battery-connected applications typically being deployed. As intermediate-load applications, including the PRDA experiments, came along, the industry raised its voltage design goals to be consistent with the 150-volt to 200-volt system operating conditions, where it had generally stayed until recently. Those system voltages resulted through application of the old transformer rule: typically, twice the system voltage plus 1000 volts, in hi-pot tests in the order of 1500 to 2000 volts. With the advent of megawatt-scale utility installations, and the economies that have been suggested that are associated with higher operating voltages (especially in the cost of array wiring and PCUs), test voltages to determine the as-produced quality of panels have moved up to 3000 to 4000 volts. With that progression in mind, the presenters in this session undertook a discussion of several aspects of high-voltage design for large-area PV arrays.

The session covered the general design goals and approaches applicable to insulation systems; what influence leakage currents and breakdown incidence might have on array operation and lifetime; and the causes of high-voltage breakdown from an empirical and analytical standpoint.

The first presentation, by R.G. Ross, Jr., JPL, identified the technical requirements for achieving adequate high-voltage design, and recommended long-term high-voltage reliability goals. Three basic types of concerns associated with voltage breakdown resistance were described: (1) prevention of worst-case voltage breakdown due to system Voc at high insolations and low temperatures or transient overvoltages; (2) reduction of leakage currents below ground-fault trip levels, and (3) long-term leakage-current effects on array reliability that have O&M implications.

T.D. Harrison of Sandia National Laboratories then described experiences to date in voltage breakdown failures in the PRDA experiments. Although no problems had been identified as directly related to module breakdown at those sites, a number of system operating trips had been experienced due to

ground-fault interrupts. The potential for workmanship failures in modules was described with respect to experience on one of the Sandia 30-kW arrays.

This presentation led to a discussion of array ground-fault detection methods and grounding philosophy for utility systems.

In contrast with the field experience, J.S. Griffith of JPL related the results of high-voltage testing during the block qualification programs. An important finding was that although module designs can be provided that meet electrical isolation requirements, assuming one or more iterations of the design process, a new problem of maintaining grounding continuity of all exposed frame surfaces is typically not well addressed.

The final part of the session consisted of two talks by G.R. Mon and E.F. Cuddihy, both of JPL, that dealt with the theory and mechanisms of voltage-breakdown phenomena.

Mon identified three types of insulation failures: intrinsic failure due to uniform bulk stress of the encapsulant, failure due to a localized flaw creating a high stress zone, and, failure due to long-term electrochemical corrosion that changes material properties. He described investigations at JPL that are concentrating on the last type.

In the final talk of the session, Cuddihy described a new theoretical description of the breakdown process that is analogous to mechanical proportional limits, which has the potential of providing an improved high-voltage design methodology.

In summary, the high-voltage design session defined system requirements, related the current status of field and laboratory test experience with breakdown, and described the current R&D directions supporting improved design capabilities for high-voltage PV arrays.

The conclusions of the work described are that (1) additional experience with actual systems operating at higher voltage are needed, (2) more research on time dependent variables is required, and (3) guidelines for setting leakage current allowables and maximum systems voltages must be developed.

ELECTRICAL INSULATION DESIGN REQUIREMENTS AND RELIABILITY GOALS

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The solar cells in a photovoltaic module must be electrically isolated from module exterior surfaces to satisfy a variety of safety and operating considerations. To judge the performance and reliability of the insulation system, it is necessary to understand the technical requirements and reliability goals.

Technical requirements involve principally the capability of withstanding the differential voltage from the solar cells (maximum system voltage, plus and minus) to the module frame (which is tied to earth ground potential to eliminate possible shock hazards). The maximum system voltage includes consideration of maximum open-circuit array voltages achieved under low-temperature ($0^{o}C$), high-irradiance ($100\ mW/cm^2$) conditions, as well as transient overvoltages due to, for example, system feedback of lightning transients. The latter is bounded by the characteristics of incorporated voltage-limiting devices such as MOVs.

A second important requirement is the limiting of array leakage currents under normal operating conditions. This requirement is driven by the demands of array ground-fault detection systems, which require that "normal" leakage-current levels be below the threshold trip level set to note a voltage breakdown. The required leakage level is a function of the number of modules per detection system and the system operating voltage. A second important leakage current consideration is that of controlling current-dependent electrochemical corrosion between the cell string and the module frame.

Because voltage breakdown tends to occur at insulation flaws and sites of stress concentration, voltage withstand level is found to vary widely from module to module. Screening out of manufacturing defects is usually accomplished by testing each module at a hi-pot voltage level of twice the worst-case system voltage plus 1000 volts. Passing this hi-pot test is the key module requirement on initial voltage-withstand performance.

Long-term field performance must additionally include the expected degradation of the insulation materials and construction through the action of weathering and voltage-stress exposure. Delamination, cracking and electrochemical corrosion are important degradation mechanisms. Electrochemical corrosion is caused by array leakage currents, which lead to the migration of corrosion products between the solar cells and module frame. With time the products bridge the insulation with a conductive path, which results in a short to the grounded module frame. The level of corrosion is proportional to the total level (amp-hours) of ionic leakage current as influenced by module temperature and humidity conditions; electronic leakage current associated with the conduction of electrons does not lead to corrosion.

Allowable levels of long-term field failures are generally established by economic considerations of allowable O&M costs. For modules where breakdown is largely constrained to occur between the cell circuit and the module peripheral frame, it is useful to address the allowable number of breakdowns per year per mile of module periphery. A nominal value currently being used is no more than one breakdown per 10 miles per year. This low level corresponds to one breakdown every two months for a one-megawatt photovoltaic plant.

ELECTRICAL INSULATION DESIGN REQUIREMENTS AND RELIABILITY GOALS

JET PROPULSION LABORATORY

R.G. Ross, Jr.

Insulation Design Requirements

- **Prevent voltage breakdown from cell strings to grounded components**
  - **Worst-case system voltage (100 mW/cm^2, 0°C)**
  - **Worst-case transient overvoltage (MOVs)**
- **Maintain leakage currents below trip level of ground-fault detectors**
  - **Dependent on array area served by detector**
  - **Dependent on temperature and humidity**
- **Maintain failure levels consistent with allowable O&M costs**

Voltage Breakdown Statistical Considerations

- **Allowable O&M costs require statistically low levels of breakdown**
- **Voltage withstand is found to vary widely from module to module**
- **Prudent design utilizes conservative material properties and thoughtful consideration of stress concentration, flaw and environmental aging effects**
- **100% proof testing (hi-pot test at twice system voltage plus 1000 volts) is used to screen out manufacturing defects**

Voltage Breakdown Requirements

- **Short-term module proof-test yield**
- **Long-term dc system voltage endurance**
  - **Resistive voltage division**
  - **Geometric stress concentration**
  - **Long-term degradation effects**
    - **Mechanical integrity (delamination, cracking)**
    - **Intrinsic voltage withstand**
    - **Changes in relative resistances**
    - **Electrochemical effects**
- **Transient ac voltage endurance**
  - **Capacitive voltage division**
  - **Geometric stress concentration**
  - **Environmental aging effects**
    - **Intrinsic voltage withstand**
    - **Changes in relative capacitances**

Strawman Degradation Allocations: 30-Year-Life Advanced Technology, 1982 $

Type of Degradation	Program Plan Allocation	Revised Allocation	Specific Mechanism	Mechanism Allocation
Fixed Drop in Power	8%	4%	Soiling Mismatch	3% 1%
Constant Degradation Rate	0.65%* per year	0.45% per year	Cell open circuit Cell corrosion Yellowing	0.00001 per year 0.2% per year 0.2% per year
Constant O&M Rate	$2.28/m^2 per year	$1.07/m^2 per year	Voltage breakdown Glass breakage Mod. open circuits Structures upkeep Electrical upkeep Grounds upkeep	0.1/mile/year† 0.002 per year† 0.002 per year† $200/acre/year□ $500/acre/year□ $200/acre/year□

*5% average loss over 30 years at 12½% discount rate
†At $140 per replacement of 1.5 m^2 module
□At 1350 m^2 of array per acre (1:3 packing)

Array Leakage Current Considerations

Total leakage current must be below ground-fault detector trip level

- **Electronic currents**
  - **Conduction of electrons between cell string and grounded components**
- **Ionic currents**
  - **Transport of (metallic) ions between cell string and grounded components**
  - **Electrolytic corrosion (plating)**
  - **Polarity dependent**
  - **Temperature-humidity development**

Allowable Array Leakage Current vs Ground-Fault Detector Design

kW * Per Detector	m^2 Per Detector	Maximum Array Leakage ($\mu A/m^2$)		
1	10	500	5000	–
10	100	50	500	5000
100	1000	5	50	500
1000	10000	0.5	5	50
Detector Trip Current		5 ma	50 ma	500 ma
Shock Risk		Low	Mod	High
Fire (Arc) Risk		Nil	Low	Mod

*10% Efficiency at 100 mW/cm^2

Summary

- **Voltage breakdown requirements established by allowable yield losses and field O&M costs**

- **Leakage current requirements established by ground-fault detector trip level and allowable electrochemical corrosion**

FIELD EXPERIENCE WITH VOLTAGE BREAKDOWN IN PHOTOVOLTAIC ARRAYS

SANDIA NATIONAL LABORATORIES

T.D. Harrison

NEW MEXICO ENGINEERING INSTITUTE

J.P. Fernandez

Purpose

The purpose of this paper is to reveal the good news about voltage breakdown experience on all intermediate, flat-plate, PRDA 38 arrays in the field.

Definitions

A PV array is defined as an assembly that consists of PV modules, a structure to support the modules, wiring that carries electrical power generated by the modules to a load, and wiring that grounds the structure. Voltage breakdown is defined as irreversible damage to an electrical insulator that establishes an unwanted path through which electrical energy is dissipated.

PV System Studied

Information about voltage breakdown in the field was obtained from logbooks, site event reports, interviews with operators and visits to the PV arrays by Sandia personnel. The arrays studied are listed in Table 1.

Table 1. Field Experience with Voltage Breakdown in PV Arrays

Location	Number of of Modules	Manufacturer of Modules	Normal Operating Voltage	Start Date	Number of Breakdowns
Beverly High School	3200	Solar Power	260	April 1981	0
Lovington Square	3360	Solar Power	260	April 1981	0
Newman Power Station	576	Solar Power	134	January 1981	0
Oklahoma Center	1512	Solarex	350	February 1982	0

Results

Table 1 indicates that voltage breakdown experience with all flat-plate, PRDA 38 arrays in the field has been good. The paper could stop here except for the fact that there have been reports of voltage breakdown along with numerous interruptions of array operation that could be interpreted as being caused by voltage breakdown.

Reported Voltage Breakdown

There are two arrays that have experienced voltage breakdown problems. One is the 35-kW array at San Bernardino (not a PRDA project), which comprises 1152 Solarex modules (single crystal cells) and operates at a nominal 250 V. In April 1982, which was early in the life of the array, there were numerous ground-fault interruptions. An investigation revealed many of these to be caused by a burr on a tab piercing a mica insulator. The tab was part of an assembly that held a bypass diode in a junction box attached to the module. The manufacturer replaced all washers with ones that had been deburred, and the problem disappeared. The exact number of breakdowns is not known. They were numerous.

The second array to experience voltage breakdown is the 30-kW Battelle array in Sandia's Photovoltaic Advanced Systems Test Facility (PASTF). It comprises 480 Solec modules and operates at a nominal 400 V. There have been three voltage breakdown events. Because all three were similar, only one will be discussed here. In January 1983, immediately after the array was turned on, operators detected current leakage to ground. Visual inspection revealed no cause. They continued to operate the array with a light load until there was visual and audible arcing. Upon inspection of the field, they found a module with cracked glass and a burned area in the lower left corner. There were approximately 150 V on this module.

The construction of the module was such that a metal frame overlapped the bus bar. Both the Jet Propulsion Laboratory (JPL) and Sandia agree that delamination of the insulation occurred and opened an electrical path from the bus to the frame.[1] This problem is also judged to be the result of poor process control by the manufacturer.

This particular array was constructed to test hypotheses for the reduction of balance of system costs. The modules are believed to have been trimmed in size to fit into the array. In some places, there was too much trimming. The modules were not qualified under any JPL criteria.

Voltage breakdowns in both the above arrays were caused by poor quality control practices by the two manufacturers.

Problems with Connections and Pigtails

Early in the lives of five arrays, problems developed with connections and pigtails.

Solar Power originally designed its 36-cell module with only 1 bypass diode. At the suggestion of JPL, a second diode was added so that in case of a problem, only 18 cells would be lost. Both diodes were installed in the box that housed the connection for the pigtail (Figure 1). A number of early module failures led to a decision by Solar Power to rework the connections, under warranty, in the field. After the rework, it was necessary to replace 11 modules at Beverly, 18 at Lovington, and 19 at Newman. The reason for the replacements was loss of power from the module and not voltage breakdown. The need for the rework and replacements was poor process control on the part of the manufacturer.

It has been necessary to replace five modules at the Oklahoma Center for Sciences and Arts (OCSA) project because of no power output. There was no

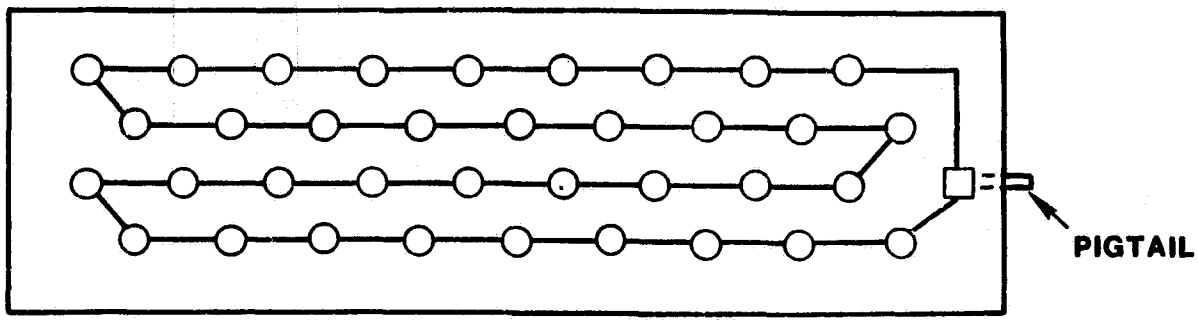

Figure 1. Wiring Configuration for Solar Power Module G12-361-CT

feedback from Solarex, but available evidence points to connector or pigtail problems as being the cause of failure.

At San Bernardino and at Oklahoma City, water in the connectors was a problem. The water, not detectable voltage breakdown, caused loss of power. It was a problem that was correctable in the field.

Problems with Power Interruptions

All intermediate PV systems, including concentrators, have experienced numerous power interruptions, which include many ground-fault interruptions. There is no evidence that any of these interruptions are associated with voltage breakdown in the arrays. In fact, there are four pieces of evidence that indicate that they are not associated with voltage breakdown in the array.

First, frequent walkthrough inspection revealed no visual evidence of voltage breakdown. Second, voltage breakdown is usually aggravated with time. The incidence of ground-fault interruptions has decreased, helped by desensitizing the interrupter. Third, regression analyses prepared by Sandia and New Mexico Solar Energy Institute reveal no statistically significant degradation of power with respect to time. Voltage breakdowns in the array would allow dissipation of power before it reaches the load. Fourth, there is a small sample of incidents that show causes of ground-fault interruptions that are definitely not related to the array.[2]

Conclusions

There has been only one cause of voltage breakdown in the five PV arrays in the field. At San Bernardino, burrs on washers pierced insulation. This problem was in the connector and not in the module per se and was caused by poor quality control. Voltage breakdowns did occur in the modules in the Battelle array at Sandia. It is significant that the modules had not been qualified by JPL and were of secondary importance to the objective for constructing the array. There have been numerous array interruptions that could be associated with voltage breakdown. However, there is an increasing body of circumstantial evidence that points to causes other than voltage breakdown for the interruptions. The voltage breakdown problems that have been encountered were the fault of poor process and/or quality control by the manufacturer.

References

1. S. Johnson and A. Shumka, "Part Failure Analysis Report No. 3061," (Pasadena, CA: Jet Propulsion Laboratory, March 1983).

2. Field Service Reports, Lovington, Beverly, CDC, MCC, MT Laguna," (Irvine, CA: Helionetics Inc., no date).

HIPOT AND CONTINUITY QUALIFICATION TEST EXPERIENCE

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Hipot (high voltage potential) and module frame continuity tests are important parts of determining the suitability of solar modules for deployment into large arrays for electrical power production. Since field arrays operate at hundreds of volts above (or below) ground potential at some point in the field, it is necessary to assure adequate voltage isolation of the solar cell circuits. This subject is discussed in this presentation as outlined in Figure 1. The discussion is based on test procedures used at the Jet Propulsion Laboratory and as given in JPL Reports 5101-161 and -162.

The purpose of hipot and continuity testing (Figure 2) is to reveal potentially hazardous voltage conditions of modules before field installation. It also reveals leakage currents that potentially may result in significant loss of power or cause ground fault system problems. The tests reveal first, the current leakage potential and second, how the leakage or hazardous voltages will be distributed. Notice the word "potentially" is used in all cases. If the hipot current leakage is a few microamperes too high or the frame continuity a few milliohms too high, one can't say that the module would be an immediate catastrophe if mounted in an array. However, the tests generally do indicate any weaknesses in the design that are potentially hazardous and need to be corrected.

The hipot test procedure described in Figure 3 will be discussed first. Figure 4 shows typical equipment used. The Hipotronics HD115 tester supplies the needed voltage and measures the current leakage. The polyurethane boards shown in Figure 4 help isolate the lead wires and reduce any spurious current leakage external to the module. The dial gauges have been found to be of insufficient accuracy for a pass/fail tester and frequent calibrations are done using the equipment in Figures 5 and 6.

A closely related measurement is performed during the environmental exposures of modules to temperature, humidity, and mechanical cycling tests. Figure 7 shows the equipment used to monitor the cell string isolation from ground during mechanical cycling. Circuit resistance to ground should not change appreciably during the environmental stresses.

Several problems and questions of interpretation of test procedures arise during hipot testing as listed in Figure 8. It is becoming more prevalent to ship glass laminates without metal frames. Frames of the recommended design should be fabricated and used if the

modules are to be hipot test qualified for deployment. If modules have unattached metal components, bonding them together will permit testing. However, grounding of all separate metal elements in the field will be necessary. These and other problems are shown in Figures 9 to 13.

The zinc-based feedthrough connector shown in Figure 9 and at the left side of Figure 10 had very low current leakage (0.6 μ A) but corroded badly in the Block V humidity-freeze test. The module manufacturer substituted the stainless feedthrough shown at the right on Figure 10 containing what appeared to be the same internal rubber pottant. However, the latter passed 60 μ A of current resulting in hipot test failure in the connector alone. A minor change in the additives in the rubber caused the excessive leakage.

Figure 11 shows the back side of a simulated roof section holding a module laminate. The galvanized drip troughs around the glass laminate shown in Figures 11 and 12 were unconnected and required bonding wires (Figure 11). The module failed hipot because the black rubber gasket around the laminate was slightly conductive.

Polyvinyl butyral is a popular encapsulant and generally has adequate dielectric strength at room temperature to pass the hipot test. However, leakage increases by about 400 times at hot day field temperatures (Figure 13). If high ground fault currents might be a problem in a particular large array, modules should undergo leakage tests at elevated temperatures.

The Biddle corona (partial discharge) tester shown in Figure 14 is very useful for diagnosis of hipot failure.

The continuity test used at JPL is discussed next with illustrations in Figures 15 through 22. As shown in Figure 15 the JPL Block IV tests required a continuity test between metal components of the module frame with a 50 milliohm upper limit. Block V required a continuity test but without a stated limit. At first the same value was used as had been used for Block IV: 50 milliohms. Recently, a high current continuity test was adopted. Current is passed through the module frame at a level of twice the short circuit current. Maximum voltage drop permissible is 1 volt from the beginning of the test through a two minute hold period. This high current test was based on an interim report of a JPL-Underwriters Lab study. The final report, UL 1703, is the same test except it calls for only a 1/2 volt drop.

Figure 16 shows the relationship between these tests. The module milliohm resistance is plotted against module short circuit curent. The milliohmmeter test used in Block IV and early Block V was independent of module current. The more recent tests appear as slanting straight lines on log paper. At high module currents the old test was easier to pass and vice versa for low module currents. This comparison assumes that high current will not burn out or weld together point contacts at the joints and that the basic frame resistance remains unchanged.

Figure 17 shows a module with a typical 4-element metal frame. The ground lug shown is at the lower right. If there is none provided, a site is chosen arbitrarily. Any pair of sides chosen for the continuity test has two possible current paths, clockwise and counterclockwise. Thus, a failure of two or more joints must occur to be detected. The continuity test must include three pairs of sides such as 1&2, 1&3, and 1&4.

Figure 18 shows a continuity test setup using a Simpson Model 1699 milliohmmeter. Sometimes the resistance is greater than the instrument's 50Ω full scale limit. A Fluke 8060A multimeter shown at the left is used for resistance levels above 50 Ω. Most of the testing done in the past was done using the milliohmmeter and the data presented here was all obtained that way. In the photograph this module shows good continuity with approximately zero resistance. However, in Figure 19 modest forces are being applied to the corner resulting in a reading on the next meter scale of over 100 milliohms, a continuity test failure. At JPL the test is ordinarily run with and without "handling forces" applied.

Figure 20 shows the test setup for the newer high current continuity test. The power supply provides current to the module, generally through the precision shunt shown here. The dial gauges are only coarse indicators but now, at low voltage and high current, digital voltmeters are used to give precise values.

Some of the problems encountered in continuity testing are given in Figure 21. The first noted is non-conductive metal surfaces, primarily anodized aluminum. These types of surfaces must be ground off to expose base metal. The test lead battery clamps at the attachment points may have high contact resistance resulting in errors. (At the suggestion of a questioner at the Workshop, this error can be eliminated by moving the DVM voltage sensor leads from the battery clips to the module frame). Obviously, no continuity test can be run unless the metal frame elements are connected. In the field, all of these separate metal elements should be grounded. Again, the laboratory environment can be a problem. Temperature can change the physical position of the metal elements and change the resistance.

Figure 22 shows a portion of a two-piece, U-shaped metal frame joined by a riveted joint at each end of the module. The rivets seemed to be well installed and tight. Behind the flange is an ordinary inspection mirror showing the small metal clip that serves to hold the two pieces together. Unbelievably, these two parallel joints showed a combined resistance of over 200 megohms.

The results of the testing are shown in Figures 23-25. For the approximately 250 individual modules in Figure 23, initially 10 and 12% failed hipot and continuity, respectively. All of these didn't complete environmental tests so there is a smaller population for final tests. 19 and 29% failed final tests, respectively. For the data on sets of modules, one failure per set is considered a failure of the whole set.

For the sets there was initially a 26% failure in hipot and 9% in continuity. After environmental testing, these failures went to 42%. The last two columns take the most critical viewpoint. If we use the criterion that any failure of hipot or continuity, either before or after environmental exposure, causes the set to fail, there was a 73 percent failure rate. In spite of these gloomy statistics, most of these problems could be easily fixed. A little more care in fabrication, keeping the busbars and other conductors a little farther from the frames, better metal joining, etc. would lower the failure rates significantly.

Figure 24 shows the voltages at failure of individual modules. Initially, the clear bars show that relatively few modules failed until the 1000-2000 V range was reached. Over half of all modules that failed did so in this range below 2000 V. After environmental tests the voltage at failure rises with none failing below 500 V but a considerable number getting to 3000 V only to fail in less than 1 minute.

Figure 25 shows the resistance in ohms at failure. Initially, there were more failures at over one ohm than at less than one ohm. After environmental testing the situation was reversed. The right side of Figure 25 is distorted. Initially, high resistance was read simply as "greater than 50 Ω". Later, the digital ohmmeter was used showing that most of these "greater than 50 ohms" were probably "greater than 10 megohms." Therefore, these two bars should be considered in the same group. Notice there are no readings between 10 and 50 ohms and probably, nothing between 10 ohms and several megohms.

In summary, the hipot and continuity tests have clearly defined limits for pass-fail in contrast to the visual inspection where limits are somewhat indefinite or non-existent. All of these tests result in many failed modules. In fact, a majority of the module designs fail if the criterion of one failure per set of eight is used. A majority of the failures can be prevented by simple changes in design or in module processing.

HIPOT AND CONTINUITY QUALIFICATION TEST EXPERIENCE

JET PROPULSION LABORATORY

John S. Griffith

Figure 1. Contents

- PURPOSE OF HIPOT AND CONTINUITY TESTING
- HIPOT TESTING - EQUIPMENT, PROCEDURES, PROBLEMS
- CONTINUITY TESTING - EQUIPMENT, PROCEDURES, PROBLEMS
  - OLD AND NEW PROCEDURES - MILLIOHMMETER VS HIGH CURRENT
- RESULTS OF RECENT TESTS

Figure 2. Purpose of Hipot and Continuity Testing

- REVEAL POTENTIALLY HAZARDOUS VOLTAGE CONDITIONS OF INSTALLED MODULES
- REVEAL LEAKAGE CURRENTS THAT POTENTIALLY MAY RESULT IN SIGNIFICANT LOSS OF POWER OR CAUSE GROUND FAULT SYSTEM PROBLEMS
- REVEAL BY THESE TWO TESTS FIRST, THE CURRENT LEAKAGE POTENTIAL AND SECOND, HOW THE LEAKAGE OR VOLTAGES WILL BE DISTRIBUTED.

Figure 3. Hipot Test

- APPLY DC VOLTAGE AT A RATE NOT TO EXCEED 500 V/SEC TO 3000V, BOTH POLARITIES, BETWEEN THE MODULE CELL STRING AND THE METAL FRAME AND HOLD FOR ONE MINUTE.
- LEAKAGE IS LIMITED TO 50 μA WITH NO SIGNS OF ARCING OR FLASHOVER.

Figure 4. Hipot Test Setup

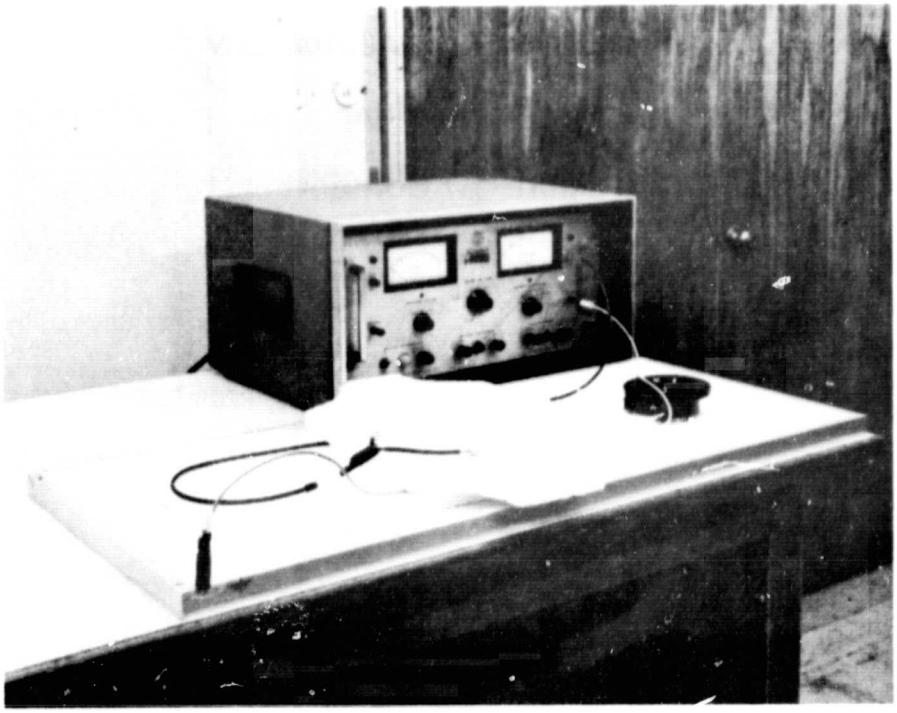


Figure 5. Voltage Dial Calibration

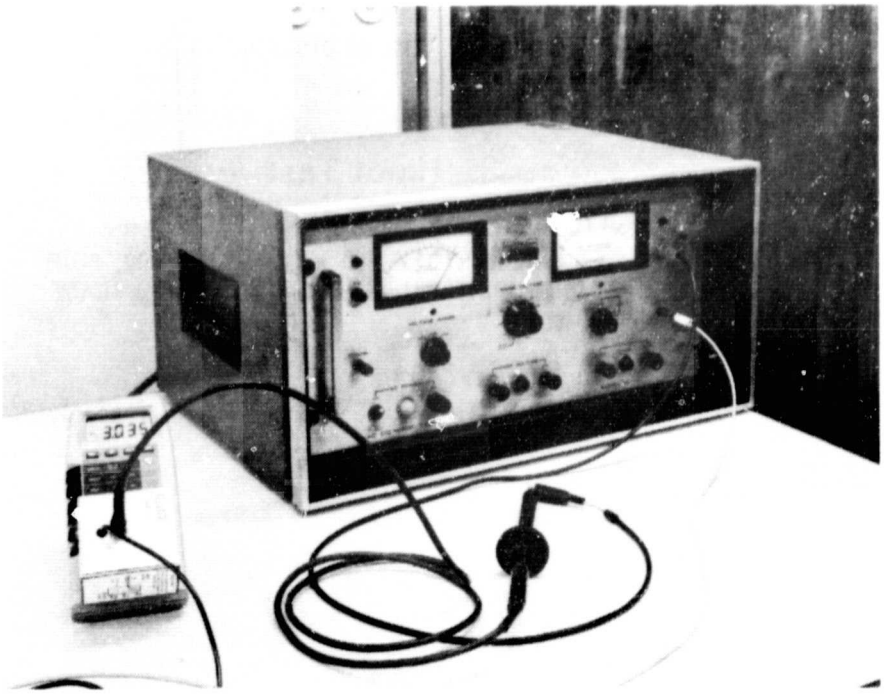


Figure 6. Current Dial Calibration

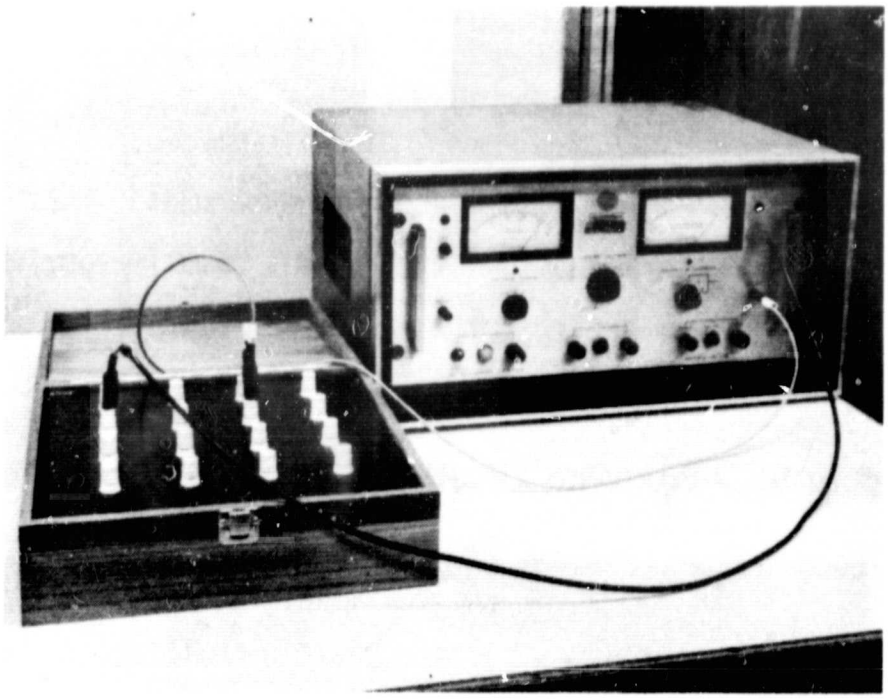


Figure 7. Voltage Isolation Monitoring During Test

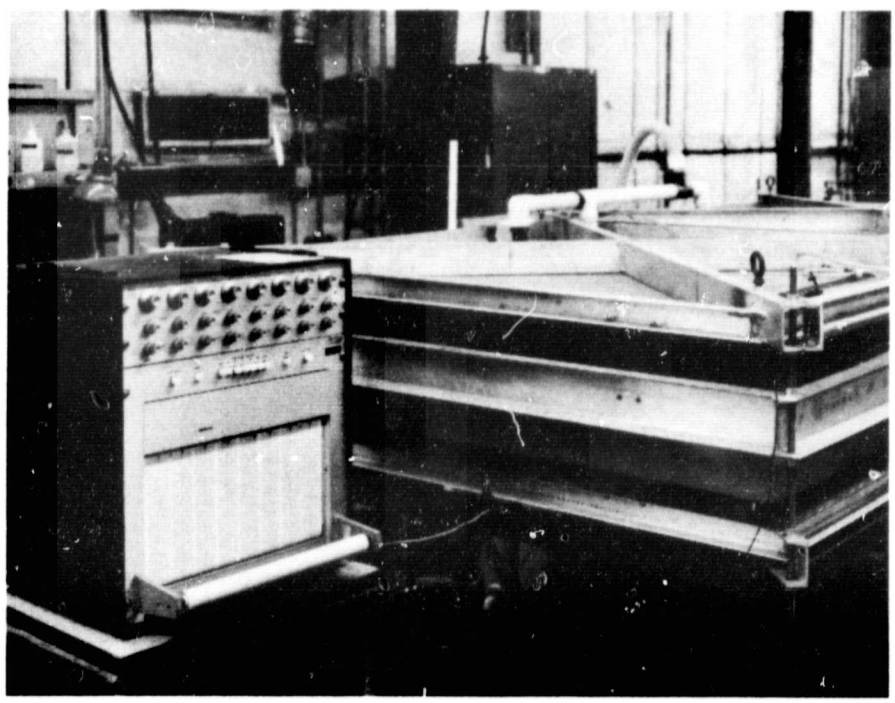


Figure 8. Hipot Testing Problems

- NO METAL FRAMES ON THE MODULE
  - NO TEST?
  - BUILD A FRAME IF THERE IS A RECOMMENDED DESIGN
- MODULE HAS METAL COMPONENTS BUT THEY ARE NOT ATTACHED
- ELECTRICALLY CONDUCTIVE ELASTOMERS – GASKETS, CONNECTOR POTTANTS
- LABORATORY AMBIENT ENVIRONMENT – TEMPERATURE, HUMIDITY, HANDLING FORCES

Figure 9. J-Box With Zinc-Based Connector Feedthrough

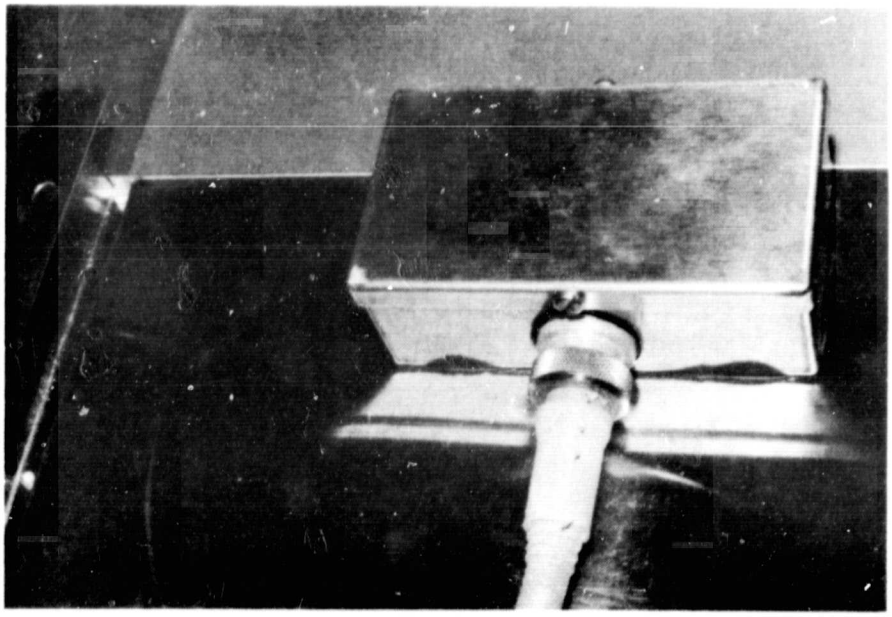


Figure 10. Zinc Alloy and Stainless Feedthroughs

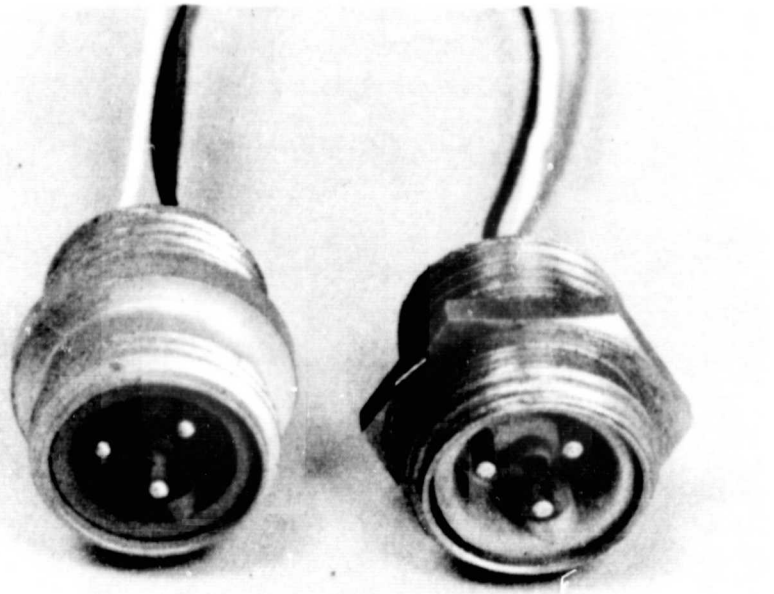


Figure 11. Module in Simulated Roof Section

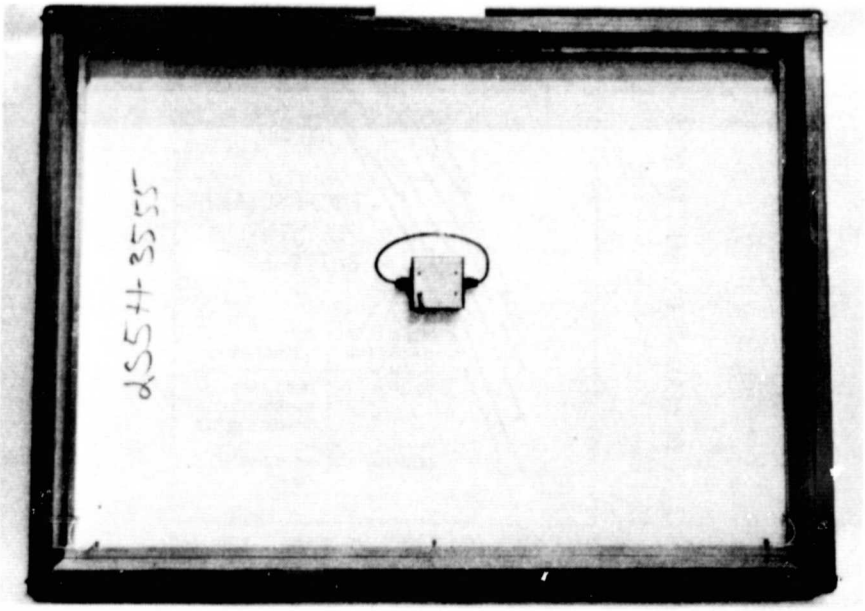


Figure 12. Roof Drip Troughs and Module Gasket

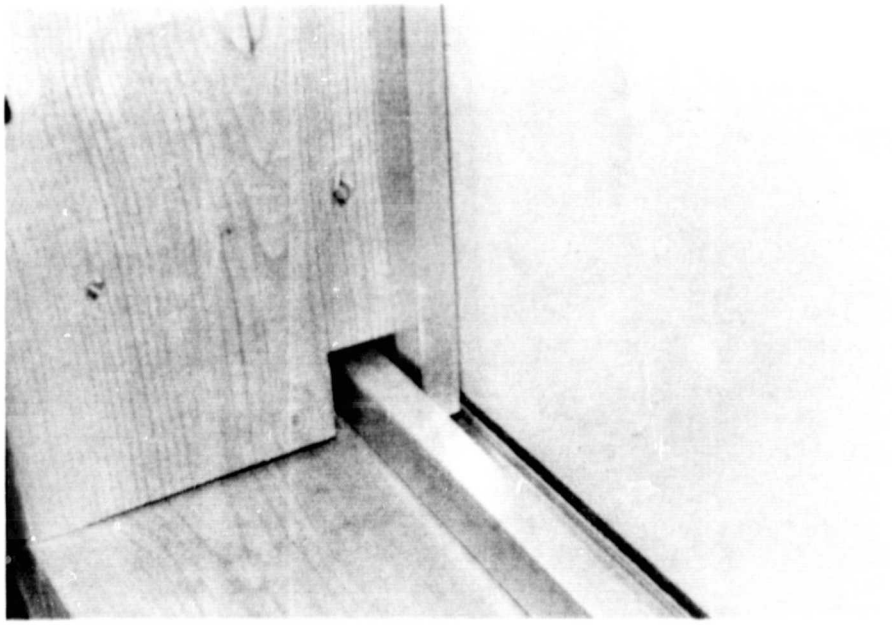


Figure 13. Dc Leakage Current vs Temperature and Voltage

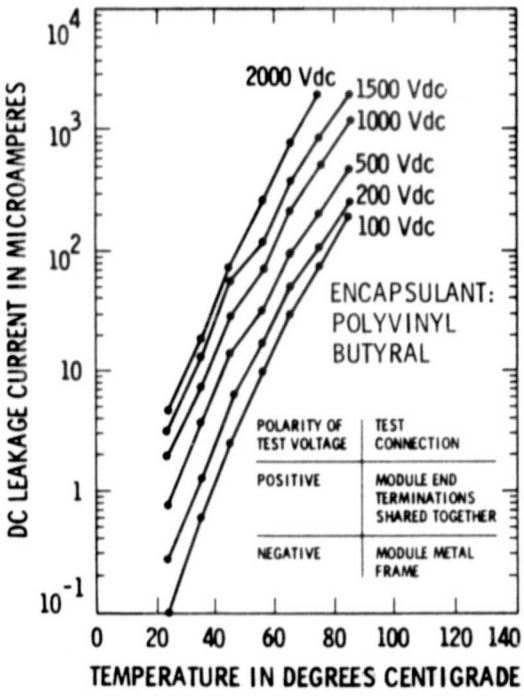


Figure 14. Biddle Corona Tester

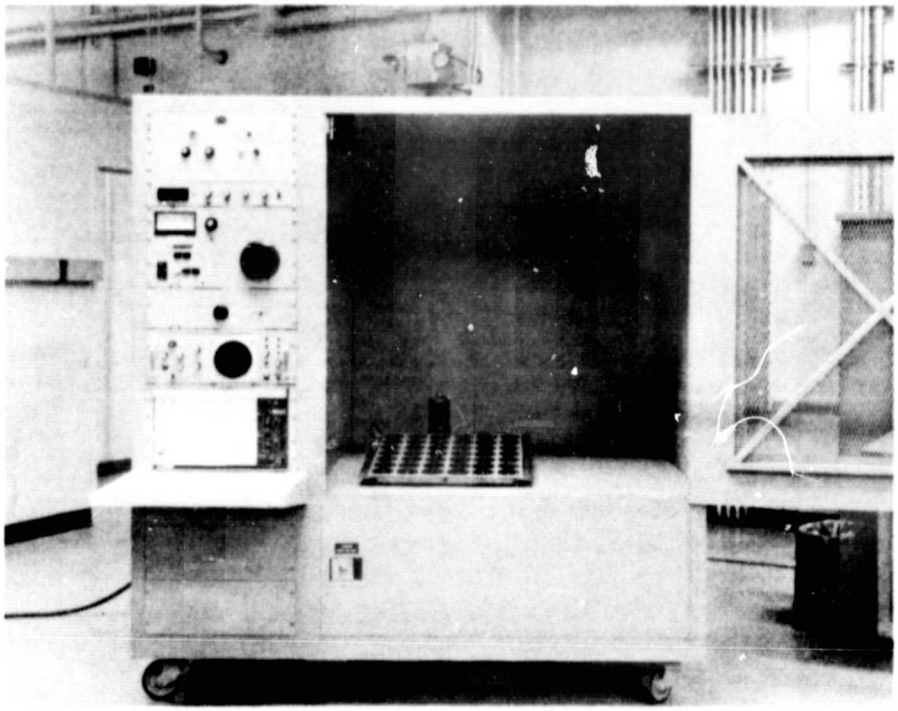


Figure 15. Continuity Test

- BLOCK IV: 50 MILLIOHMS MAX RESISTANCE BETWEEN METAL COMPONENTS OF THE MODULE FRAME.
- BLOCK V: CONTINUITY TEST WAS REQUIRED BUT THE TEST VALUES WERE UNDEFINED UNTIL RECENTLY.
  - EARLY ON – SAME LIMITS WERE USED AS FOR BLOCK IV: 50 MILLIOHMS.
  - LATELY – APPLY CURRENT FROM ZERO TO TWICE THE SHORT CIRCUIT CURRENT IN FIVE SECONDS BETWEEN GROUND AND THE OTHER METAL COMPONENTS AND HOLD FOR TWO MINUTES. MAXIMUM VOLTAGE DROP IS ONE VOLT.
  - UL 1703 – ALSO TWICE THE SHORT CIRCUIT CURRENT BUT MAXIMUM VOLTAGE DROP ALLOWED IS 1/2 VOLT.

Figure 16. Continuity Test: Various Test Limits

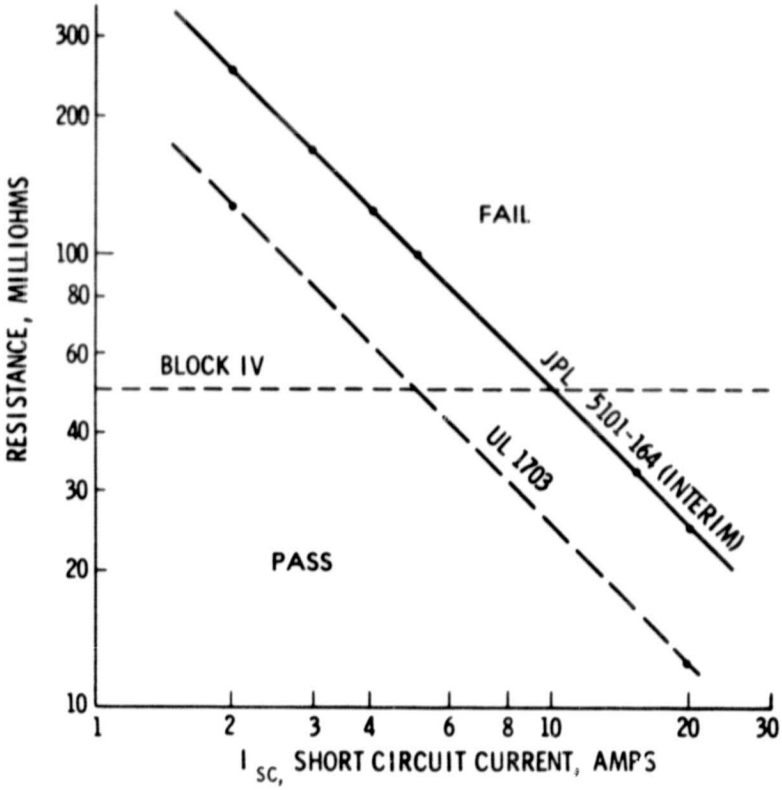
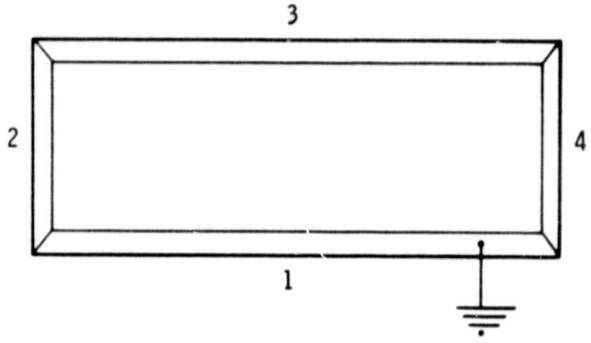


Figure 17. Continuity Test: Four-Component Metal Frame



- FAILURE MEANS 2 OR MORE JOINTS HAVE HIGH RESISTANCE
- TEST 3 POSITIONS: SIDES 1-2, 1-3, 1-4

Figure 18. Continuity Test Setup

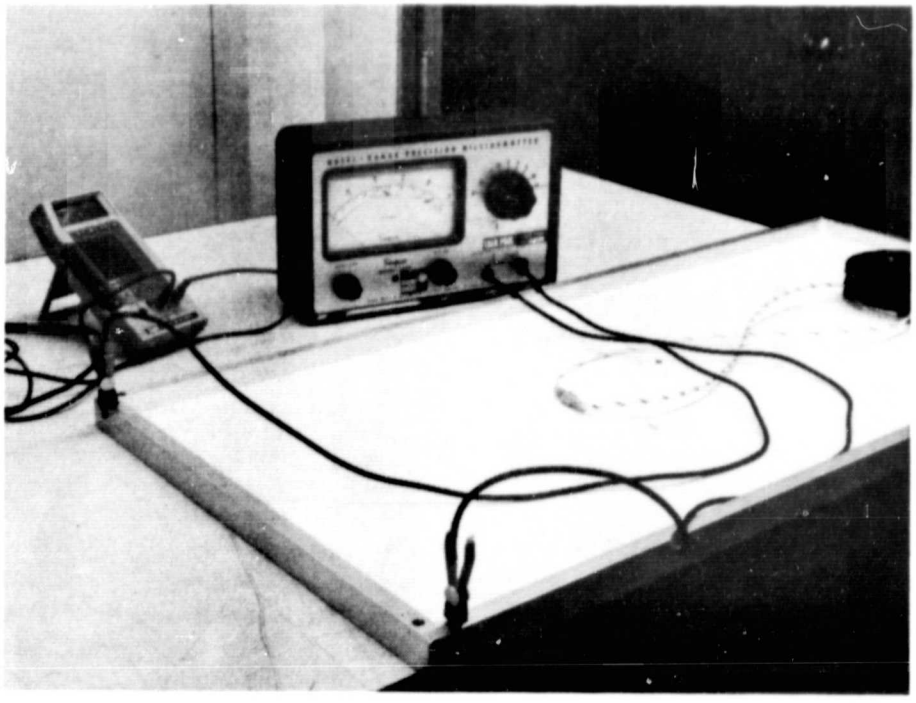


Figure 19. Applying Moderate Forces to Corner Joint

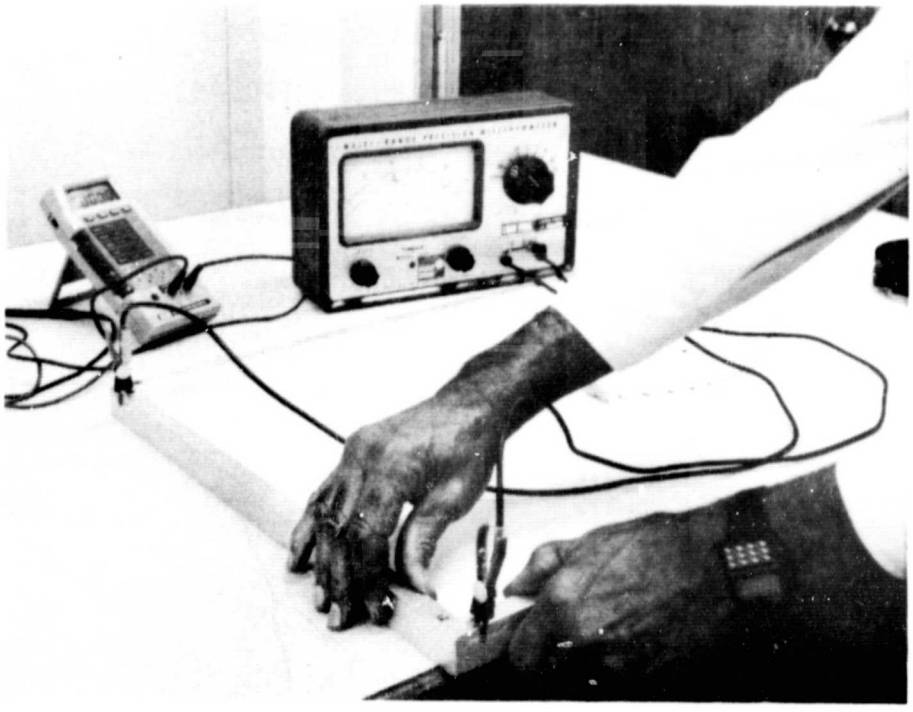


Figure 20. High-Current Continuity Test

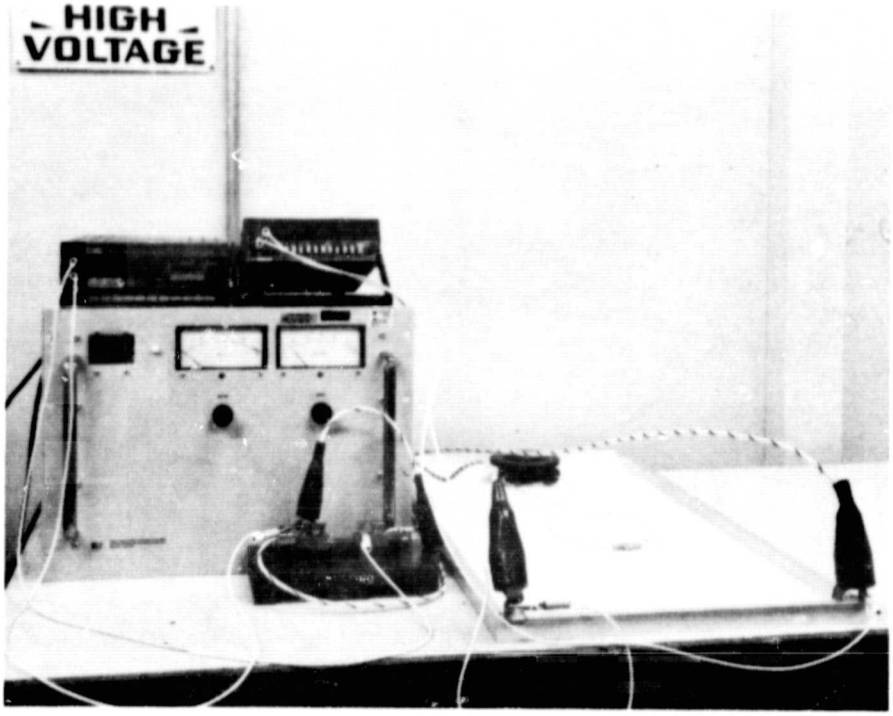


Figure 21. Continuity Test Problems

- NON-CONDUCTIVE METAL SURFACES - PAINT, ANODIZING
  - GRIND OFF SURFACE AT TEST LEAD CONTACT POINTS
- CONTACT RESISTANCE AT TEST LEAD ATTACHMENT POINTS
- METAL FRAME ELEMENTS SEPARATED BY PLASTIC ELEMENTS
- LABORATORY ENVIRONMENT - AMBIENT TEMPERATURE, HANDLING FORCES

Figure 22. High-Resistance Riveted Joint

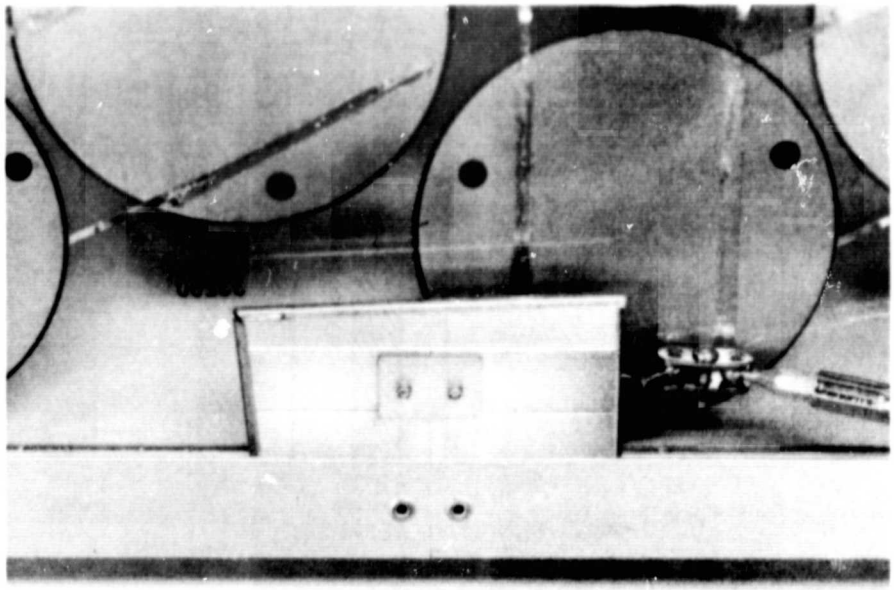


Figure 23. Results of Hipot and Continuity Tests

		INITIAL TESTS		FINAL TESTS		SETS THAT FAILED ONE OF THE FOUR TESTS	
		NUMBER TESTED	PERCENT FAILED	NUMBER TESTED	PERCENT FAILED	NUMBER OF SETS	PERCENT FAILED
INDIVIDUAL MODULES	HIPOT	280	10	160	19		
	CONTINUITY	238	12	122	29		
SETS OF MODULES*	HIPOT	35	26	31	42	25	73
	CONTINUITY	33	9	24	42		

*A SET OF MODULES IS A GROUP OF MODULES OF THE SAME TYPE FROM A MANUFACTURER AND AVERAGES EIGHT IN NUMBER

Figure 24. Voltage at Failure: Hipot Test

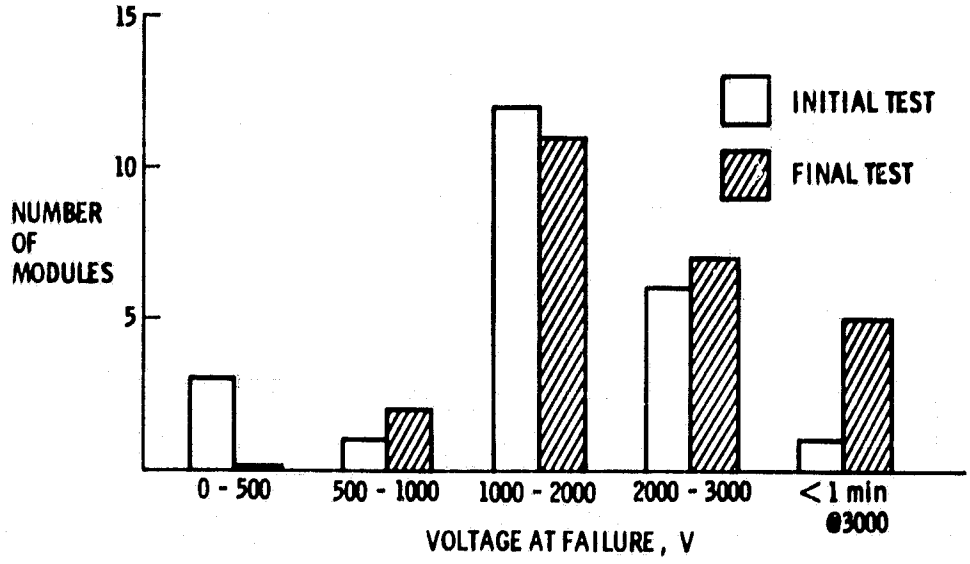


Figure 25. Resistance at Failure: Continuity Test

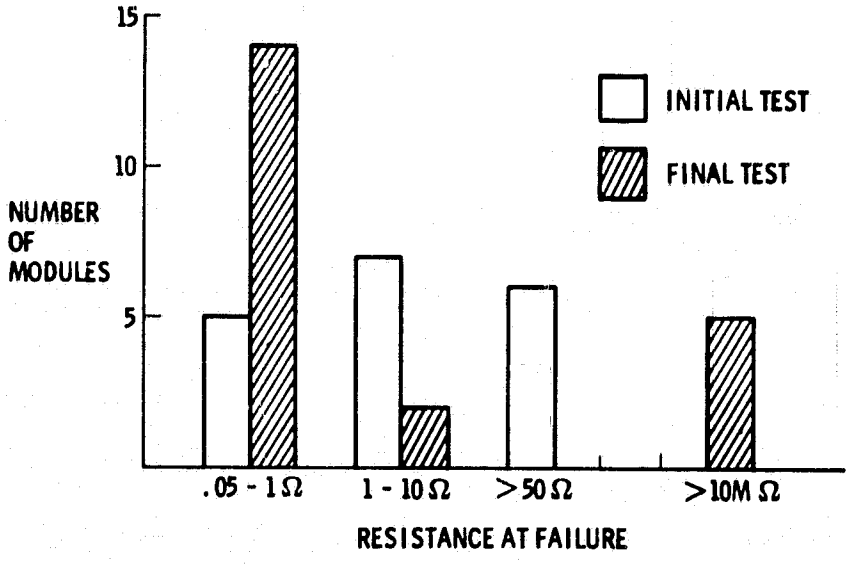


Figure 26. Summary

- HIPOT AND CONTINUITY TESTS HAVE CLEARLY DEFINED LIMITS FOR PASS-FAIL IN JPL PROCEDURES
    - CONTINUITY LIMITS FOR BLOCK V TESTS ARE DERIVED FROM UNDERWRITERS LABORATORY STUDIES
- THESE TESTS RESULT IN MANY FAILED MODULES. A MAJORITY OF THE MODULE DESIGNS FAIL IF THE CRITERION OF ONE FAILURE PER SET OF EIGHT IS USED
- A MAJORITY OF THE FAILURES CAN BE PREVENTED BY SIMPLE CHANGES IN DESIGN OR MODULE PROCESSING

LABORATORY EXPERIENCE WITH VOLTAGE BREAKDOWN

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Voltage breakdown failures in photovoltaic module electrical insulations lead to loss of entire source circuits and require costly maintenance and replacement. Avoiding such catastrophes requires that modules be designed so that voltage breakdown either never occurs or occurs so rarely that it affects the least life-cycle energy costs insignificantly. To achieve this desired balance of cost and reliability, the module design engineer must understand the failure mechanisms and use data on materials and failure rates to suppress or retard them. In this report, recently obtained failure mechanism information, rate data and materials property data are presented together with a qualitative model of module-failure prediction.

Two fundamental voltage breakdown mechanisms have been identified: (1) electronic, in which some as yet not completely understood electron-insulation interaction occurs involving measurable erosion (consumption) of insulation material, and (2) electrochemical, in which ions of anode material dissolve into and diffuse through the bulk insulation, eventually forming a conductive anode-to-cathode path (cell-to-frame). In this mechanism, the insulation is not eroded by electron interaction, but rather is permeated by conductive ions.

Applied electrical stresses in photovoltaic modules are generally low (30 to 50 volts/mil) but localized stress enhancers, such as voids or conductive inclusions in the encapsulation or sharp edges and burrs on electrodes, result in highly divergent local fields that may lead to immediate or eventual breakdown.

The effects of electrode offsets (interconnect tabs soldered to the cell underside) and sharp points (corners, cracks, burrs, etc.) are presented in Figure 4, in which the performance of real unencapsulated cells is compared with theoretical prediction. For small gaps, offsets determine the stress concentration, whereas at larger gaps the global electrode geometry (sharp point, cylinder, etc.) governs the stress enhancement.

In an attempt to characterize the statistical failure behavior of back-surface cover films, many small sections of large-area sheets of various thicknesses and layers of Mylar and Tedlar were subjected to increasing uniform stresses until breakdown occurred. Typical results are presented in Figures 6 and 7. Note that probability of failure decreases rapidly with increasing thickness (Figure 6, experimental data) and layering (Figure 7, theoretical calculations). The material in Figure 7 also predicts a higher failure probability for larger-area modules.

The effect of temperature-humidity exposure on statistical characterization of Tedlar failures is presented in Figure 8, where it is observed that for a given applied voltage stress, the probability of failure increases as a result of the exposure.

The mechanism of electrochemical corrosion is depicted in Figure 9. Under the applied voltage difference between cell and frame, cell metallization is ionized and dissolves into the encapsulation. Concentration and voltage gradients drive the ions to the frame, forming either a conductive breakdown path or dendritic growths that eventually extend the cathode to the anode (Figure 10). The presence of water and elevated temperatures accelerate this process.

The coatings industry (paint-on-metal) has determined that metal electrochemical corrosion is most pronounced at spots where the coating resistivity is low, and the converse. This has been found to be true of polymer-protected solar-cell metallization. The resistivity of ethylene vinyl acetate (EVA) and polyvinyl butyral (PVB) were determined over a range of temperatures and humidities by measuring the material resistance between embedded electrodes (Figure 12). Results are shown in Figure 13. Resistivity decreases (electrochemical cell corrosion increases) with increasing temperature and humidity, although the effect of humidity is not significant on EVA.

In an extensive parametric test, two-cell module combinations of three encapsulants [EVA, room-temperature vulcanized (RTV), PVB] and three cell metallization system (Ag-paste, Ni-solder, Ti-Pd-Ag) were tested for 1944 hours at 85°C and at three different humidities (2.5%, 70%, 98%) and voltages (0 V, 30 V, 60 V).

Silver-metallized cells encapsulated in PVB are shown in Figure 15 in pre-exposure condition. Three of these are shown in Figure 16 in post-exposure condition. Visual analysis of changes provides valuable insights into potential failure mechanisms.

Information obtained visually is correlated with electrical measurements in an attempt to quantify phenomena. Variables monitored electrically are listed in Figure 17. I-V curves were obtained before and after exposure, from which changes in series and shunt resistance, short-circuit current, and maximum power output are determined. During the 1944 hours of exposure, series and shunt resistance, junction and insulation capacitances and their associated loss factors, insulation resistance, and dc discharge inception voltage were monitored periodically.

Insulation resistance versus time is plotted in Figures 18 through 20 for cells featuring silver metallization encapsulated with EVA, RTV, and PVB, respectively. EVA shows little change of resistance with time or humidity level. The highest humidity exposure of RTV results in a steady decrease of insulation resistance, and the response to different humidity levels of PVB is pronounced. These data correlate with visual observations: EVA-encapsulated samples exhibit little electrochemical degradation; RTV samples exhibit somewhat more, and PVB shows significantly more degradation.

Similar results are obtained from the insulation capacitance data. Pre-exposure and post-exposure values are the same, but during exposure, absorbed water drives up the measured capacitance, especially in PVB-encapsulated specimens.

Dc discharge inception voltage (DIV) versus time is plotted for PVB-encapsulated samples in Figures 22 through 24. DIV is the lowest voltage at which sustained 5 pC discharges are observed. It is observed that DIV decreases upon exposure (except at 70% RH) and recovers after exposure. The anomaly at 70% RH is as yet unexplained. It is important to realize, however, that discharge-free modules at the time of manufacture may suffer discharges under field-exposure conditions.

Typical results of I-V curve maximum-power output data are presented in Figure 25. ESO (EVA/silver) degrades more rapidly than EA (EVA/trimetal), indicating greater stability of the passivated versus the non-passivated silver metallization systems. Comparing EA with PA (PVB/trimetal), it is concluded that the PVB affords less protection to the cell than does EVA.

Assuming that the bulk of the anode-cell maximum power output reduction results from metallization corrrosion, and realizing that metallization corrosion is an interfacial charge transfer phenomenon, the normalized (to pre-exposure values) maximum power output is plotted against the total unit area charge transferred (obtained by monitoring leakage currents (see Figure 26). These preliminary data indicate that for unencapsulated cells, Ni-solder metallizations are more corrosion-resistant than passivated silver metallizations; on encapsulated cells, the two metallizations exhibit comparable performance. These data suggest the possibility of predicting module (electrochemical) life from in-situ leakage-current measurements.

In summary, electrochemical corrosion occurs in photovoltaic modules exposed to controlled high-temperature and high-humidity environments. Power-output reduction is linked with interfacial charge transfer as being responsible for the corrosion. Hence, this mechanism will be observed in the field. The rate of corrosion has not yet been determined.

The topics covered in his report have several implications for improved module design. These are listed in Figure 28.

The ultimate goal of developing a life-cycle cost-design algorithm for selecting and sizing electrical insulation for photovoltaic modules has not yet been achieved. The next step requires using site-specific environmental data together with experimental degradation-rate data to achieve a life-prediction capability. This achieved, a complete costing algorithm will soon be available.

LABORATORY EXPERIENCE WITH VOLTAGE BREAKDOWN

JET PROPULSION LABORATORY

G.R. Mon

Figure 1. Motivation

- The problem:
  - Electrical insulation failures (voltage breakdown) are catastropic, resulting in loss of source circuits, and costly, requiring maintenance and replacement
- Objective:
  - Design modules so that voltage breakdown never occurs or occurs so rarely that its impact on least life-cycle energy costs is insignificant

Figure 2. Approach

- Experimental
  - Define voltage breakdown and determine breakdown failure mechanisms
  - Determine failure rates and/or probabilities
  - Establish extent to which module design parameters, material and geometric, suppress or retard the failure mechanisms
- Analytical
  - Develop algorithm to predict frequency of voltage breakdown using module design parameters and ambient site conditions as input
  - Determine life-cycle cost of deliverable energy

Figure 3. Voltage Breakdown: Failure Mechanisms

- **Intrinsic breakdown: an electronic breakdown mechanism induced by large uniform stress**
  - Electromechanical breakdown
  - Thermal breakdown
- **Flaw-induced breakdown: stress enhancers result in localized, highly divergent stresses even though the applied stress may be uniform and of modest magnitude**
  - Divergent field breakdown (inclusions, electrode projections, sharp edges)
  - Internal discharge breakdown (voids)
- **Electrochemical breakdown: anode-electrolyte (cell-pottant) interactions result in metallization dissolution and diffusion through the encapsulant, forming a conductive path to ground (frame)**

Figure 4. Laboratory Experience With Flaw-Induced Breakdown (Electrode Effects: Offsets and Sharp Points)

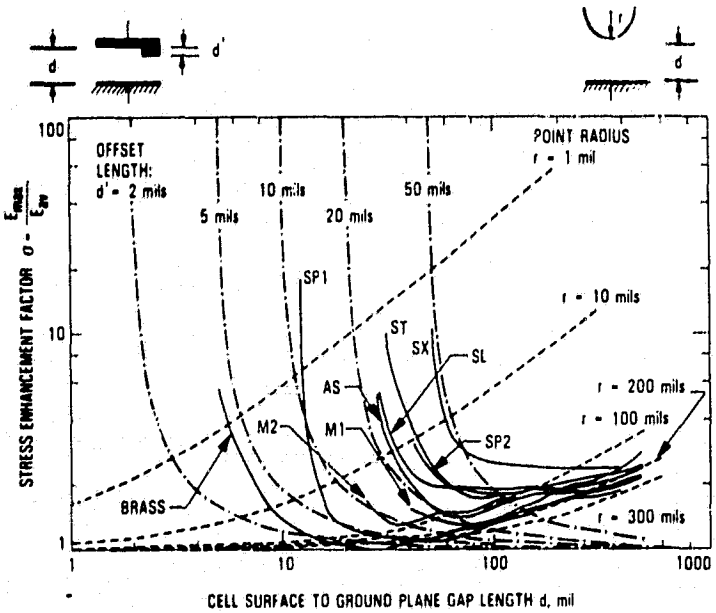
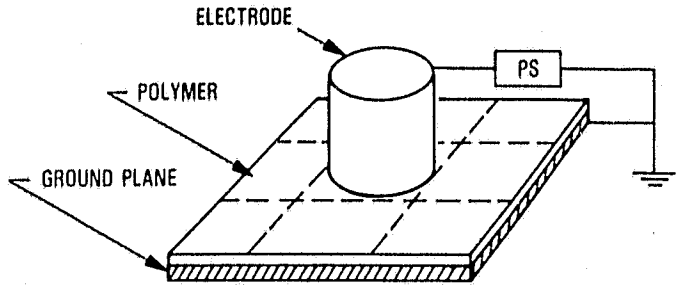


Figure 5. Laboratory Experience With Flaw-Induced Breakdown (Dielectric Effects)

- **Experimental arrangement:**



- **Results**
  - **Stress-probability characterization of back-cover films (Mylar, Tedlar)**
  - **Reduction of dielectric strength due to thermal aging**
  - **Fewer layers of thicker films (e.g., 2 layers of 3-mil Mylar) is the indicated cost-optimal solution to a manufacturing yield problem**

REF: Mon, G.R., "Defect Design of Insulation Systems for Photovoltaic Modules," IEEE Photovoltaics Specialists Conference 1981

Figure 6. Voltage Breakdown Characteristics of Single-Layer Mylar and Tedlar Films

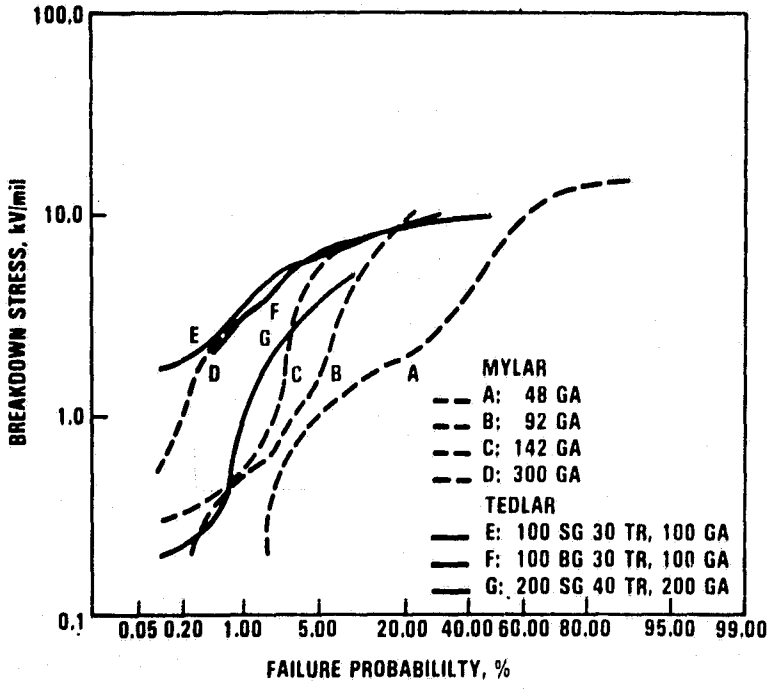


Figure 7. Failure Probability of Modules Using Indicated Number of Layers of 1.42-mil Mylar Insulating Film

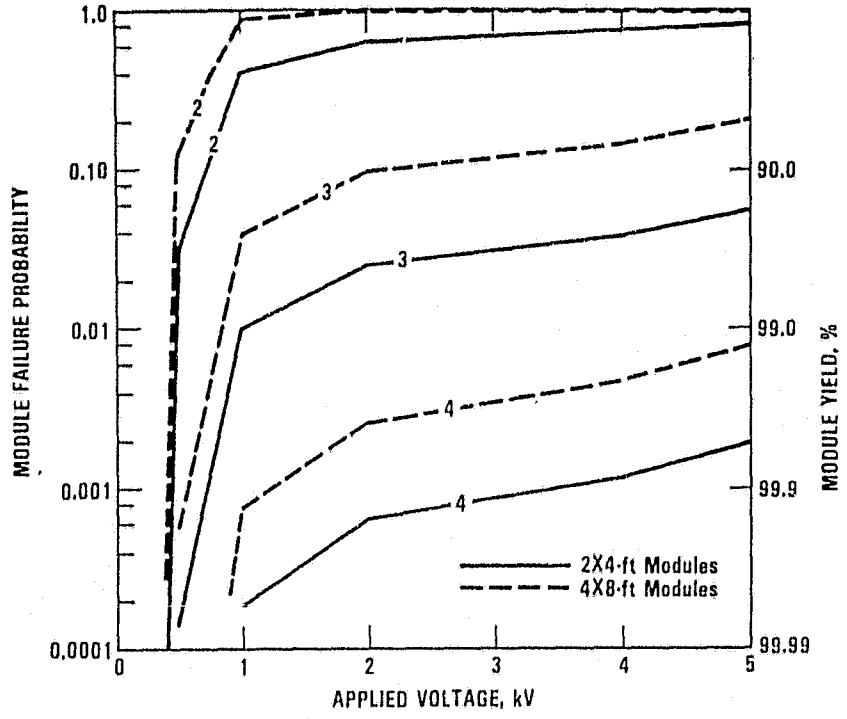


Figure 8. Voltage Breakdown Characteristics of 4.00-mil Experimental White Tedlar, Unaged vs Aged (1704 h at 40°C / 93% RH)

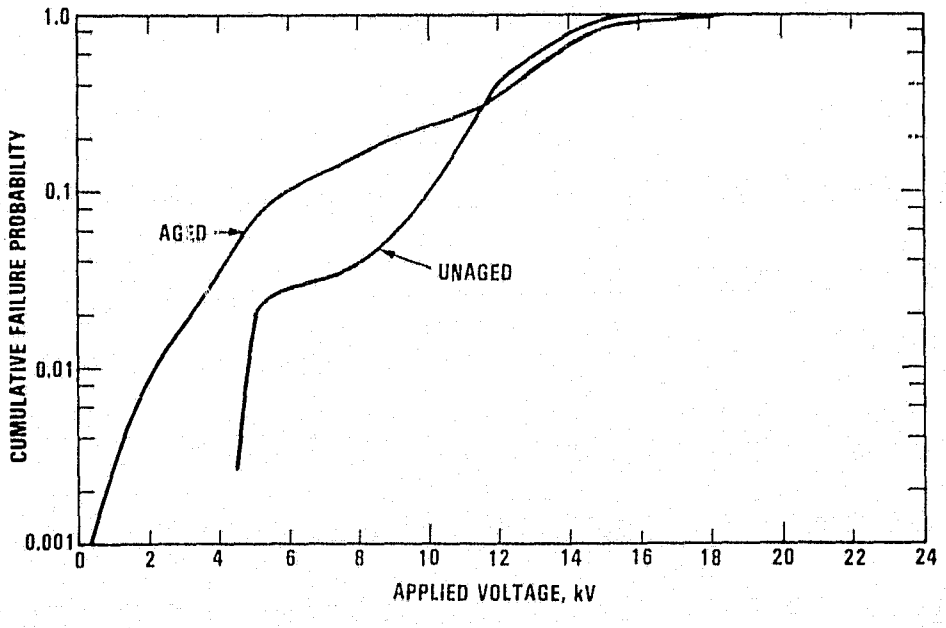


Figure 9. Corrosion Mechanism Overview

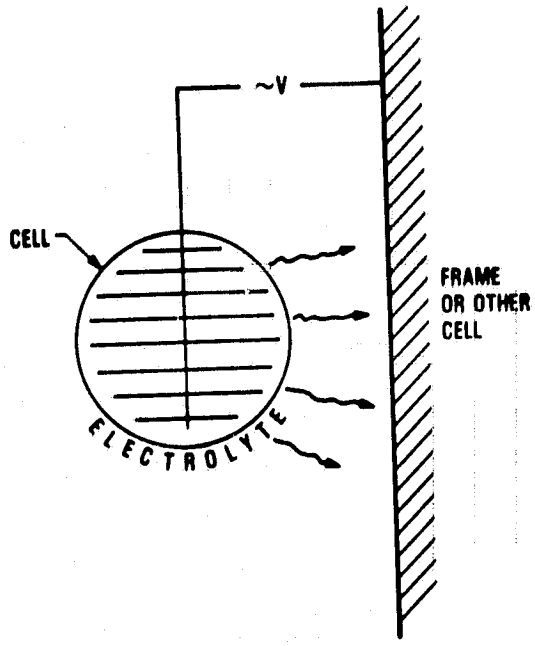


Figure 10

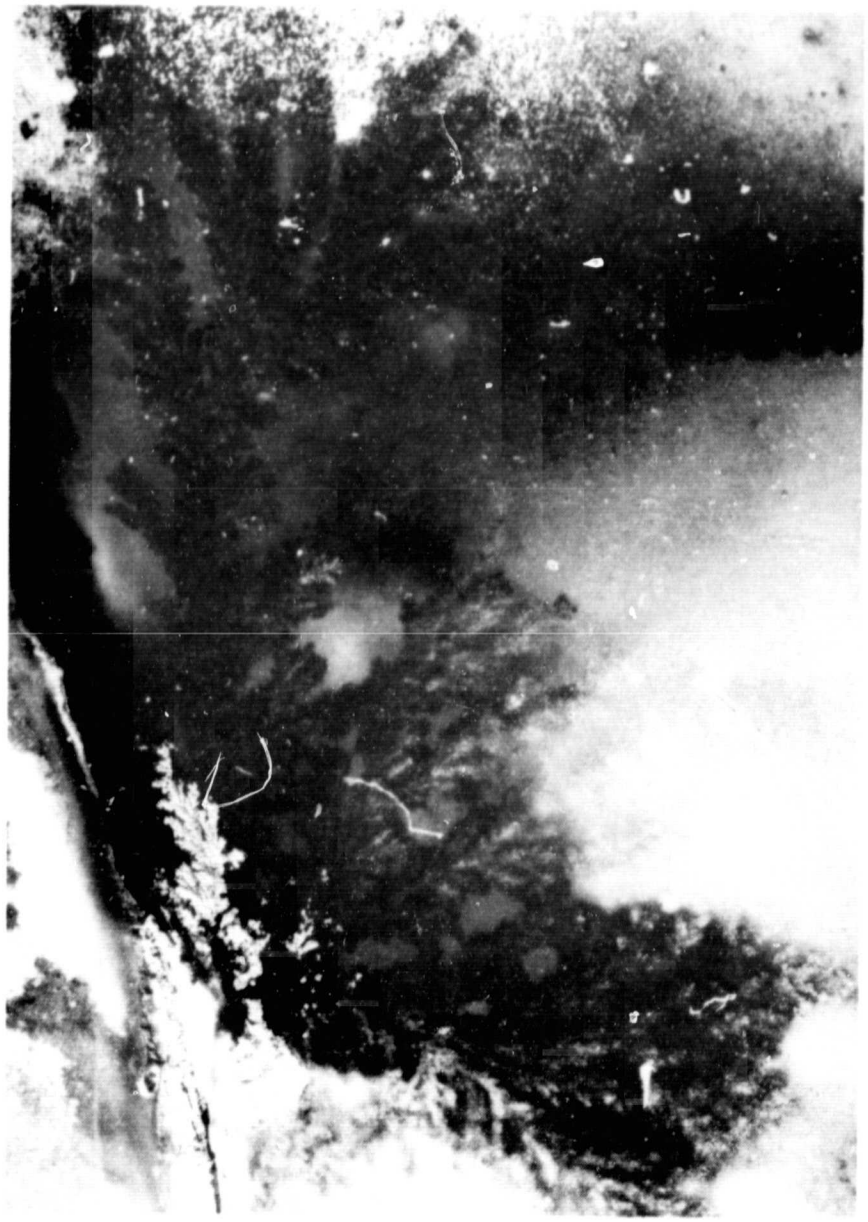


Figure 11. Laboratory Experience With Electrochemical Degradation (Electrode-Dielectric Interfacial Effects)

- Dielectric resistivity as a function of temperature and relative humidity
- Variation with time of exposure to constant T/RH environments of
  - Insulation resistance
  - Insulation capacitance
  - DC discharge inception voltage
- Power output
  - Variation with humidity after 1944 h at 85°C
  - Variation with charge transfer across cell-pottant interface

Figure 12. Experimental Setup

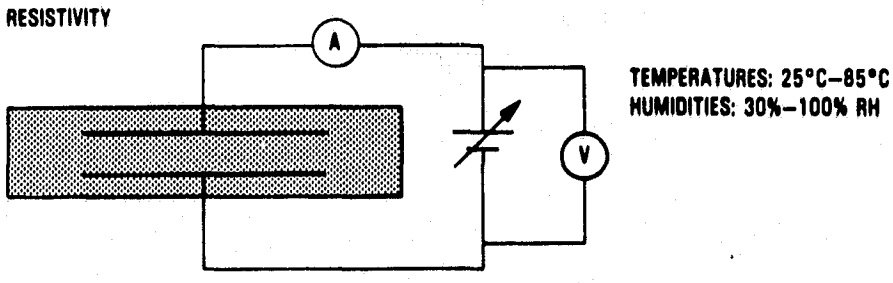


Figure 13. Resistivity vs RH With Temperature as Parameter

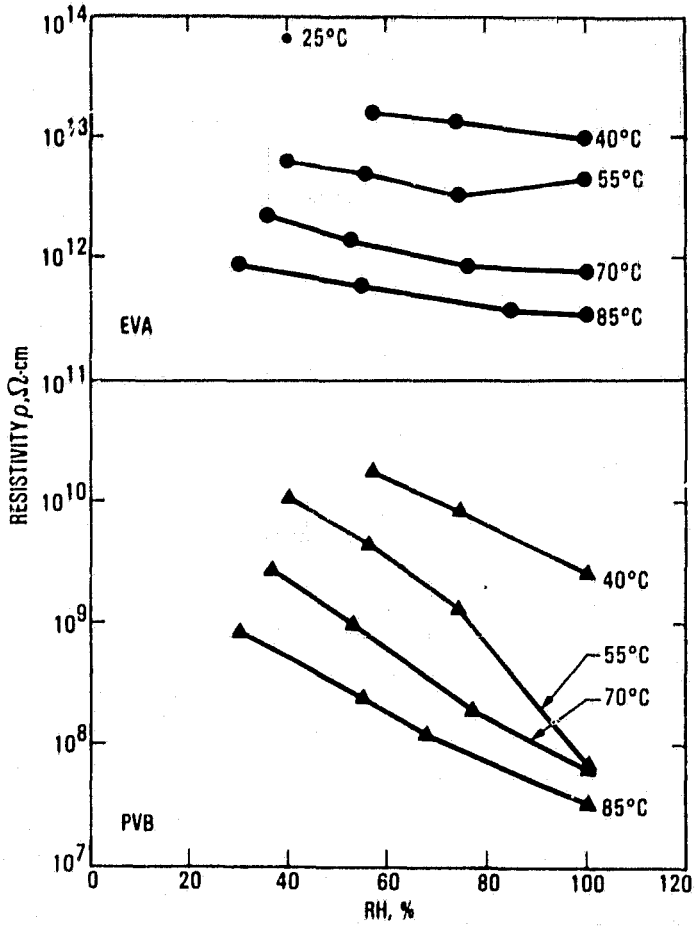


Figure 14. Intercell and Cell-Frame Corrosion Experiment

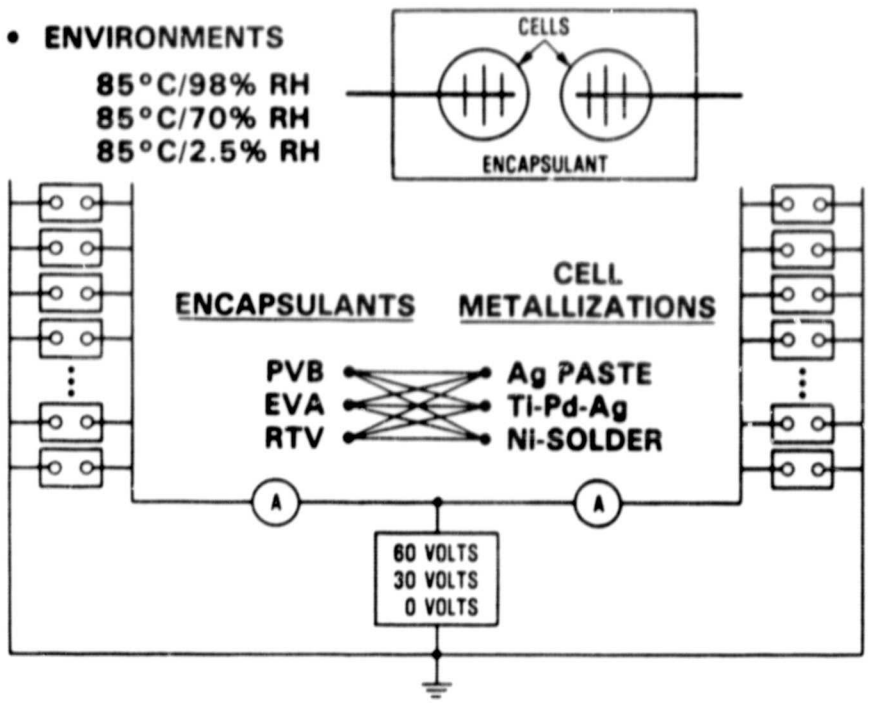


Figure 15

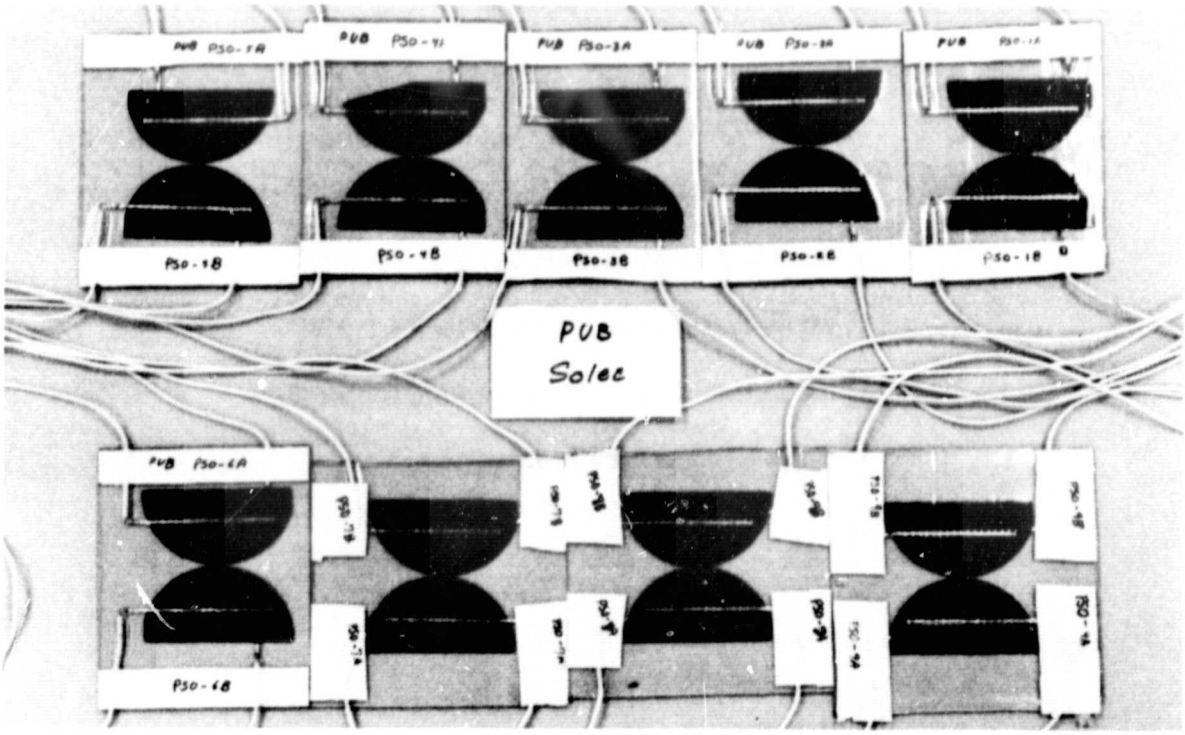


Figure 16

Figure 17. Variables Monitored in Corrosion Experiment

- **Light I-V curves (pre-test and post-test)**
- **In situ**
  - **Series resistance R_S**
  - **Shunt resistance R_{SH}**
  - **Junction capacitance C_J; loss factor D_J**
  - **Insulation resistance R_I**
  - **Insulation capacitance C_I; loss factor D_I**
  - **Dc discharge inception voltage DIV**

Figure 18. R_{INSUL} vs Time (ESO: 85°C)

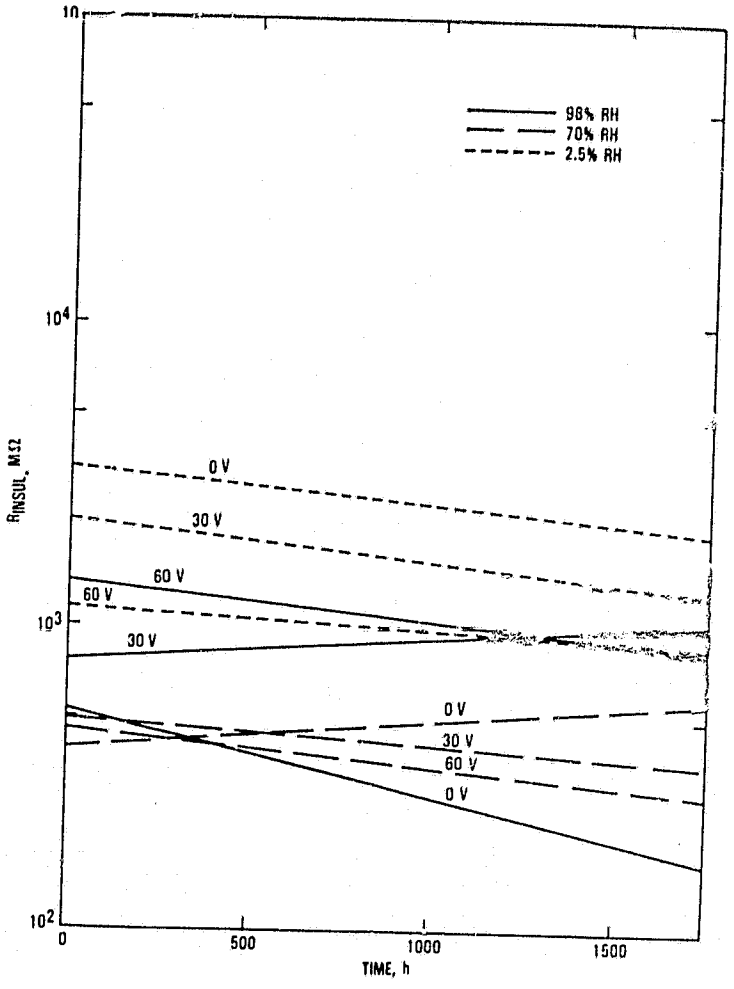


Figure 19. R_{INSUL} vs Time (RSO: 85°C)

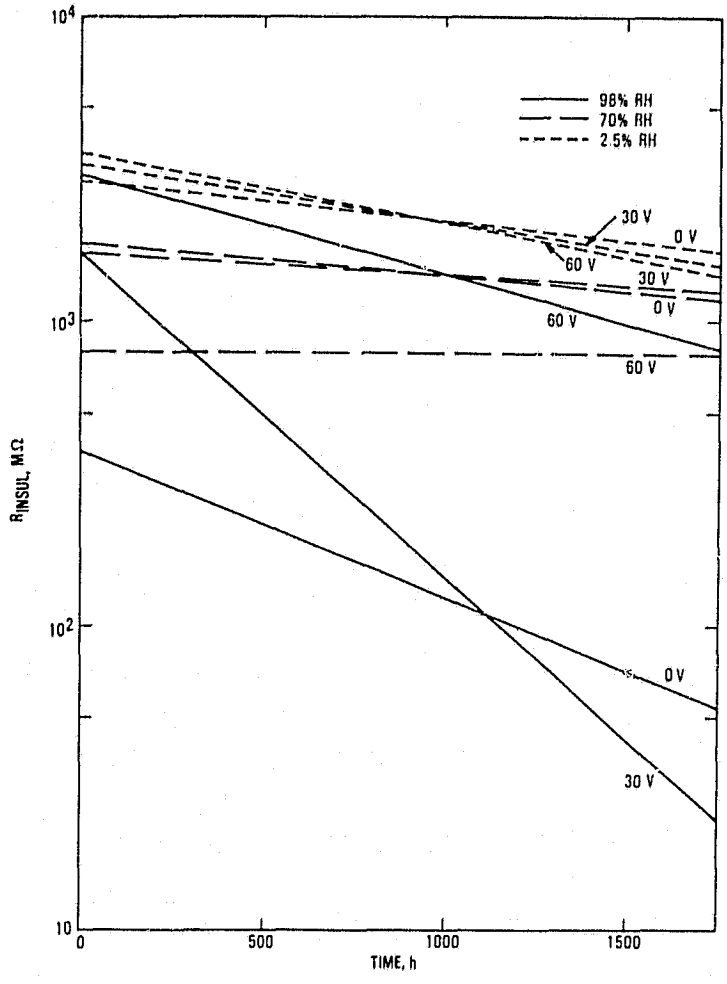


Figure 20. R_{INSUL} vs Time (PSO: 85°C)

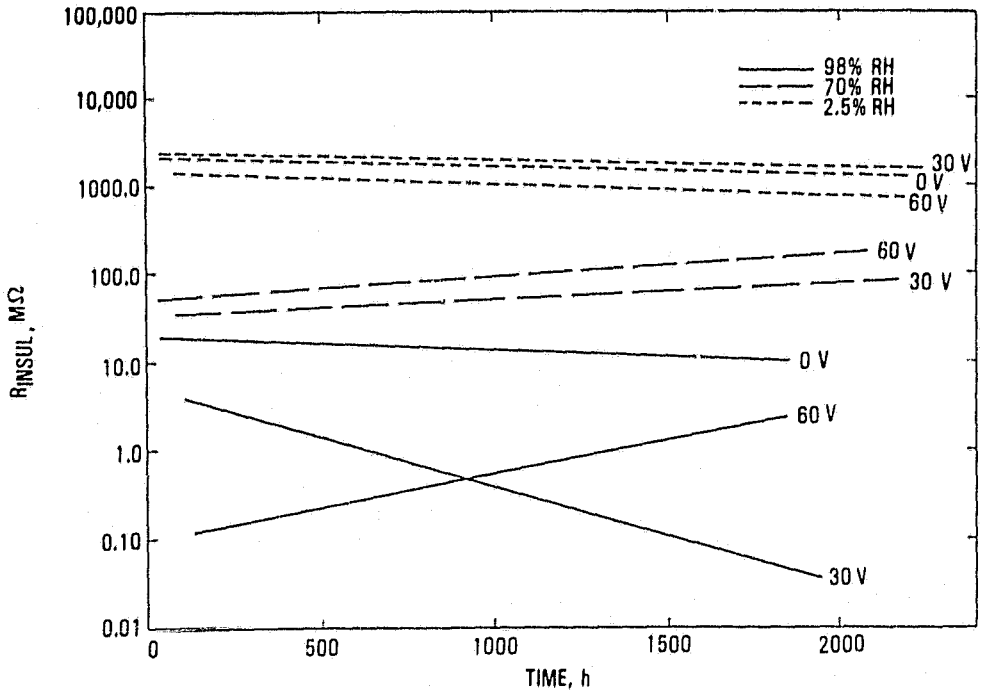


Figure 21. Insulation Capacitance Data (General)

- **Pre-test and post-test insulation capacitance measurements are about the same**
- **Insulation capacitance increases in value when exposed to environment**
- **Insulation capacitance increases with time of exposure at a rate dependent on the amount of absorption of water ($\epsilon \approx 75$)**

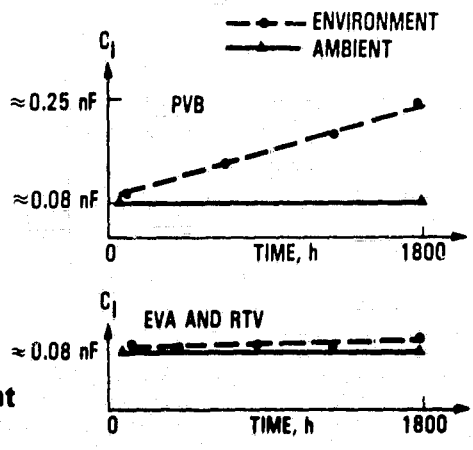


Figure 22. Dc DIV (kV) vs t, h: 85°C / 2.5%

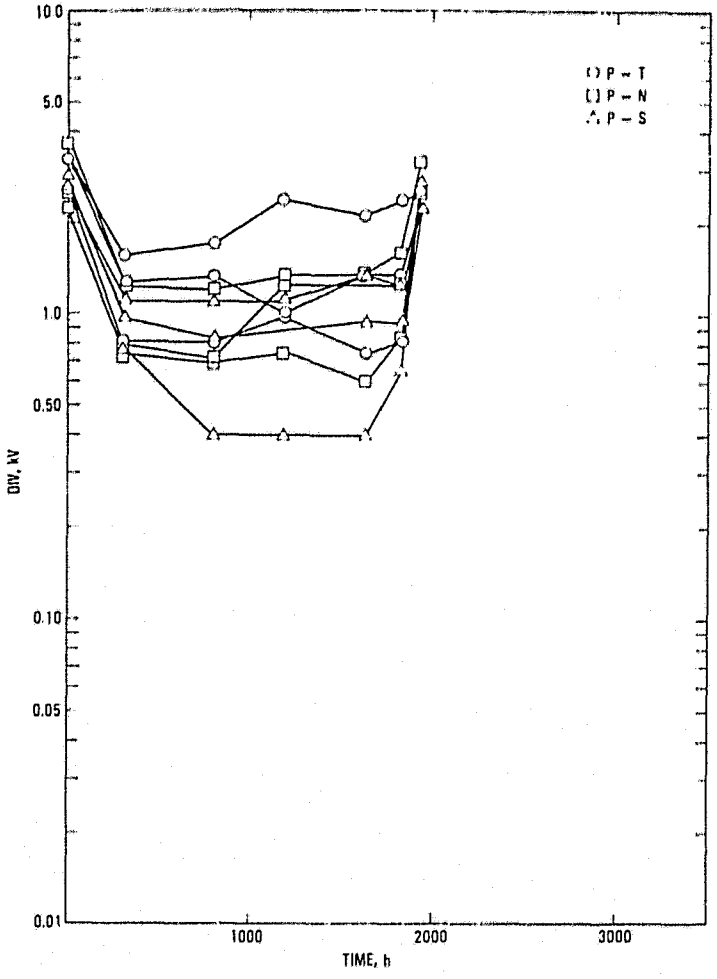


Figure 23. Dc DIV (kV) vs t, h: 85°C / 70% RH

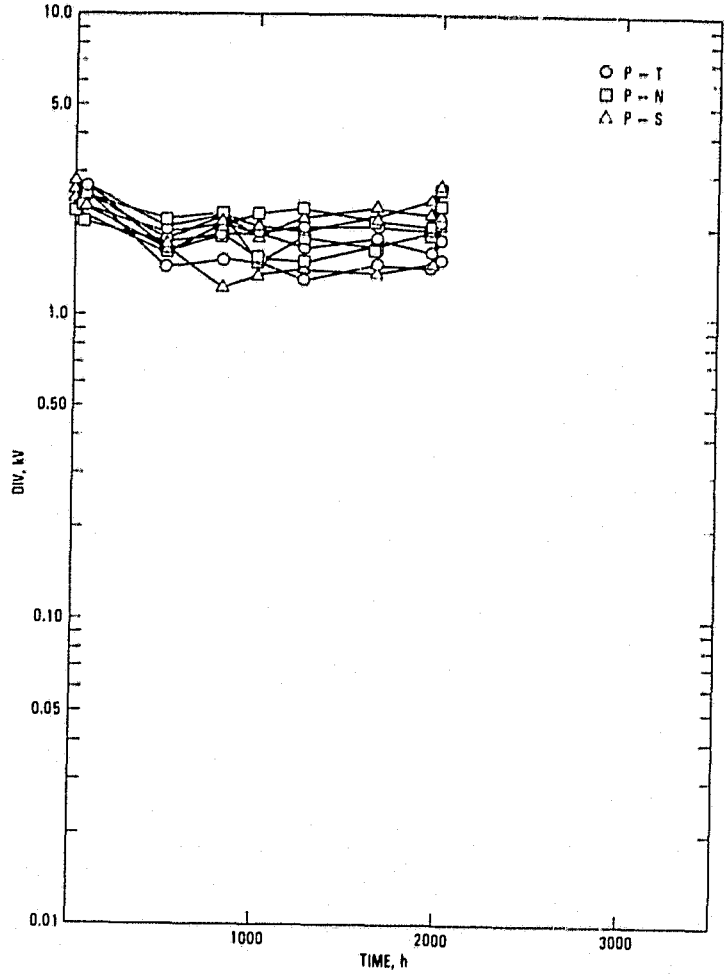


Figure 24. Dc DIV (kV) vs t, h: 85°C / 98% RH

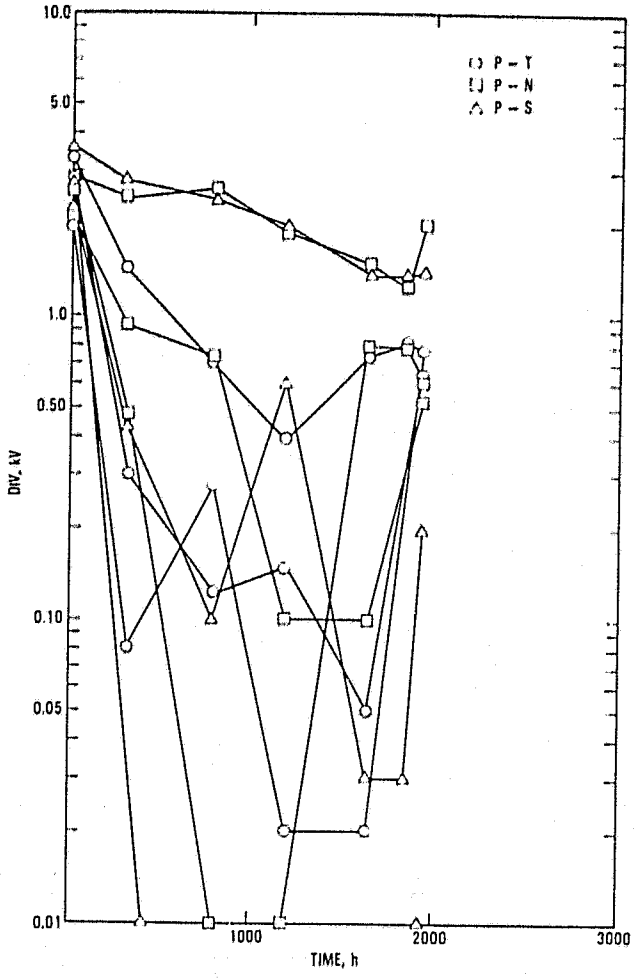


Figure 25. Power Reduction in Two-Cell Modules as a Function of Relative Humidity

Temperature 85°C; Exposure time 1944 h

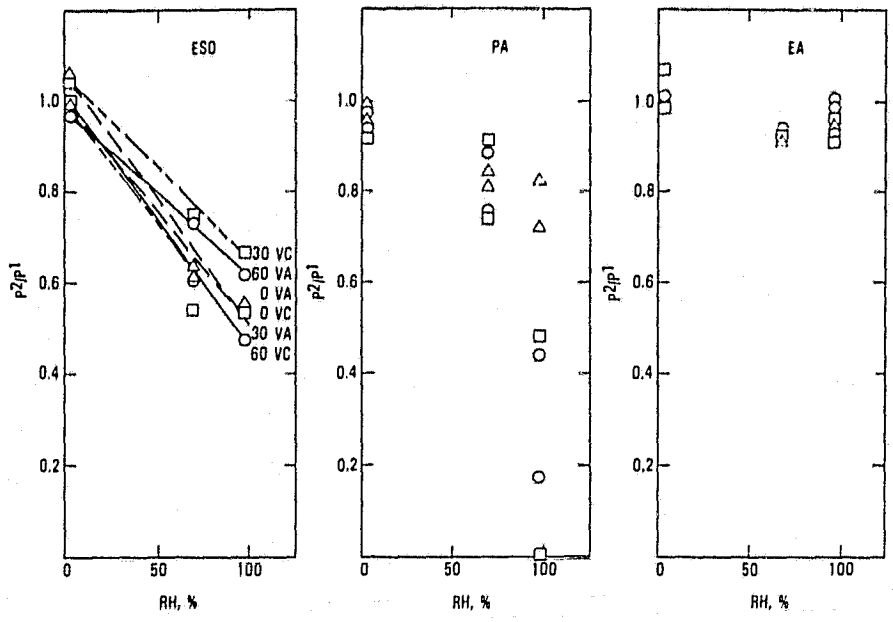


Figure 26. Power Output as a Function of Charge Transferred Across Cell-Pottant Interface

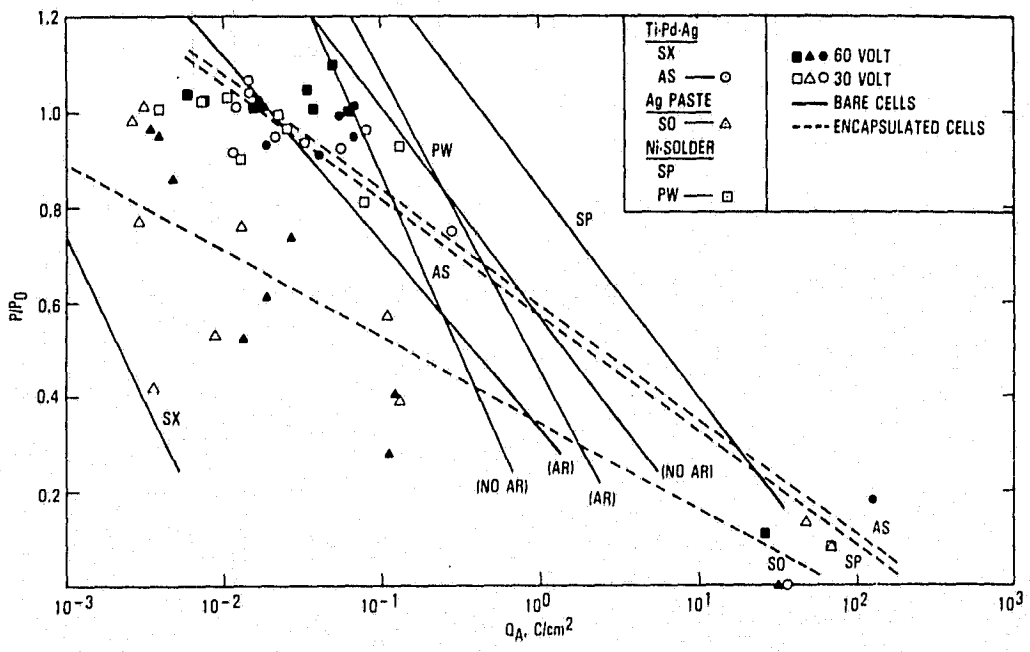


Figure 27. Summary: Failure Mechanisms, Causes and Effects

Parameter Monitored	Parameter Variation	Observed Degradation	Probable Mechanism
Series resistance	$R_S \uparrow$	Metallization Dissolution	Electrochemical electrode-electrolyte reactions between metallization and pottant
Short-circuit current	$I_{sc} \downarrow$	Discoloration of encapsulation; reduced optical transmission	Diffusion of metallization into encapsulation resulting in metallization-encapsulant interactions catalyzed by high temperature and moisture levels
Insulation resistance and capacitance	$R_I \downarrow$ $C_I \downarrow$	—	Absorption of moisture
Discharge inception voltage	DIV $\downarrow$	Conducting paths between high-voltage cell and ground, electrical breakdown	Diffusion of metallization from cell to cell or from cell to frame

Figure 28. Electrochemical Data: Conclusions

- Encapsulation-metallization rankings
- At high temperature and moisture concentration levels, permeated water increases the pottant dielectric permittivity (insulation capacitance) and hence the electric field strength in voids and at inclusions, resulting in lower partial-discharge inception levels
- There is direct experimental evidence that high temperature and humidity levels decrease encapsulant resistivity, resulting in increased charge transfer (electrochemical degradation) at the cell-pottant interface and decreased cell power-output levels

Figure 29. Implications for Module Design

- Flaw-induced breakdown
  - Blunt edges on all electrified and grounded conductive components
  - Use void-free, inclusion-free encapsulations or use impregnant to reduce stress levels in voids
  - Operate below partial-discharge inception voltage
- Electrochemical breakdown
  - Use low moisture absorptivity encapsulants
  - Use low ion-content encapsulants
  - Use electrochemically passive metallizations
  - Use liberal safety margin (distance) between cells and between cell and frame (ground)

BREAKDOWN OF ORGANIC INSULATORS

Edward F. Cuddihy
Jet Propulsion Laboratory
Pasadena, CA 91109

Solar cells and their associated electrical interconnects and leads are being encapsulated in transparent elastomeric materials such as ethylene vinyl acetate (EVA), polyvinyl butyral (PVB), room-temperature vulcanized (RTV) silicones and a few others. Among their many purposes in a photovoltaic module, one of the most important for these elastomeric encapsulation materials is to function as electrical insulation. This includes internal insulation between adjacent solar cells, between other encapsulated electrical parts, and between the total internal electrical circuitry and external metal frames, grounded areas, and module surfaces. Catastrophic electrical breakdown of the encapsulant insulation materials or electrical current through these materials or module edges to external locations can lead to module failure and can create hazards to humans.

The aging deterioration of organic insulation material subjected to long-term electrical stresses is extremely complex. In an outdoor environment, there may also be thermal, mechanical and chemical actions that may be simultaneously occurring in an electrically stressed material, which may further contribute to insulation breakdown. Other mechanisms that can lead to electrical breakdown of organic insulators can originate in manufacturing defects (voids, cracks, etc.) and/or ionic impurities (electrochemical effects) and from aging (i.e., delamination, mechanical generation of cracks, and chemical generation of ionic components).

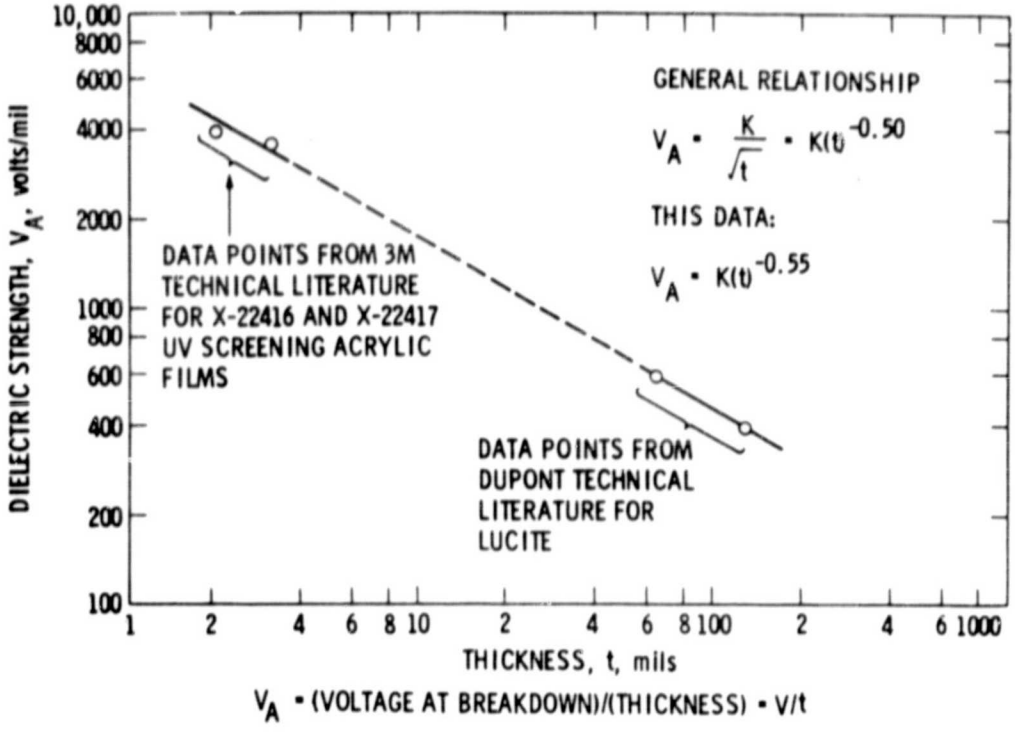
With a view toward electrical insulation stability, advanced elastomeric encapsulation materials are being developed that are intended to be intrinsically free of in-situ ionic impurities, have ultralow water absorption, be weather-stable (UV, oxygen), and have high mechanical flexibility. Despite these positive efforts toward improving insulation durability and reliability, a capability of predicting the service life of organic insulation materials is not yet a realized technology. Efforts to develop a method of assessing the life potential of organic insulation materials in photovoltaic modules are described.

BREAKDOWN OF ORGANIC INSULATORS

JET PROPULSION LABORATORY

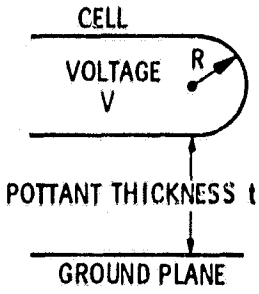
Edward F. Cuddihy

Dielectric Strength of PMMA Acrylic



V_A = (VOLTAGE AT BREAKDOWN)/(THICKNESS) = V/t

Spectrolab Computer Data



$V_A/(dV/dt)_{max}$	(t/2R)
0.9116	0.25
0.8200	0.50
0.7004	1.00
0.5648	2.00
0.3916	5.00
0.2968	10.00
0.2305	20.00
0.1898	50.00

$$V_A = V/t = (dV/dt)_{max} (2R)^{0.54} (t + 2R)^{-0.54}$$

Similarity of Dielectric Strength Equations

EMPIRICAL $\longrightarrow$ $V_A = K t^{-1/2}$

COMPUTER THEORY $\longrightarrow$ $V_A = (dV/dt)_{max} (2R)^{1/2} (t + 2R)^{-1/2}$

GENERAL FORM

$$V_A = K (t + a)^{-n}$$

$$V_A = K a^{-n} = (dV/dt)_{max} \quad AT \quad t = 0$$

Needle Electrodes: Exact Solution for Tip-to-Tip

$$(dV/dt)_{max} = \frac{V_A t (1 + 2R/t)^{1/2}}{2R \tanh^{-1} \left\{ t/(t + 2R) \right\}^{1/2}}$$

AS $t \longrightarrow 0$

$$V_A = (dV/dt)_{max} (2R) (t + 2R)^{-1}$$

Needle Electrodes: Exact Solution for Tip-to-Ground-Plane

$$(dV/dt)_{max} = 2\, V_A\, t\, P/Ln\,(Q)$$

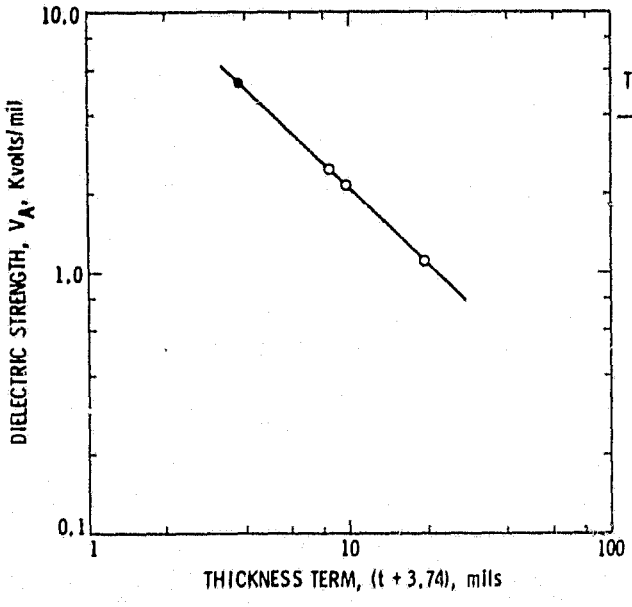
$$P = (1 + R/t)^{1/2}/R$$

$$Q = \left\{2t + R + 2t^{1/2}(t + R)^{1/2}\right\}/R$$

AS $t \longrightarrow 0$

$$V_A = (dV/dt)_{max}(R)^{0.7}(t + R)^{-0.7}$$

Dielectric Strength of A-9918 EVA



THICKNESS t, mils	AVERAGE DC BREAKDOWN VOLTAGE, KV	AVERAGE DIELECTRIC STRENGTH, V_A = V/t, KV/mil
4.7	11.7	2.49
6.0	13.0	2.17
15.7	17.6	1.12

$V_A = 19173\,(t + 3.74)^{-0.96}$

$(dV/dt)_{MAX}$ @ t = 0 = 5404 volts/mil

Comparison of EVA and PMMA Dielectric Strength Data

EXPERIMENTAL DATA FIT

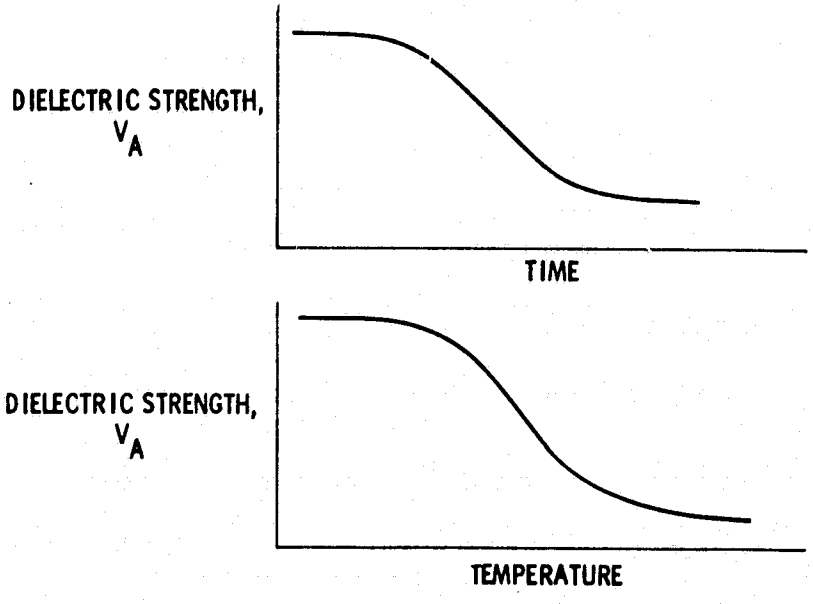
PMMA $\quad V_A = 8009\,(t + 0.87)^{-0.63}$

(EL)/(GP) $\quad (dV/dt)_{max} = (8009)\,(0.87)^{-0.63} = 8740$ volts/mil

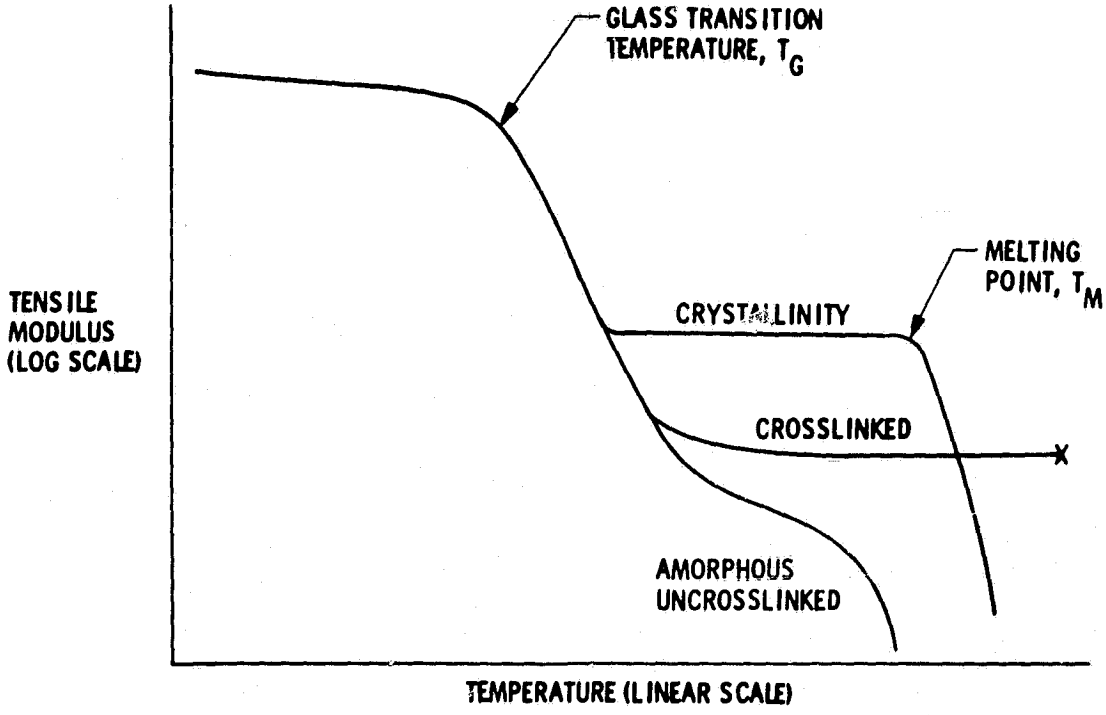
EVA $\quad V_A = 19173\,(t + 3.74)^{-0.96}$

(EL)/(EL) $\quad (dV/dt)_{max} = (19173)\,(3.74)^{-0.96} = 5404$ volts/mil

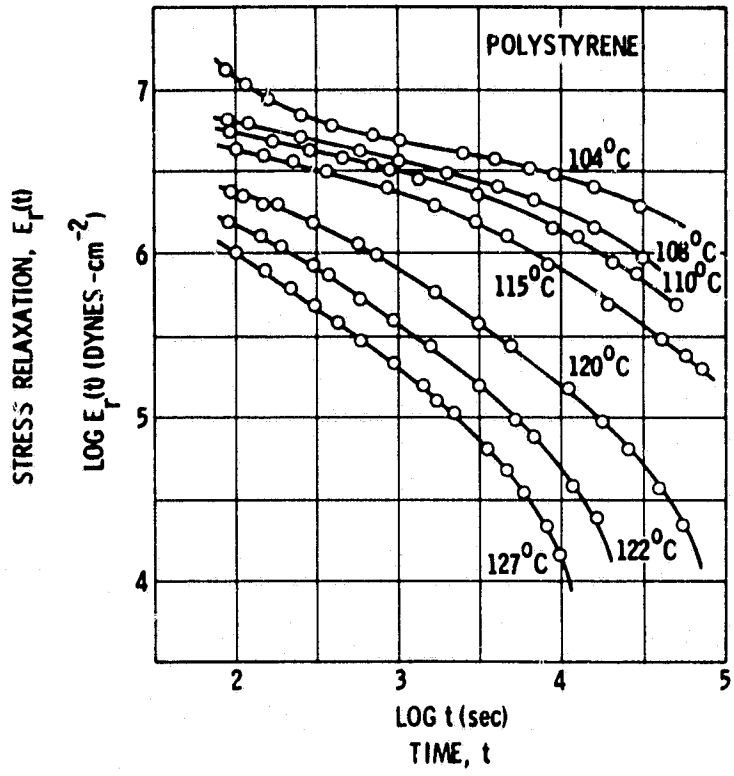
Dc Voltage Dielectric Strength Behavior (Literature)



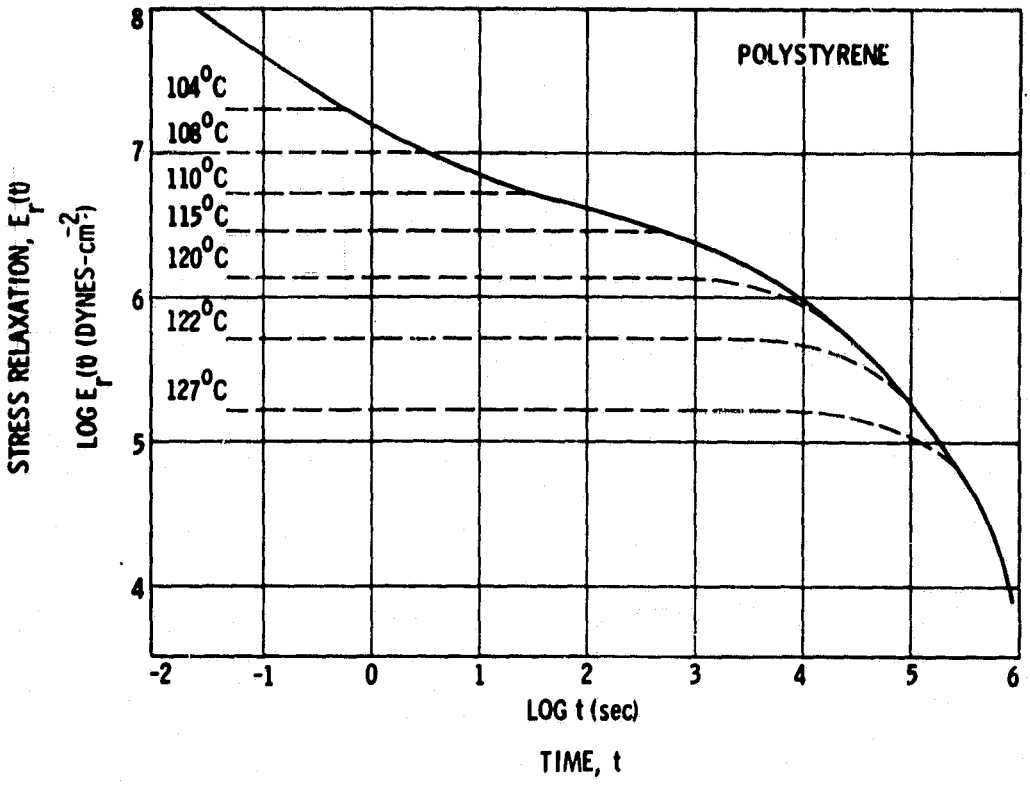
Generalized Mechanical Property Behavior of Crosslinked and Crystalline Polymers



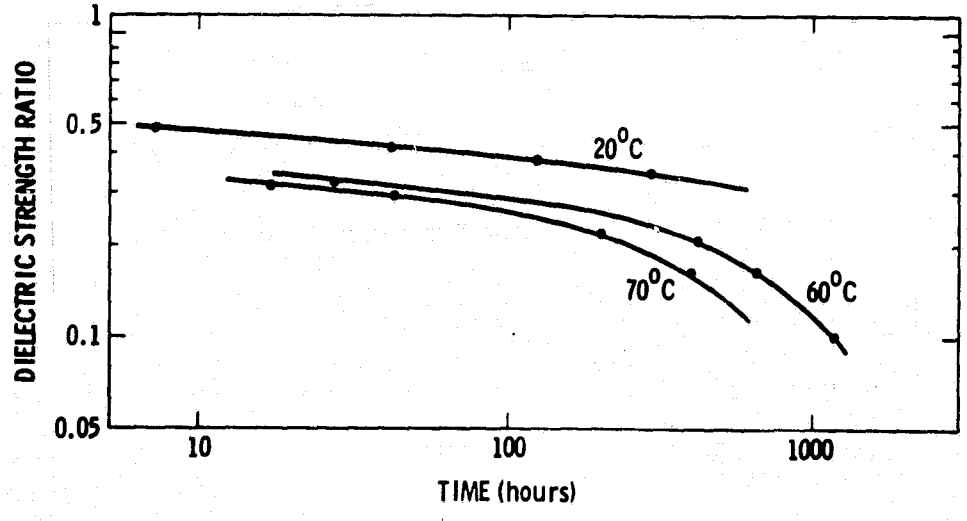
Time-Temperature Superposition: Parametric Data Curves



Time-Temperature Superposition: Master Curve for Time Extension



Dielectric Strength of Polyethylene



DATA SOURCE: PROFESSOR LUCIANO SIMONI
UNIV. OF BOLOGNA (ITALY)

OMIT 70
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167

DINNER SPEAKER

SACRAMENTO MUNICIPAL UTILITY
DISTRICT 100-MW_e
PHOTOVOLTAIC POWER PLANT

J. Mattimoe, SMUD

SACRAMENTO MUNICIPAL UTILITY DISTRICT 100-MW_e PHOTOVOLTAIC POWER PLANT

SACRAMENTO MUNICIPAL UTILITY DISTRICT

John Mattimoe

SMUD's Interest in Photovoltaic Power

- Provides a new source of generating capacity
- Addresses summer daytime peak load
- Represents a renewable resource insulated from escalating fuel prices
- Provides plentiful and reliable energy in our sunny area

Topics

- SMUD's resource plan
- SMUD's interest in photovoltaic power

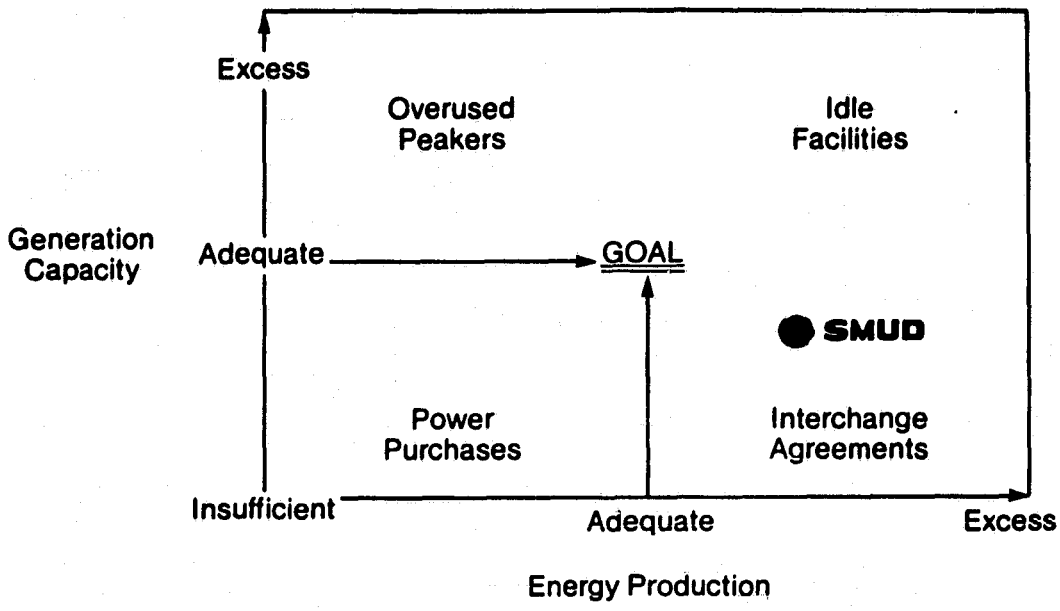
Generation Resources

Existing Facilities	Type	Resources Capacity (MW)	Resources Energy (GWH/Yr)	Costs (1983 $) Capital ($/kW)	Costs (1983 $) Energy (¢/kWH)
American River	Hydro (Normal Year)	649	1,725	215	0.75
Rancho Seco	Thermal (Summer Rating)	875	4,496	500	1.67
WAPA	Purchase	360	2,200	N/A	0.90
SMUDGEO-1	Geothermal	65	427	1,474	5.70
		1,949	8,848		

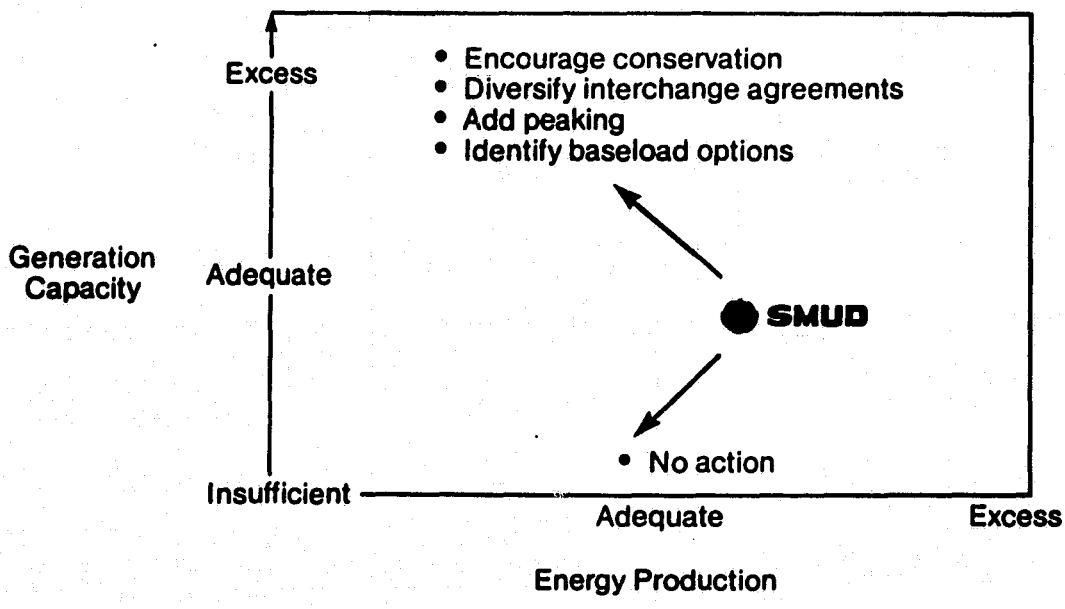
- Interchange Agreement
  - — PG&E provides standby energy and capacity
  - — PG&E uses all SMUD excess energy and capacity
  - — Contract ends January 1988

Resource Plan

SMUD - 1983



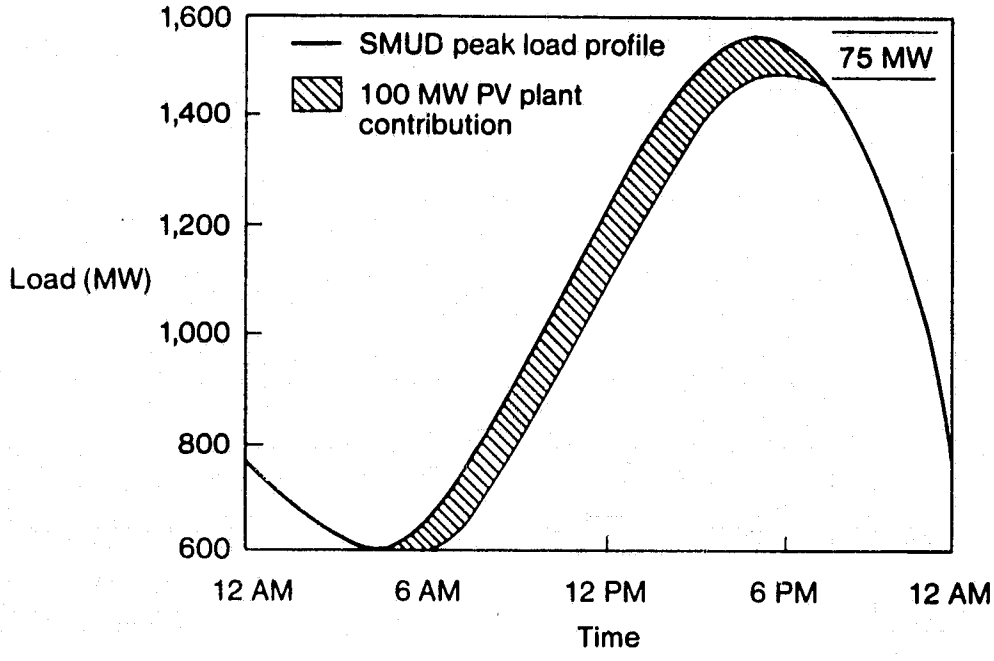
Projection to 1988



Committed and Potential Resources

Committed	Year On-line	Capacity (MW)	Costs (1983 $) Capital ($/kW)	Energy (¢/kWH) First Year	Energy (¢/kWH) Levelized
Geothermal no. 1	1984	65	1,474	5.7	8.3
Jones Fork Hydro	1986	10	2,847	6.1	6.6
Photovoltaics	1986	7	3,200	13.1	13.4
CCPA Geothermal	1988	36	2,008	6.7	9.5
Combustion Turbine	1988	50	550	11.0	17.0
Others					
Coal	1990	250	2,500	5.4	6.1
Hydro	1990	300	2,700	10.4	10.5
Geothermal	1990	>70	2,100	6.8	9.6
Photovoltaics	1993	>100	3,200	13.1	13.4

PV Power Meets SMUD Load

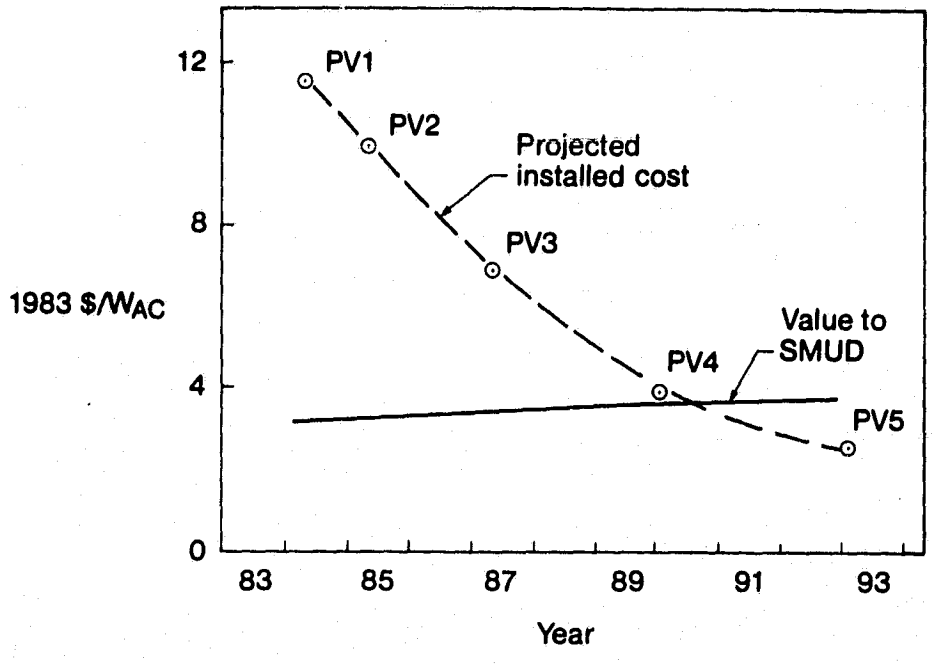


- Photovoltaics provide on-peak power

SMUD's PV Project

- The photovoltaic project continues SMUD's tradition of innovation.
- The value of photovoltaic power to SMUD is $3,200/kW (1983 $).
- SMUD's resource plan includes 100 MW of photovoltaic power by 1993.

Cost and Value of PV Power



SESSION III

DESIGNING FOR ARRAY SAFETY

R.S. Sugimura, Chairman

OMIT TO P.167

SESSION III

DESIGNING FOR ARRAY SAFETY

Chairman: R.S. Sugimura, Jet Propulsion Laboratory

SUMMARY

This session consisted of six presentations that examined array safety from three different perspectives: the utility perspective, which summarized the Sacramento Municipal Utility District (SMUD) policy toward fire, security, and electrical safety; a historical overview, which summarized dc wiring-system grounding techniques and ground-fault protection systems used in large PV arrays sponsored by the U.S. Department of Energy (DOE); and four presentations that addressed specific grounding and fault-protection issues. These issues included: the use of step-and-touch potential calculations to limit hazardous voltages; the capability and suitability of various types of industrial dc power switchgear for control and protection; the details of SMUD PV1 grounding and fault-protection systems; and the design tradeoffs associated with the need for a standard ground mat for the array subfield.

The first presentation, by B. Dilts of SMUD, addressed "Utility Policy Toward Electrical and Fire Safety and Security." SMUD's approach to electrical safety was to implement presently established safety standards. This resulted in the use of stringent design guidelines that required, for example, standard ground mats for the array field in accordance with IEEE-80. Other examples included complex and costly methods for bonding underground or buried connections using exothermic welds. Based on these experiences, plans for the remaining phases will consider the implementation of more flexible standards to provide cost-effective safety systems that maintain a level of safety consistent with utility practice. This approach includes evaluating the use of alternate ground-connection techniques and including the 1000 pier foundations as part of the grounding calculations.

For SMUD PV1, fire from external sources is considered an unlikely event, although future phases may have to consider means of preventing brush or grass accumulation that may create a fire hazard.

Security measures reflect SMUD's concern for the safety of untrained persons that might wander onto the site, and the protection of plant equipment. A security fence with perimeter alarms is to be provided, along with security response teams that can be at the site in less than 30 minutes.

Additional plans for future phases include using surface or above-ground wiring, instead of underground wiring, to obviate trenching with a back hoe. The cable ways will be about two inches deep by four inches wide, using slip-form construction.

The second presentation, by [illegible]. Simburger of Aerospace Corp., identified major "Dc Wiring System Grounding and Ground-Fault Protection Issues for

Central Station Photovoltaic Power Plants." Although there appears to be no consensus on the choice between solid and resistance grounding, presently deployed large photovoltaic arrays are using center-tap-grounded dc wiring systems connected by a neutral conductor to a single-point ground. The majority of the discussion portion of the presentation centered on the pros and cons of a resistance-grounded circuit as used in the SMUD design. The circuit consists of a 40K resistor in parallel with a 1K resistor wired so that the 1K resistor can be removed from the circuit before allowing maintenance workers into the array field. In this configuration the fault current is limited to 25 mA. Personnel protection is predicated on two assumptions: that there are no other ground faults in the circuit, and that access to the array field is limited to trained persons.

The issue of using procedures to protect personnel rather than relying on ground-fault protection was considered an economic tradeoff between the cost of the ground-fault protection equipment and the costs associated with time to perform maintenance activities, estimated to be three to four times longer, with the lines hot. The consensus was that the level of safety afforded to maintenance workers was the same in either case.

The third presentation, by W.J. Stolte of Bechtel Group, Inc., addressed "Photovoltaic System Grounding and Fault Protection." The approach was to limit hazardous voltages by providing a ground system that would provide a safe path for fault currents. Maximum allowable step-and-touch potentials and the site-specific soil resistivity were used to calculate the time required for a fault device to clear.

The discussion portion of this presentation dealt with step-and-touch potentials and the need for a ground mat under the array. The consensus was that dc fault currents expected from an array are so small that dc step-and-touch potentials are not a problem. The problem is with the ac system, due to the power conditioner being situated in the center of the array subfield (as is the case with almost all current central-station designs). This results in subtransmission ac voltage being brought right to the center of an array subfield. Since standard utility practice is to have a Y-grounded transformer, the ac system is tied to the ground mat in the array subfield. The alternative, a completely undergrounded ac system, is considered unsafe from the utility viewpoint.

It was pointed out that even without a ground mat, a ground system still exists. This consists of the array support structures, rebar-reinforced concrete foundations spaced at approximately 36-foot intervals in the case of SMUD.

Additionally, a possible benefit seen at the ARCO facility at Lugo, which has a center-tapped ground system through a 10-ohm resistor, is flow of both positive and negative currents into the ground mat. The ground mat appears to minimize mismatch losses by balancing current throughout the array subfield, resulting in a current of 1/10 amp, as opposed to 5 to 10 amps.

The fourth presentation, by N.A. Marshall of Hughes Aircraft Co., titled "Electrical Safety for High Voltage Arrays," summarized the capability and suitability of various types of industrial dc power switchgear for control

and fault protection. Three different classes of disconnect devices addressed were: the cold disconnect, load interrupters and fault interrupters. Under the cold disconnects, Amp Solarlok connectors were mentioned, along with the fact that any ac circuit breaker could be used as long as open-circuit voltage is present during the disconnect operation. An example of load interrupters consisted of a device that magnetically and thermally manipulated the arc to assure a reliable interrupt. The fault-interrupters example provided was a fast-acting, high-voltage dc fuse, basically a fusable link with precisely established melt-and-clear characteristics.

In summary, a limited selection of appropriate cost-effective dc power switchgear exists. In response to a question concerning specific costs, several examples were provided: a 1000-SA dc contactor costs $385 to $400; fuses cost $80 to $90 apiece; and the smaller contactors vary all the way from $40 to $400.

The other two points dealt with dc bus voltages. For larger dc power systems, the designer will have to accept increased resistive losses--that is, I^2R losses will increase. On the other hand, if bus voltages are above 1000 volts dc, higher-rated dc devices are required, and some needed devices, such as high-voltage dc fuses, may not presently exist.

The fifth presentation, by D. Rosen of Acurex Corp., addressed "Grounding and Fault Protection of the SMUD PV1 Array," and provided design details that accommodated SMUD's standard design practices while providing some unique solutions to problems of ground-fault protection and detection.

The discussion portion of this presentation dealt with two areas: the impact on system cost because of the need for the insulation system to be rated at 1000 volts, and how the ground-fault system is used to locate a ground fault anywhere in the array field.

With the SMUD design, the principal effect of a high system voltage is on the cost of the module encapsulation system. Because of the very limited number of contactors in the system, the total cost difference between the 600-volt and 1000-volt or 1500-volt contactors is very small. As mentioned in an earlier session, the cost impact of increasing cable ratings from 600 volts to 1000 volts is also very small. The biggest uncertainty is in the area of the module encapsulation system and, from earlier talks, it appears that more research is needed to understand the behavior of encapsulation materials undergoing voltage stress.

Ground-fault location techniques consist of two approaches. The first is to inject an ac signal onto the neutral to detect a ground fault on the neutral itself. The second is to monitor the dc voltage across the neutral to sense ground faults along the source circuits. Since a ground fault occurring along a source circuit will cause the neutral point to rise to a dc voltage equal to the product of the module (panel) voltage and the number of modules (panels) between the neutral and the fault, the position of the fault with respect to neutral can be determined.

At this point it is necessary to go into the field to locate the array that has the fault. Two techniques are envisioned. The first involves a common cable fault-locating approach in which an ac signal is injected onto the cable and then a magnetic pickup is used to follow the signal until it disappears at the fault location. The other approach is a little more cumbersome and involves disconnecting arrays from ground and monitoring when the neutral voltage goes away.

In response to a question regarding panel removal: the approach is to open-circuit the plus and minus polarities of the subfield from the rest of the field and the inverter and put the system in the so-called maintenance mode, which is the high-resistance mode that limits the ground-fault current in that subfield to something on the order of 10 mA. The panel can now be removed safely, since the small amount of current can now be interrupted by the quick disconnects.

The last presentation, by G.R. Engmann of Black & Veatch Engineers-Architects, was titled "Photovoltaic Central Station Grounding System Design Requirements." The need for an array-field ground-pad configuration was questioned because PV array fields are essentially distributed energy sources and therefore result in very low energy densities. Although the use of conventional substation grounding techniques for areas of major power concentrations and within the area of the substation was advocated, other areas, such as the array fields, were considered likely candidates for eliminating the ground mat. By utilizing the structural contact with earth from the array support foundations, an adequate ground system could be provided. A relatively strong case was presented by emphasizing that the risk of hazardous step-and-touch potential in an array field is comparable to the risk in areas just outside the major structures of a steam generating station and in areas adjacent to a substation situated in a residential district where a fence that is surrounding a substation may not be tied to that substation grid.

DP
omit

UTILITY POLICY TOWARD ELECTRICAL AND FIRE SAFETY AND SECURITY

SACRAMENTO MUNICIPAL UTILITY DISTRICT

Bryan Dilts

The utility industry has a history of maintaining safe, secure facilities although energy sources are by nature hazardous. This is achieved through implementation of established standards of safety and security. With each new generation source come new concerns for safety and security that may not be resolved by application of existing standards. The SMUD PV1 power plant has several significant differences for which the utility has proposed solutions.

Electrical Safety

Due to the distributed nature of solar energy, grounding and protection techniques applicable to conventional generation facilities may not be appropriate. In PV1, SMUD has elected to apply standards of grounding that limit step-and-touch potentials through the use of standard ground mats. In future phases, however, SMUD plans to perform an evaluation of that grounding requirement and of the foundations as grounding electrodes.

Protection of persons and equipment is important because of the distributed nature of the field. Access is limited to cognizant persons, however, and protection may be analyzed from an economic basis as well. The solutions for SMUD PV1 are innovative and are discussed in some detail.

Fire Safety

The danger of fire in the array field for SMUD PV1 is limited. There is no possibility of fire from external sources; thus only equipment protection to avoid fire-causing circumstances need be considered. In future phases, however, the field will have to be mowed annually to avoid the possibility of grass or brush fires spreading to the site. The control building is equipped with fire extinguishers.

Security

The distributed nature of the field is such that security must be maintained to keep untrained persons out of the site. The SMUD PV1 field is equipped with a security fence as well as perimeter detection alarms. Security will respond in under 30 minutes to any intrusion. This approach will limit the possibility of an untrained person entering the site and causing damage to himself or the plant equipment.

D/2

DC Wiring System Grounding and Ground Fault Protection Issues for Central Station Photovoltaic Power Plants

Edward J. Simburger
The Aerospace Corporation
Los Angeles, California

The DC wiring system for a photovoltaic power plant presents a number of unique challenges to be overcome by the plant designers. There are a number of different configurations that the grounding of the DC wiring system can take, and the choice will affect the number and type of protective devices required to ensure safety of personnel and protection of equipment. Figure 1 summarizes the major grounding and fault protection considerations that must be taken into account when selecting the basic overall circuit configuration.

The small-scale (residential) and intermediate-sized systems deployed under the DOE-funded demonstration projects have used many different types of circuit configuration. On the other hand, all of the conceptual designs developed to date for central station photovoltaic power plants utilize a center-tap-grounded DC wiring system with nominal operating voltage of ± 1000 VDC. The central station photovoltaic power plants under construction or in operation in the U.S. also utilize a center-tap-grounded DC wiring system but have operating voltages in the range of ±250 VDC to ± 350 VDC. Figure 2 summarizes the location of the DC wiring system circuit ground for the largest experiments fielded to date and for large central station conceptual designs. Figure 3 summarizes the system design considerations which led designers to select center-tap wiring systems for central station applications.

A system that uses a center-tap ground can be either resistance grounded or solidly grounded, as indicated in Figure 4. Each method has some advantages and disadvantages with respect to personnel safety, equipment protection, and appropriate operating environments for the various components that make up the plant. The issues of interest include the level of shock hazard to personnel from ground faults, the level of damage that can be sustained by plant equipment during ground faults, the location and method of ground fault detection, the necessity of ground fault interruption equipment, the standoff insulation level for plant equipment, and the operating and maintenance procedures for the particular plant. As illustrated in Figure 5, protection of personnel and equipment from ground faults in a photovoltaic system can be implemented by either interrupting the fault current or by limiting the fault current to levels tolerable to both personnel and equipment. Figures 6 through 8 illustrate the various configurations (individual grounding of source-circuit center taps or single point grounding via a neutral conductor) that solid or resistance grounded systems can take and indicate the location of protection equipment that would be required for each circuit configuration.

The inherent advantages and disadvantages of each type of circuit grounding (resistance or solid) along with the personnel safety and equipment protection issues for each of these grounding methods are presented in this paper.

Solidly Grounded Circuits

The center taps of the source circuits can be connected directly to the ground mat individually. The apparent advantages and disadvantages of this approach are shown in Figure 10. The mismatch losses between the positive and negative halves of the subfield are minimized because the ground connection allows a path for mismatch currents to flow between the positive and negative halves of individual source circuits. If ground fault interruption is provided for the individual source circuits, the presence of a ground fault would not require immediate (within 4 to 8 hours) attention by maintenance personnel. Instead, corrective action could be postponed until a period of routine maintenance. The presence of significant DC currents flowing in the ground mat could pose a corrosion problem for any buried metals, structural components, or the conductors that compose the ground mat itself. Harmonic currents that are generated by the power conditioning unit and flow through the ground mat may cause problems for control, instrumentation, and communication circuits that utilize the ground mat for ground reference. Since the magnitude of a ground fault current would be equal to at least the short circuit current of an individual source circuit and could be as high as the short circuit current of the entire subfield, depending upon the location of the ground fault, some form of ground fault interruption would be required to protect personnel and equipment.

Another method of solidly grounding the source-circuit center taps would be via a neutral conductor which is connected to the ground mat at a single point. As shown in Figure 10, this method would have all of the advantages of the previous method, at the expense of having some additional field wiring, and would avoid the disadvantages associated with having multiple connections between the source-circuit center taps and the ground mat.

Resistance-Grounded Source Circuits

The center taps of the source circuits can be connected to the ground via individual resistors. The apparent advantages and disadvantages of this approach are shown in Figure 11. The presence of a fairly large impedance between the center tap of each source circuit and the ground mat would prevent mismatch currents between the positive and negative halves of the source circuits from flowing through the ground mat and would thereby increase the overall mismatch losses. These impedances, however, would eliminate the disadvantages associated with multiple connections between the source-circuit center taps and the ground mat. Ground fault protection for personnel and equipment would be dependent upon the current-limiting features of the high impedance connection to the ground mat, and the presence of a single ground fault in the array field would make this method of ground fault protection ineffective. A method of effectively detecting ground faults would therefore be required, and correction of the ground fault by maintenance personnel as soon as practical would be necessary in order to maintain the integrity of the ground fault protection system. While the voltage stress to ground would be limited to one-half the open

circuit line-to-line voltage during normal operations, the maximum voltage stress to ground could be as high as the full line-to-line open circuit voltage during the occurrence of a ground fault on one of the poles.

A neutral conductor can also be utilized in a resistance grounded system and would have the advantage of requiring only one grounding resistor and surge protection device for an entire subfield. It would also have the other advantages listed in Figure 11 for the individual source circuit resistance grounding scheme, at the expense of some additional field wiring. Additionally the neutral conductor would provide a conducting path between the positive and negative halves of the subfield that would minimize mismatch losses.

Effective ground fault detection may be difficult in a resistance grounded system when the grounding resistor is sized to protect personnel. Since the small currents that are tolerable by personnel are comparable to currents associated with externally generated noise and transients, a large number of nuisance ground fault indications would be expected in such a system. Equipment, however, can tolerate currents that are well above the noise threshold. A system using a dual-valued grounding resistor, as shown in Figure 12, could satisfy these conflicting reqirements by providing a small resistance (and good ground fault detection) when personnel are absent and a much larger resistance when personnel are present.

Figures 13 and 14 summarize the experience with ground faults and ground fault detecting equipment that has been gained at the Lovington and Sky Harbor DOE-funded intermediate-scale experiments.

Conclusions

As a result of examining the various advantages and disadvantages of the four basic methods of connecting the DC wiring system center tap to ground, it is felt that the use of a neutral conductor would be justified because of the problems it eliminates for either solid or resistance grounding of the source circuits. The cost penalty incurred because of the additional field wiring required should be minimal and would be more than offset by increased performance and reduced maintenance costs.

It is more difficult to identify a clear-cut winner with respect to the choice between solid and resistance grounding. At present, resistance grounded systems have an advantage because of the current unavailability of cost-effective DC switchgear with the voltage and current ratings required for interruption of ground faults at the source circuit level. However, such switchgear could be developed if there were sufficient market to warrant production. The trade-offs would then be between the additional equipment needed for the solidly grounded system, as shown in Figure 15, and the additional maintenance and higher voltage withstand requirement for the resistance grounded system. Thus the final resolution as to the preferred method of connecting the DC wiring system center taps to ground will probably not be found in the near future.

DC WIRING SYSTEM GROUNDING AND GROUND-FAULT PROTECTION ISSUES FOR CENTRAL-STATION PHOTOVOLTAIC POWER PLANTS

AEROSPACE CORP.

Edward J. Simburger

Figure 1. What Are the Circuit Grounding and Fault Protection Considerations for Large Arrays?

- MAJOR SAFETY ISSUES
  - PERSONNEL SAFETY
  - EQUIPMENT SAFETY
- MAJOR CONSIDERATIONS FOR CIRCUIT TOPOLOGY
  - LOCATION OF GROUND CONNECTION IN THE CIRCUIT
  - METHOD OF CONNECTING THE CIRCUIT TO GROUND
- MAJOR PROTECTION SYSTEM FUNCTIONS
  - OVERCURRENT / REVERSE-CURRENT-PROTECTION
  - OVERVOLTAGE / SURGE PROTECTION
  - PROTECTION OF PERSONNEL FROM DANGEROUS CURRENTS

Figure 2. What Is the Optional Location of the Circuit Ground?

- THE LOVINGTON, BEVERLY HIGH SCHOOL, AND SKY HARBOR INTERMEDIATE-SIZED PROJECTS USE ONE-POLE-GROUNDED DC WIRING SYSTEMS
- THE SMUD, ARCO LUGO, AND ARCO CARRISA PLAIN CENTRAL-STATION PROJECTS USE CENTER-TAP-GROUNDED DC WIRING SYSTEMS
- ALL CENTRAL STATION CONCEPTUAL DESIGNS UTILIZE CENTER-TAP-GROUNDED DC WIRING SYSTEMS (Black and Veatch, Martin-Marietta, Aerospace)

Figure 3. What Considerations Led Designers to Select Center-Tap Dc Wiring Systems for Central-Station Applications?

- PERSONNEL SAFETY
- MINIMUM CIRCUIT VOLTAGE TO GROUND
- MINIMUM i^2R LOSSES
- MINIMUM MISMATCH LOSSES
- MINIMUM MAGNITUDE OF GROUND FAULT CURRENTS

Figure 4. What Are the methods of Connecting the Circuit Center Tap to Ground?

- SOLID GROUNDING OF INDIVIDUAL SOURCE CIRCUITS
- SINGLE POINT SOLID GROUNDING via A NEUTRAL CONDUCTOR
- RESISTANCE GROUNDING OF INDIVIDUAL SOURCE CIRCUITS
- SINGLE POINT RESISTANCE GROUNDING via A NEUTRAL CONDUCTOR

Figure 5. Personnel and Equipment Protection Options

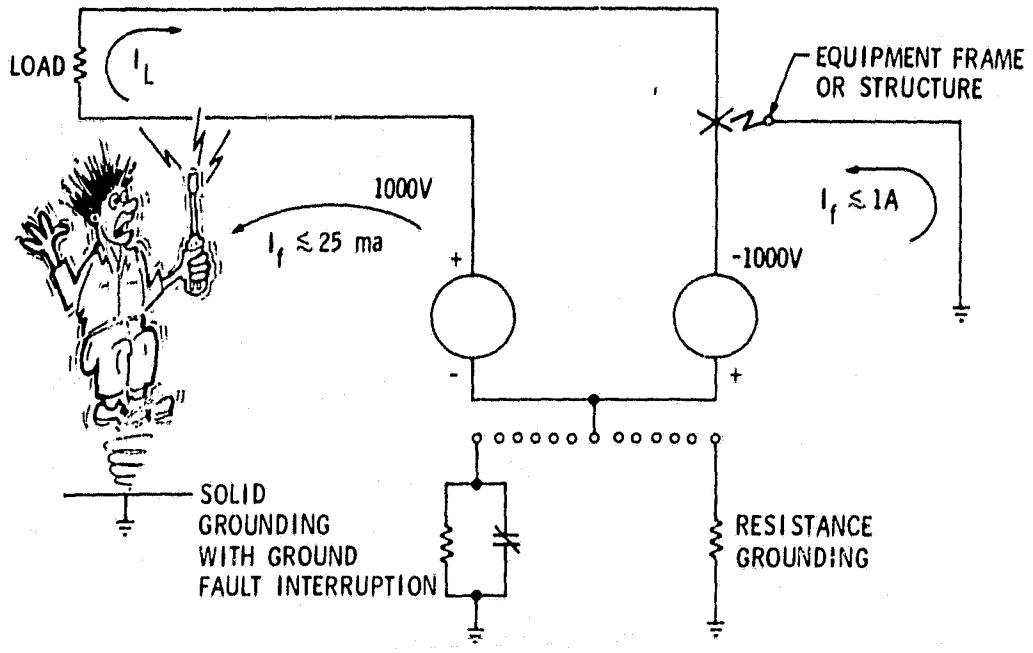


Figure 6. Dc Wiring System With Solid Grounding of Individual Source Circuits

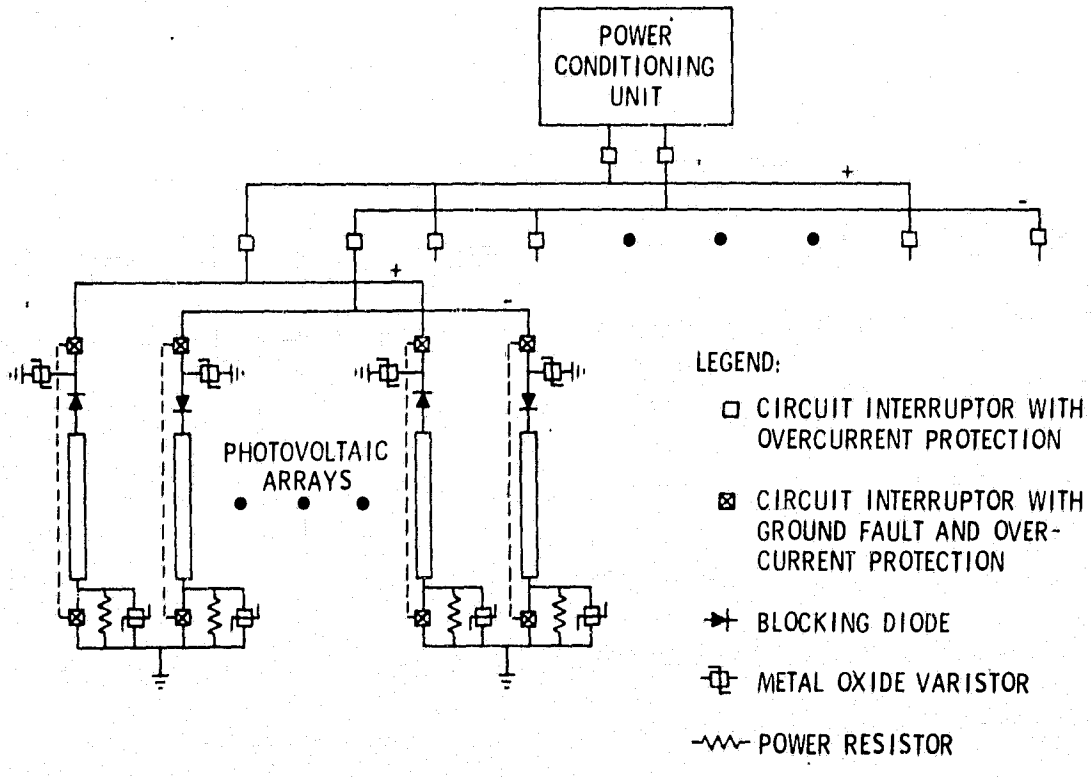


Figure 7. Dc Wiring System With Single-Point Solid Grounding by a Neutral Conductor

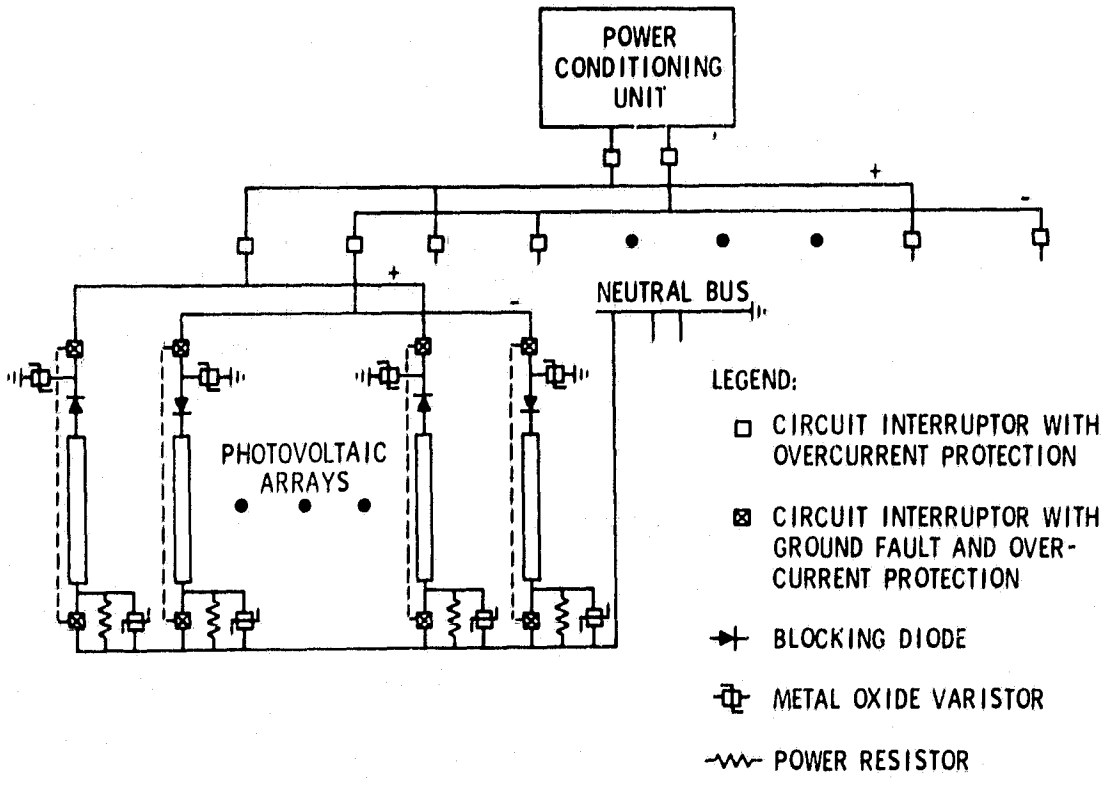


Figure 8. Dc Wiring System With Resistance Grounding of Individual Source Circuits

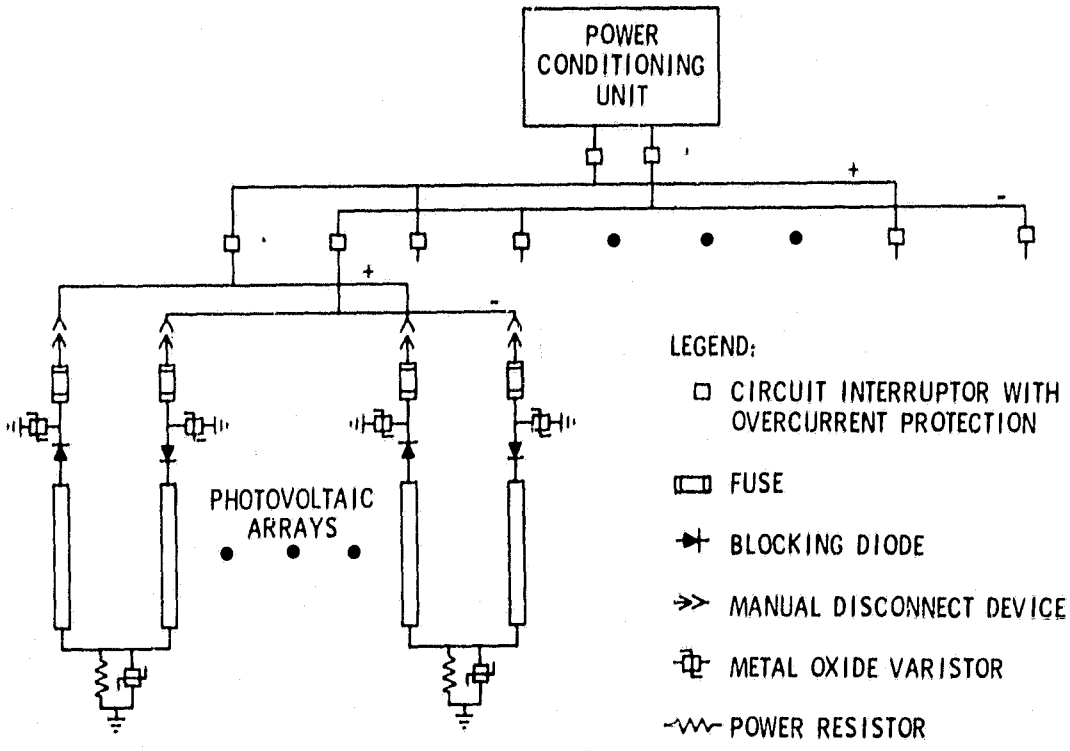
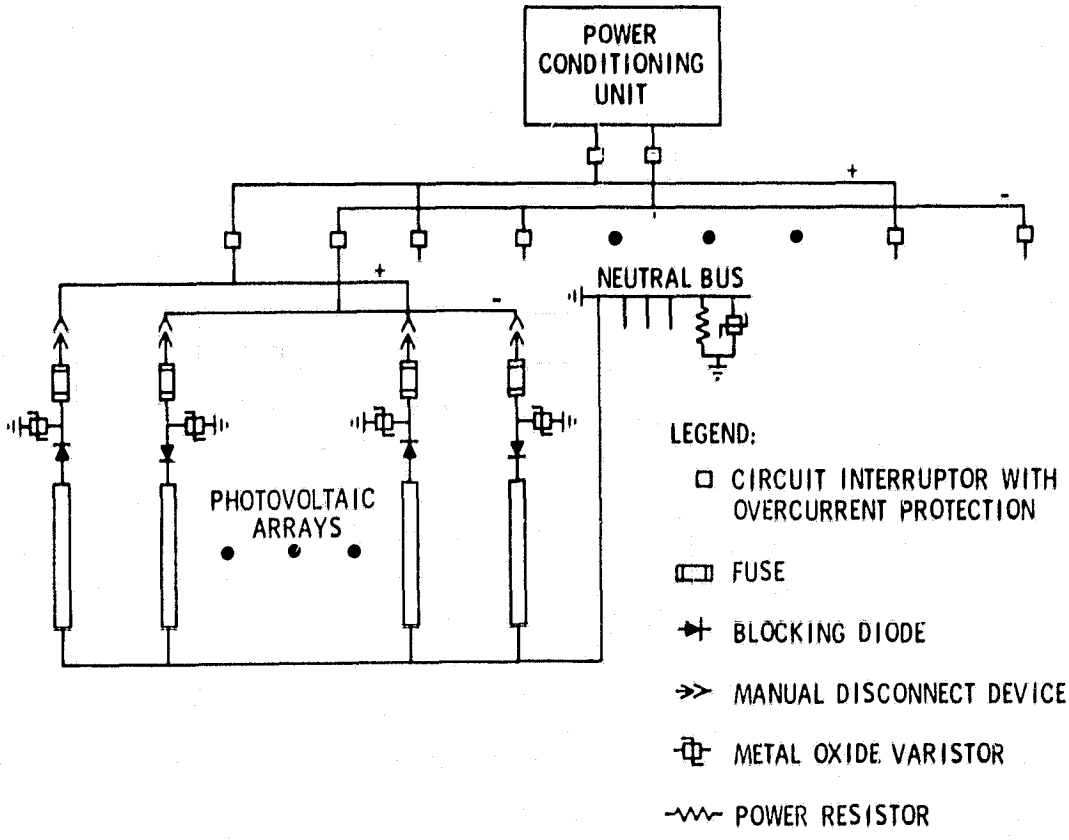


Figure 9. Dc Wiring System With Single-Point Resistance Grounding by a Neutral Conductor



Figures 10 and 11. Advantages and Disadvantages of Various Methods of Connecting Circuit Center Tap to Ground

TYPE OF GROUND CONNECTION	ADVANTAGES	DISADANTAGES
SOLID GROUNDING OF INDIVIDUAL SOURCE CIRCUITS	• MINIMIZES FIELD WIRING • MINIMIZES MISMATCH LOSSES • GROUND FAULTS WOULD NOT REQUIRE IMMEDIATE ATTENTION BY MAINTENANCE (if ground fault interruptor is provided) • LIMITS THE MAXIMUM VOLTAGE TO GROUND TO 1/2 OF THE LINE-TO-LINE OPEN CIRCUIT VOLTAGE	• ALLOWS MULTIPLE PATHS THROUGH THE GROUND MAT FOR ARRAY-GENERATED DC CURRENTS • ALLOWS MULTIPLE PATHS THROUGH THE GROUND MAT FOR HARMONIC CURRENTS GENERATED BY THE PCU • MAGNITUDE OF GROUND FAULT CURRENTS CAN BE AS HIGH AS THE SUBFIELD SHORT CIRCUIT CURRENTS (ground fault interruptor required)
SINGLE POINT SOLID GROUND via A NEUTRAL CONDUCTOR	• MINIMIZES MISMATCH LOSSES • GROUND FAULTS WOULD NOT REQUIRE IMMEDIATE ATTENTION BY MAINTENANCE (if ground fault interruptor is provided) • LIMITS THE MAXIMUM VOLTAGE TO GROUND TO 1/2 OF THE LINE-TO-LINE OPEN CIRCUIT VOLTAGE	• SOME ADDITIONAL FIELD WIRING REQUIRED • MAGNITUDE OF GROUND FAULT CURRENTS CAN BE AS HIGH AS THE SUBFIELD SHORT CIRCUIT CURRENTS (ground fault interruptor required)

TYPE OF GROUND CONNECTION	ADVANTAGES	DISADVANTAGES
RESISTANCE GROUNDING OF INDIVIDUAL SOURCE CIRCUITS	• MINIMIZES FIELD WIRING • LIMITS THE MAGNITUDE OF GROUND FAULT CURRENTS	• REQUIRES A SEPARATE GROUNDING RESISTOR FOR EACH SOURCE CIRCUIT • INCREASES OVERALL MISMATCH LOSSES IN SUBFIELD • REQUIRES EFFECTIVE GROUND FAULT DETECTION AND IMMEDIATE ATTENTION BY MAINTENANCE IN THE EVENT OF A GROUND FAULT • MAXIMUM VOLTAGE TO GROUND IS THE SAME AS THE LINE-TO-LINE OPEN CIRCUIT VOLTAGE
SINGLE POINT RESISTANCE GROUNDING via A NEUTRAL CONDUCTOR	• MINIMIZES MISMATCH LOSSES • LIMITS THE MAGNITUDE OF GROUND FAULT CURRENTS • REQUIRES ONLY ONE GROUNDING RESISTOR FOR ENTIRE SUBFIELD	• SOME ADDITIONAL FIELD WIRING REQUIRED • REQUIRES EFFECTIVE GROUND FAULT DETECTION AND IMMEDIATE ATTENTION BY MAINTENANCE IN THE EVENT OF A GROUND FAULT • MAXIMUM VOLTAGE TO GROUND IS THE SAME AS THE LINE-TO-LINE OPEN-CIRCUIT VOLTAGE

Figure 12. Protection for Personnel and Equipment in Resistance-Grounded Systems

- GROUND FAULT CURRENTS OF 25 mA MAXIMUM TO PROVIDE PROTECTION FOR PERSONNEL
- HIGH-IMPEDANCE GROUNDING RESISTORS MAKE GROUND FAULT DETECTION DIFFICULT AND CAN DECREASE THE NOISE IMMUNITY OF THE INSTRUMENTATION CONNECTED TO THE ARRAY
- EQUIPMENT CAN TOLERATE GROUND FAULT CURRENT MANY TIMES HIGHER THAN PERSONNEL CAN

A DUAL-VALUED GROUNDED RESISTOR CAN SATISFY THE NEEDS OF BOTH PERSONNEL SAFETY AND EQUIPMENT PROTECTION

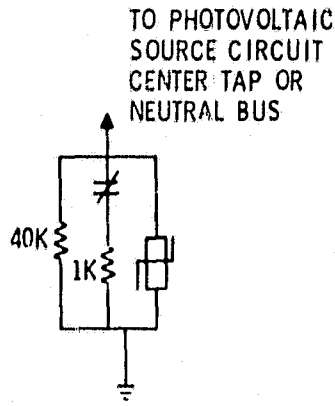


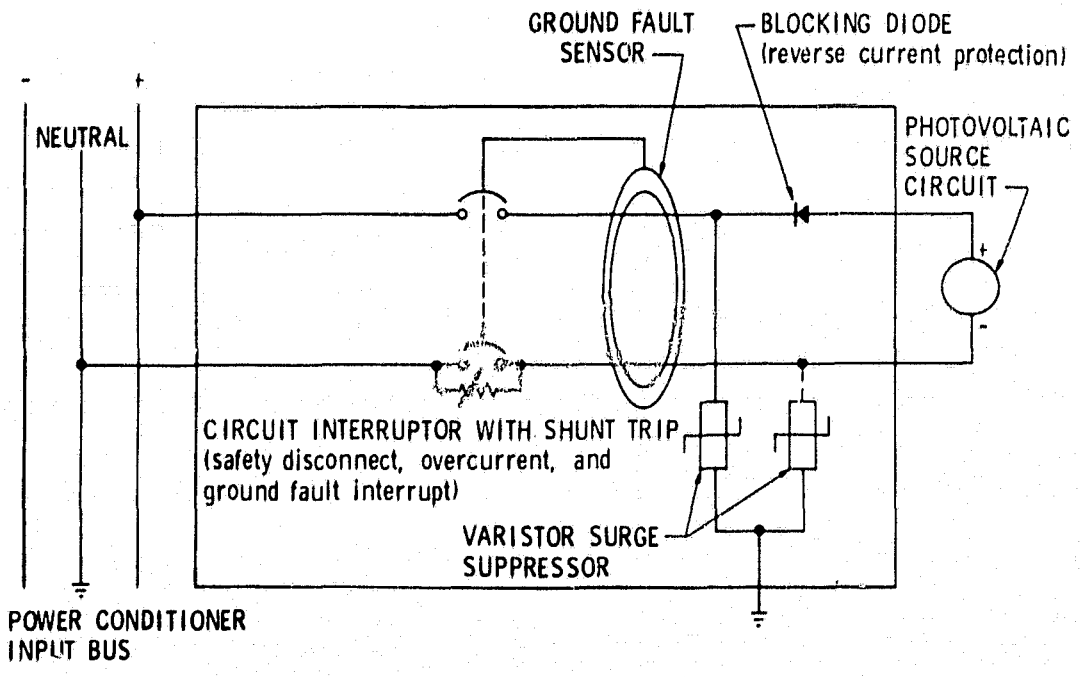
Figure 13. Lovington Experience With Ground Fault Interrupt (GFI) System

- PRIMARY ROLE OF GFI IS PERSONNEL PROTECTION
  - NUMEROUS UNDOCUMENTED (GFI) TRIPS HAVE BEEN CAUSED BY MAINTENANCE PERSONNEL DURING TESTING AND MAINTENANCE OF THE ARRAY
- VERN RISSER ESTIMATES THAT THERE HAVE BEEN BETWEEN 12 AND 20 GFI TRIPS PER YEAR
- FOR THE MONTHS OF APRIL, MAY AND JUNE 1982 THERE WERE 10 DOCUMENTED GFI TRIPS
- MOST GFI INITIATED OUTAGES WERE RESET WITHOUT ANY CORRECTIVE ACTION (most are of the nuisance type)
- THE MAJORITY OF GROUND FAULT TRIPS OCCUR DURING WET WEATHER

Figure 14. Sky Harbor Experience With Ground Faults

- ORIGINAL DESIGN FOR SKY HARBOR PROJECT CALLED FOR A 1000 OHM RESISTANCE GROUND WITH GROUND FAULT INDICATION
- WITH THE RESISTANCE GROUND, A GROUND FAULT IN THE ARRAY CAUSED DAMAGE TO PARTS OF THE INSTRUMENTATION SYSTEM
- SINGLE POINT SOLID GROUNDING SOLVED THE INSTRUMENTATION SYSTEM PROBLEM
- THERE HAVE BEEN 60 TO 75 GROUND FAULTS DURING THE FIRST 18 MONTHS OF OPERATION
  - 15 DUE TO INFANT MORTALITY OF CELLS
  - 45 DUE TO ARCING OF BYPASS DIODES TO GROUND WHEN MOISTURE GETS INSIDE THE MODULE
  - ONE DUE TO A BLOCKING DIODE FAILURE (fault current was over 700 A)
- AN AVERAGE OF 2 MAN HOURS OF MAINTENANCE TIME WAS EXPENDED TO REPAIR EACH OF THE GROUND FAULTS
- THERE ARE PLANS TO IMPLEMENT A GROUND FAULT DETECTION SYSTEM THAT WOULD INITIATE A PCU SHUTDOWN AND STOW THE ARRAYS WHEN GROUND FAULT CURRENTS EXCEED 40 TO 45 AMPERES

Figure 15. Source-Circuit Interface



PHOTOVOLTAIC SYSTEM GROUNDING AND FAULT PROTECTION

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San Francisco, CA 94119

Under contract to Sandia National Laboratories, Bechtel is conducting a study of the grounding and fault protection aspects of large photovoltaic power systems. Broadly, the overlapping functions of these two plant subsystems include providing for the safety of personnel and equipment.

Grounding subsystem design is generally governed by considerations of personnel safety and the limiting of hazardous voltages to which they may be exposed during the occurrence of a fault or other misoperation of equipment. A ground system is designed to provide a safe path for fault currents. Metal portions of the modules, array structures, and array foundations can be used as a part of the ground system, provided that they and their interconnection are designed to be suitably reliable over the life of the plant. Deterioration effects, such as chemical and electrolytic corrosion, must be taken into account in the design process. Site soil resistivity is a major design factor which also must be accommodated.

The electrical protection subsystem can include both passive and active devices to protect personnel and equipment. Some protection devices, such as surge arrestors, also require connection to a suitable grounding subsystem for proper operation. Several alternative types of fault protection and detection equipment can be designed into the source circuits and dc buses feeding the input terminals of the subfield power conditioner. This design process requires evaluation of plausible faults, equipment, and remedial actions planned to correct faults. The evaluation should also consider life cycle cost impacts.

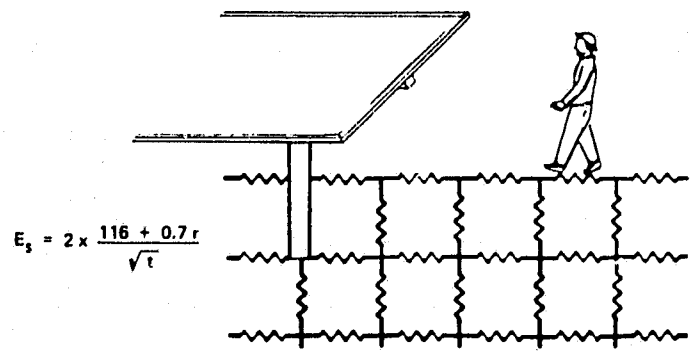
C-3

PHOTOVOLTAIC SYSTEM GROUNDING AND FAULT PROTECTION

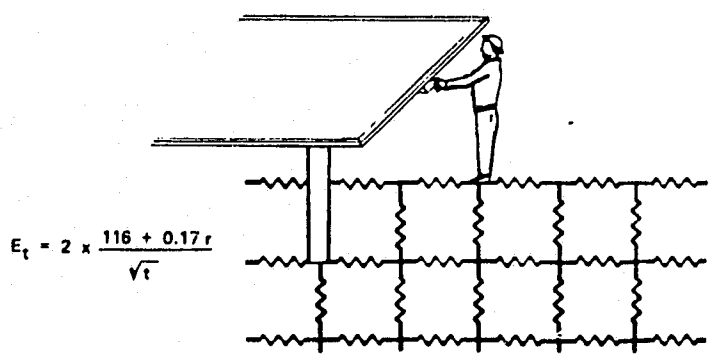
BECHTEL GROUP, INC.

W.J. Stolte

Step-and-Touch Potentials



$$E_s = 2 \times \frac{116 + 0.7\,r}{\sqrt{t}}$$



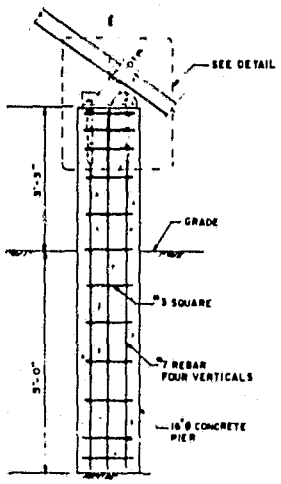
$$E_t = 2 \times \frac{116 + 0.17\,r}{\sqrt{t}}$$

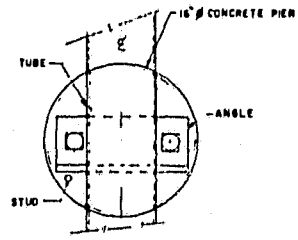
r = SOIL RESISTIVITY (NEAR SURFACE)

$0.008 < t < 5$ sec.

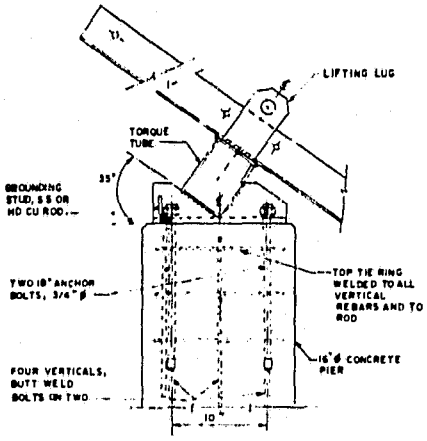
Flat-Plate Array Foundation

FOUNDATION AND ASSEMBLY ELEVATION:

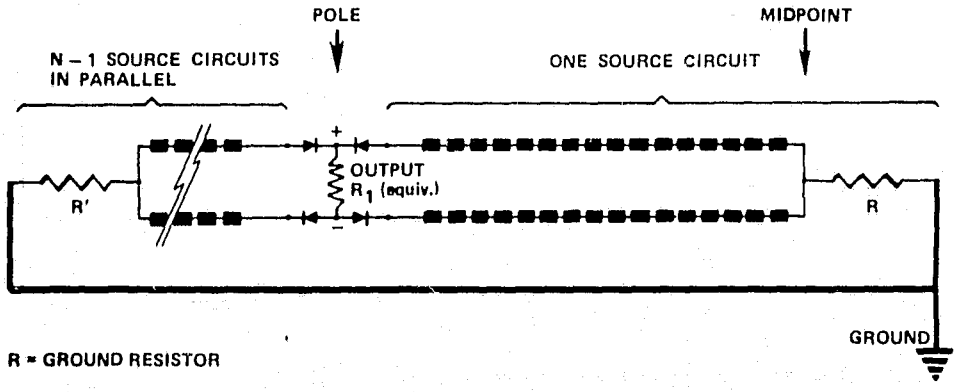




TOP VIEW



Array Subfield Equivalent Circuit

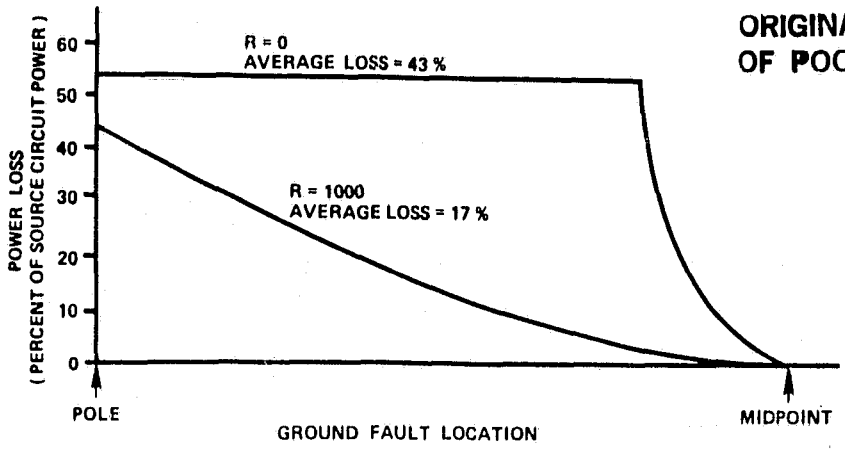


R = GROUND RESISTOR

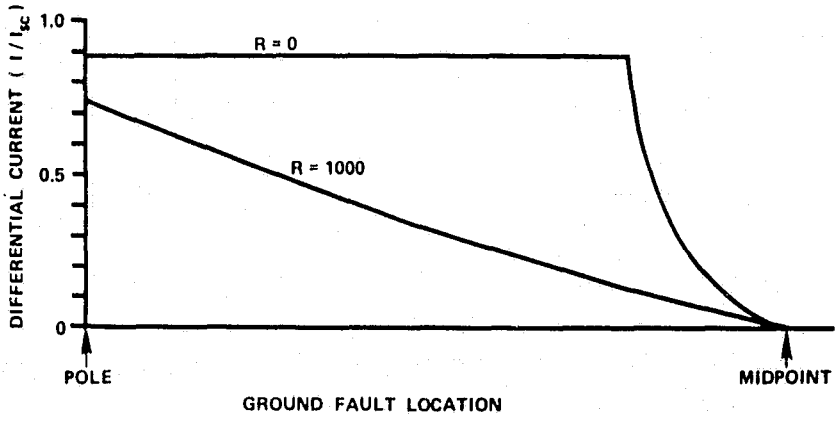
$R' = R / (N - 1)$

$$R_1 = \frac{V_{\text{source circuit @ max. power}}}{N \times I_{\text{source circuit @ max. power}}}$$

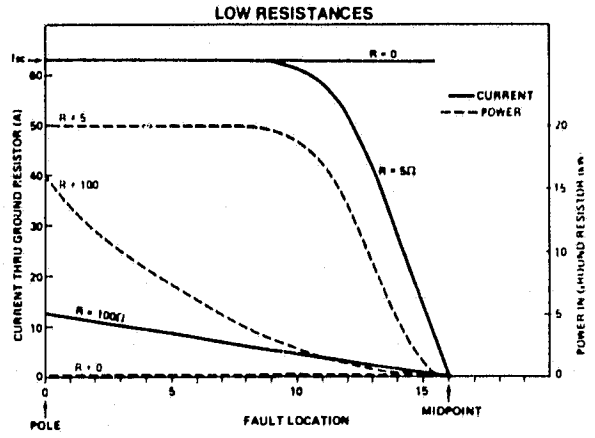
Power Lost in Subfield Due to Short to Ground in One Source Circuit

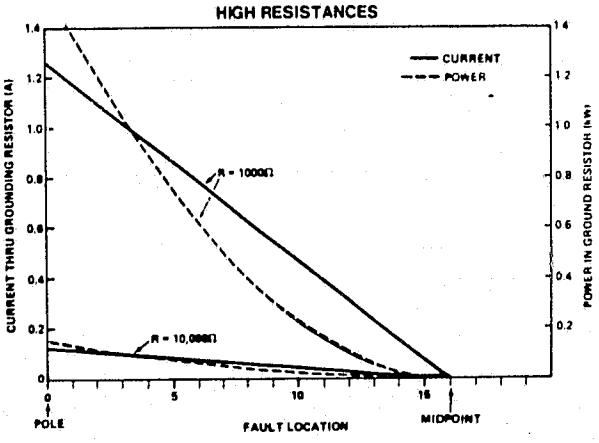


Differential Current at the Terminals of a Source Circuit With a Short to Ground

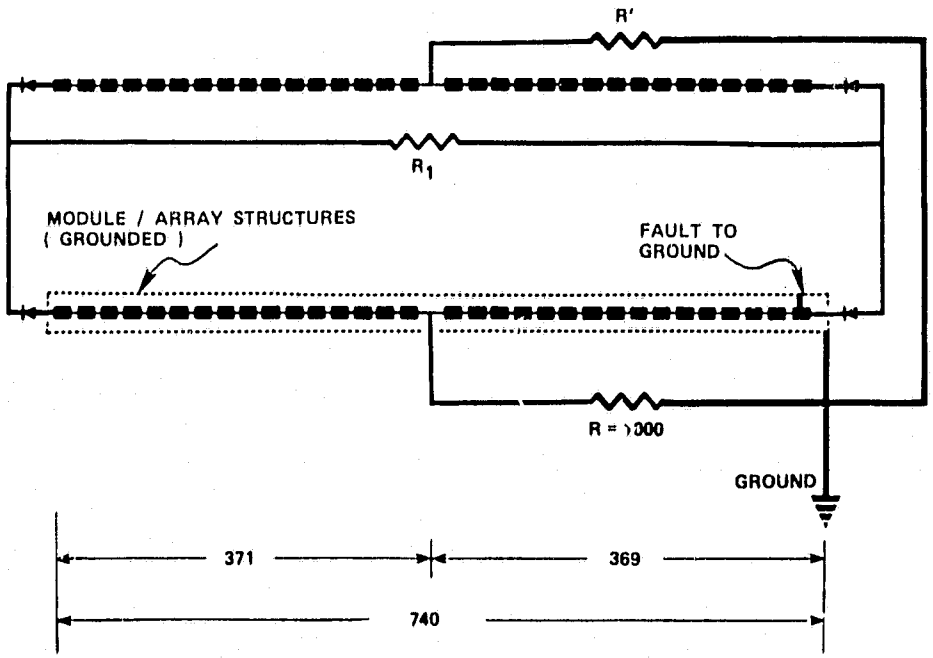


Current and Power Through Midpoint Grounding Resistor With Load Removed (Open Circuit) and Fault to Ground





Voltages for a Resistance-Grounded Source Circuit With a Fault Near One Pole



ELECTRICAL SAFETY FOR HIGH VOLTAGE ARRAYS

Neil A. Marshall
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This presentation explores a number of key electrical safety requirements for the high voltage arrays of central station photovoltaic power systems. The suitability of representative industrial DC power switchgear for control and fault protection was evaluated. Included were AC/DC circuit breakers, electromechanical contactors and relays, load interruptors, cold disconnect devices, sectionalizing switches, and high voltage DC fuses. As appropriate, steady state and transient characteristics were analyzed. Failure modes impacting upon operation and maintenance safety were also identified, as were the voltage withstand and current interruption levels.

Other papers in the Research Forum cover such topics as grounding, fault protection, insulation design, voltage breakdown, surge diversion, and DC wiring topologies. This discussion is however specifically directed toward examination of the power control capabilities of the types of DC switchgear and apparatus of concern in central station PV power.

To provide a comparison baseline, a peak DC bus voltage of one kilovolt has been assumed for a modular power building block of a megawatt. From Gonzales et. al. [1], a representative bipolar configuration would yield an Optimum Center Voltage (OCV) of + 325 VDC, and correspondingly, a maximum Open Circuit Voltage (VOC) of Tess than 1000 VDC.

The task of switching DC power becomes increasingly formidable as the voltage and current levels increase. Much higher DC voltages and currents are of course routinely involved in both electrical propulsion and bulk DC power transmission. For the present PV requirement however, increase of the stress levels, particularly voltage, much above the baseline values given, materially restricts available hardware in the marketplace.

Dynamically, the existence of a current zero is pivotal in the interdiction of power flow. In AC applications, if the interrupter contacts should open at the precise moment the current passes through zero, an arc would not form. This fortituous circumstance occur only infrequently because of the random timing of the switching event, and the presence of line inductance. At some point in the interuption process, even if asynchronous, an AC current reversal must take place.

DC current is however undirectional. Magnetic energy is stored in the circuit inductance, and upon interruption, the arc forms. The energy is ultimately converted to heat in the switching contacts and its surroundings. In DC air-magnetic circuit breakers and contactors, the arc is magnetically and thermally manipulated to assure reliable interruption and reduce erosion. The DC voltage must be higher than the system voltage for a period set by the current level, the inductance and the voltage differential. Otherwise, the resulting arc reignition can be of serious consequence to system safety. Other techniques for assurance of safe interruption of DC power include the use of capacitive counter-currents, snubbers, and related current commutation techniques to achieve a current zero.

The review draws extensively upon Hughes' experience in the design and installation of the 300 kW Photovoltaic Higher Education National Exemplar Facility (PHENEF) at the Georgetown University. The DC power collection field of this system features:

a. A bipolar ± 228VDC (OCV) array field consisting of 124 parallel bipolar strings, each rated at 5 ADC peak.

b. 30 kW pk power summing branches, ten in number, originating at a corresponding number of remote diode/CB panelboards. These panelboards in turn sum the current from up to 16 strings, a source circuit.

c. CB/Diode isolation down to each half-string or eighteen series modules.

d. Contactor/DC fuse protected branch terminations in the DC Power Collector Center.

Power system safety and freedom from systematic outages may be assured only if the protective elements have been properly selected and perform to specification. The switchgear attributes were examined in regard to those electrical stresses of the baseline system, as well as the Georgetown installation.

DC contactors in the smaller NEMA sizes (1 through 4) may be used in lower voltage and current applications, typically to 250 VDC and to 100 ADC. Permanent magnet blowouts must be included to assure contact survivability and positive load circuit interruption at rated DC current. The blowouts additionally provide an overload interruption capability limited to about 200% of steady state current. If the magnetic blowouts are not included, at maximum rated voltage, the safe current interruptions levels must be reduced by a factor of 15X-25X. Double-break, or series contacts, and electromagnetic blowouts producing increased magnetic flux for arc threading are alternatively used to achieve higher fault interruption levels.

As in the case of thyristor protection, various resistor-capacitor or diode-resistor-capacitor snubbers have been successfully employed in parallel with the interrupting contacts. These networks commutate the load current, thus permitting the dielectric between the parting gap to recover before the dv/dt capacitor reaches full charge. A virtually arcless interruption is thus assured.

The larger, definite-purpose contactors, NEMA size 7 to 900 amperes, are available from most major U.S. electrical manufacturers. They feature double-break contacts with permanent magnet blowouts, and are usually rated to 500 VDC. Under abnormal conditions, they will interrupt up to about 200% load current.

The most advanced DC contactors feature electromagnetic coil blowout, fault current-aided armature (make-and-latch) "hold-in", and highly developed refractory arc-chutes. These premier devices are produced by a number of U.S. manufacturers. Ratings are typically to 1000 VDC for a single contact, at currents to several thousands amperes. These devices have a true fault interruption capability, and can survive many thousands of load-break operations. They are probably the most valuable switchgear item available to the array field designer. A typical device would be rated 1000 ADC at 1000 VDC. Four of these are used in the Georgetown system, two as subfield disconnects and two as crowbars.

The classical low voltage AC circuit breaker is somewhat of an orphan in the DC switching marketplace. These thermal-magnetic circuit breakers are available in a myriad of ratings from virtually every U.S. switchgear manufacturer. Only a very few of the designs are however rated for DC service. When a DC capability exists, a representative derating factor would be from 600 VAC to 250 VDC. In some instances, two series poles are specified to achieve the DC rating. The AC fault current interruption rating of even the smallest moulded case circuit breaker is excellent, typically 10 kA RMS at 120 VAC; a corresponding DC capability is however not claimed.

Another valuable fault interruption device is the fast acting high voltage DC fuse. The melt and clear characteristics of HVDC fuses, and those used in AC distribution applications have been precisely established. Various current/time characteristics can be specified and procured. For example, Georgetown branch circuit fuses will clear at 140% overload.

Cold sectionalizing devices play an important role in central station arrays. A PV power collection network sums the contribution of a number of lower power generating networks. In keeping with approved utility and ANSI practices, such faulted circuits should be capable of sectionalization, in order to minimize the extent of the outage and if possible, permit the balance-of-system to deliver power. If a "cold" disconnect can be assured, almost any adequately rated UL recognized AC safety switch can be used to confidently isolate a faulted network, once the current flow has been

interdicted by other means. In the PHENEF system appropriately rated CBs are used for both load break and sectionalization. The AMP Solarlok connector system is used to interconnect all of the 4,464 PV modules into the 124 bipolar strings and to tap off each neutral. This cold disconnect device has been UL recognized for 450 VDC at 7 AMP service, including accidental load break at 150% overload.

Both the shortcomings as well as the superior attributes of protective switchgear and devices potentially deployable in central station applications have been characterized. Except for high voltage contactors, fuses and cold disconnects a broad selection of apparatus is not available, even for the baseline central station power levels. This present disparity will by no means diminish as the ratings of the power building blocks increase.

If the DC bus voltages were to be held to below 1000 VDC, expansion of the modular DC power ratings could be achieved only by accepting the increased resistive losses resulting from the expanded planar array field. If the power expansion were accompanied by raising the bus voltage, the power losses as the result of the larger collection area would become more tolerable. Higher voltage rated devices, principally those of the air-magnetic circuit breaker and contactor type would however be required. Sectionalizing switches, typically at the ANSI HV distribution levels, as well as Metallic Oxide Varistors surge arrestors should be readily available. Higher voltage DC fuses may present a future procurement problem.

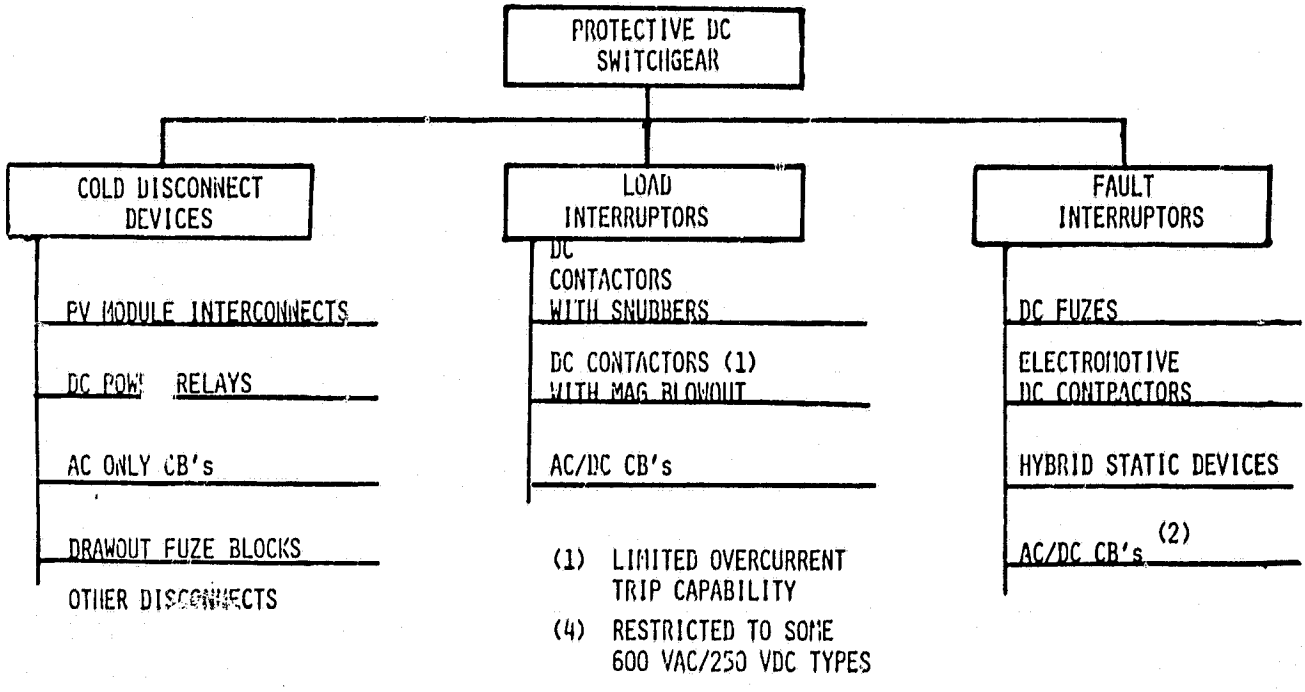
Reference (1) Gonzales cc; Hill.6M; Ross, R.G. Jr.
"Photovoltaic Array - Power Conditioner Interface Characteristics"; JPL Flat Plate Solar Array Project 5101-202 Dec 15, 1982

ELECTRICAL SAFETY FOR HIGH-VOLTAGE ARRAYS

HUGHES AIRCRAFT CO.

Neil A. Marshall

Classification of Dc Switching Devices



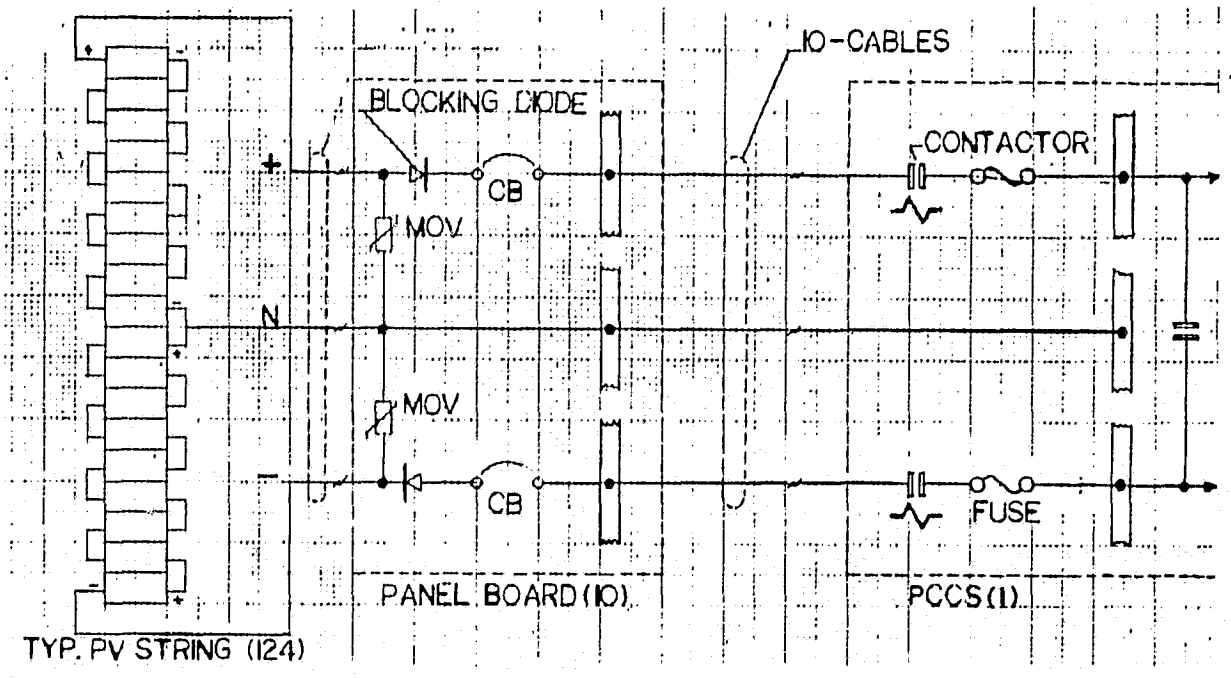
Reference System Configurations

PARAMETER	HUGHES/GU PHENEE	BASELINE CENTRAL STATION MODULE
PEAK POWER @ SOC	300 kW PK	1 MW PK
CONFIGURATION	BIPOLAR NEUTRAL RESISTIVELY GROUNDED	BIPOLAR
OCV (OPTIMAL CENTER VOLTAGE)	± 228 VDC	± 300 VDC
MAIN BUS CURRENT AT PEAK POWER	660 ADC	1660 ADC
OPEN CIRCUIT VOLTAGE (MAX. VOC)	<800 VDC	<1000 VDC

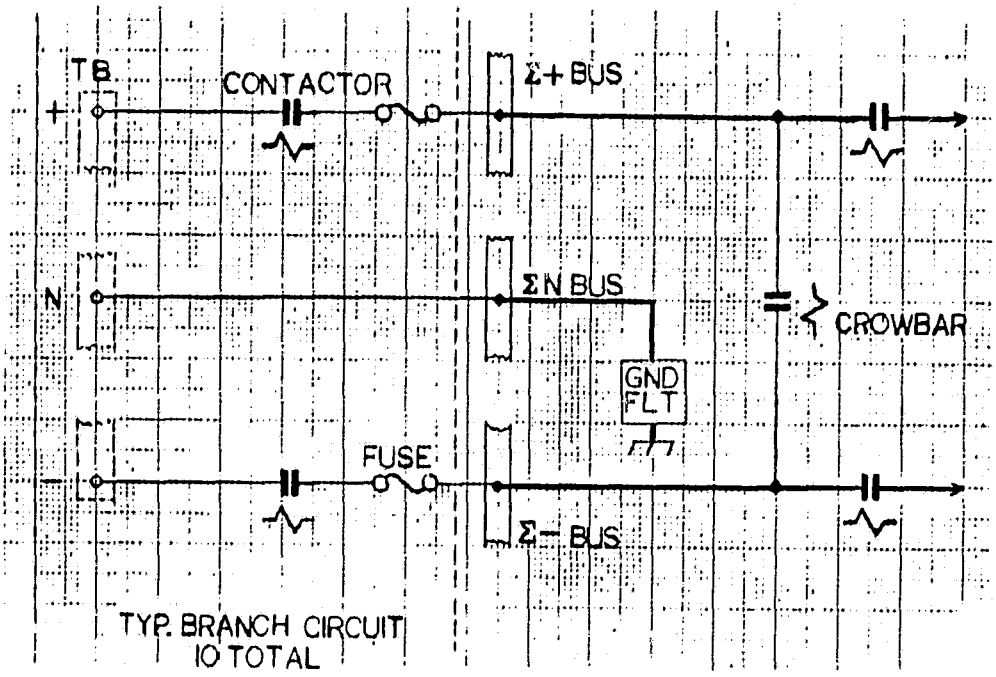
PHENEF Comparative Advantages of Bipolar Operation

- MAINTAINS AN ACCEPTABLY HIGH LINE-TO-LINE VOLTAGE, WHILE DIVIDING THE DIELECTRIC WITHSTAND BY 2 X:
- COLLATERALLY LOWERS THE HV AND GROUND ARCHING HAZARD.
- ELIMINATES NEUTRAL CURRENT FLOW – MAKES FOR SUPERIOR GROUND FAULT RELAYING.
- MATERIALLY EASES DC SWITCHGEAR SELECTION REQUIREMENTS AND COST.
- DECREASES "SNEAK" CIRCUIT GALVANIC CORROSION.
- CAN ASSIST IN INTEGRATED ARRAY ENERGY DELIVERY THROUGH CROSS STRAPPING.

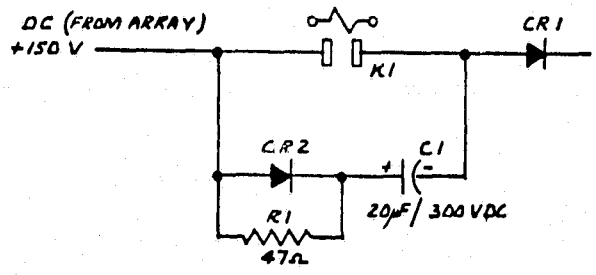
Simplified PHENEF Block Diagram



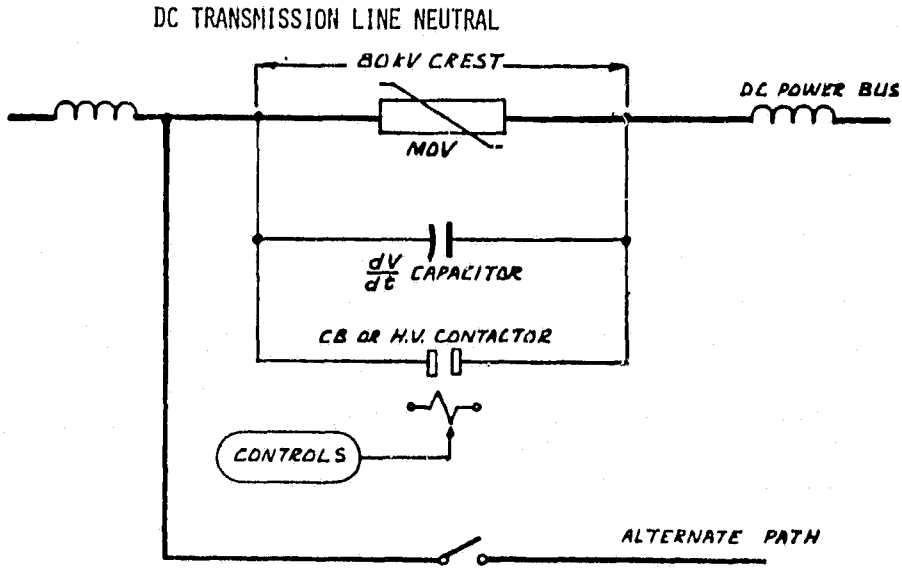
Dc Collection: PHENEF



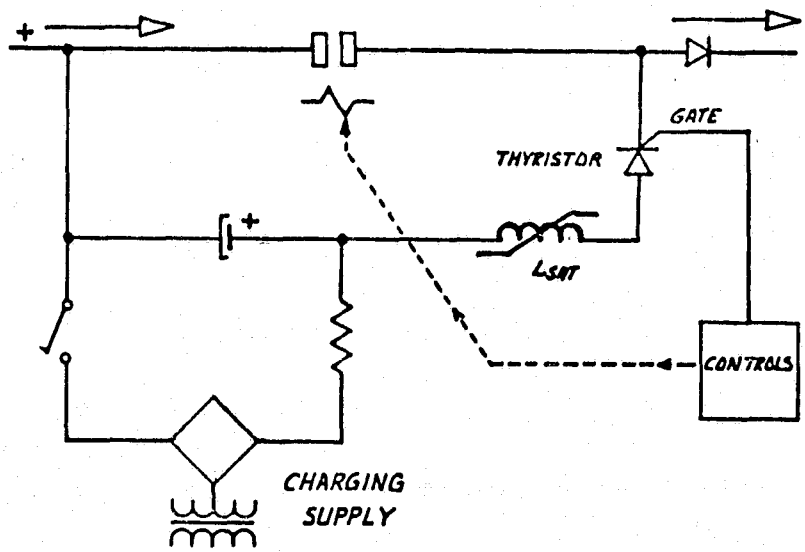
Arcless Dc Power Interruption: Snubber Method



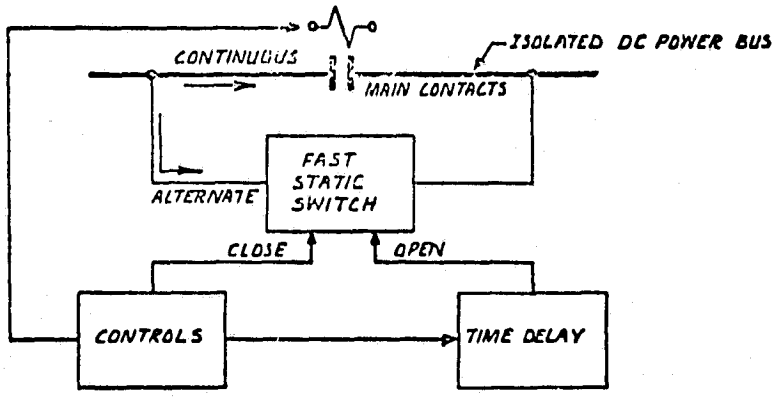
HVdc Power Transfer With Commutating Capacitor



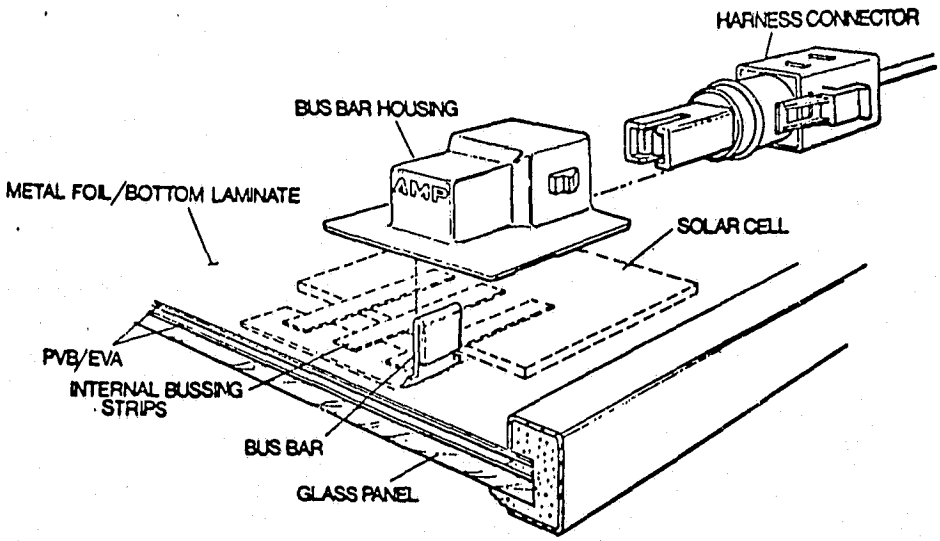
Arcless Dc Power Interruption: Current Zero Method



ARCLESS DC INTERRUPTION:
BYPASS STATIC SWITCH



Solarlok Connector System



GROUNDING AND FAULT PROTECTION OF THE SMUD PV1 ARRAY

Dan Rosen
Acurex Corporation
Mountain View, California

If large terrestrial photovoltaic (PV) powerplants are to provide an economic source of generation, low-cost, reliable and easily maintainable systems must be developed. In addition, if the system is to be a central station powerplant owned and operated by an electric utility, the design must also be consistent with utility specifications and design standards. This paper presents the particular solutions developed to address these issues, with regard to grounding and fault protection, for the first phase of the Sacramento Municipal Utility District's (SMUD) 100-MW_{AC} PV powerplant. This plant, known as PV1, is nominally rated at 1 MW_{AC} and is scheduled to be in operation by the spring of 1984.

The grounding and fault protection system was designed in accordance with SMUD's standard practices. The design limits step-and-touch potentials to acceptable levels in accordance with IEEE STD 80 -- IEEE Guide for Safety in Substation Grounding. The maximum available fault current used for the calculations was 1,560A at the 12.47 kV_{AC} interface. All exposed metal (e.g., array support structures) is bonded to the grid and all buried ground connections are of the exothermic weld type per SMUD standards.

The ground system is composed of a buried bare copper ground grid, with no credit taken for the grounding capability of the 1,000 pier foundations in the array field. Each of the 112 arrays are bonded to the grid at both ends and in the middle, at the drive unit. Flexible grounding jumpers are provided to bond the other support posts to the array panels (the nylon bearings at each support would otherwise isolate the posts from the array and ground grid). This design is fairly conventional and meets all design requirements. However, the large amount of copper required and the quantity of exothermic welds (over 500) results in high cost. The estimated cost for this part of the system is on the order of $100,000, or $0.08 per peak DC watt. Inclusion of the pier foundations in the grounding calculations, as well as the use of alternate connection techniques, are being evaluated for future phases to reduce costs.

The DC bus is center tap resistance neutral-grounded and operates at a maximum open circuit voltage of ±500 VDC. Resistance grounding was selected to provide a ground reference for the array, to prevent the DC bus from floating to unacceptably high voltages with respect to ground, while also limiting DC ground fault current to acceptable levels. A two-stage grounding system was selected to provide personnel protection during maintenance activities and to allow sufficient sensitivity for detection and location of ground faults during normal operation. Normally, the neutral ground resistance is 1,000 ohms, while in the maintenance mode the resistance is 40,000 ohms.

The PV1 array field is divided into four subfields, each with a separate netural and DC power collection bus. Electrically operated contactors permit isolation of any subfield from the remainder of the plant at any time, even during operation. All elements of each subfield, down to the panel level, are capable of being isolated from the plant by quick-disconnect-type nonload-break connectors.

Maximum ground fault current for any ground fault occurring on the DC system is limited to 2A in the normal grounding mode and 50 mA in the maintenance mode. By monitoring the current flowing through the ground resistor (actually the neutral voltage with respect to ground) it is possible to detect ground faults. The netural voltage is proportional to array voltage, fault resistance, and fault location with respect to the neutral. A fault located on the neutral can therefore not be detected because there are no solar cells in the circuit to drive current through the ground resistor. However, it is important to identify and repair faults on the neutral, since this would negate the effect of the ground resistor on subsequent faults. To accomplish this an AC fault injection signal is provided. The neutral (AC) voltage measured in response to this signal is a function only of the ground fault resistance and can be used in conjunction with the neutral (DC) voltage and appropriate curve fitting techniques to identify all faults, including those occurring on the neutral, as well as to determine approximate fault locations.

It is believed that this system will provide a cost-effective solution to the problem of providing equipment and personnel protection against DC ground faults, while minimizing the time necessary to locate and repair faults when they do occur.

In summary, the design of the PV1 grounding and fault protection system accommodates SMUD's standard design practices while providing some unique solutions to the problems of ground fault protection and detection. Additional engineering analysis, and plant operating experience, will permit optimization of the current design for use in future plants.

GROUNDING AND FAULT PROTECTION OF THE SMUD PV1 ARRAY

ACUREX CORP.

Dan Rosen

Design Requirements

- PROVIDE EQUIPMENT AND PERSONNEL PROTECTION
- FACILITATE MAINTENANCE
- COMPLY WITH SMUD STANDARD PRACTICES
- ACCOMPLISH AT ACCEPTABLE COSTS (CONSISTENT WITH COST GOALS FOR COMMERCIAL PV POWERPLANTS)

Design Basis

- DESIGN FOR ACCEPTABLE STEP AND TOUCH POTENTIALS IN ACCORDANCE WITH IEEE STD 80-IEEE GUIDE FOR SAFETY IN SUBSTATION GROUNDING
- ALL EXPOSED NON-ENERGIZED METAL COMPONENTS MUST BE BONDED TO THE GROUND GRID
- ALL UNEXPOSED (E.G., BURIED) GROUND CONNECTIONS MUST BE OF THE EXOTHERMIC-WELD TYPE
- USE SOIL RESISTIVITY VALUE OF 220 OHM-M (DEVELOPED BY BECHTEL DURING DESIGN OF RANCHO SECO)
- MAXIMUM AC FAULT CURRENT EQUALS 1,560A AT THE 12.47-kV INTERFACE

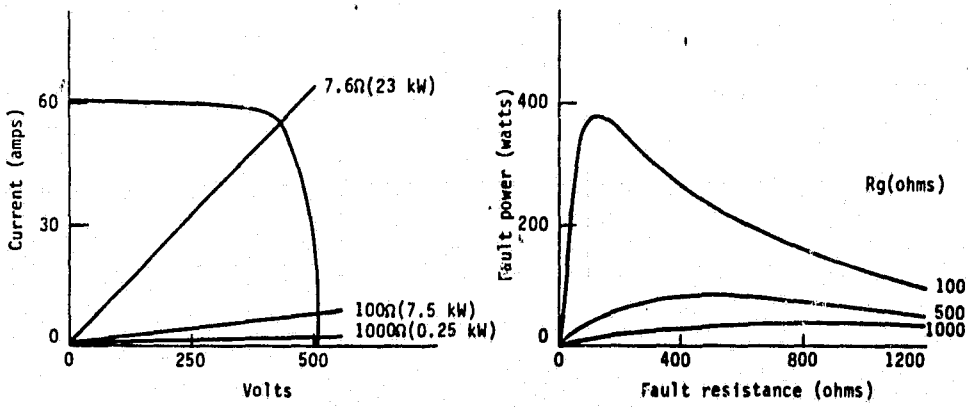
Dc Ground Faults

- MAXIMUM DC VOLTAGE = 1,000V (±500V)
- THE PLANT CONTAINS 28,672 1-FT X 4-FT MODULES OR:
  - -- 2.7 ACRES OF ENCAPSULANT
  - -- 54.3 MILES OF MODULE PERIMETER
- MODULE GROUND FAULTS CAN BE EXPECTED TO OCCUR
- PERSONNEL MUST BE PROTECTED FROM EXPOSURE TO LETHAL ARRAY VOLTAGES
- DAMAGE TO FAULTED AND ADJACENT EQUIPMENT MUST BE MINIMIZED
- LOST ENERGY RESULTING FROM FAULTS MUST BE MINIMIZED

Dc Neutral Resistance Ground

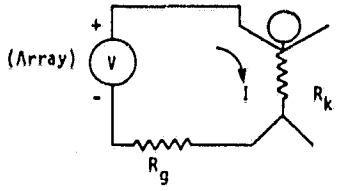
- LIMITS DC FAULT CURRENT
- PROVIDES GROUND REFERENCE
- FACILITATES FAULT LOCATION
- PRECEDENT IN INDUSTRY (E.G., DISNEY WORLD 480-V_{AC} SYSTEM)
- CAN RESULT IN PRESENCE OF FULL-SYSTEM VOLTAGE ACROSS SOME MODULES DURING FAULT CONDITIONS

Ground Resistor Selection



Dc Ground Current Limits for Personnel Safety

- NOT MUCH IN THE LITERATURE REGARDING DC
- REVIEW OF IEEE 80 INDICATES THAT:
  - -- MAXIMUM BODY CURRENTS FOR SUSTAINED FAULTS SHOULD BE LIMITED TO LESS THAN SAFE LET-GO VALUES
  - -- SAFE LET-GO VALUES FOR AC ARE ABOUT 9 mA
  - -- SAFE DC LEVELS MAY BE AS MUCH AS 5 TIMES THOSE AT 60 Hz (45 mA)
- EQUIVALENT CIRCUIT FOR BODY CURRENT

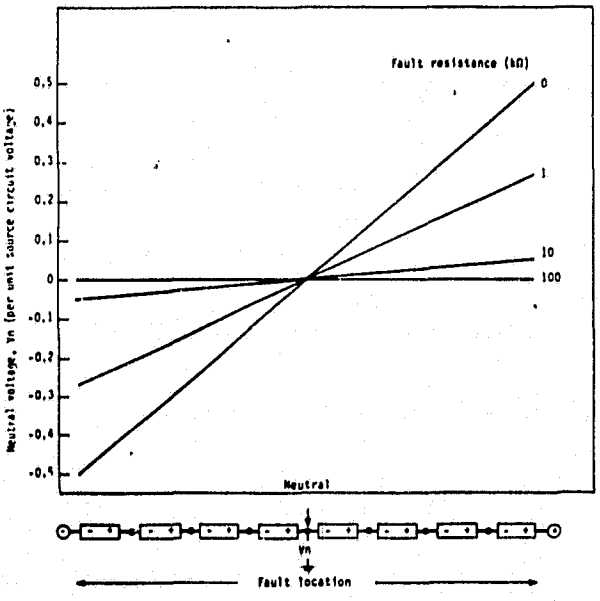


WHERE: V = 1/2 SOURCE CIRCUIT VOLTAGE = 500 V_{DC}
R_K = BODY RESISTANCE = 1,000 Ω (IEEE80)
R_G = GROUND RESISTANCE
I = BODY CURRENT

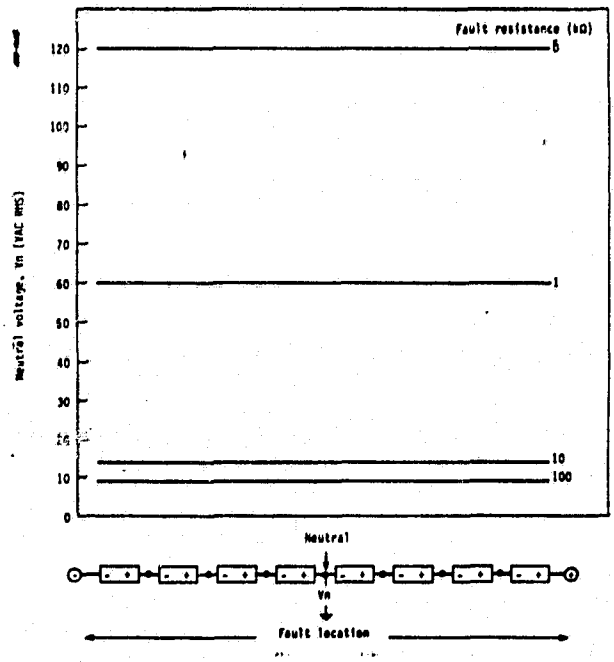
$$I = \frac{V}{R_K + R_G}$$

$$R_G = \frac{V}{I} - R_K = \frac{500}{0.045} - 1{,}000 = 10.1\ K\Omega$$

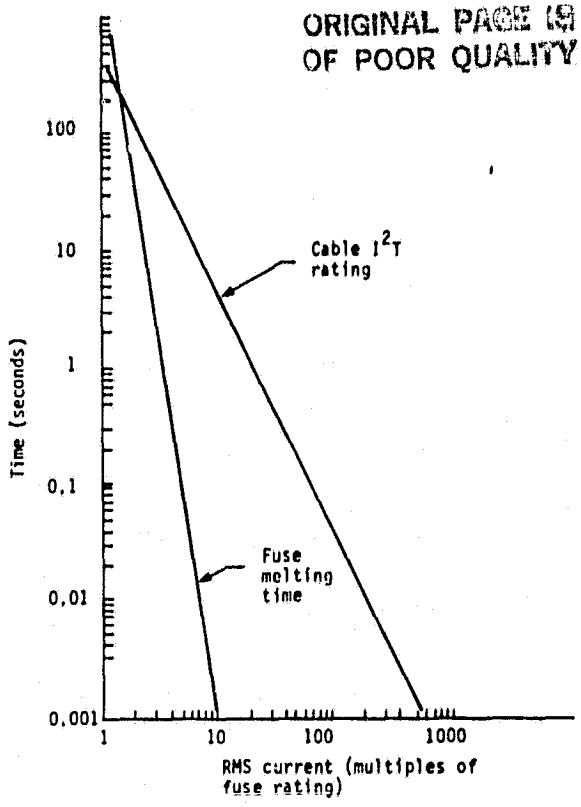
Ground Fault Location



SOURCE CIRCUIT NEUTRAL DC VOLTAGES

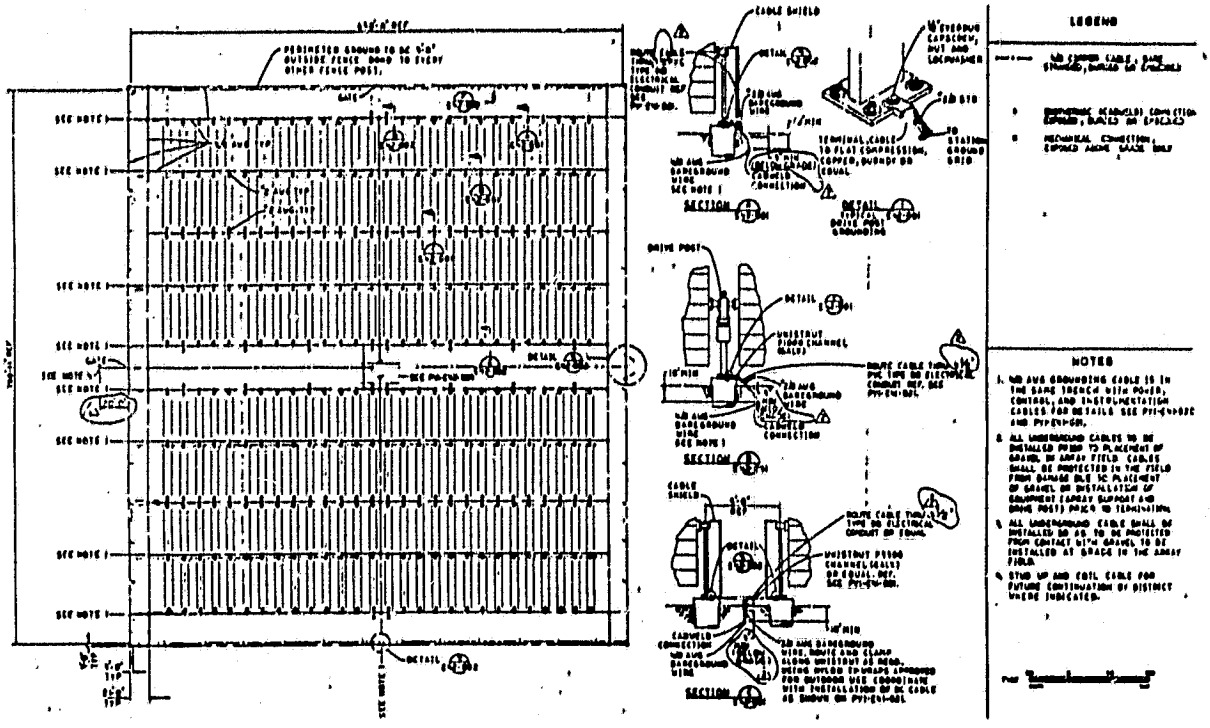


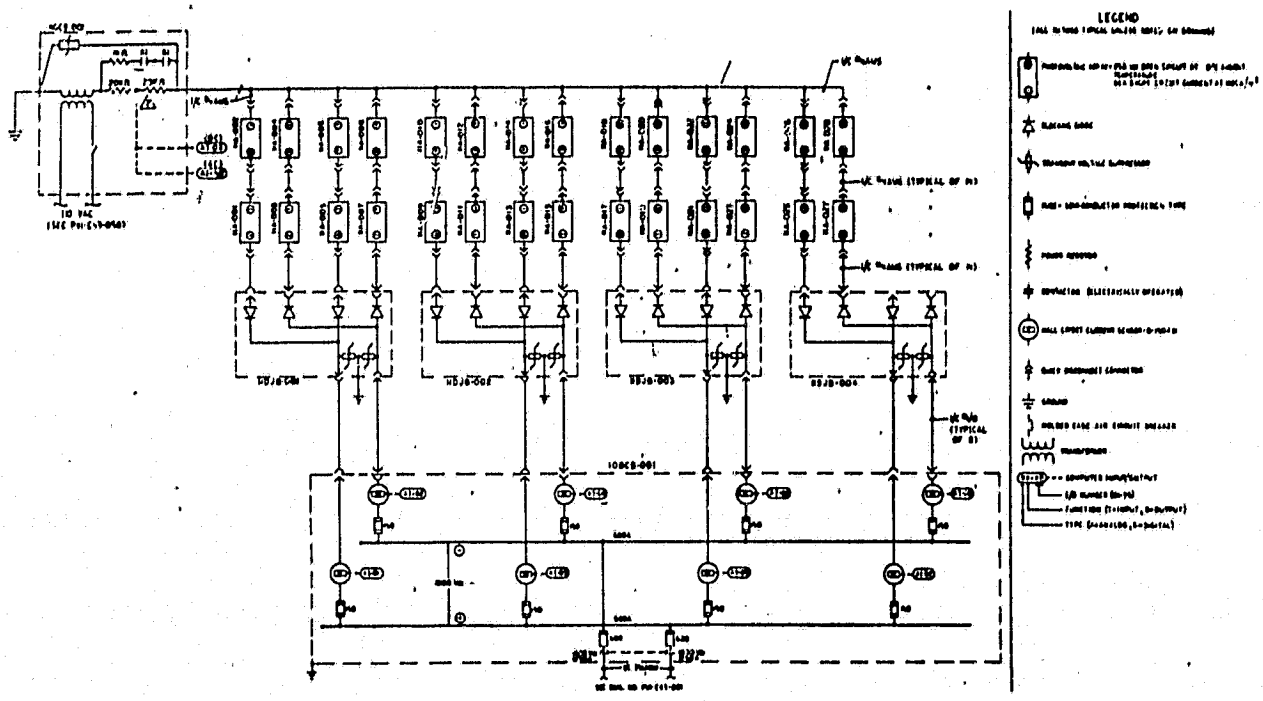
SOURCE CIRCUIT NEUTRAL AC VOLTAGES



Summary

- THE SMUDPV1 GROUNDING SYSTEM IS DESIGNED TO MINIMIZE STEP-AND-TOUCH POTENTIALS PER IEEE 80
- ALL EXPOSED METAL IS BONDED TO THE GRID
- A TWO STAGE RESISTIVE DC NEUTRAL GROUND SYSTEM IS USED TO PROVIDE EQUIPMENT AND PERSONNEL PROTECTION
- FAULT INJECTION AND LOCATION EQUIPMENT IS PROVIDED TO FACILITATE IDENTIFICATION AND REPAIR OF GROUND FAULTS
- FUSE COORDINATION WITHIN THE DC SYSTEM IS COMPLICATED BY THE LIMITED FAULT CURRENT AVAILABLE AND IS A TRADEOFF BETWEEN AVOIDANCE OF NUISANCE TRIPPING AND THE NEED TO PROTECT EQUIPMENT AT LOW INSOLATION LEVELS





PHOTOVOLTAIC CENTRAL STATION STEP AND TOUCH POTENTIAL CONSIDERATIONS IN GROUNDING SYSTEM DESIGN

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Kansas City, Missouri

The probability of hazardous step and touch potentials is an important consideration in central station grounding system design. Steam turbine generating station grounding system design is based on accepted industry practices and there is extensive in-service experience with these grounding systems. A photovoltaic (PV) central station is a relatively new concept and there is limited experience with PV station grounding systems. The operation and physical configuration of a PV central station is very different from a steam electric station. A PV station bears some similarity to a substation and the PV station step and touch potentials might be addressed as they are in substation design. However, the PV central station is a generating station and it is appropriate to examine the effect that the differences and similarities of the two types of generating stations have on step and touch potential considerations.

There are many considerations in generating station grounding systems, and some of these, such as surge protection, cathodic protection, as well as step and touch potentials have been examined in the report prepared for Sandia National Laboratories (Reference 1). This paper is confined to step and touch potential considerations.

Step and touch potentials occur when current flows through earth. In this context, earth is defined to be the media under foot, e.g., sod, crushed rock, and concrete. Earth current can be the result of normal electrical system operation. In some applications, it might be permissible to use earth as a return conductor from load to source. In addition, there are leakage currents to earth from all energized electrical equipment. However, normal electrical system operation rarely leads to high earth currents. Hazardous step and touch potentials are usually the result of large earth currents due to phase-to-ground faults.

It is usual steam generating station design practice to provide metallic conducting paths for all phase-to-ground faults that could occur in the generating station, and thereby eliminate high earth currents. A PV generating station can also be designed to eliminate high earth currents due to polarity-to-ground and phase-to-ground faults. In either case, there might be a substation located in close proximity to the generating station and there could be high earth currents for phase-to-ground faults in the substation. Table 1 lists earth current magnitude for normal operation and ground faults in substations, steam electric, and PV generating stations.

TABLE 1. EARTH CURRENT

	Steam Electric Generating Station	Photovoltaic Generating Station	Substation
Normal Operation			
ac	leakage	leakage	leakage
dc	negligible	leakage	negligible
Faults			
ac	small	small	large
dc	small	small	small

Steam electric generating station design usually includes a conductor to buried metallic grounding electrodes from steel structures, high energy rotating equipment enclosures, and the enclosures of electrical distribution and utilization equipment. This assures that fault currents will have a metallic return path. Grounding of steam station structures and equipment can be accomplished with a grid, like that shown on Figure 1. A grid is selected because it is a cost-effective design for the major station structures. Since large earth currents are not expected in a steam electric station, the ground system need not be designed as a grid to reduce step and touch potentials. Also, it is accepted practice to provide a grounding system in steam station areas that have equipment or structures, but not in all areas of the station.

Direct current polarity-to-ground faults in a PV generating station are current-limited by nature of the PV cell, and metallic return paths may not be necessary. Acceptable fault current return paths can be accomplished through design of the dc source circuit and local ground connections. One dc source and collection circuit conceptual design is shown on Figures 2 and 3. The PV station ac power collection system can achieve control of ground fault currents by circuit design that eliminates ground fault currents, or installation of conductors to assure a metallic return path for all phase-to-ground faults. Fault currents in the array ac tracking power system can be controlled with metallic conductors installed with the powe. conductors. Therefore, PV generating station fault currents are limited, or metallic conductor paths are provided, and step and touch potentials due to operation of the PV generating station alone are not a safety concern. Large earth currents are eliminated, just as they are in a steam generating station, and the PV generating station ground system meets the requirements with dispersed ground points instead of a more expensive grid configuration.

A substation is generally located adjacent to a steam electric or PV generating station. High phase-to-ground fault currents from remote sources and high earth currents are possible. Typically, there is a substation ground grid similar to that shown on Figure 4. The substation ground grid is designed to assure that step and touch potentials will not exceed safe levels within the substation. However, the earth currents might be so large that it is not practicable to achieve a tolerable limit to step and touch potentials outside of the substation. The step and touch potentials outside of the substation are due to ground potential gradients caused by earth current density in the

resistance of the earth from the substation grid to the remote source of the fault. In order to assure that step and touch potentials are within tolerable levels outside of the substation, the resistance of the earth from the ground grid to the remote source must be reduced to a small value or the earth current density must be limited. This is usually not achievable.

For a substation located in close proximity to a steam electric generating station, it is effective and inexpensive to connect the substation ground grid to the generating station grid. Earth current density is reduced because the grid area is increased and the grid resistance with respect to remote earth is reduced. The generating station grounding system has a grid configuration, and step and touch potentials are usually within tolerable levels in the major structures. However, step and touch potentials in generating station areas that are remote from the major structures may not have a ground grid, and step and touch potentials may exceed tolerable levels in these areas.

A substation located in close proximity to a PV generating station could have phase-to-ground fault earth currents from remote fault sources. High earth currents are possible, just as they are possible for a substation at a steam generating station. However, it would be expensive to connect the ground grid of the substation to the PV generating station ground system. In order to achieve metallic conductor connection of the substation ground grid to all grounds in the PV generating station grounding system, all of the generating station ground points would first be interconnected, and then connections would be made between the generating station and substation ground systems.

In Reference 1, an integrated PV generating station and substation grounding system is suggested, with an estimated total system cost range of $\$0.60/m^2$ to $\$1.30/m^2$ of array area. The estimated cost is a function of grounding system conductor size and the size of the array field. Figure 5 shows a grounding grid configuration for the fixed flat plate 100 MW PV generating station shown on Figure 6. Figure 7 is the mesh potential diagram for the grid. Earth resistivity of 500 ohm-meters and substation fault current of 20 kA was assumed. The unequal spacing of the grid on Figure 5 provides protection over most of the field and minimizes cost. The grid would cost approximately $\$1.30/m^2$ of array area, using a 4/0 AWG conductor.

A PV generating station ground system and the substation ground grid could remain unconnected. Step and touch potentials that occur in the PV generating station area could exceed tolerable levels just as potentials can exceed tolerable limits in some areas of a steam electric generating station. The earth current, due to substation phase-to-ground fault, will probably concentrate in areas near the high voltage transmission lines that connect the substation to the utility system. However, metal structures in contact with earth, such as fences, pipelines, and steel-reinforced concrete, affect the earth current distribution and significant earth return current could be present in the PV field. Significant earth return current density in the PV field could expose utility personnel to elevated ground potential gradients.

The risk of hazardous step and touch potentials in a PV generating station with a grounding system that is not connected to an adjacent substation ground grid is comparable to the risk experienced in most areas outside of the major structures of steam electric generating stations. In addition, the risk in

the PV generating station is comparable to the risk that exists in areas adjacent to substations and under transmission lines located throughout the electric utility system.

The conceptual design for the EPRI PV generating station (Reference 2) was based on the assumption that a 230 kV substation would be located next to the PV generating station. That grounding system design did not include a grid to limit step and touch potentials, because the level of risk of hazardous step and touch potentials is no greater in the PV area than it is in steam electric generating stations and areas open to the general public.

REFERENCES

1. Sandia National Laboratories, Bechtel Group, Inc., "Photovoltaic System Grounding and Fault Protection Guidelines."

2. Electric Power Research Institute, "Integrated Photovoltaic Control Station Conceptual Design."

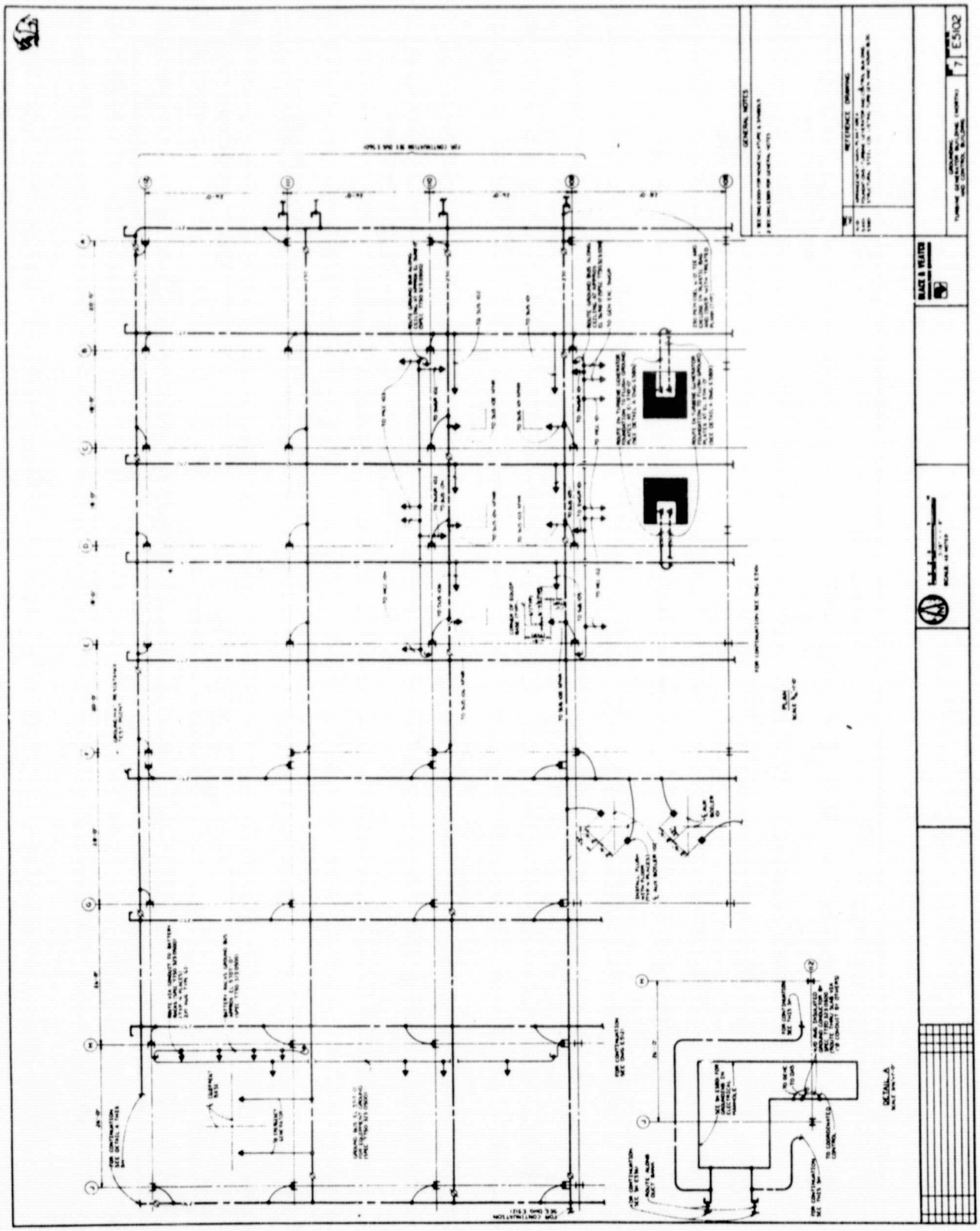


Figure 1

Figure 2

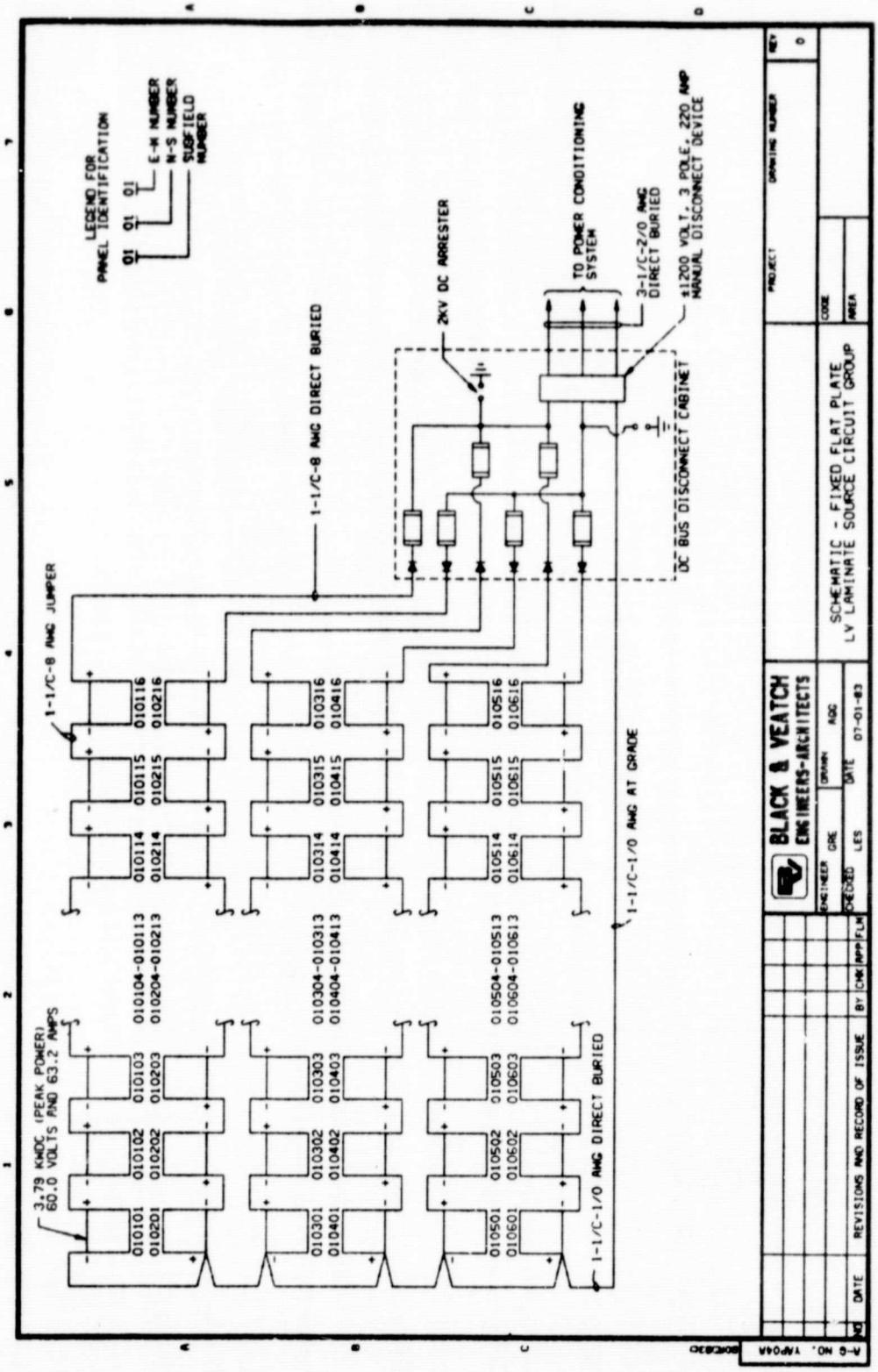
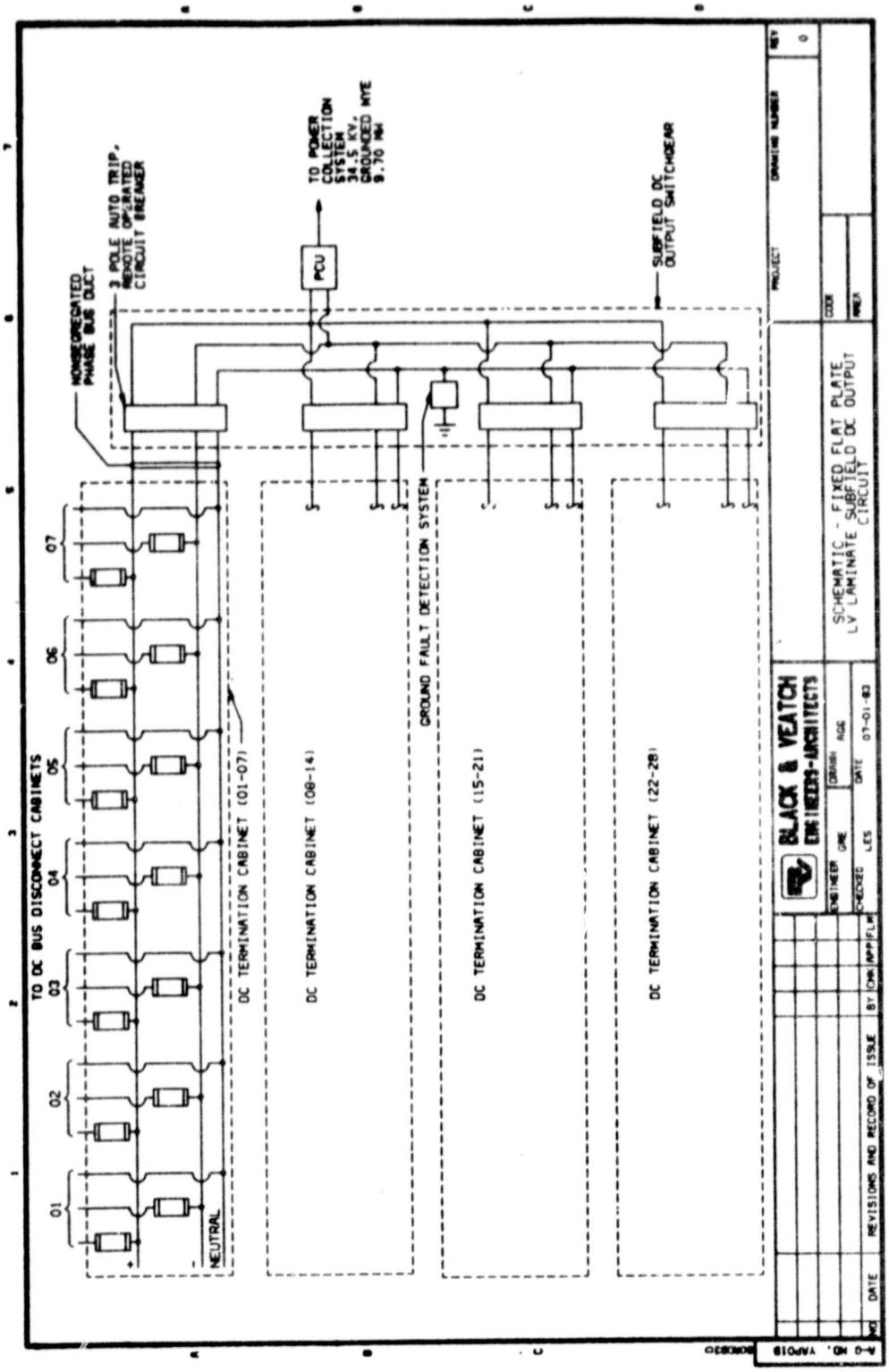


Figure 3



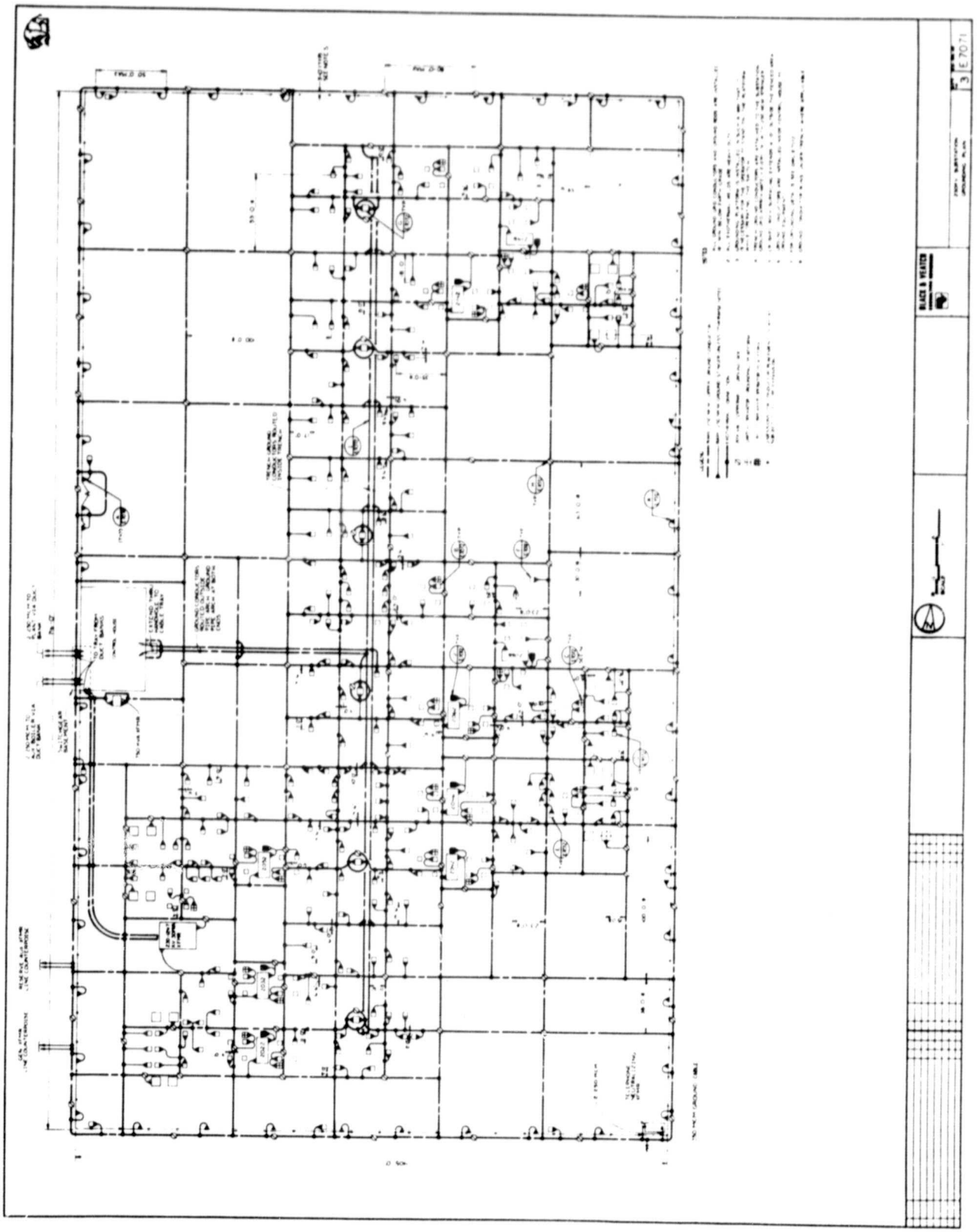
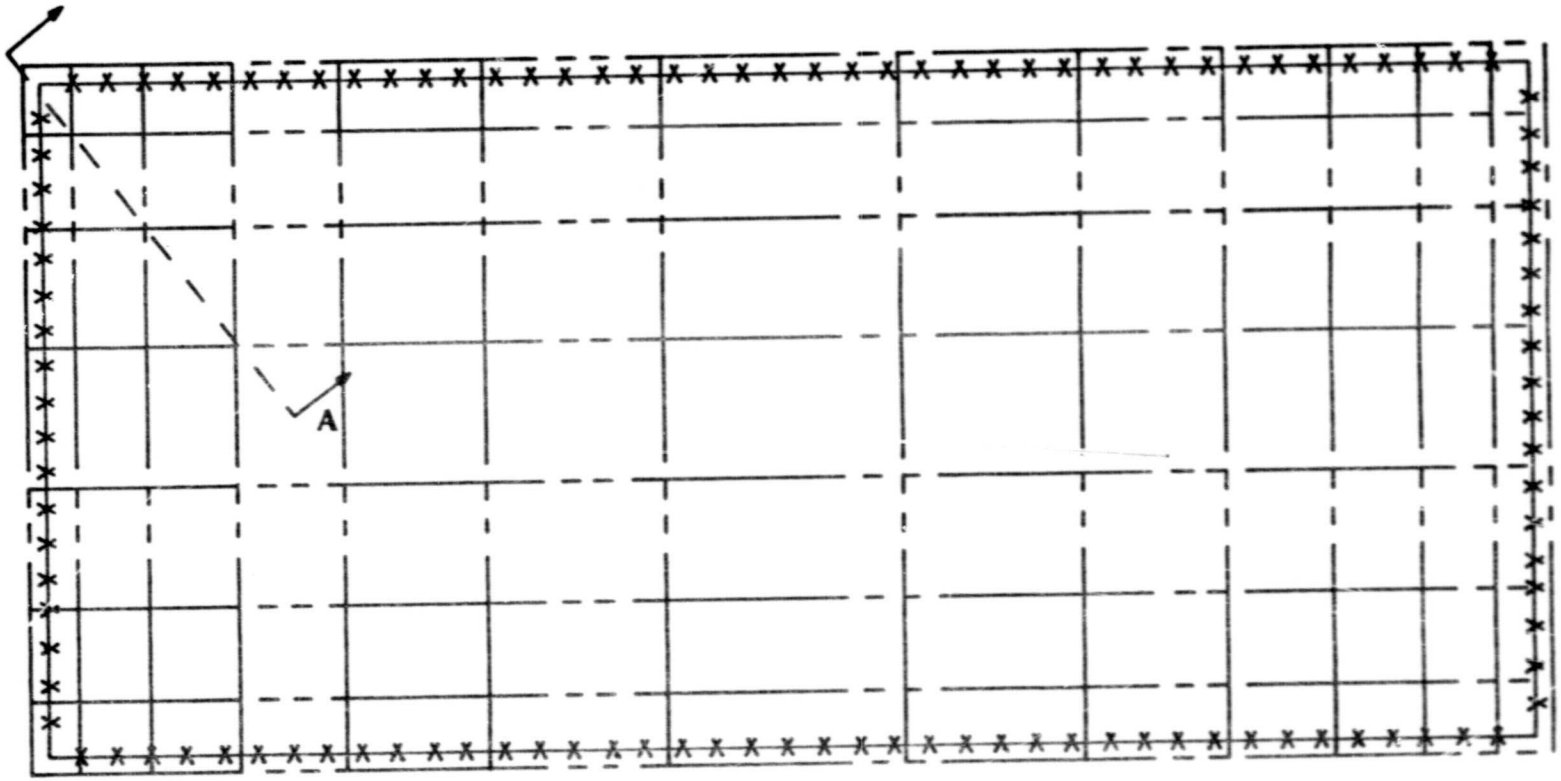


Figure 4

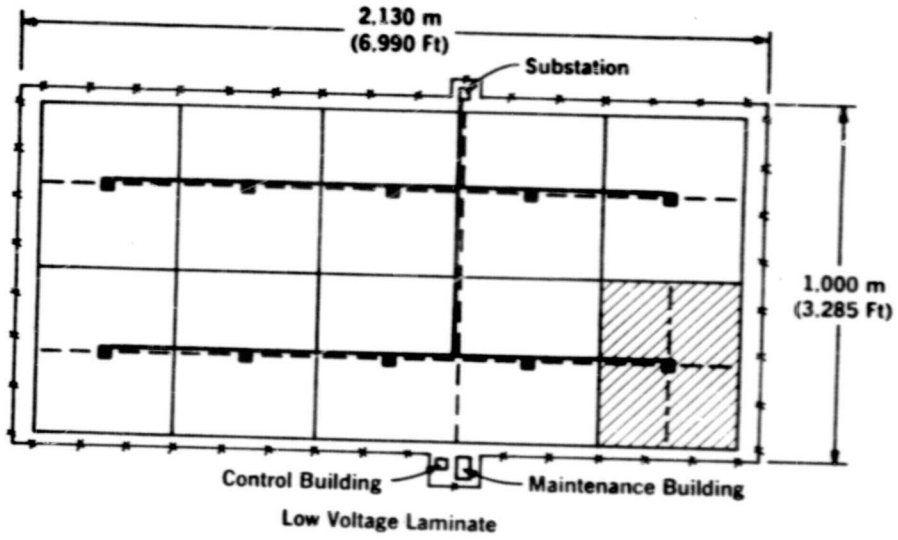
Figure 5



Scale: 1" = 200 Meters'

Fence Line as Shown in Figure 6

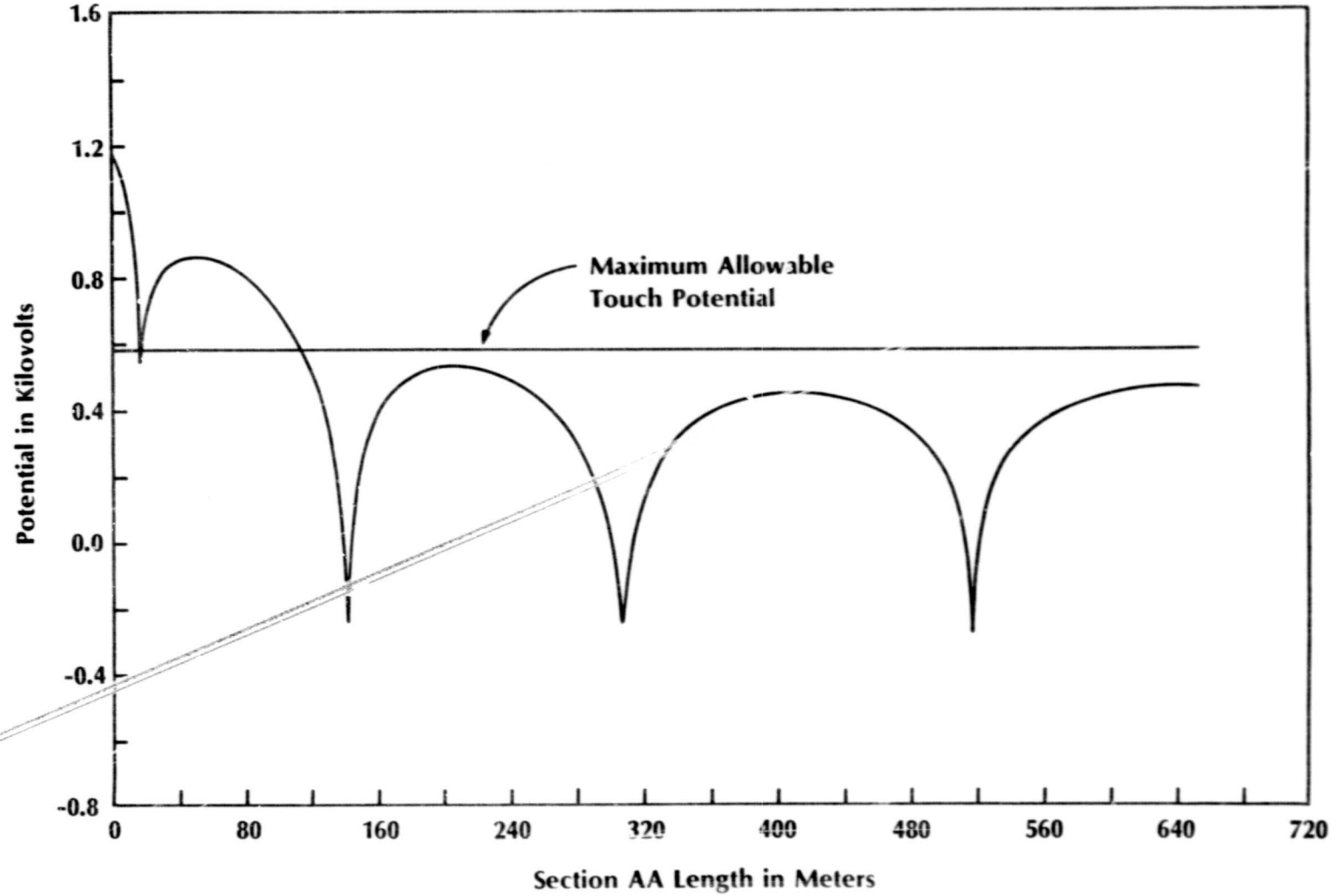
Figure 6



Specifications:
LV Array Area: 799,000 m²
LV Land Area: 530 Acres
LV Plant Rating: 87 MW SW; 73 MW SE
LV Peak Plant Capacity: 97 MW
Row Orientation: E-W
Row Spacing: 5.5 m (18 Ft)
Ground Cover Ratio: 0.44

Legend
- PCU (10 Total)
- Subfield (10 Total)
- Security Fencing
- Oiled Gravel Road
- Access Aisle (Typical of Each Subfield)
- AC Collection Cabling

Figure 7. Touch Potential With Respect to GPR



SESSION IV

ARRAY AND MODULE STRUCTURAL INTERFACE DESIGN

S. Levy, Chairman

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SESSION IV

ARRAY AND MODULE STRUCTURAL INTERFACE DESIGN

Chairman: S. Levy, Black & Veatch

SUMMARY

The session titled Array/Module Structural Interface Design consisted of three papers. It started with R. Spencer and V. Wong of Acurex stating what they desired in terms of standardization for the interface. They emphasized the structural interface but also discussed electrical interfaces. The next paper, presented by J. C. Arnett, presented ARCO Solar's investigation of hot-spot heating due to shading for utility-size systems. The last paper, by W. E. Dombert of Solarex, questioned if the industry was ready for standards.

Arnett's paper presented comparisons of results from analytical and experimental investigations on module hot spots due to shading: although high temperatures ($\Delta T \simeq 70^{\circ}$) were found, no irreversible deleterious effect occurred. Long-term testing is continuing at ARCO. The papers by Arnett and Dombert presented a great number of viewgraphs illustrating the variety of methods used by both manufacturers in meeting requirements that had been placed upon them for their product. The variety of systems that use their produce ranges from the Solarex breeder building to small individual panels. They showed a very impressive range in the variety of demands on panels and a challenge for their standardization.

The differing opinions on the need for standardization raised the question: are we all speaking about the same thing when we speak of standards? The IEEE (an approved ANSI issuing body for standards) definition of a standard is a list of terms, definitions, and symbols, expositions of scientific methods of measurements and test performance, etc., characteristics of performance and safety requirements associated with devices, equipment, etc., and recommendations reflecting current state of the art in an application to engineering. The IEEE classifies its standards into three categories: (1) mandatory requirements, (2) recommended practices, and (3) guides.

Interface standards cited by Acurex were geometric, by size -- 4 ft on centers for the bolt holes, 16 ft x 9 ft panels, etc.; electrical -- a single pigtail and interconnect type, voltage and current ratings; and last, environmental -- withstand wind loads of 80 miles an hour, etc. What was not mentioned, for instance, was the structural interface -- the mechanical loads that must be transmitted. It seems that the real question we were discussing in this session was standards vis-a-vis specifications. There are ANSI standards which use "Thou shalts" to specify the item, e.g., 1/4-in.-20 screw shall have 1/4-in. OD and 0.050-in. pitch with its prescribed tolerances. Then there is a whole group of other standards established by manufacturers for commonality

and exchange/interchange. In the electrical industry these are known as NEMA standards. Acurex implied a desire for manufacturers' standards, under which certain sizes and bolt holes would be accepted.

Another type of standard is referred to as codes: the UBC, Universal Building Code; NEC, National Electric Code; NESC, the National Electric Safety Code. Still another class is certifications such as the UL label. Underwriter's Laboratories has specifications that a product must meet to be certified. Then each utility has its practices and procedures -- Southeast utilities specify 110 miles per hour for calculating wind loads; in the SMUD project, 80-miles-per-hour wind loads were sufficient.

One reason Acurex advocated standards was to ease bid evaluation and reduce system design time. ARCO Solar, I sensed, desires specifications. In essence, I heard Arnett say "Tell us what you want our system to do for you and we, the manufacturer, can best meet the performance and interface specifications you have specified." It gives flexibility to integrate in the design function some novelty, such as elimination of the frame on the module and go to laminates with the adhesively bonded hat sections that Arnett showed.

Solarex, in Dombert's presentation, questioned the timeliness of standards. Dombert said that the system is evolving rapidly to pin down manufacturers' standards. These standards should be industry (manufacturers') standards. I would like to make another comment on standards: "standards are a consensus of all parties involved." The reason standards have such a long gestation is that everybody has to agree before it can become a standard.

In the near term, I believe PV systems should be specification-dominated instead of standards-dominated. That means we should continue qualification tests, such as hail and so so, that are applicable. In the future, I think the large systems will continue to be specification-dominated because the manufacturer may want the flexibility of meeting that production demand by a variety of means, which gives him an edge and gives the buyer an improved product. Standard product lines will evolve and may even develop into manufacturer's standards similar to NEMA. The areas that I believe have to be studied by JPL and others is the electrical interchangeability, especially if you worry about production, shadowing and mismatch, which have been commented on earlier.

INTERFACE STANDARDIZATION

Robert Spencer and Vernon Wong
Acurex Corp.
Mountain View, California

Central-station applications create a large and attractive market for photovoltaics in the near future. However, some significant barriers lie between the industry of today and realization of that market. Manufacturing capacity and price are two principal impediments. The utilities, which are the future system owners, are gaining experience with central-station PV power through the Sacramento Municipal Utility District, Hesperia and similar small central-station installations. SMUD has recognized that competition must be maintained to help reduce prices. So little standardization exists that the cost is driven upward to redefine mechanical and electrical interfaces for each vendor. New structures are required for each vendor and nonoptimum field geometries result from attempts to include more than one vendor in an array field. Standards at some hardware level are required.

Areas of Standardization

Jet Propulsion Laboratory has already made significant progress in identifying standards for environmental stability and operational stability. The American Society for Testing Materials (ASTM), European Community and IEC are involved in preparation of performance measurement standards. However, significant areas of required standards still exist. The system design standards for safety, wiring, grounding and system protection have an impact on PV interfaces. The mechanical and electrical interfaces, however, are the most critical areas needing design standardization.

Mechanical and Electrical Interfaces

Placing maximum limits on panel size will allow structure designers to bound their sizing calculations, and standardizing attachment points relieves the limitations on mechanical design. Standard panel voltages and hot-spot criteria will enable the system designer to address reliability and system performance. Eventually, panel annual performance and capacity factor values must become standard to establish planning for utilities. This is not necessary in the short term.

INTERFACE STANDARDIZATION

ACUREX CORP.

Robert Spencer
Vern Wong

System Design Requirements

MAXIMIZE VALUE TO OWNER
MINIMIZE INITIAL SYSTEM COST
MINIMIZE OPERATION COST
MAXIMIZE LIFETIME OF SYSTEM

> LOWEST NPV OF ENERGY AND CAPACITY

VALUE TO OWNER IS THE ENERGY & ON PEAK CAPACITY
TRACKING DESIGNS ARE RESULT OF PUSH FOR INCREASED VALUE

THE LONGER SYSTEM LIFE DEPENDS ON AVOIDING LIFE LIMITING DESIGNS
JPL QUALIFICATION TESTING PROGRAM HAS PROVIDED MOST INFORMATION

MINIMIZING COSTS OF COMPONENTS AND OPERATION DEPEND ON STANDARDS

Why Standards?

MASS PRODUCTION OF BOS COSTS

DEFINED BOUNDARY CONDITIONS FOR COMPONENTS

NO SPECIALS OR JOB SPECIFIC DESIGNS FOR BOTH MANUFACTURER AND BOS DESIGNER

MANUFACTURER'S PRODUCTS ARE MORE DIRECTLY COMPARABLE

What to Standardize

MOUNTING INTERFACE

MAXIMUM PHYSICAL SIZE AND WEIGHT

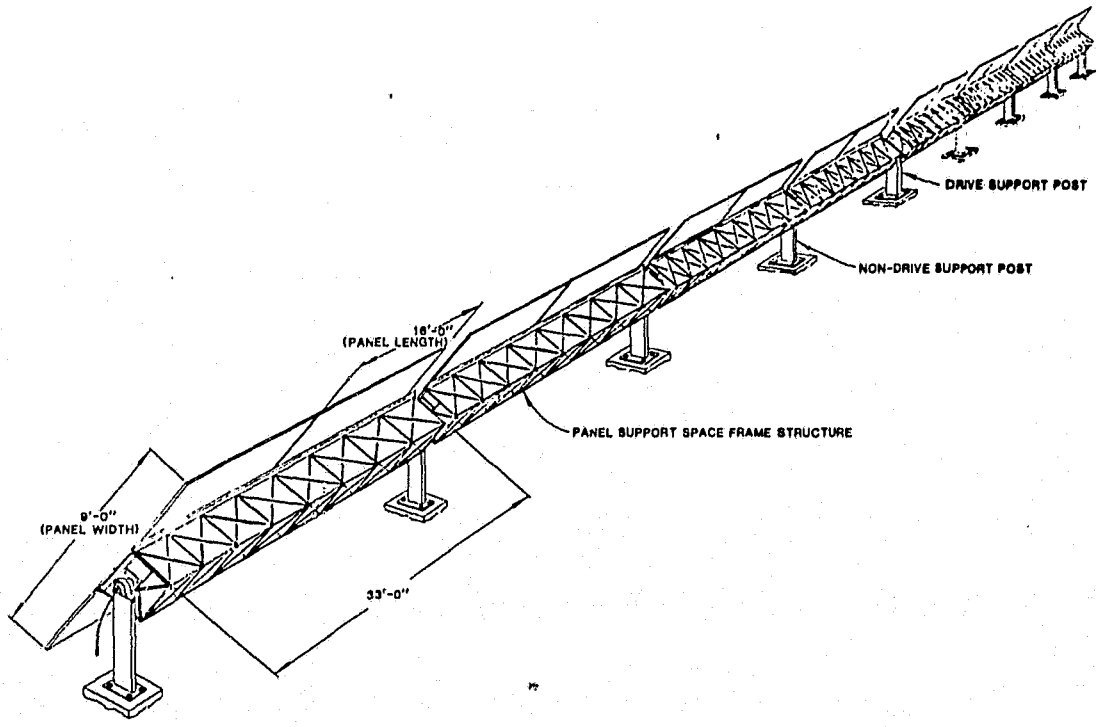
ENVIRONMENTAL STABILITY

ELECTRICAL INTERFACE

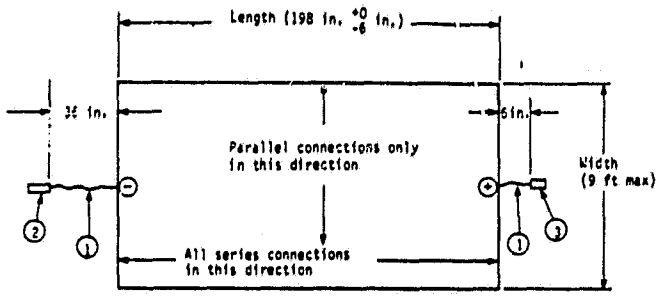
CIRCUIT CONFIGURATION

PANEL VOLTAGE

Array Design



Electrical Constraints



- SELECT GROUP OF PANEL VOLTAGES

Panel-Mechanical Interface: Envelope Standardization

REQUIREMENTS	DESIGN IMPACT
PANEL LENGTH, 16'-6", +0 -6"	• SUPPORT STRUCTURE OPTIMIZATION - LENGTH - STRUCTURAL STIFFNESS - WEIGHT • SHIPPING CONSIDERATIONS OF PANEL AND SUPPORT STRUCTURES
PANEL WIDTH, 108" MAXIMUM	• SUPPORT POST OPTIMIZATION - HEIGHT - STRUCTURAL STRENGTH • SHIPPING CONSIDERATION OF PANEL
C.G. LOCATION ABOVE MTG. INTERFACE, 2.5" ± 0.1"	• C.G. BALANCE OF ARRAY ASSY • DYNAMIC (FREE-VIBRATION) ANALYSIS

Panel-Mechanical Interface: Panel Attachment Standardization

REQUIREMENT	DESIGN IMPACT
ATTACHMENT POINTS, 48" AXIAL SPACING	• COMMON INTERFACE FOR ALL PANEL SUPPLIERS FOR FIXED & ROTATING STRUCTURES • TRANSFER PANEL LOADS INTO THE SUPPORT STRUCTURE
ATTACHMENT POINTS, 48" LATERAL SPACING	• AS ABOVE • OPTIMIZE ATTACHMENT POINT LOCATION (¼ CHORD) ON PANEL

Panel-Mechanical Interface: Structural Standardization

REQUIREMENTS	DESIGN IMPACT
PANEL WEIGHT, 3.0 LB/FT	• C.G. BALANCE OF THE ARRAY • STATIC SIZING OF STRUCTURAL MEMBERS • DYNAMIC (FREE VIBRATION) ANALYSIS
PANEL LOADING, 15 PSF	• WIND LOADING AND DEADWEIGHTS TO SIZE PANEL FRAME, SUPPORT STRUCTURE, POSTS AND FOUNDATION
TORSIONAL DEFLECTION, ½ DEG/FT OF LENGTH	• HANDLING LOAD CONDITIONS • ARRAY ROTATION UNDER WIND APPLIED PITCHING MOMENTS
CORROSION PROTECTION	• SATISFY 30-YEAR SERVICE LIFE - PANEL FRAME - SUPPORT STRUCTURES & POSTS • MATERIAL SELECTION - COMPATIBILITY - UV STABILIZED - WEATHERABILITY

D18

EVOLUTION OF INTEGRATED PANEL STRUCTURAL DESIGN AND INTERFACES FOR PV POWER PLANTS

J.C. Arnett, A.J. Anderson and R.E. Robertson
ARCO Solar Industries
Woodland Hills, California

Historically, framed PV modules of about 1 x 4-ft size have been individually mounted in the field on fixed support structures and interconnected electrically with cables to build higher-power arrays. When ARCO Solar saw the opportunity in 1982 to marry its PV modules with state-of-the-art heliostat trackers developed by ARCO Power Systems, it became obvious that mounting individual modules was impractical. For this project, the framed modules were factory-assembled into panels and interconnected with cables before being mounted on the trackers.

Since then, ARCO Solar has made considerable progress and gained substantial experience in the design and fabrication of large PV panels. Constraints and criteria considered in these design activities included static and dynamic loads; assembly and transportation equipment and logistics; structural and electrical interfaces, and safety and grounding concerns. This evolution of integrated PV panel design at ARCO Solar is discussed.

EVOLUTION OF INTEGRATED PANEL STRUCTURAL DESIGN AND INTERFACES FOR PV POWER PLANTS

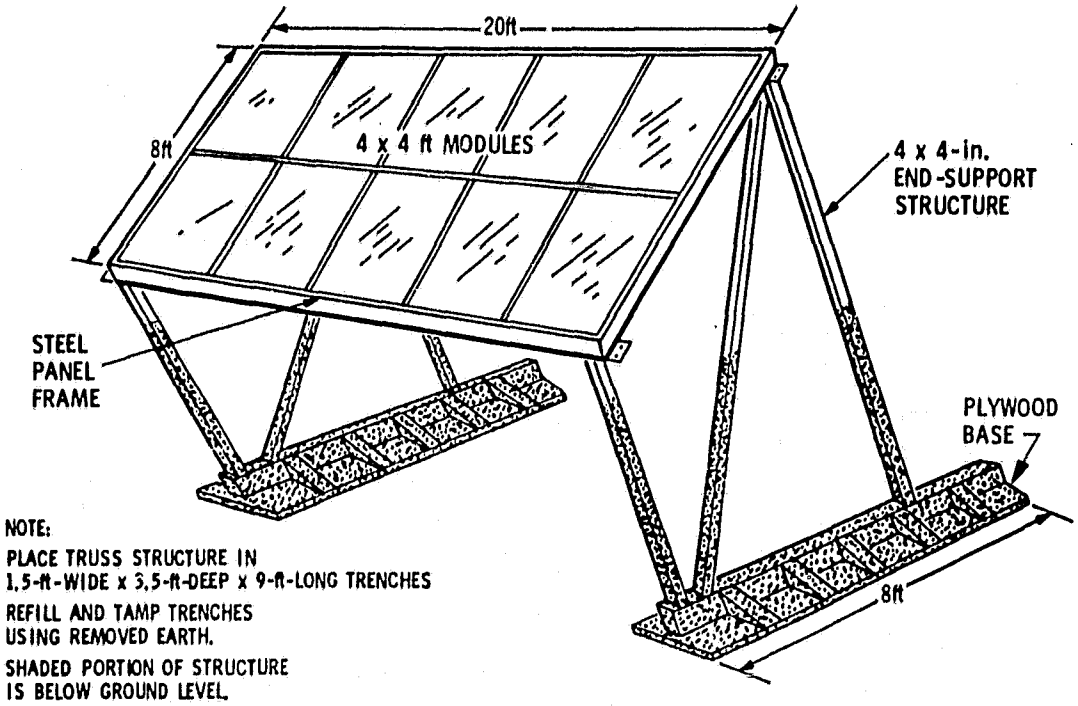
ARCO SOLAR INDUSTRIES

J.C. Arnett
A.J. Andeson
R.E. Robertson

Integrated Panel Evolution

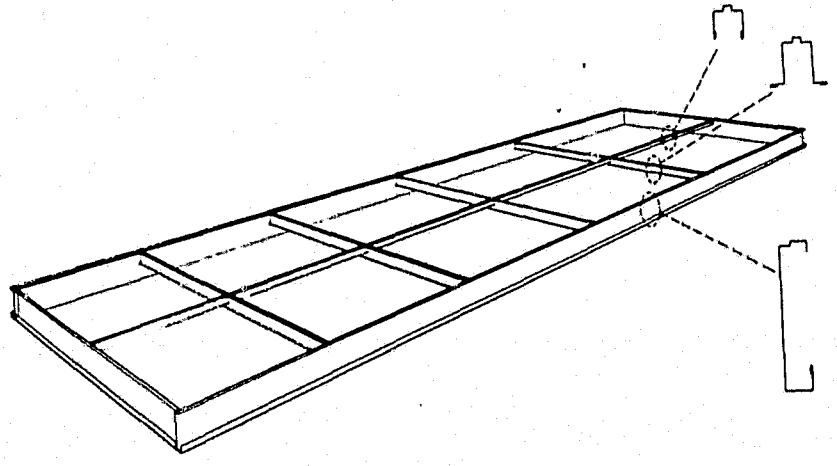
- FIXED TILT INSTALLATIONS
- STRUCTURAL DESIGN STUDIES
- LUGO PANEL (FACTORY ASSEMBLY)
- SMUD PV1 PANEL (FACTORY ASSEMBLY)
- CARRISA INTEGRATED PANEL
- SMUD PV2 INTEGRATED PANEL

JPL Low-Cost Array Structure

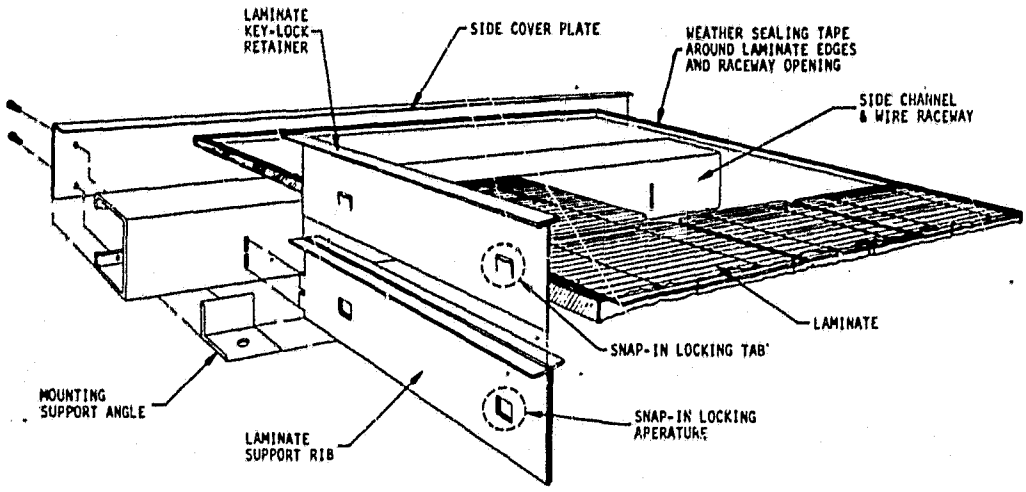


NOTE:
PLACE TRUSS STRUCTURE IN
1.5-ft-WIDE x 3.5-ft-DEEP x 9-ft-LONG TRENCHES
REFILL AND TAMP TRENCHES
USING REMOVED EARTH.
SHADED PORTION OF STRUCTURE
IS BELOW GROUND LEVEL.

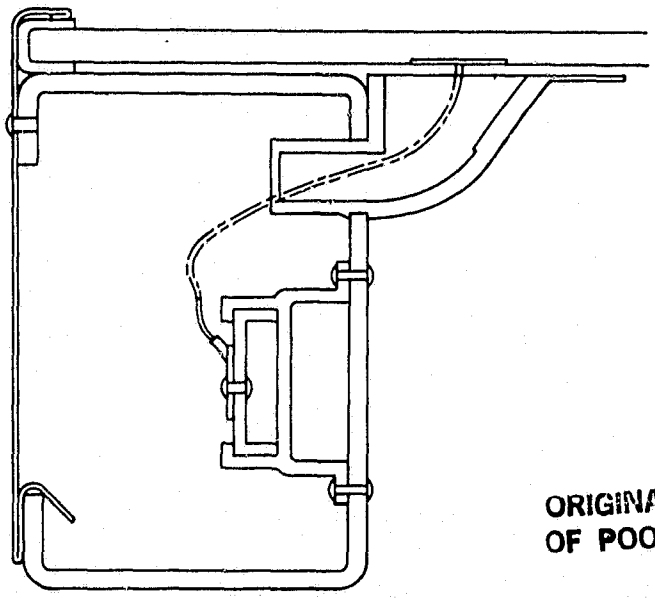
JPL Low-Cost Frame Structure



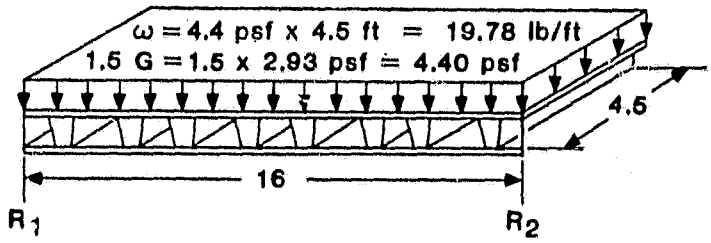
Exploded View of Integrated Support Structure



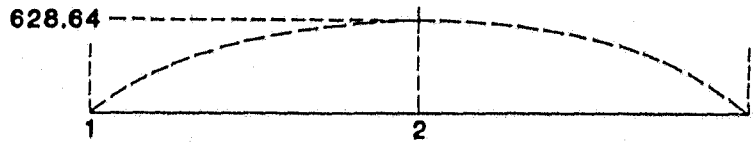
Carrisa Panel Section View



CROSSMEMBER LOADING DUE TO HANDLING



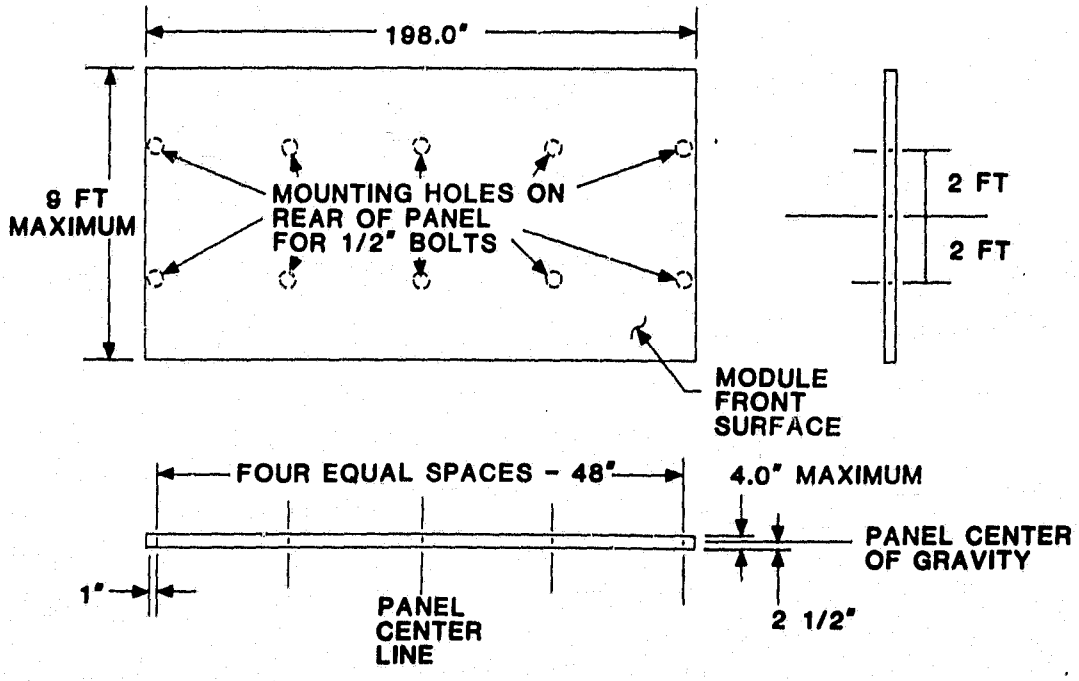
MOMENT DIAGRAM



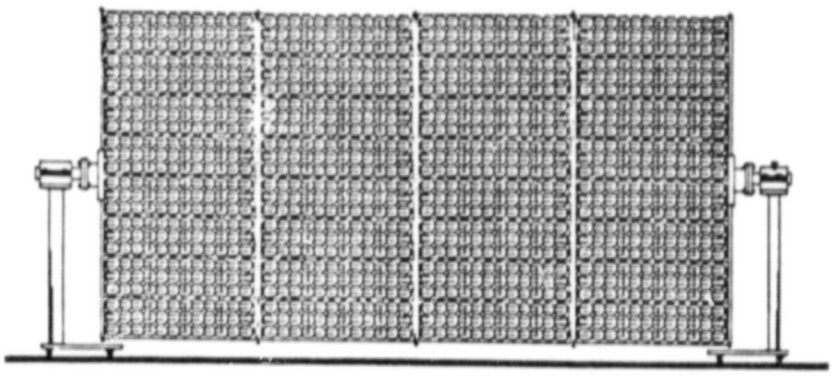
σb = 35,642 psi σtu = 50,000 psi

M.S. +0.40

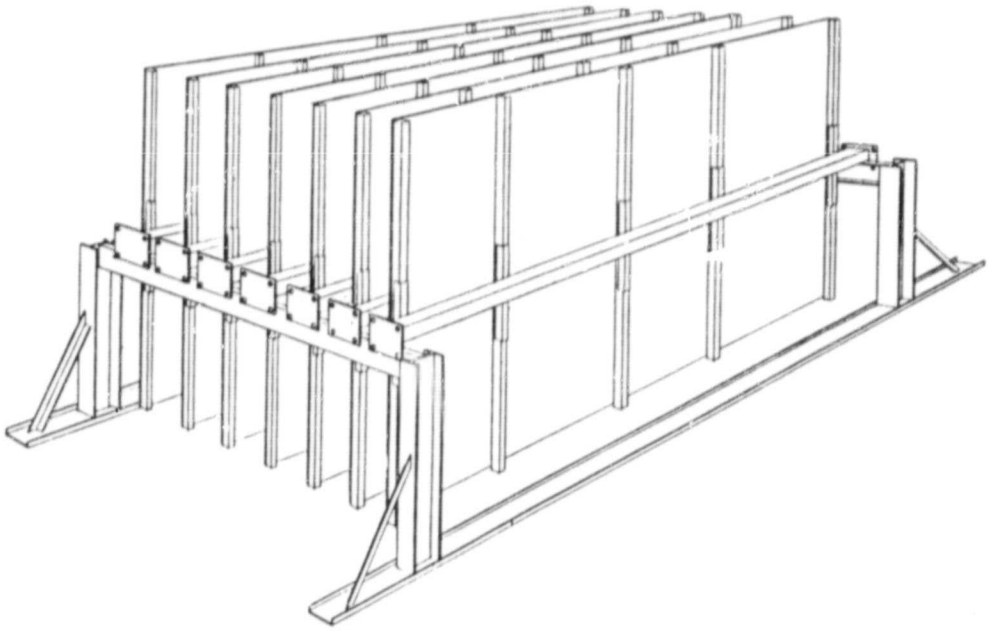
SMUD PV2 Interface



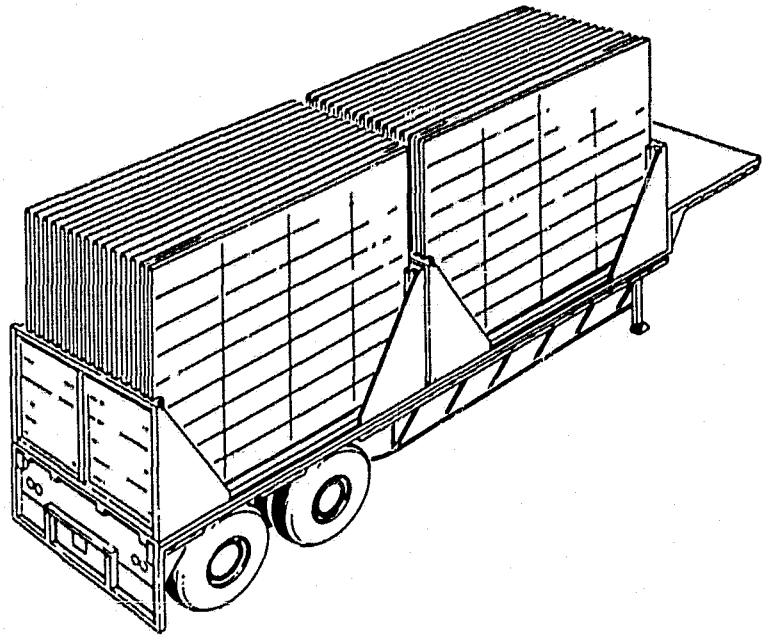
Panel Assembly Fixture for 8 x 16 ft SMUD PV1 Panel



Transit/Storage Rack for 8 x 16 ft SMUD PV1 Assembled Panels



Transit/Support Rack for 9 x 16 ft Integrated Panels on Low-Bed Trailer



Design Evolution Summary

- REDUNDANT STRUCTURE ELIMINATED
- ELECTRICAL GROUNDING SIMPLIFIED
- ELECTRICAL ISOLATION PROVIDED
- WEIGHT REDUCTION BENEFITS TRACKER
- PANEL SIZE INFLUENCED BY LOGISTICS

IS STRUCTURAL INTERFACE STANDARDIZATION BENEFICIAL?

W. E. Dombert
SOLAREX CORPORATION
Rockville, Maryland

INTRODUCTION

Almost everyone will agree that, generally, standards are necessary and beneficial. But in regard to standards for the structural interfaces established in the design of flat plate photovoltaic (PV) generator arrays for central power stations there are at this time important questions to be considered. While there appear to be in the power industry no structural interface standards for transformers, turbines and generators, switchgear, etc., the PV generator case is different: For one, there will be many thousands of similar, repetitive PV module and array elements in any one station, which would suggest possible benefits from standardization.

Central station flat plate systems can take the following four forms:

Fixed Angle, Large Field
1 Axis Tracking
2 Axis Tracking
Fixed Angle, Large Building

This presentation will discuss factors applicable to these types of systems; details given relate to the first and last; the previous two discussions have well covered details of the other approaches.

MODULE AND ARRAY HISTORICAL BACKGROUND

Historically, module and panel sizes and structural configurations have varied widely. There has been a developing and learning process in every aspect of the technology from cells through every assembly form and size up to and including kilowatt constructions. A brief look at a part of Solarex history will be instructive if an overlay of application to the four possible general system forms is also considered.

Figure 1 shows an array of 10-8½ watt Lexan-covered modules cemented to a reinforced steel plate. The rear view is shown in Figure 2. This construction represents the state-of-the-art of both modules and arrays of about 8 years ago. During the next six years cells, modules, and arrays each progressed through a number of generations of development.

Figure 3 is the rear view of an 8-module array using present production Solarex type SX-120 modules. It includes our standard structural elements and also shows a method used for cross-strapping modules. This eliminates two additional vertical rails and corresponding legs normally used. This cost-effective construction limits the rated wind velocity to about 90 MPH.

Figure 4 shows two 400 watt military application subarrays made from Solarex type SX-120 modules bolted to two longitudinal angles and centrally supported. The face size is 3½' x 15½'.

Figure 5 is a general view of a 17KW grid-interactive system installed about a year ago. Figure 6 is a rear close-up. There is a fixed central tube, welded angular clips and bolted vertical angles to which framed Solarex type PL-120 modules are fastened.

The Solarex "Breeder" shown in Figure 7 is an example of a large dual-purpose (array and factory) construction. This 200KW peak array face is 100' high and 368' long. The Solarex type PL-120 modules were gasketed, and individually clamped through cap-strips to a substructure "egg crate" of aluminum extrusions. This substructure is bolted to the primary steel structure, designed to withstand 110 MPH winds, shown in Figure 8. Modules were installed by means of a carriage which rode up and down the structure face. Non-framed gasketed Solarex modules are also being installed in the 300 KW peak grid-interactive Georgetown University facility in a program managed by Hughes Aircraft Company. The modules are mounted on the south wall and on a double-peaked roof of a 10-story building in Washington, D.C. These large array and building applications could well prefigure the distributed, yet central-station-controlled, power-producing south-wall of cities of the future.

PRESENT CONSIDERATIONS

Standardization subjects of general interest to the PV industry as a whole are listed in Figure 9.

In regard to environment, there is within the United States alone a very wide range of environmental conditions for temperatures, snow and hail, and for wind loadings. Designing modules and single structural solutions to these ranges would result in inefficient designs.

There are emerging third generation PV cell technologies, such as ribbon and amorphous, which will develop their own optimum physical module and array considerations. To the extent that industry groups can help channel the module forms for greater standardization, this could be a worthwhile service. However, premature standardization which would restrict the natural and optimum form of development could be expensive and self-defeating. In addition to the cell technology effects, the high reliability possibilities and the weight penalties of hermetically sealed modules, the cost and weight advantage potential of plastic faceplates and structures could all have as much impact on change of form and mounting methods in the future as have been experienced in the past.

Larger modules are being considered by many to be cost-effective in materials and labor; Solarex production and development sizes are listed in Figure 10.

Standardization topics of specific interest to Central Station Owners and other topics of interest to PV manufacturers are listed in Figure 11.

For systems which are designed for a 20- to 30-year life expectancy it makes little sense to assume that parts interchangeability between various manufacturers is necessary or desirable. It may even be impractical for the original manufacturer to provide an interchangeable element 10 or more years after manufacture.

Since PV systems are not yet economic in central power and many other applications, tax allowances and write-offs are necessary. The national energy allowance of 15% and the R&D allowance of 25%, and other tax benefits are highly beneficial. Uniqueness of structural design for the next few years rather than standardization could help justify and obtain R&D tax benefits.

The SMUD I program mechanical and structural design, while purposely adaptable to a variety of module sizes was thereby a relatively expensive structure; the SMUD II program structure, while less restrictive to module manufacturers, still represents a structural compromise and increased cost over a fully integrated design. This is not to say that there may not be other benefits to SMUD in using this design.

SUMMARY

The PV industry is evolving and developing as rapidly as in the past. There are a wide variety of applications both within and outside of the electric power Central Station requirements; there are a number of developing technologies and manufacturing practices; there are many desirable forms of power systems and of modules; there are a wide range of environmental limits to be considered; there is a need for effective cost reduction in line with each PV manufacturer's plant investment limitations.

Structural interface standardization may be highly desirable in any one major project, but not at this time in the overall PV industry. Attempts to mandate such standardization will act as a deterrent to long-range improvements. In specific projects structural standardization should be defined at the largest practical interface, leaving the maximum possible freedom to the module and array manufacturer.

There is a corollary area, however, where detailed standards would benefit the industry; the matter of Standard Practices. Work being done towards definition of acceptable/desirable practices in materials, finishes, fastening and locking methods, grounding techniques, lightning protection, etc., and in handling the environmental ranges, should be continued.

IS STRUCTURAL INTERFACE STANDARDIZATION BENEFICIAL?

SOLAREX CORP.

W.E. Dombert

Figure 1. Early Production 85-W Array

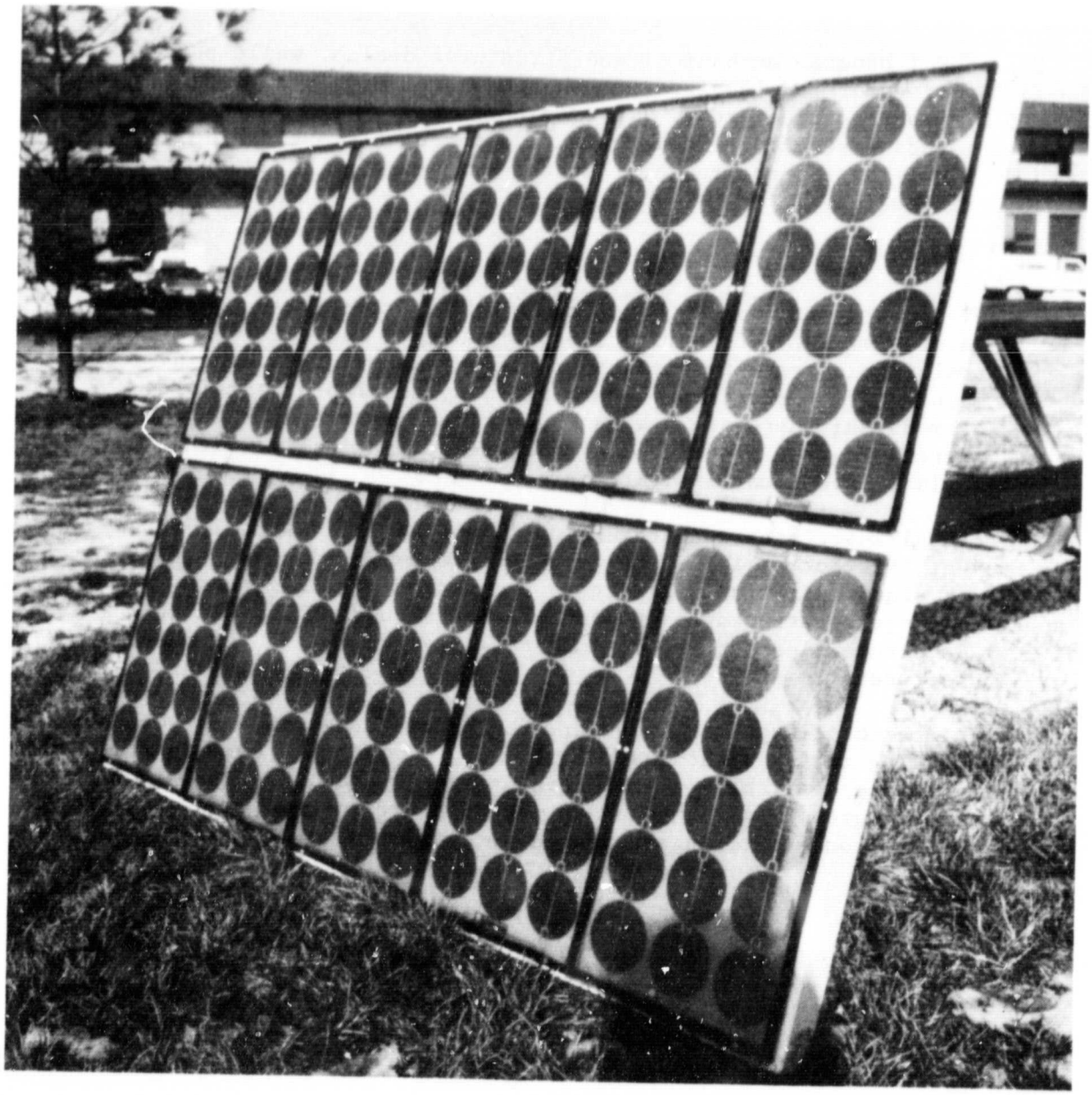


Figure 2. Array Steel Back Plate

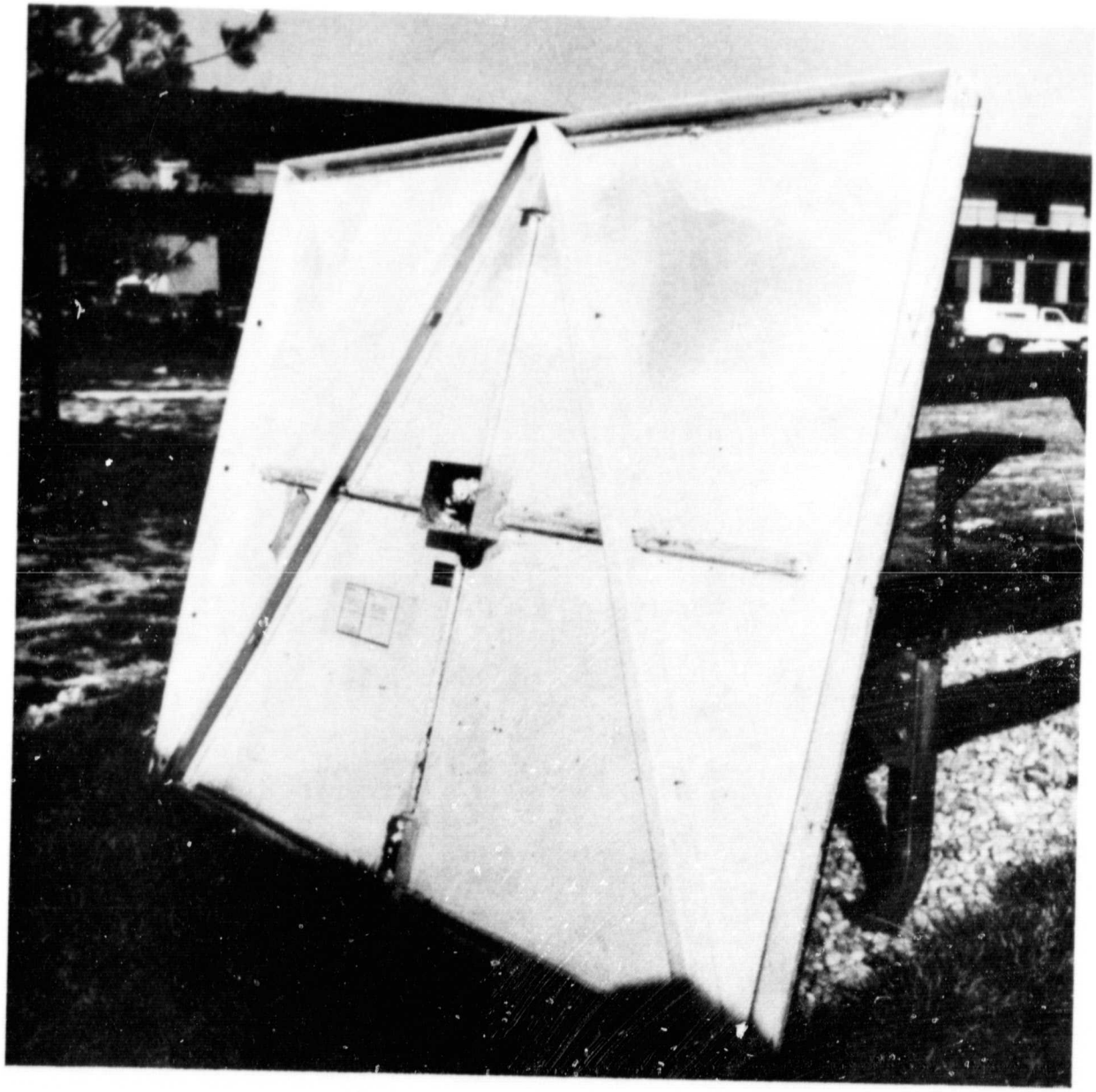


Figure 3. 320-W Configuration

Figure 4. Two 400-W Subarrays

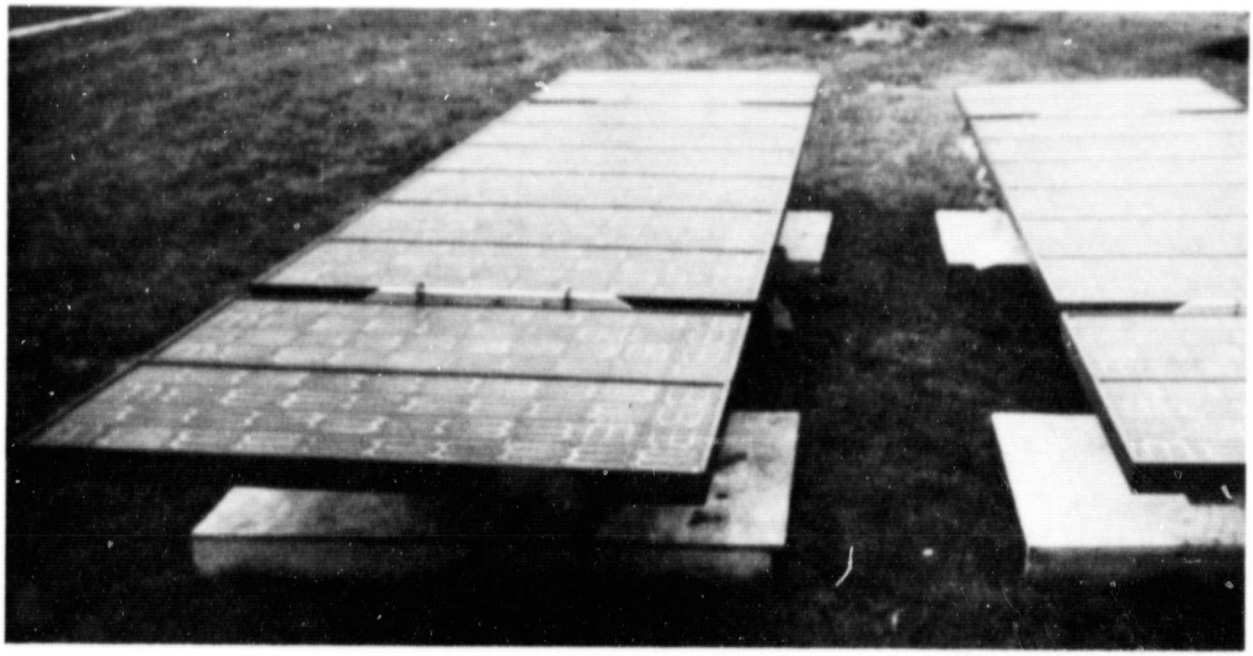


Figure 5. Grid-Interactive Power System

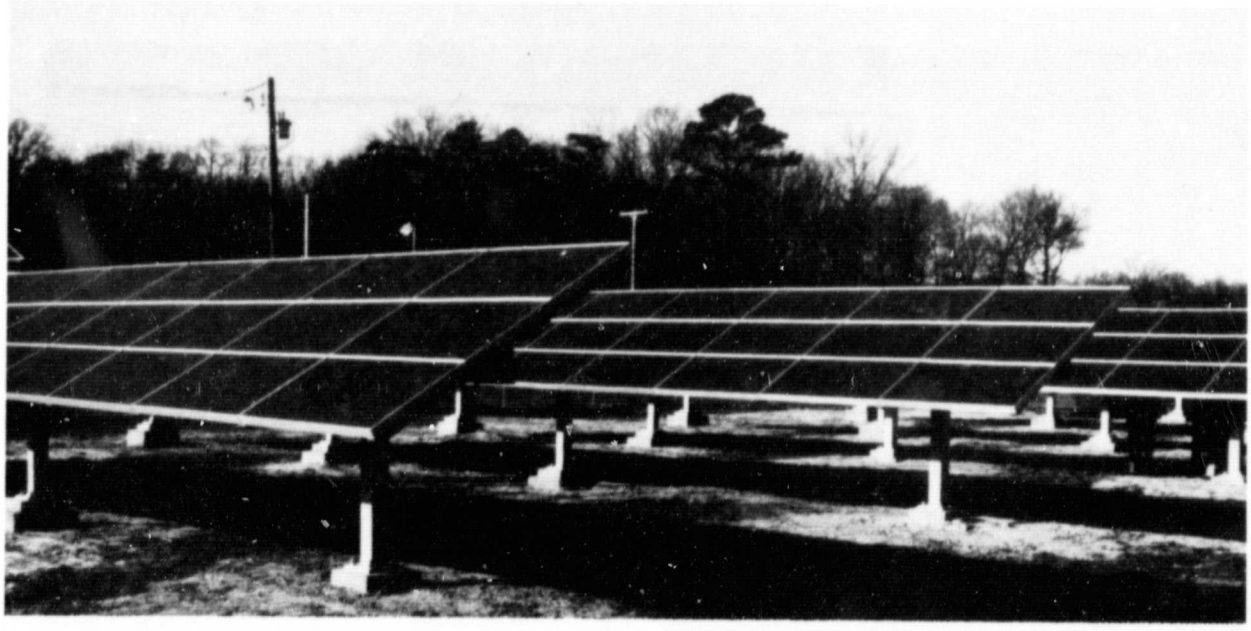


Figure 6. Closeup of PL-120 Mounting Structure

Figure 7. Solarex Breeder Array Face

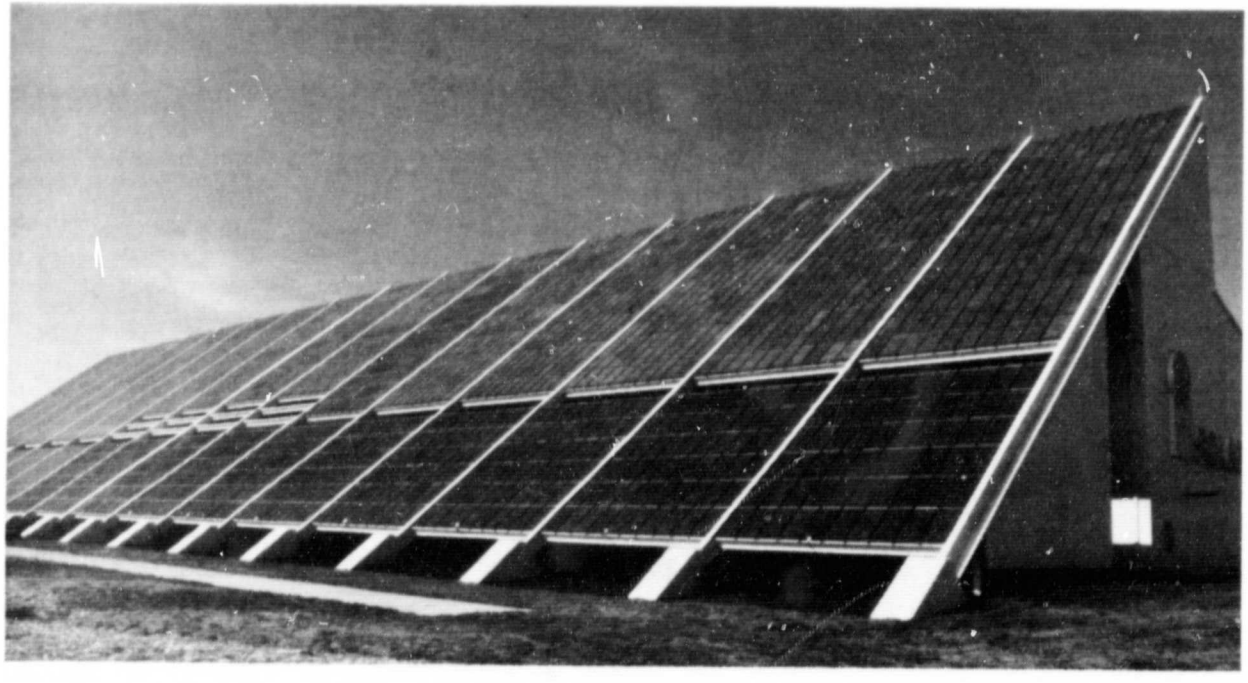


Figure 8. Breeder Array Primary Structure

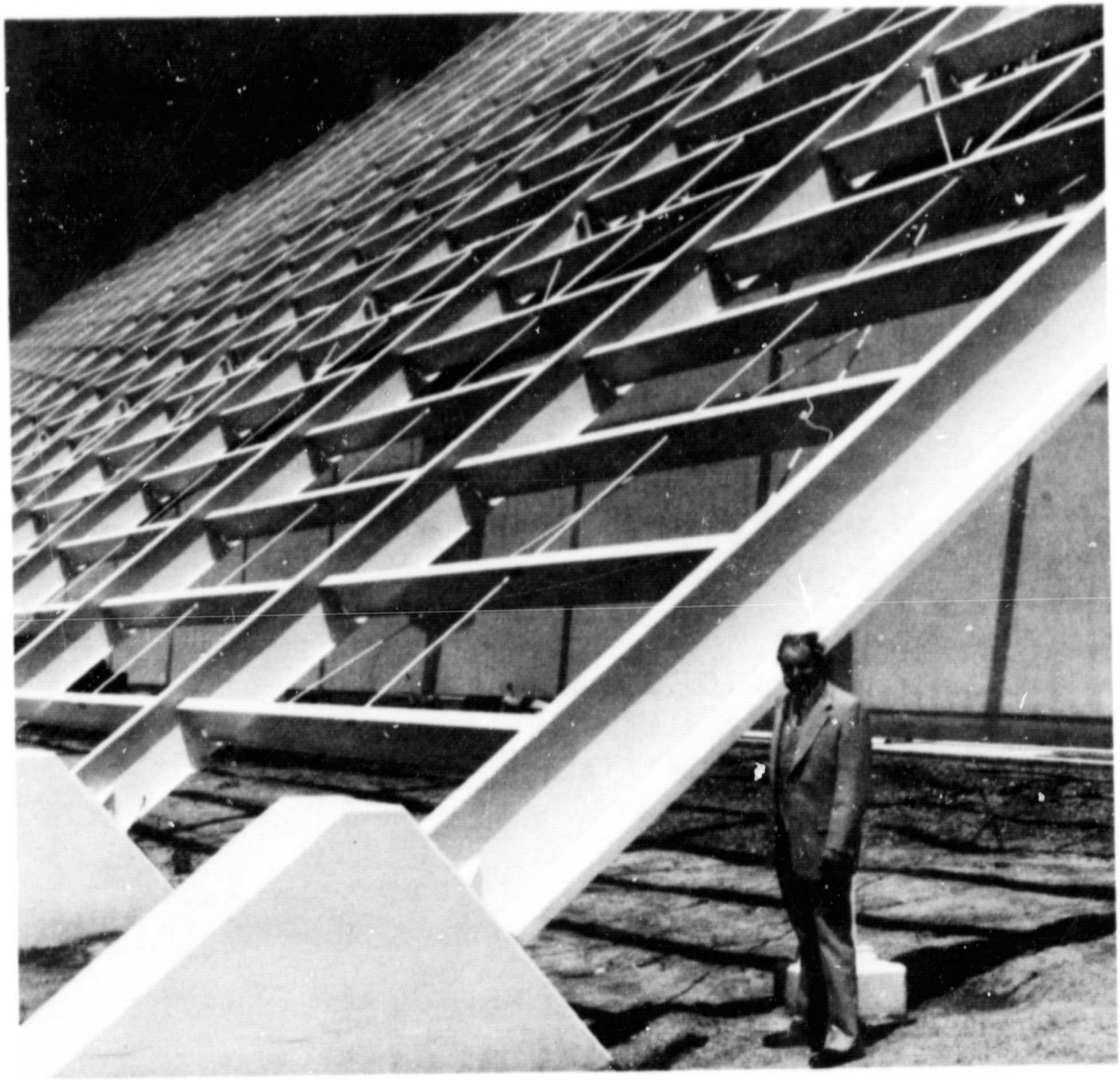


Figure 9. Standardization Areas of General Interest

- FORM, FIT, AND FUNCTION
- FRAMED VS. FRAMELESS MODULES
- SIZE OF MODULE/ARRAY
- ENVIRONMENTAL REQUIREMENTS RANGE
- RELATIVE POSITION OF "BOS" COSTS
- CONSIDERATION OF EMERGING TECHNOLOGIES
  - RIBBON AND AMORPHOUS
  - HERMETICALLY SEALED MODULES
  - PLASTIC FACEPLATES
  - PLASTIC STRUCTURES
  - LARGER MODULES

Figure 10. Solarex Large PV Modules

MODEL NUMBER	WATTS PEAK	FACE DIMENSION
SX-120	40	17.5" X 42.0"
PL-120	70	25.75" X 50.5" **
C-80-1	72	23.62" X 47.25" **
PL-200	80	25.25" X 54.5"
PL-300	130	38.0" X 54.5"
PL-400	160	25.25" X 109.0"
PL-600	260	38.0" X 109.0"

** MODULE MADE WITH A GASKET, NOT A FRAME.

Figure 11. Areas of Interest to Central Stations

- NUMBER OF COMPETITIVE SUPPLIERS
- COSTS OF REPLACEMENT PARTS
- EFFECT ON TAX CREDITS
- IMPETUS OF SMUD PROGRAM

AREAS OF INTEREST TO MANUFACTURERS:

- EFFECT OF STANDARD ON EXISTING MANUFACTURING
- ADAPTABILITY OF STANDARD PRODUCT TO OTHER APPLICATIONS

SUMMARY

- GENERAL STRUCTURAL INTERFACE STANDARDS NOT RECOMMENDED
  - TOO MANY DESIRABLE VARIABLES
- FOR SPECIFIC PROJECTS, STANDARDS MADE AT LEVEL OF LARGEST POSSIBLE INTERFACE
- DO DEVELOP STANDARD STRUCTURAL PRACTICES

SESSION V

QUALIFICATION TESTING AND ELECTRICAL MEASUREMENTS

L.D. Runkle, Chairman

OMIT TO P. 253 257

SESSION V

QUALIFICATION TESTING AND ELECTRICAL MEASUREMENT

Chairman: L.D. Runkle, Jet Propulsion Laboratory

SUMMARY

Speakers at the session on qualification testing and electrical measurements represented all facets of photovoltaic enterprise; a customer, two system contractors, one manufacturer and a national laboratory. The views presented avoided the particular biases one might expect from each organizational entity. The customer, a utility, concerned that PV is not yet 'tried and true' equipment, relied heavily on qualification, verification and electrical measurement procedures, provided by national laboratories to assure reliability and performance. The system contractor, likewise responsible for ensuring durability and performance, saw the qualification testing requirements as a vehicle for providing that ensurance. The particular manufacturer cautiously avoided enthusiastic endorsement of a standard qualification testing program, but in the course of tracing the evolution of the qualification requirements, seemed to concede that there were benefits. The representative of the national lab described in more detail the qualification tests used by the laboratory, related experience with the tests as a design tool, offered an assessment of the limitations and the logical constraints of the current test program, and offered some alternatives. The vital topic of electrical measurements was also addressed and the problems confronted by manufacturers and users alike elicited far more interest than did the techniques of the qualification testing.

During the discussions that followed the presentations, the remarks occasionally took a different emphasis than might have been expected from the title of the talk. In the case of the presentation of G.R. Cox of SMUD, the questioning was not about the levels and kinds of qualification testing but rather was directed at performance measurements. Items highlighted included (1) the fact that SMUD found it necessary to use a performance measurement standard produced by the Commission of European Communities for the simple reason that standards activity in the United States has not yet come up with one; (2) the need for a source of calibrated reference cells; (3) various procedural matters involving where the environmental exposures and performance measurements are done, (4) the need to understand the relationship between module production power measurements and field power measurements, and (5) the spectral irradiance distribution that is used in making the performance measurements.

Again, in the discussion following the talk given by M.I. Smokler of JPL, there was no commentary on the qualification testing parameters of levels; instead, the problems of electrical performance measurement were aired. Particular attention was drawn again to the problem of obtaining calibrated reference cells with which to perform the measurements. The present perception of the manufacturers is that reference cell calibration is a favor,

which is available only at JPL or SERI. It was pointed out that at least one commercial organization, DSET, can provide calibration, but that the spectral irradiance standards add confusion to the problem since for all practical purposes, DSET can provide a primary calibration only for a global standard spectrum, whereas present PV measurement practice for flat-plate collectors calls out a direct standard spectrum. Spotts of Tideland Signal reinforced the importance of establishing uniform measurement practices and mentioned a sequence of worldwide round-robin tests that his company is involved in to get a handle on repeatability and accuracy of measurement.

D.B. Cohen of Hughes Aircraft Co. provided the view of the system contractor for the Georgetown PHENEF Project in dealing with a module manufacturer to obtain qualified modules. He presented the requirements of the module procurement specification, which defined the electrical and mechanical characteristics of the module and the quality assurance provisions. The electrical performance characteristics and performance measurements procedures were carefully defined. Hughes solved the procedure problem by using as their own a draft ASTM standard to obtain globally calibrated reference cells, and then established their own procedure for performance measurement. For qualification testing, Hughes chose to adopt the JPL Block V requirements and added other requirements as well, including an Underwriters Laboratories fire-resistance test. Hughes also expanded acceptance testing to include a diode verification test as well as visual inspection, hi-pot, and electrical performance. The Hughes procedures governed reference cell calibration, use of calibrated modules, simulator verification, performance measurement and source inspection. This attention to detail represents the approach of one sophisticated customer in purchasing photovoltaic modules. As in the previous presentations, the discussion focused upon the problems of performance measurement, once again highlighting the absence of acceptable standards that could facilitate commerce.

In the talk presented by J.C. Arnett of ARCO Solar, the meeting finally addressed the environmental requirements of the qualification tests. It became clear that the manufacturers are very wary of the effect on commerce of the qualification requirements imposed by JPL on its contractors in the course of the module development program. Although the specifications written by JPL were for the purpose of increasing the reliability of modules, which they were effective in doing, they are also perceived as qualification standards, which they are not. The tendency is for a customer (if he is aware of the DOE program) blindly to demand compliance with the latest JPL specification regardless of the application. This is, of course, because there is no other U.S. specification or standard available to use. The forum was also told that manufacturers <u>do</u> perform environmental stress tests on their own modules, but not necessarily or even usually the same tests as are used by JPL. The sense that environmental tests are useful in some as yet unknown way to determine lifetime but should not be imposed by an agency external to the manufacturer emerged during this presentation.

T.J. Lambarski of BDM presented the paper on "Qualification Testing for a Central Station," prepared by D.L. Forrester. The hierarchy of management of the Lugo 1-MW facility, an ARCO project, clearly shifted the emphasis of this discussion from module and array qualification testing to central-station qualification. Lambarski described the Lugo facility and the tests that

generally confirmed the operation and safety of individual trackers, dc switchgear, ac components, tracker control, the data acquisition system and systems-level operations and control. Although there was considerable discussion of various system test problems, there was no discussion of overall system efficiency measurements or the basis for determining electrical performance.

Standing back and considering the papers and discussion in this session, devoted to qualification and electrical performance measurements for photovoltaic solar arrays in central stations, a number of observations and conclusions can be drawn. In no particular orders, they are:

1. There is a dichotomy over the need for formal qualification testing of photovoltaic modules or arrays. The manufacturers believe that they are now part of a mature industry that knows what it should give the customer. The customers, whether system contractor or utility, do not perceive the solar industry as fully matured and still want independently imposed qualification criteria.

2. The status of performance measurements standards provides a dilemma for customers and manufacturers alike. With no consensus performance measurement standard, there is no common base for comparing the performance of competing modules.

3. Manufacturers, national laboratories and the user community give inadequate support to the development of voluntary consensus standards for electrical performance, but until these come into being and are consistently applied, the photovoltaic industry will <u>not</u> be perceived as mature.

UTILITY POLICY TOWARD QUALIFICATION TESTING AND ELECTRICAL MEASUREMENT

Graeme R. Cox
Sacramento Municipal Utility District
Sacramento, California

The responsibility of any electric utility is to provide its customers with a reliable power supply. Attaining this goal requires reliable equipment and systems, from turbine generators to switchgear to overhead lines. In many cases, there is adequate reliability history on which decisions can be based. However, in some cases, testing is required to determine the reliability of new and unknown equipment and systems. In the instance of photovoltaics, such testing includes qualification (QT), verification (VT), and electrical measurement (EM) tests.

It has been and will continue to be SMUD's policy to employ QT, VT, and EM in order to provide the reliability assurance required for the SMUD PV Project. Qualification testing is used to help determine the long-term effects of environmental exposure on laminates and modules and to provide information on possible failure mechanisms under various conditions. In the past, SMUD asked manufacturers to provide this information for review. However, in future phases, SMUD will be conducting its own QT to assure both adequate test conditions and uniformity of testing between manufacturers. Verification testing is used to determine environmental effects on assembled subsystems, such as an array; to evaluate performance features, such as tracking accuracy; and to evaluate the operations and maintenance requirements of the system. As PV technology evolves, SMUD will perform these tests, not only in the area of manufacturing, but also in the area of panel and array design. Electrical Measurement provides the basis for payment ($/W) and produces data used in project planning. SMUD will be expending more effort to refine this process in areas such as reference cell calibration and air mass correlation in order to increase its accuracy, and therefore, its value to SMUD.

Some requirements of testing may be relaxed, such as certain qualification tests, while others may be tightened in order to provide not only SMUD, but the industry as a whole, with both better understanding and more reliable photovoltaics in the future.

QUALIFICATION, VERIFICATION AND ELECTRICAL MEASUREMENT TESTING APPROACH FOR THE SMUD PV PROJECT

SACRAMENTO MUNICIPAL UTILITY DISTRICT

Graeme Cox

Background

- District's responsibility to ratepayers
- Need for reliable equipment and systems to meet this requirement
- Purchase "tried and true" equipment whenever possible
- Experience and operational history required with bids from equipment vendors
- Some equipment has no operational history to draw on
- Audit and source inspect heavily in these cases
- Due to the nature of PV, more is required
- This is where Qualification, Verification and Electrical Measurement Testing comes in for the SMUDPV Project

Qualification Testing (QT)

- District's policy to use QT to evaluate long term effects of environmental exposure on laminates/modules
- Tests covered: T-50,T-200,H-F,MI,Twist,Hot Spot, Hi-Pot,Ground Continuity,Power Degradation
- District required manufacturers to provide QT data in Phase I
- Modules used as test sample
- District to perform QT in current and future phases
- Assures better consistancy of testing methods
- Assures better testing uniformity between manufacturers
- Current and future QT will cover: T-50,T-200,H-F, Hi-Pot,Ground Continuity,Power Degradation
- QT will not cover: MI,Twist,Hot Spot
- Sub-panels to be used as test samples

Verification Testing (VT)

- District's policy to utilize VT to evaluate: environmental effects on sub-systems, performance, O&M
- VT performed by Acurex, District's A&E
- Specific VT covered: static loading,natural frequency, system grounding,mechanical operation,tracking accuracy, hot spotting,generation performance
- In current and future phases, District is to continue VT as both new products develop (i.e. amorphous technology) and as system design changes(i.e. array structures, tracking mechanisms)
- Example: Aluminized steel vs. Galvalume

Electrical Measurement (EM)

- District's policy to use EM to define power, which is the basis for payment ($/W), and for future planning
- Phase I area of concern: Reference cell calibration
- In current and future phases, vague areas are to be clarified
- From a utility standpoint, there is a very real need for a national/international standard for PV EM

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QUALIFICATION TESTS AND ELECTRICAL MEASUREMENTS: PRACTICE AND PROBLEMS

JET PROPULSION LABORATORY

Melvin I. Smokler

As part of the Flat-Plate Solar Array Project, JPL has subjected 138 different module designs to qualification tests and has performed electrical measurements on well over a thousand modules representing more than 150 designs. From this experience, conclusions are drawn regarding results and problems, with discussion of the need for change or improvement.

The qualification test sequence has included application of environmental and electrical stresses to the module. With few exceptions, the tests have revealed defects necessitating module design or process changes. However, the continued need for these tests may be questioned on the basis of technical and logistical factors. Technically, the current test sequence does not cover all design characteristics, does not include all field conditions and is not known to represent the desired 30-year module life. Logistically, the tests are time-consuming and costly, and there is a lack of fully qualified independent test organizations.

Alternatives to the current test program include simplification based on design specification and site environment, and/or the use of warranties or other commercial practices. These approaches do not seem adequate to permit elimination of qualification tests. Therefore, it appears important to improve the test scenario and to continue the use of qualification tests.

Electrical measurement at JPL has included the use of the Spectrolab LAPSS, the manufacture and sunlight calibration of reference cells according to the existing standard, and supplying JPL contractors with such cells. Nominal Operating Cell Temperature (NOCT) and module temperature coefficients have also usually been measured so that data could be referred to NOCT as well as to standard temperatures. Performance has usually been determined at 100 mW/cm^2 irradiation only. This system has proven satisfactory in that it is repeatable and in that contractor data has usually correlated well with JPL data. However, the system does not address problems of measurement in commercial practice, such as the need for additional measurement standards, the need for better solar simulators (for production use) and the lack of a source of calibrated reference cells.

A more complex commercial problem is the difficulty of purchasing modules in terms of price per unit performance under field conditions. This approach requires definition of field conditions, translation of field conditions to production test conditions, and timely determination of module NOCT and of module measurement coefficients.

Purpose of Qualification Test

To obtain timely evidence that a photovoltaic module of a specific design will meet its performance requirements during field operation

JPL Block V Qualification Test Program: Major Elements

- **Temperature test**
  200 thermal cycles; period 6 hours or less; -40°C to +90°C
- **Humidity-freeze test**
  85°C - 85% RH soak; 10 days; temperature dropped to -40° once per day
- **Mechanical load cycling test**
  10,000 cycles; peak amplitudes ± 2.4 kPa
- **Twist test**
  Mount deflected to 20 mm/m of module width
- **Hail test**
  Simulated hail impact on front of module; hail diameter 25.4 mm; hail velocity 23.2 m/s
- **Hot-spot test**
  100-hour operation with cells in back bias
- **Degradation evaluation**
  Power measurement; ground continuity; high voltage isolation; visual inspection

JPL Qualification Test Experience

- **138 Designs tested**

  Sources: Blocks I through V programs; commercial procurements

  Design details: Variety of cell sizes, shapes, materials
  Variety of collector, interconnect and circuit designs
  Silicone rubber, PVB and EVA encapsulants
  Variety of superstrates, substrates
  Variety of module sizes and frames
  Variety of terminal configurations and materials

- **For more than 95% of the designs, the tests revealed design or processing defects**

  Examples:
  Encapsulant delamination or breakdown
  Insulation breakdown
  Interconnection failures
  Cell cracks
  Short circuits
  Terminal box distortion
  Structural failure of frames
  Ground continuity failures

Technical Limitations of the Block V Test Sequence

- **Does not cover all design characteristics**
  - **Bypass diodes**
  - **Current imbalance (hot-spot test)**
- **Does not cover all field environments**
  - **Ultraviolet radiation**
  - **Salt spray**
  - **Back-side hail**
  - **Dirt, dust**
- **Does not cover all safety requirements**
  - **Fire resistance**
- **Is not correlated to 30-year life**

Logistical Constraints of Qualification Testing

- Inadequacy of independent commercial test facilities
- Time required for test sequence
- Cost of performing tests
- Limitation in allowable dimensions of test samples

Technical Alternatives

- Make test application-specific

  Possible changes: Reduce peak mechanical load
  Increase hail parameters
  Add back-side hail test
  Improve hot-spot test
  Add diode test
  Add salt spray test
  Add fire resistance

- Specify some proven design details and eliminate some tests

  Examples: Specify superstrate, eliminate hail test
  Specify superstrate or substrate and frame detail, eliminate mechanical loading test
  Specify diode frequency, eliminate hot-spot test

  Risks: No check on assumptions
  No check on current processes

Commercial Alternative: Warranty

- Can be made long enough to protect against infant mortality
- Can possibly be made long enough to detect some design and processing problems
- Can probably not be made long enough to secure adequate life

IMPORTANCE: For PV, the required operational life is critical to economic viability

Qualification Test Practice and Problems: Conclusions

- To date the tests have proven necessary
- The test sequence should be expanded to overcome current technical limitations
- A solution is needed to the inadequacy of independent commercial test facilities
- A solution is needed to the practical limitations on test sample dimensions
- Some alternative measures can be employed to reduce test stresses and/or eliminate some tests, thus reducing cost and time required

JPL Electrical Measurements Experience: Blocks I to V Practice

• Simulator:	Spectrolab LAPSS
• Reference cells:	Manufacture and sun-calibrate reference cells (direct normal irradiance) made from cell material supplied by module contractors; supply reference cells to contractors
• Temperature coefficients:	Measure on modules in temperature chamber or extrapolate from cell measurements
• NOCT:	Measure on module
• Measurement sequence:	Measure module at lab temperature under 100 mW/cm^2 irradiance Extrapolate to standard temperature and to NOCT

JPL Electrical Measurements Experience: Block V Variants

- **Simulator:** Now filtered to AM1.5 spectrum
- **Reference cells:** Not manufactured by or provided by JPL

  (but secondary calibration service is now available to contractors)
- **Temperature coefficients:** Not measured; use common values according to generic cell process

JPL Electrical Measurements Experience: Results

- **Repeatability:** ± 1.5%
- **Correlation with contractor data (Block III): within 3%**
  - **Contractor sources:** Sun
    Tungsten
    Xenon

Measurement Problems

- JPL
  - Reference cells: Lengthy procedure for primary solar calibration
  - NOCT Measurement: Lengthy procedure
  - Temperature coefficient measurement: Module size has outgrown facility size
- INDUSTRY
  - Reference cells: No independent commercial sources
  - Simulators: Excessive irradiance nonuniformity in production equipment
  - Measurement procedure: Lack of adequate standards

- COMMERCIAL
  - Present (STC) rating system does not reflect field conditions
    - Module price comparisons not realistic
    - No incentive for optimizing design for field irradiance and temperature
  - Rating system difficulties
    - Definition of field conditions
    - Module evaluation for field conditions
      - Measurement complexity
      - Timely evaluation of NOCT and temperature coefficients
      - Conversion of field conditions to production test criteria

Measurement Practice and Problems: Conclusions

- **JPL measurement practice has been satisfactory for JPL contracts**
- **A solution is needed to the inadequacy of independent commercial sources for reference cells**
- **A solution is needed for irradiance nonuniformity**
- **Better measurement procedures and standards are needed**
- **A practical means is needed for procuring modules at prices that relate to field irradiance and temperature conditions**

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QUALIFICATION AND TESTING OF MODULES

Dean B. Cohen
Hughes Aircraft Company
Long Beach CA

This paper discusses the experience gained in procuring solar modules soon to be installed on the Photovoltaic Higher Education National Exemplar Facility (PHENEF) at Georgetown University. The 300 KW peak Photovoltaic Array consists of 4464, 2' x 4', polycrystalline solar cell modules produced for Hughes by the Solarex Corporation. The performance requirements for the modules are described in a detailed, 19 page procurement specification which defines physical and electrical characteristics and extensive quality assurance provisions including requirements for an interface control drawing and qualification and acceptance testing.

MODULE ELECTRICAL CHARACTERISTICS:

72 Watts Minimum Lot Average at 16.2 Volts
67 Watts Minimum at 16.2 Volts
Measured at 1000 W/m^2, AM 1.5, 28 C
3000 Volt Electrical Voltage Insulation
3 Encapsulated Bypass Diodes (12 Cells/Diode)
Solarlok Connectors (UL Recognized)

Though the specification itself defines the basic design parameters, the vendor is required to generate an interface control drawing which identifies the configuration, dimensions, parts, materials, process specifications and quality assurance provisions used in module fabrication. This provided Hughes the opportunity to review and comment on all of the vendor's process specifications and quality assurance procedures used in the production of the PHENEF modules. The intent was not to dictate how the modules were made but, to insure receipt of the specified modules through proper documentation and controls. In addition, any significant revision to materials, processes and quality assurance procedures require Hughes approval.

Qualification testing requirements basically followed those defined in JPL's Block V Module Specification 5101-162; e.g.: Thermal cycle test, humidity freeze test, mechanical loading test, twisted mounting surface test, hail impact test and hot spot endurance test. The modules successfully passed those tests performed by JPL. Two additional qualification tests were imposed by Hughes: Shunt diode temperature monitoring during the Hot Spot Endurance Test and a Standard 790 Class C and a Fire Resistance Test performed by Underwriters Laboratories.

Acceptance testing requirements specify that the vendor subject every module to a full mechanical/physical examination, an electrical performance test, a voltage insulation test and a diode verification test. The voltage insulation test is performed on a sample of the roof mounting structure and must show less than 50 micro-amps at 3000 volts. The diode verification test guarantees that there are no shorts or opens in any of the three imbedded shunt diodes.

Electrical performance testing is conducted using five Hughes furnished reference solar cells calibrated by DSET Laboratories to ASTM procedures: "Standard Method for the Calibration and Characterization of Non-Concentrator Terrestrial Photovoltaics Reference Cells Under Global Irradiance". Two cells are retained by the vendor for performance testing, two are retained by the Hughes inspector for sample testing, and one is mounted on the PHENEF roof.

The electrical performance characteristics of two PHENEF modules were carefully determined. These two "calibrated" modules are used to verify that the simulator and its data acquisition system are properly functioning. The I-V curve of a calibrated module is obtained before and after daily acceptance testing. The daily calibrated module I-V curves must match the predetermined curves by $\pm$ 2% or acceptance testing is considered invalid.

Module matching is achieved by sorting the modules into 12 different current groups at 16.2 volts. Eighteen modules of the same current group form a ciruit and are packed in the same shipping container.

To assure the vendor properly performs acceptance testing on every module, Hughes samples a number of modules from each manufacturing lot repeating the acceptance tests described above. All sampled modules must be repeatable within $\pm$ 2% before the entire manufacturing lot (200-400 modules) is accepted by Hughes.

The implementation of this comprehensive quality asurance program has helped Hughes achieve a high level of confidence that the modules currently being delivered satisfy the PHENEF program requirements.

QUALIFICATION AND TESTING OF MODULES

HUGHES AIRCRAFT CO.

Dean B.Cohen

Georgetown University Photovoltaic Higher Education National Exemplar Facility (PHENEF)

320 kW PV ARRAY

4464 TOTAL MODULES

2 CELLS PARALLEL X 36 CELLS SERIES

9.3 cm X 9.5 cm POLYCRYSTALLINE CELLS

2' X 4' UNFRAMED

72 WATTS MINIMUM AVERAGE

SOLARLOK CONNECTORS, UL RECOGNIZED

3 SHUNT DIODES

Product Specification

HUGHES HUGHES AIRCRAFT COMPANY	TITLE PRODUCT SPECIFICATION SOLAR CELL MODULE PHENEF PROGRAM	NUMBER SEP 11395 CODE IDENT NO. 82577	REV I TOTAL PAGES

REVISIONS

EFF	AUTHORITY	LTR	DESCRIPTION	DATE	APPROVED
	DCN #390197	A	REVISED PER DCN #390197	5/26/82	
		B	Added Figure 1	7/9/82	
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		I	Revised per EO #1015	10-21-93	

APPROVALS

	DATE		DATE
Dean B Cox	5/12/82		
J.J. Wolff	5/12/82		

11611B CS JUN 74

Procurement Specification

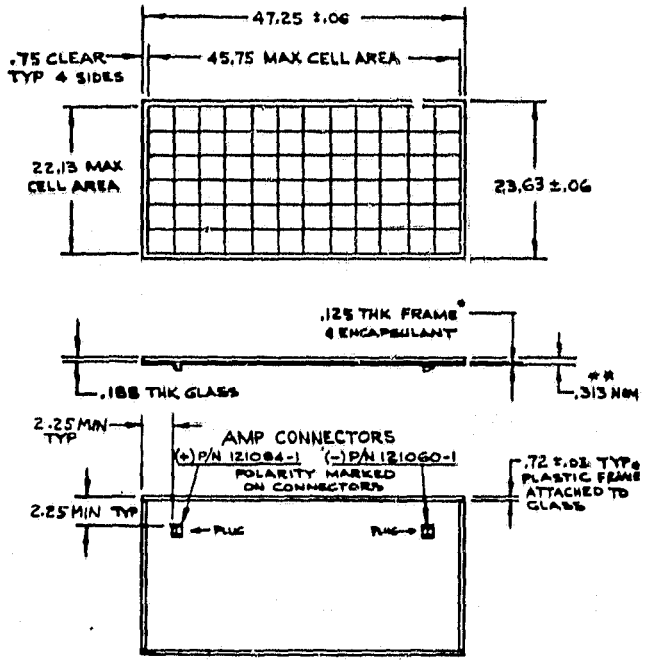
DEFINES:

- ELECTRICAL CHARACTERISTICS
- MECHANICAL CHARACTERISTICS
- QUALITY ASSURANCE PROVISIONS

Module Electrical Characteristics

- 72 WATTS MINIMUM LOT AVERAGE AT 16.2 VOLTS
- 67 WATTS MODULE MINIMUM AT 16.2 VOLTS
- MEASURED AT 1000 W/M^2, AM 1.5, 28^{o}C
- 3000 VOLT ELECTRICAL VOLTAGE INSULATION
- 3 ENCAPSULATED BYPASS DIODES (12 CELLS/DIODE)
- SOLARLOK CONNECTORS (UL RECOGNIZED)

Mechanical Characteristics



* PLASTIC "FRAME" PIECES TO BE FABRICATED FROM .125 THK FIBERGLAS FILLED POLYESTER LAMINATE.
** THE FRAME/GLASS/GLUE STACKUP DIMENSION MAY VARY ± .020 INCH MAXIMUM OVER THE ENTIRE FRAME SURFACE OF EACH MODULE.

Physical Defects (Rejections)

1. CRACKED OR BROKEN FRONT SURFACE.
2. DIRTY OR CONTAMINATED FRONT SURFACE.
3. CRACKED OR BROKEN CELLS WHICH:
   - A. ISOLATE A PORTION OF A CELL FROM + OR - INTERCONNECT.
   - B. THROUGH AN INTERCONNECT SOLDER JOINT.
   - C. ARE CAUSED BY POINT IMPACT.
4. CRACKED OR BROKEN INTERCONNECTS.
5. CELLS WITH UNSOLDERED SOLDER JOINTS.
6. LAMINATE VOIDS OR DELAMINATIONS IN EXCESS OF JPL 5101-21.
7. LOOSE OR BROKEN TERMINALS OR TERMINAL HOUSINGS.
8. BROKEN DIODES OR DIODE CONNECTIONS.

Quality Assurance Provisions

- o INTERFACE CONTROL DRAWING (ICD)
- o QUALIFICATION TESTING
- o ACCEPTANCE TESTING

Interface Control Drawing (ICD)

- o o SPECIFICATION DEFINES BASIC PARAMETERS
- o o INTERFACE CONTROL DRAWING IDENTIFIES:
  - o CONFIGURATION
  - o DIMENSIONS
  - o PARTS
  - o MATERIALS
  - o PROCESS SPECIFICATIONS
  - o QUALITY ASSURANCE PROVISIONS
- o o THE ICD AND SUBTIER DOCUMENTS MUST BE APPROVED BY HUGHES
- o o SIGNIFICANT REVISIONS TO ICD & SUBTIER DOCUMENTS MUST ALSO BE APPROVED BY HUGHES

Qualification Testing

- JPL's BLOCK V MODULE SPECIFICATION 5101-162

  THERMAL CYCLE TEST
  HUMIDITY FREEZE TEST
  MECHANICAL LOADING TEST
  TWISTED MOUNTING SURFACE TEST
  HAIL IMPACT TEST
  HOT SPOT ENDURANCE TEST

- ADDITIONAL TESTS

  SHUNT DIODE TEMPERATURE MONITORING DURING HOT SPOT ENDURANCE TEST
  UNDERWRITER'S LABORATORIES #790 CLASS C FIRE RESISTANCE TEST
  WALKABILITY TEST

Shunt Diode Temperature Monitoring

- THREE DIODE WAFERS POTTED WITHIN MODULE
- NOT PERFORMED DURING JPL HOT SPOT ENDURANCE TEST
- DIODE TEMPERATURE MONITORED:

  MODULE SHORT CIRCUIT THROUGH DIODE

  100 HOURS

  NO DELETERIOUS EFFECTS

Acceptance Testing

- EACH MODULE SUBJECT TO:
  - MECHANICAL/PHYSICAL INSPECTION
  - VOLTAGE INSULATION TEST
    - <50 u AMPS @ 3000 VDC
    - USES SAMPLE OF ACTUAL SUPPORT STRUCTURE
  - DIODE VERIFICATION TEST - OPENS & SHORTS
    - ACCEPTABLE (I-V) CURVE SHOWS NO SHORTS
    - DARK REVERSE VOLTAGE SHOWS NO OPENS
  - ELECTRICAL PERFORMANCE TEST
    - I-V CURVE @ 1000 W/M^2, AM 1.5, 28°C
    - I @ 16.2 - CURRENT GROUPS
    - HUGHES SUPPLIED REFERENCE CELLS

Reference Cells

- FIVE 2 X 2 CM CELLS PROVIDED BY SOLAREX
  - 2 EA. - SOLAREX FOR ACCEPTANCE TESTING
  - 2 EA. - HUGHES SOURCE INSPECTION FOR SAMPLE VERIFICATION
  - 1 EA. - MOUNTED ON PHENEF ROOF
- IDENTICAL IN TYPE TO MODULE'S CELLS
- FABRICATED AND CALIBRATED BY DSET LABORATORIES, ARIZONA
- TO ASTM DRAFT DOCUMENT #178 "STANDARD METHOD FOR THE CALIBRATION AND CHARACTERIZATION OF NON-CONCENTRATOR TERRESTRIAL PHOTOVOLTAIC REFERENCE CELLS UNDER GLOBAL IRRADIANCE"

Reference Cell Calibration

- o GLOBAL CALIBRATION
- o NATURAL SUNLIGHT
- o CALIBRATED AGAINST CALIBRATED PYRANOMETER
- o CONDITIONS:
  - INTENSITY $> 900\ W/M^2$
  - INTENSITY STABILITY $< \pm 0.5\%$
  - TURBIDITY COEFFICIENT .267 ± 5% @ $\lambda = 0.5$ MICROMETERS
  - AIRMASS $1.0 < AM < 2.0$
  - WATER VAPOR $0.75 < WV < 2.25$ cm
  - PRODUCT $1.0 < (AM) \times (WV) < 3.5$
- o DATA - MINIMUM OF 5 MEASUREMENTS OVER AT LEAST 2 DAYS

Calibrated Modules

- o TWO MODULES
- o I-V CURVES GENERATED USING EACH OF 5 REFERENCE CELLS
  - EACH OF 5 REFERENCE CELLS
  - VENDOR SIMULATOR
- o AVERAGE I-V CURVE DETERMINED FOR EACH MODULE
  - (I.E. CALIBRATED I-V CURVE)
- o CHECKED USING JPL SIMULATOR

Simulator Verification

- CALIBRATED MODULE TESTED UNDER VENDOR SIMULATOR BEFORE AND AFTER ACCEPTANCE TESTING DAILY
- BOTH I-V CURVES MUST AGREE WITHIN ± 2% OF CALIBRATED I-V CURVE
  - ACCEPTANCE TESTING OF MODULES O. K.
  - VERIFIES SIMULATOR/DATA ACQUISITION SYSTEM
- NON-AGREEMENT - ACCEPTANCE TESTING NOT VALID

Hughes Source Inspection

- MANUFACTURING LOT 200 - 400 MODULES
- ALL DATA REVIEWED
- THREE MODULES SELECTED AT RANDOM
- FULL ACCEPTANCE TEST & INSPECTION REPEATED BY HUGHES INSPECTOR:
  - MECHANICAL/PHYSICAL INSPECTION -- WITHIN SPEC TOLERANCES
  - VOLTAGE INSOLATION TEST -- WITHIN SPEC TOLERANCES
  - DIODE VERIFICATION TEST -- WITHIN SPEC TOLERANCES
  - ELECTRICAL PERFORMANCE TEST -- WITHIN ± 2% OF ORIGINAL CALIBRATED MODULE VERIFIED USING HUGHES REFERENCE CELL ± 2%
- ALL THREE MODULES MUST BE ACCEPTABLE TO BUY-OFF LOT

Conclusions

STRINGENT SPECIFICATION GUARANTEES

- ENVIRONMENTAL PERFORMANCE
- STRUCTURAL/PHYSICAL INTERFACES
- ELECTRICAL PERFORMANCE
  - SOLAREX CURRENTLY DELIVERING MODULES 4% ABOVE REQUIREMENT
- COST EFFECTIVE
  - CHEAPER TO ASSURE FACTORY MODULE PERFORMANCE THAN TO ADJUST IN FIELD

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QUALIFICATION TESTING AND ELECTRICAL MEASUREMENT EXPERIENCE: A MANUFACTURER'S VIEW

J.C. Arnett, J.E. Cooley and T.L. Wingert
ARCO Solar Industries
Woodland Hills, California

The first market for photovoltaic devices was in aerospace applications, which have attendant criteria of high reliability in extreme environments and high efficiency due to spacecraft constraints. The high costs necessary to satisfy these criteria are tolerated by this market. With the emergence of the second market for PV, remote-power terrestrial applications, the need for a new set of standards was recognized. Early users of terrestrial PV did not have approved and accepted national and international standards available of the types provided by consensus organizations such as IEEE, ASTM, UL and IEC. In many cases these users were driven to adopt the only criteria available at the time, i.e., the JPL Block Specifications. Users did not fully understand that these documents, and their successively more rigorous revisions, were written more to force the advancement of module design technology and to reduce costs than they were to support specific applications, such as remote water delivery. The need for widely accepted standards appropriate to such systems is only now being addressed by consensus groups.

The third major market for PV, megawatt-scale utility-grid-connected power plants, is developing rapidly, as indicated by the recent purchase of 1.2 MW by the Sacramento Municipal Utility District. A series of photovoltaic module environmental qualification and performance characterization tests has been completed for this project, through the cooperative efforts of a combined industry-utility-government team. This paper describes ARCO Solar's experiences as a participant in this activity including an assessment of the applicability, completeness and appropriateness of the testing procedures and of the acceptance criteria for megawatt-sized procurements for utilities. Like the stand-alone users, the utility industry is interested in obtaining low costs, but additional concerns exist related to reliability and durability, safety, grounding and overall system criteria including performance prediction (related to output power acceptance testing), power quality and dispatchability. For purposes of this first major purchase of photovoltaic modules and panels by the utility industry, there was a carry-over of the JPL specifications. The need exists for further development, assessment, and selection of qualification and testing standards and evaluation criteria specifically addressing these additional concerns for utility-connected PV power-plant applications.

C-4

QUALIFICATION TESTING AND ELECTRICAL MEASUREMENT EXPERIENCE: A MANUFACTURER'S VIEW

ARCO SOLAR INDUSTRIES

J.C. Arnett
J.E. Cooley
T.L. Wingert

Markets for Photovoltaics

- **AEROSPACE**
- **REMOTE TERRESTRIAL**
- **UTILITY POWER PLANTS**

Aerospace Market

- **STANDARDS DEVELOPED BY:**
  - **-NASA AGENCIES**
  - **-AEROSPACE INDUSTRY**
- **WELL DEFINED, COMPLETE STANDARDS AND TEST ENVIRONMENTS FOR:**
  - **-SPACE ENVIRONMENT**
  - **-HIGH RELIABILITY**
  - **-HIGH PERFORMANCE**
- **HIGH COST JUSTIFIED BY APPLICATION**

Remote Terrestrial Market

- NO APPLICATION SPECIFIC STANDARDS READILY AVAILABLE
- NATIONAL PHOTOVOLTAIC ACT ENABLED JPL BLOCK PROCUREMENTS
  - ASSESS STATE OF TECHNOLOGY
  - ADVANCE DESIGN METHODOLOGY
  - REDUCE COST
- INTERNATIONAL STANDARDS NOW BEING DEVELOPED
  - PRIMARILY PERFORMANCE MEASUREMENT
  - CONSUMERS CAN'T SUPPORT EXPENSIVE TESTING AND STANDARDS

Module Specification History

• BLOCK I	5-342	1ST GENERATION	OCT 75
• BLOCK II	5-342-1B	2ND GENERATION	DEC 76
• BLOCK III	5-342-1C	2ND GENERATION UPDATE	MAY 77
• PRDA 38	5101-65	INTERMEDIATE-LOAD CENTER (ILC)	OCT 77
• BLOCK IV	5101-16A	ILC (3RD GENERATION)	NOV 78
	5101-83	RESIDENTIAL (2ND GENERATION)	NOV 78
• MTR	5101-138	1982 TECHNICAL READINESS ILC	JAN 80
• BLOCK V	5101-161	ILC (4TH GENERATION)	FEB 81
	5101-162	RESIDENTIAL (3RD GENERATION)	FEB 81

Qualification Test Evolution

TESTS	MODULES					TEST LEVELS
	BLOCK I	BLOCK II	BLOCK III	BLOCK IV* RES/ILC	BLOCK V* RES/ILC	
THERMAL CYCLE	100	50	50	50	200	-40°C TO +90°C, CYCLES AS INDICATED
HUMIDITY CYCLE	X	5	5	5	10	5 CYCLES AT 95% RH, 25°C TO 40°C OR 10 CYCLES AT 85% RH, -40°C TO +85°C (BLK I, 70°C AT 90% RH, 68 H)
MECHANICAL LOADING CYCLE		100	100	10000	10000	2400 N/m^2 (50 lb/ft^2) CYCLES AS INDICATED
WIND RESISTANCE				X	X	UNDERWRITERS LAB TEST NO. 997 (RESIDENTIAL ONLY)
TWIST		X	X	X	X	ONE CORNER LIFTED 2 cm/m OF LENGTH
HAIL IMPACT				20	25	10 HITS WITH ICE BALLS, DIA AS INDICATED (mm)
ELECTRICAL ISOLATION		1500	1500	1500/ 2000	1500/ 3000	50 μA MAX CURRENT AT VOLTAGE INDICATED
HOT-SPOT ENDURANCE					X	100 h SHORT CIRCUITED AT 100 mW/cm^2, NOCT

*RES: RESIDENTIAL, ILC: INTERMEDIATE LOAD CENTER

Utility PV Power Plant Market

SMUD PV1 FIRST MAJOR ATTEMPT TO BUY PV BY A UTILITY

-PERFORMANCE MEASUREMENT BASED ON NASA STANDARD

-RELIABILITY/DURABILITY TESTS ADOPTED FROM JPL BLOCK V SPECIFICATIONS

-QUALIFICATION ACCERTANCE CRITERIA IDENTICAL TO PRODUCTION CRITERIA

SMUD PV2: LESSONS FROM PV1 INCORPORATED

-PERFORMANCE MEASUREMENTS TIED TO CEC METHOD

-SOME TESTS ELIMINATED

-ENVIRONMENTAL TEST ACCEPT/REJECT CRITERIA

D23

N84 32706

QUALIFICATION TESTING FOR A CENTRAL STATION

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Qualification testing for a Central Station Photovoltaic (PV) Facility depends to a great extent on the system design, (fixed versus tracking), and the level of data acquisition/control which is incorporated into the system. The basic elements which require qualification tests include:

- o DC Power Production/Collection
- o Tracker Control
- o Power Conversion Systems
- o AC Utility Interface
- o System Level Control
- o Data Acquisition/Reporting

This paper principally discusses the qualification tests from the Lugo (ARCO) 1 MW Facility which were completed in January 1983. The philosophy and many of the procedures are applicable to any central station PV facility.

I. LUGO DESCRIPTION

The Lugo 1 MW PV Facility consists of 108 two-axis, flat plate trackers each of which is series/parallel connected to provide ± 260 volts at approximately 18 amperes. The facility occupies approximately 20 acres with the power being collected at a centrally located equipment/control building. Power from six trackers is collected in the field at a power collection center (PCC). Nine such PCC's exist in each of two subfields (A&B).

The main DC switchgear contains the capability of switching the DC power to either two 500 kVA inverters or one 1,000 kVA inverter. The 480 volt, 3Ø AC output is stepped up to 12 kV and interfaced to the Southern California Edison (SCE) grid at the west end of the facility. A small weather station is located next to the control building to provide data necessary to the operation and performance evaluation of the system.

Two small computer systems are incorporated into the facility. One controls the trackers and the second acquires and processes system performance data. The two systems are cross-coupled such that the data acquisition system can issue "control" commands under certain conditions.

II. QUALIFICATION TESTS

The qualification tests on the Lugo 1 MW PV Facility covered the following areas:

- o Individual Trackers
- o DC Switchgear
- o AC Components
- o Power Conversion Units
- o Tracker Control
- o Data Acquisition System
- o System Level Operations/Control

A. INDIVIDUAL TRACKER TESTS

The tracker tests included all tests which were repeated at each of the 108 trackers. Test objectives for several functional areas were consolidated to avoid multiple trips to individual trackers. Items which were tested include:

- o DC Power Components/Wiring
- o Ground Fault Detection
- o DAS/Control Wiring
- o Tracker Limit Switches

Testing of the DC wiring was started during the series interconnections of PV panels. The open circuit voltage was measured after each four series connections ($\sim$ 80 volts). A special audible alarm was used which detected ground faults as the series connections were made.

Completed trackers were tested with procedures developed from figure 4. Measurements included $\pm$ Voc, Isc (through 0.1 ohm load) and the forward voltage drop across the blocking diode. A ground fault condition was simulated and the voltage was checked for amplitude and polarity both locally and at the input to the data acquisition system (DAS) in the control building. Temporary jumpers were installed so that both the DAS and spare cables were tested. Sound powered phones were connected on the control loop cables for communications between the trackers and the control room technician. This also provided initial check-out of the control loop. The DC wiring to each PCC was verified by measuring each tracker's Voc at the PCC input terminals. Testing was performed according to detailed procedures which provided step-by-step records of each tracker's tests.

Each tracker has two limit switches for each of the four directions of movement. These limit switches were tested by a combination of local and computer controlled drive of the tracker. The computer would drive a group of eighteen trackers to near the limit and a local control box was used to check the limit switches.

B. DC SWITCHGEAR TESTS

Tests on the two subfields were accomplished in the DC switchgear inside the electrical equipment building. Voc for each group was measured at the input terminals to verify the field wiring. Voltage and current monitors were tested and calibrated. A two point calibration of current was done by measuring Isc from one and two trackers through a 0.1 ohm, 0.1% resistor.

The capability to switch the dc input between one 1000 kva inverter and two 500 kva inverters was also tested and subfield Voc was measured at the inverter inputs to verify proper wiring.

C. AC COMPONENTS

The AC system elements are shown in figure 5. All elements of the main AC switchgear were factory tested. The in-field tests included:

- o Voltage measurements at the field transformers
- o Tests on the diesel generator
- o Tests for the un-interruptible power supply (UPS)

A final AC system test verified that the utility interlock will prohibit system operation if the SCE breaker is tripped.

D. POWER CONVERSION UNITS

The power conversion units were tested at great length during factory acceptance. The in-field tests consisted of:

- o Verification of proper phasing
- o Emergency shut down/control
- o Automatic wake-up/shut down
- o Operation at high power levels
- o DAS interface

E. TRACKER CONTROL

Tracker control tests were accomplished after all limit switch operations had been demonstrated. These tests included:

- o Wake-up routines
- o Stowing routines
- o Tracker alignment calibration
- o Automatic tracking demonstration

The wake-up routine sends the trackers to the East limit switch which is the reference point for the control system. Each tracker is then individually controlled by the computer for tracking operations.

Stowing of the trackers occurs under four conditions, 1) loss of AC power, 2) high winds, 3) overtemperature in the control room and 4) loss of DAS input. These conditions were all simulated to complete stowing tests.

Tracker alignment calibration was done for both axis of alignment. The vertical axis was referenced from the lower limit switch. The horizontal axis was referenced from the East limit. Proper alignment occurs when the sunlight shaft (caused by the gap between tracker halves) is vertical on the support pedestal. Individual adjustments to trackers are stored in the computer reference files.

Automatic tracker demonstration included wake-up, tracking stow/return tests and the midnight return of all trackers to the pre-wake-up position.

F. DATA ACQUISITION SYSTEM

A function diagram of the Lugo data acquisition system is shown in figure 6. The tests on the DAS included:

- o Analog input signal calibration
- o Digital signal verification
- o Control system operation
- o Data conversion/display
- o Remote monitor/display functions
- o Hard disk storage/retrieval

G. SYSTEM LEVEL TESTS

System level tests were accomplished to complete the final Lugo qualification testing. These tests included:

- o Automated unattended operation
- o Emergency operating conditions
- o Tare loss measurements
- o Overall system efficiency measurements

System level tests were accomplished over a two-week period and were partially concurrent with DAS and Tracker Control Tests.

III. LUGO CONCLUSIONS/OBSERVATIONS

Problems that occurred during Lugo testing resulted primarily from lack of early planning. Neither the system design nor the construction schedule were impacted by the need for qualification tests. A significant oversight in the Lugo tests was testing at the panel (eight parallel module) level. These were intended to be tested at the factory but delivery schedules preempted the tests. Several panels had module polarities reversed. Panel level short circuit current tests would reveal this. Tracker level tests of Isc did not suffice because of the bypass diode at each panel.

The solution to this problem points out an interesting result of Lugo qualification testing and subsequent testing throughout this year, namely, the sensitivity of the tracker ground currents to array problems. Ground currents flow due to mismatch between the two tracker array halves. The miswired panels were discovered through analysis of the ground currents. The loss of a single cell produces a noticeable ground current and in several cases bird droppings caused ground currents exceeding 0.5 amperes.

IV. QUALIFICATION TEST PHILOSOPHY

Testing of a PV Central Station is not particularly different from any other system. There are three principal elements, 1) preparation 2) execution, and 3) documentation.

A. PREPARATION

Early test planning is important in any system. The qualification tests can and should have input both to the system design and the construction schedule. Test objectives should be consolidated where possible to streamline the test time. Test designs should be simple. In-field labor may be local union craftpersons. Straight foward tests and easy to use equipment produce the best results.

Good detailed test procedures are essential. They force well thought tests. They also provide a vehicle for review which is an essential ingredient to test preparation. The review cycle should include the construction contractor.

B. TEST EXECUTION

Qualification testing should maximize in-plant testing. It costs less and can be better supported by designers and special test equipment. Items which are good candidates for in-plant tests include:

- Assembled panels of PV modules
- AC/DC Switchgear
- Power Conversion Units
- Data Acquisition/Control Systems

In-field tests should start as soon as a sustained test effort can be maintained. Construction should be scheduled so that completed elements of the PV arrays can be made available for test. The in-field tests occupy the majority of test time.

The most important element of in-field testing is qualified, on-site support. Something will go wrong and work-arounds must be implemented. There is no substitute for someone who is thoroughly familiar with the system.

Another major consideration is safety. It is well known that a PV system can't be turned-off. Don't let anyone forget it. Emphasize safety in the procedures and during tests.

C. DOCUMENTATION

Keep good test records. Detailed procedures force this to a great extent. Be certain that system corrections and test exceptions are well documented. These have a way of getting lost in the final system documentation. This can have a serious affect during life cycle maintenance.

QUALIFICATION TESTING FOR A CENTRAL STATION

THE BDM CORP.

Donald L. Forrester

Figure 1. General Layout

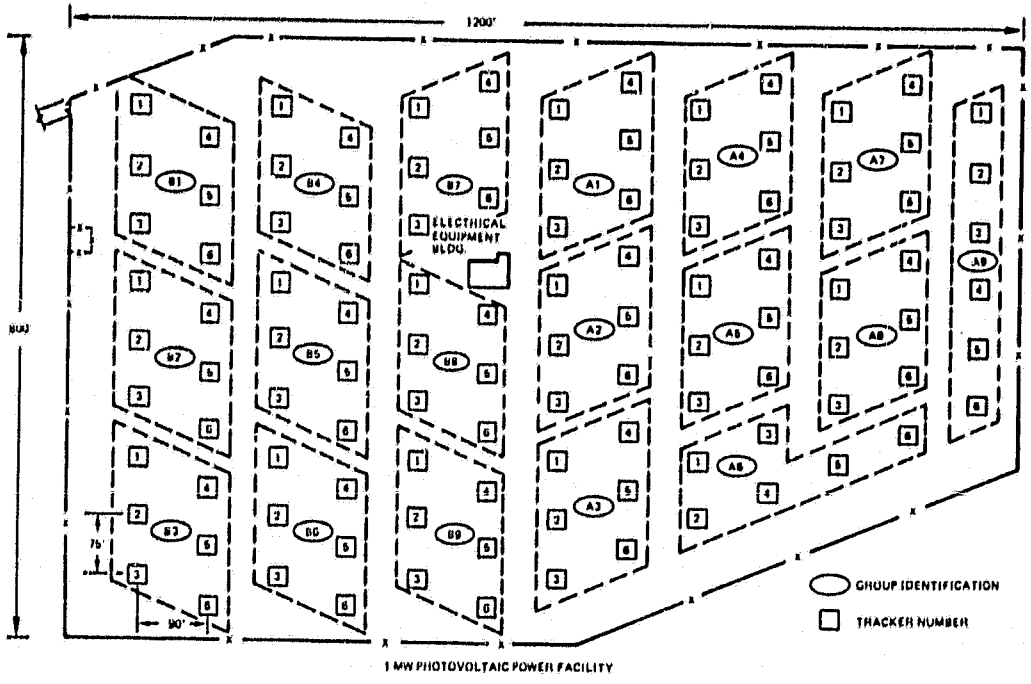
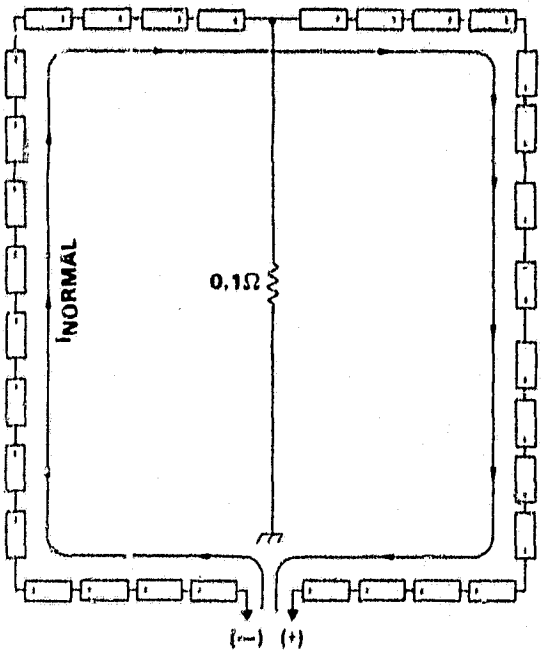
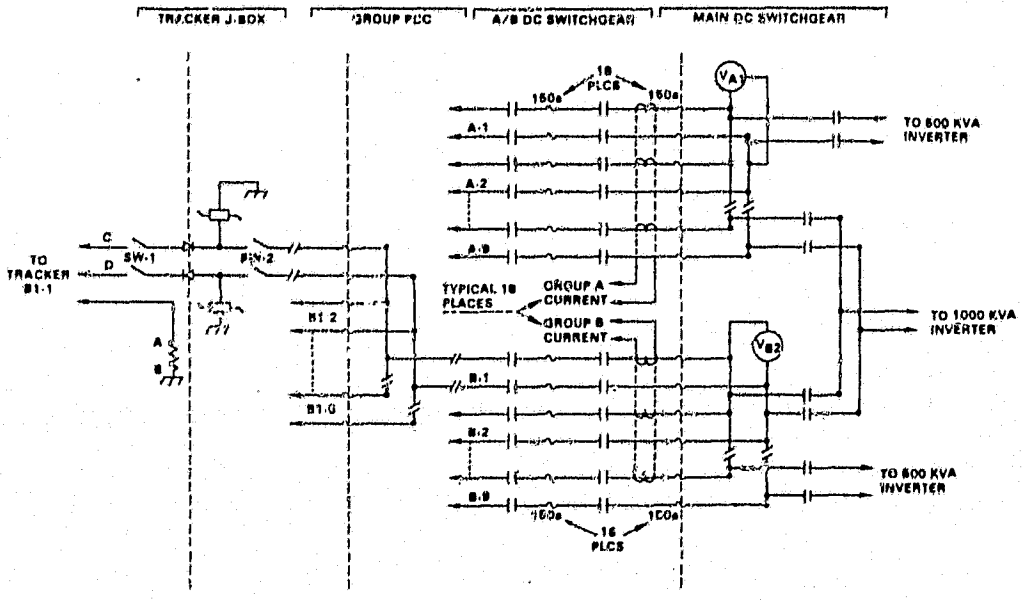


Figure 2. Typical Tracker, Lugo 1 MW PV Facility



- 8 PARALLELED MODULES PER PANEL
- 16 SERIES PANELS PER TRACKER-HALF:
  - 8 ARE M-51 MODULES
  - 8 ARE 16-2000 MODULES
- CENTER-TAP IS GROUNDED THROUGH 0.1Ω RESISTOR

Figure 3. Dc System Simplified Wiring Diagram



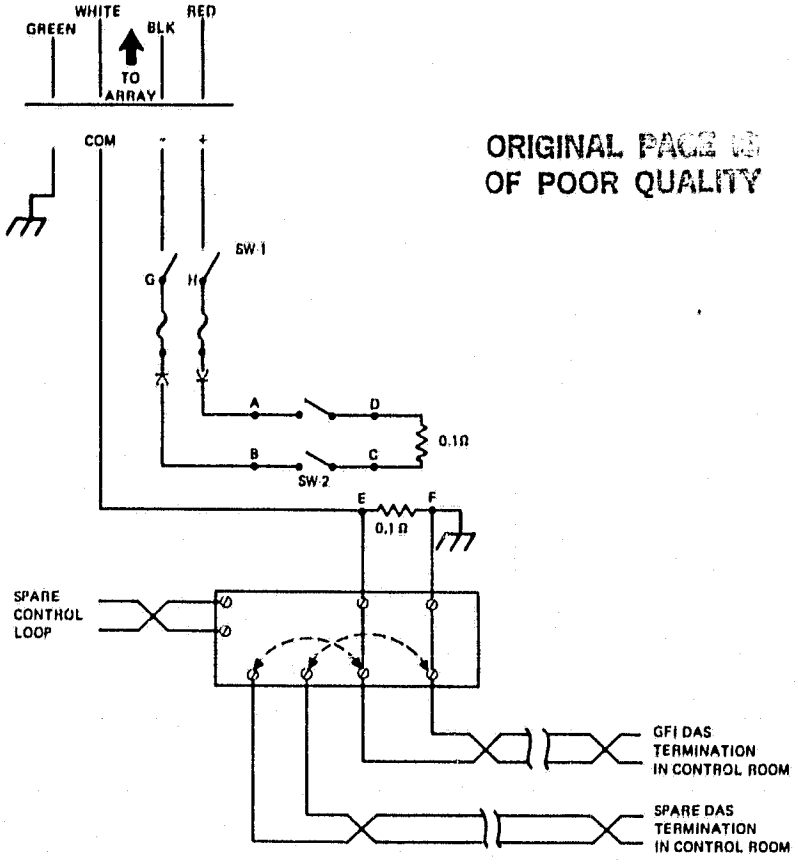
Lugo Qualification Tests

1) INDIVIDUAL TRACKER
2) DC SWITCHGEAR
3) AC COMPONENTS
4) POWER CONVERSION UNITS
5) TRACKER CONTROL
6) DATA ACQUISITION SYSEM
7) SYSTEM LEVEL OPERATIONS/CONTROL

Individual Tracker Tests

- DC POWER COMPONENTS/WIRING
- GROUND FAULT MONITOR
- DAS/CONTROL CABLING
- TRACKER LIMIT SWITCHES

Figure 4. J-Box Dc and DAS Cabling Test



Test Record Sheet: J-Box Dc and DAS Cabling Tests

TRACKER #_____

NOTE: Refer to figure I-3 for connection point and clarification.

CAUTION

Lethal voltages may exist both at the input and output connections of a tracker J-Box. Use extreme care when working inside the J-Box. These tests should not be done at insolation levels < 400 mW/cm^2.

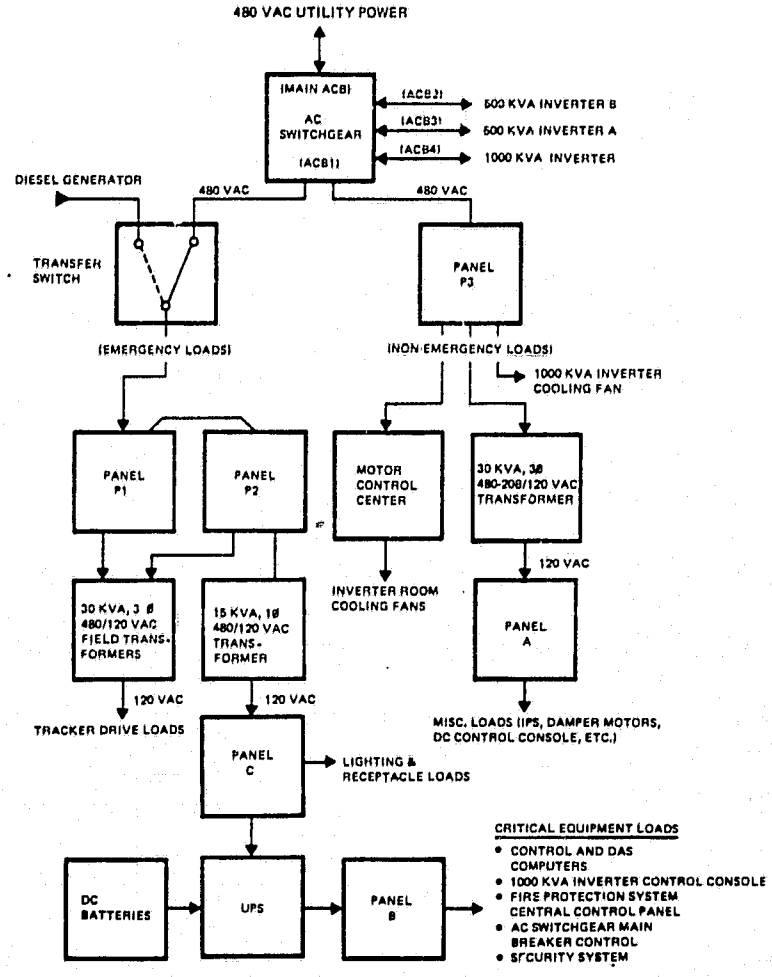
STEP	BY	TEST OPERATION	CHECKOFF
1.	TN-1	Verify SW-1 and SW-2 are open	_____
2.	TN-1	Verify zero voltage (D to C)	_____
3.	TN-1	Install 0.1 Ω, 100-watt resistor (D to C)	_____
4.	TN-1	Connect voltmeter from point A and B to Ground	_____
5.	TN-1	Close SW-1	_____
6.	QA	Record V_{OCA} = _____ V_{OCB} = _____	_____
7.	TN-1	Connect voltmeter from D to C	_____
8.	TN-1	Close SW-2	_____
9.	QA	Record V_{SC} = _____ volts	_____
10.	QA	Calculate I_{SC} = 10 V_{SC} = _____ amps	_____
11.	TN-1 QA	Measure and record diode voltage drop V_{HA} = _____ volts (< 1.0 V) V_{BG} = _____ volts (< 1.0 V)	_____
12.	TN-1 QA	Measure and record the GFI voltage V_{EF} = _____ volts (< 5.0 mV)	_____
13.	TN-1	Open SW-1 and SW-2	_____
14.	TN-1	Short negative output (C to F)	_____
15.	TN-1	Jumper GFI cable terminals to spare cable terminals with test leads	_____
16.	TN-1	Remove fuse from negative lead	_____

1) VOC AT INPUT TERMINALS
VERIFIES FIELD WIRING

2) ISC FOR TWO TRACKERS
CALIBRATE CURRENT MONITORS

3) CONTROL SWITCHING BETWEEN INVERTERS

Figure 5. Ac Electrical Block Diagram



Ac Tests

1) FACTORY SWITCHGEAR

2) FIELD TRANSFORMERS

3) DIESEL GENERATOR

4) UNINTERRUPTABLE POWER SUPPLY

5) UTILITY INTERLOCK

Power Conversion Unit Tests

- PROPER PHASE WITH UTILITY
- EMERGENCY SHUT DOWN/CONTROL
- AUTOMATIC WAKE-UP/SHUT DOWN
- HIGH POWER OPERATION
- DAS INTERFACE

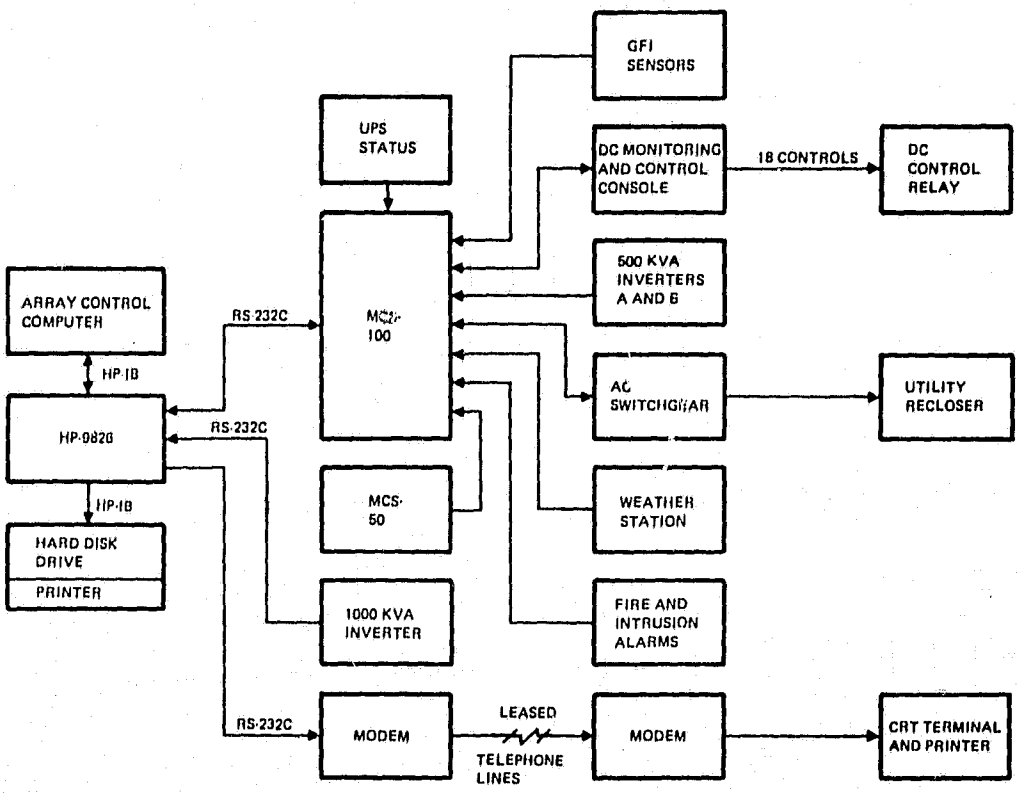
1) WAKE-UP ROUTINE

2) STOWING TESTS

3) TRACKER ALIGNMENT CALIBRATION

4) AUTOMATIC TRACKING

DAS Functional Diagram



DAS Tests

- **ANALOG INPUT CALIBRATION**
- **DIGITAL SIGNAL VERIFICATION**
- **CONTROL SYSTEM OPERATION**
- **DATA CONVERSION/DISPLAY**
- **REMOTE MONITOR/DISPLAY**
- **HARD DISC STORAGE/RETRIEVAL**

System Level Tests

1) **AUTOMATIC UNATTENDED OPERATION**

2) **EMERGENCY OPERATING CONDITIONS**

3) **TARE LOSS MEASUREMENTS**

4) **OVERALL SYSTEM EFFICIENCY**

Lugo Conclusions and Observations

1) **TEST PLANNING SHOULD HAVE STARTED SOONER AND BEEN INTEGRATED INTO DESIGN AND CONSTRUCTION SCHEDULING**

2) **PANEL LEVEL TESTS WERE PREEMPTED DUE TO TIGHT SCHEDULE**

   — **WOULD HAVE ELIMINATED MUCH TRACKER TROUBLESHOOTING**

3) **GROUND CURRENTS PROVIDE SENSITIVE PERFORMANCE INFORMATION**

Qualification Test Philosophy

1) **GOOD PREPARATION**
   - — EARLY TEST PLANNING
   - — CONSOLIDATE OBJECTIVES
   - — DESIGN SIMPLE TEST
   - — DETAILED PROCEDURES
   - — THOROUGH REVIEW

2) **EXECUTION**
   - — MAXIMIZE IN-PLANT TESTS
   - — START EARLY
   - — PROVIDE QUALIFIED IN-FIELD SUPPORT
   - — EMPHASIZE SAFETY

3) **DOCUMENTATION**
   - — COMPLETE TEST RECORDS
   - — WELL-DOCUMENTED CORRECTIONS/ EXCEPTIONS

SESSION VI

ARRAY MAINTENANCE ISSUES

Edward J. Simburger, Chairman

OMIT TV
END

SESSION VI

ARRAY MAINTENANCE ISSUES

Chairman: E.J. Simburger, Aerospace Corp.

SUMMARY

Although there were a number of speeches from diverse backgrounds, there was overall convergence on a small number of operations and maintenance issues. These are:

Allowable O&M Cost
Array O&M Strategy
Determination of Failure Modes and Rates
Determination of O&M Cost

Allowable O&M Cost

The amount of money that can be spent for operation and maintenance of a photovoltaic power plant will have to be a relatively small fraction of the revenues generated by power production. The results of a number of studies of central-station design have indicated that annual O&M costs in the range of $2.00 to $2.50 per square meter per year are consistent with a levelized bus-bar energy cost of $0.15 kWh. Paul Henry pointed out in his presentation that the sensitivity of levelized electricity cost to O&M costs is only $0.008 per kWh for each dollar per square meter of annual O&M cost. For the base case, where O&M costs were assumed to be $2.28 per square meter per year, a reduction in O&M costs to zero would result in a reduction in levelized electricity cost of only $0.018 per kWh. Thus the overall positive effect that can be obtained from further reductions in projected O&M cost is small.

It should be pointed out, however, that the cost of O&M procedures is not the only consideration. Under many circumstances, increased O&M activity will also correspond to increased outage frequency and, therefore, to lost energy production. This factor would also lead to sn increase in bus-bar energy cost.

Array O&M Strategy

The consensus regarding O&M strategy that emerged from this session is as follows:

(1) There should be no replacement of modules that degrade or fail but do not otherwise adversely affect overall array performance.

(2) Some module replacement would be required where a failure affected either safety, protection of equipment, or the overall performance of the array.

As D. Rosen pointed out in his presentation, the key to a no-module-replacement policy is to build fault tolerance into the array by appropriate design features. To minimize the O&M cost associated with locating and repairing any catastrophic failures in the array, the overall plant design should include some fault-locating equipment and should provide for easy replacement of components.

Determination of Failure Modes and Rates

The various failure mechanisms and failure rates for the photovoltaic modules and balance-of-system components that would make up a central-station photovoltaic power plant are not now well understood. A number of installations whose size approaches that of an actual utility-scale plant exist, and the data on failure rates and mechanisms in these systems will be invaluable.

However, there does not seem to be any mechanism in place for collecting, categorizing, analyzing, and disseminating this type of data. It has been suggested that the photovoltaic community take the initiative and develop an O&M reporting system. Such a system should incorporate the features that the North American Electric Reliability Council (NERC) has included in its Generating Availability Data System (GADS).

Determination of O&M Costs

Like failure modes and rates, O&M costs are not well defined. If one were to look at some of the early experiments that were funded by the DOE-PRDA program, one could become quite discouraged. However, when one considers the experimental nature of these projects, the initial startup problems for first-of-a-kind systems, the infant mortality of the equipment and the small size of these systems, then the numbers presented by T.D. Harrison are not surprising or necessarily worrisome. And, in fact, as R.E.L. Tolbert indicated in his discussion of the Lugo 1-MW plant, O&M costs for that installation are expected to come close to the $2.50 per square meter per year figure after about one more year of operation.

As with the failure modes and rates, we need to develop a mechanism to gather information about O&M costs in these early systems and to differentiate the steady-state costs from costs associated with the initial startup, experimental nature, and small size of these systems. Again, this data-gathering system could be modeled after the NERC-GADS reporting system.

Conclusion

In conclusion, it seems that the PV industry has, to quote P.K. Henry, developed a "perception that PV will be a highly reliable, low-O&M power source." Thus, to reinforce this perception, it seems that accurate and meaningful data on the failure modes and rates of PV systems and on actual O&M costs are of paramount importance.

Dean Cohen of Hughes Aircraft Co. provided the view of the system contractor for the Georgetown PHENEF Project in dealing with a module manufacturer to obtain qualified modules. He presented the requirements of the module procurement specification, which defined the electrical and mechanical characteristics of the module and the quality-assurance provisions. The electrical performance characteristics and performance measurements procedures were carefully defined. Hughes solved the procedure problem by using as their own a draft ASTM standard to obtain globally calibrated reference cells and then established their own procedure for performance measurement. For qualification testing, Hughes chose to adopt the JPL Block V requirements and added other requirements as well, including an Underwriters Laboratories, Inc., fire-resistance test. Hughes also expanded acceptance testing to include a diode verification test as well as visual inspection, hi-pot, and electrical performance. The Hughes procedures involved reference-cell calibration, use of calibrated modules, simulator verification, performance measurement and source inspection. This attention to detail represents the approach of one sophisticated customer in purchasing photovoltaic modules. As in the previous presentations, the discussion focused upon the problems of performance measurement, once again highlighting the absence of acceptable standards that could facilitate commerce.

In the talk by James Arnett of ARCO Solar, Inc. the meeting finally addressed the environmental requirements of the qualification tests. It became clear that the manufacturers are very wary of the effect on commerce of the qualification requirements imposed by JPL on its contractors in the course of the module development program. Although the specifications written by JPL were for the purpose of increasing the reliability of modules, which they were effective in doing, they are also perceived as qualification standards, which they are not. The tendency is for a customer (if he is aware of the DOE program) blindly to demand compliance with the latest JPL specification regardless of the application. This is, of course, because there is no other U.S. specification or standard available to use. The forum was also told that manufacturers do perform environmental stress tests on their own modules, but not necessarily or even usually the same tests as those used by JPL. The sense that environmental tests are useful in some as-yet-unknown way to determine lifetime, but should not be imposed by an agency external to the manufacturer, emerged during this presentation.

Tim Lambarski of BDM Corp. presented a paper on "Qualification Testing for a Central Station" prepared by Don Forrester. The hierarchy of management of the Lugo 1-MW facility, an ARCO project, clearly shifted the emphasis of this discussion from module and array qualification testing to central-station qualification. Lambarski described the Lugo facility and the tests that generally confirmed the operation and safety of individual trackers, dc switchgear, ac components, tracker control, the data acquisition system and system-level operation and control. Although there was considerable discussion of various system test problems, there was no discussion of the overall system efficiency measurements or the basis for determining the electrical performance.

Standing back and considering the papers and discussion in this session devoted to qualification and electrical performance measurements for photovoltaic solar arrays in central stations, a number of observations and conclusions can be drawn. In no particular order, they are:

1. There is a dichotomy of perception of the need for formal qualification testing of photovoltaic modules or arrays. The manufacturers believe that they are now part of a mature industry that knows what it should give the customer. The customers, whether system contractor or utility, do not see the solar industry as fully matured and still want independently imposed qualification criteria.

2 The status of performance measurements standards creates difficulty for customers and manufacturers alike. With no consensus performance measurement standard, there is no common base for comparing the performance of competing modules.

3. Manufacturers, national laboratories and the user community give inadequate support to the development of voluntary consensus standards for electrical performance, but until these come into being and are consistently applied, the photovoltaic industry will <u>not</u> be perceived as mature.

OPERATION AND MAINTENANCE EXPERIENCE IN PHOTOVOLTAIC ARRAYS

SANDIA NATIONAL LABORATORIES

T.D. Harrison

NEW MEXICO ENGINEERING INSTITUTE

J.P. Fernandez

Introduction

This paper presents strategies and costs for operation and miantenance (O&M) for two fixed, flat-plate PV arrays. A survey of all PRDA 38 fixed, flat-plate PV arrays shows that the strategies for conducting O&M are generally similar but costs vary somewhat. A PV array is that part of a PV system that comprises the modules, the support structure, and the wiring necessary for transmission of electrical power to the load and for grounding.

The two arrays selected are Beverly High School (Massachusetts) and Lovington Square Shopping Center (New Mexico). They were selected because they are operating in a steady-state condition and are very similar. Both arrays use the same modules (Solar Power Model G12-361-CT). They are both part of a 100-kW system, both systems were designed by the same architectural and engineering (A&E) firm (Stone and Webster), both comprise two subsystems, both use 75-kW Helionetics Power Conditioning Subsystems (PCSs) to convert dc power to ac power, and both feed power to the grid through isolation transformers.

The differences in the arrays are that the one at Beverly High School has 3,200 modules in 40 subarrays, compared with 3,360 modules in 42 subarrays at Lovington, Beverly is in a more northerly latitude (42.67°) than Lovington (32.56°), and there is more precipitation at Beverly than at Lovington.

Strategy

The elements of the strategy for O&M follow:

1. Periodic walkthrough inspections
2. Periodic inspection of modules
3. Maintenance of grounds

The goal of this program is to reduce of human intervention to a minimum.

Approach to Determining O&M Costs

There are three categories that make up the cost of O&M:

1. The value of energy lost to downtime
2. The cost of labor and materials for scheduled operations
3. The cost of labor and materials for unscheduled operations

To determine the value of energy lost to downtime for the array, the number of daylight hours (calculated sunrise to calculated sunset) in each month was deter-

mined. Using data from onsite data acquisition equipment and also from energy meters, the number of hours of operating time was determined. The difference between daylight hours and operating hours is downtime.

Figures 1 and 2 display the results of calculating downtime for a selected 12-mo period. The shape of the curve for daylight hours is not smooth because the number of days in a month varies. January, for example, shows more daylight hours than February even though the days in February are longer. The reason is that there are 3 more days in January than in February. The curve for Beverly is further complicated by the fact that it is based on the days on which the meters were read. The interval between meter readings at Beverly did not always correspond to the number of days in the month.

The white area in the bars represents total system downtime during daylight hours. The causes for this downtime were categorized and quantified into such elements as insufficient insolation, module replacement, etc., using logbooks, site event reports, visits to the arrays, and interviews with operators. This paper considers only those categories of downtime that concern the array.

Operations that comprise scheduled operations are defined in O&M manuals. The primary sources of information for cost are the same as those mentioned above. Unscheduled operations are defined in logbooks, site event reports, interviews with operators, formal reports prepared by operators, and records at Sandia.

Beverly High School Array

Downtime -- Available records do not show any time when the complete array was down for reasons attributable to the array. There were periods when a small part of the array was down. These occurred during module rework, module replacement, and performance of diagnostics on modules. It is estimated that 20 kW were lost for 30 h. The cost of electricity during the period of downtime was $0.07/kWh. The value of electrical energy lost was then $42.00.

Scheduled O&M -- From Figure 3, the following constitute scheduled O&M.

1.	Weekly sensor cleaning	175 h
3.	Monthly field inspection	90 h
5.	Weed control	45 h
6.	Module diagnostics	30 h
		340 h

The 340 h over a 2.5-yr period represent an average of 136 h/yr of scheduled maintenance on the array.

Unscheduled maintenance -- From Figure 3, the following items constitute unscheduled maintenance.

2.	Module rework	170 h
4.	Road repair	70 h
7.	Module replacement	22 h
		262 h

Of the above, module rework was made necessary by poor process control by the manufacturer. It is unlikely that any further rework will be needed.

Road repair was made necessary by erosion of a dirt road. Grading plus the addition of approximately $1000 worth of gravel should substantially reduce the need for future road repair.

Module replacement was made necessary because the manufacturer failed to rework all modules successfully. The need for some module replacement is foreseen, but at a reduced rate. Vandalism could be a cause for module replacement.

Discussion of O&M Costs -- O&M costs on the array for a 30-mo period sum as follows:

Value of energy lost to downtime	$ 42
Scheduled maintenance @ $25/h	8,500
Unscheduled maintenance @ $35/h	9,170
Materials	1,000
	$18,712

The value of the 283,931 kWh produced during the same period (costed at $0.07/kWh) is $19,875.

Lovington Square Shopping Center Array

Downtime -- As at Beverly, there is no record of the total array being down because of a fault in the array. The quantity of energy lost is estimated to be the same as at Beverly, i.e., 600 kWh, but at a value of $0.05/kWh, which equals $30.00.

Scheduled O&M -- From Figure 4, the following constitute scheduled O&M.

1.	Periodic walkthrough inspections	225 h
3.	Weed control	60 h
4.	Module diagnostics	50 h
6.	Semiannual inspection	10 h
		345 h

The 225 h of walkthrough inspection accomplished the same tasks as did the 175 h of weekly sensor cleaning and 90 h of monthly field inspection at Beverly. Scheduled O&M required an average of 138 h/yr, compared with 136 h/yr at Beverly.

Unscheduled O&M -- From Figure 4, the following constitute unscheduled maintenance.

2.	Module rework	175 h
5.	Module replacement	36 h
		211 h

The reasons for module rework and module replacement were the same for Lovington as for Beverly.

Discussion of O&M costs -- O&M costs on the array for the 30-mo period sum as follows:

Value of energy lost to downtime	$ 30
Scheduled maintenance @ $25/h	8,625
Unscheduled maintenance @ $35/h	7,385
Materials	0
	$16,040

The value of the 493,523 kWh produced during the same period (costed at $0.05/kWh) is $24,676.

Discussion of O&M Costs at Beverly and Lovington and Future Plans

The O&M costs for the arrays at the two projects are compared in Table 1.

Table 1. Comparison of O&M Costs ($)

	Energy Lost	Scheduled O&M	Unscheduled O&M	Materials	Total	Value of Energy
Beverly	42.00	8,500	9,170	1,000	18,712	19,875
Lovington	30.00	8,625	7,385	0	16,040	24,676

Road repair was a significant expense at Beverly while it was no expense at Lovington. It amounted to $3,450. In the beginning, the roads at Lovington were better prepared at greater expense than at Beverly. This appears to be a situation where a trade-off between higher initial cost or higher maintenance costs is necessary.

The value of electricity produced at Beverly was $19,875 compared with $24,676 at Lovington. Three elements account for the difference:

1. There were some system problems at Beverly not associated with the array, which increased system downtime.

2. Considerably more solar energy fell on the array at Lovington than on the array at Beverly.

3. The quantity of energy produced at Lovington was much higher than at Beverly.

Plans are being carried out to extend the operation of both PV systems through December 1984. In both cases the system owners, Beverly Public Schools and Lea County Electric, have agreed to bear a major share of the cost. During this extra year of operation, studies will be made to determine methods for reducing human intervention and thus the cost of operation and maintenance.

Conclusion

Both systems are operating in good health. Both systems have the potential for operating at a profit. Two factors can contribute to profitable operations: (1) reduce the cost of scheduled maintenance and (2) consider the rising cost of electricity.

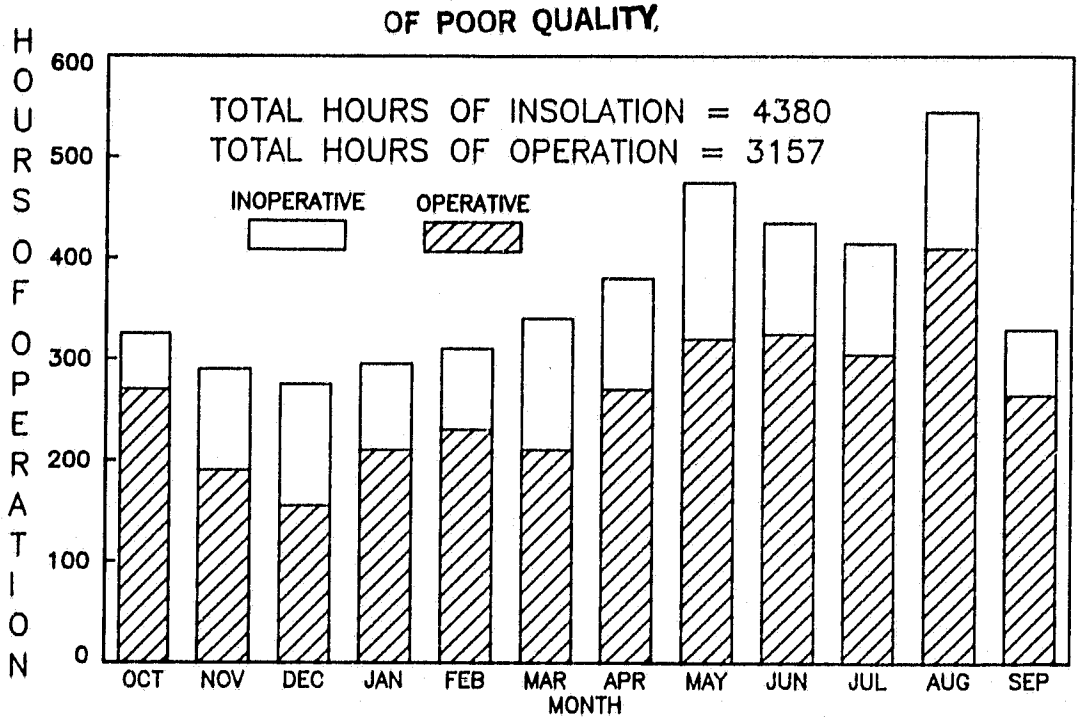


Figure 1. Beverly High School, Hours of Operation, October 1982 to September 1983

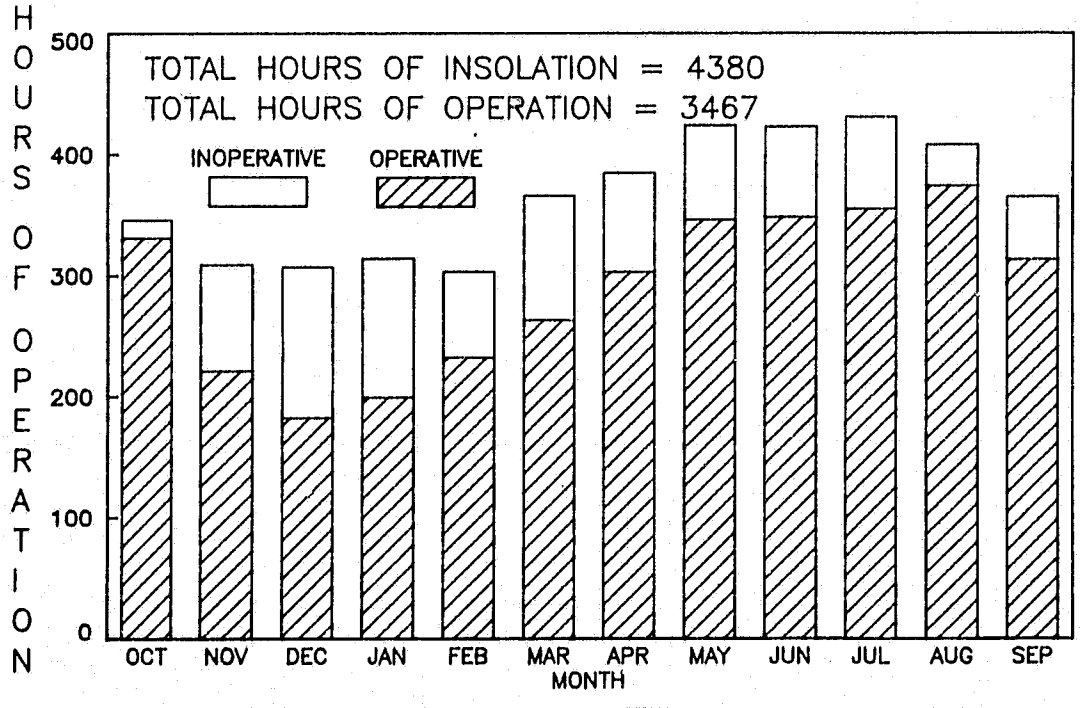


Figure 2. Lovington Shopping Center, Hours of Operation, October 1982 to September 1983

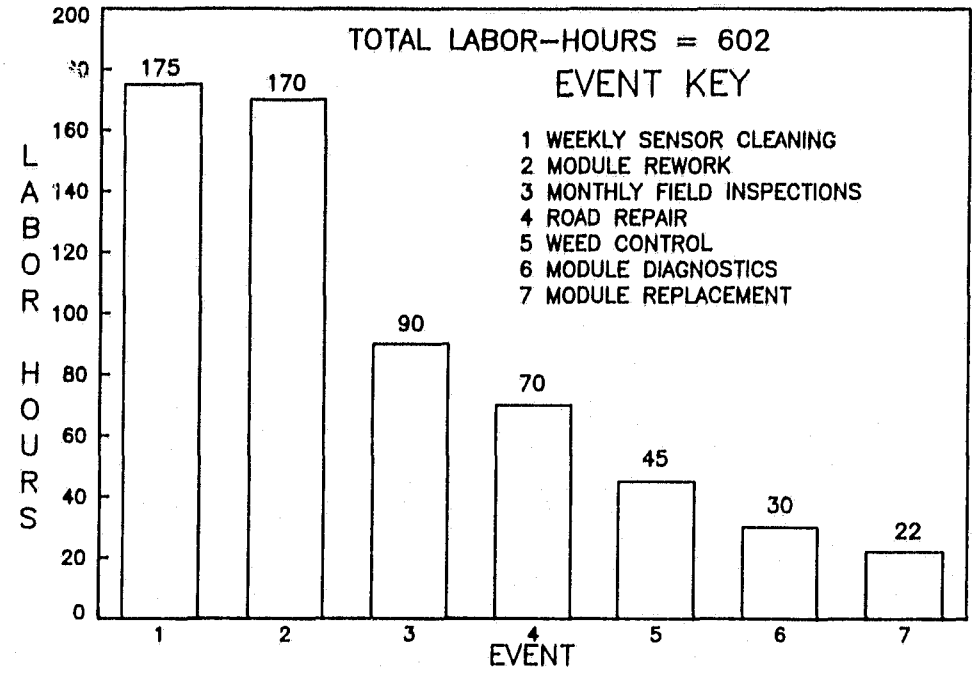


Figure 3. Beverly High School, Labor Summary, April 1981 to September 1983

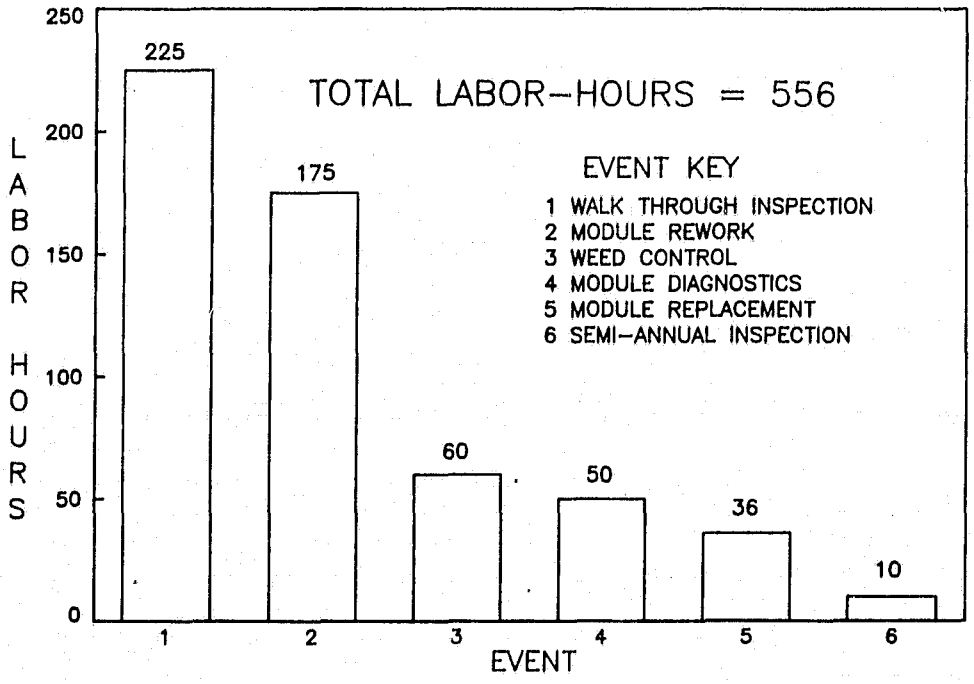


Figure 4. Lovington, Shopping Center, Labor Summary, April 1981 to September 1983

PLANNING FOR FIELD MAINTENANCE

Dan Rosen
Acurex Corporation
Mountain View, California

The cost effectiveness of large central station photovoltaic powerplants will depend both on the industry's ability to reduce construction costs and the ability of the plants to operate with minimal maintenance. This is important because maintenance adds to the plant's operating costs while often reducing its energy output. Plants should therefore be designed to facilitate maintenance and minimize downtime. Plant designs must also maintain equipment and personnel safety during maintenance activities.

It is important to remember, however, that what is of most interest to the utility, or other owner, is the total cost of energy generation. This cost is determined by both the plant first costs and the costs of operating and maintenance (O&M). If the total cost is not competitive with other sources of generation, potential owners will quickly lose interest. Designs must result in plants that do not require excessive maintenance.

Unfortunately, we do not have an adequate data base to permit full understanding of maintenance requirements. Maintenance requirements can generally be divided into two categories. Some activities, such as array washing, may only be necessary if they provide adequate payback. Other activities, such as repair of ground faults, will be mandated by personnel and equipment safety concerns. The first generation of large PV powerplants, now coming online, will provide much useful data in these areas. Until sufficient data is available, the following general design guidelines should be considered.

Plants should be designed to minimize the occurence of fault conditions that could result in plant damage and/or maintenance requirements. For example, optimizations that result in relatively high DC system voltages to save only a few cents per watt in plant costs should be carefully weighed against the increased probability of module ground faults. Such "fine tuning" of plant first costs might best be saved for future generation plants, when the long-term risks of ground faults may be better understood.

Plan designs should provide adequate access for personnel and maintenance equipment. Grouping of blocking diodes, fuses, and other such equipment in easily accessible locations will facilitate routine inspection, and perhaps prevent some failures.

Means should be included in the design to isolate failed portions of the plant, both to minimize their affect on plant operation and to allow replacement. Isolating devices may be automatically operated with load break capability, such as DC contactors or circuit breakers, or they may be manual nonload break, such as quick-disconnect-type cable connectors. The added

expense of contactors or circuit breakers provided to isolate relatively small portions of the array field may not be justifiable. This is particularly true if faults are infrequent, as they likely must be to result in acceptable O&M costs.

Finally, the designs should provide features which minimize repair times, such as including fault-locating equipment and easily replaceable components.

In addition to waiting for plant operating data to become available, the industry should continue to investigate areas which may result in lower maintenance costs. These include innovative design configurations as well as identification of equipment failure mechanisms, such as the dielectric breakdown of module encapsulants.

Photovoltaic powerplant maintenance requirements, and plant designs optimized to accommodate these requirements, will result from an iterative process involving engineering analysis, plant design, and evaluation of operating data. There is much to learn, but we are on the road to finding out.

PLANNING FOR FIELD MAINTENANCE

ACUREX CORP.

Dan Rosen

Design Requirements

- PLANT DESIGNS MUST FACILITATE SCHEDULED AND UNSCHEDULED MAINTENANCE WITH MINIMUM INTERRUPTION TO OPERATION
- EQUIPMENT AND PERSONNEL PROTECTION MUST BE MAINTAINED DURING MAINTENANCE ACTIVITIES
- PLANT DESIGNS SHOULD BE COMPATIBLE WITH ALLOWABLE MAINTENANCE COSTS
  - -- UTILITIES WILL NOT WANT TO OWN AND OPERATE POWERPLANTS THAT COST MORE TO MAINTAIN THAN THEY ARE WORTH, NO MATER HOW EASY IT IS TO DO SO
- THE BOTTOM LINE IS THE TOTAL COST OF GENERATION

Array Field Maintenance

- SOME MAINTENANCE ACTIVITIES WILL BE BASED STRICTLY ON ECONOMIC TRADEOFFS:
  - -- ARRAY WASHING
  - -- REPLACEMENT OF DEGRADED MODULES
- SOME MAINTENANCE ACTIVITIES WILL BE DICTATED BY EQUIPMENT AND PERSONNEL SAFETY REQUIREMENTS:
  - -- MODULE GROUND FAULTS
  - -- DIODE FAILURES

First Costs vs Operating Costs

- TRADEOFFS EXIST BETWEEN THE COSTS OF DESIGN FEATURES AND RESULTING REDUCTIONS IN O&M COSTS
- DESIGN FEATURES SHOULD FACILITATE MAINTENANCE ACTIVITIES WITHOUT ADDING UNACCEPTABLE FIRST COSTS
- IN MANY CASES SUFFICIENT OPERATING EXPERIENCE IS NOT YET AVAILABLE TO PERMIT OPTIMIZATION

Design Guidelines

- MINIMIZE OCCURENCE OF FAULT CONDITIONS/DAMAGE
  - -- APPROPRIATE DC VOLTAGE LEVELS
  - -- BLOCKING DIODES
  - -- BYPASS DIODES (IF REQUIRED)
  - -- FUSES
  - -- LIMIT FAULT CURRENTS (E.G., RESISTIVE GROUNDING)
  - -- SERIES/PARALLEL CONNECTION OF CELLS, MODULES, ETC.
- PROVIDE ADEQUATE ACCESS TO ALL EQUIPMENT
  - -- ARRAYS
  - -- DIODES
  - -- FUSES
- PROVIDE MEANS TO ISOLATE ARRAY ELEMENTS
  - -- DC CONTACTORS OR CIRCUIT BREAKERS
  - -- QUICK DISCONNECT CONNECTORS
- MINIMIZE REPAIR TIMES
  - -- FAULT LOCATION
  - -- MODULE REPLACEMENT

What Can We Do for the Future?

- DEVELOP AND REFINE MAINTENANCE REQUIREMENTS AND STRATEGIES BASED ON INITIAL EXPERIENCES WITH OPERATION OF LARGE POWERPLANTS
- WORK WITH THE UTILITIES AND OTHER POTENTIAL PLANT OWNERS AND OPERATORS TO UNDERSTAND HOW THEY APPROACH PLANT MAINTENANCE
- CONTINUE TO INVESTIGATE INNOVATIVE DESIGNS WHICH MINIMIZE MAINTENANCE REQUIREMENTS OR FACILITATE IN-FIELD MAINTENANCE ACTIVITIES
- CONTINUE TO INVESTIGATE EQUIPMENT FAILURE MECHANISMS SUCH AS DIELECTRIC BREAKDOWN OF ENCAPSULANTS IN ORDER TO IMPROVE THE RELIABILITY OF FUTURE PLANTS

ECONOMIC IMPLICATIONS OF OPERATION AND MAINTENANCE

P. K. Henry
Jet Propulsion Laboratory
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In projecting ahead to the day when large-scale central station PV generating facilities are commonplace, one of the large uncertainties is the cost of operations and maintenance and the attendant implications for system economic viability. Field experience with large arrays is very limited as it is only now that anything resembling "large-scale" is being fielded. The operations and maintenance (O&M) experience in the next few years will, without doubt, profoundly affect the user perception of PV as to whether or not it is a reliable technology. This presentation examines the various components of O&M, reviews some published estimates of O&M costs and places O&M in the perspective of the National Photovoltaic Program goals.

The various components of O&M are shown in Figure 1. Collector cleaning requirements vary widely from site to site; from very minimal or no cleaning required in desert or rural areas to frequent cleaning in industrial and urban areas. The nature of the front surface affects the light transmission losses due to dirt accumulation with glass and some polymer films showing the least loss and silicones showing significant dirt accumulation problems. Cleaning may also vary with season since fewer cleanings would be required during rainy seasons.

Structures, wiring and ground maintenance would be associated mostly with any recurring site specific problems of drainage, erosion, weed control, etc. Structures and wiring would require only periodic inspections barring catastrophic damage to the array by nature. Tracking arrays with bearings and drive units, may require somewhat more maintenance. Historically, power conditioning systems have been one of the more troublesome components of PV arrays. However, further experience with PCUs in large arrays should lead to much more reliable power conditioning. In addition, there is the possibility that manufacturers may offer service contracts for about 2% to 3% per year of the PCU capital costs.

The operation of PV central station arrays up to several tens of megawatts will be, for the most part, automated and unattended. For very large arrays, some on-site operations personnel will probably be required.

The need and strategies for module replacement depend heavily on the ability of the module and array design to tolerate failures in cells and interconnects without economically intolerable power losses and maintenance costs. Fault tolerant designs for modules and arrays are becoming available.

The degree and placement of bypass diode protection is still an open question. Some module replacement will probably be required in a thirty year life array. Consequently, fault detection methods need to be refined to detect failed modules and attention should be given in the initial design of module mounting to permit expeditious module replacement.

A representative, but certainly not exhaustive, summary of estimates for O&M costs from various recent system studies are shown in Figure 2. The many similarities between the results of the studies reflect similar assumptions. The total O&M costs per year are calculated to be in the range of $\$2.00/m^2$-yr to about $\$2.50/m^2$-yr.

The goal of the National PV Program is to develop the technology capable of producing electricity at \$0.15/kWh (1982\$). The equation used for the levelized electricity cost in the National Photovoltaic Program Five Year Research Plan (May 1983) is shown in Figure 3. It shows how the annual O&M cost (\$MSQOM in the equation) is incorporated into the levelized electricity cost calculation. Note that the annual O&M cost assumed in the plan is $\$2.28/m^2$-yr.

Figure 4 plots the sensitivity of levelized electricity cost to O&M costs with all other factors in the equation held constant at the values shown in Figure 3. The sensitivity is 8 mils change in levelized electricity cost per $\$/m^2$-yr change in O&M costs. This would indicate that O&M is probably not one of the more sensitive parameters in the calculation of levelized electricity costs. Indeed, even if O&M costs were reduced to zero, Figure 4 shows the levelized electricity cost to be reduced by only 1.8¢/kWh.

The principal observations of this presentation are summarized in Figure 5. Of particular note is the last bullet. This author has communicated with a wide spectrum of people over the past several years, both in and outside of the photovoltaic community. An equally wide spectrum of views are held on every aspect of photovoltaics but one, and that is reliability. There is a widespread perception that PV will be a highly reliable, low O&M power source. The systems being fielded now and in the next few years will either reinforce or tarnish this perception, a very valuable asset for the future that should be jealously preserved.

ECONOMIC IMPLICATIONS OF OPERATION AND MAINTENANCE

JET PROPULSION LABORATORY

P.K. Henry

Components of O&M

- Collector cleaning
  - Site-specific
  - Collector front-surface-specific
  - Season-specific
- Structures, wiring and grounds maintenance
  - Drainage, erosion and weed control site-specific
  - Structures, wiring periodic inspections only
- PCU maintenance
  - Historically troublesome
  - Possible service contracts at 2% to 3% of PCU capital costs
- Operations
  - Plant performance monitoring and reporting automated
- Module replacement
  - Fault-tolerant designs becoming available
  - Probably some replacement required

O&M Estimates From Various System Studies

		BECHTEL(1)	RCA(2)	BATTELLE(3)	BLACK & VEATCH(4)
MODULE CLEANING	($/m²·yr)	0.20	0.12	0.20	0.24
STRUCTURES GROUNDS WIRING	($/m²·yr)	1.00	0.26	0.86	
PCU	($/m²·yr)	0.22-0.33*	0.05		1.00 **
	($/kWp·yr)	(1.66-2.79)*	(0.42)		
OPERATIONS	($/m²·yr)	0.50			0.28
MODULE REPLACEMENT	($/m²·yr)	0.30		0.00	0.37

(1) EPRI AP-2475, Photovoltaic Balance-of-System Assessment, June, 1982.
(2) Stronix, A. J., and A. H. Firester, "Conceptual Design of 50MW Central Station PV Power Plant," IEEE PES 1983 Winter Meeting
(3) Carmichael, D. C., et. al., Development of a Standard Modular Design for Low-Cost Flat-Panel Photovoltaic Array Fields, SAND81-7183, Sandia National Laboratories, 1983.
(4)

*Estimated from Bechtel report by taking 2% to 3% of PCU capital cost of $83/kWp
**Add $0.30 if array is tracking.

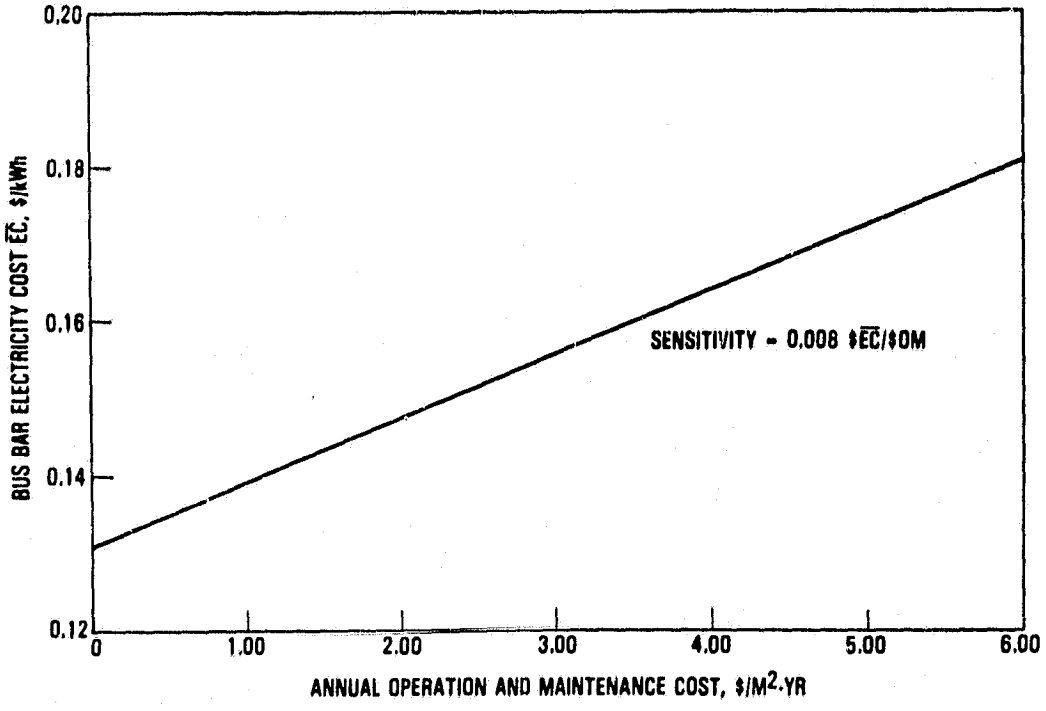
Program Goals and Economic Assumptions

Levelized Electricity Cost Equation From Program Plan:

$$\overline{EC} = \left[\frac{FCR}{8760 \cdot CF}\right] (INDC)\,[A(\$MSQMD + \$MSQBS) + \$KWBS] + A \cdot G \cdot CRF \left[\frac{\$MSQOM}{8760 \cdot CF}\right]$$

$\overline{EC}$	levelized electricity cost in current dollars	$0.15/kWh	CRF	capital recovery factor for a 12.5% discount rate and 30-year lifetime	0.129
FCR	fixed charge rate	0.18		average peak isolation	1.0kW/m²
	general inflation rate	0.085		balance-of-system efficiency	0.81
	discount rate	0.125		module efficiency	10% to 25%
CF	annual system capacity factor	0.27	$MSQBS	BOS area-related cost	50-75 $/m²
INDC	indirect cost multiplier	1.50	$KWBS	BOS power-related costs	$150/kW
G	present worth factor based on a 12.5% discount rate and 30-year lifetime	18	$MSQOM	annual O&M costs	$2.28/m²·year

Sensitivity of EC to O&M Costs



Summary

- Projected O&M costs are a rather small contributor to bus-bar electricity costs
- Therefore, deviations from projected costs can't help much in reducing electricity cost but can hurt
- Need for unattended operation apparent
- Appropriate module replacement strategies still a question mark; failed module detection still a problem
- Maintenance requirements of high-power PCUs unknown
- Image of PV as a highly reliable, low O&M power source is a very valuable asset and should be jealously preserved

THIRD-PARTY OPERATOR VIEW OF OPERATIONS AND MAINTENANCE

ARCO SOLAR INDUSTRIES

R.E.L. Tolbert

ARCO Solar 1 MW PV Plant O&M Experience

- START-UP ACTIVITIES
- REMOTE MONITORING
- UTILITY COORDINATION
- SECURITY
- SAFETY
- STAFFING
- TRAINING
- EQUIPMENT AND SUPPLIES
- PUBLIC RELATIONS
- SYSTEM RELIABILITY
- PERFORMANCE ANALYSIS

Startup Activities

- **RESPONSIBILITIES**
  - -CONTRACTOR
  - -PROJECT TEAM
  - -OPERATIONS GROUP
- **CHECK-OUT PLAN**
  - -FACTORY ACCEPTANCE TESTING
  - -FIELD INSPECTION
  - -UNIT TESTING
  - -SYSTEM TESTING
- **ACCEPTANCE TESTING**
  - -WRITTEN CHECK-LIST
  - -TRIAL PERIOD
  - -MANUAL OPERATION
  - -AUTOMATIC OPERATION
- **MAJOR ELEMENTS**
  - -PHOTOVOLTAIC PANELS
  - -TRACKERS
  - -SWITCHGEAR
  - -INVERTERS
  - -COMPUTERS
  - -FIRE CONTROL

Remote Monitoring

- **DATA ACQUISITION SYSTEM**
  - -OPERATION
  - -PERFORMANCE
  - -WEATHER
  - -EVENTS
- **CRT TERMINAL MONITORING**
  - -ALARMS
  - -24 HOUR COVERAGE
  - -NOTIFICATION LIST
- **SIGNIFICANT EVENTS**
  - -STOW-CONTROL ROOM TEMPERATURE
  - -STOW-EMERGENCY/FIRE
  - -HALON PRE-DISCHARGE
  - -HALON DISCHARGE
  - -INTRUSION ALARM TRIPPED
  - -AC OFF-IPS NOT ON
  - -ERROR SHUTDOWN-INVERTER
  - -GROUND FAULT-MAIN BUSS
  - -UPS BATTERY FAILURE
  - -UPS BY-PASS

Utility Coordination

- INTERCONNECTION DESIGN
- PROTECTION EQUIPMENT
  - -VOLTAGE
  - -FREQUENCY
  - -CURRENT
  - -PHASE SEQUENCE
- POWER QUALITY MEASUREMENTS
- MAIN DISCONNECT
  - -AUTOMATIC RECLOSURE
  - -MANUAL RECLOSURE
- PUBLIC RELATIONS
  - -TOURS
  - -PUBLICATIONS
  - -VIP VISITS

Security

- FENCING
- CONTROL BUILDING
  - -DOOR/WINDOW CONTACTORS
  - -VIBRATION SENSORS
  - -MOTION DETECTION
  - -ALARMS
- REMOTE MONITORING
- LOCAL SURVEILLANCE
- VANDALISM

Safety

- GROUNDING
- FAULT DETECTION
- INTERLOCKS
- LOCK-OUTS
- TRAINING
- EQUIPMENT
  - -GLOVES
  - -HARD HATS
  - -METERS
  - -TWO-MAN RULE
- SIGNS

Staffing

- IN-HOUSE OPERATION AND MAINTENANCE GROUP
  - - MANAGER
  - - FIELD ENGINEERS
  - - ELECTRONIC TECHNICIAN
- STAFF SUPPORT
  - - INSTRUMENTATION
  - - COMPUTER HARDWARE/SOFTWARE
  - - TESTING
  - - SAFETY
  - - SECURITY
- CONTRACT SUPPORT
  - - ROUTINE
  - - ON-CALL
- SUPPLIERS
  - - INVERTERS
  - - DAS
  - - TRACKER ELECTRONICS

Training

- SAFETY
- SYSTEM START-UP/SHUTDOWN
- COMPUTER OPERATION
- PHOTOVOLTAIC TECHNOLOGY
- ELECTRICAL TROUBLESHOOTING
- TRACKER ADJUSTMENT
- OPERATION AND MAINTENANCE MANUAL
- VENDOR LITERATURE
- DRAWINGS (RED-LINED)

Equipment and Supplies

- PLANT EQUIPMENT
  - -SCISSORS LIFT
  - -MULTIMETERS
  - -HAND TOOLS
  - -VEHICLES
- SPARE PARTS
  - -MODULES
  - -DIODE BOXES
  - -TRACKER CONTROLLERS
  - -TRACKER MOTORS
  - -FUSES
  - -INVERTER LOGIC CARDS
  - -INVERTER LEGS
  - -COMPUTER CARDS
  - -DC CONTACTORS
- EXPENDABLE SUPPLIES
  - -FUEL
  - -LUBRICANTS
  - -COMPUTER PAPER

System Reliability

- **PREVENTATIVE MAINTENANCE (SCHEDULED)**
  - -VISUAL INSPECTION
  - -AIR FILTERS
  - -GEAR DRIVE LUBRICATION
  - -BATTERIES
  - -DIESEL FUEL
  - -HVAC EQUIPMENT
  - -BOLT TORQUE
- **CORRECTIVE MAINTENANCE (UNSCHEDULED)**
  - -PV MODULES
  - -BYPASS DIODES
  - -TRACKER ELECTRONICS
  - -LIMIT SWITCHES
  - -SWITCHGEAR FUSES/CONTACTORS
  - -INVERTERS
  - -COMPUTERS
  - -MONITORING SYSTEM

Performance Analysis

- PEAK POWER
- DC/AC LOSSES
- AC ENERGY
- WEATHER
- ACTUAL vs. PREDICTED
- TREND ANALYSIS