NASA-TM-86307 19840025643

NASA Technical Memorandum 86307

THEORETICAL AND EXPERIMENTAL STUDIES OF ERROR IN SQUARE-LAW DETECTOR CIRCUITS

William D. Stanley, Chase P. Hearn, and
James B. Williams

SEPTEMBER 1984

National Aeronautics and
Space Administration

Langley Research Center
Hampton, Virginia 23665

SUMMARY

This paper assesses the deviation of semiconductor diode square-law detectors from the "ideal" input-output response. The nonlinear circuit response is analyzed by means of a power series expansion containing terms through the fourth degree, from which the significant deviation from square-law can be predicted. It will be assumed that the detectors under study are operated at input signal levels for which a power series truncated after the fourth term produces a reasonably accurate representation.

Two basic circuit configurations are considered: one, in which the bias current is fixed, and the other in which the mean current can change with the application of a signal.

Experimental investigations of the circuit arrangements are described, which showed substantial agreement with the results predicted by the analytical models. Factors contributing to differences under certain conditions are explained.

Although most practical circuits employ the fixed bias configuration, results obtained from this study suggest that the flexible bias circuit may have some advantages in many cases.

LIST OF SYMBOLS

A_0, A_1, A_2, A_3, A_4	power series coefficients of diode current
B_0, B_1, B_2, B_3, B_4	power series coefficients of diode voltage
C_2, C_4	coefficients of mean shift in voltage for fixed bias circuit with sinusoidal input
D_2, D_4	coefficients of mean shift in voltage for flexible bias circuit with sinusoidal input
i_D	diode current
i'_D	initial form of diode current before adjustments for dc shift
I_n	ratio of nth and (n-1)th input power levels
I_{DO}	modified diode current after shift
I_{DQ}	quiescent diode bias current
ΔI_{DQ}	second-order shift term in dc shift test
I_o	reverse diode saturation current
I_s	dc shift in diode current
I_{1p}	peak value of first-order diode current term

k_1, k_2 coefficients in output voltage versus input power function

k Boltzmann's constant = 1.38×10^{-23} J/K

M_n ratio of successive measured output voltage values divided by ratio of successive measured input power values

P power

P_{in} input power to test circuit

P_n nth measurement of detector input power

$P_{out}^{(1)}, P_{out}^{(2)}, P_{out}^{(3)}, P_{out}^{(4)}$ measured output power level at fundamental and first three harmonics

q electronic charge = 1.6×10^{-19} C

R equivalent resistance in diode circuit

T absolute temperature in Kelvin

V_B dc voltage of bias supply

V_{co} capacitor dc voltage in series diode circuit

V_D diode voltage

V_D' low-pass zonal diode output voltage with modulated input waveform

V_d = $V_D - V_{DQ}$

V_d' time-varying portion of diode voltage in test circuit

V_{DQ} quiescent diode bias voltage

V_i rms value of input voltage

V_n nth measurement of detector output voltage

V_p peak value of input voltage

V_s dc shift in bias current

v_i instantaneous input voltage

v_m measured voltage at output of test circuit

v_o output voltage of series diode circuit

v_s instantaneous signal voltage (also Thevenin equivalent voltage in test circuit)

x = $\alpha R I_{DQ}$ = normalized independent variable

α	$= q/\eta kT$
Δ	deviation from linearity in output detected voltage
Δ_n	value of Δ resulting from nth measurement
ϵ	base of natural logarithms
η	diode non-ideality factor

MOTIVATION FOR RESEARCH

The radiometric measurement of geophysical surface parameters is a problem of significant interest in remote sensing studies currently being conducted by the National Aeronautics and Space Administration at Langley Research Center. While radiometer systems have been in existence for several decades, the prediction to which absolute accuracy can be performed has always remained somewhat elusive. Recent efforts to establish absolute accuracies well under 1 K have been made, and significant efforts are currently underway to reduce the overall errors to absolute minimum levels.

As a detailed investigation of all the contributing error factors has been made, components and subsystems that have been traditionally assumed ideal are being carefully scrutinized. Deviations from the ideal that might be insignificant for overall error levels exceeding 1 K could be quite important at the current accuracy levels of interest.

A major component in a radiometer is the square-law detector, which is typically a Schottky barrier diode operated in a region in which the significant output voltage is proportional to the square of the input voltage. Since the square of the input voltage is proportional to power, the detected output voltage is proportional to the input power. A recent study by Hearn (ref. 1) has determined that a fractional deviation in the square-law characteristic of 1 percent can result in an uncertainty of the order of 0.5 K in the measurement. Therefore, the accuracy of the square-law detector is considered to be a major factor in establishing the overall accuracy to the level desired.

Although diodes operating as square-law detectors have been used for several decades, a search of the literature revealed very little detailed analysis or data concerning the deviation from the ideal square-law form. The analysis papers either simplified the mathematical model to the point where it could not be applied to realistic circuits (ref. 2), or a totally different objective than error analysis was present. Experimental data from specific diode manufacturers were studied, but such results were primarily empirical in nature (refs. 3 and 4).

The lack of definitive information of the type desired can probably be explained by the nonlinear nature of the diode's characteristics and the difficulty in applying a simplified mathematical treatment. Apparently many of the existing square-law detector circuits have evolved through empirical methods, and such circuits have been quite appropriate when error bounds have not been stringent.

GENERAL APPROACH

The general approach used in this study has centered on various forms of power series expansions of the nonlinear circuit equations when a diode is present. Simplified circuit forms were employed, although care was taken to ensure that realistic circuits could be represented as extensions of these simplified forms. Two particular circuit forms, hereafter referred to as the shunt diode form and the series diode form, were initially investigated. However, as will be demonstrated later, the underlying mathematical forms are quite similar in structure, and virtually all results of interest can be inferred from either circuit. Due to implementation considerations, the remainder of the study was performed with the shunt diode form. It is felt that most realistic square-law detectors can be reduced to forms to which the analysis of this paper can be adapted.

From the standpoint of bias operating point, two types of shunt diode circuits were considered. The first type will be referred to as the fixed bias circuit. In this circuit, a fixed dc bias current is established by either a current source or a voltage source in series with a very large resistance. An obvious constraint in such a circuit is the requirement that the time average of the current through the diode must remain constant. This circuit form appears to be the most widely employed type and is given as the suggested square-law detector circuit in most manufacturers' application notes.

A second type of biasing arrangement will be referred to hereafter as a flexible bias circuit for reasons that will be clear later. With this form, the average bias current shifts with the application of a signal.

Certain properties of the flexible bias circuit are different than those of the fixed bias circuit and could present advantages in certain circuits. This paper will be concerned with analyzing and comparing the results of the two bias forms. Separate studies are currently being continued to determine possible advantages and disadvantages of each form.

Consider the standard description of the voltage-current characteristic of a diode, given by the Shockley equation, or

$$i_D = I_o\left(\varepsilon^{qV_D/\eta kT} - 1\right) \tag{1}$$

where

i_D diode current

v_D diode voltage

I_o reverse saturation current (typically 1 nA to 1 μA)

q electronic charge = 1.6×10^{-19} C

k Boltzmann's constant = 1.38×10^{-23} J/K

T absolute temperature in kelvin

η "non-ideality" factor (typically from 1 to 2)

The inverse relationship of equation (1) is

$$v_D = \frac{\eta kT}{q} \ln\left(\frac{i_D + I_o}{I_o}\right) \tag{2}$$

For convenience in many expressions that follow, the definition $\alpha = q/\eta kT$ will be made. The parameter α has the dimensions of V^{-1}. In the range of normal operation, $\varepsilon^{\alpha v_D} \gg 1$ and $i_D \gg I_o$. With these inequalities and the preceding definition, the diode relationships become

$$i_D \simeq I_o \varepsilon^{\alpha v_D} \tag{3}$$

$$v_D \simeq \frac{1}{\alpha} \ln \frac{i_D}{I_o} \tag{4}$$

Henceforth, these results will be assumed as equalities. It should be noted that the results that follow were first developed with the more exact forms of equations (1) and (2), and the approximations were made at the end. However, the results are the same with the approximations made at the beginning, and this approach will be used here.

DYNAMIC ANALYSIS OF FIXED BIAS CIRCUIT

The first diode circuit to be used as a model for analysis is shown in figure 1(a). The diode is assumed to be biased by a constant current source of value I_{DQ}. (In practice, a voltage source in series with a large resistance is often used.) The signal input source is v_s, and R represents all net series resistance, including the source internal resistance, diode ohmic resistance, and any added resistance. Although the instantaneous voltage v_D across the diode will vary with time, the presence of the capacitor forces the mean value of the diode current to be $\overline{i_D} = I_{DQ}$. This constraint is the major characterizing feature of the fixed bias circuit and distinguishes it from the flexible bias circuit to be considered later. This particular circuit form is also a shunt diode circuit, based on the fact that the output voltage is taken across the diode.

The simple circuit of figure 1(b) represents the steady-state dc circuit without a signal. The bias source establishes a dc voltage V_{DQ} across the diode and a dc current I_{DQ} through it. Refer also to figure 2 for a graphical representation using the classical load line approach. The quiescent Q-point is established by the intersection of the voltage-current characteristic curve and the horizontal line $i_D = I_{DQ}$. Note that the capacitor is also charged to a voltage V_{DQ}.

Assume now that a signal v_s is applied, and assume that the capacitive reactance is negligible in the frequency range of interest. The dynamic circuit is shown in figure 1(c), and the corresponding load line analysis is shown in figure 2 with the aid of the dynamic load lines. As the signal varies, a family of load lines could be constructed as illustrated in figure 2 by two bounded cases. (The relative shifts are exaggerated here for illustration.) For the positive input peak, a load line of the form of L1 can be constructed, and for a negative peak, L2 is applicable. The slope of these lines is $-1/R$. Due to the nonlinear character of the diode characteristic, the positive change in current is greater than the magnitude of the negative current change. This would initially appear to change the mean value of the current. However, the mean value constraint forces an effective shift in operating point downward in the diode curve so as to maintain a constant mean current. The mean diode voltage, however, will decrease in the process, and this difference represents the desired output voltage change. The shift phenomenon will be analyzed in detail in the next section.

Next, an analytical formulation for the signal diode current will be made. Even though the effective operating point of the diode will shift with the application of a signal, its effect will be neglected for small signal analysis, and the circuit model of figure 1(c) will be used. Application of Kirchhoff's current law at the right-hand upper junction yields

$$\frac{v_s + V_{DQ} - v_D}{R} + I_{DQ} - i_D = 0 \tag{5}$$

Solution for i_D and substitution of v_D in terms of i_D from (4) yield

$$i_D + \frac{v_s}{R} - \frac{1}{\alpha R} \ln \frac{i_D}{I_D} + \frac{V_{DQ}}{R} + I_{DQ} \tag{6}$$

A power series expansion of i_D as a function of v_s will now be performed. Terms up through the fourth degree will be retained since the latter term is the most significant in predicting the deviation from the square-law model. Thus, assume that

$$i_D = A_0 + A_1 v_s + A_2 v_s^2 + A_3 v_s^3 + A_4 v_s^4 \tag{7}$$

To evaluate the coefficients, the first four derivatives of i_D with respect to v_s must be determined. This requires implicit differentiation in each case since i_D appears both as a linear term and the argument of a logarithmic function in (6). The derivatives are evaluated at $i_D = I_{DQ}$, and the results are summarized as follows:

$$A_0 = I_{DQ} \tag{8}$$

$$A_1 = \frac{\alpha I_{DQ}}{1 + \alpha R I_{DQ}} \tag{9}$$

$$A_2 = \frac{\alpha^2 I_{DQ}}{2(1 + \alpha R I_{DQ})^3} \tag{10}$$

$$A_3 = \frac{\alpha^3 I_{DQ}(1 - 2\alpha R I_{DQ})}{6(1 + \alpha R I_{DQ})^5} \tag{11}$$

$$A_4 = \frac{\alpha^4 I_{DQ}\left[1 - 8\alpha R I_{DQ} + 6(\alpha R I_{DQ})^2\right]}{24(1 + \alpha R I_{DQ})^7} \tag{12}$$

The diode voltage v_D can be expressed as

$$v_D = v_s + V_{DQ} - R(i_D - I_{DQ}) \tag{13a}$$

$$v_D \approx B_0 + B_1 v_s + B_2 v_s^2 + B_3 v_s^3 + B_4 v_s^4 \tag{13b}$$

The B_k coefficients can be derived by the same approach followed in the derivation of the A_k coefficients. These coefficients and their relationships to the A_k coefficients are

$$B_0 = V_{DQ} \tag{14}$$

$$B_1 = \frac{1}{1 + \alpha R I_{DQ}} = \frac{A_1}{\alpha I_{DQ}} \tag{15}$$

$$B_2 = \frac{-\alpha^2 R I_{DQ}}{2(1 + \alpha R I_{DQ})^3} = -RA_2 \tag{16}$$

$$B_3 = \frac{-\alpha^3 R I_{DQ}(1 - 2\alpha R I_{DQ})}{6(1 + \alpha R I_{DQ})^5} = -RA_3 \tag{17}$$

$$B_4 = \frac{-\alpha^4 RI_{DQ}\left[1 - 8\alpha RI_{DQ} + 6(\alpha RI_{DQ})^2\right]}{24(1 + \alpha RI_{DQ})^7} = -RA_4 \tag{18}$$

In the preceding coefficients, as well as others that will arise later, the product αRI_{DQ} appears as a key parameter in determining the behavior of the term. Observe that the forms of B_2, B_3, and B_4 are the same as A_2, A_3, and A_4 except for the sign and the multiplier R in the B_k coefficients. However, there is a difference between the form of A_1 and B_1.

Normalized coefficients of the preceding power series expansions are shown in figure 3, and the corresponding tabulated data are provided in table 1. It can be observed from the preceding definitions that the constants A_2, A_3, and A_4 are proportional, respectively, to the constants B_2, B_3, and B_4. The functions Y_2, Y_3, and Y_4 on figure 8 may be used to determine the appropriate A or B coefficients as indicated. Since A_1 and B_1 are different, they require separate functions. The independent variable in all cases is the normalized variable $x = \alpha RI_{DQ}$.

The first-order constants A_1 and B_1 are monotonic functions of x, with A_1 increasing and B_1 decreasing. The second-order constants A_2 and $|B_2|$ have maxima at $x = 0.5$. (The constant B_2 is minimum at this point in a negative sense, but the magnitude is the significant effect.) The third-order constants A_3 and $|B_3|$ have a maximum at $x = 0.132962$, a minimum at $x = 1.9371$, and a zero at $x = 0.5$. The fourth-order coefficients A_4 and $|B_4|$ have several maxima and minima, and there are zeros at $x = 0.13962$ and $x = 1.19371$. A point of significance that will be used in later discussions is that the sign of A_4 (or B_4) in the range $0.13962 < x < 1.19371$ is opposite to the sign of A_2 (or B_2) in the same range. However, for $x < 0.13962$ or $x > 1.19371$, the sign of A_4 (or B_4) is the same as that of A_2 (or B_2).

It will now be shown that the properties of the series diode circuit are functionally equivalent to those of the shunt diode circuit. Consider the simplified series diode circuit is shown in figure 4(a), the dc circuit shown in figure 4(b), and the correspondiong dynamic circuit shown in figure 4(c). The quiescent dc voltage across the capacitor in this case is $V_{co} = V_{DQ} + I_{DQ}R$.

A dynamic analysis for the series form may be performed by first writing a loop equation for the circuit of figure 4(c) along the outer loop. The equation reads:

$$-v_s - V_{DQ} - RI_{DQ} + v_D + Ri_d = 0 \tag{19}$$

Solution for i_D and substitution of equation (4) for v_D yields

$$i_D = \frac{v_s}{R} - \frac{1}{\alpha R} \ln \frac{i_D}{I_o} + \frac{V_{DQ}}{R} + I_{DQ} \tag{20}$$

Comparison of equations (20) and (6) for the shunt diode case reveals that the equations for i_D in the two cases are identical. A series expansion for i_D in this case will thus have the same coefficients as in equation (7).

The output voltage in this case is the voltage across the resistor R, given by

$$v_o = Ri_D \tag{21}$$

A series expansion for v_o would thus have coefficients of the exact same form (including sign) as for i_D except for the multiplier R. Thus, the properties of the series diode circuit are functionally equivalent to those of the shunt diode circuit, differing only with respect to a possible sign and a multiplicative constant. Henceforth, only the shunt diode circuit will be considered in the analysis.

DC ANALYSIS OF FIXED BIAS CIRCUIT

An expanded and somewhat exaggerated illustration of the dc behavior of the quiescent point of the shunt diode circuit with application of signal is shown in figure 5. Operation of the diode must be maintained along the characteristic curve shown. Due to the curvature, the change in current for the positive half of a symmetrical input cycle will be greater in magnitude than the corresponding change for the negative half-cycle. This might lead to the erroneous conclusion that the mean value of the current would increase, an impossibility in the constant bias circuit. In fact, however, the Q-point shifts downward to a new point Q' such that the mean current is maintained at the value I_{DQ}. In a sense, the concept of Q-point is somewhat ambiguous in this case since the average value remains at I_{DQ}, but the concept of the shift is meaningful in explaining the circuit operation.

An analysis of the shift will now be performed based on the assumption of a specific input signal. Assume that the input v_s is given by

$$v_s = V_p \cos \omega t \tag{22}$$

This signal can be inserted in the power series expansion of equation (7) in order to determine the form of the instantaneous diode current. Although the effective shift in operating point might suggest that the coefficients in equation (7) be evaluated at the new point, but for the small signal case, the coefficients are evaluated at the quiescent point Q.

After substitution of equation (22) in equation (7) and subsequent expansion, the initial form of the current obtained (denoted by i_D') is

$$i_D' = A_0 + \frac{A_2 V_p^2}{2} + \frac{3}{8} A_4 V_p^4 + \left(A_1 V_p + \frac{3}{4} A_3 V_p^3\right) \cos \omega t$$

$$+ \left(\frac{A_2 V_p^2}{2} + \frac{A_4 V_p^4}{2}\right) \cos 2\omega t + \frac{A_3 V_p^3}{4} \cos 3\omega t + \frac{A_4 V_p^4}{8} \cos 4\omega t \qquad (23)$$

The mean value of i_D' is given by the first three terms of equation (23). Since $A_0 = I_{DQ}$, this situation is obviously impossible if the mean value is to remain fixed at I_{DQ}. What happens is that the constant term in the series shifts downward to maintain I_{DQ} constant.

Let

$$i_D = i_D' + I_s \qquad (24)$$

where i_D is the actual current and I_s is the shift. It is assumed that all components other than the dc component are not significantly affected by the shift. Denoting mean values by $(\bar{\ })$, the constraint $\overline{i_D} = I_{DQ}$ yields

$$\overline{i_D} = \overline{i_D'} + I_s = A_0 + \frac{A_2 V_p^2}{2} + \frac{3}{8} A_4 V_p^4 + I_s$$

$$= I_{DQ} \qquad (25)$$

Substitution of $A_0 = I_{DQ}$ results in

$$I_s = -\frac{A_2 V_p^2}{2} - \frac{3}{8} A_4 V_p^4 \qquad (26)$$

The current i_D is then

$$i_D = A_0 + \left(A_1 V_p + \frac{3}{4} A_3 V_p^3\right) \cos \omega t + \left(\frac{A_2 V_p^2}{2} + \frac{A_4 V_p^4}{2}\right) \cos 2\omega t$$

$$+ \frac{A_3 V_p^3}{4} \cos 3\omega t + \frac{A_4 V_p^4}{8} \cos 4\omega t \qquad (27)$$

In the neighborhood of I_{DQ}, the voltage v_D can be expanded in a power series expansion in terms of the current i_D starting with the form of equation (4). The result is

$$v_D = V_{DQ} + \frac{1}{\alpha I_{DQ}}(i_D - I_{DQ}) - \frac{1}{2\alpha I_{DQ}^2}(i_D - I_{DQ})^2$$

$$+ \frac{1}{3\alpha I_{DQ}^3}(i_D - I_{DQ})^3 - \frac{1}{4\alpha I_{DQ}^4}(i_D - I_{DQ})^4 \qquad (28)$$

The series of equation (27) can then be substituted in the series of equation (28). Only dc terms through the fourth degree will be retained. By careful inspection, those terms can be sorted out of the rather unwieldy expression obtained. After appropriate expansion and simplification, the mean voltage $\bar{v}_D$ can be expressed as

$$\bar{v}_D = C_0 + C_2 V_p^2 + C_4 V_p^4 \qquad (29)$$

where $C_0 = V_{DQ}$. The voltage shift V_s, which represents the desired dc output, is given by

$$V_s = C_2 V_p^2 + C_4 V_p^4 \qquad (30)$$

where

$$C_2 = -\frac{\alpha}{4(1 + \alpha R I_{DQ})^2} \qquad (31)$$

and

$$C_4 = -\frac{\alpha^3}{64}\frac{\left[7 + 6(\alpha R I_{DQ})^2\right]}{(1 + \alpha R I_{DQ})^6} \qquad (32)$$

Curves depicting the nature of C_2 and C_4 on a normalized basis are shown in figure 6, and some representative values are listed in table 2.

ANALYSIS OF FLEXIBLE BIAS CIRCUIT

Consider the shunt diode circuit model shown in figure 7. This circuit represents a simplified form in which the dc circuit and the dynamic circuit have the same basic structure, and for reasons that will be clear shortly, it will be denoted as a

flexible bias current. The quiescent operating point is established by the dc bias source and the resistance R. When the signal v_s is applied, operation is about the quiescent point in accordance with the load line concept shown in figure 8. In this case, however, the dc and dynamic load lines are identical. Since the mean current is not constrained as was the case for the fixed bias circuit, both the mean value and the quiescent point move up the voltage-current characteristic curve.

A loop equation for the circuit of figure 7 reads

$$-V_B - v_s + Ri_D + v_D = 0 \tag{33}$$

Solution for i_D and substitution of equation (4) for v_D yields

$$i_D = \frac{v_s}{R} - \frac{1}{\alpha R} \ln \frac{i_D}{I_o} + \frac{V_B}{R} \tag{34}$$

Comparison of equation (34) with equation (6) reveals that the form of the current is the same as that of the fixed bias circuit as given by equation (6). (The constant terms differ in form, but these values affect only the dc terms in the series expansions.)

Due to the similarity of the terms, the results of equations (5) through (18) are generally valid. There is, however, a restriction that must be imposed relative to the permissible signal level. When the signal level is sufficiently small that the bias shift is small compared to the quiescent current I_{DQ}, the various A_k and B_k coefficients evaluated at I_{DQ} may be assumed to be valid. When the bias shift is significant in comparison with I_{DQ}, however, the accuracy of the coefficients evaluated at I_{DQ} must be carefully investigated. Certain experimental data regarding this situation will be considered in a later section.

For the moment, assume signal levels sufficiently small such that the coefficients evaluated at I_{DQ} are valid. The diode voltage v_D will be of the form of equation (13b) with the B_k constants given by equations (14) through (18).

A significant fact regarding the flexible bias circuit is that the coefficients for the dc shift are of the same general form as for the dynamic signal coefficients.

Assume that the signal v_s is a sinusoid of the form of equation (22). When this function is inserted in equation (13b) and expanded, there results

$$v_D = B_0 + \frac{B_2 V_p^2}{2} + \frac{3}{8} B_4 V_p^4 + \left(B_1 V_p + \frac{3}{4} B_3 V_p^3 \right) \cos \omega t$$

$$+ \left(\frac{B_2 V_p^2}{2} + \frac{B_4 V_p^4}{2} \right) \cos 2\omega t + \frac{B_3 V_p^3}{4} \cos 3\omega t + \frac{B_4 V_p^4}{8} \cos 4\omega t \tag{35}$$

The dc voltage shift V_s in the flexible bias circuit is simply

$$V_s = \frac{B_2}{2} V_p^2 + \frac{3}{8} B_4 V_p^4 \tag{36a}$$

$$= D_2 V_p^2 + D_4 V_p^4 \tag{36b}$$

where

$$D_2 = - \frac{\alpha^2 RI_{DQ}}{4(1 + \alpha RI_{DQ})^3} \tag{37}$$

and

$$D_4 = - \frac{\alpha^4 RI_{DQ}\left[1 - 8\alpha RI_{DQ} + 6(\alpha RI_{DQ})^2\right]}{64(1 + \alpha RI_{DQ})^7} \tag{38}$$

These results can be compared with equations (31) and (32) for the fixed bias case. Curves depicting the nature of D_2 and D_4 on a normalized basis are shown in figure 9, and some representative values are listed in table 3.

SQUARE-LAW DETECTOR ERROR

A possible desired output of a square-law detector circuit is the dc shift V_s for the shunt diode circuit. The analysis thus far has been based on a pure sinusoidal input, in which the output can be directly related to the input on a deterministic basis. Strictly speaking, of course, the signal in the case of a total power radiometer is a random process in which a statistical formulation is required for analysis. However, the manner in which the error process under investigation arises with a sinusoidal input is directly correlated with that of the random process signal, and in view of experimental considerations, the sinusoidal assumption will be made here.

Reviewing previous results, the dc shift for the constant bias circuit driven by a sinusoid is of the form

$$V_s = C_2 V_p^2 + C_4 V_p^4 \tag{39}$$

where C_2 and C_4 were defined by equations (31) and (32). The dc shift for the flexible bias circuit (in the case where the shift is small) is of the form

$$V_s = D_2 V_p^2 + D_4 V_p^4 \tag{40}$$

where D_2 and D_4 were defined by equations (37) and (38). The constants C_2 and D_2 represent the sensitivities of the respective detector forms, i.e., the ratio of output to (input voltage)^2. By a simple scaling process, these constants can in turn be converted to the form of output voltage to input power ratios.

The constants C_4 and D_4 represent error terms inasmuch as they contribute to deviations from the ideal square-law form. Other even-numbered powers (e.g., sixth power) also contribute to deviations from the ideal model, but the assumption that the fourth-degree term is the most significant term is valid over a wide operating range.

Although the actual levels of C_2 and D_2 are important, a significant indication of the error is the ratio of the fourth-degree coefficient to the second-degree coefficient, i.e., either C_4/C_2 or D_4/D_2.

Curves depicting the behavior of the individual constants and their ratios are given in figures 10 and 11. These curves are based on a specific test circuit whose parameter values are reasonably close to those encountered in practical circuits. The details of the particular circuit will be discussed in a later section, but the assumption is that $\eta = 1.04$ for the particular diode and $R = 178.2\Omega$. Although the curves are based on these specific data, the results are reasonably general and vary only with respect to absolute level differences and shifts of the operating point current scale. Corresponding representative tabulated values are given in tables 4 and 5.

Comparison of C_2 of figure 10 and D_2 of figure 11 reveals that the fixed bias circuit is more sensitive and would thus provide a larger dc output voltage for a given input power. However, the C_4/C_2 ratio is considerably larger than the D_4/D_2 ratio and thus the fixed bias circuit appears to have a larger relative error. In all fairness to the fixed bias circuit, the assumption is that the constants evaluated at I_{DQ} remain fixed and this is a point of vulnerability. For small signal operation, however, these conclusions should be reasonably valid.

For the fixed bias circuit the C_4/C_2 ratio decreases monotonically but never reaches zero. In contrast, D_4/D_2 has two zeros, which are located for the particular circuit at about 20 μA and 180 μA, respectively. Operation at either of these points could theoretically eliminate all errors caused by the significant fourth-degree term. The sign of D_4 is opposite to that of D_2 in the region from 20 μA to 180 μA. The significance of the proceeding properties will be discussed in a later section.

CLIPPING PHENOMENON

In order for the power series representations of the diode voltage or current to be valid when truncated above the fourth-degree term, the circuit must be "weakly nonlinear." For certain conditions, the circuit operates under "strongly nonlinear" conditions, and some of the results may be misleading or even erroneous.

The most profound area in which the strongly nonlinear condition was encountered was in the analysis of the power detector function for the fixed bias circuit at low bias currents. An analysis of the behavior of C_2 and C_4 in figure 10 would

suggest that the power detector curve should deviate above the ideal square-law model as the input power increases, and this phenomenon was observed in the case of moderate and higher bias currents. However, at lower bias currents, the curve drops below the square-law curve, which cannot be accounted for by the series model with second- and fourth-degree terms. In fact, by a very laborious analysis, the sixth-degree coefficient was calculated and found to have the same sign as the second- and fourth-degree terms in the pertinent region, which fails to explain the phenomenon.

The apparent explanation for the negative deviation of the power transfer curve at larger input power levels is a type of clipping phenomenon. The effective Q-point moves toward the origin when a signal is applied as previously discussed. The instantaneous current moves up and down from the modified Q-point in accordance with the input signal. For sufficiently large input signal, the downward change results in the current reaching a value of zero. At that point, the Shockley equation is generally no longer valid, particularly in regard to the various derivatives. The current and voltage are thus "clipped" at this point, and a strong condition of nonlinearity exists. Whenever this condition occurs, it becomes the dominating effect, and the pattern that would be predicted from the power series is generally invalid.

It is relatively easy to predict the general conditions that lead to this phenomenon, but it is more difficult to predict the precise level of input signal at which it occurs for a given bias level. In general, when the sum of the magnitude of the dc current shift and the peak signal current measured from the modified Q-point is equal to the unmodified dc bias current, clipping will occur. When one attempts to use the various coefficients to predict this condition, however, the validity of the coefficients must be questioned since the shift is relatively large.

A suggested first-order approximation for the purpose of determining a "gross bound" of operation can be determined empirically by the following approach: Assume that the dc shift is dominated by the second-degree term and the magnitude is $A_2V_p^2/2$. Assume further that the peak instantaneous current change is dominated by the first-degree term, whose magnitude is A_1V_p. The approximate condition for clipping is that $A_2V_p^2/2 + A_1V_p = I_{DQ}$, where as a gross approximation, A_1 and A_2 are evaluated at I_{DQ}. For a given I_{DQ}, the two separate terms may be readily calculated and their sum compared with I_{DQ}. With only a few interactions, the gross level satisfying this condition may be approximated.

At very low bias currents, the peak instantaneous current (first order term) tends to be three to four times as large as the bias shift. As the bias current increases, both the bias shift and the peak signal increases, but the former increases faster than the latter. Somewhere above 100 μA, the condition for clipping results in equal dc and first-order changes.

The approximate signal level at which clipping occurs varies from about -16 dBm at $I_{DQ} = 10$ μA to about -9 dBm at $I_{DQ} = 80$ μA. At $I_{DQ} = 180$ μA, a signal level of about -2 dBm results in the clipping condition.

One question of interest concerns the input power level at which the power series solution is invalid. Assuming operation in the weakly nonlinear region, the coefficients in the series may be used with more confidence to determine these conditions. However, the conditions are somewhat subjective since any criterion is rather arbitrary.

When the dc shift in the fixed bias circuit is of primary interest, an arbitrary criterion was established to determine the power level at which the dominant term (second-degree) is equal to 10 percent of the bias current. However, to ensure that the dominant second-degree term plus the fundamental term is not excessive, the latter term and the sum were also calculated at the given power level.

The dominant portion of the dc shift is given by $A_2V_p^2/2$. Substitution of A_2 from equation (10) and equating this value to $0.1I_{DQ}$ gives

$$\frac{\alpha^2 I_{DQ} V_p^2}{4(1 + \alpha R I_{DQ})^3} = 0.1 I_{DQ} \tag{41}$$

This results in

$$V_p^2 = \frac{0.4(1 + \alpha R I_{DQ})^3}{\alpha^2} \tag{42}$$

For the experimental circuit, it will be established later that $V_p^2 = 26.96P_{in}$. When this quantity and the value of α are substituted in equation (42), there results

$$P_{in} = 10.6049 \times 10^{-6}(1 + 6665.4I_{DQ})^3 \tag{43}$$

Let I_{1p} represent the peak value of the first-order term. This quantity is

$$I_{1p} = A_1 V_p = \frac{\alpha I_{DQ} V_p}{1 + \alpha R I_{DQ}} \tag{44}$$

where A_1 from equation (9) has been employed. Substitution of appropriate values from the experimental circuit results in

$$I_{1p} = \frac{194.212 I_{DQ} \sqrt{P_{in}}}{1 + 6665.4 I_{DQ}} \tag{45}$$

Tabulated values of P_{in} (converted to dBm), I_{1p}, and the total shift as a function of bias current are given in table 6. Both I_{1p} and the shift are tabulated as positive values, but it should be understood that the shift is toward the origin from the operating point.

From the tabulated data, it is observed that the total shift is an appreciable fraction of the bias current. However, as long as clipping does not occur, this does not necessarily imply that the series representation is invalid since the level of the dc shift may be the dominant effect as a power detector. The fact that usable power detectors operate at the power levels shown is an indication of that condition.

Based on the criteria employed, clipping is observed to occur at the higher bias current levels, and this would suggest that the power level used to establish a 10 percent shift in bias current would be excessive in those cases.

From the data listed, one could infer that the approximate maximum power level for accurate power detection with the fixed bias circuit should be maintained to a level of -20 dBm to -10 dBm. The lower power level is associated with smaller bias currents. At higher bias currents, operation close to the -10 dBm level might be more reasonable, but some caution should be exercised.

EXPERIMENTAL INVESTIGATION

General

The research described so far has been supported, and occasionally guided, by a parallel program of experimental investigation and verification. Despite the simplicity of the circuits, the experimental phase required rather sophisticated instrumentation to provide the accuracy, sensitivity, and dynamic range needed to evaluate the test circuits at input signal levels producing only small deviations from true square-law, which was the regime of interest. For that reason, this section is dedicated to describing the measurement techniques and configurations, the experimental detector circuits, and finally, a discussion of the experimental results and a comparison of those results with the theory developed earlier. The experimental phase was intended to verify or corroborate the theory and consisted of measuring (a) harmonic response vs dc bias and (b) input to (low-pass zone) output "linearity."[1] The first test served to verify the correctness of and the region of validity of the power series model. The second group of tests evaluated the test circuits in a manner consistent with their application as square-law detectors or demodulators in which only the low-pass zone output is of interest. Finally, these tests were performed on practical versions of the two fundamental configurations heretofore described as "fixed-bias" and "flexible-bias" circuits.

Test Circuits

The detector test circuits were designed with the constraint that they must be reducible to the equivalent circuits of figures 1 and 7 and also be compatible with instrumentation having 50 Ω input and output impedances. These requirements were met by "imbedding" in the diode in back-to-back resistive L-pads as shown in figure 12. The target value for the series resistance R in figures 1 and 7 was 180 Ω.

The fixed-bias circuit of figure 12(a) provides dc bias current through a 330 kΩ series resistor ranging in value from 330 kΩ to 1.2 MΩ, and approximates a constant-

---

[1]Linear in the sense that the detector output voltage is directly proportional to the input power applied to the detector.

current source. The dc output voltage is monitored through an RF decoupling network which isolates the diode from capacitive loading by the dc voltmeter and reduces the level of the RF voltage applied to the dc voltmeter, thereby minimizing the possibility of meter rectification.

The flexible-bias test circuit shown in figure 12(b) provides what amounts to a constant voltage source bias having an internal resistance of about 5 Ω. The internal resistance of the microampere meter used to monitor diode current is effectively in series with R; however, its effect was reduced to negligible proportions by limiting the series resistance of the meter to 3.3 Ω and bypassing it capacitively so that it approximated a short at RF and an open for video frequencies. The same diode was transferred between the two test circuits to eliminate diode dissimilarities. The diode used was an HP 2350 Schottky Barrier type, having a nonideality factor of 1.04.

Harmonic Response Measurement

This test offered a straightforward means for verifying the power-series description of the diode relationships between the magnitudes and signs of the power series coefficients and the dc bias current. The detector under test (D.U.T.) was driven by a 2 MHz cw signal, and the amplitude of the fundamental and harmonics through the fourth were measured as functions of bias current. By making the input power level a parameter, it was also possible to determine the drive levels at which the small-signal model became invalid. The levels were measured on a spectrum analyzer having a 70 dB on-scale dynamic range. This was inadequate for the lower drive levels, for which the higher harmonic levels were as far as 130 dB below the fundamental term. This problem was alleviated by placing a 35 dB rejection filter at the carrier frequency in the signal-conditioning path between the D.U.T. and the spectrum analyzer. The sensitivity of the measurement system was then set by the internal noise of the low-noise preamplifier. The overall configuration for this test is shown in figure 13. Absolute levels were determined by correcting the levels indicated on the spectrum analyzer by the gain correcting factors of the signal conditioning subsystem: 9.1 dB at 2 MHz, and 44.4 dB at 4, 6, and 8 MHz.

Linearity Tests

In this series of tests, the input power-output voltage linearity of the square-law detectors was evaluated, using both cw and modulated excitations. Only the low-pass zone output was measured, with all carrier and higher frequency components being filtered-out. The modulation rate was made high enough so that the blocking capacitor in the fixed-bias circuit was essentially a short circuit. The linearity test configurations are shown in figure 14. A low-pass bandwidth of 10 kHz was selected to pass both the fundamental and the second harmonic of the 3 kHz modulating signal.

In making these linearity tests, it became obvious that the most logical approach had shortcomings, which can be appreciated by a review of what is involved in the standard approach to characterizing transmission nonlinearity. If V is the output of the D.U.T. to input power P, the "standard" measurement proceeds as follows:

(1) Measure $V(P)$ over the full range of P

(2) Plot $V(P)$ vs P

(3) Establish the "best straight-line," by curve-fitting or interpolation

(4) Measure or compute Δ_n, the deviation of $V(P_n)$ from "best straight-line"

(5) Compute $\Delta_n \Big/ \left[V(P_n) + \Delta_n\right]$

The procedure is tedious, involves much data processing, and is probably inaccurate if accomplished by "eye-ball" interpolation. An alternative procedure was developed which is applicable to the assessment of small nonlinearities that is much simpler than the "standard procedure." This method is based on the assumption that the deviation from transmission linearity in the D.U.T. can be represented by a single nonlinear term of the input variable, and on the measurement of the output voltage ratio V_n/V_{n-1} corresponding to a precisely known input power ratio P_n/P_{n-1} which can be determined to a high degree of accuracy.

In the case of the detectors under study here, they are ideally linear in the sense that V is proportional to P_{in}, in which case the quantity

$$M_n \equiv \frac{V_n/V_{n-1}}{P_n/P_{n-1}} \tag{46}$$

will equal unity. Conversely, the D.U.T. is not linear if M_n does not equal unity. It can be either larger or smaller than unity. The quantity M_n can be directly related to the fractional deviation of the function $V(P)$ from straight-line, subject to the assumption followed throughout this paper that the input-output relationship of the device used as a detector is representable as a power series in the input voltage, containing terms through the fourth. That is

$$v_D = B_0 + B_1 v_s + B_2 v_s^2 + B_3 v_s^3 + B_4 v_s^4 \tag{47}$$

which means that for zero-mean inputs, the low-pass output of the detector is

$$V = \overline{v_D} = B_2 \overline{v_s^2} + B_4 \overline{v_s^2} \tag{48}$$

Since v_s^2 is proportional to P, and v_s^4 is proportional to P^2, it is possible to express equation (48) as

$$V = k_1 P + k_2 P^2 \tag{49}$$

The utility of M_n, given by equation (46), for evaluating the effect of nonzero k_2 in equation (49) can be appreciated by substituting equation (49) into equation (46) and defining $I_n \equiv P_n/P_{n-1}$ and $\Delta_n \equiv k_2 P_n^2$. Thus,

$$M_n = \frac{k_1 P_n + k_2 P_n^2}{k_1 P_{n-1} + k_2 P_{n-1}^2} = \frac{1 + \frac{k_2 P_n^2}{k_1 P_n}}{1 + \left(\frac{1}{I_n}\right)\frac{k_2 P_n^2}{k_1 P_n}} = \frac{1 + \frac{\Delta_n}{k_1 P_n}}{1 + \left(\frac{1}{I_n}\right)\frac{\Delta_n}{k_1 P_n}} \qquad (50)$$

From this, the fractional deviation from straight-line at input level P_n can be found as

$$\frac{\Delta_n}{k_1 P_n} = \frac{I_n(M_{n-1})}{I_n - M_n} \qquad (51)$$

Thus, the procedure for determining $\Delta_n/k_1 P_n$ in terms of ratios consists of the following steps:

(1) Measure and ratio V_n and V_{n-1}

(2) Compute M_n from step (1), a precise knowledge of the input attenuation ratio P_n/P_{n-1}, and equation (46)

(3) Compute $\Delta_n/k_1 P_n$ from step (2) and equation (51)

In addition to its brevity, an advantage of this technique is that the effects of instrumentation errors associated with measuring the output voltage are significantly reduced by ratioing V_n and V_{n-1} when they do not differ greatly, as when I_n is 1 decibel.

ANALYSIS OF HARMONIC TEST CIRCUIT

Consider the simplified form of the test circuit shown in figure 15. Inasmuch as input power to the circuit was measured during the test, it is convenient to express all levels in the circuit relative to the input power. Let P_{in} represent the input power, and let V_i represent the RMS input voltage. Based on an assumed 50 Ω matched input, the power is $P_{in} = V_i^2/50$ or

$$V_i = \sqrt{50 P_{in}} = 7.071\sqrt{P_{in}} \qquad (52)$$

Let v_s = Thevenin voltage seen by the diode. For an instantaneous loaded input voltage v_i, the Thevenin voltage is

$$v_s = \frac{356.4}{356.4 + 330} \times v_i = 0.5192 v_i \tag{53}$$

The Thevenin equivalent resistance R seen by the diode is $R \cong 178.2\ \Omega$.

Let v_D represent the output voltage across the diode as determined from the mathematical models developed earlier, and let v_m represent the voltage indicated by the spectrum analyzer. These voltages are related by

$$v_m = \frac{26.42}{26.42 + 330} \times v_D = 0.0741 v_D \tag{54}$$

For $v_i = V_p \cos \omega t = \sqrt{2V_i} \cos \omega t$, it is readily determined that $v_s = 0.7343 V_i \cos \omega t$. When this signal voltage is substituted in the series of equation (13b), the result for the time-varying portion v_d' of the signal after expansion is

$$\begin{aligned} v_d' = {} & (0.7343 B_1 V_i + 0.2969 B_3 V_i^3) \cos \omega t \\ & + (0.2696 B_2 V_i^2 + 0.1454 B_4 V_i^4) \cos 2\omega t \\ & + 0.09898 B_3 V_i^3 \cos 3\omega t + 0.03639 B_4 V_i^4 \cos 4\omega t \end{aligned} \tag{55}$$

Considering the measured value to be the time-varying portion, substitution of equation (55) in equation (54) yields

$$\begin{aligned} v_m = {} & (0.05441 B_1 V_i + 0.02200 B_3 V_i^3) \cos \omega t \\ & + (0.01998 B_2 V_i^2 + 0.0177 B_4 V_i^4) \cos 2\omega t \\ & + 0.007334 B_3 V_i^3 \cos 3\omega t + 0.002693 B_4 V_i^4 \cos 4\omega t \end{aligned} \tag{56}$$

Let $P_{out}^{(1)}$, $P_{out}^{(2)}$, $P_{out}^{(3)}$, and $P_{out}^{(4)}$ represent the measured power associated with frequency ω, 2ω, 3ω, and 4ω, respectively. Since the impedance is 50 Ω and the voltage expression of equation (56) involves peak values, the various power values are

$$P_{out}^{(1)} = \frac{(0.05441 B_1 V_i + 0.02200 B_3 V_i^3)^2}{100} \tag{57}$$

$$P_{out}^{(2)} = \frac{(0.01998 B_2 V_i^2 + 0.01077 B_4 V_i^4)^2}{100} \tag{58}$$

$$P_{out}^{(3)} = \frac{(0.007334B_3V_i^3)^2}{100} \tag{59}$$

$$P_{out}^{(4)} = \frac{(0.002693B_4V_i^4)^2}{100} \tag{60}$$

DISCUSSION OF MEASURED DATA

Harmonic Response Measurements

Using the procedure discussed in the section entitled "Experimental Investigation," the fundamental, second harmonic, third harmonic, and fourth harmonic components were measured as a function of the bias current. The bias current was varied from 1 μA to 1000 μA in approximately logarithmic steps. Tests were performed with both the fixed bias circuit and the flexible bias circuit. At small signal levels, the results agreed closely with those predicted from the mathematical model. At large signal levels, the shift in operating point results in some deviation due to the shift phenomenon previously discussed. However, this concept is of secondary interest in the particular discussion here and will be ignored. Since most of the results of the fixed and flexible bias circuits were virtually identical, only one set will be presented here.

Based on the procedures discussed in the section entitled "Analysis of Harmonic Test Circuit," the predicted power levels were calculated using the mathematical models developed. The results are compared with the measured levels in figures 16, 17, and 18 for input power levels of -10 dBm, -15 dBm, and -5 dBm, respectively. Corresponding tabular data for the calculated values are given in tables 7, 8, and 9. The general forms of the functions are in obvious agreement. The difference between predicted and measured values is less than 1 dB for the first-order component over most of the range. For second-, third-, and fourth-order components, the difference varies from well under 1 dB to the order of 3 dB or so, depending on the portion of the curves. Predicted maximum and minimum points are within a few percent of measured values. Considering the wide range of signal levels and attenuation (100 dB and greater), the uncertainties of various components, and imperfections in the mathematical model of the diodes, these results are felt to be quite reasonable. It is concluded that the mathematical model predicts the general behavior for the harmonic response based on a power series expansion.

Detector Sensitivity Measurements

Since the input power is proportional to the square of the input voltage, the ideal square-law detector circuit should provide an output voltage proportional to the input power. Several extensive tests were performed with the circuit and experimental procedures discussed earlier for the purpose of investigating the linearity of the output voltage as a function of input power.

Curves indicating the dc output response of the fixed bias circuit with bias current as a parameter are shown in figure 19. Ideally, these curves should have a slope proportional to the C_2 function of figure 10, and the deviation should have the form of the C_4 function. (The voltage changes were negative as indicated by fig. 10, but the magnitude is shown in fig. 19.) The predicted slope as a function

of increasing bias current is clearly evident. Theoretically, the deviation from linearity should result in an upward shift in the curves, and this is evident at higher bias currents. However, at lower bias currents, the clipping phenomenon appears to dominate.

The ac output of the fixed bias circuit is shown in figure 20. The forms for these functions will be discussed after the results obtained with the flexible bias circuit are introduced.

Curves indicating the dc output response of the flexible bias circuit are shown in figure 21. The slopes of these curves should ideally follow the D_2 function of figure 11, and the deviations should be a function of D_4. Further, the clipping phenomenon is not as pronounced as in the fixed bias circuit since the average diode current is unconstrained and can increase with the application of an input signal, thus providing a partially compensating feature.

Observe in figure 21 how the slope increases as the bias current increases from 10 μA to 80 μA and decreases for higher bias currents. This feature is readily evident also from figure 11. Ideally, $D_4 = 0$ for bias currents of about 20 μA and 180 μA.

The ac output voltage curves for the flexible bias circuit shown in figure 22 have the same forms as for the dc case. Referring back to the ac curves in figure 20 for the fixed bias circuit, the clipping phenomenon results in substantial shifts, but the general pattern has a similar nature to the functions of figures 21 and 22.

Linearity Measurements

Using the procedure described earlier, a series of tests were performed to determine the differential linearity of the test circuits as a function of the input power. The test results for the fixed bias circuit with bias currents of 10, 20, 40, 80, 180, and 320 μA are shown in figures 23 through 28.

For bias currents of 10 and 20 μA, the negative nonlinearity of both the dc and ac curves between about -20 dBm and -10 dBm is believed to be a result of clipping as previously discussed. The ac curves at 40 and 80 μA are expected to display negative nonlinearity, and this phenomenon is observed. The ac curve at 180 μA has the expected flat behavior, and the dc curve has the expected positive nonlinearity. Finally, both curves show expected positive nonlinearity at 320 μA. In all cases, there is a noise region of uncertainty of about ±0.02 or so in the fractional nonlinearity at the lower end of the power range, so the results in that region are inconclusive.

The test results for the flexible bias circuit with bias currents of 10, 20, 40, 80, 180, and 320 μA are shown in figures 29 through 34. Since the ac and dc results are the same in this case, only the ac curves are shown. The clipping effect is not nearly as significant in this case due to the effective upward shift in bias.

For a bias current of 10 μA, the fractional nonlinearity is positive as shown in figure 29. The wide range of linearity, resulting from a null in the fourth-degree coefficient, is evident at 20 μA as shown in figure 30.

Negative nonlinearity is observed at both 40 and 80 μA as shown in figures 31 and 32. The second null of the fourth-degree coefficient is evident at 180 μA as shown in figure 33. Finally, a positive nonlinearity is observed again at 320 μA as shown in figure 34.

DISCUSSION OF BIAS SHIFT IN FLEXIBLE BIAS CIRCUIT

As a means of establishing the groundwork for further investigation of applications of the flexible bias circuit, the shift of the bias current with the application of a signal as noted earlier will now be investigated. It is assumed in this analysis that the dc shift is dominated by the second-degree term. For a sinusoidal input of the form of equation (22), the dc shift ΔI_{DQ} is assumed to be of the form of the second term in the series of equation (23) and is

$$\Delta I_{DQ} = \frac{A_2}{2} V_p^2 = \frac{\alpha^2 I_{DQ} V_p^2}{4(1 + \alpha R I_{DQ})^3} \tag{61}$$

where the definition of A_2 in equation (10) was used. The value of V_p^2 may in turn be related to the input power for the experimental circuit by the procedure discussed in the section "Analysis of Harmonic Test Circuit." The relationship is

$$V_p^2 = (0.7343 V_i)^2 = (0.7343)^2 (50 P_{in}) = 26.96 P_{in} \tag{62}$$

Substitution of equation (62) in equation (61) and assumption of the circuit and diode parameter values yield

$$\Delta I_{DQ} = \frac{9429.6 P_{in} I_{DQ}}{(1 + 6665.4 I_{DQ})^3} \tag{63}$$

Let I_{DO} represent the modified bias current with signal. This quantity is

$$I_{DO} = I_{DQ} + \Delta I_{DQ} \tag{64}$$

Curves displaying the modified bias current as a function of the input power, with the initial bias as a parameter, are shown in figure 35. The corresponding tabulated data are shown in table 10. The bias shift increases with increasing input signal as would be expected. The relative shift is greater at smaller bias currents.

The calculated and experimental values are in very close agreement over a wide range of operating conditions. In fact, some of the curves nearly coincide over certain intervals. Over most of the operating regions, the calculated values tend to be slightly higher than the measured values. However, there are a few intervals in which the curves cross and the situation reverses as noted by the labels.

CONCLUSIONS

Analytical models employing power series expansions for predicting the response of square-law detectors have been investigated. Both fixed bias and flexible bias circuits were considered.

An extensive experimental investigation to establish the validity of the mathematical models was conducted. Good correlation between predicted and measured results was established in most cases. Where significant deviations were noted, logical explanations were formulated to explain those deviations. In addition to verification of the mathematical models, special calibration and measurement procedures were established.

The dc detection gain of the fixed bias circuit is higher than that of the flexible bias circuit. The basic mathematical model predicts that the ac detection gains of the fixed and flexible bias circuits are the same, and this property was observed at low input power levels. However, at larger input signal levels, measured data indicate that the flexible bias circuit shows less deviation from the ideal square-law form. These results suggest that the flexible bias circuit, which has apparently not heretofore been applied to square-law detection circuits, should be investigated further.

APPENDIX A

MODULATED WAVEFORM RESPONSE

The purpose of this development is to establish the validity of using a modulated waveform for testing the ac response of the diode. The series of equation (13b) will be used as the basis of the development although any of the power series forms in the text would suffice. The form of the particular series is

$$v_D = B_0 + B_1 v_s + B_2 v_s^2 + B_3 v_s^3 + B_4 v_s^4 \tag{A1}$$

Assume an AM signal of the form

$$v_s = V_p(1 + m \cos \omega_m t) \cos \omega_c t \tag{A2}$$

where m = modulation factor, ω_m = angular modulating frequency, and ω_c = angular carrier frequency. The low-pass zonal output is found by substituting equation (A2) into equation (A1) and taking only the low-frequency components extending from dc through the highest harmonic of ω_m. The result of this procedure may be expressed as

$$\begin{aligned} v_D' = {} & B_0 + \frac{1}{2} B_2 V_p^2 \left[1 + \frac{m^2}{2} + \frac{3}{4} \frac{B_4}{B_2} V_p^2 \left(1 + 3m^2 + \frac{3}{8} m^4\right)\right] \\ & + mB_2 V_p^2 \left[1 + \frac{3}{2} \frac{B_4}{B_2} V_p^2 \left(1 + \frac{3}{4} m^2\right)\right] \cos \omega_m t \\ & + \frac{1}{4} m^2 B_2 V_p^2 \left[1 + \frac{3}{2} \frac{B_4}{B_2} V_p^2 \left(3 + \frac{m^2}{2}\right)\right] \cos 2\omega_m t \\ & + \frac{3}{8} m^3 V_p^4 \cos 3\omega_m t + \frac{3}{64} m^4 B_4 V_p^4 \cos 4\omega_m t \end{aligned} \tag{A3}$$

where the terms are arranged in order of ascending harmonics of ω_m and grouped to facilitate a comparison between the desired outputs arising from the second-degree term of equation (A1) and these undesired, or error outputs arising from the fourth-degree term. For example, the ratio of the undesired to the desired components of the dc output is, neglecting B_0,

$$\frac{\frac{3}{4}\frac{B_4}{B_2}V_p^2\left(1 + 3m^2 + \frac{3}{8}m^4\right)}{1 + \frac{m^2}{2}} \tag{A4}$$

which approaches $\frac{3}{4}\frac{B_4}{B_2}V_p^2$ as m approaches zero. In the case of the component of ω_m, this ratio for m small is $\frac{3}{2}\frac{B_4}{B_2}V_p^2$. The point to be made is that the ac response of the detector provides an indicator of nonlinearity that differs from the dc nonlinearity by a factor which is dependent upon m. For small values of m, this factor approaches two. Thus, the ac measurement is preferable since the uncertainties associated with removing B_0 from a dc measurement do not exist. This was borne out in the experimental phase where significantly better results were obtained with the ac method of nonlinearity characterization.

REFERENCES

1. Hearn, Chase P.: Effect of Nonideal Square-Law Detection on Static Calibration in Noise-Injection Radiometers. NASA TM 85684, January 1984.

2. Hardy, Walter N.; Gray, Kenneth W.; and Love, A. W.: An S-Band Radiometer Design With High Absolute Precision. IEEE Trans. Microwave Theory and Tech., Vol. MTT-22, No. 4, April 1974, pp. 382-390.

3. Hewlett-Packard Inc.: Hot Carrier Diode Video Detectors. Application Note 923.

4. Hewlett-Packard Inc.: Dynamic Range Extension of Schottky Detectors. Application Note 956-5.

TABLE 1.- TABULATED VALUES OF NORMALIZED COEFFICIENTS OF POWER SERIES EXPANSIONS FOR i_D and v_D (SEE FIG. 3)

$\alpha RI_{DQ} \triangleq x$	$y_1 = RA_1 = \frac{x}{1+x}$	$y_2 = \frac{RA_2}{\alpha} = -\frac{B_2}{\alpha} = \frac{x}{2(1+x)^3}$	$y_3 = \frac{RA_3}{\alpha^2} = -\frac{B_3}{\alpha^2} = \frac{x(1-2x)}{6(1+x)^5}$	$y_4 = \frac{RA_4}{\alpha^3} = -\frac{B_4}{\alpha^3} = \frac{x(1-8x+6x^2)}{24(1+x)^7}$	$y_1' = B_1 = \frac{1}{1+x}$
0	0	0	0	0	1
.05	.047619	.02160	5.8764×10^{-3}	9.1056×10^{-4}	.95238
.01	.090909	.037566	.008279	5.5592×10^{-4}	.90909
.13962	.122515	.047167	.008725	0	.87749
.2	.166667	.057870	.008038	-8.3724×10^{-4}	.83333
.3	.230769	.068275	.005387	-1.7132×10^{-3}	.76923
.4	.285714	.072886	.002479	-1.9605×10^{-3}	.71429
.5	.333333	.07407407	0	-1.82899×10^{-3}	.66667
.6	.375	.073242	-.001907	-.0015274	.625
.7	.411765	.071240	-.003287	-.0011799	.58824
.8	.444444	.068587	-.004234	-.00084937	.55556
.9	.473684	.065607	-.004846	-.00056216	.52632
1.0	.5	.0625	-.005208	-.00032552	.5
1.1	.523810	.059389	-.005387	-.00013742	.47619
1.19371	.544152	.056537	-.005433	0	.45585
1.2	.545455	.056349	-.005433	8.0181×10^{-6}	.45455
1.3	.565217	.053423	-.005386	1.17725×10^{-4}	.43478
1.4	.583333	.050637	-.005275	1.9841×10^{-4}	.41667
1.5	.6	.048	-.00512	2.56×10^{-4}	.4
1.6	.615385	.045517	-.004938	2.9549×10^{-4}	.38462
1.7	.629630	.043184	-.004739	3.2097×10^{-4}	.37037

TABLE 2.- TABULATED VALUES OF NORMALIZED COEFFICIENTS OF POWER SERIES EXPANSION FOR DC VOLTAGE SHIFT WITH FIXED BIAS (SEE FIG. 6)

x	$4C_2/\alpha$	$64C_4/\alpha^3$
0	-1	-7
.05	-.90703	-5.2347
.1	-.82645	-3.9852
.15	-.75614	-3.0847
.2	-.69444	-2.4247
.25	-.64	-1.9333
.3	-.59172	-1.56211
.4	-.51020	-1.05717
.5	-.44444	-.74623
.6	-.39063	-.54598
.7	-.34602	-.41181
.8	-.30864	-.31871
.9	-.27701	-.25209
1.0	-.25	-.20312
1.1	-.22676	-.16627
1.2	-.20661	-.13794
1.3	-.18904	-.11578
1.4	-.17361	-.09817
1.5	-.161	-.08397
1.6	-.14793	-.07238

TABLE 3.- TABULATED VALUES OF NORMALIZED COEFFICIENTS OF POWER SERIES EXPANSION FOR DC VOLTAGE SHIFT WITH FLEXIBLE BIAS (SEE FIG. 9)

x	$4D_2/\alpha$	$64D_4/\alpha^3$
0	0	0
.02	-0.018846	-0.014667
.04	-.035560	-.020962
.052	-.044664	-.021888
.06	-.050377	-.02161
.08	-.063507	-.018597
.1	-.075131	-.013342
.1396	-.09433	0
.2	-.11574	.020094
.3	-.13655	.041117
.35	-.14225	.045612
.4	-.14577	.04705
.45	-.14761	.046247
.5	-.14815	.043896
.6	-.14648	.036657
.7	-.14248	.028318
.8	-.13717	.020385
.9	-.13121	.013492
1	-.125	.007813
1.1	-.11878	.003298
1.1937	-.11307	0
1.2	-.11270	-.0001924
1.3	-.10685	-.002825
1.4	-.10127	-.004762
1.5	-.096	-.006144
2	-.07407	-.008230
2.3	-.06400	-.007739
2.4	-.06106	-.007476

TABLE 4.- CALCULATED SECOND- AND FOURTH-DEGREE COEFFICIENTS FOR FIXED BIAS TEST CIRCUIT WITH $n = 1.04$ and $R = 178.2\ \Omega$ (SEE FIG. 10)

I_{DQ}, μA	C_2	C_4	C_4/C_2
1	-9.228	-5500	596.1
2	-9.107	-5287	580.6
5	-8.758	-4706	537.4
10	-8.219	-3901	474.6
20	-7.280	-2742	376.7
50	-5.260	-1116	212.1
80	-3.978	-548	137.8
100	-3.367	-368.9	109.6
180	-1.932	-112.8	58.39
300	-1.039	-34.79	33.47
500	-.4981	-9.102	18.27
1000	-.1591	-1.103	6.928

TABLE 5.- CALCULATED SECOND- AND FOURTH-DEGREE COEFFICIENTS FOR FLEXIBLE BIAS TEST CIRCUIT WITH $n = 1.04$ AND $R = 178.2\ \Omega$ (SEE FIG. 11)

I_{DQ}, μA	D_2	D_4	D_4/D_2
1	-0.061098	-4.9263	80.630
2	-.11980	-8.8860	74.174
5	-.28245	-16.0310	56.757
10	-.51358	-17.1179	33.330
20	-.85638	-1.8233	2.129
20.9471	-.88211	0	0
50	-1.3149	36.3770	-27.6649
57.3061	-1.3533	38.2930	-28.2963
100	-1.3466	25.4412	-18.8930
179.0990	-1.0573	0	0
200	-.98158	-2.8908	2.9451
392.7767	-.51692	-5.5870	10.8082
500	-.38316	-3.8961	10.1683
1000	-.13838	-.75087	5.4260
75.015	-1.38533	35.8914	-25.9082
80	-1.3834	34.1438	-24.6810
300	-.6928	-6.7298	9.7139

TABLE 6.- INPUT POWER LEVEL PRODUCING A 10 PERCENT SHIFT IN QUIESCENT CURRENT AND THE CORRESPONDING TOTAL PEAK SHIFT

I_{DQ}, μA	P_{in}, dBm	I_{lp}, μA	Total shift, μA
1	-19.66	0.635	0.735
2	-19.57	1.273	1.473
5	-19.32	3.215	3.715
10	-18.90	6.532	7.532
20	-18.11	13.466	15.466
50	-16.00	36.514	41.514
80	-14.18	62.650	70.650
100	-13.09	81.646	91.646
180	-9.47	168.846	186.846
200	-8.71	193.208	*213.208
500	-.64	658.23	*708.23
1000	6.79	1751.04	*1851.04

*Clipping occurs in these cases.

TABLE 7.- CALCULATED POWER LEVELS AND CORRESPONDING COEFFICIENTS FOR HARMONIC MEASUREMENTS IN FIXED BIAS CIRCUIT AT -10 dBm LEVEL (SEE FIG. 16 FOR COMPARISON WITH MEASURED VALUES)

I_{DQ}, μA	Power series coefficients				Harmonic power levels, dBm			
	B_1	B_2	B_3	B_4	$P_{out}^{(1)}$	$P_{out}^{(2)}$	$P_{out}^{(3)}$	$P_{out}^{(4)}$
1	0.9934	-0.1222	-1.4834	-13.1368	-38.38	-86.06	-98.30	-111.07
2	.9868	-.2396	-2.8317	-23.6960	-38.46	-80.37	-92.68	-105.94
5	.9677	-.5649	-6.1564	-42.7492	-38.69	-73.36	-85.94	-100.82
10	.9375	-1.0272	-9.7556	-45.6479	-39.04	-68.79	-81.94	-100.25
20	.8824	-1.7128	-12.1935	-4.8621	-39.63	-65.27	-80.00	-119.70
20.9471	.8775	-1.7642	-12.2073	0	-39.68	-65.08	-79.99	$-\infty$
50	.7500	-2.6298	-6.1509	97.0053	-40.94	-62.52	-85.95	-93.70
75.015	.6667	-2.7707	0	95.7106	-41.82	-62.01	$-\infty$	-93.82
100	.6000	-2.6932	4.0269	67.8432	-42.62	-62.01	-89.62	-96.81
179.0990	.4558	-2.1146	7.6014	0	-44.83	-63.50	-84.11	$-\infty$
200	.4286	-1.9632	7.4922	-7.7088	-45.35	-64.06	-84.23	-115.70
500	.2308	-.7663	2.8835	-10.3895	-50.82	-72.01	-92.53	-113.10
1000	.1305	-.2768	.7242	-2.0023	-55.89	-81.00	-104.53	-127.41

TABLE 8.- CALCULATED POWER LEVELS AND CORRESPONDING COEFFICIENTS FOR HARMONIC MEASUREMENTS IN FIXED BIAS CIRCUIT AT -15 dBm LEVEL (SEE FIG. 17 FOR COMPARISON WITH MEASURED VALUES)

I_{DQ}, μA	Power series coefficients				Harmonic power levels, dBm			
	B_1	B_2	B_3	B_4	$P_{out}^{(1)}$	$P_{out}^{(2)}$	$P_{out}^{(3)}$	$P_{out}^{(4)}$
1	0.9934	-0.1222	-1.4834	-13.1368	-43.35	-97.51	-113.30	-131.07
2	.9868	-.2396	-2.8317	-23.6960	-43.43	-91.72	-107.68	-125.94
5	.9677	-.5646	-6.1564	-42.7492	-43.62	-84.43	-100.94	-120.82
10	.9375	-1.0272	-9.7556	-45.6479	-43.92	-79.45	-96.94	-120.25
20	.8824	-1.7128	-12.1935	-4.8621	-44.46	-75.31	-95.00	-139.70
20.9471	.8775	-1.7642	-12.2073	0	-44.51	-75.08	-94.99	$-\infty$
50	.7500	-2.6298	-6.1509	97.0053	-45.84	-71.89	-100.95	-113.70
75.015	.6667	-2.7707	0	95.7106	-46.82	-71.42	$-\infty$	-113.82
100	.6000	-2.6932	4.0269	67.8432	-47.70	-71.59	-104.62	-116.81
179.0990	.4558	-2.1146	7.6014	0	-50.03	-73.50	-99.11	$-\infty$
200	.4286	-1.9632	7.4922	-7.7088	-50.56	-74.12	-99.23	-135.70
500	.2308	-.7663	2.8835	-10.3895	-55.96	-82.22	-107.53	-133.10
1000	.1305	-.2768	.7242	-2.0023	-60.95	-91.11	-119.53	-147.41

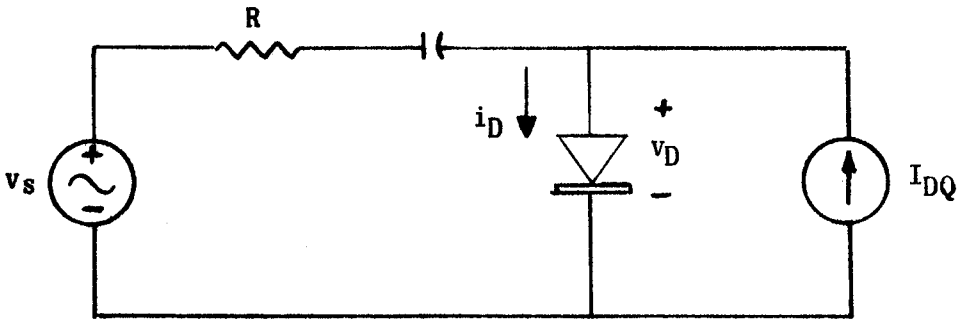
TABLE 9.- CALCULATED POWER LEVELS AND CORRESPONDING COEFFICIENTS FOR HARMONIC MEASUREMENTS IN FIXED BIAS CIRCUIT AT -5 dBm LEVEL (SEE FIG. 18 FOR COMPARISON WITH MEASURED VALUES)

I_{DQ}, μA	Power series coefficients				Harmonic power levels, dBm			
	B_1	B_2	B_3	B_4	$P_{out}^{(1)}$	$P_{out}^{(2)}$	$P_{out}^{(3)}$	$P_{out}^{(4)}$
1	0.9934	-0.1222	-1.4834	-13.1368	-33.44	-72.06	-83.30	-91.07
2	.9868	-.2396	-2.8317	-23.6960	-33.57	-67.11	-77.68	-85.94
5	.9677	-.5644	-6.1564	-42.7492	-33.94	-60.65	-70.94	-80.82
10	.9375	-1.9272	-9.7556	-45.6479	-34.46	-56.99	-66.94	-80.25
20	.8824	-1.7128	-12.1935	-4.8621	-35.19	-55.13	-65.00	-99.70
20.9471	.8775	-1.7642	-12.2073	0	-35.24	-55.08	-64.99	-∞
50	.7500	-2.6298	-6.1509	97.0053	-36.26	-54.89	-70.95	-73.70
75.015	.6667	-2.7707	0	95.7106	-36.82	-54.19	-∞	-73.82
100	.6000	-2.6932	4.0269	67.8432	-37.37	-53.50	-74.63	-76.81
179.0990	.4558	-2.1146	7.6014	0	-39.24	-53.50	-69.11	-∞
200	.4286	-1.9632	7.4922	-7.7088	-39.74	-53.86	-69.23	-95.70
500	.2308	-.7663	2.8835	-10.3895	-45.36	-61.37	-77.53	-93.11
1000	.1305	-.2768	.7242	-2.0023	-50.68	-70.65	-89.53	-107.41

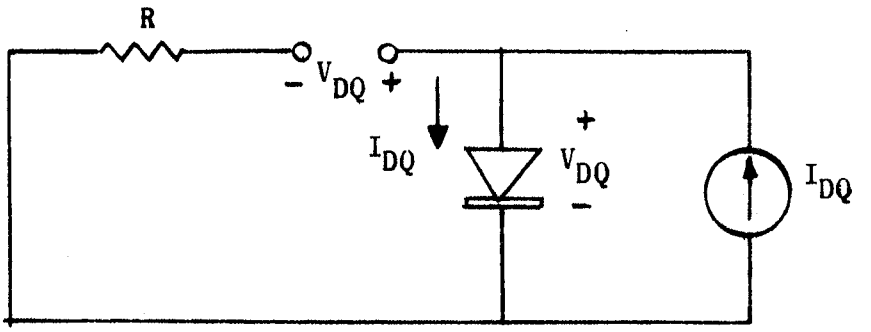
TABLE 10.- CALCULATED AND MEASURED MODIFIED BIAS CURRENT FOR FLEXIBLE BIAS CIRCUIT (SEE FIG. 35)

P_{in}, dBm	Modified bias current in μA after shift with I_{DQ} as a parameter									
	Calculated					Measured				
	I_{DQ} = 10 μA	I_{DQ} = 20 μA	I_{DQ} = 80 μA	I_{DQ} = 180 μA	I_{DQ} = 300 μA	I_{DQ} = 10 μA	I_{DQ} = 20 μA	I_{DQ} = 80 μA	I_{DQ} = 180 μA	I_{DQ} = 300 μA
-2	59.02	101.74	212.04	280.60	366.13	60	87	163	257	360
-3	48.94	84.93	184.88	259.91	352.53	49	75	150	242	350
-4	40.93	71.57	163.31	243.47	341.72	40	64	137	230	340
-5	34.57	60.97	146.18	230.42	333.14	34	56	127	220	330
-6	29.52	52.54	132.57	220.05	326.33	29	49.5	118	212	322
-7	25.50	45.85	121.76	211.81	320.91	24.5	43.9	111	206	320
-8	22.31	40.53	113.17	205.27	316.61	21.5	39	105	200	319
-9	19.78	36.31	106.35	200.07	313.19	18.8	35.5	100	196	317
-10	17.77	32.96	100.93	195.94	310.48	17	32	97	192	315
-11	16.17	30.29	96.62	192.66	308.32	15.5	30	94	190	
-12	14.90	28.17	93.20	190.06	306.61	14.2	28	91	189	
-13	13.89	26.49	90.49	187.99	305.25	13.5	26	89	187	
-14	13.09	25.16	88.33	186.35	304.17	12.8	24.9	87.8	186	
-15	12.46	24.10	86.62	185.04	303.31	12.3	24	86.2	185	310
-16	11.95	23.25	85.26	184.00	302.63	12	23.1	85.8	183	
-17	11.55	22.58	84.18	183.18	302.09	11.7	22.5	85	183	
-18	11.23	22.05	83.32	182.53	301.66	11.3	22	84	182	
-19	10.98	21.63	82.63	182.01	301.32	11.1	21.5	83.6	181	
-20	10.78	21.30	82.09	181.59	301.05	11	21	83	181	305

(a) Shunt Diode Circuit



(b) DC Circuit



(c) Dynamic Circuit

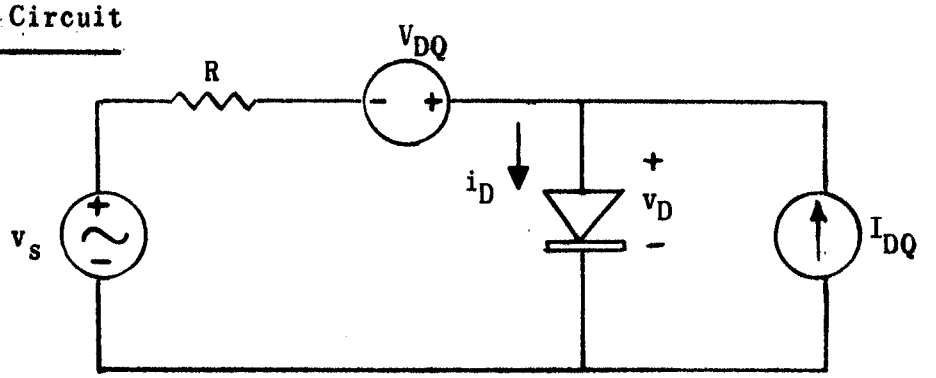


Fig. 1. Shunt diode fixed bias detector circuit and models employed in analysis.

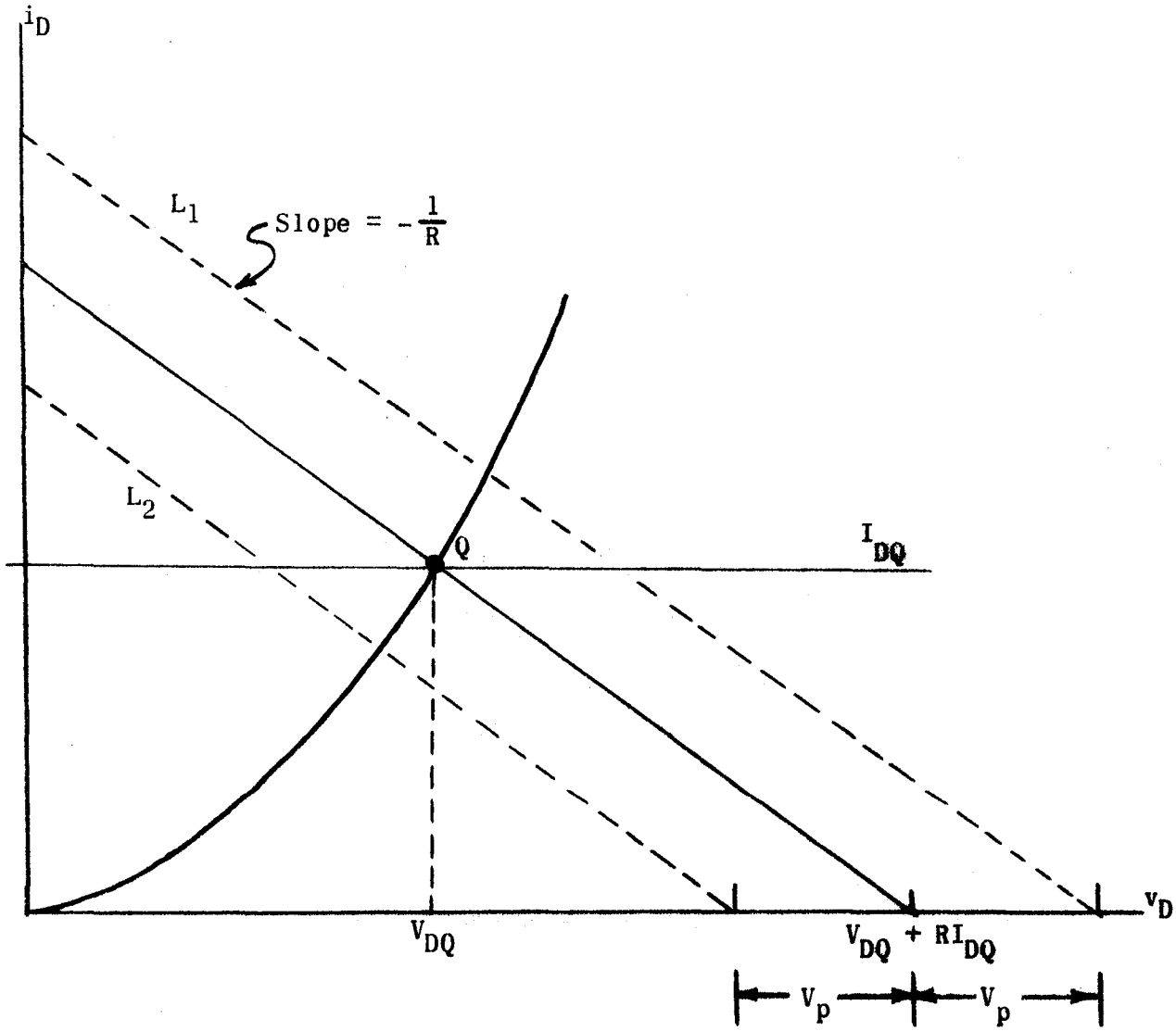


Fig. 2. Load line representation of fixed bias detector circuit.

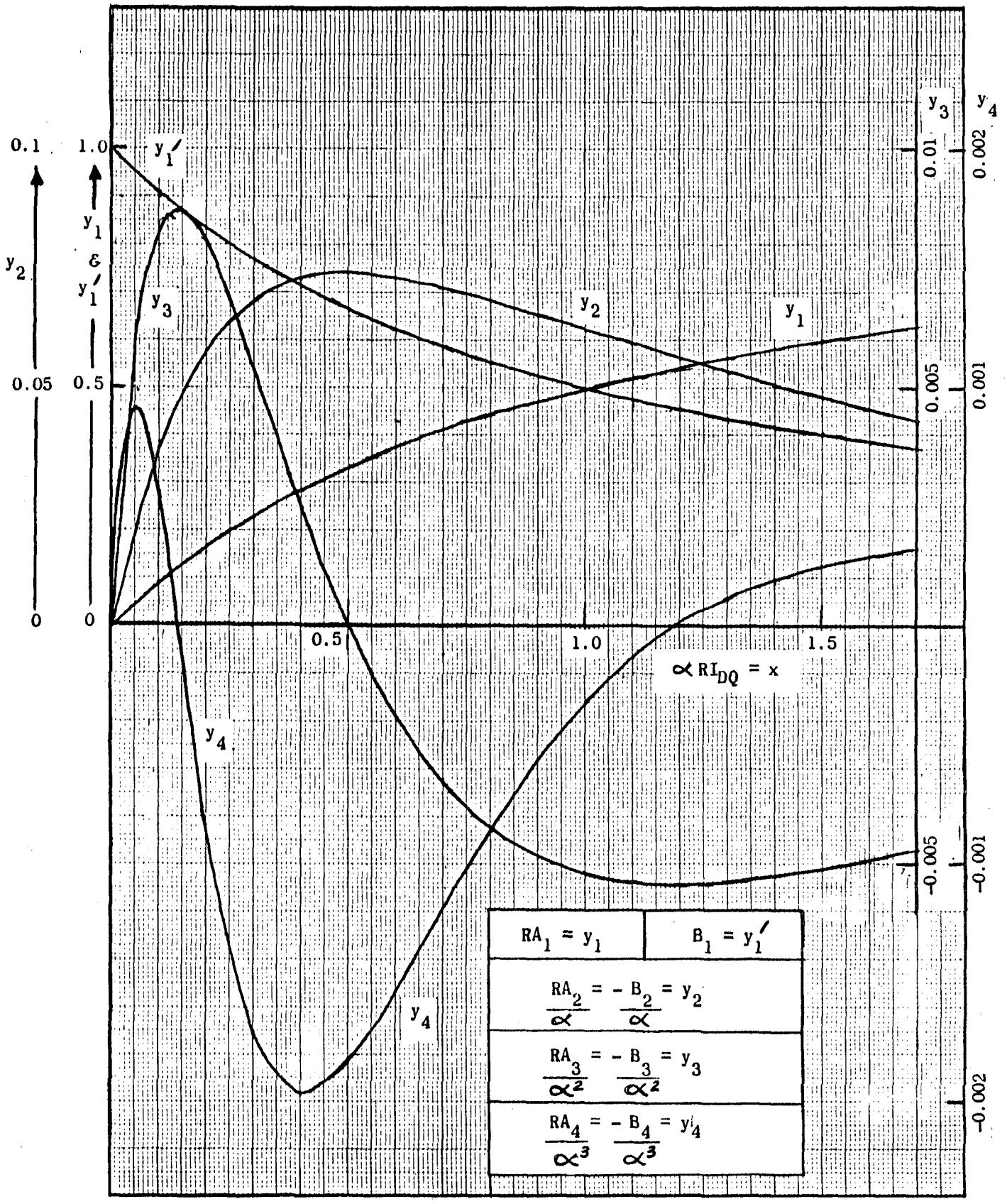
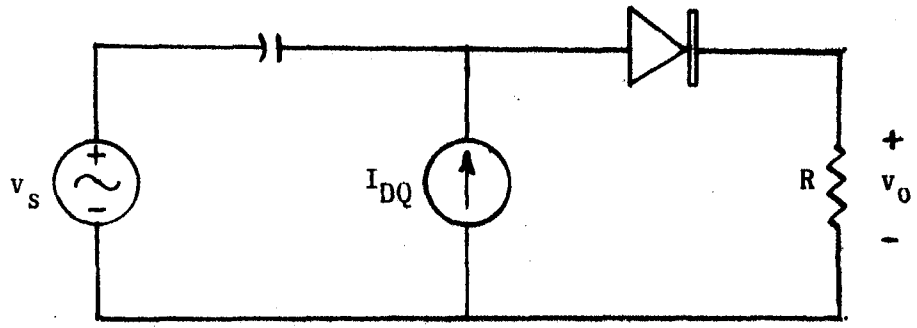
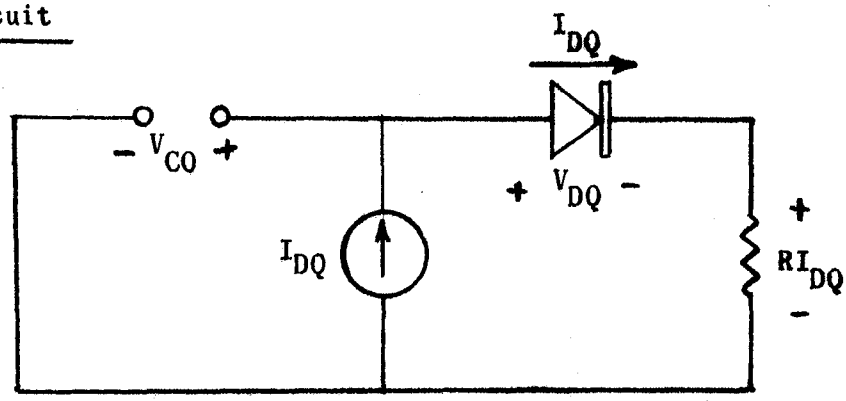


Fig. 3. Normalized coefficients of power series expansion for i_D and v_D.

(a) Series Diode Circuit



(b) DC Circuit



(c) Dynamic Circuit

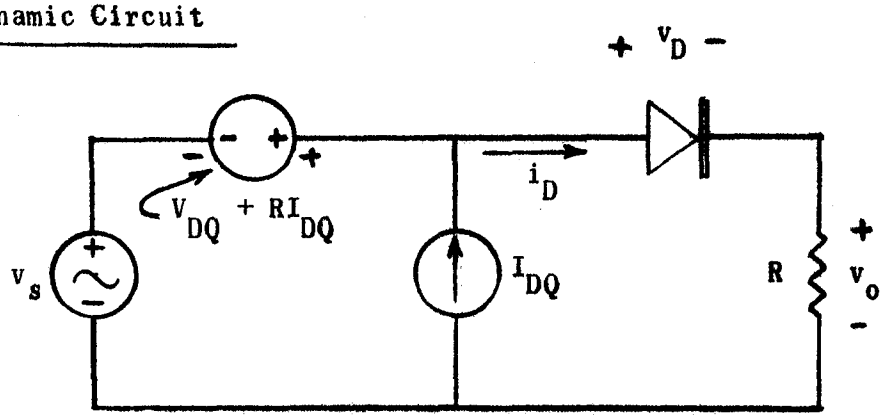


Fig. 4. Series diode fixed bias detector circuit and models employed in analysis.

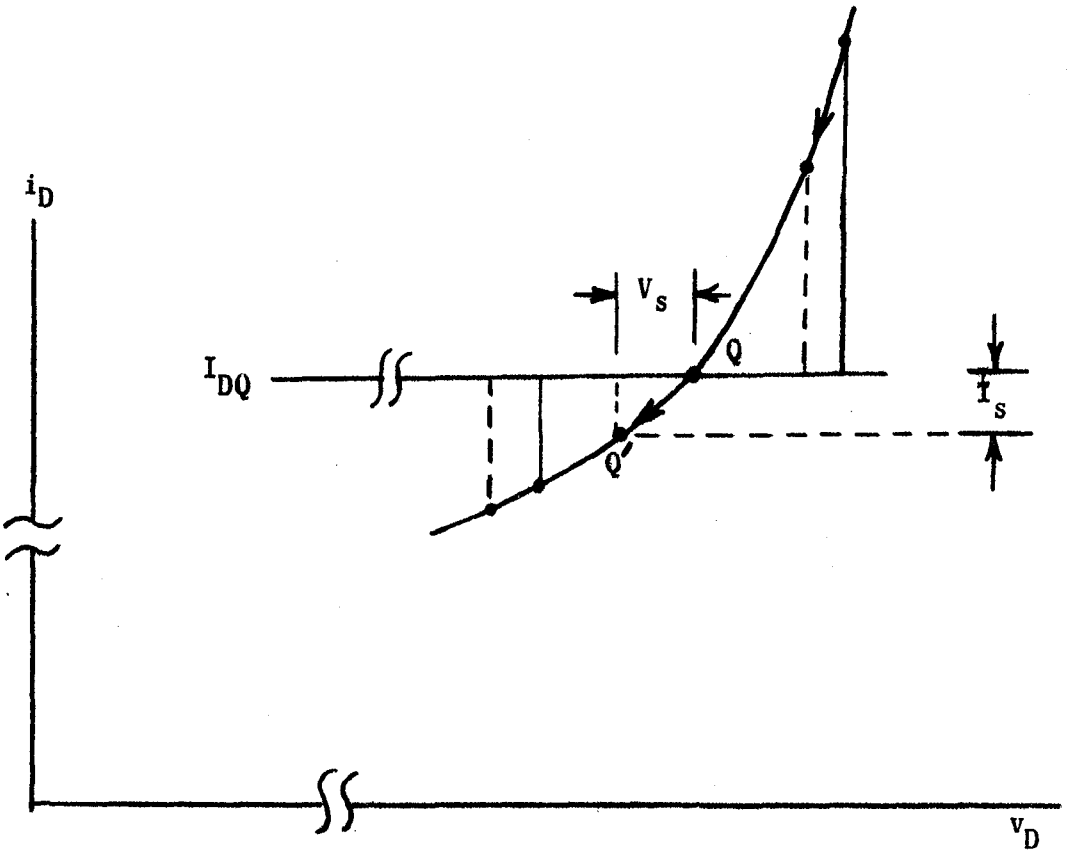


Fig. 5. Effective shift of Q-point with application of signal in shunt diode circuit.

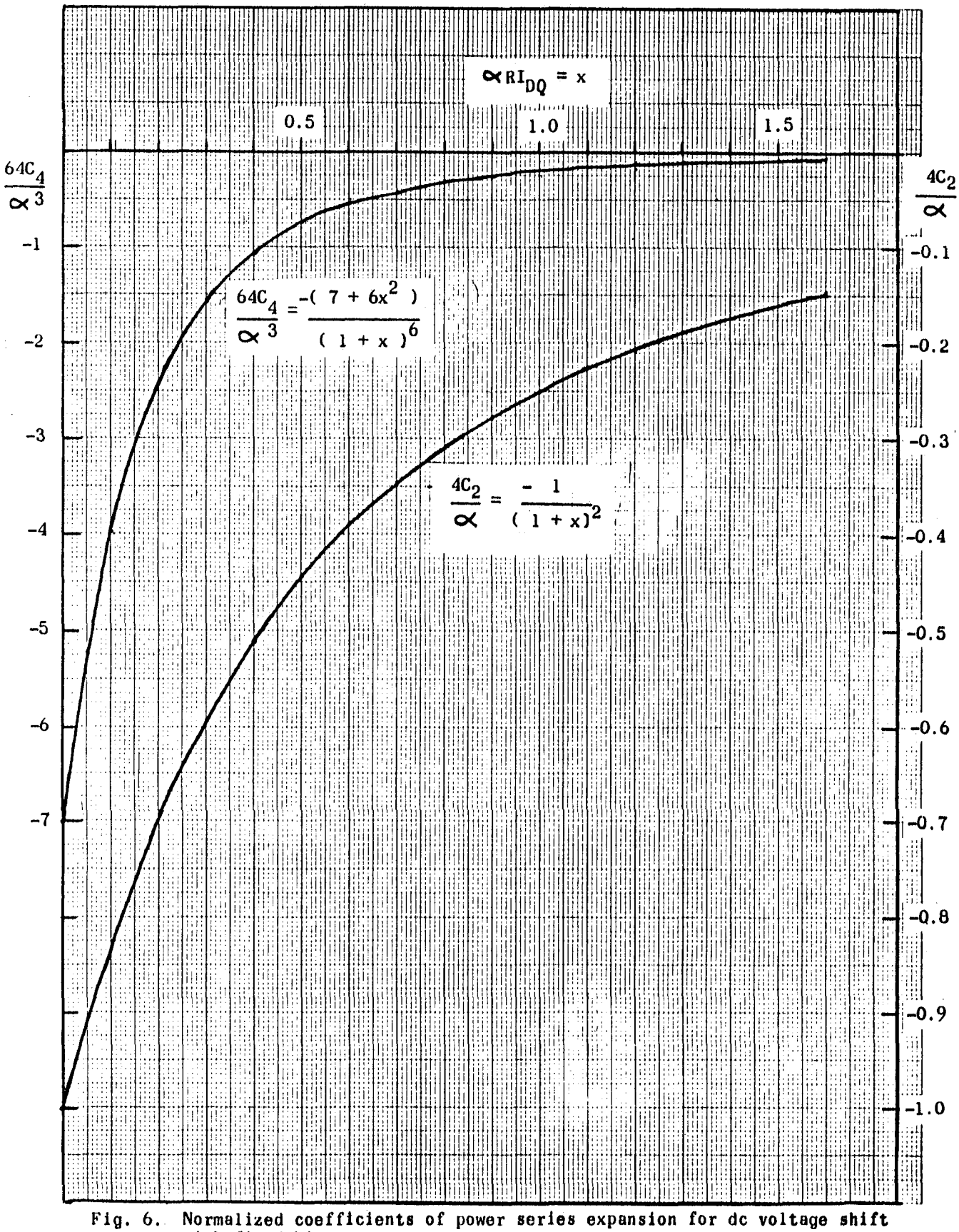


Fig. 6. Normalized coefficients of power series expansion for dc voltage shift with fixed bias.

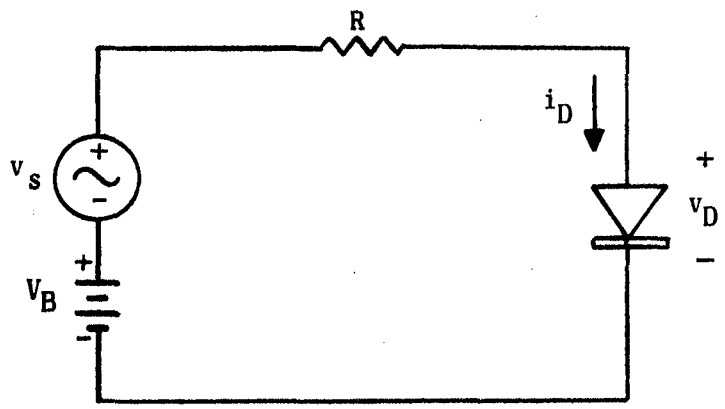


Fig. 7. Flexible bias diode circuit model.

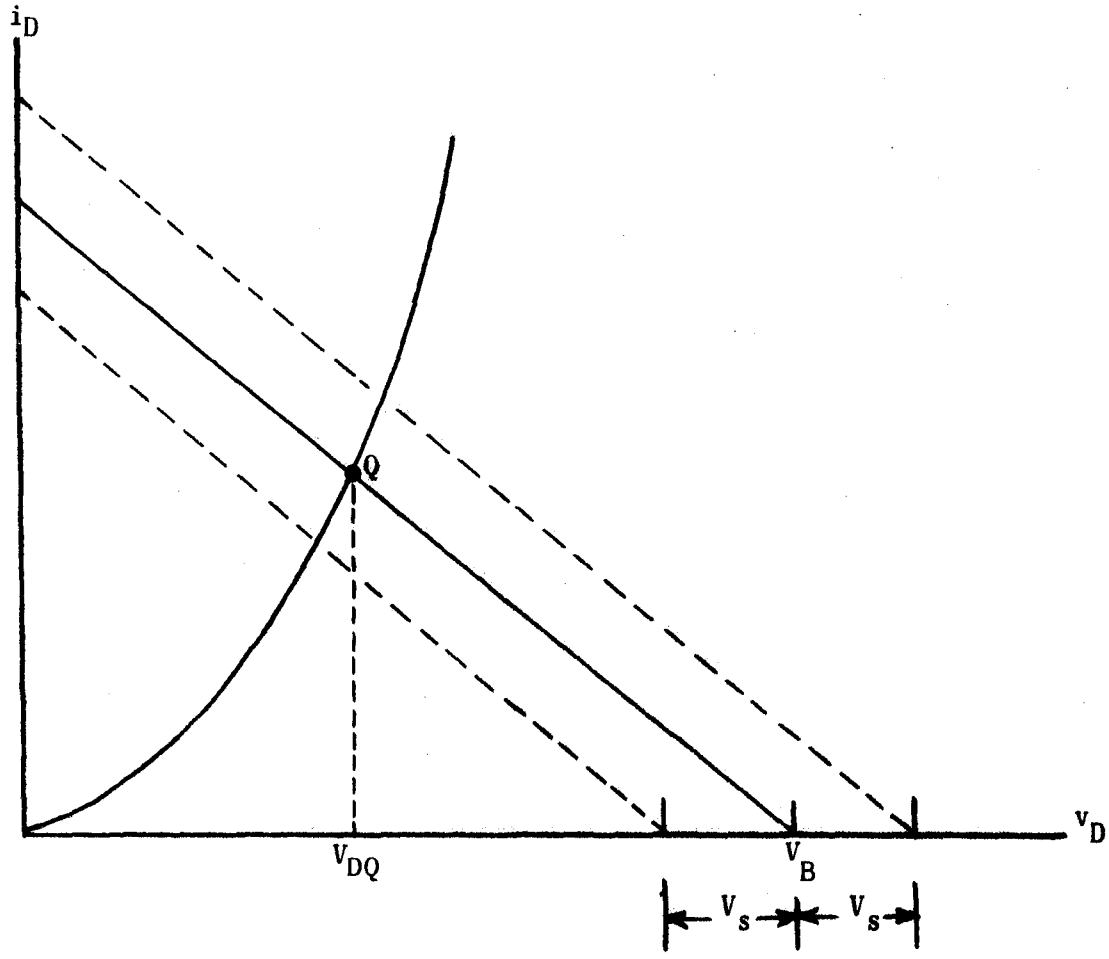


Fig. 8. Load line representation of flexible bias detector circuit.

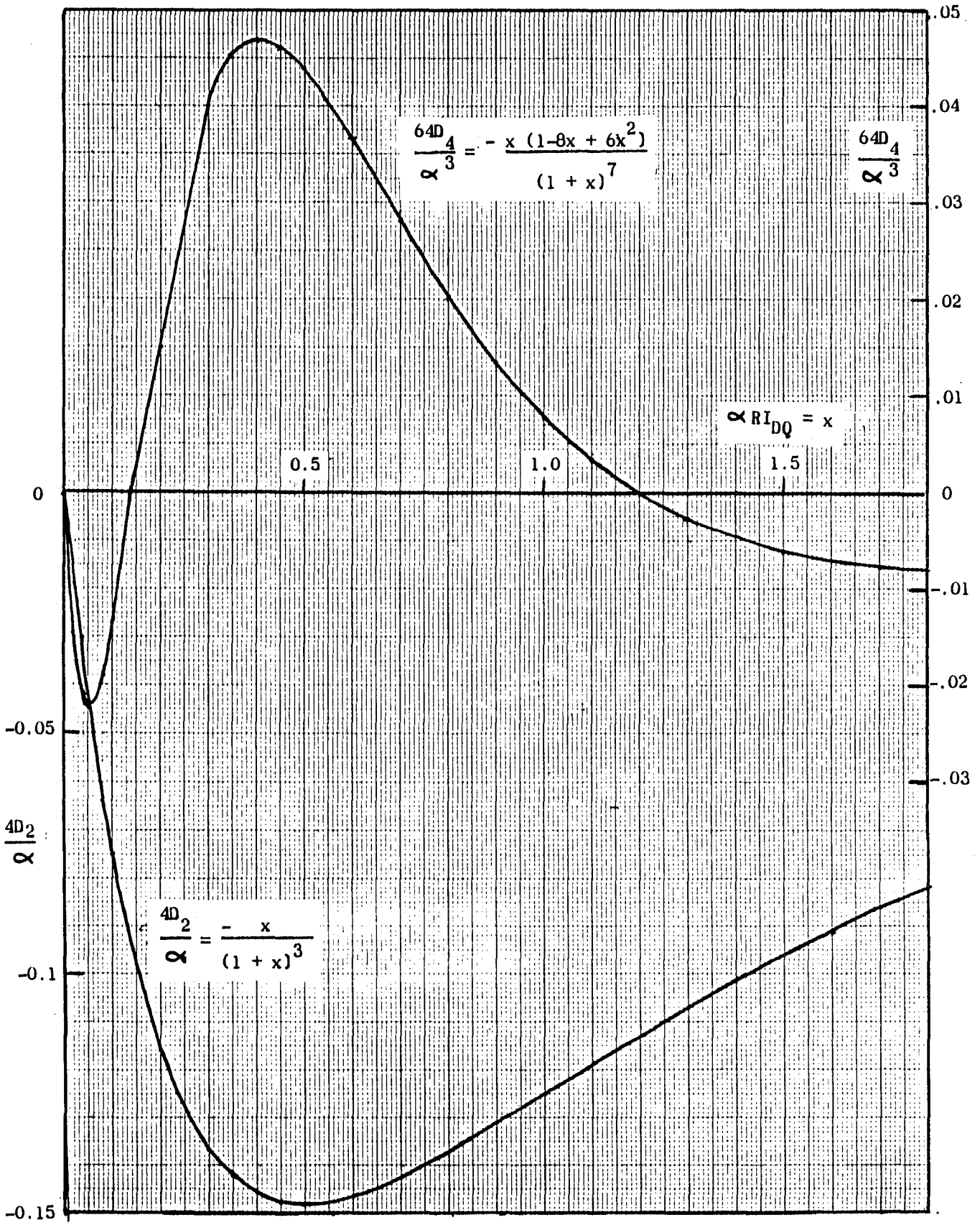


Fig. 9. Normalized coefficients of power series expansion for dc voltage shift with flexible bias.

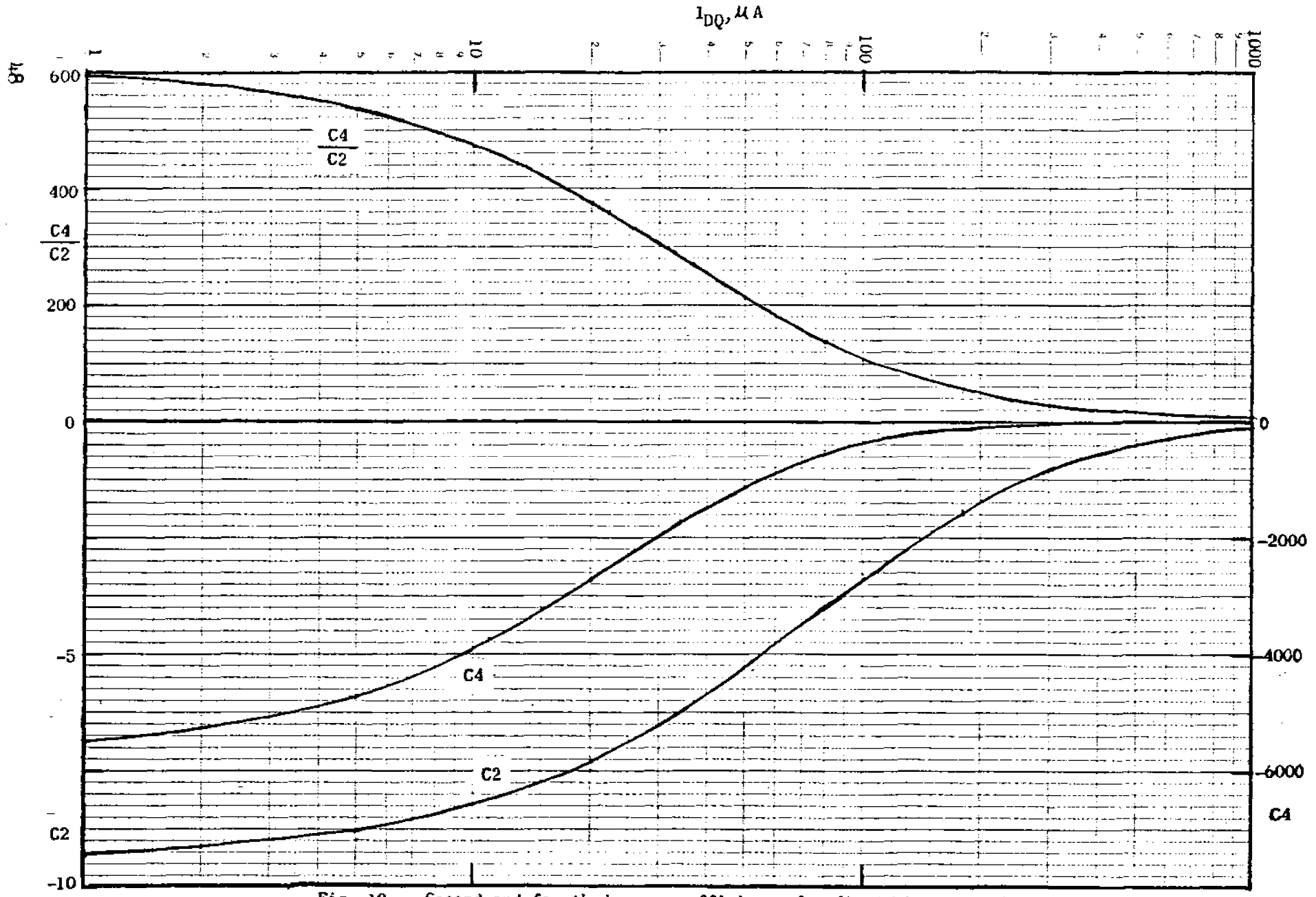


Fig. 10. Second and fourth degree coefficients for fixed bias test circuit.

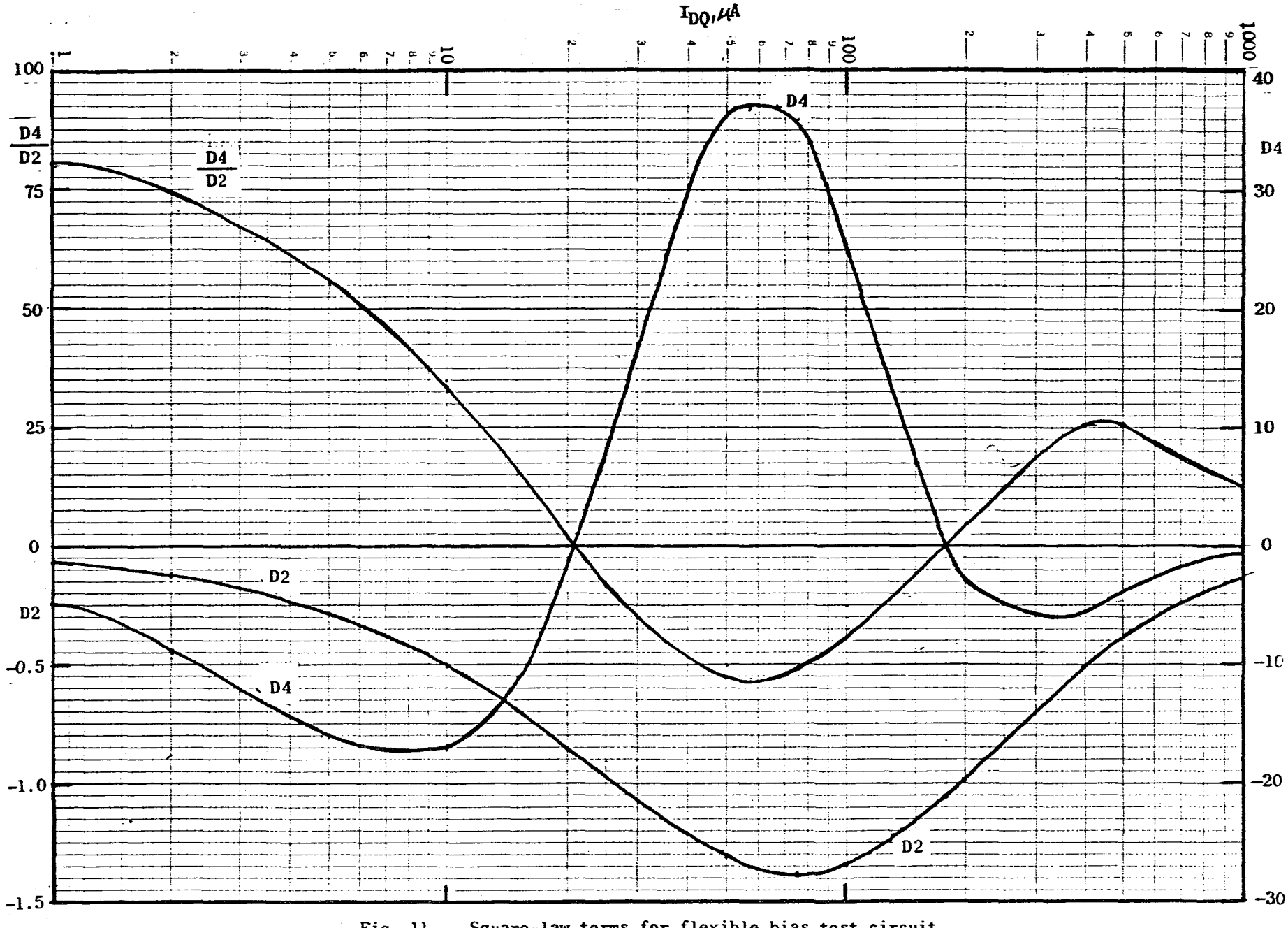
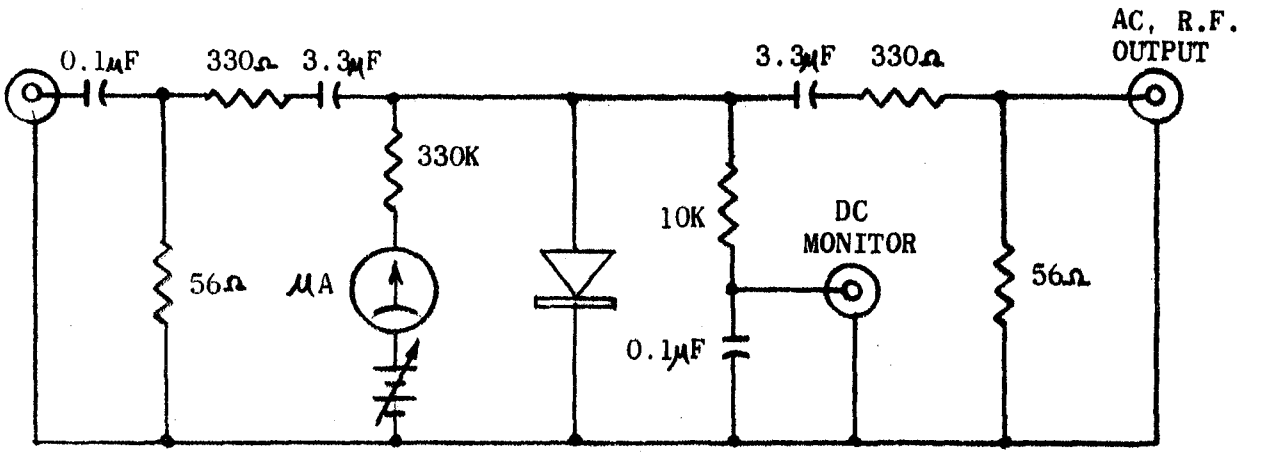
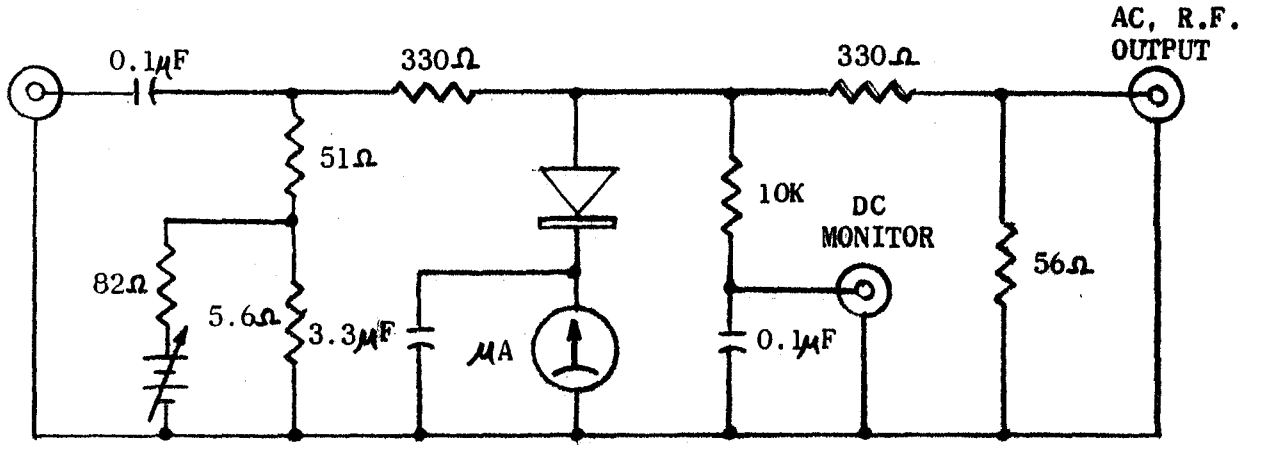


Fig. 11. Square-law terms for flexible bias test circuit.



(a). Fixed-Bias Test Circuit



(b). Flexible-Bias Test Circuit

Fig. 12. Detector Test Circuits

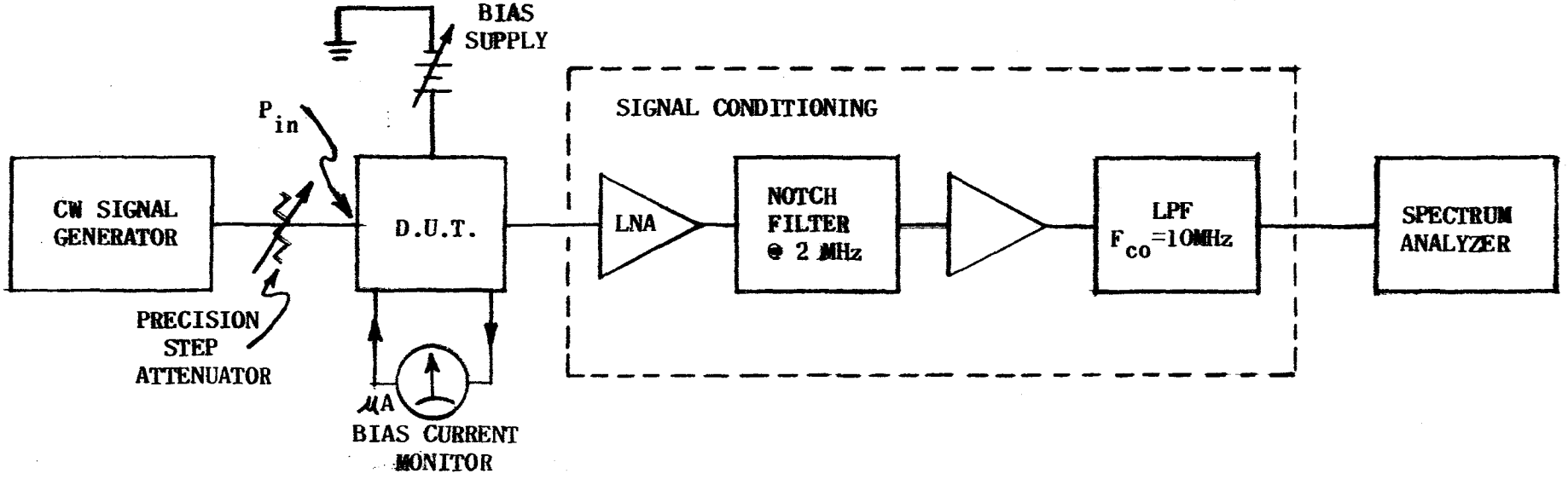


Fig. 13. Harmonic-Response Measurement Configuration

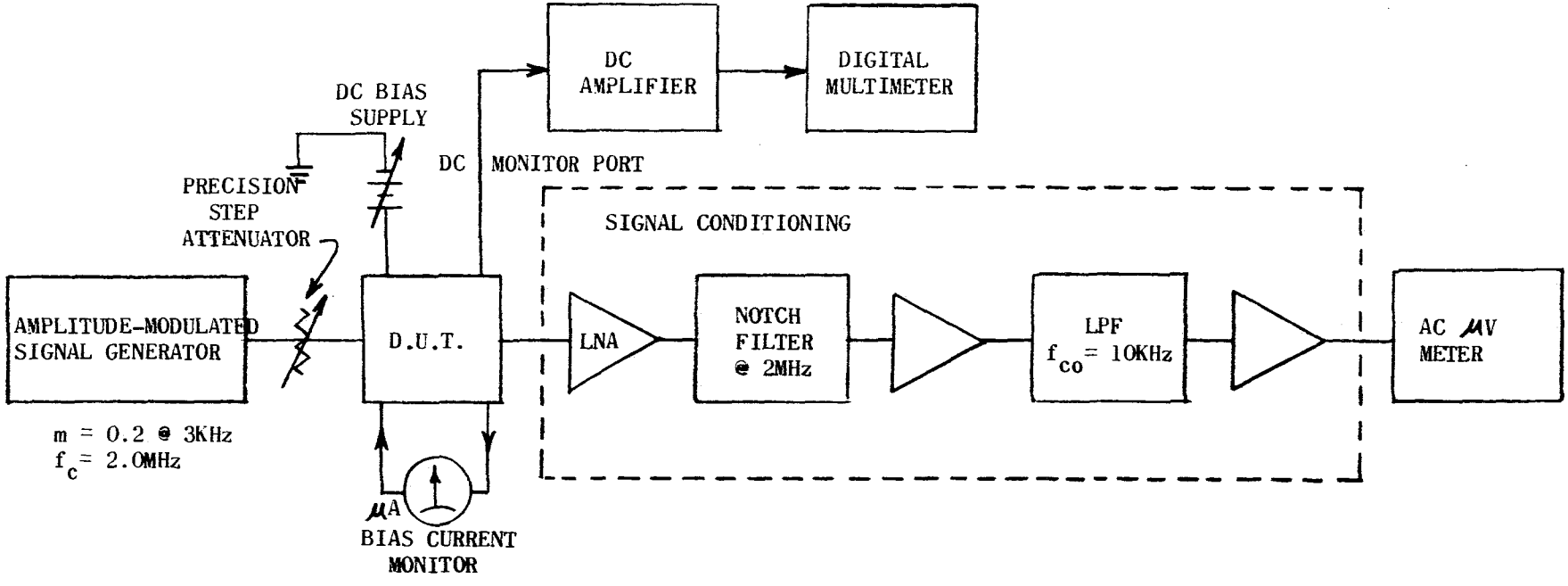


Fig. 14. Video and dc Linearity Measurement Configuration

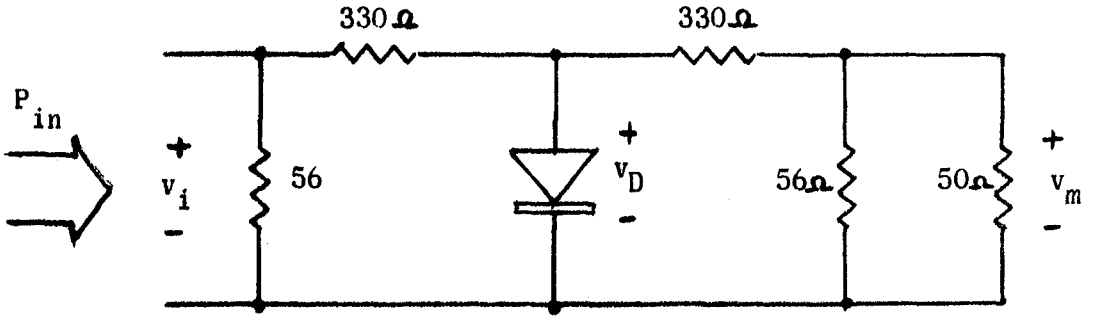


Fig. 15. Simplified form of test circuit.

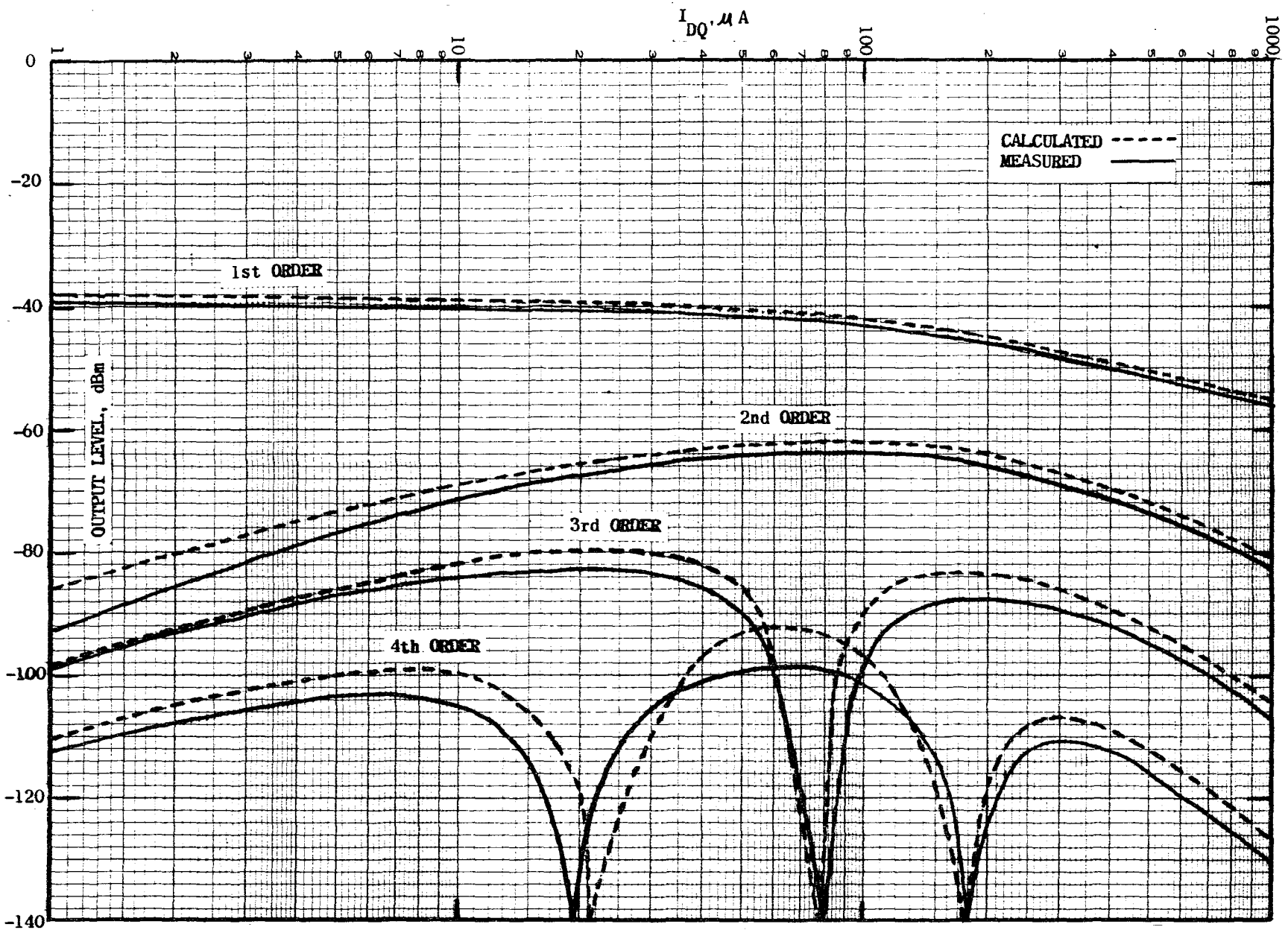


Fig. 16. Calculated and measured power levels in harmonic test at input power level of -10 dBm.

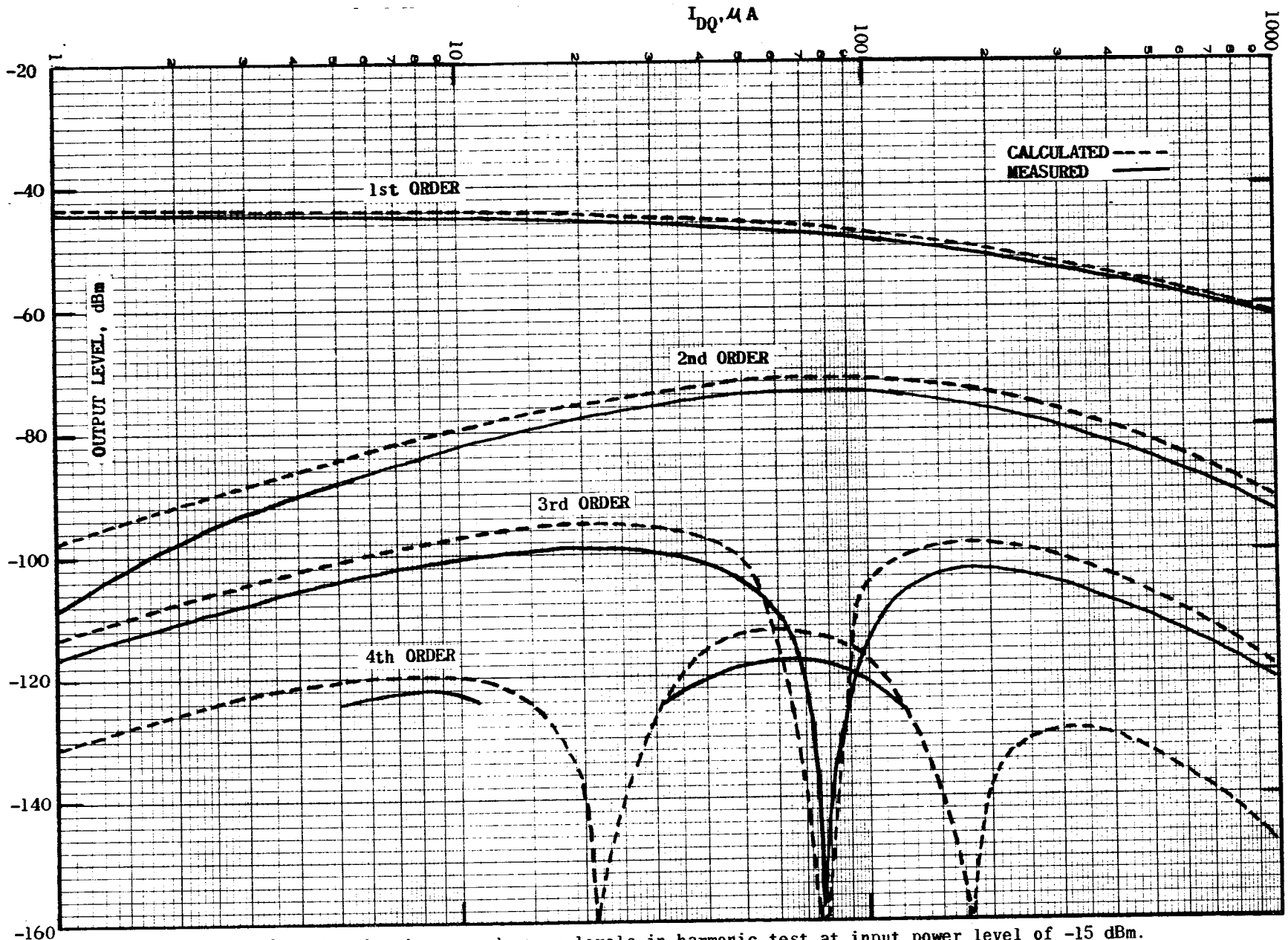


Fig. 17. Calculated and measured power levels in harmonic test at input power level of -15 dBm.

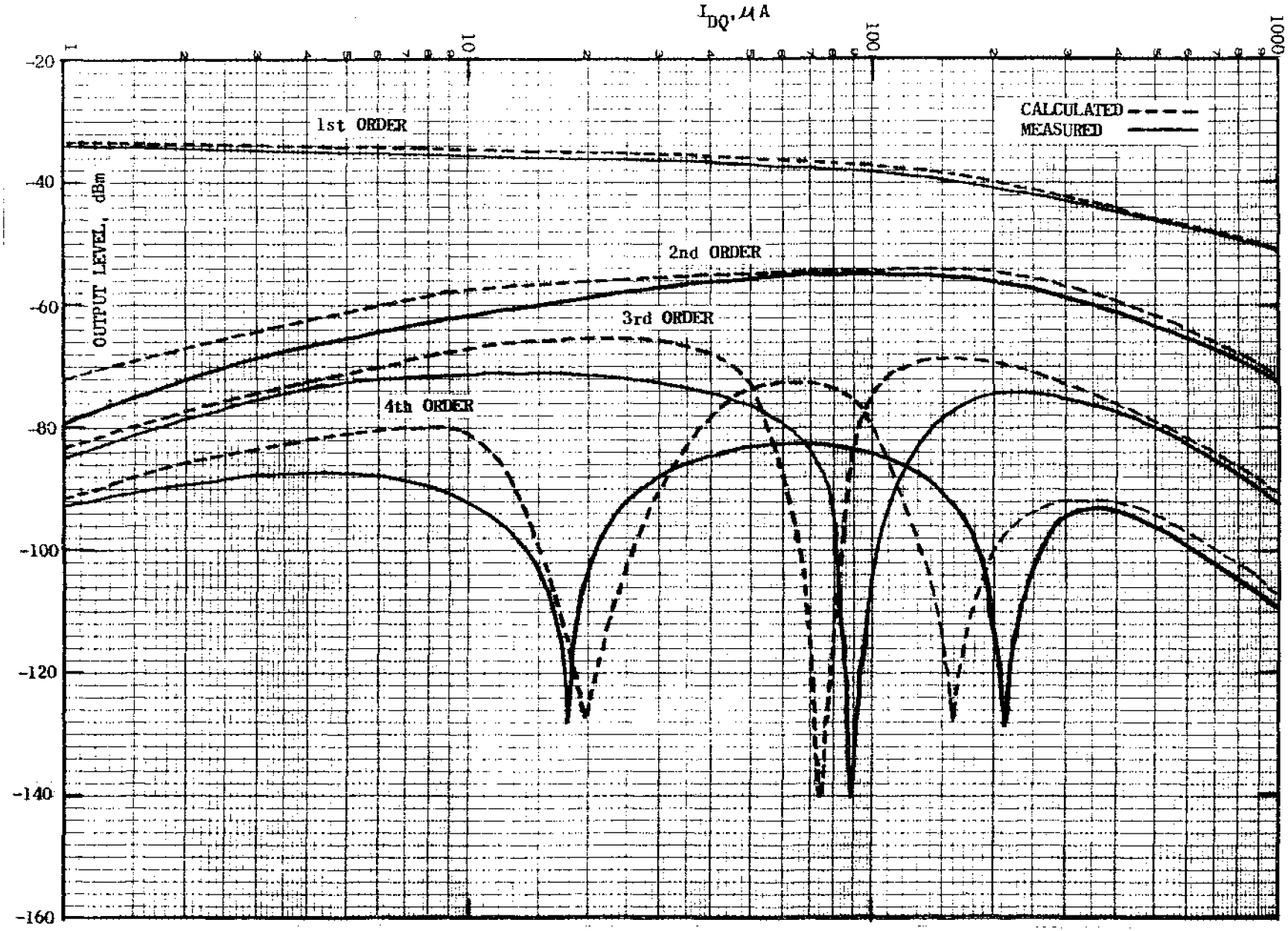


Fig. 18. Calculated and measured power levels in harmonic test at input level of -5 dBm.

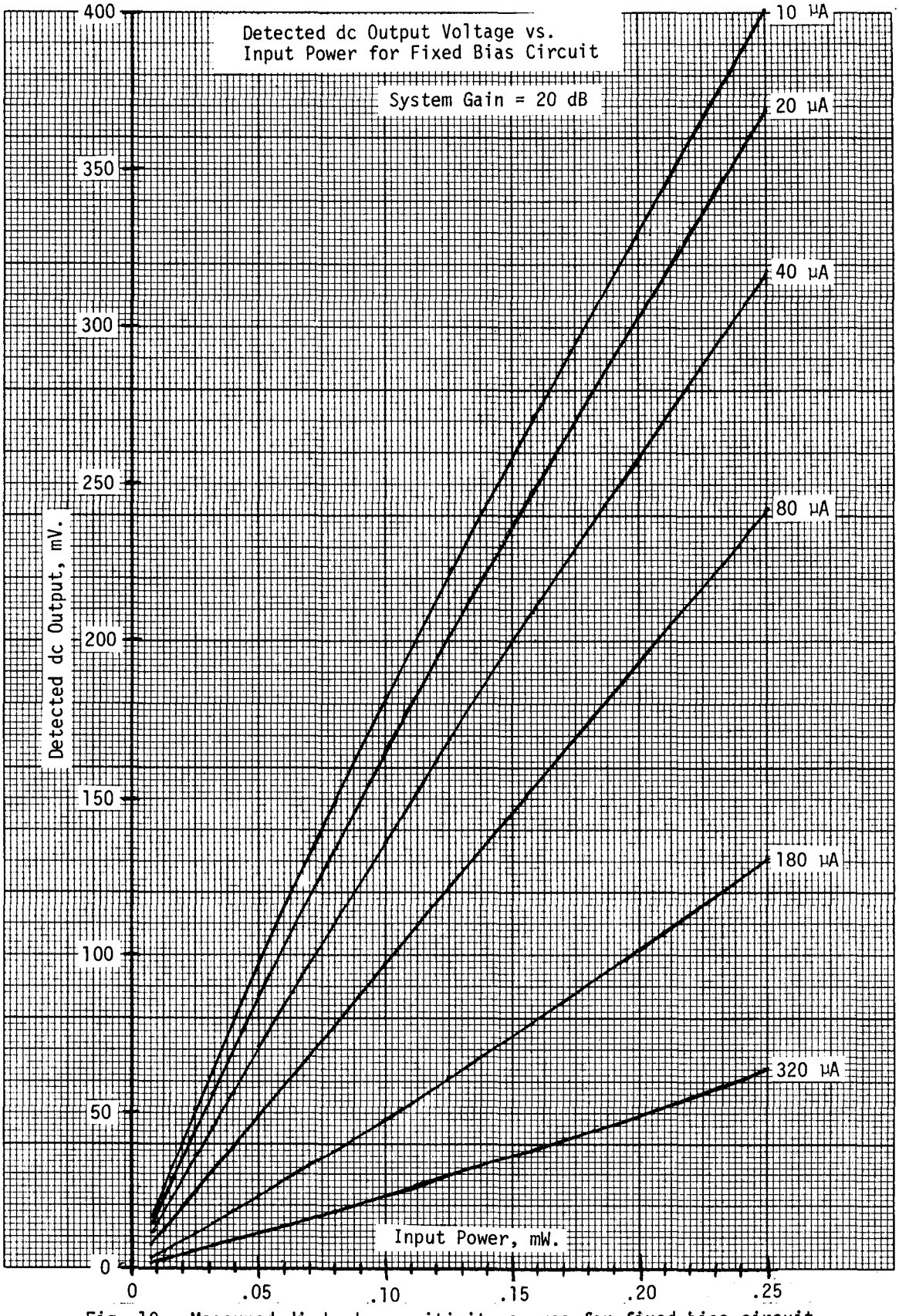


Fig. 19. Measured diode dc sensitivity curves for fixed bias circuit.

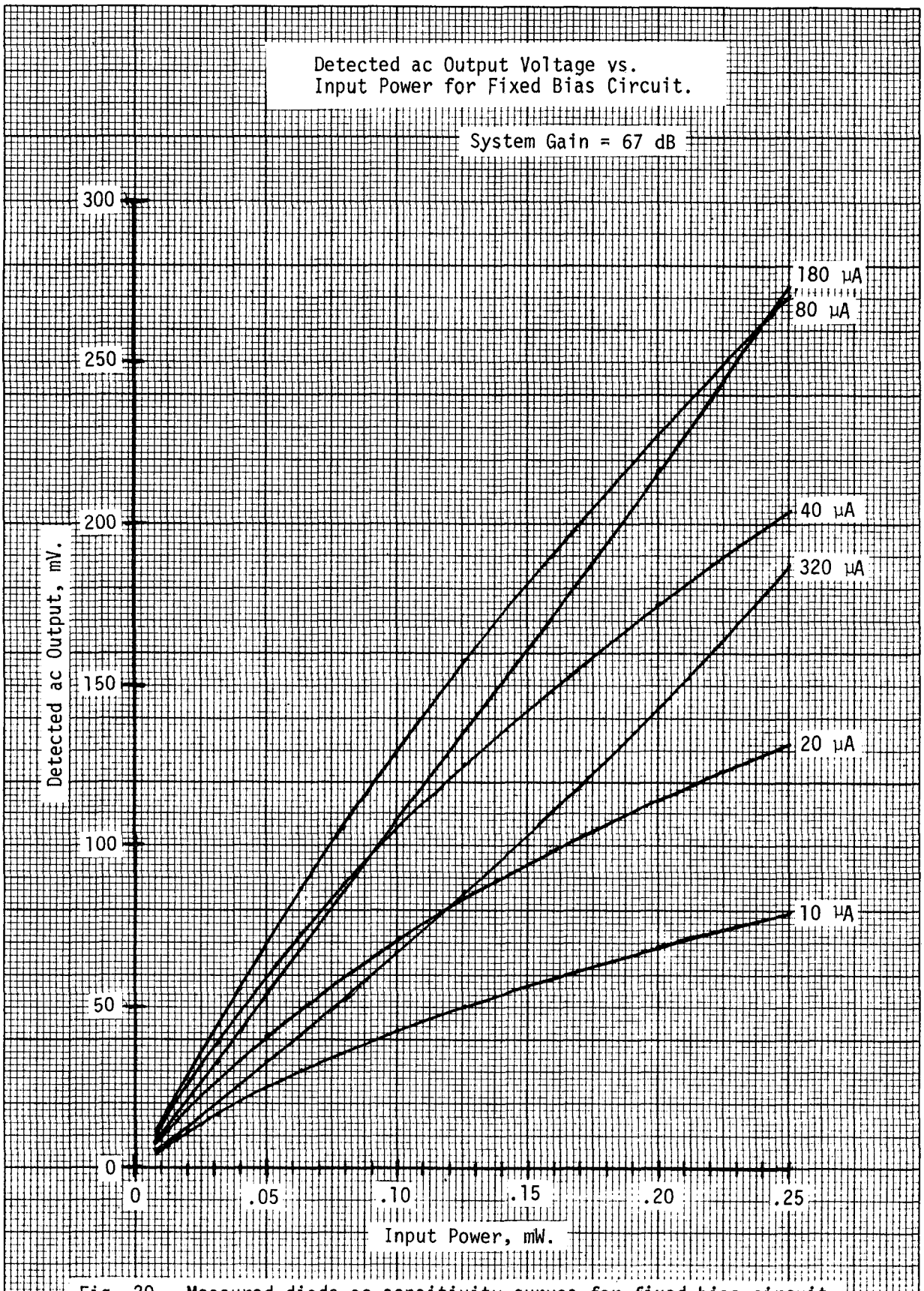


Fig. 20. Measured diode ac sensitivity curves for fixed bias circuit.

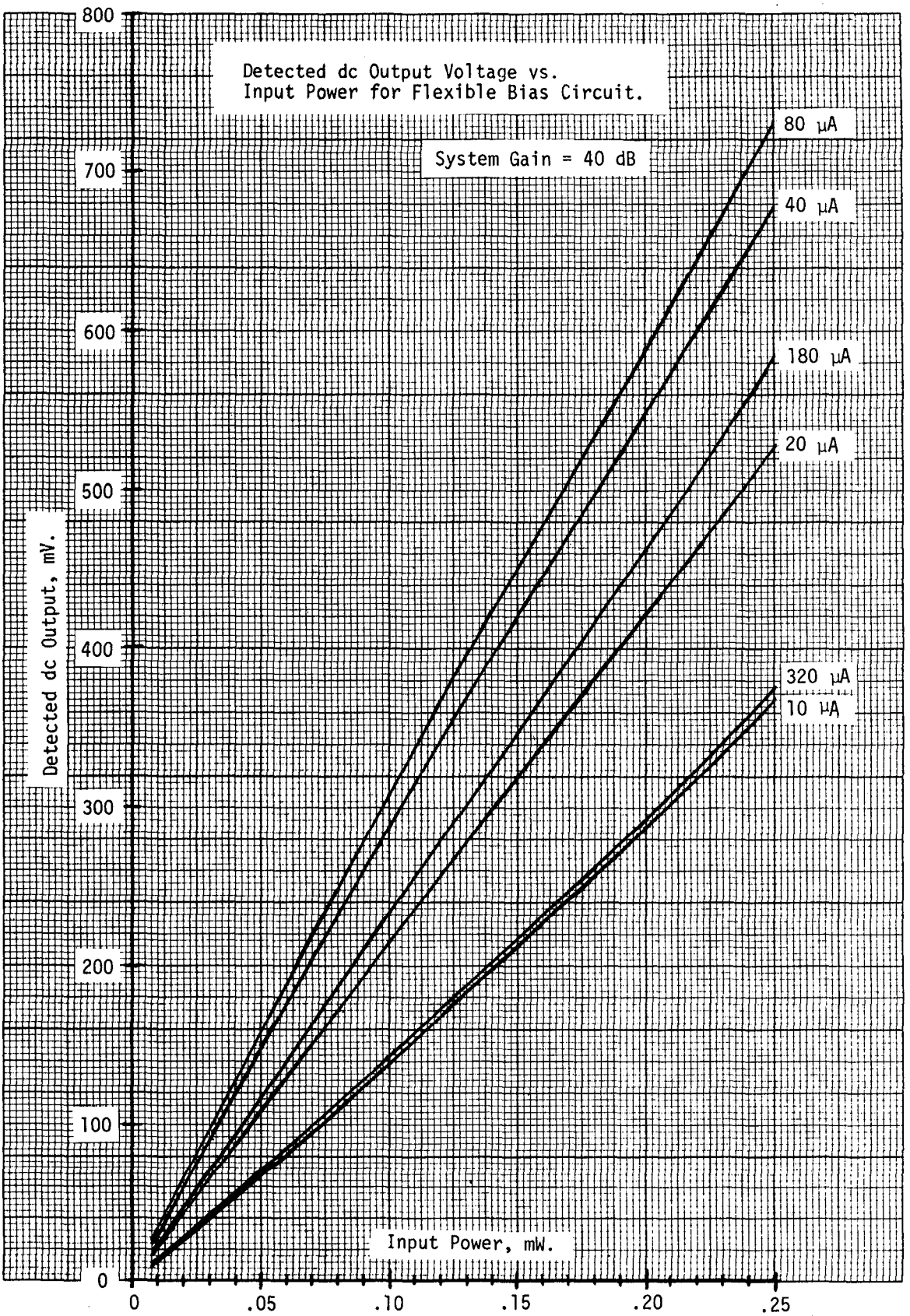


Fig. 21. Measured diode dc sensitivity curves for flexible bias circuit.

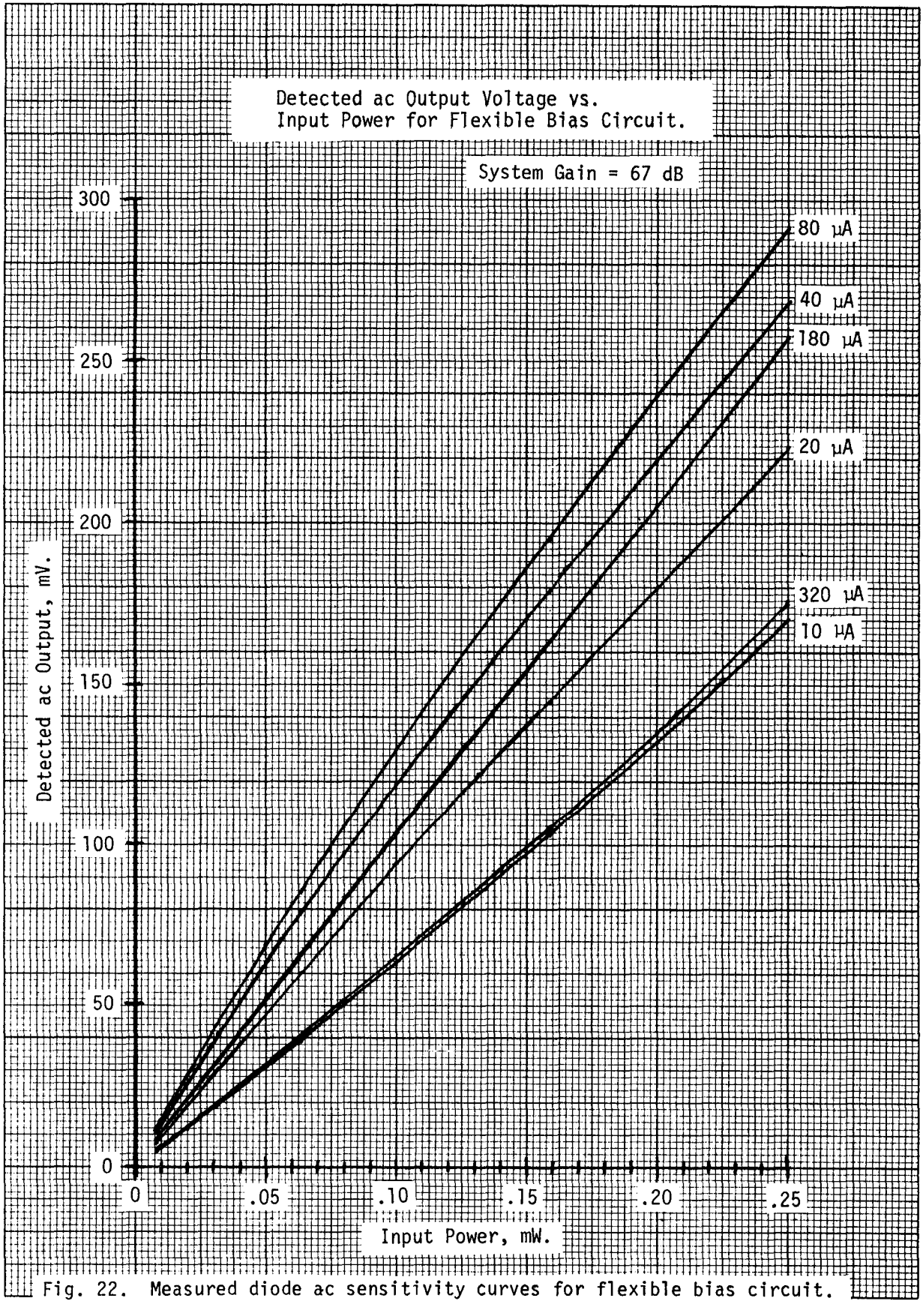


Fig. 22. Measured diode ac sensitivity curves for flexible bias circuit.

D.U.T.: Fixed-bias S.L.D. OPERATING CONDITIONS: BIAS = 10 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.3088	+.1111
-29	1.2553	0.0000	+0.0000	1.2694	+.0575
-28	1.2534	0.0000	+0.0000	1.2643	+.0446
-27	1.2647	0.0000	+0.0000	1.2750	+.0402
-26	1.2677	0.0000	+0.0000	1.2747	+.0268
-25	1.2396	0.0000	+0.0000	1.2429	+.0138
-24	1.2586	0.0000	+0.0000	1.2616	+.0118
-23	1.2595	0.0000	+0.0000	1.2623	+.0107
-22	1.2545	0.0000	+0.0000	1.2507	-.0149
-21	1.2548	0.0000	+0.0000	1.2514	-.0133
-20	1.2395	1.2386	-.0036	1.2313	-.0331
-19	1.2553	1.2528	-.0099	1.2471	-.0312
-18	1.2523	1.2483	-.0159	1.2410	-.0432
-17	1.2660	1.2600	-.0221	1.2464	-.0695
-16	1.2675	1.2610	-.0236	1.2434	-.0840
-15	1.2410	1.2310	-.0402	1.2140	-.1029
-14	1.2581	1.2475	-.0400	1.2250	-.1163
-13	1.2574	1.2467	-.0404	1.2209	-.1274
-12	1.2570	1.2357	-.0776	1.2049	-.1746
-11	1.2551	1.2315	-.0860	1.1967	-.1935
-10	1.2514	1.2245	-.0985	1.1860	-.2154
-9	1.2532	1.2228	-.1098	1.1802	-.2345
-8	1.2549	1.2158	-.1368	1.1674	-.2696
-7	1.2625	1.2176	-.1508	1.1641	-.2892
-6	1.2633	1.2132	-.1655	1.1573	-.3052

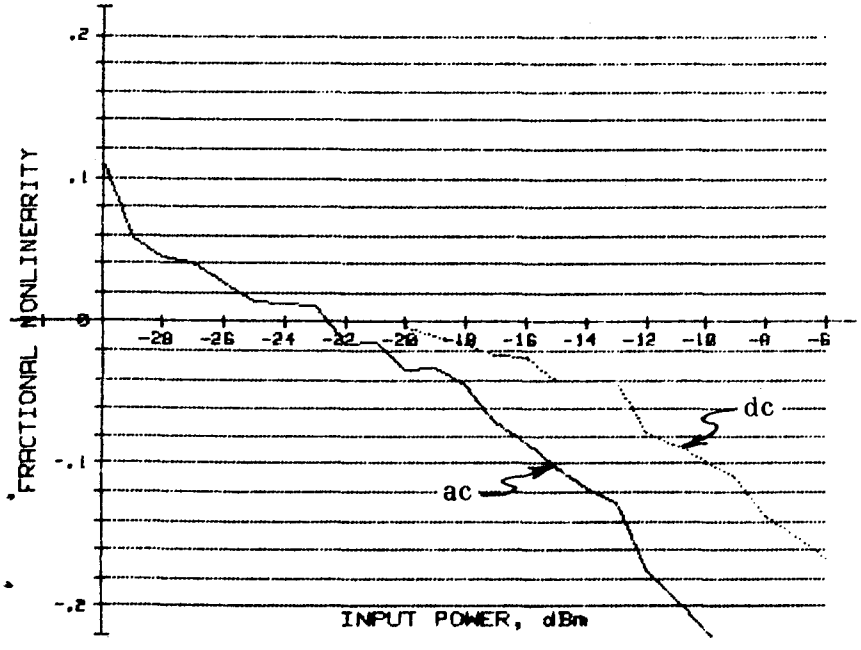


Figure 23. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Fixed-bias S.L.D. OPERATING CONDITIONS: BIAS = 20 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2951	+.0556
-29	1.2553	0.0000	+0.0000	1.2683	+.0528
-28	1.2534	0.0000	+0.0000	1.2628	+.0381
-27	1.2647	0.0000	+0.0000	1.2719	+.0278
-26	1.2677	0.0000	+0.0000	1.2702	+.0094
-25	1.2396	0.0000	+0.0000	1.2444	+.0204
-24	1.2586	0.0000	+0.0000	1.2566	-.0076
-23	1.2595	0.0000	+0.0000	1.2597	+.0005
-22	1.2545	0.0000	+0.0000	1.2507	-.0150
-21	1.2548	0.0000	+0.0000	1.2507	-.0160
-20	1.2395	1.2389	-.0024	1.2299	-.0385
-19	1.2553	1.2558	+.0018	1.2476	-.0297
-18	1.2523	1.2521	-.0009	1.2426	-.0376
-17	1.2660	1.2604	-.0208	1.2494	-.0596
-16	1.2675	1.2629	-.0168	1.2454	-.0773
-15	1.2410	1.2351	-.0241	1.2168	-.0932
-14	1.2581	1.2499	-.0312	1.2267	-.1110
-13	1.2574	1.2514	-.0231	1.2244	-.1166
-12	1.2570	1.2391	-.0661	1.2078	-.1661
-11	1.2551	1.2373	-.0661	1.2003	-.1835
-10	1.2514	1.2299	-.0801	1.1886	-.2082
-9	1.2532	1.2285	-.0907	1.1824	-.2287
-8	1.2549	1.2215	-.1186	1.1712	-.2601
-7	1.2625	1.2246	-.1298	1.1661	-.2847
-6	1.2633	1.2177	-.1524	1.1587	-.3024

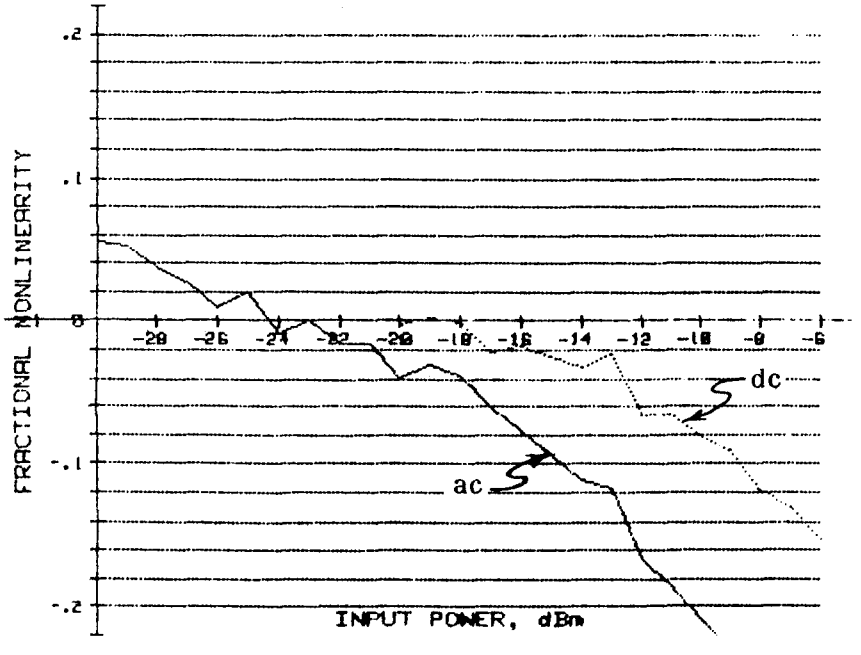


Figure 24. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Fixed-bias S.I.D. OPERATING CONDITIONS: BIAS = 40 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2881	+.0290
-29	1.2553	0.0000	+0.0000	1.2637	+.0334
-28	1.2534	0.0000	+0.0000	1.2589	+.0218
-27	1.2647	0.0000	+0.0000	1.2700	+.0205
-26	1.2677	0.0000	+0.0000	1.2719	+.0158
-25	1.2396	0.0000	+0.0000	1.2413	+.0073
-24	1.2586	0.0000	+0.0000	1.2585	-.0006
-23	1.2595	0.0000	+0.0000	1.2619	+.0091
-22	1.2545	0.0000	+0.0000	1.2514	-.0123
-21	1.2548	0.0000	+0.0000	1.2507	-.0160
-20	1.2395	1.2409	+.0061	1.2324	-.0289
-19	1.2553	1.2577	+.0093	1.2497	-.0217
-18	1.2523	1.2560	+.0146	1.2442	-.0312
-17	1.2660	1.2644	-.0060	1.2529	-.0472
-16	1.2675	1.2675	+.0001	1.2530	-.0519
-15	1.2410	1.2389	-.0088	1.2213	-.0767
-14	1.2581	1.2550	-.0121	1.2345	-.0854
-13	1.2574	1.2587	+.0049	1.2300	-.0983
-12	1.2570	1.2471	-.0372	1.2198	-.1297
-11	1.2551	1.2460	-.0348	1.2107	-.1529
-10	1.2514	1.2392	-.0466	1.1975	-.1829
-9	1.2532	1.2401	-.0497	1.1934	-.1987
-8	1.2549	1.2332	-.0798	1.1794	-.2396
-7	1.2625	1.2360	-.0936	1.1758	-.2618
-6	1.2633	1.2328	-.1063	1.1650	-.2881

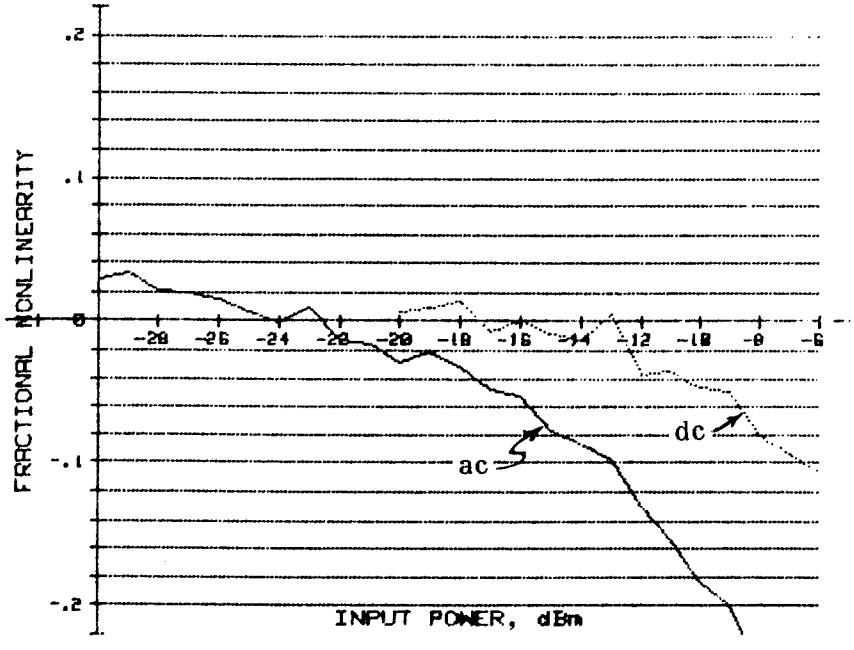


Figure 25. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Fixed-bias S.L.D. OPERATING CONDITIONS: BIAS = 80 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2853	+.0186
-29	1.2553	0.0000	+0.0000	1.2608	+.0217
-28	1.2534	0.0000	+0.0000	1.2594	+.0241
-27	1.2647	0.0000	+0.0000	1.2674	+.0104
-26	1.2677	0.0000	+0.0000	1.2713	+.0138
-25	1.2396	0.0000	+0.0000	1.2442	+.0195
-24	1.2586	0.0000	+0.0000	1.2610	+.0091
-23	1.2595	0.0000	+0.0000	1.2645	+.0194
-22	1.2545	0.0000	+0.0000	1.2547	+.0008
-21	1.2548	0.0000	+0.0000	1.2546	-.0008
-20	1.2395	1.2362	-.0134	1.2385	-.0038
-19	1.2553	1.2606	+.0212	1.2548	-.0019
-18	1.2523	1.2545	+.0088	1.2511	-.0049
-17	1.2660	1.2718	+.0224	1.2605	-.0202
-16	1.2675	1.2726	+.0195	1.2616	-.0217
-15	1.2410	1.2434	+.0099	1.2335	-.0303
-14	1.2581	1.2643	+.0243	1.2487	-.0354
-13	1.2574	1.2668	+.0376	1.2481	-.0351
-12	1.2570	1.2569	-.0004	1.2359	-.0771
-11	1.2551	1.2580	+.0116	1.2309	-.0880
-10	1.2514	1.2552	+.0154	1.2218	-.1077
-9	1.2532	1.2582	+.0201	1.2159	-.1319
-8	1.2549	1.2525	-.0094	1.2038	-.1728
-7	1.2625	1.2577	-.0184	1.1996	-.2015
-6	1.2633	1.2563	-.0259	1.1889	-.2309

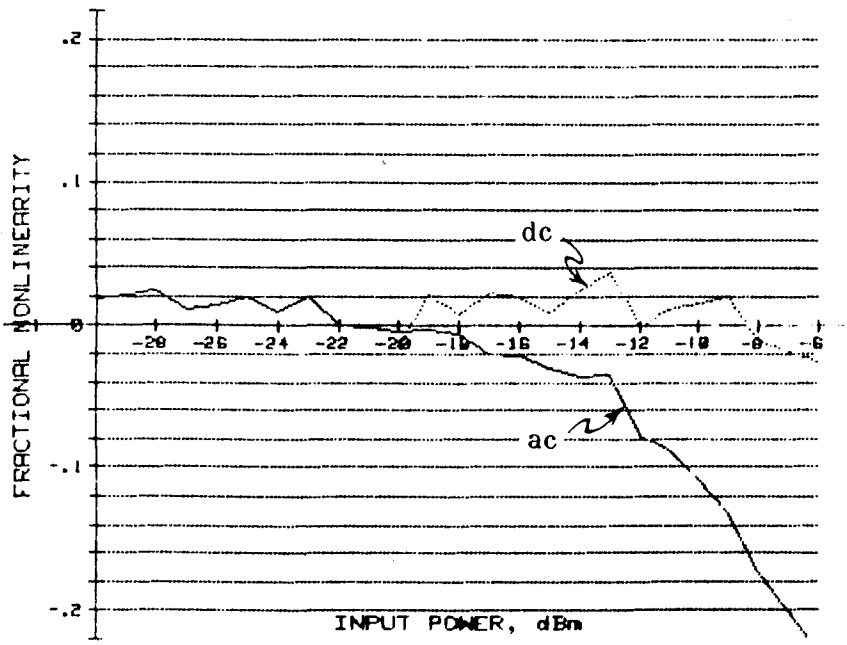


Figure 26. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Fixed-bias S.L.D. OPERATING CONDITIONS: BIAS = 180 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2945	+.0531
-29	1.2553	0.0000	+0.0000	1.2579	+.0102
-28	1.2534	0.0000	+0.0000	1.2576	+.0166
-27	1.2647	0.0000	+0.0000	1.2706	+.0228
-26	1.2677	0.0000	+0.0000	1.2725	+.0181
-25	1.2396	0.0000	+0.0000	1.2426	+.0126
-24	1.2586	0.0000	+0.0000	1.2609	+.0090
-23	1.2595	0.0000	+0.0000	1.2664	+.0270
-22	1.2545	0.0000	+0.0000	1.2565	+.0077
-21	1.2548	0.0000	+0.0000	1.2589	+.0163
-20	1.2395	1.2442	+.0203	1.2418	+.0097
-19	1.2553	1.2552	-.0006	1.2605	+.0206
-18	1.2523	1.2650	+.0523	1.2592	+.0277
-17	1.2660	1.2582	-.0284	1.2695	+.0134
-16	1.2675	1.2740	+.0250	1.2733	+.0222
-15	1.2410	1.2519	+.0469	1.2459	+.0205
-14	1.2581	1.2669	+.0352	1.2665	+.0333
-13	1.2574	1.2739	+.0674	1.2703	+.0522
-12	1.2570	1.2668	+.0392	1.2617	+.0186
-11	1.2551	1.2705	+.0635	1.2627	+.0304
-10	1.2514	1.2701	+.0791	1.2625	+.0457
-9	1.2532	1.2782	+.1071	1.2630	+.0399
-8	1.2549	1.2777	+.0965	1.2566	+.0067
-7	1.2625	1.2913	+.1199	1.2660	+.0131
-6	1.2633	1.2978	+.1460	1.2539	-.0347

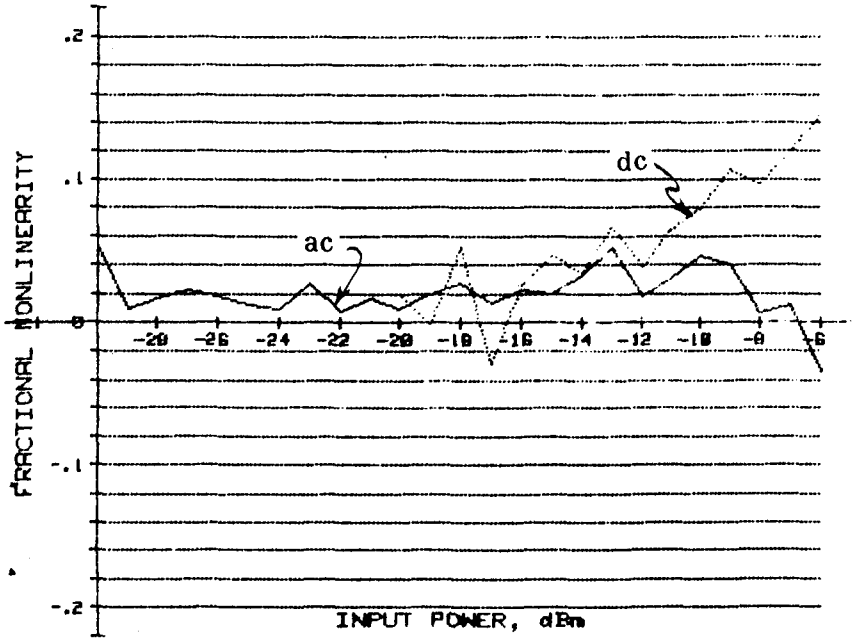


Figure 27. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Fixed-bias S.L.D. OPERATING CONDITIONS: BIAS = 320 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2905	+.0381
-29	1.2553	0.0000	+0.0000	1.2689	+.0553
-28	1.2534	0.0000	+0.0000	1.2565	+.0124
-27	1.2647	0.0000	+0.0000	1.2728	+.0316
-26	1.2677	0.0000	+0.0000	1.2798	+.0468
-25	1.2396	0.0000	+0.0000	1.2462	+.0281
-24	1.2586	0.0000	+0.0000	1.2641	+.0215
-23	1.2595	0.0000	+0.0000	1.2666	+.0277
-22	1.2545	0.0000	+0.0000	1.2576	+.0122
-21	1.2548	0.0000	+0.0000	1.2605	+.0227
-20	1.2395	1.2303	-.0369	1.2417	+.0096
-19	1.2553	1.2603	+.0197	1.2613	+.0239
-18	1.2523	1.2645	+.0502	1.2591	+.0273
-17	1.2660	1.2808	+.0583	1.2701	+.0158
-16	1.2675	1.2617	-.0210	1.2755	+.0310
-15	1.2410	1.2518	+.0462	1.2548	+.0600
-14	1.2581	1.2635	+.0210	1.2660	+.0312
-13	1.2574	1.2702	+.0515	1.2756	+.0747
-12	1.2570	1.2674	+.0421	1.2681	+.0447
-11	1.2551	1.2709	+.0652	1.2722	+.0711
-10	1.2514	1.2685	+.0719	1.2715	+.0855
-9	1.2532	1.2778	+.1050	1.2824	+.1269
-8	1.2549	1.2809	+.1113	1.2841	+.1263
-7	1.2625	1.2953	+.1386	1.3013	+.1671
-6	1.2633	1.3103	+.2078	1.3096	+.2043

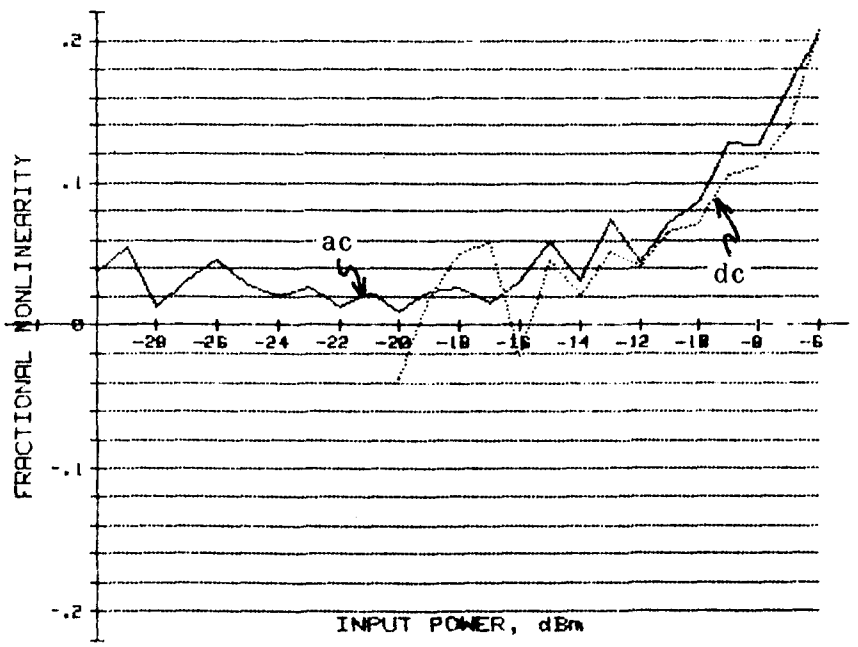


Figure 28. Fractional nonlinearity vs. input level, fixed-bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 10 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.3026	+.0855
-29	1.2553	0.0000	+0.0000	1.2723	+.0703
-28	1.2534	0.0000	+0.0000	1.2687	+.0635
-27	1.2647	0.0000	+0.0000	1.2871	+.0909
-26	1.2677	0.0000	+0.0000	1.2742	+.0249
-25	1.2396	0.0000	+0.0000	1.2507	+.0481
-24	1.2586	0.0000	+0.0000	1.2620	+.0132
-23	1.2595	0.0000	+0.0000	1.2685	+.0355
-22	1.2545	0.0000	+0.0000	1.2616	+.0283
-21	1.2548	0.0000	+0.0000	1.2602	+.0216
-20	1.2395	0.0000	+0.0000	1.2456	+.0261
-19	1.2553	0.0000	+0.0000	1.2635	+.0329
-18	1.2523	0.0000	+0.0000	1.2590	+.0270
-17	1.2660	0.0000	+0.0000	1.2726	+.0254
-16	1.2675	0.0000	+0.0000	1.2780	+.0407
-15	1.2410	0.0000	+0.0000	1.2510	+.0429
-14	1.2581	0.0000	+0.0000	1.2730	+.0604
-13	1.2574	0.0000	+0.0000	1.2734	+.0650
-12	1.2570	0.0000	+0.0000	1.2731	+.0661
-11	1.2551	0.0000	+0.0000	1.2732	+.0754
-10	1.2514	0.0000	+0.0000	1.2729	+.0916
-9	1.2532	0.0000	+0.0000	1.2768	+.1006
-8	1.2549	0.0000	+0.0000	1.2753	+.0857
-7	1.2625	0.0000	+0.0000	1.2832	+.0840
-6	1.2633	0.0000	+0.0000	1.2713	+.0312

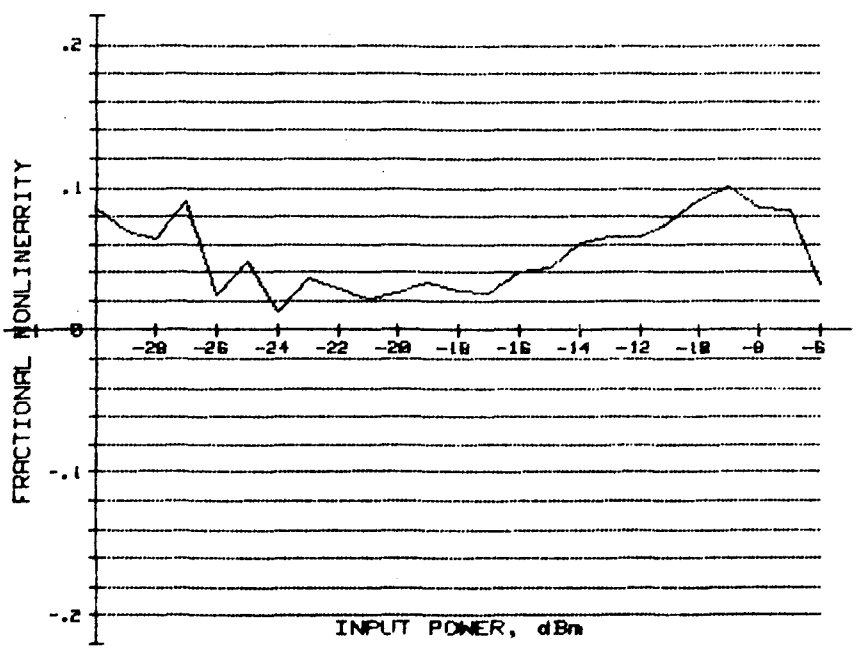


Figure 29. Fractional nonlinearity vs. input level, flexible bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 20 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.3014	+.0805
-29	1.2553	0.0000	+0.0000	1.2601	+.0187
-28	1.2534	0.0000	+0.0000	1.2617	+.0337
-27	1.2647	0.0000	+0.0000	1.2704	+.0221
-26	1.2677	0.0000	+0.0000	1.2731	+.0204
-25	1.2396	0.0000	+0.0000	1.2467	+.0305
-24	1.2586	0.0000	+0.0000	1.2612	+.0101
-23	1.2595	0.0000	+0.0000	1.2658	+.0246
-22	1.2545	0.0000	+0.0000	1.2546	+.0003
-21	1.2548	0.0000	+0.0000	1.2563	+.0058
-20	1.2395	0.0000	+0.0000	1.2407	+.0052
-19	1.2553	0.0000	+0.0000	1.2571	+.0070
-18	1.2523	0.0000	+0.0000	1.2548	+.0098
-17	1.2660	0.0000	+0.0000	1.2655	-.0019
-16	1.2675	0.0000	+0.0000	1.2686	+.0043
-15	1.2410	0.0000	+0.0000	1.2414	+.0016
-14	1.2581	0.0000	+0.0000	1.2472	-.0410
-13	1.2574	0.0000	+0.0000	1.2603	+.0110
-12	1.2570	0.0000	+0.0000	1.2510	-.0229
-11	1.2551	0.0000	+0.0000	1.2500	-.0196
-10	1.2514	0.0000	+0.0000	1.2451	-.0246
-9	1.2532	0.0000	+0.0000	1.2474	-.0225
-8	1.2549	0.0000	+0.0000	1.2391	-.0591
-7	1.2625	0.0000	+0.0000	1.2462	-.0594
-6	1.2633	0.0000	+0.0000	1.2417	-.0772

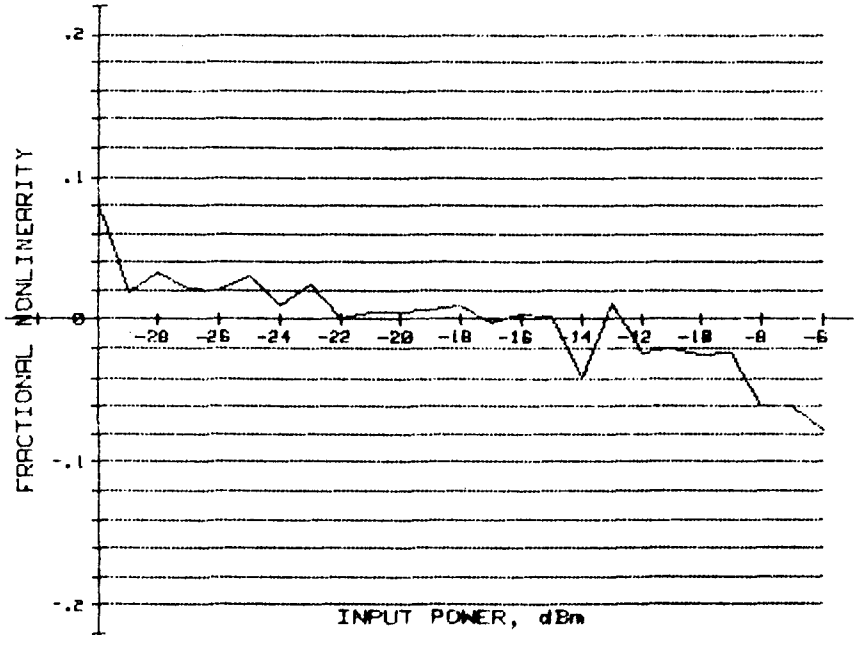


Figure 30. Fractional nonlinearity vs. input level, flexible bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 40 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2940	+.0515
-29	1.2553	0.0000	+0.0000	1.2615	+.0244
-28	1.2534	0.0000	+0.0000	1.2594	+.0238
-27	1.2647	0.0000	+0.0000	1.2687	+.0155
-26	1.2677	0.0000	+0.0000	1.2692	+.0057
-25	1.2396	0.0000	+0.0000	1.2451	+.0232
-24	1.2586	0.0000	+0.0000	1.2590	+.0015
-23	1.2595	0.0000	+0.0000	1.2637	+.0163
-22	1.2545	0.0000	+0.0000	1.2553	+.0032
-21	1.2548	0.0000	+0.0000	1.2557	+.0036
-20	1.2395	0.0000	+0.0000	1.2371	-.0096
-19	1.2553	0.0000	+0.0000	1.2552	-.0005
-18	1.2523	0.0000	+0.0000	1.2496	-.0105
-17	1.2660	0.0000	+0.0000	1.2598	-.0227
-16	1.2675	0.0000	+0.0000	1.2603	-.0264
-15	1.2410	0.0000	+0.0000	1.2322	-.0357
-14	1.2581	0.0000	+0.0000	1.2476	-.0393
-13	1.2574	0.0000	+0.0000	1.2524	-.0191
-12	1.2570	0.0000	+0.0000	1.2337	-.0846
-11	1.2551	0.0000	+0.0000	1.2354	-.0725
-10	1.2514	0.0000	+0.0000	1.2296	-.0812
-9	1.2532	0.0000	+0.0000	1.2256	-.1004
-8	1.2549	0.0000	+0.0000	1.2192	-.1260
-7	1.2625	0.0000	+0.0000	1.2254	-.1271
-6	1.2633	0.0000	+0.0000	1.2202	-.1451

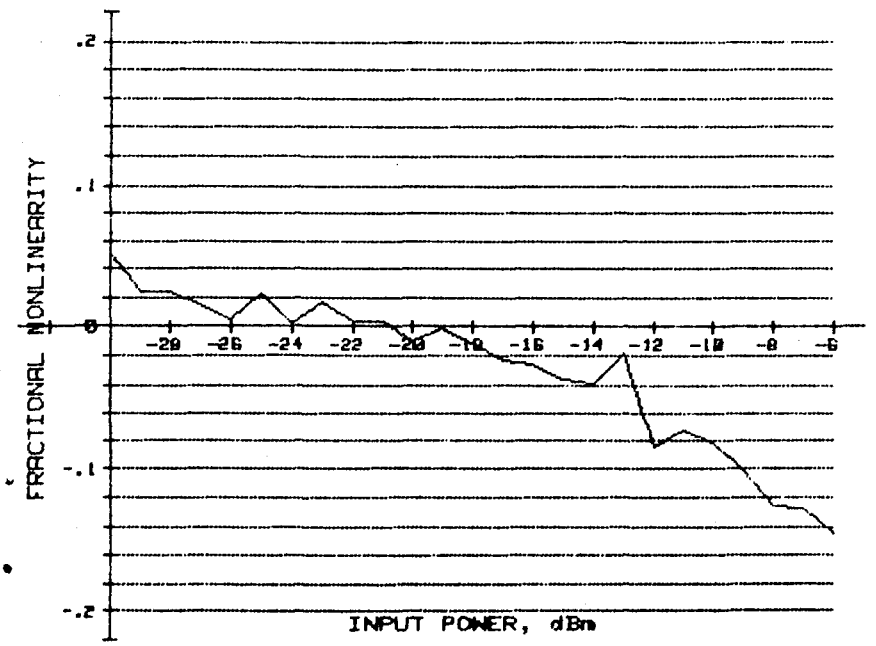


Figure 31. Fractional nonlinearity vs. input level, flexible bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 80 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2918	+.0430
-29	1.2553	0.0000	+0.0000	1.2594	+.0161
-28	1.2534	0.0000	+0.0000	1.2479	-.0214
-27	1.2647	0.0000	+0.0000	1.2654	+.0026
-26	1.2677	0.0000	+0.0000	1.2684	+.0027
-25	1.2396	0.0000	+0.0000	1.2455	+.0252
-24	1.2586	0.0000	+0.0000	1.2615	+.0114
-23	1.2595	0.0000	+0.0000	1.2591	-.0017
-22	1.2545	0.0000	+0.0000	1.2556	+.0043
-21	1.2548	0.0000	+0.0000	1.2538	-.0041
-20	1.2395	0.0000	+0.0000	1.2386	-.0036
-19	1.2553	0.0000	+0.0000	1.2545	-.0031
-18	1.2523	0.0000	+0.0000	1.2520	-.0014
-17	1.2660	0.0000	+0.0000	1.2613	-.0172
-16	1.2675	0.0000	+0.0000	1.2638	-.0135
-15	1.2410	0.0000	+0.0000	1.2343	-.0272
-14	1.2581	0.0000	+0.0000	1.2493	-.0333
-13	1.2574	0.0000	+0.0000	1.2497	-.0294
-12	1.2570	0.0000	+0.0000	1.2390	-.0661
-11	1.2551	0.0000	+0.0000	1.2370	-.0670
-10	1.2514	0.0000	+0.0000	1.2289	-.0836
-9	1.2532	0.0000	+0.0000	1.2296	-.0869
-8	1.2549	0.0000	+0.0000	1.2210	-.1201
-7	1.2625	0.0000	+0.0000	1.2239	-.1318
-6	1.2633	0.0000	+0.0000	1.2176	-.1527

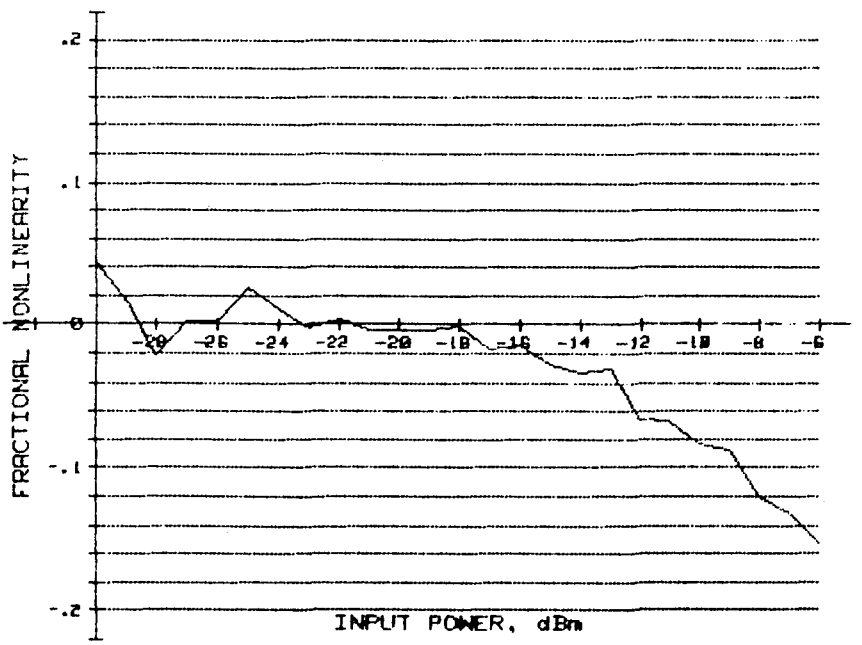


Figure 32. Fractional nonlinearity vs. input level, flexible bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 180 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2890	+.0321
-29	1.2553	0.0000	+0.0000	1.2649	+.0386
-28	1.2534	0.0000	+0.0000	1.2583	+.0195
-27	1.2647	0.0000	+0.0000	1.2692	+.0174
-26	1.2677	0.0000	+0.0000	1.2698	+.0077
-25	1.2396	0.0000	+0.0000	1.2412	+.0069
-24	1.2586	0.0000	+0.0000	1.2613	+.0104
-23	1.2595	0.0000	+0.0000	1.2681	+.0340
-22	1.2545	0.0000	+0.0000	1.2575	+.0118
-21	1.2548	0.0000	+0.0000	1.2585	+.0149
-20	1.2395	0.0000	+0.0000	1.2414	+.0083
-19	1.2553	0.0000	+0.0000	1.2587	+.0135
-18	1.2523	0.0000	+0.0000	1.2560	+.0146
-17	1.2660	0.0000	+0.0000	1.2652	-.0028
-16	1.2675	0.0000	+0.0000	1.2707	+.0121
-15	1.2410	0.0000	+0.0000	1.2429	+.0076
-14	1.2581	0.0000	+0.0000	1.2617	+.0141
-13	1.2574	0.0000	+0.0000	1.2646	+.0282
-12	1.2570	0.0000	+0.0000	1.2561	-.0035
-11	1.2551	0.0000	+0.0000	1.2576	+.0100
-10	1.2514	0.0000	+0.0000	1.2540	+.0103
-9	1.2532	0.0000	+0.0000	1.2563	+.0121
-8	1.2549	0.0000	+0.0000	1.2539	-.0040
-7	1.2625	0.0000	+0.0000	1.2568	-.0215
-6	1.2633	0.0000	+0.0000	1.2542	-.0336

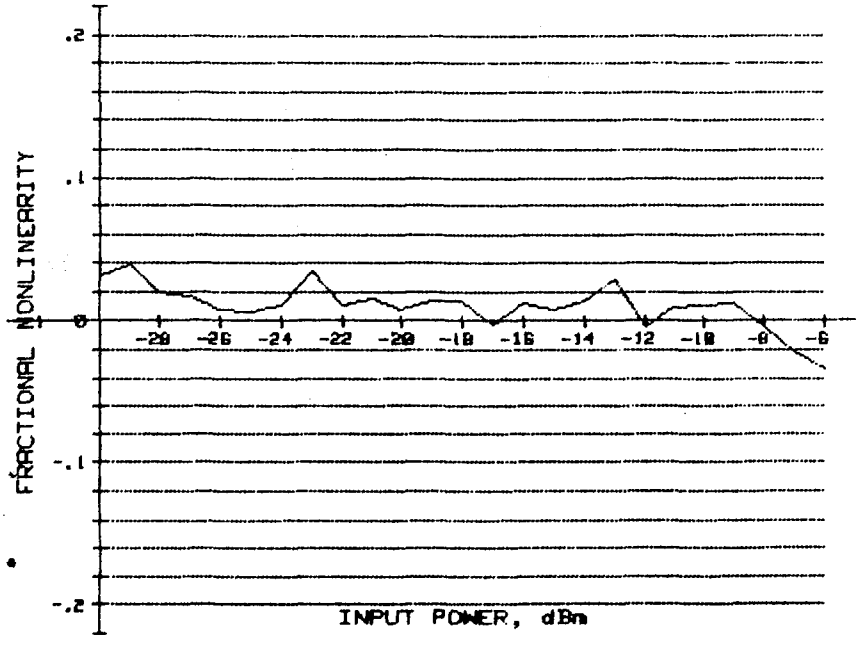


Figure 33. Fractional nonlinearity vs. input level, flexible bias configuration.

D.U.T.: Flexible-bias S.L.D. OPERATING CONDITIONS: BIAS = 320 Microamperes

INPUT LEVEL, dBm	INPUT POWER RATIO	DC OUTPUT VOLTAGE RATIO	DC FRACTIONAL NONLINEARITY	AC OUTPUT VOLTAGE RATIO	AC FRACTIONAL NONLINEARITY
-30	1.2802	0.0000	+0.0000	1.2861	+.0215
-29	1.2553	0.0000	+0.0000	1.2662	+.0439
-28	1.2534	0.0000	+0.0000	1.2629	+.0383
-27	1.2647	0.0000	+0.0000	1.2688	+.0157
-26	1.2677	0.0000	+0.0000	1.2638	-.0143
-25	1.2396	0.0000	+0.0000	1.2458	+.0263
-24	1.2586	0.0000	+0.0000	1.2614	+.0107
-23	1.2595	0.0000	+0.0000	1.2652	+.0224
-22	1.2545	0.0000	+0.0000	1.2588	+.0172
-21	1.2548	0.0000	+0.0000	1.2592	+.0175
-20	1.2395	0.0000	+0.0000	1.2418	+.0100
-19	1.2553	0.0000	+0.0000	1.2590	+.0146
-18	1.2523	0.0000	+0.0000	1.2549	+.0101
-17	1.2660	0.0000	+0.0000	1.2695	+.0135
-16	1.2675	0.0000	+0.0000	1.2711	+.0137
-15	1.2410	0.0000	+0.0000	1.2471	+.0257
-14	1.2581	0.0000	+0.0000	1.2675	+.0373
-13	1.2574	0.0000	+0.0000	1.2715	+.0572
-12	1.2570	0.0000	+0.0000	1.2623	+.0211
-11	1.2551	0.0000	+0.0000	1.2662	+.0452
-10	1.2514	0.0000	+0.0000	1.2669	+.0646
-9	1.2532	0.0000	+0.0000	1.2713	+.0758
-8	1.2549	0.0000	+0.0000	1.2701	+.0628
-7	1.2625	0.0000	+0.0000	1.2866	+.0990
-6	1.2633	0.0000	+0.0000	1.2913	+.1159

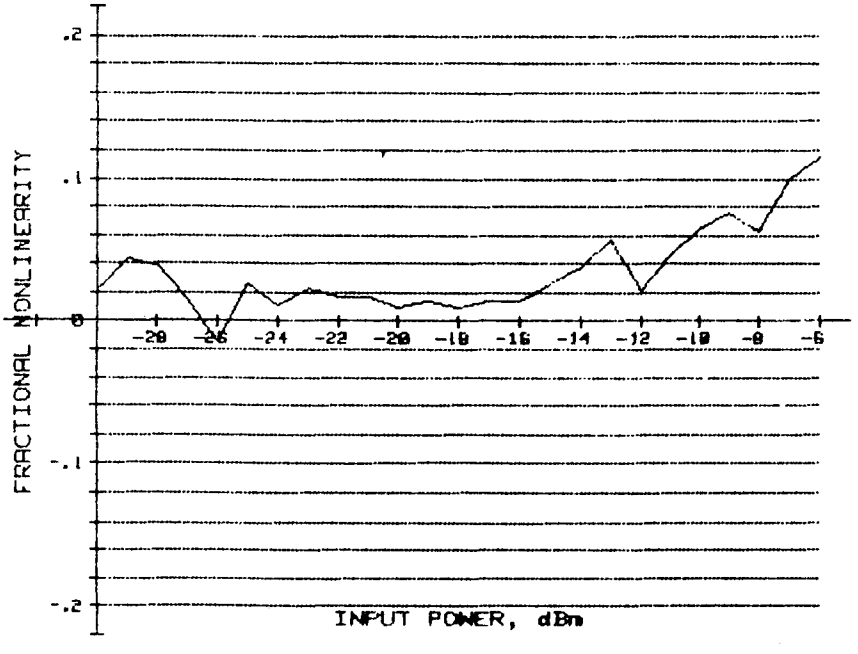


Figure 34. Fractional nonlinearity vs. input level, flexible bias configuration.

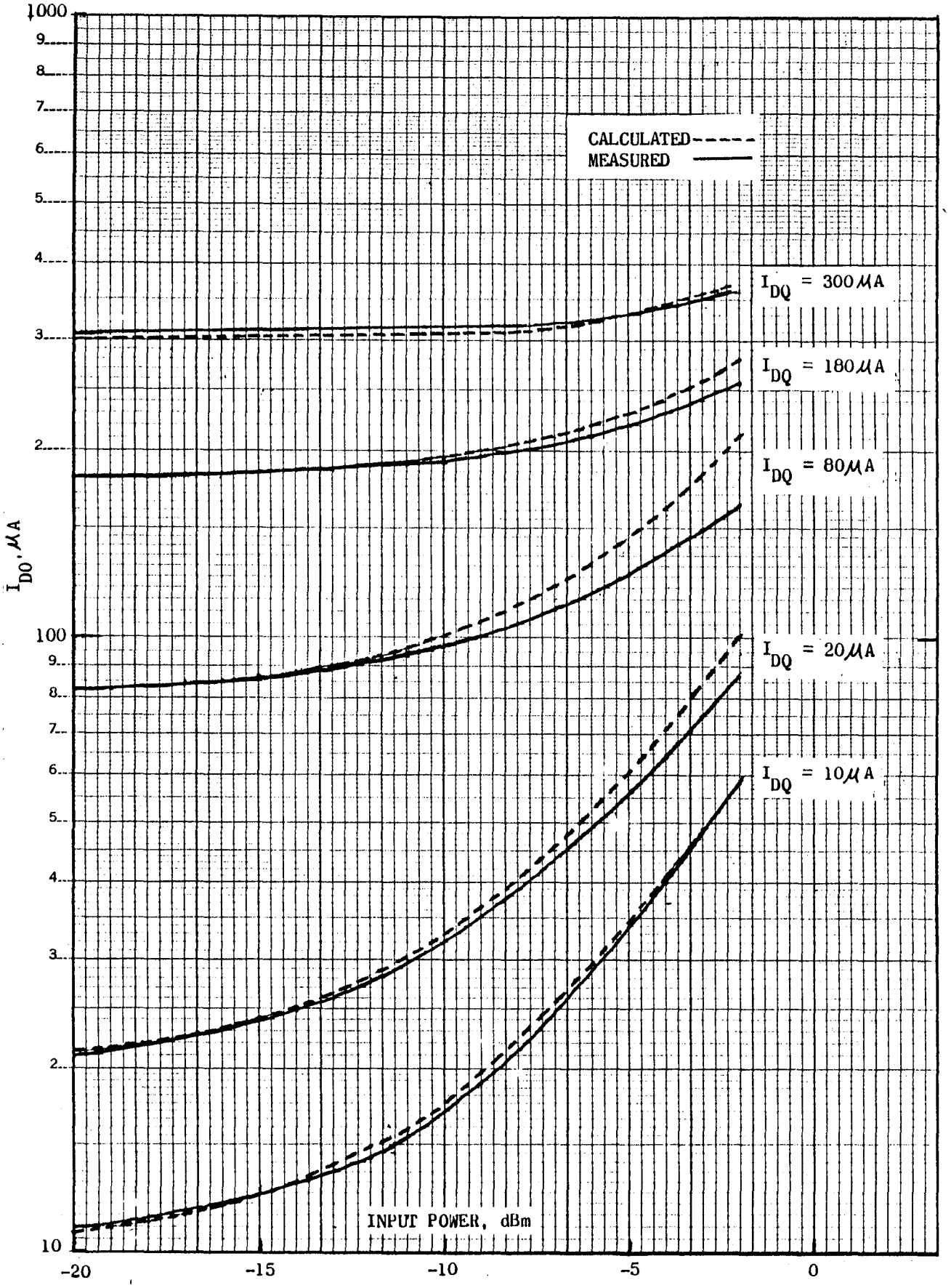


Fig 35. Calculated and measured bias shift for flexible bias circuit.

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA TM-86307		

4. Title and Subtitle	5. Report Date
THEORETICAL AND EXPERIMENTAL STUDIES OF ERROR IN SQUARE-LAW DETECTOR CIRCUITS	September 1984
	6. Performing Organization Code 506-54-23-10

7. Author(s)	8. Performing Organization Report No.
William D. Stanley, Chase P. Hearn, and James B. Williams	
	10. Work Unit No.
9. Performing Organization Name and Address	
NASA Langley Research Center Hampton, VA 23665	11. Contract or Grant No.
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Technical Memorandum
National Aeronautics and Space Administration Washington, DC 20546	14. Sponsoring Agency Code

15. Supplementary Notes

William B. Stanley: Old Dominion University, Norfolk, Virginia.
Chase P. Hearn and James B. Williams: Langley Research Center, Hampton, Virginia.

16. Abstract

Square-law detector circuits are investigated to determine errors from the ideal input-output characteristic function. The nonlinear circuit response is analyzed by means of a power series expansion containing terms through the fourth degree, from which the significant deviation from square-law can be predicted. Both fixed bias current and "flexible bias" current configurations are considered. The latter case corresponds to the situation where the mean current can change with the application of a signal. Experimental investigations of the circuit arrangements are described. Substantial agreement between the analytical models and the experimental results were established in most tests. Factors contributing to differences under certain conditions are explained.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Square-law detection	Unclassified - Unlimited Subject Category 33

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	74	A04

For sale by the National Technical Information Service, Springfield, Virginia 22161