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4-9-T-10-F

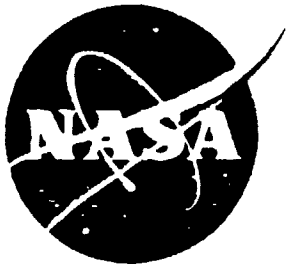
30 GHz Solid State Amplifier for Low Cost Low Data Rate Ground Terminals

Final Report
September 1984

By

Y. C. Ngan and M. A. Quijije

TRW Electronic Systems Group
One Space Park
Redondo Beach, California 90278



Prepared for

National Aeronautics and Space Administration
Lewis Research Center
21000 Brookpark Road
Cleveland, Ohio 44135

Contract No. NAS3-23266

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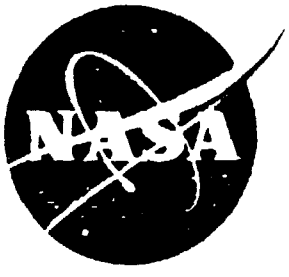

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1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
4-9-T-10-F		

4. Title and Subtitle	5. Report Date
30 GHz Solid State Amplifier for Low Cost Low Data Rate Ground Terminals	September 1984
	6. Performing Organization Code
7. Author(s)	8. Performing Organization Report No.
Y. C. Ngan and M. A. Quijije	
	10. Work Unit No.
9. Performing Organization Name and Address	11. Contract or Grant No.
TRW Electronic Systems Group One Space Park Redondo Beach, California 90278	NAS3-23266
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Final, 6/82 - 6/84
NASA Lewis Research Center 21000 Brookpark Road Cleveland, Ohio 44135	14. Sponsoring Agency Code

15. Supplementary Notes

Project Manager, D. Pope
NASA-Lewis Research Center
21000 Brookpark Road, Cleveland, OH 44135

16. Abstract

This report details the development of a 20-W solid state amplifier operating near 30 GHz. The performance represents a significant advance in the state-of-the-art in both device and circuit technology in Ka-band frequencies. The development effort involved a variety of disciplines including IMPATT device developments, circulator development, single and multiple diode circuit development, pulse modulator development, and amplifier integration and test.

The result of this effort is the development of an IMPATT amplifier which not only met or exceeded all the program objectives, but also possesses the ability to operate in the pulse mode, which was not called for in the original contract requirements. The ability to operate in the pulse mode is essential for TDMA (Time Domain Multiple Access) operation. An output power of 20 W was achieved with a 1-dB instantaneous bandwidth of 260 MHz. The amplifier has also been tested in pulse mode with 50% duty for pulse lengths ranging from 200 ns to 2 μs with 10 ns rise and fall times and no degradation in output power. This pulse mode operation was made possible by the development of a stable 12-diode power combiner/amplifier and a single-diode pulsed driver whose rf output power was switched on and off by having its bias current modulated via a fast-switching current pulse modulator. Essential to the overall amplifier development was the successful development of state-of-the-art silicon double-drift IMPATT diodes capable of reproducible, 2.5 W CW output power with 12% DC-to-rf conversion efficiency. Output powers of as high as 2.75 W has been observed. Both the device and circuit design are amenable to low cost production.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
IMPATT Diode, Kurokawa Combiner, Circulator Injection-Locked Oscillator, Stable Amplifier, TDMA, Burst Mode	Unclassified - Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified		

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FOREWORD

The work and effort described in this report was the result of a program initiated by NASA/Lewis Research Center (LeRC). Mr. D. Pope was the program manager for NASA.

The work was performed by TRW under NASA Contract NAS3-23266 for a program duration from May 1982 to June 1984. The program was under the technical direction of Dr. Y.C. Ngan. The program team consisted of Mr. M. Quijije and Mrs. C. T. Shih, who were responsible for circuit development and amplifier integration and test; and Dr. Y. Saito, Mrs. R. Dia, and Mr. K. Kurisu, who respectively were responsible for IMPATT diode material growth, processing and packaging. Special thanks are extended to Mr. W. E. Holmes and Mr M. Mlinar for significant contribution to the development of pulse modulator and multidiode stable amplifier. The authors would also like to thank Dr. T. T. Fong and Dr. C. Sun for support and encouragement.

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1. INTRODUCTION

This report details the development of a 20-W solid state amplifier operating near 30 GHz. The performance represents a significant advance in the state-of-the-art in both device and circuit technology in Ka-band frequencies. The development effort involved a variety of disciplines including IMPATT device developments, circulator development, single and multiple diode circuit development, pulse modulator development, and amplifier integration and test.

The amplifier development program is one part of a larger effort for the development of a millimeter-wave satellite communication system. Present studies of the growth in communication traffic indicate that the frequency spectrum allocated to fixed service satellites at C-and Ka-bands will reach saturation by the early 1990's. Ka-band with uplink at 27.5 - 30.0 GHz and downlink at 17.7 - 20.2 GHz is the next higher frequency band allocated for this purpose. Current plans for development of a satellite system to implement this band include the possibility of a NASA demonstration satellite in the late 1980's. To fully realize the benefit of the 30/20 GHz technology, one of the major considerations is the implementation of a high power solid state amplifier suitable for use in low cost low data rate ground terminals.

The result of this effort is the development of an IMPATT amplifier which not only met or exceeded all the program objectives, but also possesses the ability to operate in the pulse mode, which was not called for in the original contract requirements. The ability to operate in the pulse mode is essential for TDMA (Time Domain Multiple Access) operation. An output power of 20 W was achieved with a 1-dB instantaneous bandwidth of 260 MHz. The amplifier has also been tested in pulse mode with 50% duty for pulse lengths ranging from 200 ns to 2 μs with 10 ns rise and fall times and no degradation in output power. This pulse mode operation was made possible by the development of a stable 12-diode power combiner/amplifier and a single-diode

whose rf output power was switched on and off by having its bias current modulated via a fast-switching current pulse modulator. Essential to the overall amplifier development was the successful development of state-of-the-art silicon double-drift IMPATT diodes capable of reproducible 2.5 W CW output power with 12% DC-to-rf conversion efficiency. Output powers of as high as 2.75 W has been observed. Both the device and circuit design are amenable to low cost production.

This final report is organized as follows. Section 2 describes the program objectives, specifications and requirements. Section 3 contains a detailed description of the entire transmitter amplifier. The section discusses the various design approaches and tradeoffs which led to the final amplifier configuration. Section 4 presents the design methodology, fabrication and performance of IMPATT diodes developed in this program. Section 5 contains discussions on circuit development which include the IMPATT driver, the 12-diode power combiner, low loss circulators, and power conditioning circuitry. Section 6 discusses system integration. The physical description and the interface requirements of the amplifier are given in this section. Section 7 presents the measurement data and compares them with the rf requirements. Section 8 discusses the overall achievement of the program, the implications of the results, and the assessment of the future development needs. In addition to these main sections, we have also included three appendices. Appendix A is a compilation of mechanical drawings for the POC hardware. Appendix B is a reprint of Task X Report entitled "Technology Assessment" which outlines performance projections within the next three years and recommended development efforts. Appendix C is a reprint of Task VIII Report entitled "Requirement Document and Development Plan" in which future developments required to achieve a 30 GHz low-cost solid state amplifier engineering model are identified. Also included in this report is cost information for producing these amplifiers in medium quantities.

2. PROGRAM OBJECTIVES

2.1 PROGRAM OBJECTIVES

The objective of this program was to develop one proof-of-concept (POC) model of a 30 GHz solid state amplifier meeting the performance requirements presented in Section 2.2. Since high power IMPATT diodes were not then available in the Ka-band frequencies, the objective of the program was also to develop high power double-drift silicon IMPATT diodes capable of 2.5 W output power and utilize them in the amplifier development. The POC model was to demonstrate technology readiness, amenability to low cost production, and provide the data base for a 1987 low cost ground terminal experimental 30/20 GHz satellite communication system.

2.2 REQUIREMENTS

Requirements for the amplifier consistent with the program objectives were established and are presented in the following paragraphs.

2.2.1 RF Band

The instantaneous RF bandwidth shall be a minimum of 50 MHz in the band of 28.5 to 29.0 GHz.

2.2.2 RF Output Power

The RF output power over the instantaneous band shall be 20 Watts at saturation into any load characterized by a VSWR of <1.3.

2.2.3 RF Gain

The RF gain at saturation shall be 30 dB ± 1 dB, over the instantaneous bandwidth.

2.2.4 In-Band Overdrive

The amplifier shall be able to survive a steady state input of 5 dB greater than normally required to achieve saturation with no permanent degradation in performance.

2.2.5 Gain Variation

The gain shall not vary more than ±0.5 dB over the instantaneous band.

2.2.6 Gain Slope

The gain slope shall not exceed 0.15 dB/MHz in any 1 MHz portion of the instantaneous band.

2.2.7 Phase Linearity

The phase linearity at and below saturation shall not deviate from linear more than 10° P-P over the instantaneous band.

2.2.8 Harmonic and Spurious Response

The harmonic output shall be at least 50 dB below the carrier at saturation. The spurious output shall be at least 60 dB below the carrier at saturation.

2.2.9 Noise Performance

The noise performance of the amplifier shall provide minimum degradation to signal quality.

3. SYSTEM DESIGN

This section gives an overview of the POC amplifier system design. From the inception of the program, the system design has undergone some significant evolutions. We believe that it is important to review and understand some of these design evolutions so that one can better appreciate the final design for the deliverable hardware. During the preliminary design phase, two approaches were presented. The baseline approach assumes IMPATT diodes capable of 2.5 W output power. It calls for a three stage amplifier design: a single-diode input stage, a single-diode intermediate stage, and a 10-diode Kurokawa power combiner output stage. An alternate approach assumes IMPATT diodes capable of 2.0 W output power, and is similar to the baseline approach except that the output stage is now a 12-diode Kurokawa power combiner. All stages are injection-locked oscillators operating in the CW mode. Figures 3-1 and 3-2 show functional block diagrams of these two preliminary approaches.

As the development effort proceeded, it was determined that the single-diode driver is capable of sufficient gain and bandwidth such that the single-diode input stage and the single-diode intermediate stage can effectively be replaced by one single-diode driver stage. It was also decided that since the POC amplifier will ultimately be used in a TDMA system, additional design changes should be made so as to make the amplifier amenable to operating in the burst or pulse mode in which the rf output power is gated on and off at selected time intervals. One method is to simply turn all the diode currents on or off by means of high speed current modulators. The disadvantage of this method is that it will add considerable complexity to the amplifier hardware. A second approach which was seriously considered is shown schematically in Figure 3-3. Consider a train of rf pulses at frequency f_1 incident upon the amplifier input port. We assume that f_1 is within the injection-locking band of the amplifier and that the amplifier free-running frequency f_0 is lower than f_1. The amplifier is followed by a high power terminated circulator and a high-pass waveguide filter. The HPF is designed such that f_c is within the

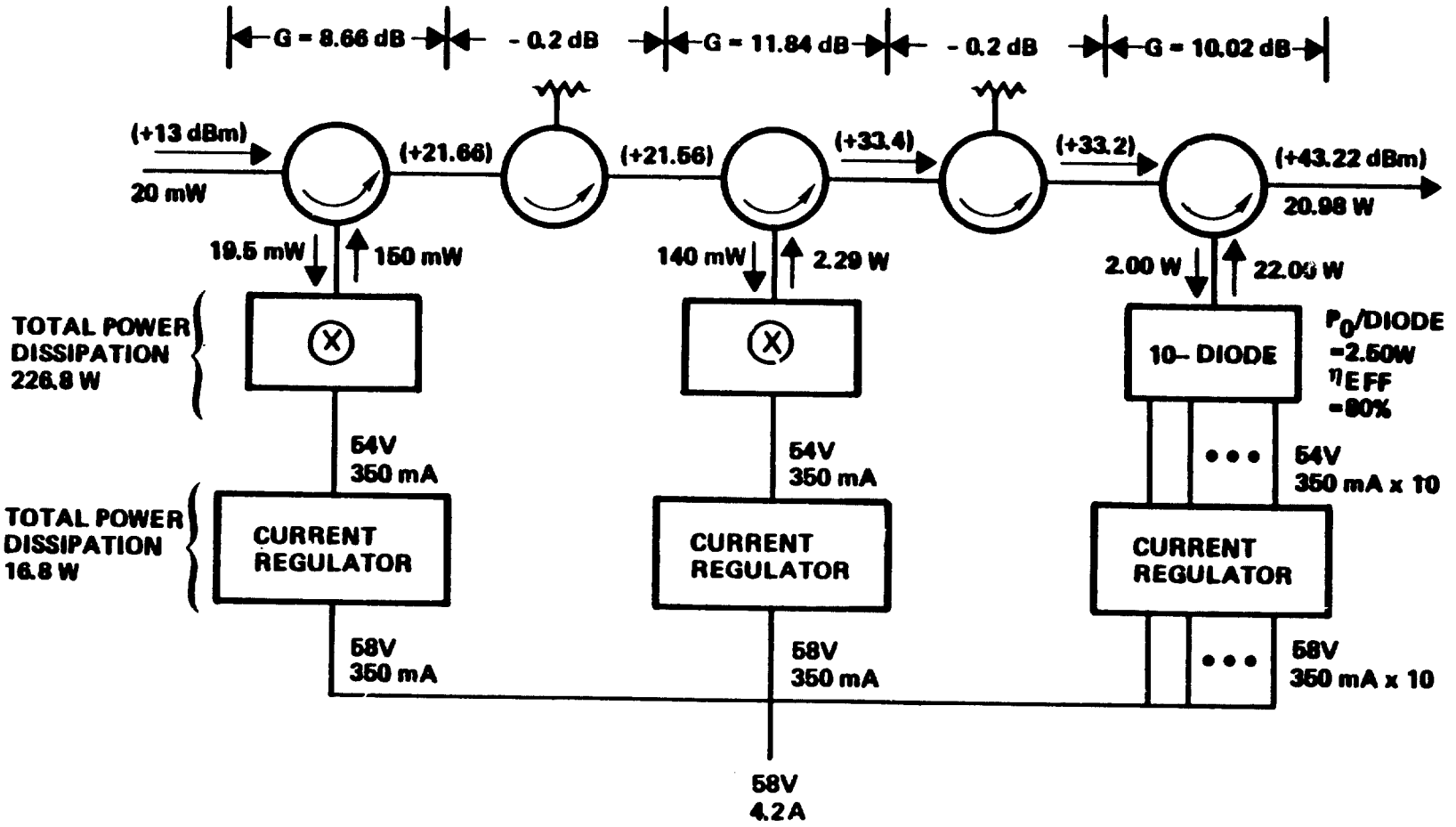


Figure 3-1. INITIAL ALTERNATE POC AMPLIFIER DESIGN

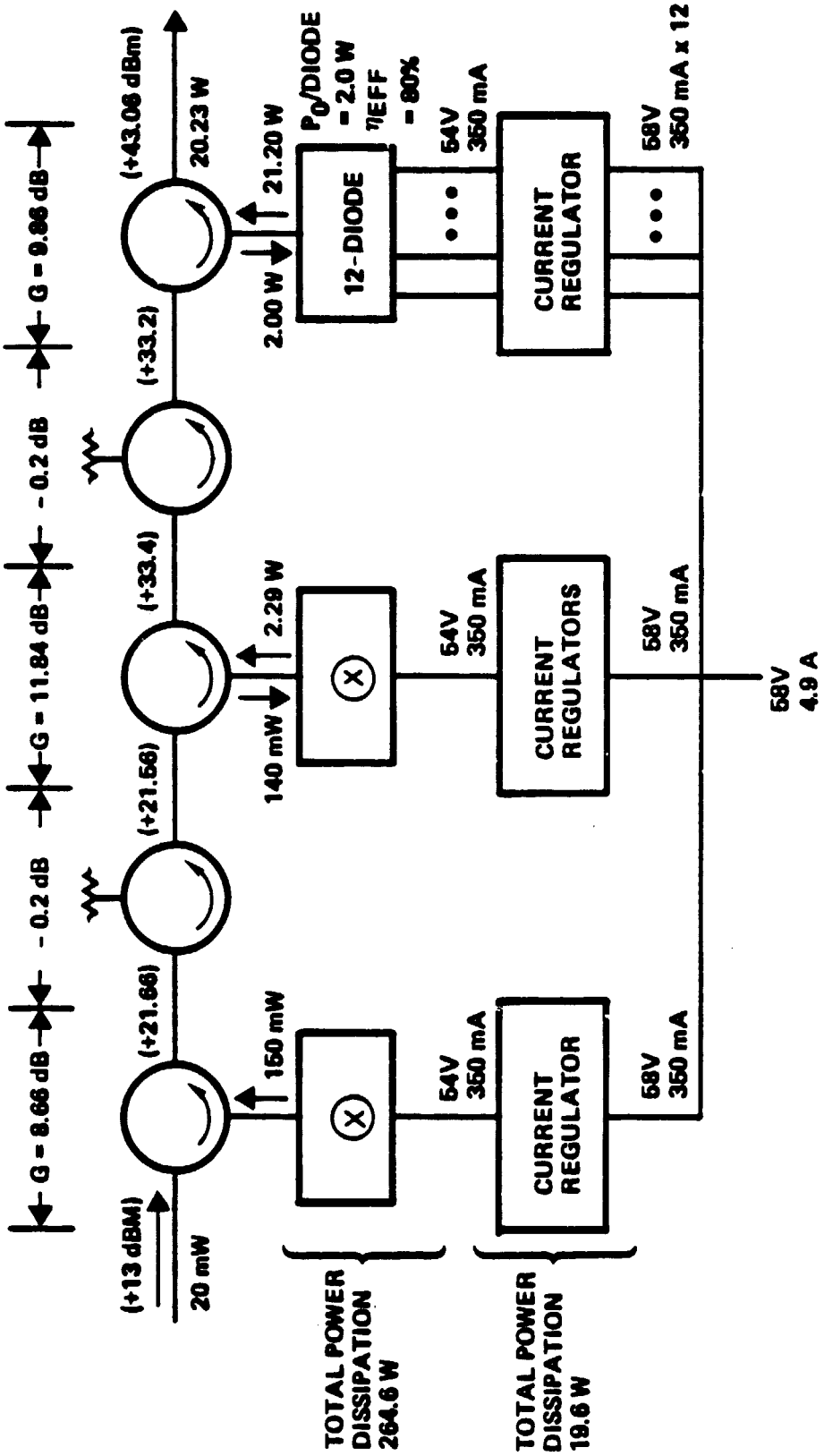


Figure 3-2. INITIAL ALTERNATE POC AMPLIFIER DESIGN

stopband and f_1 is within the passband. When the amplifier is injection-locked to f_1 , power is transmitted through the HPF. When the amplifier is unlocked, its output frequency falls back to f_0 and power is reflected back into the circulator high power load, blocking the rf transmission. The spectral description of this method is also shown in Figure 3-3. Figure 3-4 shows the swept response of a waveguide HPF near 29.0 GHz. The minimum bandwidth required to achieve 0.3 dB rejection in the passband and -30 dB rejection in the stopband is 400 MHz. This implies that if the frequency of the amplifier were to be switched in and out the HPF skirt, the amplifier must be capable of a minimum of 450 MHz injection-locking bandwidth, of which 50 MHz is the instantaneous bandwidth requirement. After a careful assessment of the amplifier gain-bandwidth budget, it was concluded that one cannot achieve the 450 MHz locking bandwidth without implementing some drastic changes, such as adding a two-diode intermediate driver. This would in turn add to the manufacturing cost of the amplifier. Based on these reasons, the HPF approach was discarded.

As will be described in Section 5, it was demonstrated later on in the program that depending on the output iris size, the power combiner can either be operated in the injection-locking mode or in the stable amplifier mode. If the power combiner were operated in the stable mode, then one can switch the output power on or off by simply gating the input power on or off. After careful consideration, it was decided that the optimum approach is to turn the driver module on and off by means of a fast switching pulse modulator. The pulse modulator switching characteristics will be entirely controlled by an external TTL trigger signal. A functional block diagram of this approach on which the POC amplifier was finally based is shown in Figure 3-5. Two design features are worth pointing out. One is that a twelve-diode design has been adopted for the power combiner primarily for reliability (Mean-time-to-failure) considerations. The other is that in actual operation, the +13 dBm pilot signal must also be gated on and off in synchronization with the driver. This, for example, can be accomplished by a high speed PIN switch and a synchronization circuit as shown in Figure 3-5 by the components enclosed within broken lines. This part of the circuit, however, was not part of the final hardware delivery.

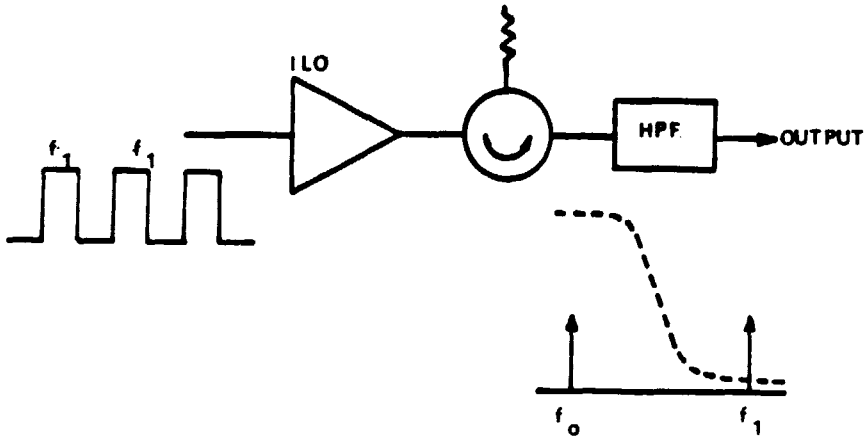


Figure 3-3. TDMA SWITCH DESIGN BASED ON HPF.

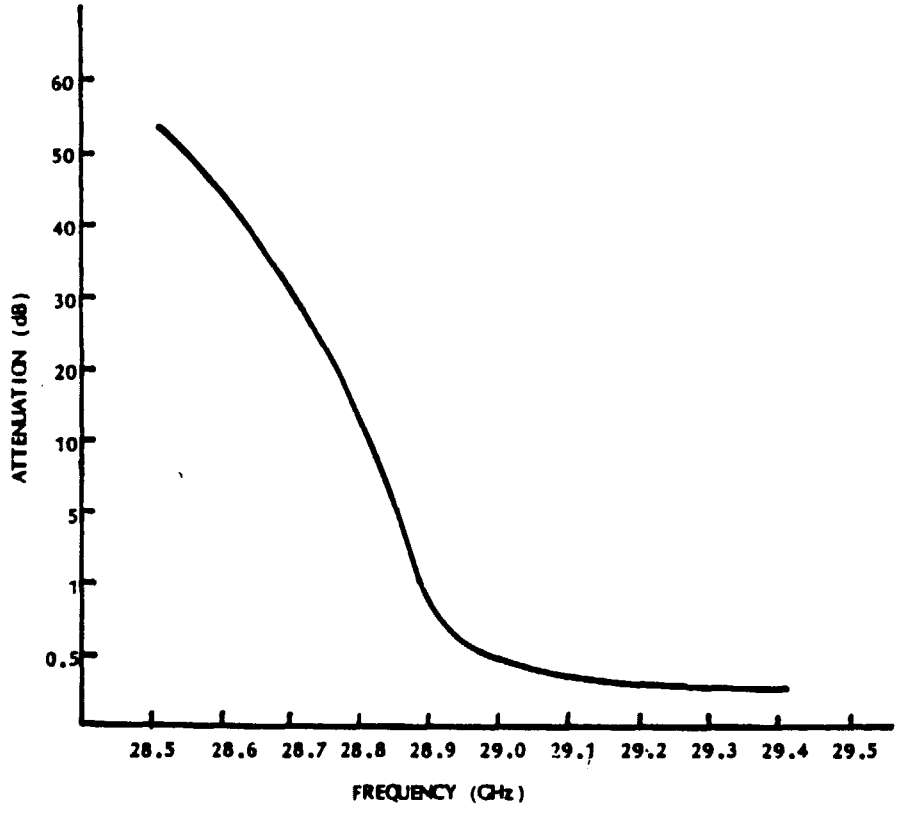


Figure 3-4. WAVEGUIDE HPF PERFORMANCE NEAR 30 GHz

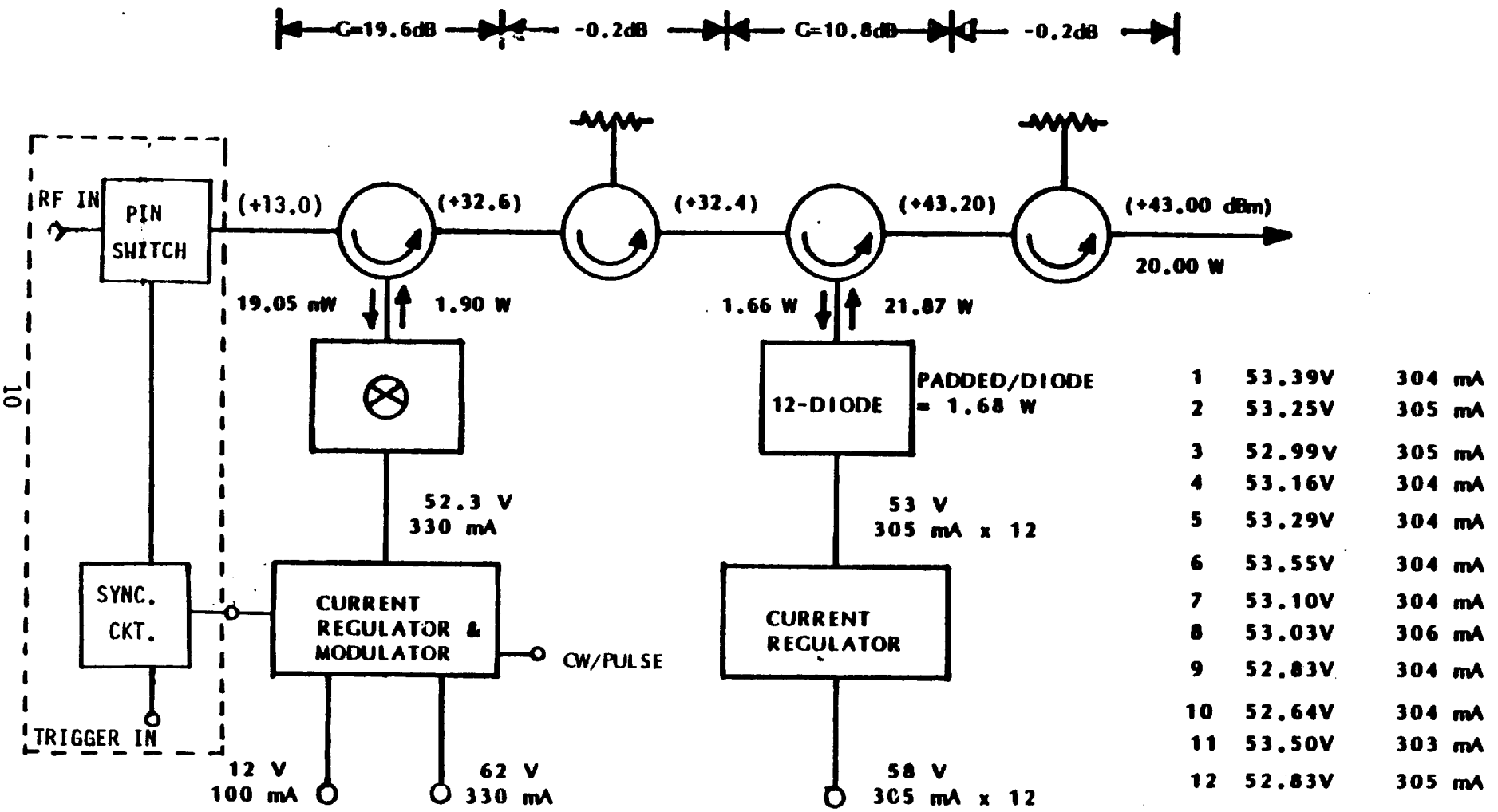


FIGURE 3-5. FINAL POC AMPLIFIER DESIGN

4. IMPATT DIODE DEVELOPMENT

The objective of the IMPATT diode development task was to design, fabricate and test double-draft silicon IMPATT diodes which meet the POC model requirements. These devices were used to verify the feasibility of the amplifier design approach and aid in the development of the POC model meeting the program objectives.

The IMPATT diode manufacturing process at TRW was designed for the production of low cost, double drift IMPATT diodes at 29 GHz. The four main tasks are silicon epitaxy, diode fabrication, diode packaging, and DC evaluation. The advantage of this process is that it is both simple and high yield, which results in low cost per diode. The two inch diameter wafers used typically yield approximately 11,000 diodes per wafer.

During Task II, the process was developed and optimized to provide high power, high efficiency silicon IMPATT diodes meeting device objectives. All performance objectives were successfully and reproducibly demonstrated within the time constraints of progrm Task II. Goals and results achieved are summarized below:

	Goal	Performance Achieved
Output Power (Watts CW)	2.5	2.7
Center Frequency	28.5-29.0	28.5
Conversion Efficiency (%)	12	12.1
Junction Temperature (°C)	250	210

This section will highlight the key accomplishments of the IMPATT diode development. The IMPATT diode design and performance data will be presented. For further details on diode processing, fabrication, and packaging, the reader may refer to Task II Report.

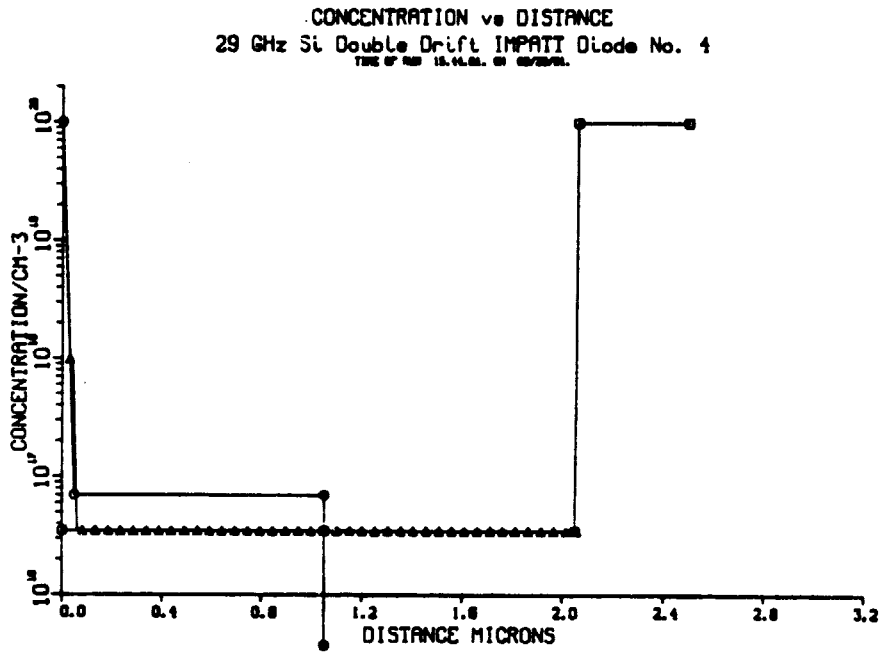


Figure 4-1. CONCENTRATION VS DISTANCE FOR 29 GHz SILICON DOUBLE-DRIFT IMPATT DIODE

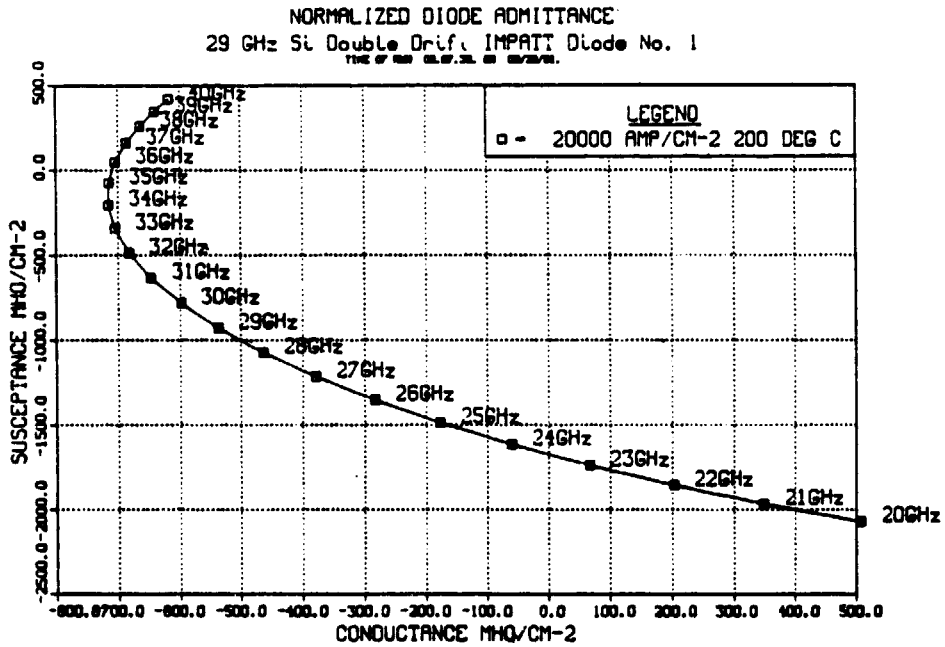


Figure 4-2. NORMALIZED DIODE ADMITTANCE FOR 29 GHz SILICON DOUBLE- DRIFT IMPATT DIODE.

Large Signal Analysis

A detailed large signal analysis was performed using theoretical modelling written by P. Blakey of the University of Michigan. Computed results for a double drift silicon IMPATT diode give the electric field, hole density, and electron density as a function of distance over the depletion region. Figure 4-3 shows the field and current density profiles and Figure 4-4 illustrates the large signal predictions for a 30 GHz IMPATT doping profile.

The large signal double-drift silicon IMPATT diode design for 30 GHz operation is summarized as follows:

$$N = 2.4 \times 10^{-6}\ cm^{-3}$$

$$N = 2.75 \times 10^{-6}\ cm^{-3}$$

$$W = 1.15\ \mu m$$

$$W = 1.0\ \mu m$$

$$V = 40\text{-}41\ V$$

It should be noted that this profile is asymetric with respect to n and p type doping concentration and drift region thickness. Large signal analysis predicts RF performance characteristics as follows:

Power Output	2.87 Watts
Frequency	30 GHz
Efficiency	12.78%
Junction Temperature	250°C

4.1 DEVICE DESIGN

A double-drift silicon IMPATT structure was selected by applying two design approaches: small signal and large signal analysis. Best device performance was achieved using a combination of the results obtained from these theoretical modelling schemes.

Small Signal Analysis

A program has been developed at TRW to determine the optimum doping concentration for an IMPATT diode operating at a given frequency. This simulation also determines the epitaxial layer thicknesses. The analysis uses the ionization rates of Grant [1] and the drift velocities of Canali, et al. [2]. The doping profile determined using this analysis is shown in Figure 4-1.

For a specified current density, operating junction temperature, and doping concentration, the device admittance can be calculated from the small signal analysis of Misawa [3]. Figure 4-2 is a computer plot of the normalized device admittance for a double-drift IMPATT diode designed for 29 GHz CW operation. A summary of the symmetric IMPATT design parameters as determined by the small signal analysis approach is given below.

DOPING CONCENTRATION (CM^{-3})	3.7×10
EPI Thickness (μM)	1.1
Current Density (KA/CM^{-2})	15
Device Diameter (μM)	50
Heat Sink Configuration	Type IIA Diamond
Breakdown Voltage (Volts)	41.2

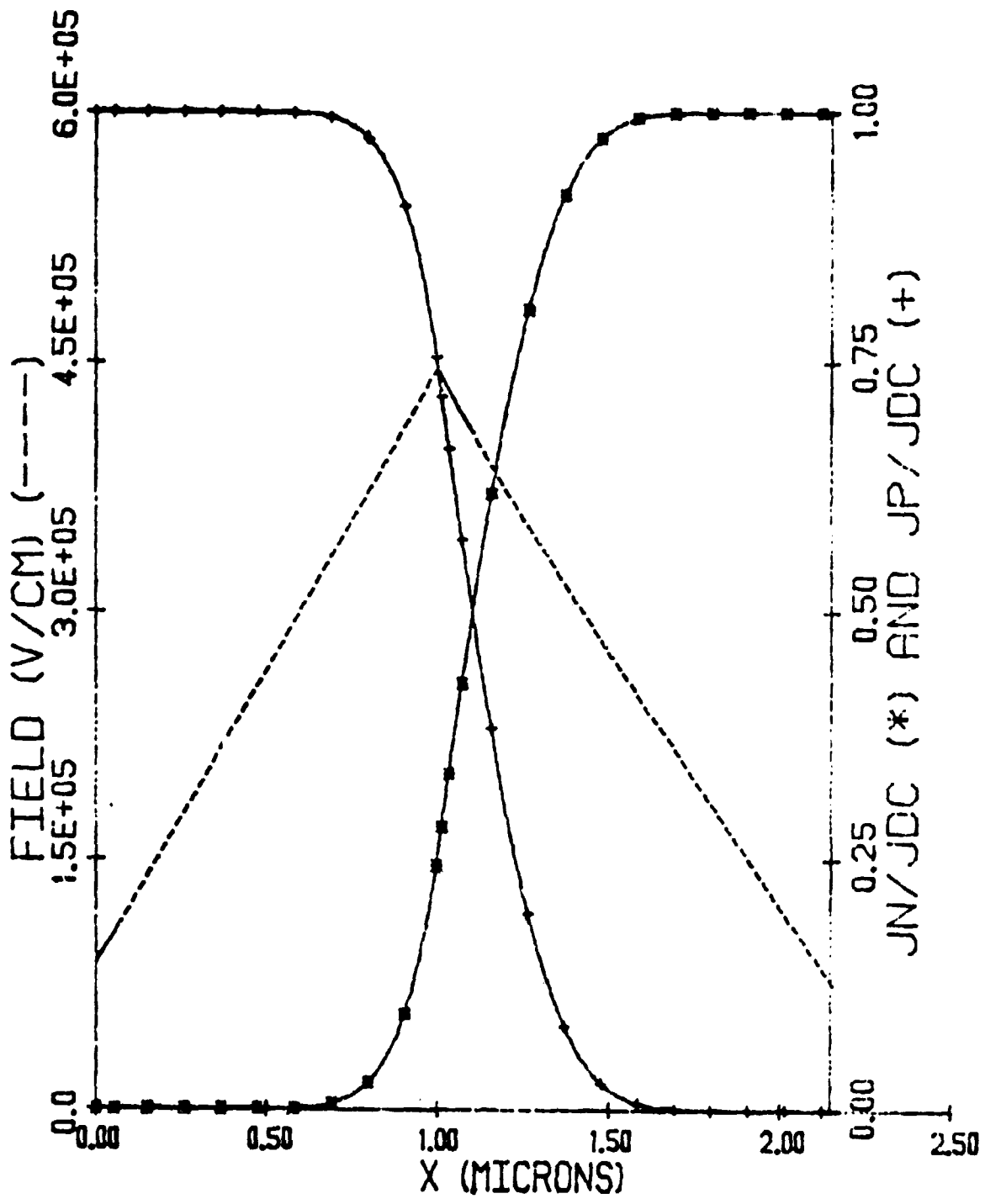


Figure 4-3. LARGE SIGNAL FIELD AND CURRENT DENSITY PROFILE

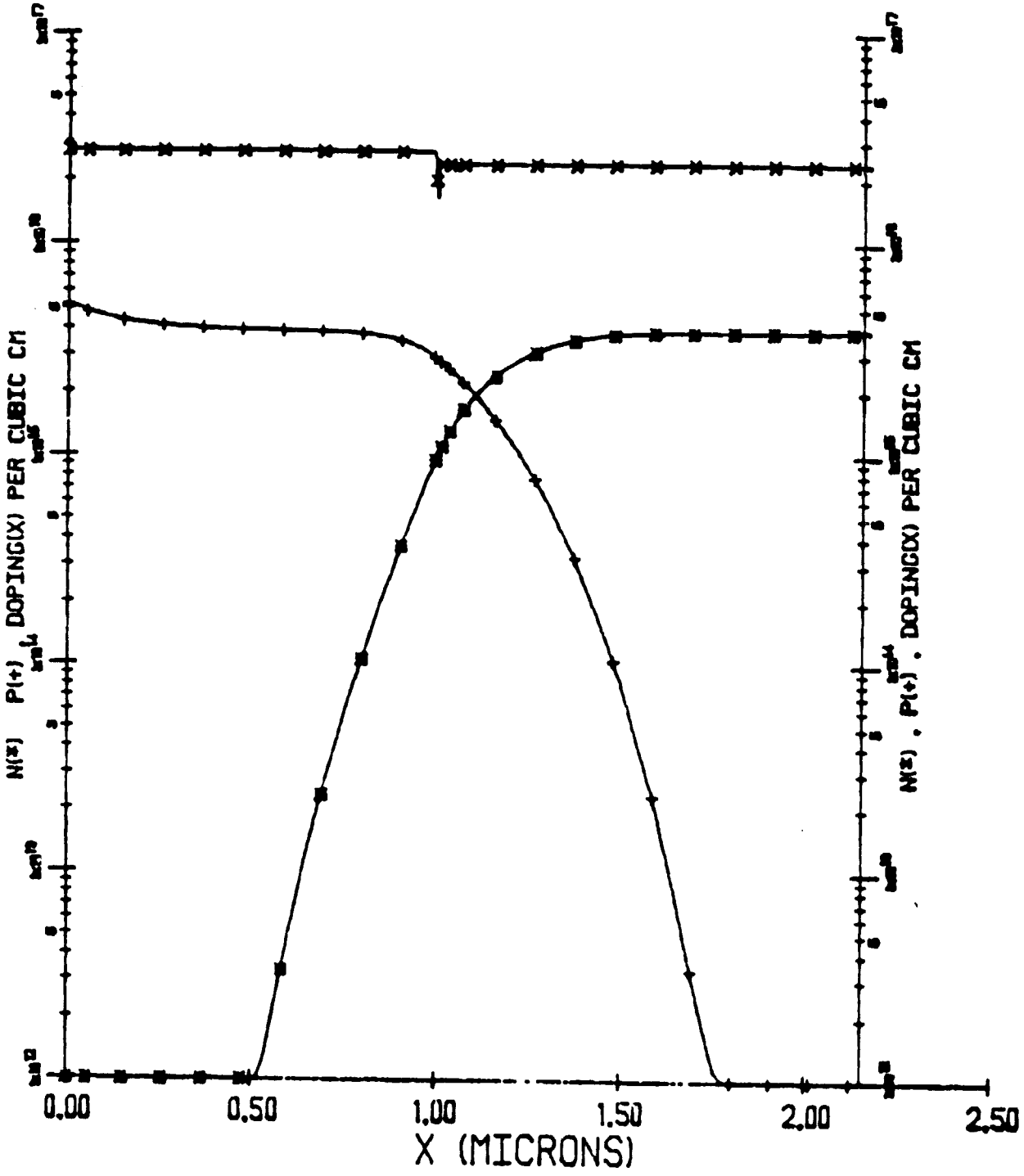


FIGURE 4-4. LARGE SIGNAL DOPING PROFILE

4.2 TEST RESULTS

The IMPATT diode is shown schematically in Figure 4-5. It consists of a hermetically sealed quartz-ring package on copper disk with the diode chip thermal-compression bonded on a Type II-A diamond heat sink for efficient heat dissipation. The diamond heatsink is gold-plated and is pressed into a 0.060-diameter copper disc. Electrical contact to the diode mesa is provided by two gold ribbons in a "cross-strap" configuration, which provides the proper series inductance ($\simeq 0.15$ nH) to the diode mesa as shown in the equivalent circuit of Figure 4-6. The copper disc is then soldered onto a screw stud as shown in Figure 4-7. The screw stud provides easy assembly and disassembly from the waveguide test cavity which was described in Section 5.1. The diodes are tested as oscillators using the test setup shown schematically in Figure 4-8 . A representative list of test data from diode lots DKA 9, 14, 26, and 33 is shown in Table 4-1.

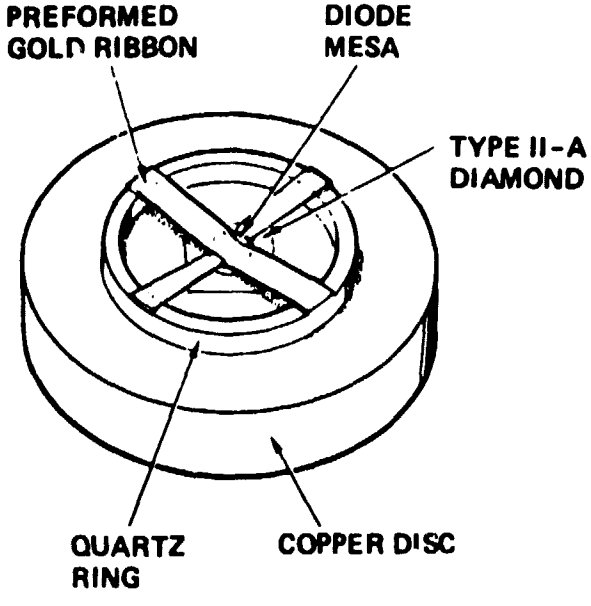


FIGURE 4-5. IMPATT DIODE QUARTZ RING PACKAGE

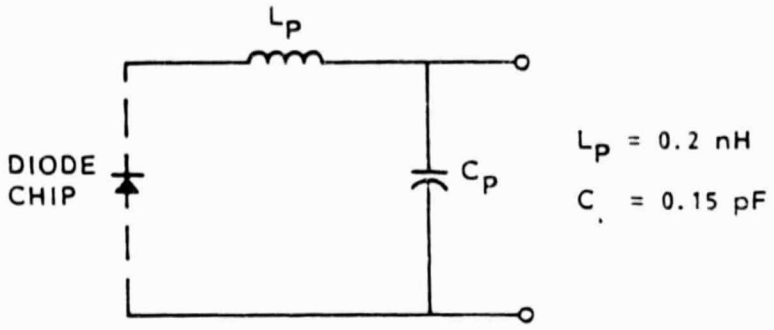


FIGURE 4-6. IMPATT DIODE EQUIVALENT CIRCUIT

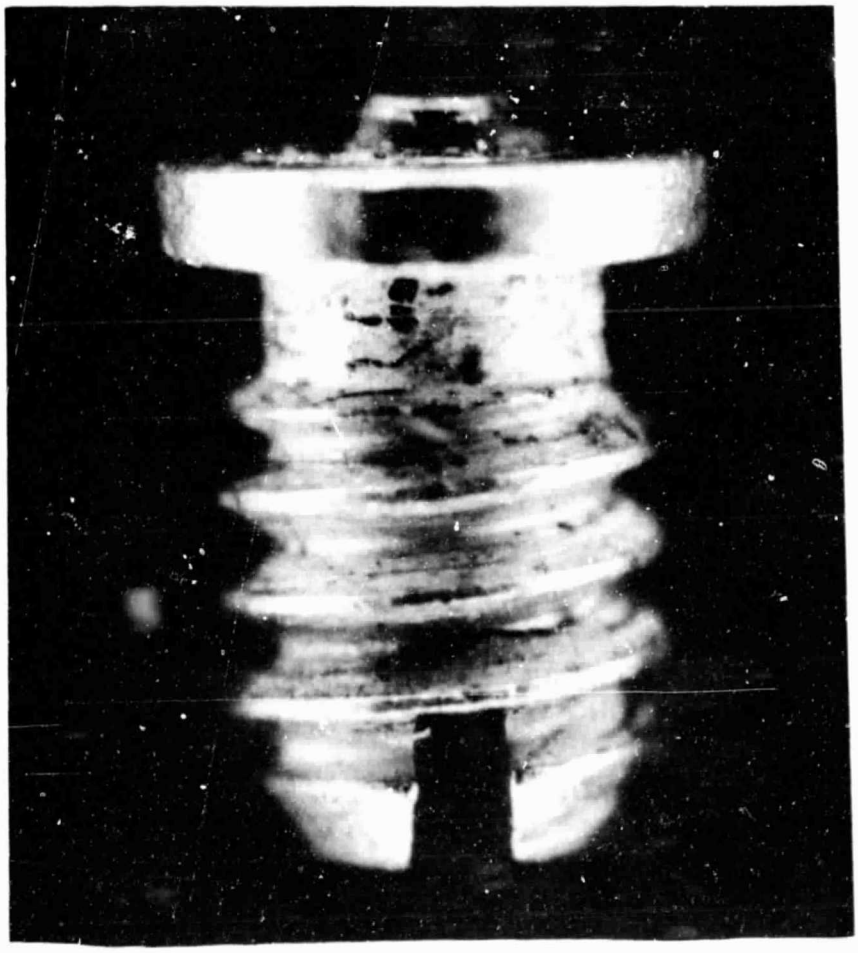


FIGURE 4-7. IMPATT DIODE SOLDERED IN A SCREW STUD.

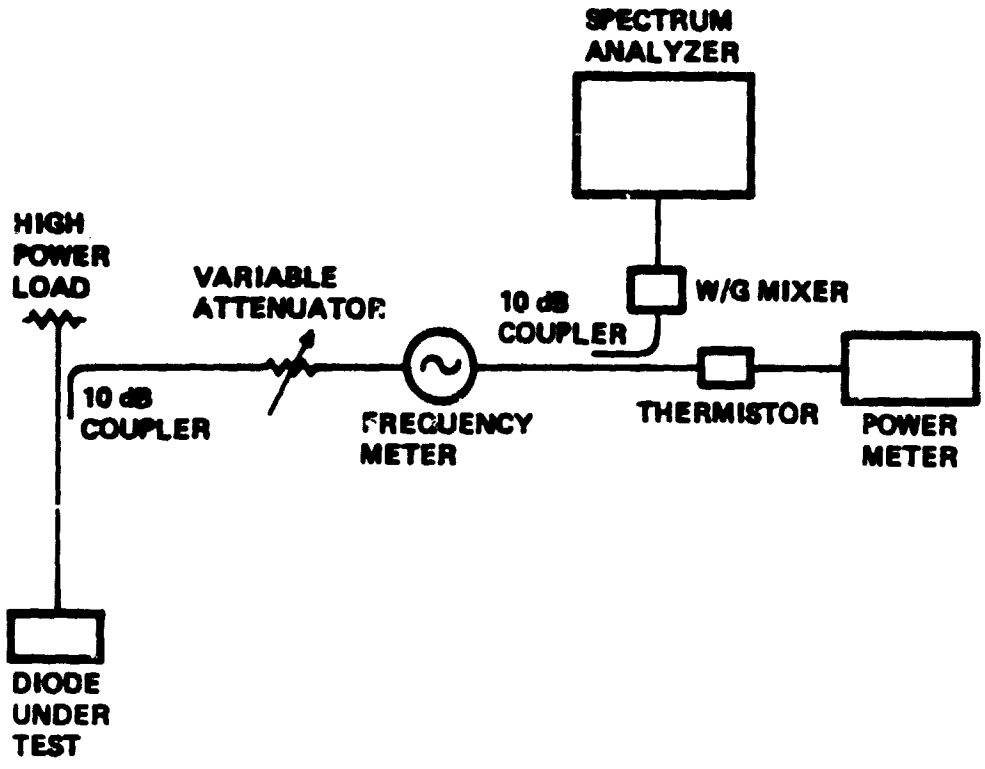


FIGURE 4-8. IMPATT OSCILLATOR TEST SETUP SCHEMATIC.

DIODE NO.	C_o (pF)	R_{TH} °C/W	FREQUENCY (GHz)	ΔT_j (°C)	P_{OUT} (W)	EFFICIENCY (%)
DKa 93-3	2.97	12.80	28.49	229	2.19	11.0
-5	2.56	12.13	29.56	223	2.34	11.7
9C-1	2.42	14.86	29.60	285	1.74	8.2
-2	2.73	14.24	30.86	200	1.58	8.6
9L-14	2.79	12.85	29.94	243	2.14	11.5
-13	2.93	11.72	30.03	200	2.19	11.4
9M-1	2.65	12.16	29.21	247	2.45	10.8
-2	2.74	11.72	29.18	237	2.45	10.8
-3	2.81	12.35	29.56	197	2.19	10.0
-4	2.62	12.74	29.62	246	2.19	10.1
-5	2.65	12.47	28.49	233	2.45	11.6
-8	2.80	12.20	29.18	207	2.14	11.2
-9	2.67	12.01	29.50	211	2.19	11.1
9P-6	2.81	12.83	29.13	228	1.78	9.6
-12	2.80	10.29	29.62	125	2.09	10.7
-15	2.79	9.96	29.10	168	2.14	11.3
DKa 14D-1	2.92	9.59	28.47	231	2.57	10.0
-2	2.98	9.88	29.84	242	2.63	10.9
-3	3.03	8.74	29.52	189	2.24	9.4
-4	2.84	9.40	28.89	204	2.50	10.2
-5	2.92	9.48	28.79	192	2.51	11.0
14E-1	2.52	12.85	29.49	236	2.34	12.0
-2	2.81	11.88	29.28	204	2.30	11.8
-3	3.01	11.41	28.8	201	2.01	11.0
-4	2.68	13.40	29.95	232	2.19	12.0
-5	2.94	11.33	28.44	210	2.57	12.1
-6	2.61	12.90	28.25	230	2.45	12.1
-8	2.69	12.17	29.55	226	2.34	11.2
-9	2.83	11.70	28.81	239	2.75	11.9
-10	2.95	11.25	28.70	191	2.04	10.7

DIODE NO.	C_o (pF)	R_{TH} (°C/W)	FREQUENCY (GHz)	ΔT_j (°C)	P_{OUT} (W)	EFFICIENCY (%)
DKa 26A-2	3.03	14.26	28.80	239	1.91	8.2
-3	2.98	12.91	28.81	211	1.95	9.0
-4	2.72	11.80	28.80	245	2.57	11.8
26A-3	2.83	11.20	28.75	200	2.34	11.5
-6	2.82	12.40	28.38	222	2.19	10.9
-8	2.88	11.48	27.99	208	2.04	10.1
-9	2.85	14.11	27.58	260	2.14	10.4
-11	2.82	14.09	28.85	258	2.04	10.0
33A-1	2.99	11.03	28.78	175	2.19	12.1
-2	2.87	14.16	29.55	242	2.45	12.6
-3	2.45	12.81	29.58	215	2.34	12.3
-4	2.83	11.70	29.52	205	2.34	11.9
-5	2.85	10.87	29.17	182	2.45	12.8
33B-1	2.83	9.83	29.13	160	2.45	12.6
-3	2.92	9.30	29.49	157	2.30	12.0
-4	2.95	10.61	28.67	178	2.39	12.4
-5	2.93	11.39	29.32	198	2.45	12.3
33C-1	2.78		28.84		2.29	11.9
-2	2.83		30.19		2.57	12.2
-3	2.79		28.58		2.45	11.3
-4	2.78		29.82		2.04	10.3
-5	2.82		29.99		2.39	12.6
-6	2.79		29.61		2.45	12.3
-9	2.81		28.94		2.00	10.5
-10	2.79		29.53		2.18	10.8
-11	2.76		29.64		2.18	9.8
-13	2.76		29.56		2.23	10.0

TABLE 4-1. REPRESENTATIVE IMPATT DIODE TEST DATA.

SECTION 4 REFERENCES

1. W. N. Grant, "Electron and Hole Ionization Rates in Epitaxial Silicon at High Electric Fields," Solid State Electronics, Vol. 15, 1972, p. 457.

2. C. Canali, et al, "Electron and Hole Drift Velocity Measurements on Silicon and Their Empirical Relation to Electric Field and Temperature," IEEE Transactions on Electron Devices, Vol. ED22, November 1975, pp. 10451046.

3. T. Misawa, "Negative Resistance in pn Junctions under Avalanche Break down Conditions, Part I and II," IEEE Transactions on Electron Devices, Vol. ED-13, January 1966, pp. 137-151.

5. CIRCUIT DEVELOPMENT

The circuit development in this program can be conveniently classified into five areas: driver stage, output stage, circulator, bias regulator, and pulse modulator. A description of the development of these circuits is presented in the following sections.

5.1 DRIVER STAGE DEVELOPMENT

The main requirement of the single-diode driver stage is a large gain-bandwidth product. To achieve such an objective, the circuit used must provide a suitable impedance locus as seen by the IMPATT diode. An impedance locus is a plot of the circuit impedance as a function of the frequency $Z(\omega) = R(\omega) + jX(\omega)$ in the complex plane with jX as the vertical axis and R the horizontal axis. When the diode impedance as a function of frequency is also plotted on the same complex plane, the intersection of the two loci indicates the oscillation characteristics of the circuit. For example, the impedance locus of an IMPATT diode is a near-straight curve with a moderate slope; the impedance locus of a single-tuned circuit (a circuit with only one resonance) is always a vertical line. The two loci are plotted in Figure 5-1. The arrows on the curves indicate the direction of increasing frequency. The intersection of the two loci is a well-defined point. The output of this circuit has a sharp spectrum with well-defined amplitude and frequency characteristics. The bandwidth characteristics of a single-tuned circuit are characterized by the rate of change of circuit reactance versus frequency, $\partial X/\partial\omega$ (or circuit susceptance versus freuency, $\partial B/\partial\omega$). A wide bandwidth is characterized by a small $\partial X/\partial\omega$. For a single-tuned cirucit, such as the one shown in Figure 5-2(a),

$$\frac{\partial X}{\partial \omega} = \frac{2R_L}{\omega} Q_{ex} \tag{5-1}$$

where $Q_{ex} = \omega L/R_L = 1/\omega R_L C$ and R_L = load resistance. The injection-locking bandwidth, $\Delta\omega$, of this circuit is [1,2]:

$$\frac{\Delta\omega}{\omega_0} = \frac{2}{Q_{ex}} \sqrt{\frac{1}{G}} \tag{5-2}$$

where ω_0 = resonant frequency of the circuit and G = power output/power input. It is readily seen that a low Q factor is essential for wideband operations.

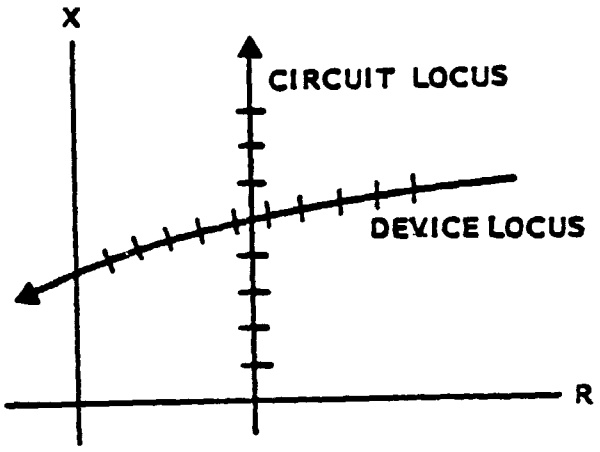
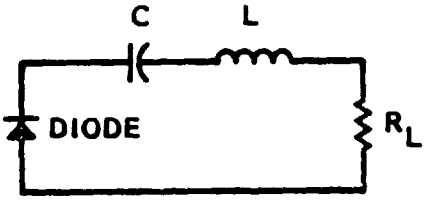
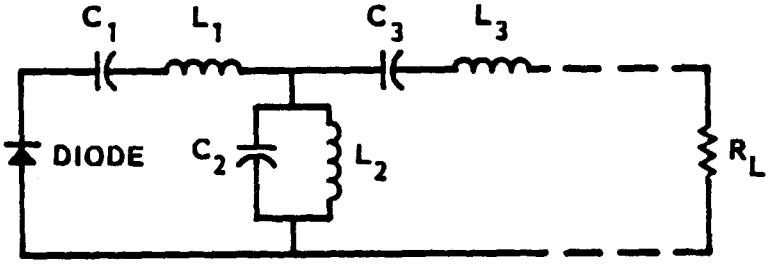


FIGURE 5-1. IMPEDANCE LOCUS OF SINGLE TUNED CIRCUITS

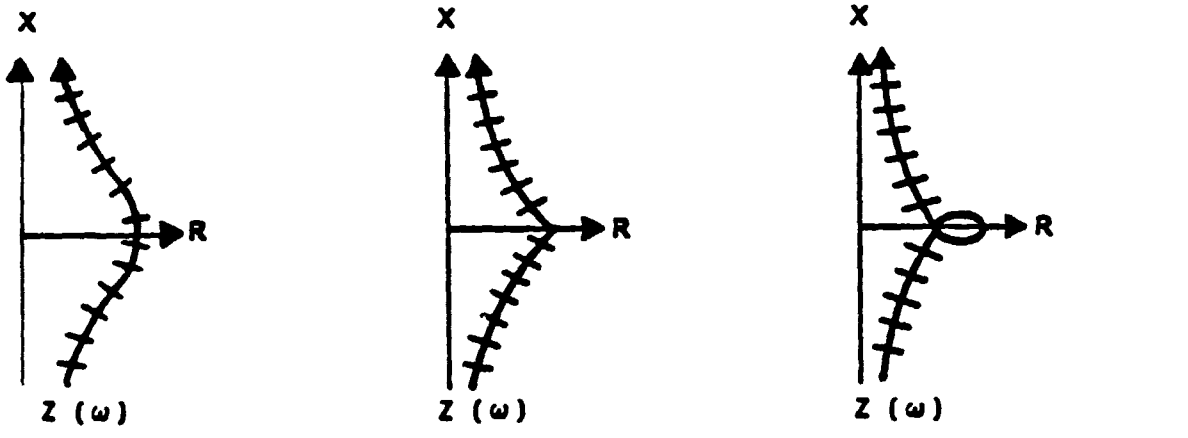


(a) SINGLE-TUNED CIRCUIT



(b) MULTI-TUNED CIRCUIT

FIGURE 5-2. EQUIVALENT CIRCUITS OF IMPATT OSCILLATORS



(a) MULTI-TUNED WIDEBAND

(b) MULTI-TUNED NOISY

(c) MULTI-TUNED MULTIPLE OSCILLATION

FIGURE 5-3. IMPEDANCE LOCI OF MULTITUNED CIRCUITS SHOWING THREE DIFFERENT CONFIGURATIONS

All waveguide oscillators are, however, multituned circuits (with more than one resonator). Circuits of this type possess a rather complicated impedance locus as indicated by three possible plots shown in Figure 5-3. The plot shown in Figure 5-3(a) is characterized by a smooth "bump" on the impedance locus centered at the resonant frequency. It can be shown that $\partial X/\partial\omega$ around the "bump" is smaller than the $\partial X/\partial\omega$ of the single-tuned circuit. Using a double-tuned circuit as an illustration, it can be shown that the rate of change of reactance versus frequency is

$$\frac{\partial X}{\partial \omega} = \frac{2R_L}{\omega} Q_{eq} \tag{5-3}$$

where Q_{eq} is the equivalent Q-factor defined by

$$Q_{eq} = Q_1 - Q_2 \quad \text{(double-tuned circuit only)} \tag{5-4}$$

with $Q_1 = \omega L_1/R_L$ and $Q_2 = \omega L_2/R_L$.
It is readily seen that even the individual Q's, Q_1 and Q_2, are high, the equivalent Q being the difference between Q_1 and Q_2 can be very small. The circuit is thus shown to be capable of wideband operations. In fact, the injection-locking bandwidth in this case is given by [3]

$$\frac{\Delta\omega}{\omega_o} = \frac{2}{Q_{eq}}\sqrt{\frac{1}{G}} \tag{5-4}$$

with the restriction that Q_1 is larger than Q_2.

In the case of $Q_1 = Q_2$, $\partial X/\partial\omega$ is zero at the resonant frequency and a sharp peak is formed on the circuit impedance locus at the intersection with the diode impedance locus, as shown in Figure 5-3(b). Since, at their intersection point, the circuit locus and the diode locus are virtually tangential, oscillation frequency and amplitude are not well defined, and the output has a noisy spectrum.

In the case of Q_1 being smaller than Q_2, the circuit locus forms a loop around the diode locus. It is easily seen that no less than two intersection points would be formed between the two loci. The result is that multiple oscillations would take place (see Figure 5-2(c)). The objective of designing a multituned oscillator circuit is, therefore, to avoid a noisy or multiple spectrum on the one hand and to achieve a wideband operation on the other.

In microwave circuits (or millimeter wave circuits, for that matter), the determination of Q factors is a very complicated business, since the circuits are made of distributed components and not lumped components. Computer-aided design was employed to alleviate the difficulty. The method makes use of a circuit model with parameters which can be identified with those of the actual circuit. A computer program is then used to calculate the circuit properties including the impedance locus. By iterating the various parameters which correspond to actual phsycial dimensions, a circuit with the proper impedance characteristics can be designed in a relatively short time. The equivalent model was developed by several researchers [4,5] and is shown in Figure 5-4. Based on this model, the various circuit characteristics are defined by:

$$Y' = j \sum_{m=1}^{\infty} \frac{\cos m\pi}{X_m} e^{-mr\pi/b} \tag{5-5}$$

$$Y_{1p} = j \sum_{m=1}^{\infty} \frac{1}{X_m} e^{-m\pi r/b} - j \sum_{m=1}^{\infty} \frac{\cos m\pi}{X_m} e^{-m\pi r/b} = Y_{2p} \tag{5-6}$$

$$Z_{0p} = j \frac{Z_0}{4} \left[k_0^2 - \left(\frac{\pi}{a}\right)^2 \right]^{1/2} \sum_{n=2}^{\infty} \frac{\left[\cos \frac{m\pi r}{a} - \cos \frac{m\pi (2d \pm r)}{a}\right]}{\left(\frac{n^2 \pi^2}{a^2} - k_0^2\right)^{1/2}} \tag{5-7}$$

$$X_m = \frac{b^2}{4} \frac{\eta}{k_0 ab} \left(\frac{m^2 \pi^2}{b^2} - k_0^2\right) \left(\frac{a}{\pi}\right) \left[K_0 (r r_m) - K_0 (2d r_m)\right] \tag{5-8}$$

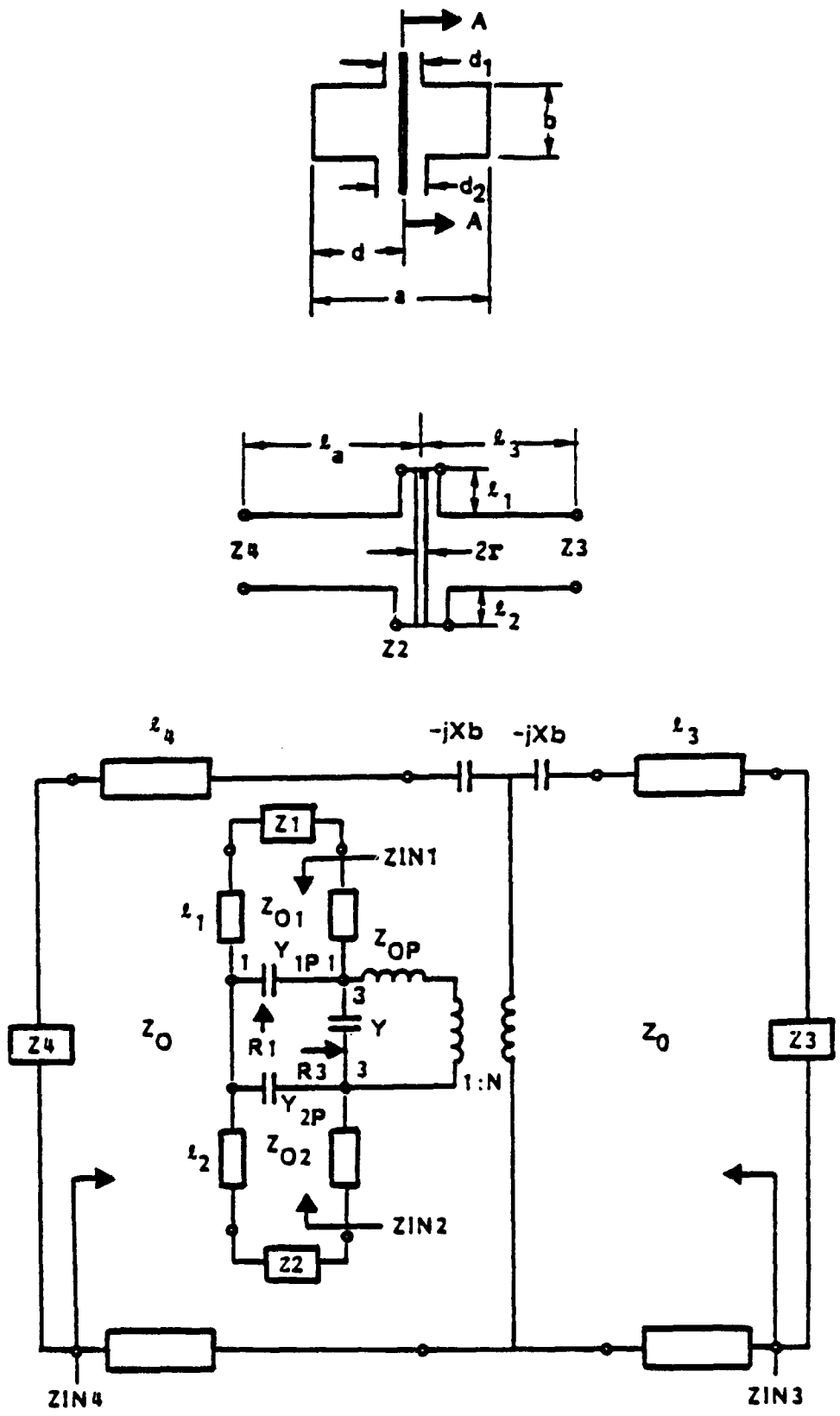


FIGURE 5-4. EQUIVALENT CIRCUIT MODEL OF A COAXIAL-WAVEGUIDE CIRCUIT FOR COMPUTER ANALYSIS

$$X_b = Z_0 \frac{a}{\lambda_g} \left(\frac{2\pi r}{a}\right)^2 \sin^2 \left(\frac{\pi d}{a}\right) \tag{5-9}$$

$$N = \sqrt{\csc \frac{\pi d}{a} \csc \frac{\pi (d \pm r)}{a}} \tag{5-10}$$

where

$$\Gamma_m = \left(\frac{m^2 \pi^2}{b^2} - k_0^2\right)^{1/2}$$

$$Z_0 = 2\eta \frac{b}{a} \frac{\lambda_g}{\lambda}$$

$$\lambda_g = 2\pi / \sqrt{k_0^2 - \left(\frac{\pi}{a}\right)^2}$$

$$\eta = 120\pi$$

$$K_0 = 2\pi/\lambda$$

K = modified Bessel function of the second kind

The model was found to have good correlation with measured data [5]. For oscillations to occur, using the IMPATT diode impedance plot shown in Figure 4-4, Section 4, the circuit resistance and reactance must satisfy the following two conditions at the operating frequency band:

$$R_{ckt} < \left| R_d \right| \tag{5-11}$$

$$X_{ckt} = -X_d \tag{5-12}$$

A computer program was used to calculate and iterate the various circuit parameters until a suitable impedance characteristic is found. One suitable set of circuit parameters was found to be:

ℓ = .0225 in.	z_1 = 1 (matched load)	2r = .046 in.
ℓ = .1575 in.	z_2 = 30 ohms	D_1 = .073 in.
ℓ = .0850 in.	z_3 = 1 (matched load)	D_2 = .052 in.
ℓ = .1350 in.	z_4 = 0 ohms	a = .280 in.
		b = .045 in.

The corresponding circuit resistance R_{ckt} and reactance X_{ckt} as a function of frequency are plotted in Figure 5-5. Also plotted in the same figure are the diode resistance R_D and reactance X_D from Figure 4-4, Section 4. It is easily seen that both the conditions of Eqs. (5-11) and (5-12) are satisfied. The intersection of X_{ckt} and X_D indicates the oscillation frequency of about 27.5 GHz.

The final configuration of the single-diode circuit is shown in Figure 5-6 in both construction form and equivalent circuit form. The circuit is a rather conventional waveguide oscillator circuit. By making the circuit parasitics minimum, such as the case of the present construction, the circuit can be shown to be triple-tuned. The three resonators are identified in the equivalent circuit, namely, the quarter-wave transformer, the quarter-wave waveguide short and the quarter-wave choke.

The operation of the circuit is as follows. The IMPATT diode requires a loading resistance of a few ohms. A full-height waveguide, on the other hand, offers an impedance of some 400 ohms. A reduced-height waveguide is therefore used to ease the problem of impedance matching. A two-step transformer is used to match the reduced-height waveguide to the standard full-height waveguide at the output. Since the two-step transformer has a wider bandwidth than the operating frequencies, it can be considered as a nonresonant ideal transformer. A two-section transformer, consisting of the bias pin and transformer shims, is used to match the reduced-height waveguide to the diode. The quarter-wave transformer has the special property that it not only transforms impedances but is also frequency-selective. It acts as a shunt resonator if seen from the high impedance side (from the reduced-height waveguide) and as a series resonator if seen from the low impedance side (from the IMPATT diode). This property is depicted in the equivalent circuit in Figure 5-6. A waveguide short circuit is placed a quarter-wave away from the bias pin in the reduced-height waveguide. The short circuit appears to the diode as an open

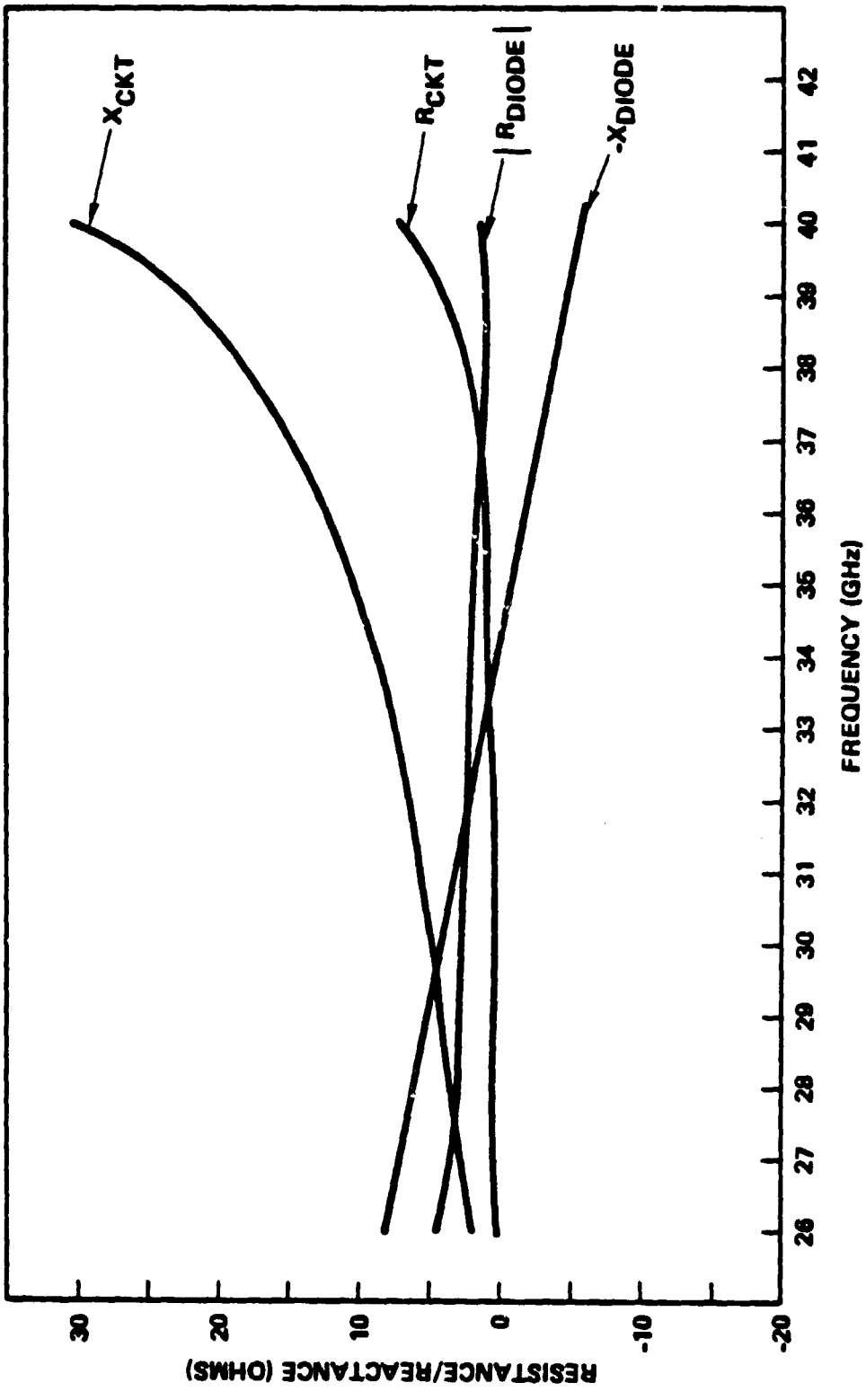
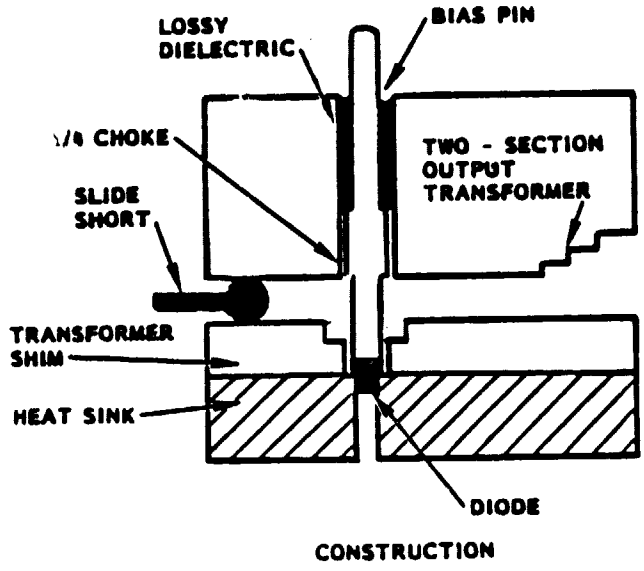


FIGURE 5-5. R/X PLOT OF COMPUTER MODEL



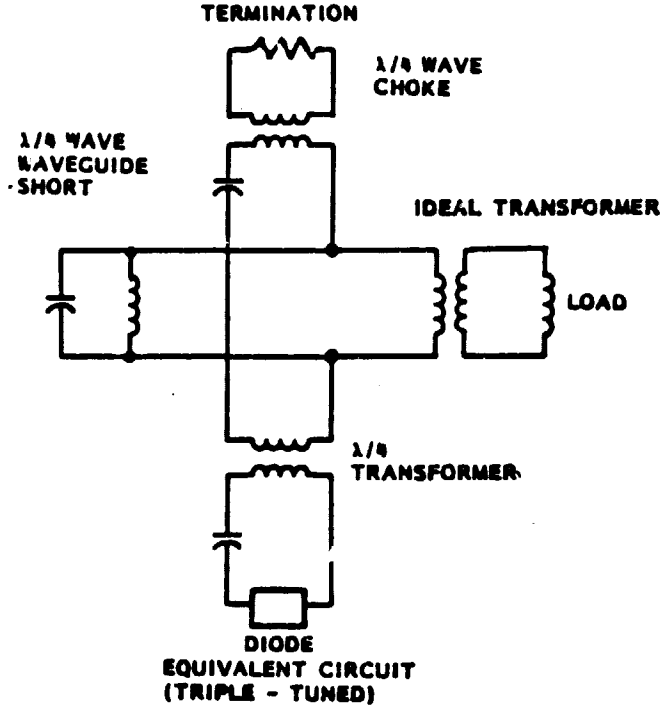


FIGURE 5-6. SINGLE-DIODE MULTITUNED CIRCUIT

circuit at the quarter-wave frequency and therefore has the property of a shunt resonator. RF power generated from the diode is shared between the load and the bias termination (formed by the lossy dielectric). A third resonator, the choke, is added to the bias port. The choke is merely a quarter-wave transformer which transforms the relatively low impedance of the bias termination to an even lower value, thereby allowing most of the RF power to go to the load.

A photograph of the single-diode circuit hardware is presented in Figure 5-7. The RF performance of this circuit is presented in Section 7.

5.2 OUTPUT STAGE

Due to the high output power requirement, the output stage is, of necessity, a multidiode circuit. Nonlinear interactions among the diodes impose restrictions on circuit performance. Consequently, the output stage is always the limiting member in the amplifier chain in terms of output power and operating bandwidth. There are two possible approaches to meet the power and operating bandwidth. One is to develop an IMPATT amplifier operating in the stable amplifier mode; the other is to develop an IMPATT amplifier operating in the injection-locked oscilator mode. At the outset, the stable amplifier was not considered as a viable approach because of gain considerations. However, as we shall see later, the stable amplifier mode was ultimatley used for the power stage because it proved to be a useful technique to achieve the so-called TDMA (time domain multiple access) burst mode operation with minimal addition of switching circuit hardware.

The basic construction of a rectangular waveguide combiner is shown in Figure 5-8. It essentially consists of a number of individual diode modules coupled to a rectangular waveguide through the sidewalls of the guide. The resonant cavity is formed by a short circuit on one end and an iris opening on the other end. The diode module is very similar to that of the driver stage. Figure 5-9(a) shows the construction of the diode module.

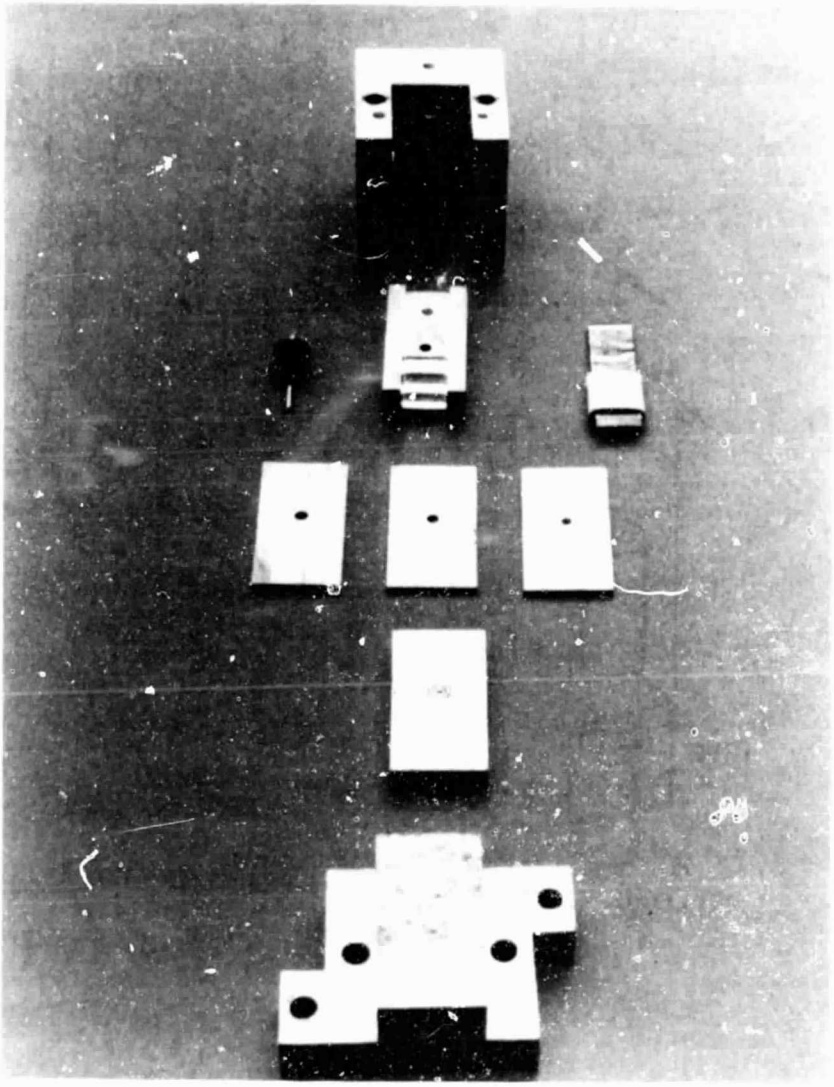


FIGURE 5-7. SINGLE-DIODE WAVEGUIDE CIRCUIT HARDWARE

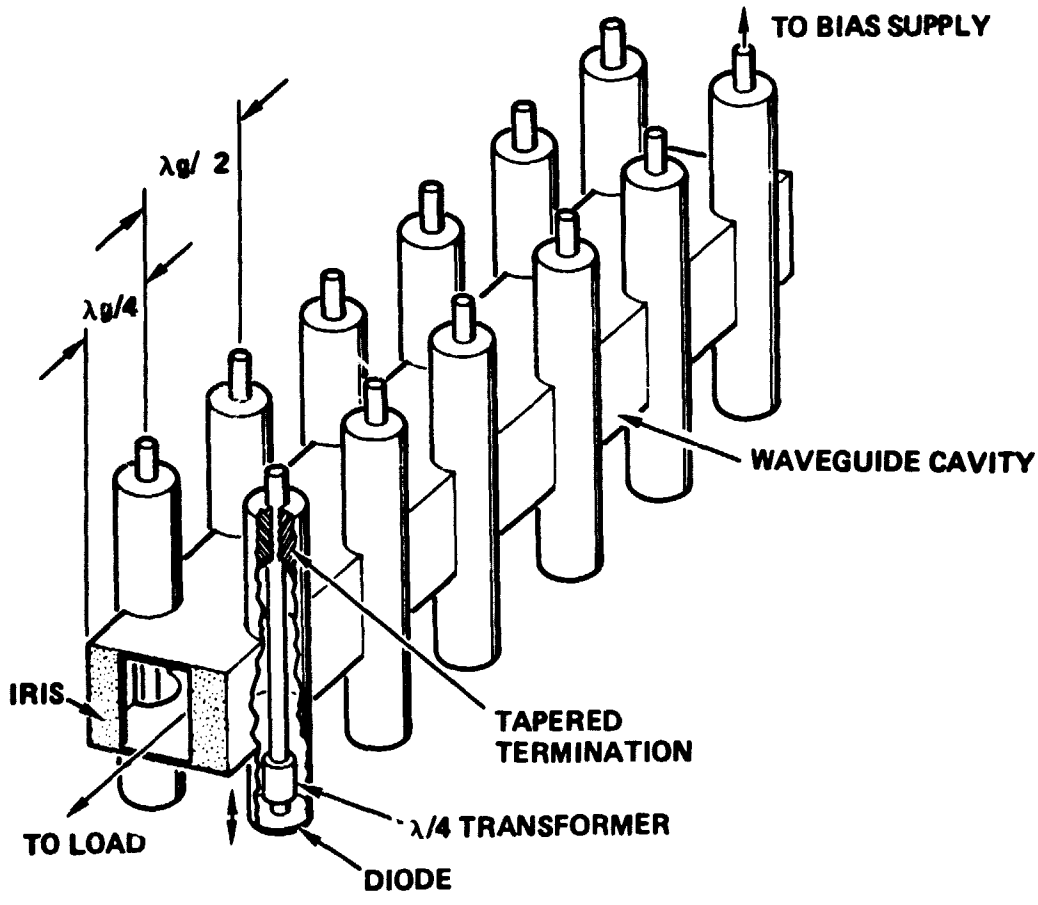


FIGURE 5-8. TWELVE-DIODE KUROKAWA COMBINER SCHEMATIC

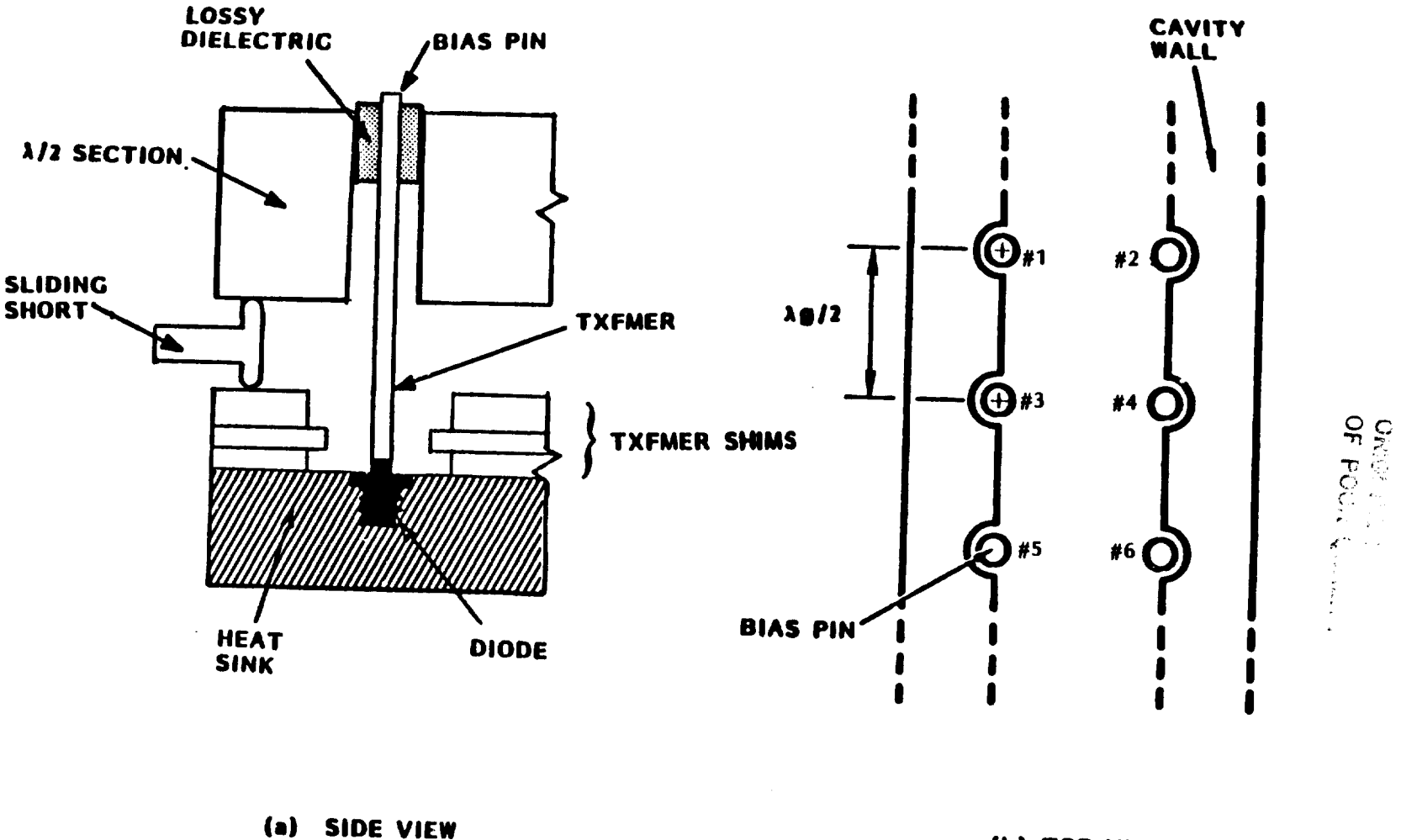
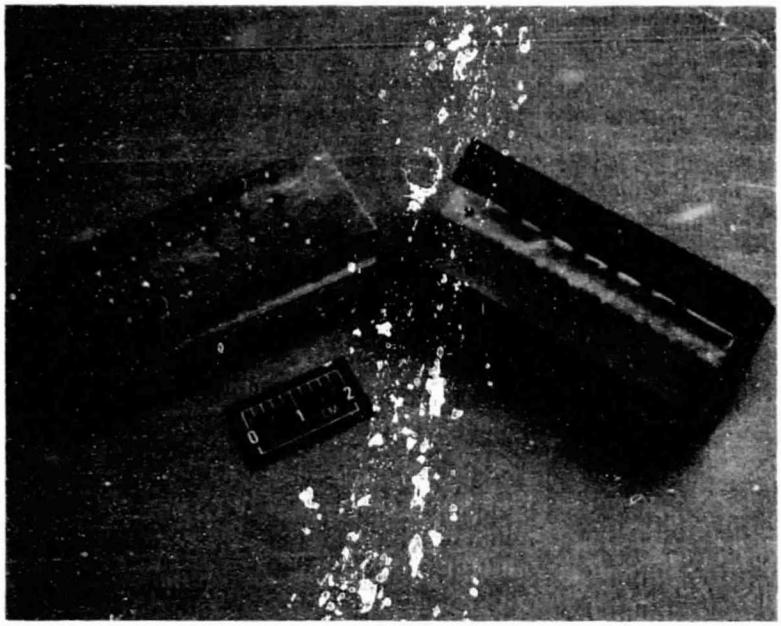


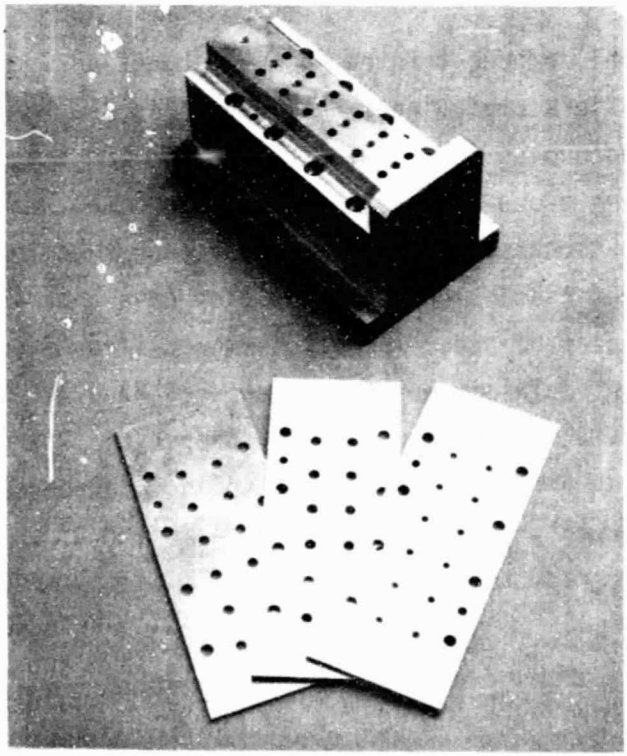
FIGURE 5-9. CONSRTRUCTION OF WAVEGUIDE CAVITY COMBINER

The transformer around the diode consists of a high impedance section, followed by a low impedance section, and then another high impedance section. The last high impedance section is approximately $\lambda/2$ from the center of the waveguide. This configuration was obtained experimentally and has been proven to be extremely reproducible. In the bias port, a half-wave section (with air as the dielectric) is used before the bias port is terminated by lossy dielectric (Eccosorb MF124). This arrangement has the merit that at the resonant frequency, the half-wave section behaves as a series resonator and is essentially a short circuit. The diode sees the load and the bias termination in series. Since the bias termination is designed to have a relatively low impedance, most of the RF power is delivered to the waveguide load. At spurious frequencies, including subharmonics, the half-wave section exhibits a high impedance, making the oscillation condition for the diode unfavorable. Spurious oscillators and other instabilities are thereby avoided or minimized. The actual hardware for the 12-diode combiner used on the output stage is shown in Figures 5-10(a) and (b). The individual components are readily identifiable.

In tuning up the 12-diode power combiner, it was found that a necessary condition for achieving efficient combining is to have each pair of diodes exhibit nearly identical rf characteristics when tested separately in a two-diode test fixture. Let us refer to Figure 5-9. Suppose diode pair #1/#2 exhibited 3.5 W of combined power at 30 GHz in a two-diode test cavity, and that diode pair #3/#4 exhibited 4.0 W of combined power at about the same frequency. (Experimentally, it was found that if the frequencies between the two pairs are under 200 MHz apart, there is virtually no difficulty in combining the four diodes.) Then, when these four diodes were tuned in a four-diode combiner with the correctly designed spacing between pairs, the pairwise output power values are additive, resulting in a four-diode combiner output of 7.5 W. The combiner efficiency, typically 80 percent, is entirely accounted for in the pairwise combining. This aspect has proven to be valid up to 16 diodes.



(A) DISASSEMBLED TOP AND BOTTOM HALVES



(B) ASSEMBLED COMBIMER AND ASSOCIATED SHIMS

FIGURE 5-10. POWER COMBINER HARDWARE

Another interesting aspect of the Kurokawa combiner is the effect of iris size on the combiner behavior. The type of iris being used in the combiner is inductive, i.e., the height of the iris is equal to the waveguide height, while the width is smaller than the waveguide width and is a variable. For a particular number of diodes in the combiner, there is a unique iris width which yields the maximum free-running output power and injection-locking bandwidth. If the iris width were increased further beyond the optimum size, then there is a point at which the combiner will cease free-running oscillation, but will put out power for a certain minimum level of input rf power. In this case, the combiner becomes a quasi-stable amplifier. If the input drive to the combiner via the circulator is in pulsed or burst form, then the output power of the combiner is also in pulsed or burst form. We have successfully used this phenomenon to achieve a 20 W solid state amplifier which can be operated in burst mode for TDMA applications. The measured performance characteristics are presented in Section 7.

5.3 CIRCULATORS

One essential component found in most injection-locking oscillators or reflection amplifiers employing IMPATT diodes is the three-port circulator. The circulator decouples the input circuit from the output circuit and, in effect, transforms a one-port network into one with two ports. Since both the input and output signals are transmitted through the circulator, the electrical characteristics of the circulator have a profound influence on the overall circuit performance. The requirements imposed on the circulators are stringent. The circulators must be capable of handling the signal power and have a wide bandwidth (with low SWR) for proper circuit operations and an adequate isolation for input/output decoupling. Moreover, the circulators must have an extremely low insertion loss - in the vicinity of 0.2 dB - so as not to further degrade the relatively low efficiency of IMPATT devices.

The development of high performance circulators was initiated at TRW in 1974. A market search had disclosed that even on special order, state-of-the-art circulators were totally inadequate for our purposes and an R&D effort was initiated to develop a low loss circulator at Ka-band. What appeared at that time as a technically ambitious task resulted not only in a device with performance characteristics far exceeding the original goals, but also led to several significant advances in ferrite component technology. Among these were improvements in analytical design methods and a better understanding of ferrite material applications, resulting in a high degree of control over performance parameters, such as insertion loss, power capacity, and thermal stability. The improvements in structural design resulted in much higher reliability components which totally outperformed, under shock and vibration, the epoxy-bonded, triangular junction designs common to the industry.

A detailed graphic representation of the TRW circulator junction is depicted in Figure 5-11. The junction consists of two ferrite discs, two dielectric spacers, a septum in the center of the cylinder dividing the junction into two turnstiles, and a dielectric tube enclosing the above parts.

Figure 5-12 indicates the electrical performance of a Ka-band TRW circulator. The upper curve represents the VSWR data and the lower curve the insertion loss data. It can be seen that for a VSWR of 1.2, the circulator has a passband from 27 to 35 GHz - a bandwidth of 8 GHz. The insertion loss in the passband is less than 0.2 dB. Figure 5-13 shows the circulator assembly used in the program. The assembly consisted of four circulator junctions in a common housing.

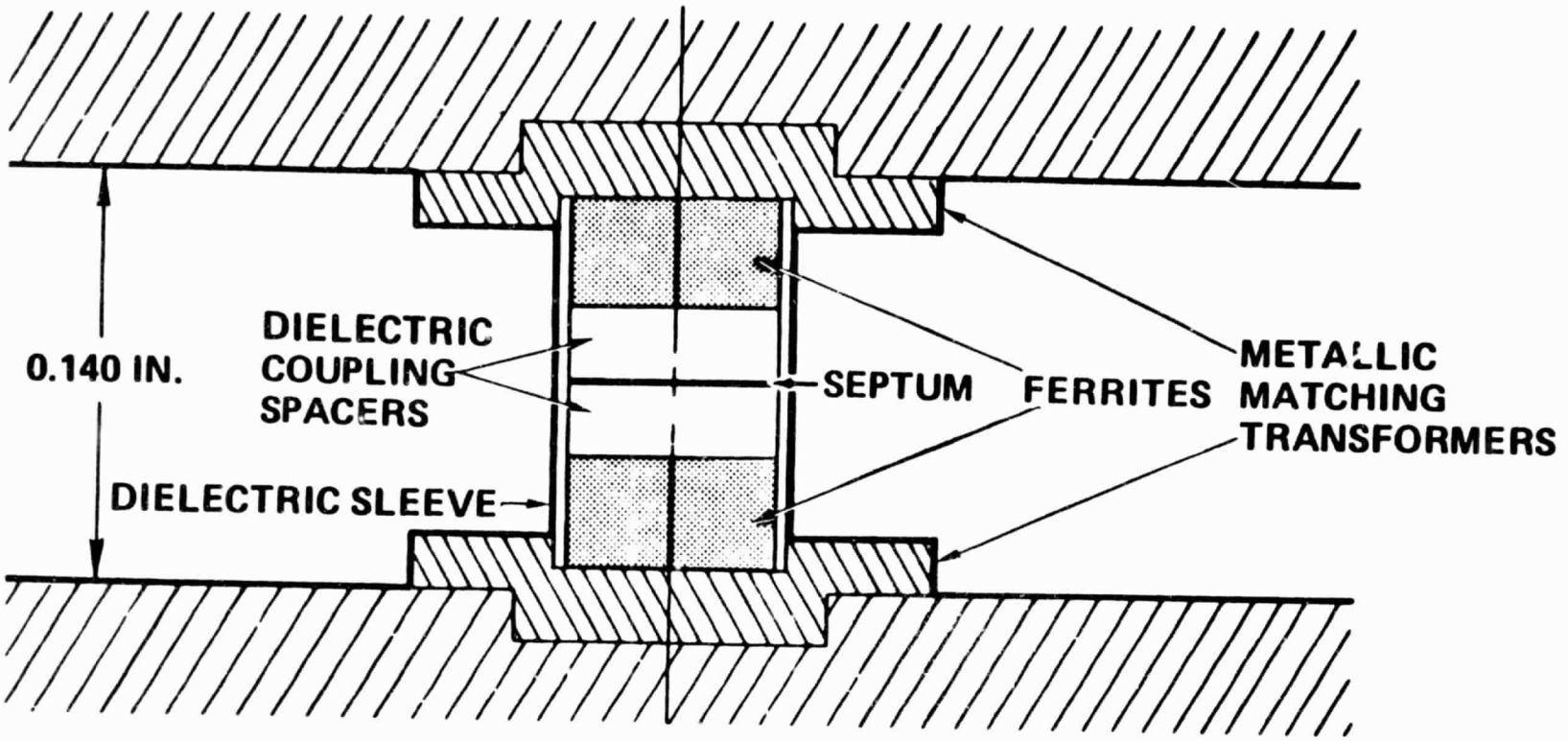


FIGURE 5-11. GRAPHIC REPRESENTATION OF CIRCULATOR JUNCTION

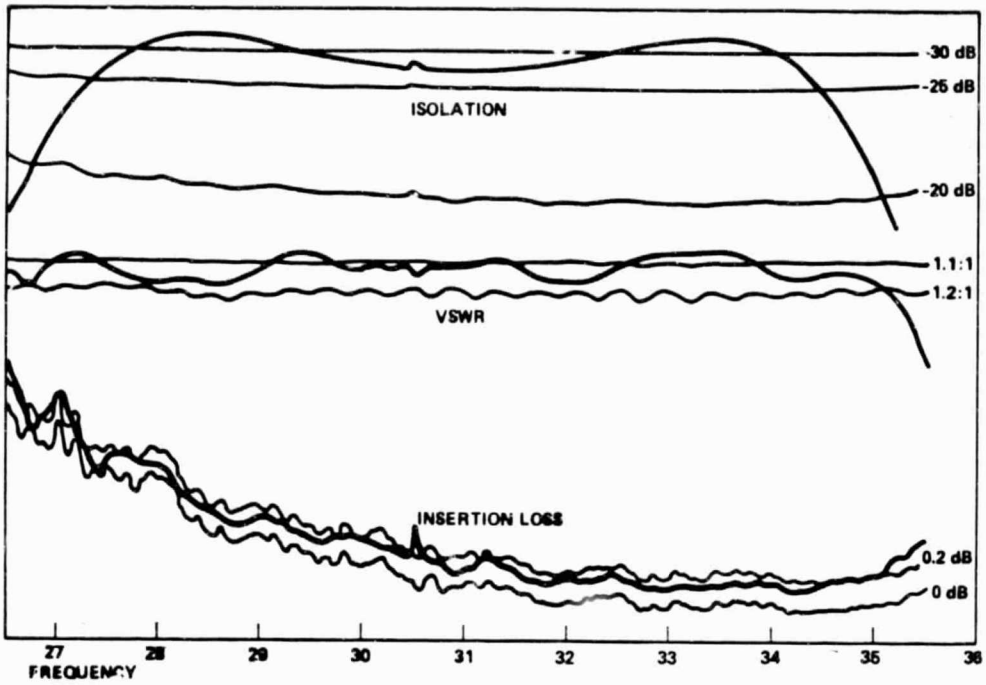


FIGURE 5-12. KA-BAND CIRCULATOR PERFORMANCE

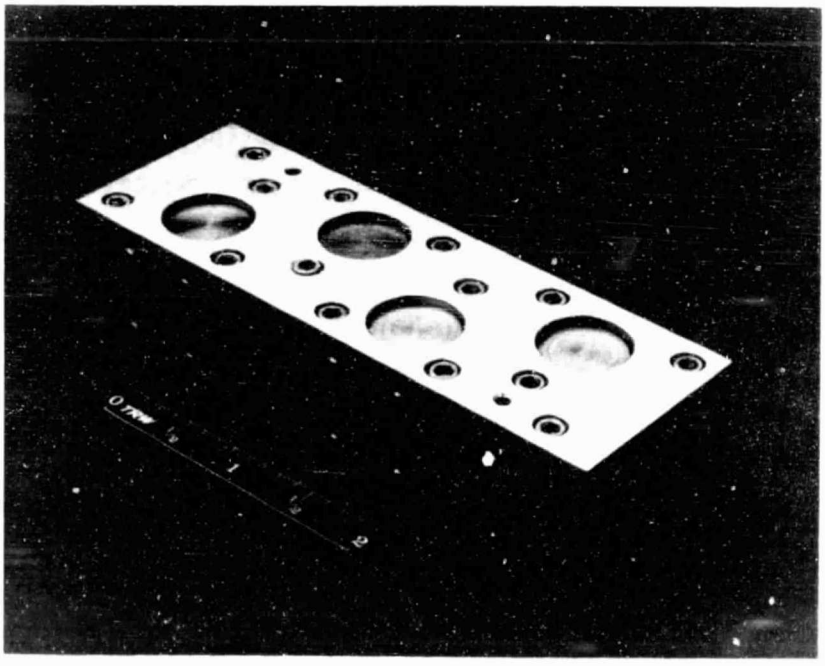


FIGURE 5-13. FOUR-JUNCTION KA-BAND CIRCULATOR

5.4 BIAS REGULATORS

The bias circuit for CW IMPATT diodes is essentially that of a current regulator (constant current source). One current regulator is needed for each CW IMPATT diode. Due to their numerous applications, current regulators of various capacity and capability have been produced by the industry in IC (integrated circuit) form. These ICs are available in large quantity at low cost.

One regulator suitable for our application in the program is the LM117HVH, manufactured by the National Semiconductor Corporation. This regulator offers internal current limit, thermal overload protection, and safe-area protection to ensure high reliability. The internal circuitry of the regulator is provided in Figure 5-14. The circuit is quite complete. Only three external components, namely, a potentiometer, a resistor, and a capacitor, are needed to connect the regulator as an adjustable constant current source. The IC can operate in a temperatue range of -55°C to +150°C. Line regulation is typically 0.005 percent; load regulation is typically 0.1 percent.

Because a minimum of 12 regulators are required for the POC amplifier, we decided from early on in the program that the regulator circuitry should be of multichannel construction with a compact mechanical design. Instead of the more widely used TO-3 IC package, we have chosen to use the much smaller TO-39 package. A comparison in size between the two is shown in Figure 5-15. Using the TO-39 packages, Figure 5-16 shows a photograph of a 14-channel PC board on which are mounted three TO-39 cans. Figure 5-17 shows a schematic diagram of the complete packaging configuration.

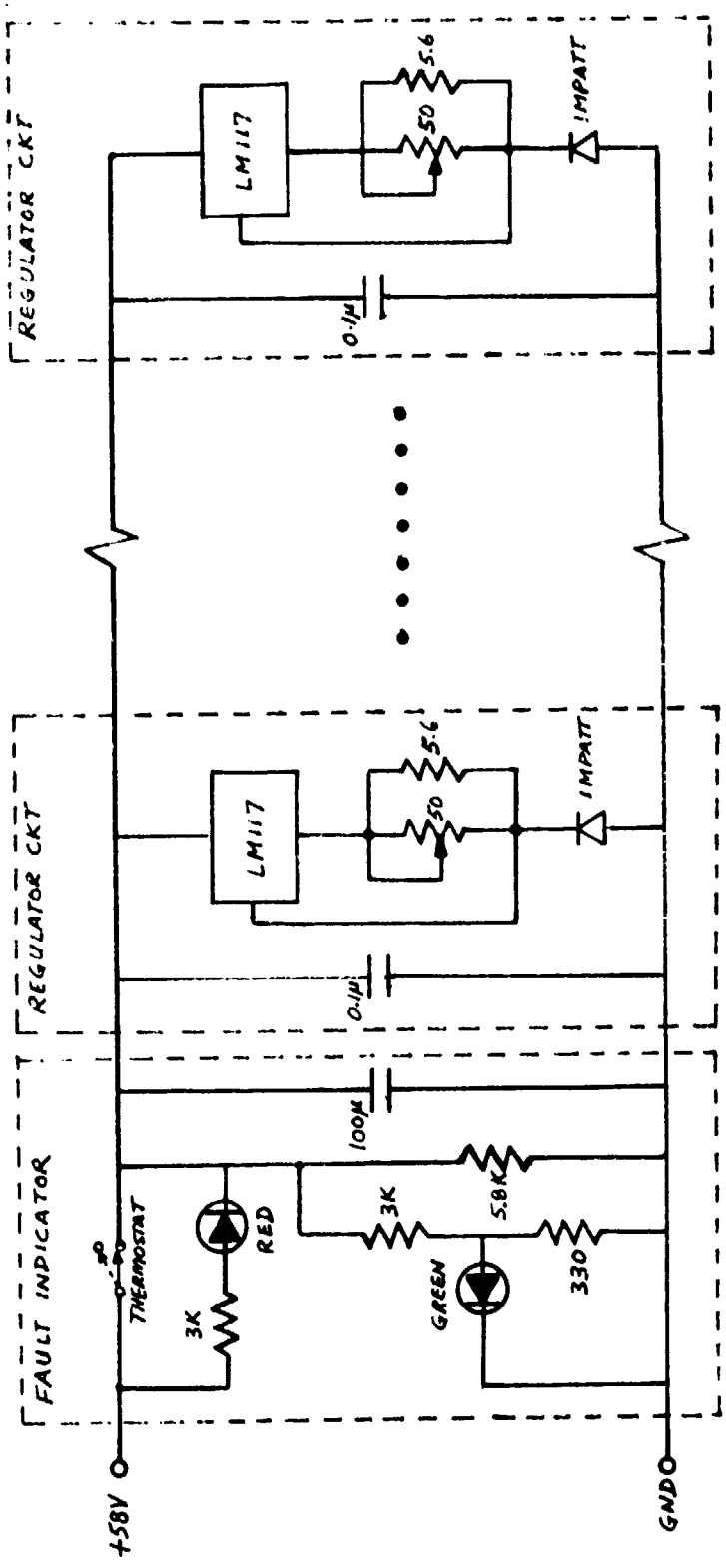


FIGURE 5-14. MULTICHANNEL CURRENT REGULATOR CIRCUIT WITH FAULT INDICATOR AND OVER-TEMPERATURE PROTECTION

FIGURE 5-15. COMPARISON BETWEEN TO-3 PACKAGE AND TO-39 PACKAGE OF AN LM117 IC

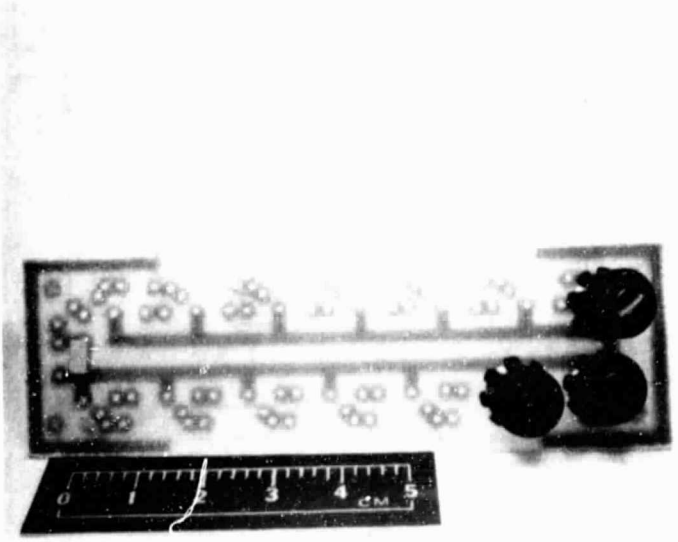


FIGURE 5-16. MULTICHANNEL REGULATOR PC BOARD

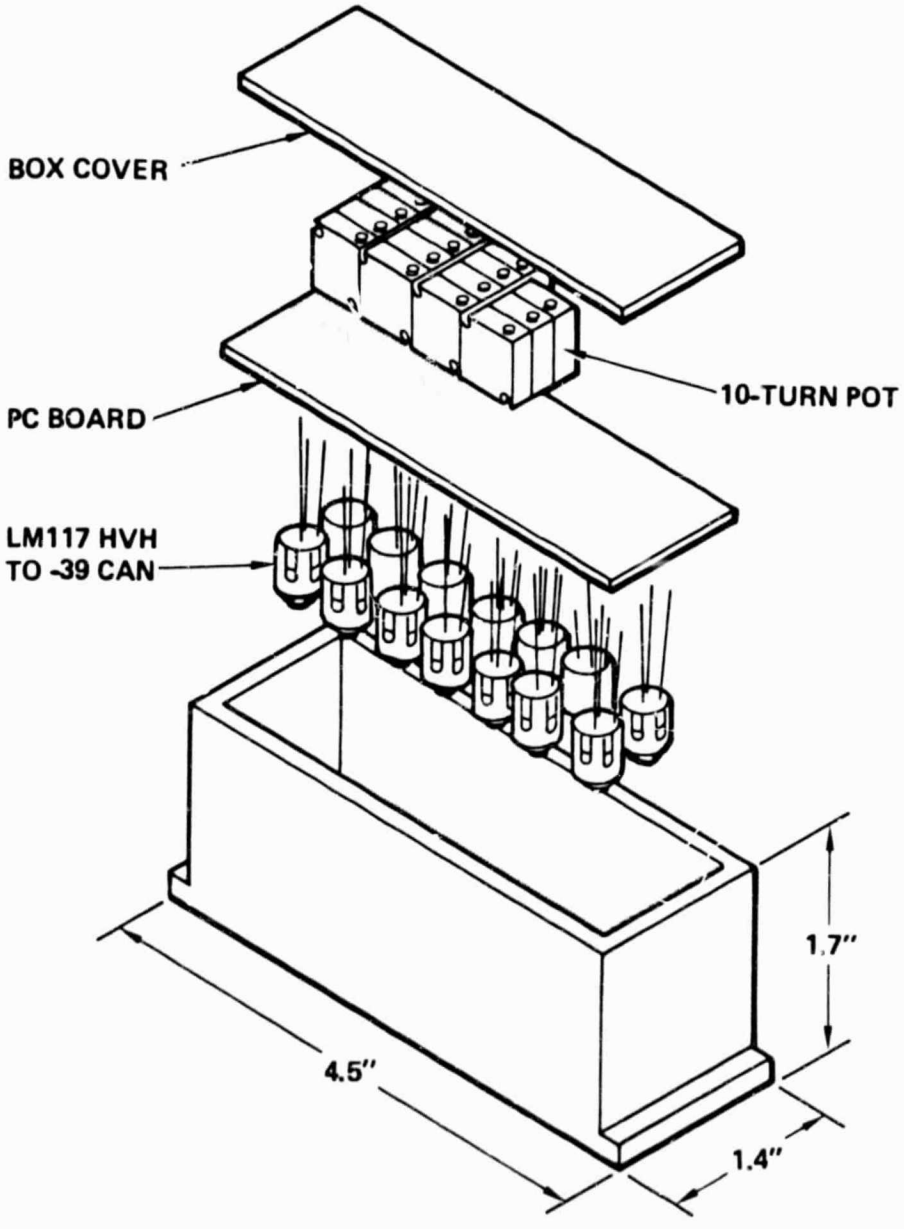


FIGURE 5-17. REGULATOR MODULE CONSTRUCTION

5.5 PULSE MODULATOR

From the system discussion in Section 3, we have, under this program, carried our POC model development work further and produced a high power amplifier amenable to burst mode operation. This is accomplished by creating a pulse rf output from the single-diode driver through pulse modulation of its bias current. The key to this development is a high speed pulse modulator whose photograph is shown in Figure 5-18. High speed VMOS FETs are used in this design. Figure 5-19 shows the circuit schematic. The function of the lower half of the circuit is to provide a constant 330 mA into point A via the +62 V line as indicated at the right side of the circuit. The upper half of the circuit provides the switching mechanism to direct this current either into the IMPATT diode or into ground. The mode selection switch at the upper left-hand-side performs three functions. In the CW mode, F_1 is turned on and F_2 is turned off, resulting in having the IMPATT diode biased at full current level at all times. In the OFF mode, F_1 is turned off and F_2 is turned on, resulting in having 90 percent of the current at A channelled through resistor R4 and then to ground, with a small portion (~30 mA) maintained through the IMPATT diode, which essentially will not cause the IMPATT to oscillate. The pulse mode is simply an alternation between the CW mode and OFF mode, controlled by a 5 V TTL signal. The advantage of maintaining a small current through the IMPATT is that it results in a low level heating of the diode junction, which minimizes the transient thermal excursion as the diode is biased from zero power to full power. This in turn minimizes the rise time of the RF pulse.

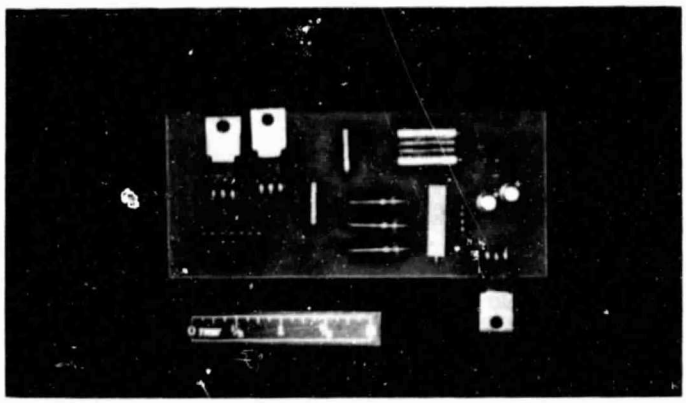


FIGURE 5-18. PULSE MODULATOR CIRCUIT

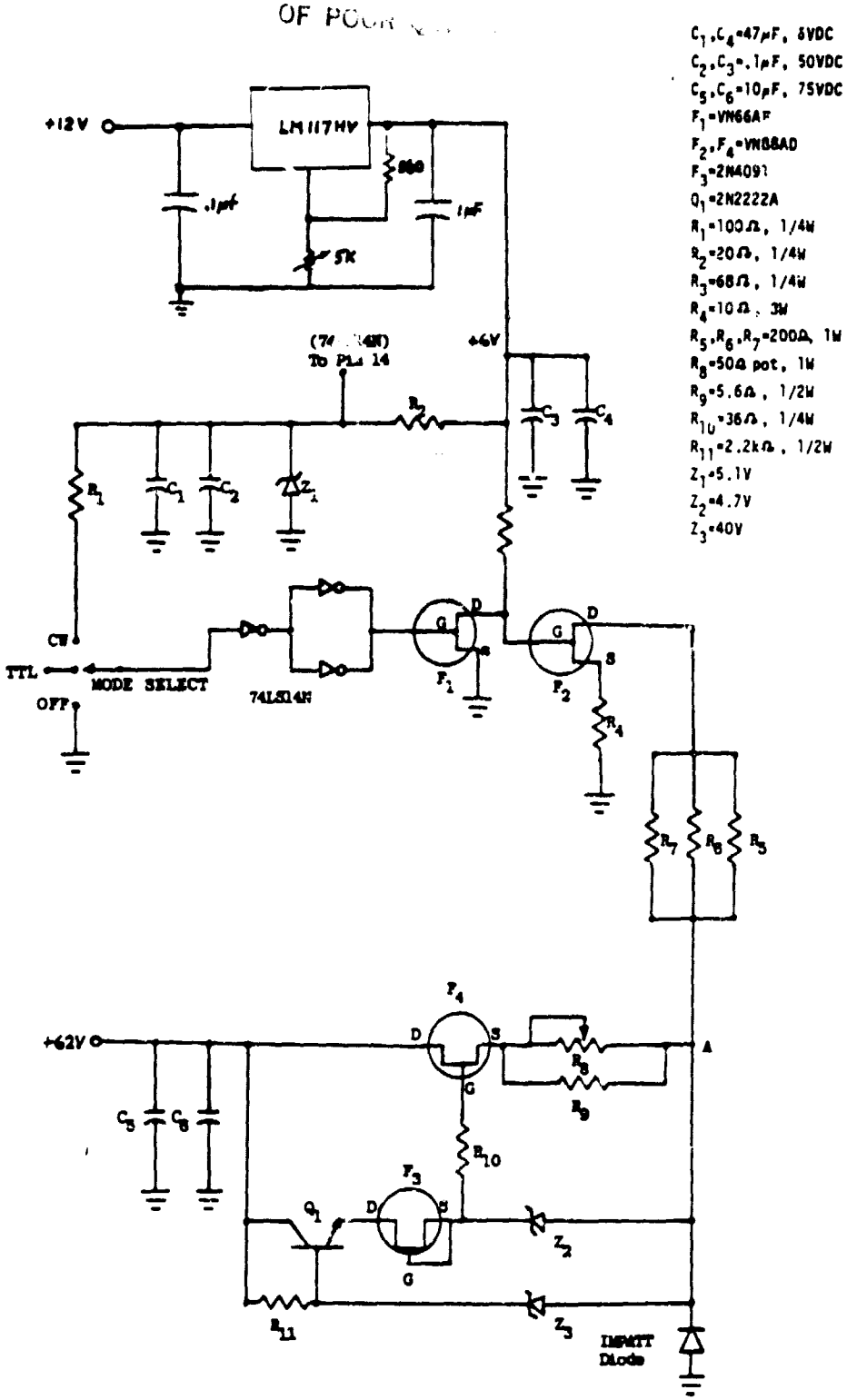


FIGURE 5-19. PULSE MODULATOR CIRCUIT SCHEMATIC

SECTION 5 REFERENCES

1. R. Adler, "A Study of Locking Phenomena in Oscillators," Proc. IEEE, Vol. 34, pp. 351-357, June 1946.

2. K. Kurokawa, "Injection Locking of Microwave Solid State Oscillators," Proc. 1EEE, Vol, 61, pp. 1386-1410, October 1973.

3. K. Kurokawa, "Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits," BSTJ, Vol. 48, pp. 1937-1955, July-August 1969.

4. Kai Chang and Roy L. Ebert, "W-Band Power Combiner Design," IEEE Trans. Microwave Theory Tech., Vol. MTT-28, April 1980, pp. 295-305.

5. R. L. Eisenhart and P. J. Kahn, "Theoretical and Experimental Analysis of a Waveguide Mounting Structure," IEEE Trans. Microwave Theory Tech., Vol. MTT-19, August 1971, pp. 706-719.

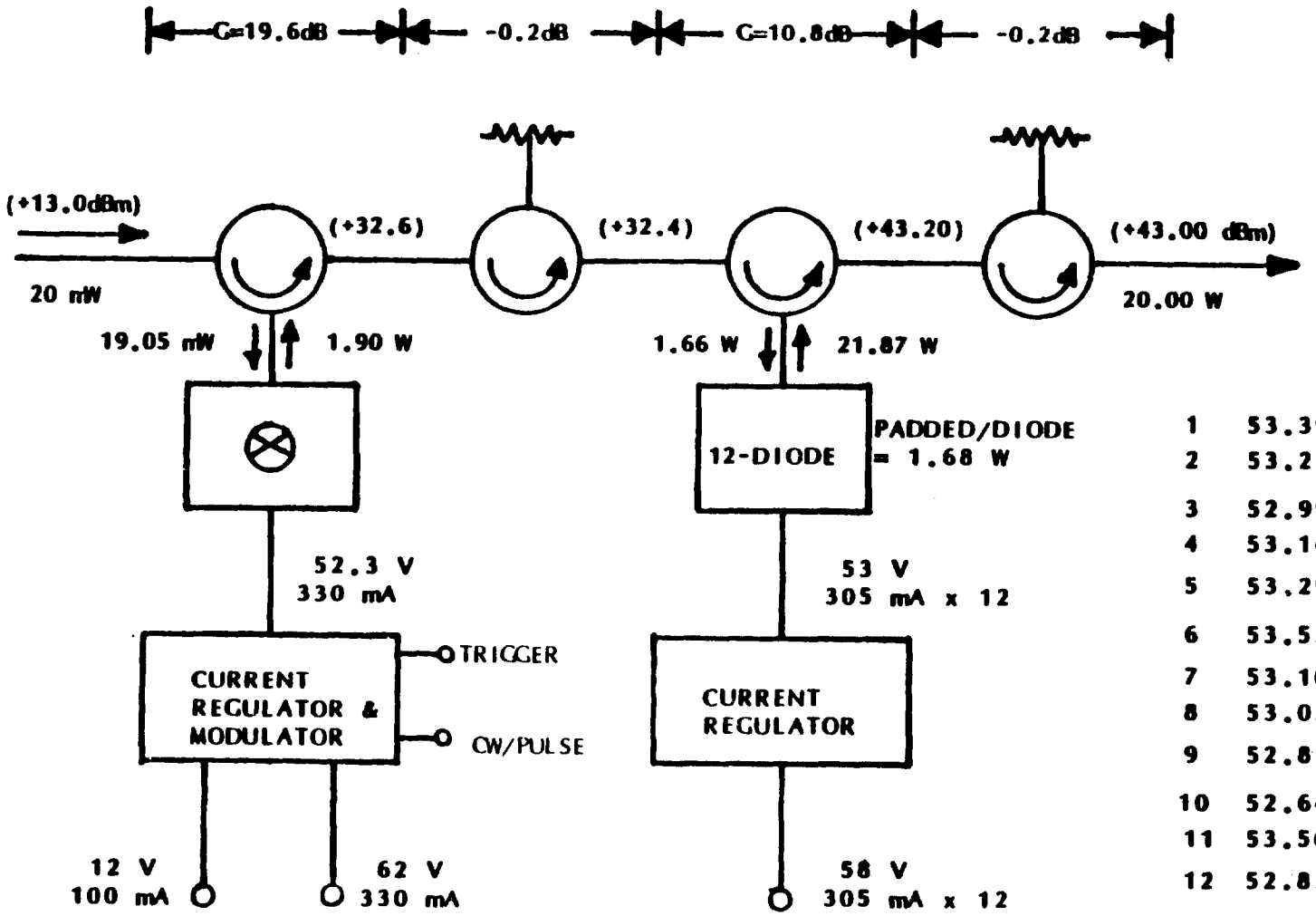
6. AMPLIFIER INTEGRATION

6.1 SYSTEM SCHEMATIC

The system schematic of the entire amplifier is shown in Figure 6-1. The system consists of one four-junction circulator assembly, two IMPATT stages, twelve current regulators, one pulse modulator, and a forced air cooling unit. The circulator assembly, the IMPATT stages, the current regulators, and the pulse modulator have been described in Section 5. There are three DC voltages required to power the amplifier, namely, +62 V, +58 V for the combiner, and +12 V for the modulator. All thirteen double-drift IMPATT diodes require operating voltages in the vicinity of 54 V. Consequently, up to +62 V is required to power the amplifier. For the pulse modulator, an additional 12 V DC input is required to power the TTL circuit. If only the 62 V supply were used, excessive voltage drop through a voltage dividing circuit will be required to arrive at +58 V and +12 V, resulting in an unnecessarily large heat dissipation. The forced air cooling unit operates from 110 VAC prime power and provides an air flow of 110 CFM through a heat exchanger unit on which the amplifier is mounted. The amplifier is also provided with an over-temperature shut off capability. When the temperature of the combiner reaches above 70°C, all DC current will be shut off and a red pilot will light up. When the amplifier is operating, a green light will light up instead.

6.2 PHYSICAL DECRIPTION

All components of the amplifier are attached to a common baseplate by screws. The component layout of the unit can be seen from the photograph of Figure 6-2. The components which are contained in the system schematic (Figure 6-1) are readily identifiable from the photograph and no further elaboration is needed. The advantage of this layout is that only the baseplate is required to be mechanically sturdy and that heat removal can be done through the same baseplate. The baseplate dimensions are 22.8 cm (9.0")



1	53.39V	304 mA
2	53.25V	305 mA
3	52.99V	305 mA
4	53.16V	304 mA
5	53.29V	304 mA
6	53.55V	304 mA
7	53.10V	304 mA
8	53.03V	306 mA
9	52.83V	304 mA
10	52.64V	304 mA
11	53.50V	303 mA
12	52.83V	305 mA

FIGURE 6-1. POC AMPLIFIER FUNCTIONAL BLOCK DIAGRAM

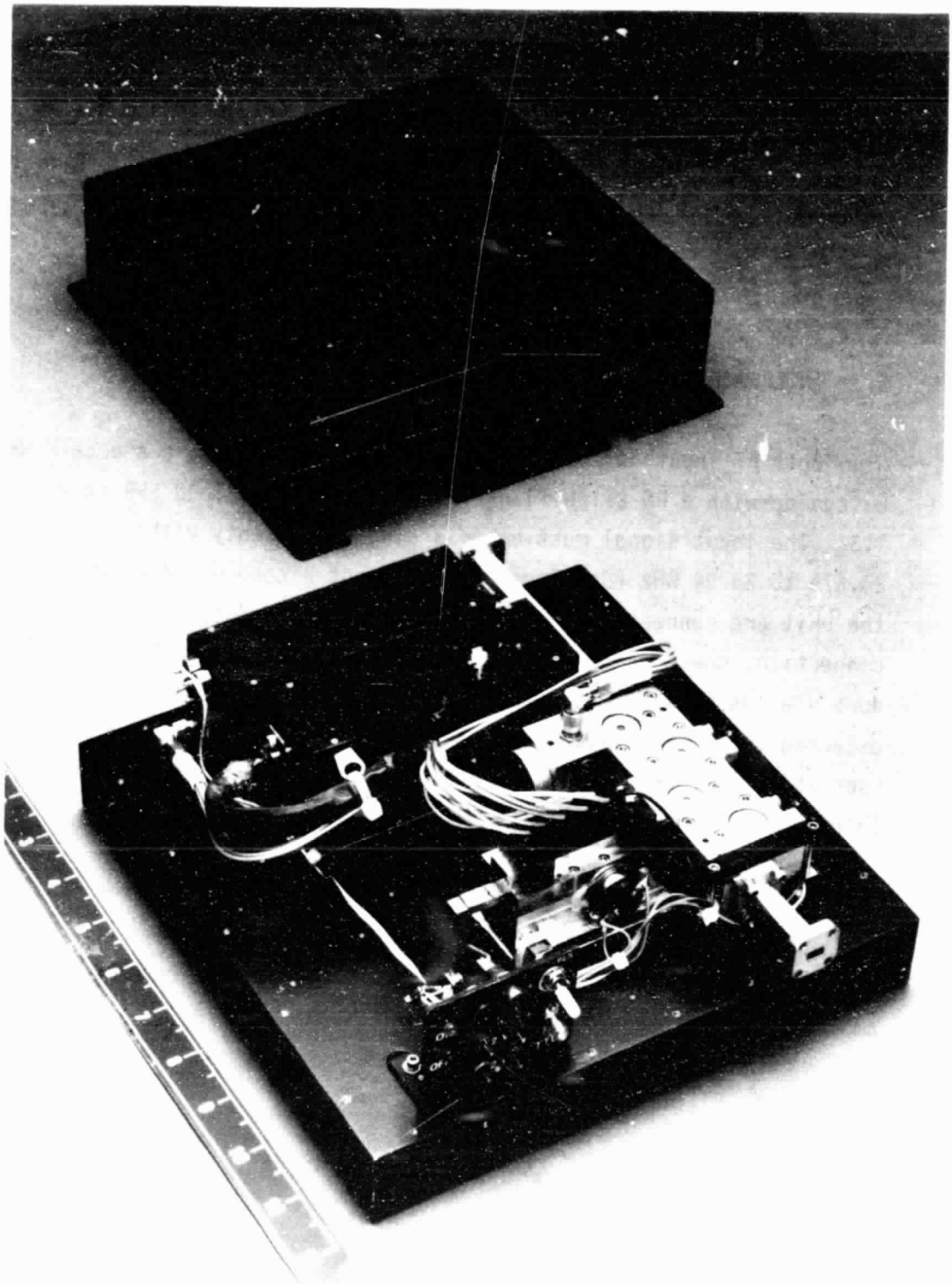


FIGURE 6-2. PHOTOGRAPH OF POC AMPLIFIER

square. The entire unit measures 9.53 cm (3.75") tall with the amplifier cover on. A forced air cooling unit is also provided with the amplifier. The amplifier is mounted into the cooling unit via six side screws. A photograph of the amplifier unit together with the forced air cooling unit is shown in Figure 6-3. The amplifier unit weighs approximately 18 pounds with the cover on.

6.3 INTERFACE REQUIREMENT

Both RF input and output connections are done via a standard WR-28 waveguide with a RG 271/U flange. The source and load SWR should not exceed 1.3. The input signal must be of a single frequency within the range from 28.675 to 28.94 GHz (see Section 7) and not exceed 0.064 W CW. DC inputs to the unit are connected through standard banana jacks, one jack for the +62 V connection, one for +58 V, and one for +12 V. The cooling of the amplifier is done via the cooling unit provided. Alternately, the amplifier unit can be detached from the cooling unit and mounted on any structure provided by the user which is conformal to the baseplate of the amplifier and has similar thermal dissipation characteristics as the cooling unit.

6.4 MECHANICAL DRAWINGS

Some relevant mechanical drawings of the various components of the amplifier are shown in Appendix A.

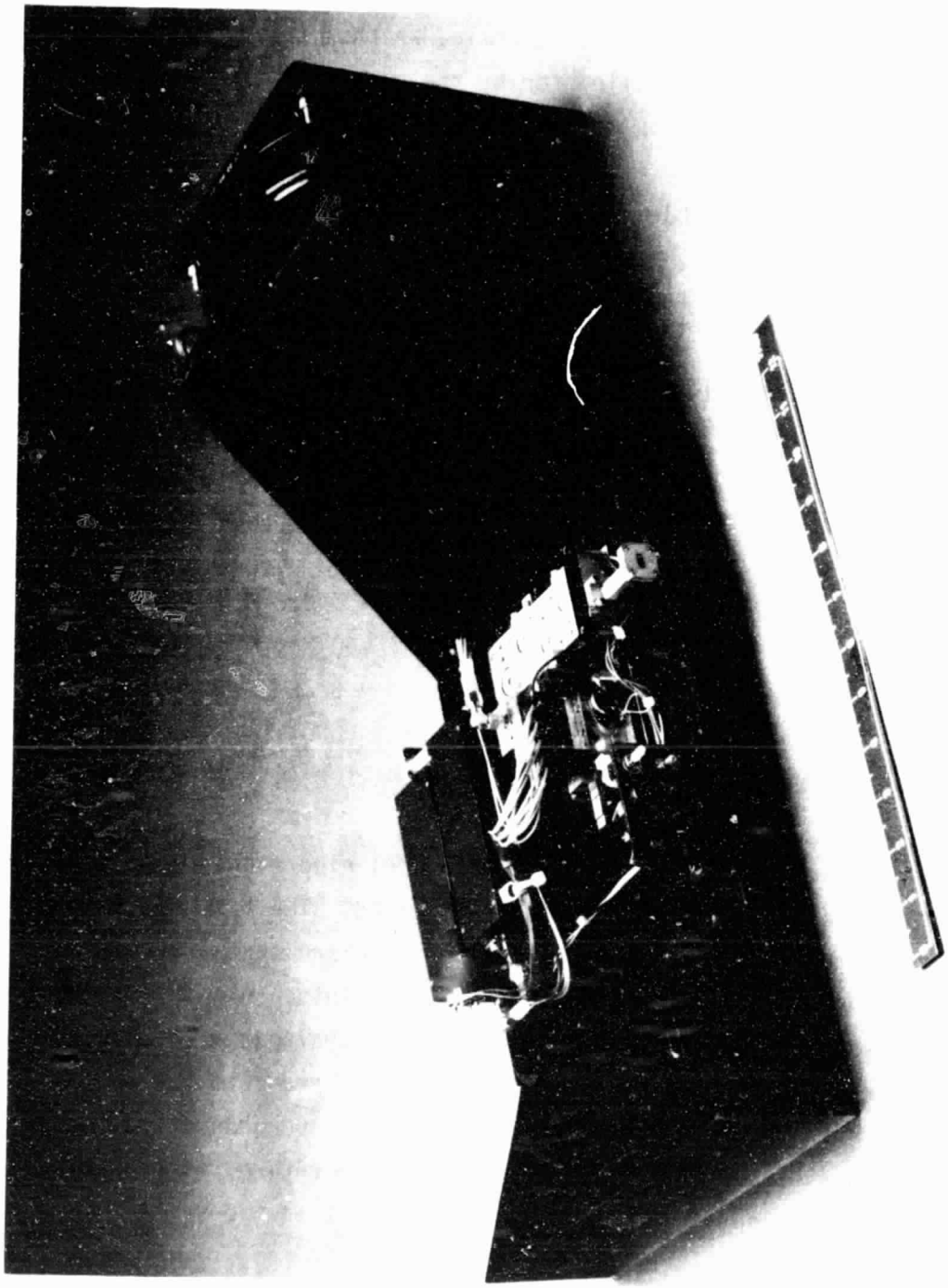


FIGURE 6-3. PHOTOGRAPH OF FOC AMPLIFIER MOUNTED IN HEAT EXCHANGER

7. AMPLIFIER PERFORMANCE EVALUATION

The test objectives are to determine whether the POC model is meeting the performance requirements called for by the contract. The requirements are identified in Table 7-1.

Table 7-1. PERFORMANCE REQUIREMENTS

RF Output Power	20 W CW Min
RF Band	28.5 to 29.0 GHz
RF Bandwidth	50 MHz
RF Power Gain (50 MHz)	30±1 dB per MHz Maximum
Gain Variation	≤+0.5 dB
Gain Slope (50 MHz)	≤+0.15 db per MHz Maximum
Phase Linearity (50 MHz)	≤10° P-P Deviation Maximum
Harmonic Response	-50 dBc Minimum
Spurious Response	-60 dBc Minimumn
Overdrive Capacity	+ 5 dB Nominal

7.1 MEASUREMENT IDENTIFICATION

To adequately characterize the POC model electrical performance, five different measurements (or tests) are required. The five measurements are listed in Table 7-1. Also listed in the table are the parameters which can be evaluated using data from the various measurements. As can be seen, the parameters in the table identify totally with the specifications listed above. All measurements listed in the table can be grouped into scalar measurements, vectorial measurements, and noise measurements. Consequently, only three different test setups are needed to perform the entire task. The test setup and test methodology are described in subsequent sections.

TABLE 7-1. POC MODEL TESTS/MEASUREMENTS

Tests/Measurements	Resulting Data for Evaluation
1. Output Power vs. Input Power	Output Power, Gain of Amplifier
2. Output Power vs. Frequency	Bandwidth, Gain Variation, Gain Slope
3. Output Spectrum	Power Levels of Coherent and Noncoherent Components
4. Output Phase vs. Frequency	Phase Linearity
5. Noise Measurements	AM/PM Noise Performance

3. TEST AND CORRECTIVE ACTION SEQUENCES

It should be noted that some measurements cannot be performed until other measurements are completed. Figure 7-1 contains a test sequence which shows the proper order of each measurement. Also shown in Figure 7-1 is the corrective action sequence. In the event that the POC model fails to meet the test objective, a diagnosis is performed to determine whether a readjustment or a redesign is necessary to improve the amplifier performance. Upon taking the corrective action, the test cycle is repeated.

7.2 MEASUREMENT DATA EVALUATION

7.2.1 RF Output Power

The RF output power of the amplifier was measured as a function of RF frequency. Three responses were recorded, namely, (a) the driver stage alone,

(b) the output stage alone, (c) the driver stage and output stage in cascade.

The test setup is shown in Figure 7-2. Since the amplifier will be operated in the injection-locking mode, a sweep source which has enough power to drive either the driver or the combiner is required. The HP sweeper unit and the Hughes TWT unit together accomplish this requirement very nicely. The TWT can put out as much as 2W rf output power, which is more than adequate to drive the combiner, according to the POC model gain budget design. By putting a variable attenuator at the TWT output port, the required +13 dBm (plus 5 dB nominal overdrive capability) for the POC amplifier can also be achieved. A power meter monitors the output power and a spectrum analyzer monitors the output spectrum.

Figure 7-3 a) and b), show the output characteristics of the drive stage for + 13 dBm, and + 18 dBm input. It is seen that the total locking bandwidth widens as the input power is increased, which is expected from injection-locking theory. Figure 7-4 is a plot of percentage locking bandwidth as a function of gain. The linear response is closely followed, with an external Q of about 20.

Figure 7-5 a), b), and c) show the CW output power of the complete two-stage amplifier when driven by + 8 dBm, + 13 dBm, and + 18 dBm, respectively. It is seen that because of the particular frequency alignments between the driver and the combiner, the increase in input drive only affects the upper end of the frequency range. Between 28.675 GHz and 28.75 GHz, an output power of 20 W (+43 dBm) was achieved, with less than 0.1 dB power and gain variation. The total locking band of the amplifier is from 28.675 GHz to 28.94 GHz, or a locking bandwidth of 265 MHz, which, when compared with the theoretical prediction of 237 MHz, shows exceptional agreement. Over the locking band, the gain or power variation is only within 1 dB.

7.2.2 RF Frequency

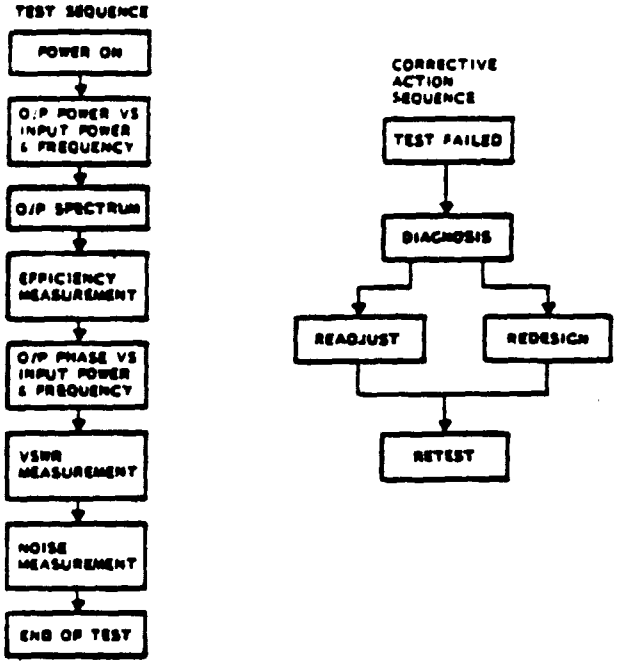


FIGURE 7-1 TEST AND CORRFCTIVE SEQUENCE

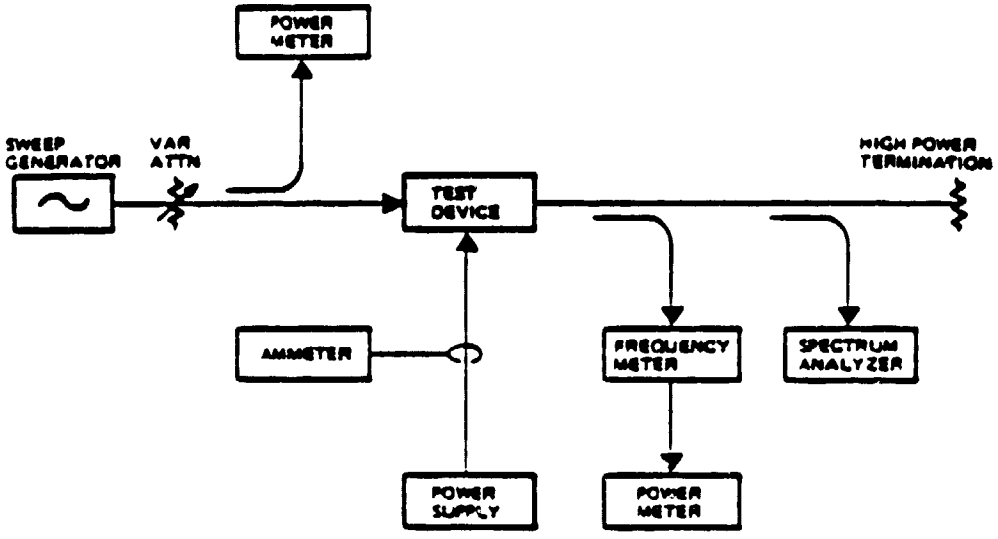
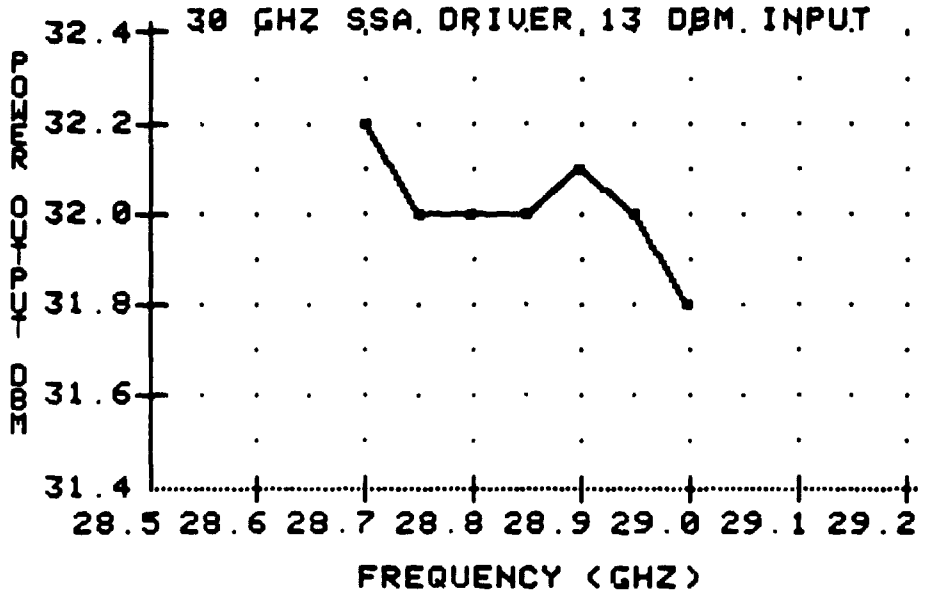


FIGURE 7-2 SCALAR MEASUREMENT TEST SETUP



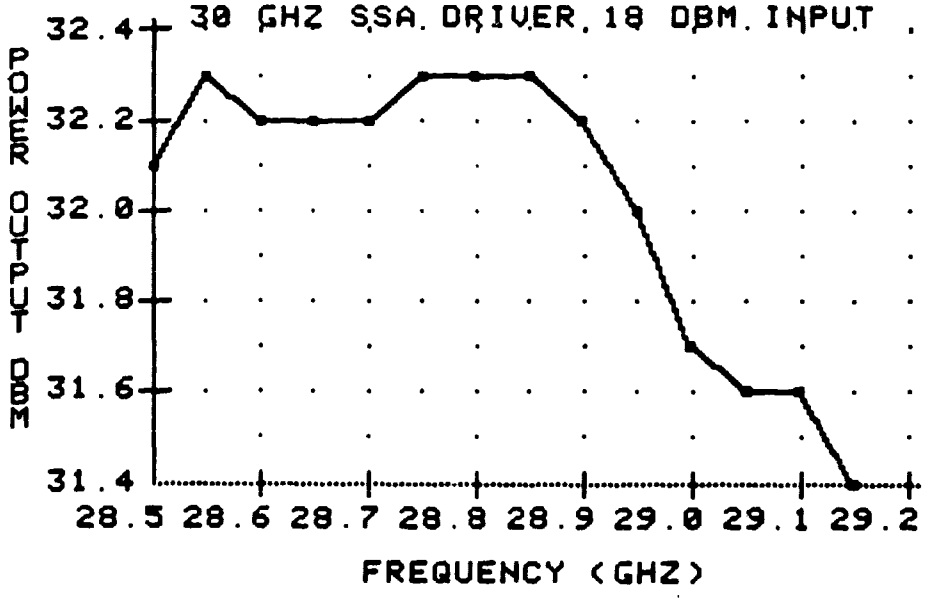


FIGURE 7-3 OUTPUT CHARACTERISTICS OF DRIVER AMPLIFIER FOR TWO DIFFERENT INPUT POWER LEVELS (+13 dBm AND + 18 dBm).

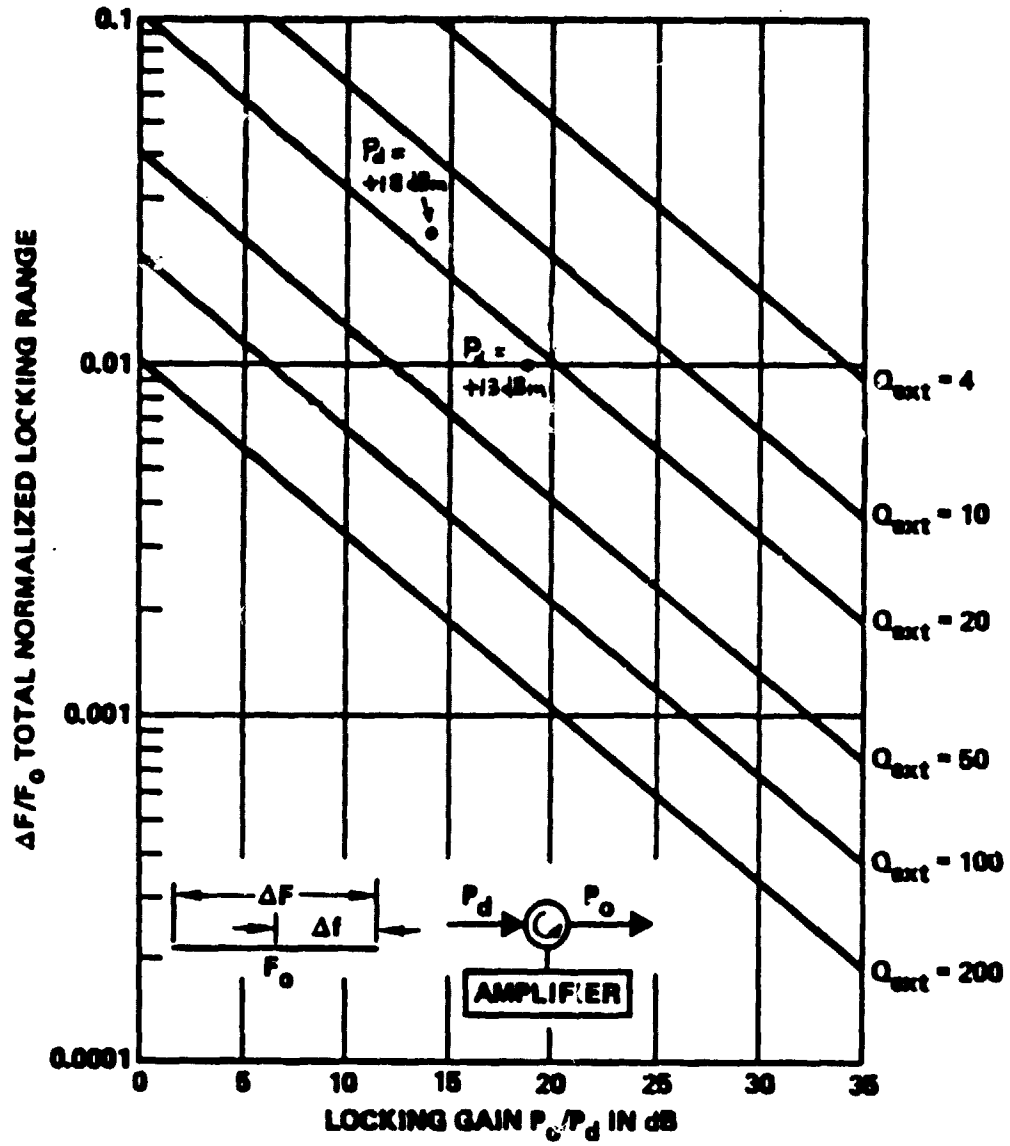


FIGURE 7-4 INJECTION LOCKING CHARACTERISTICS OF DRIVER AMPLIFIER, SHOWING A Q_{ext} OF 20

RF frequency is measured by a resonance- diP frequency meter. Bandwidth can be determined by observation with the help of a spectrum analyser. When the amplifier just broke out of lock, a "fence-spectrum" can be observed. This allows one to determine to lower and upper locking limits.

7.2.3 RF Power Gain, Gain Variation, and Gain Slope

Power gain is calculated by subtracting the input power (in dBm) from the output power (in dBm). Over the frequency range from 28.675 GHz to 28.75 GHz (or 75 MHz bandwidth), a gain of 30 dB $^{+0\ dB}_{-0.1\ dB}$ was achieved. Over the entire locking hand, a gain of 30 dB $^{+0dB}_{-1.0\ dB}$ was achieved. From Figures 7-5 a), b), or c), the maximum gain slope was seen to be < 0.01 dB/MHz.

7.2.4 Overdrive

The performance of the amplifier as described in Sections 7.2.1, 7.2.2 and 7.2.3 clearly indicates a +5 dB overdrive capacity.

7.2.5 Phase Linearity

Consider a two-port system with an input signal of phase φ_1, and an output signal of phase φ_2. If the system is linear, then the diffenital phase shift ($\varphi_2 - \varphi_1$) is proportional to the frequency f. In other words,

$$\varphi_2 - \varphi_1 = Af$$

where A is a proportionality constant independent of frequency

For any dispersive system, the differential phase shift is not a linear function of frequency, as shown schematically in Figure 7-6. The resultant deviation from linearity is defined in the Figure in relationship to a least-square fit.

Figure 7-7 shows the block diagram of the phase bridge used to measure

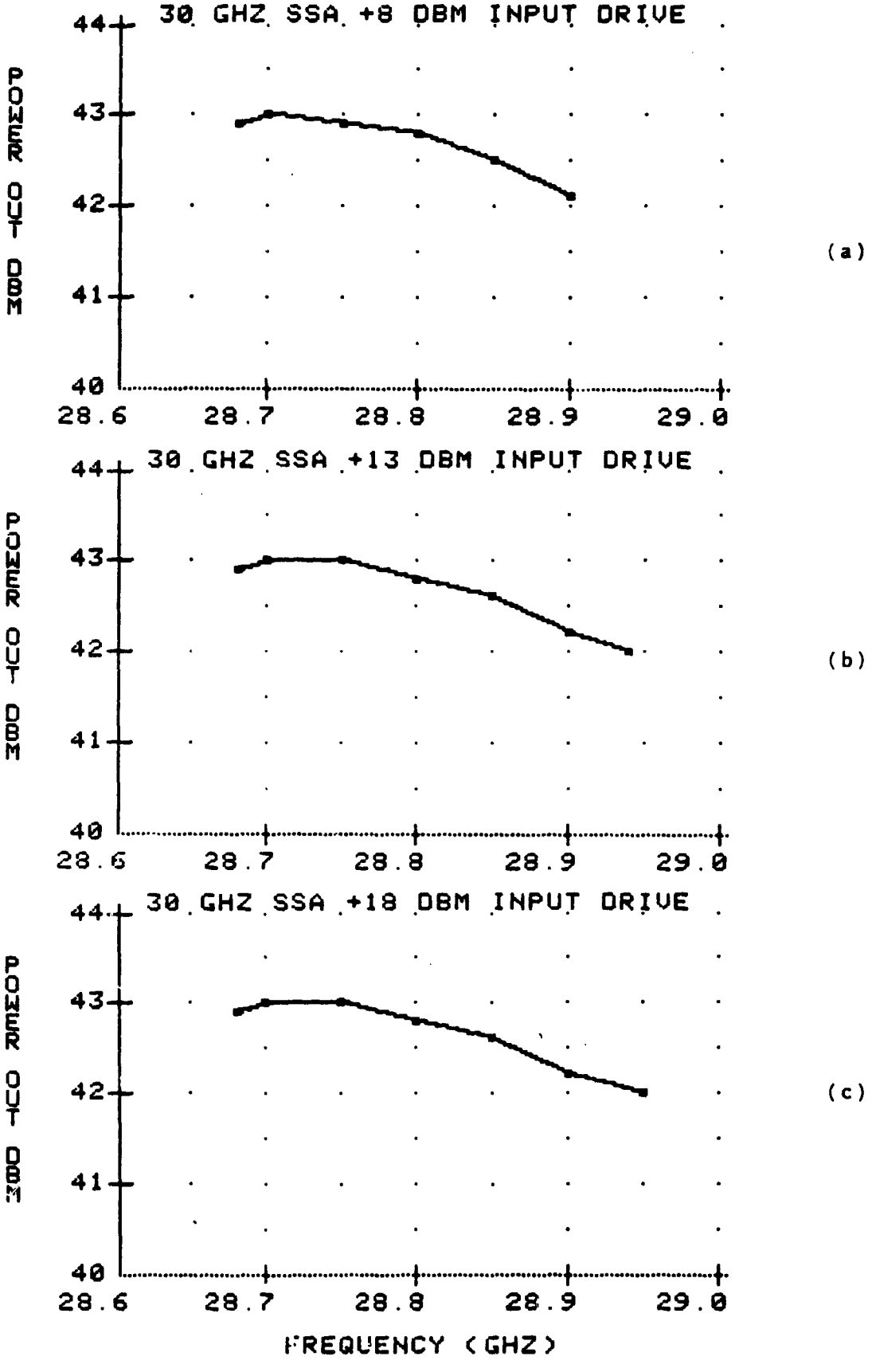


FIGURE 7-5 CW OUTPUT POWER OF TWO-STAGE AMPLIFIER

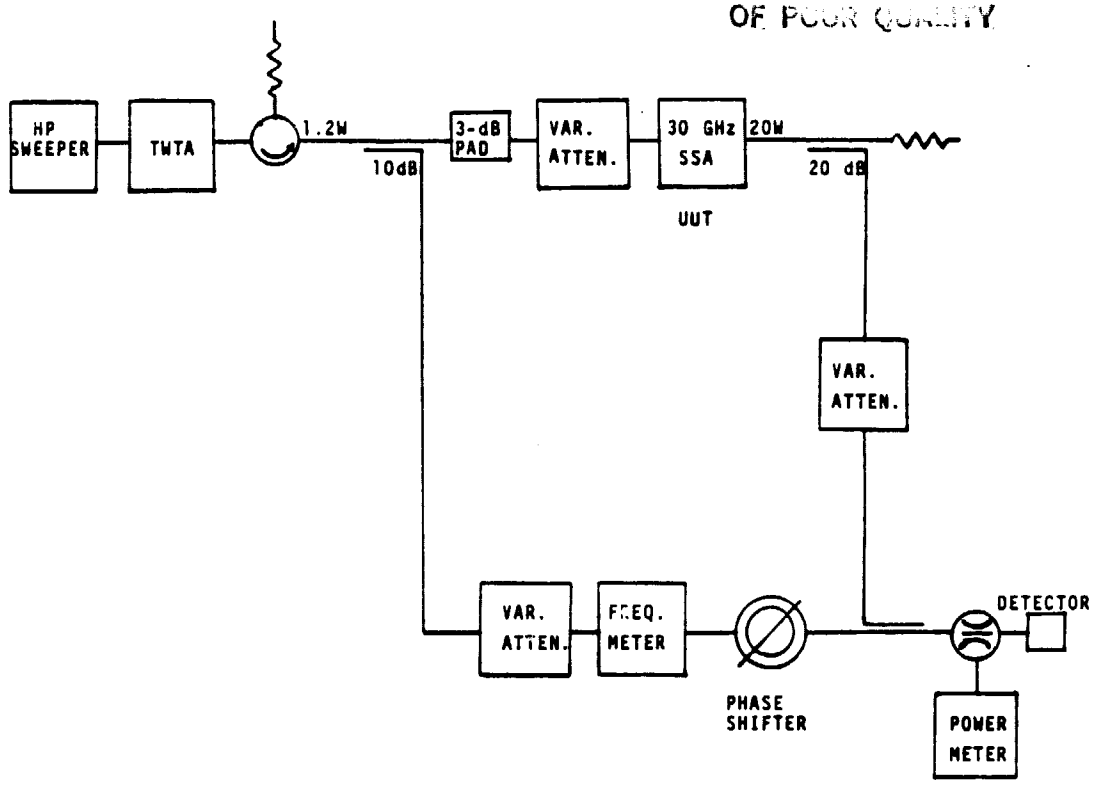


FIGURE 7-6 PHASE LINEARITY MEASUREMENT SETUP

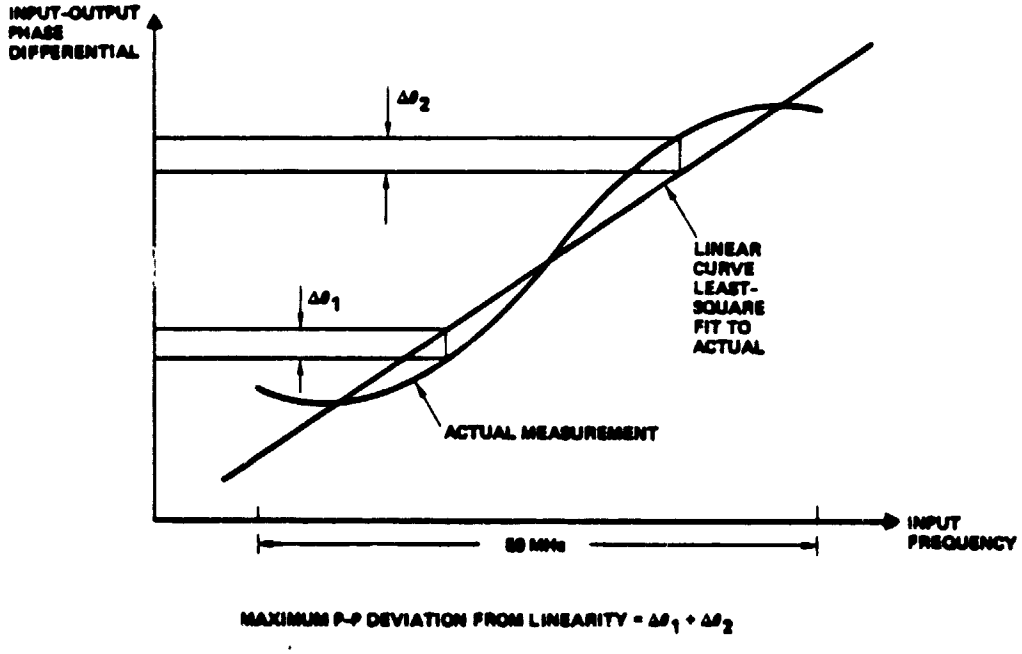


FIGURE 7-7 PHASE LINEARITY DEFINITION

phase linearity. Figure 7-8 shows the differential phase shift through the amplifier as a function of frequency. The broken line shows the least-square fit through the data points. Figure 7-9 is a magnified plot of Figure 7-8 showing the actual deviation from the least-square fit line which is normalized here to zero degree. It is seen that over any 50 MHz segment, the phase linearity is $<10°$ P-P. Over the entire 250 MHz locking band, the phase linearity is $<20°$ P-P.

7.2.6 Harmonic and Spurious Response

By downconverting the 28.75 GHz amplifier RF signal to 2 GHz, the noise floor of the measurement system can be reduced down to -60 dBc. Down to -60dBc, no harmonic or spurious responses are generated.

7.2.7 Noise Performance

The noise power at the output of the amplifier was measured as dBc (noise power in dB below carrier) with the help of an automatic noise measurement system. The noise output was measured through a 1-Hz window and for a single-sideband bandwidth of 10 MHz. For PM noise measurement, a harmonic mixer was used to downconvert the amplifier rf signal to 1.25 GHz IF, compatible with the frequency band of the noise measurement system. The harmonic mixer configuration is shown in Figure 7-10. For AM noise measurement, a conventional bridge as shown in Figure 7-11 was used. The resulting data is the noise power spectral density, as shown in Figures 7-12 and 7-13. Figure 7-12 shows the spectral density plot for PM noise (noise which appears as phase fluctuation of the carrier). Figure 7-13 shows the spectral density plot for AM noise (noise which appears as amplitude fluctuations of the carrier). Noise performance in terms of AM and PM spectral density is used exclusively to characterize oscillators of which the present amplifier is one.

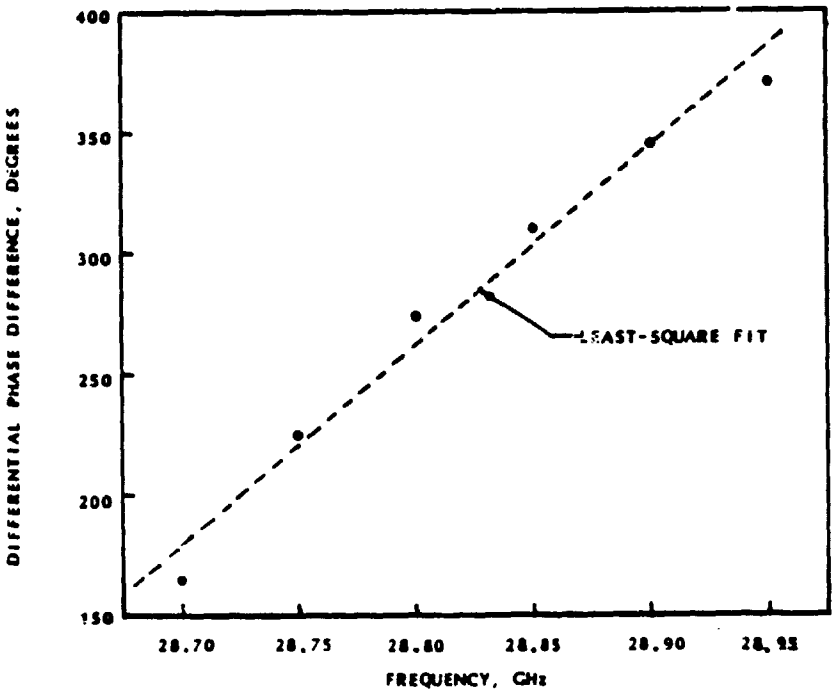


FIGURE 7-8 PHASE LINEARITY MEASUREMENT DATA WITH LEAST-SQUARE FIT

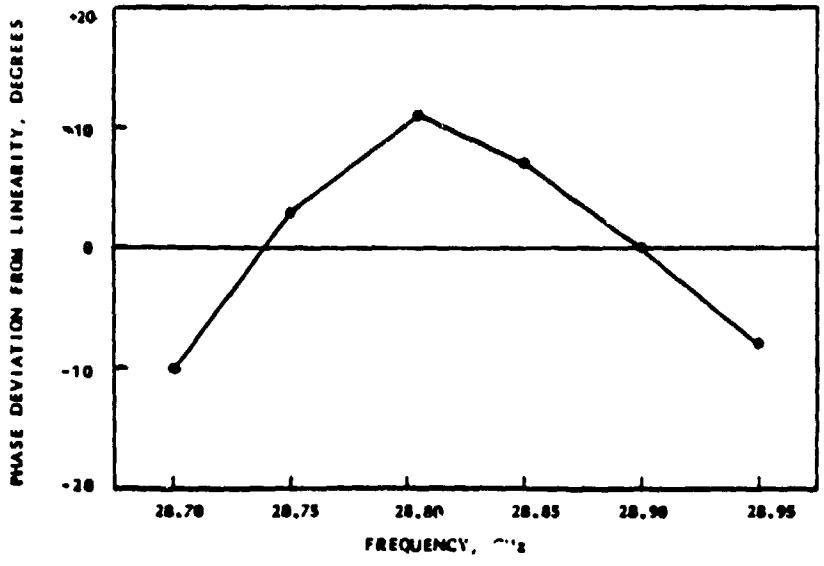


FIGURE 7-9 PHASE LINEARITY DEVIATION FROM ZERO DEGREE

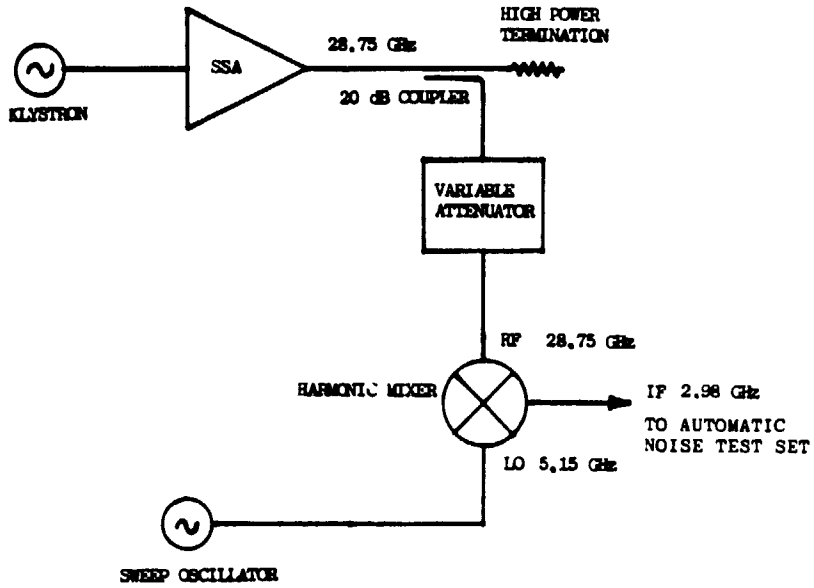


FIGURE 7-10 PHASE NOISE MEASUREMENT SETUP

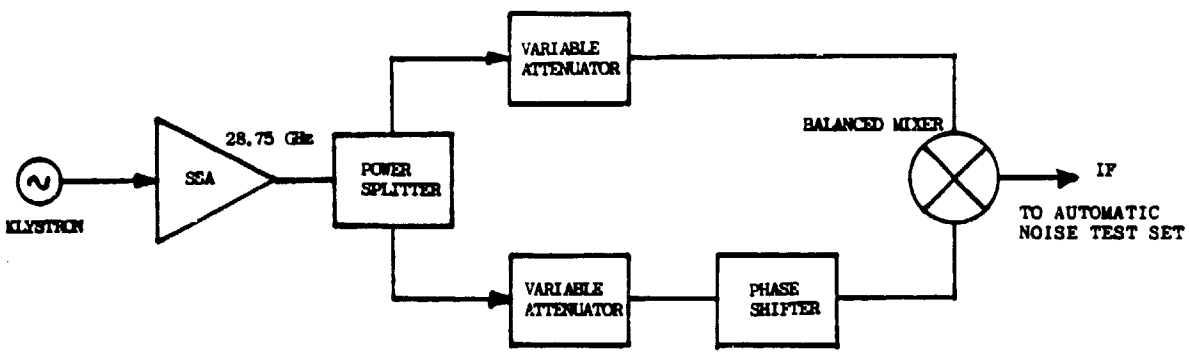


FIGURE 7-11 AM NOISE MEASUREMENT SETUP

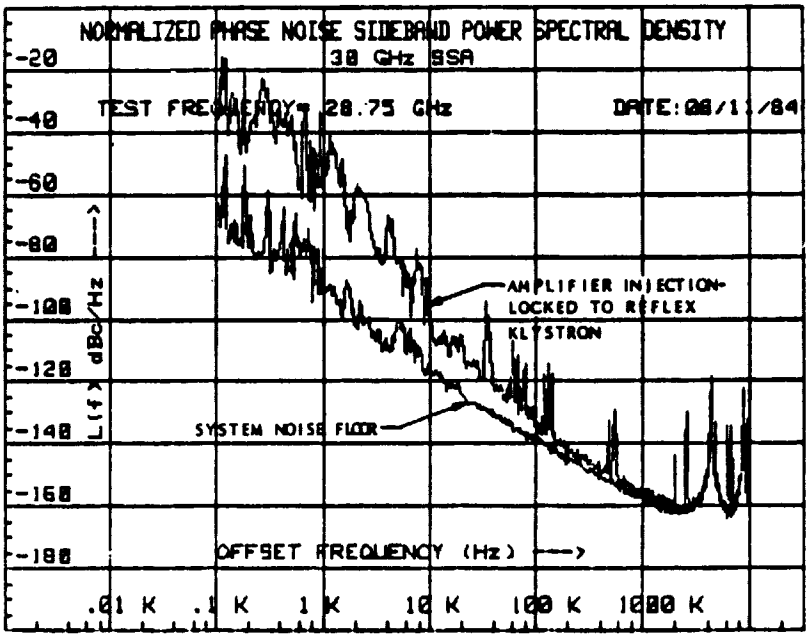


FIGURE 7-12 PHASE NOISE SPECTRUM OF AMPLIFIER INJECTION-LOCKED TO A REFLEX KLYSTRON

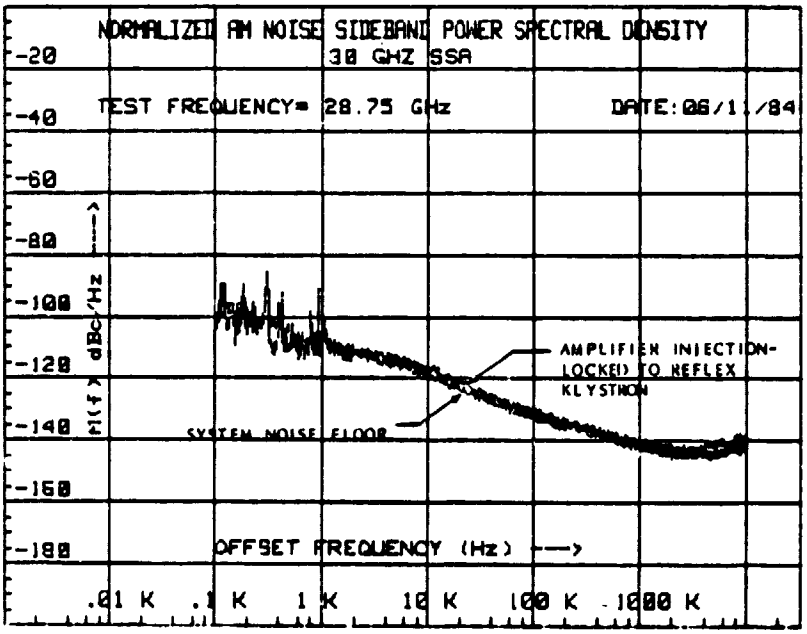


FIGURE 7-13 AM NOISE SPECTRUM

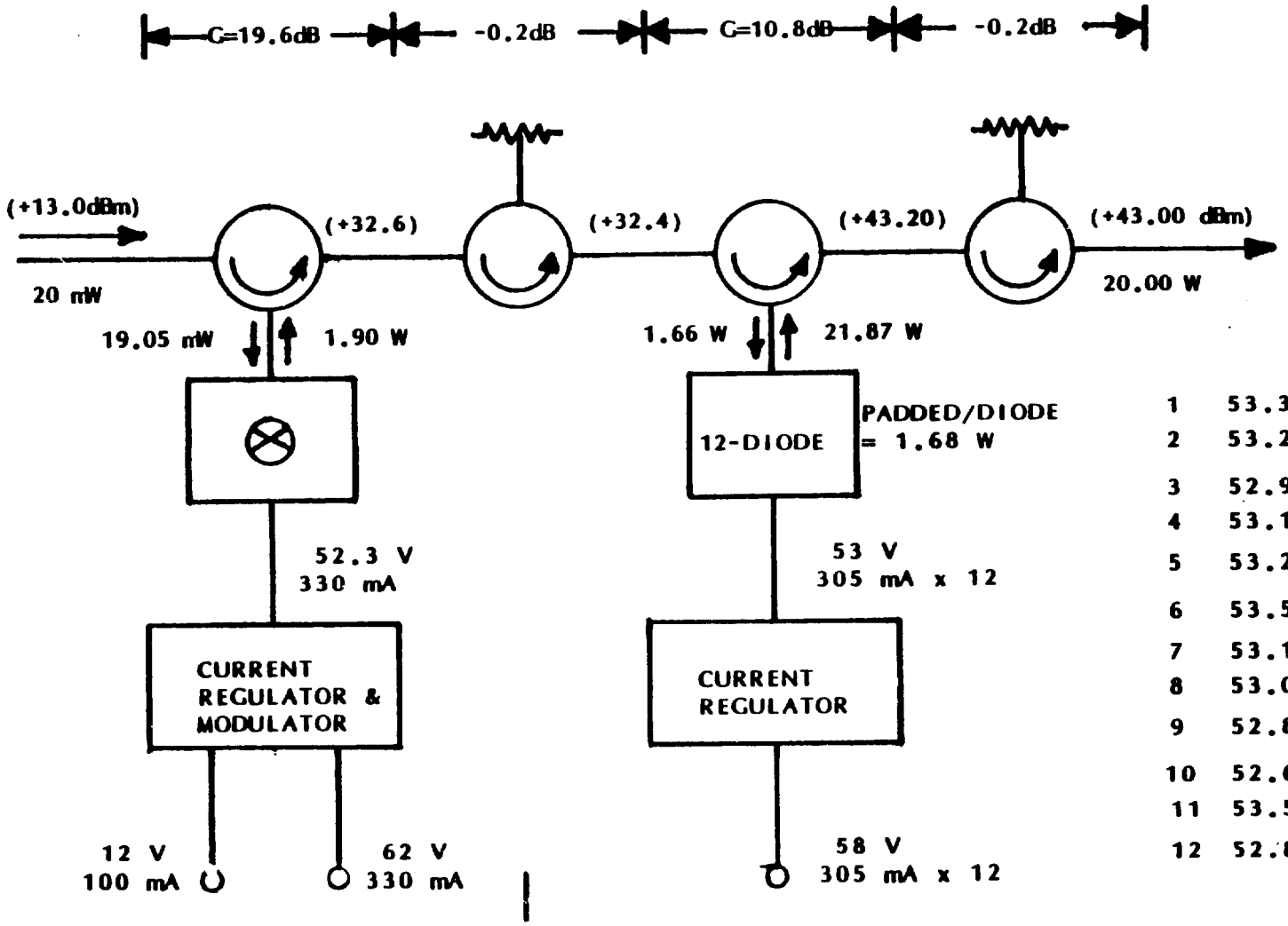
7.2.8 TDMA OPERATION

In addition to the tests required by contract, we have also developed and tested the amplifier in the TDMA burst mode operation. The functional block diagram of the final POC amplifier is shown in Figure 7-14. In this design, the power combiner output stage was tuned to the stable amplifier mode such that it puts out no rf output in the absence of an input drive. This automtically enables the combiner to operate in burst-mode. The single-diode driver, on the other hand, was made to operate in the burst mode by incorporating a fast pulse modulator which modulates the bias current to the IMPATT between 0 mA and 350 mA. For testing purpose only, a +13 dBm cw input drive was maintained. In actual TDMA operation, the input drive must be modulated in synchronization with the current modulation of the driver stage. Figures 7-15 a), b) and c) show the output power versus frequency from 50% duty cycle and three different pulse widths, namely, 200 ns, 1 μs and 2 μs.

Figures 7-16 a) and b) show the video displays of a 200 ns rf output pulse and a 2 μs rf output pulse, respectively. Figures 7-17 a) and b) show the typical rise and fall times, either of which is shown to be less than 20 ns.

7.3 SUMMARY OF TEST RESULTS

A comparison between the performance requirements and the performance achieved is shown in Table 7-2.



1	53.39V	304 mA
2	53.25V	305 mA
3	52.99V	305 mA
4	53.16V	304 mA
5	53.29V	304 mA
6	53.55V	304 mA
7	53.10V	304 mA
8	53.03V	306 mA
9	52.83V	304 mA
10	52.64V	304 mA
11	53.50V	303 mA
12	52.83V	305 mA

FIGURE 7-14 FINAL AMPLIFIER BLOCK DIAGRAM

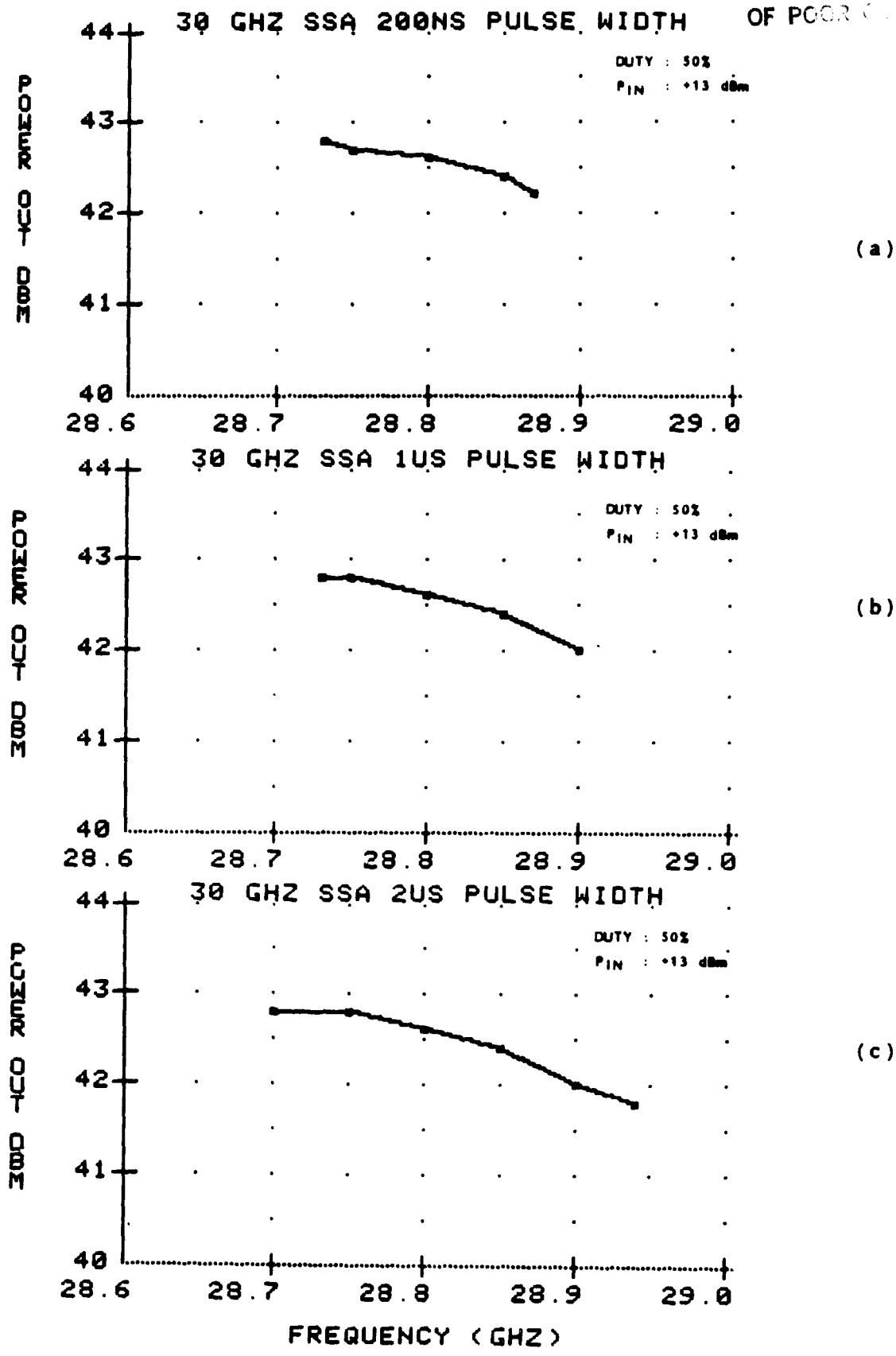
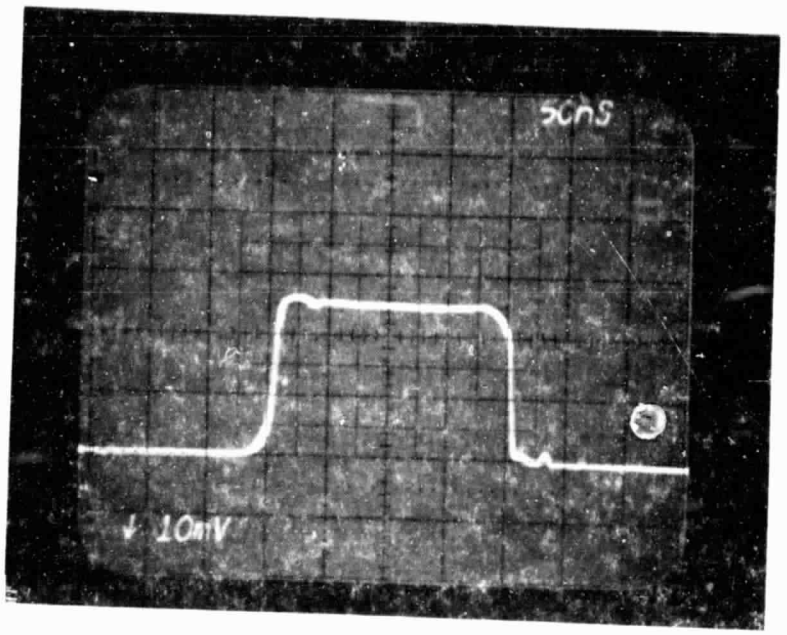
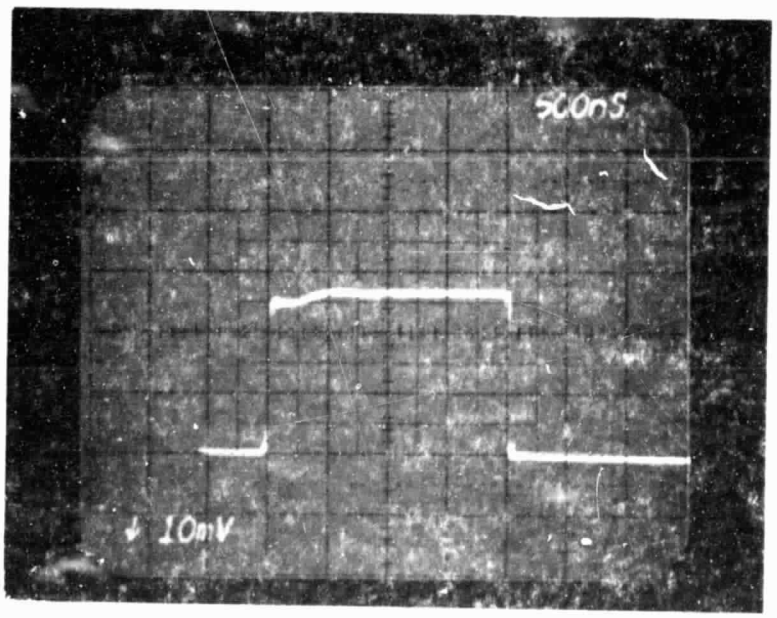


FIGURE 7-15 OUTPUT POWER CHARACTERISTICS IN BURST MODE

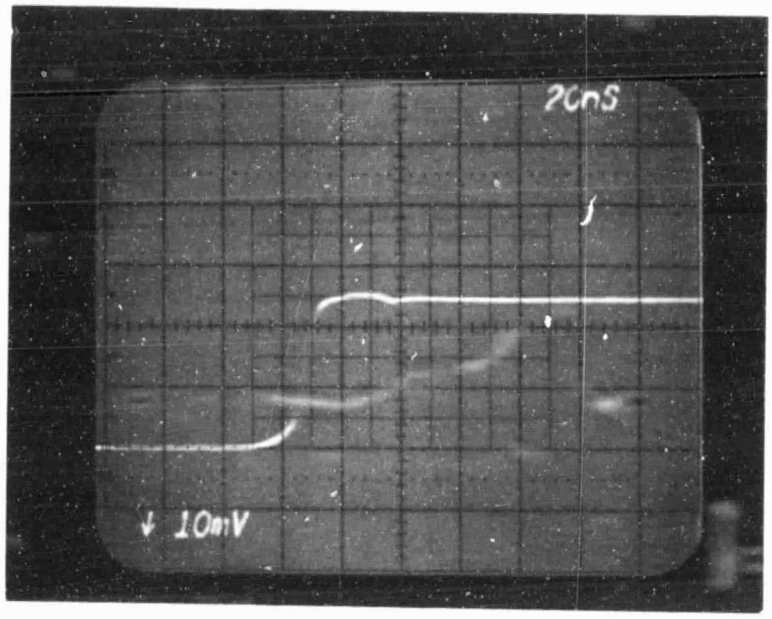


(a)

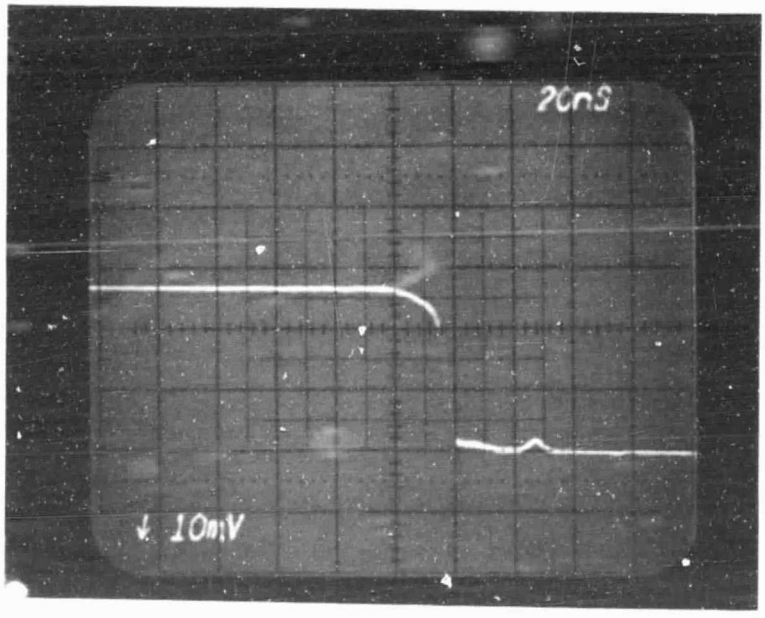


(b)

FIGURE 7-16 VIDEO DISPLAY OF RF OUTPUT PULSE FOR 200 ns and 2μs PULSE WIDTHS



(a)



(b)

FIGURE 7-17 VIDEO DISPLAY OF AMPLIFIER RF OUTPUT PULSE RISE AND FALL TIMES

Table 7-2. POC Amplifier Performance Summary

Parameter	Performance Requirement	Performance Achieved
RF Output Power	20 W	20 W
RF Band	28.5 to 29.0 GHz	28.68 to 28.94 GHz
RF Bandwidth (0.2 dB point)	Not specified	100 MHz
RF Bandwidth (1.0 dB point)	50 MHz	260 MHz
Noise Performance	Minimum	-95 dBc/Hz @ f_m = 10 kHz (FM) -120 dBc/Hz @ f_m 10kHz (AM) (For further details please refer to spectra)
RF Gain (50 MHz)	30 dB ± 1dB	30 dB $^{+\ 0\ dB}_{-.1dB}$
In-Band Overdrive	5 dB Nominal	5 dB
Gain Variation (50 MHz)	≤ + 0.5 dB	≤ +0.1 dB
Gain Slope (50 MHz)	≤ 0.15 dB/MHz	≤ 0.01 dB/MHz
Phase Linearity (50 MHz)	≤ 10° P-P	10° P-P
Harmonic Response	50 dBc	50 dBc
Spurious Response	60 dBc	60 dBc
Pulse Width	Not Required	200 ns to CW
Pulse Repetition Rate	Not Required	Up to 2.5 MHz
Pulse Rise Time	Not Required	10 ns
Pulse Fall Time	Not Required	10 ns

7.4 RELIABILITY ANALYSIS

The reliability of the POC amplifier is measured by a quantity called Mean-time-to-failure (MTTF). The MTTF of a device can be defined based on ensemble concept. Let N (t) be the number of identical devices at time t. Let us now assume that after a small time interval dt, a small number -dN has failed. According to MIL-HDBK-217D, and MIL-STD-756B, the MTTF of this device is defined as

$$MTTF = - \frac{N(t)}{dN/dt} \qquad (7\text{-}1)$$

The failure rate λ , is defined as

$$\lambda = (MTTF)^{-1} \qquad (7\text{-}2)$$

Combining equations (7-1) and (7-2), we find

$$\frac{dN}{N} = -\lambda\, dt \qquad (7\text{-}3)$$

Integrate both sides from t = 0 to t = t,

$$N(t) = N(0)\ e^{-\lambda t} \qquad (7\text{-}4)$$

The ratio N (t)/N (0) can be viewed as the probability of survival of the device as time t. Defining this probability by P (t), we have

$$P(t) = e^{-\lambda t} \qquad (7\text{-}5)$$

If there are m different types of devices in a system, and that each device has a particular failure rate, then we may generalize equation (7-5) to read

$$P_j(t) = e^{-\lambda_j t}, \qquad j = 1, 2, \ldots, m. \qquad (7\text{-}6)$$

where λ_j is the failure rate of the j^{th} device and $P_j(t)$ is the probability of survival of the j^{th} device at time t. If the probabilities of survival of the various devices are independent of one another, i.e., the failure of one device does not result in the failure of other devices within the system of interest, then the aggregate probability of survival P_S of the whole system is simply given by

$$\begin{aligned} P_S(t) &= \prod_{j=1}^{m} P_j(t) \\ &= \exp\left\{-\sum_{j=1}^{m} \lambda_j t\right\} \end{aligned} \qquad (7\text{-}7)$$

From equation (7-7), one may now define as aggregate failure rate λ_s by the following expression

$$\lambda_s = \sum_{j=1}^{m} \lambda_j \qquad (7\text{-}8)$$

If one further defines an aggregate MTTF of the system by $(MTTF)_s$, then

$$(MTTF)_s^{-1} = \sum_{j=1}^{m} (MTTF)_j^{-1} \qquad (7\text{-}9)$$

Equation (7-9) establishes the lower bound MTTF for a system of m devices in which the faiure of any one device is considered a total failure. In the estimation of the POC amplifier MTTF, we shall be solely concerned with this worst case estimate.

Of all the devices in the system, the failure rate of IMPATT diodes is the highest. Figure 7-18 shows the IMPATT diode MTTF as a function of junction temperature. To determine the junction temperature of the IMPATT diodes, one must consider the diode in the driver amplifier and the diodes in the combiner separately. The physical construction of a diode/module/heat exchanger assembly is shown in Figure 7-19. This construction is applicable to both the driver and the power combiner. Let us consider each of them separately.

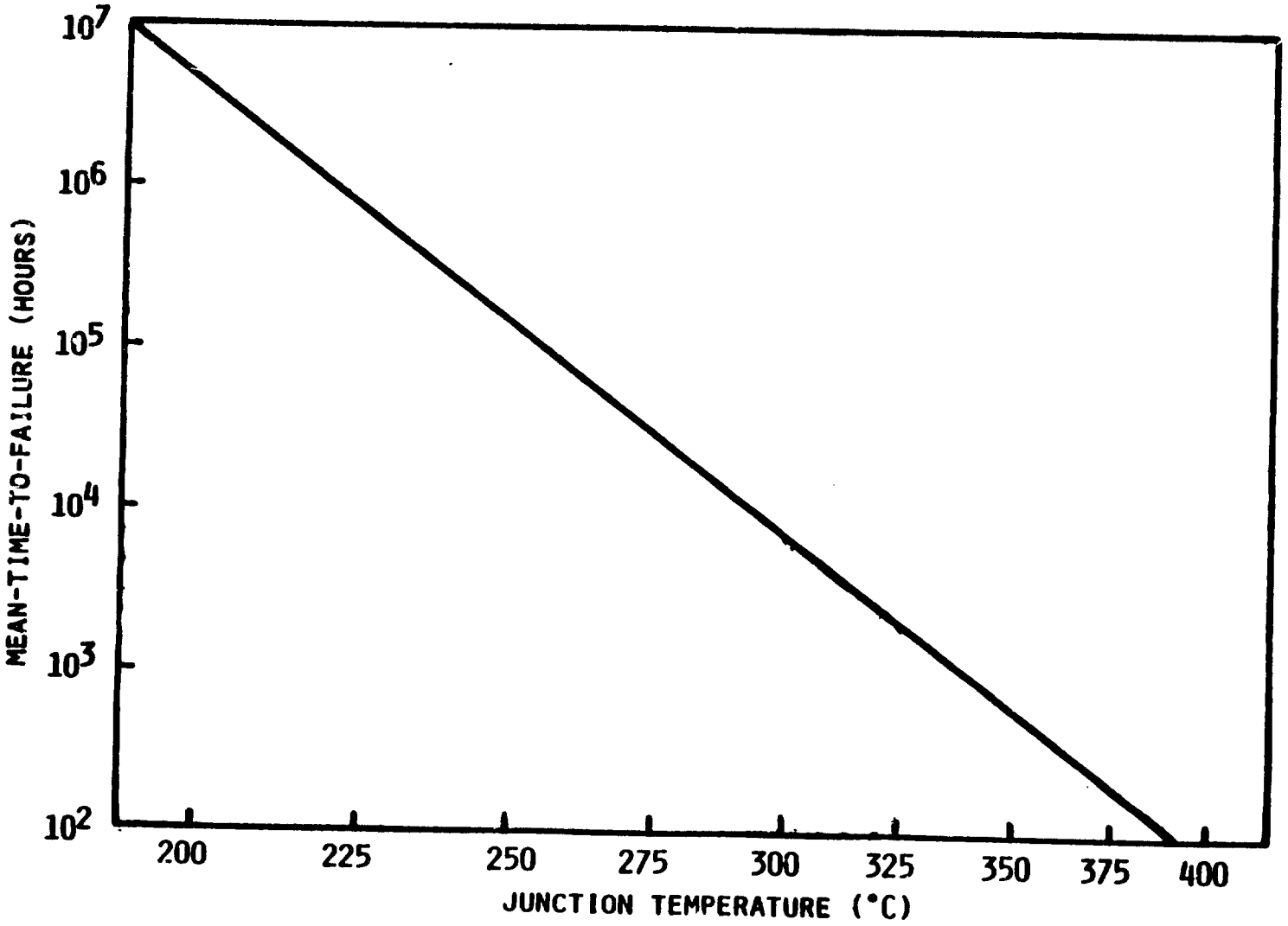


FIGURE 7-18. IMPATT DIODE MTTF VERSUS JUNCTION TEMPERATURE

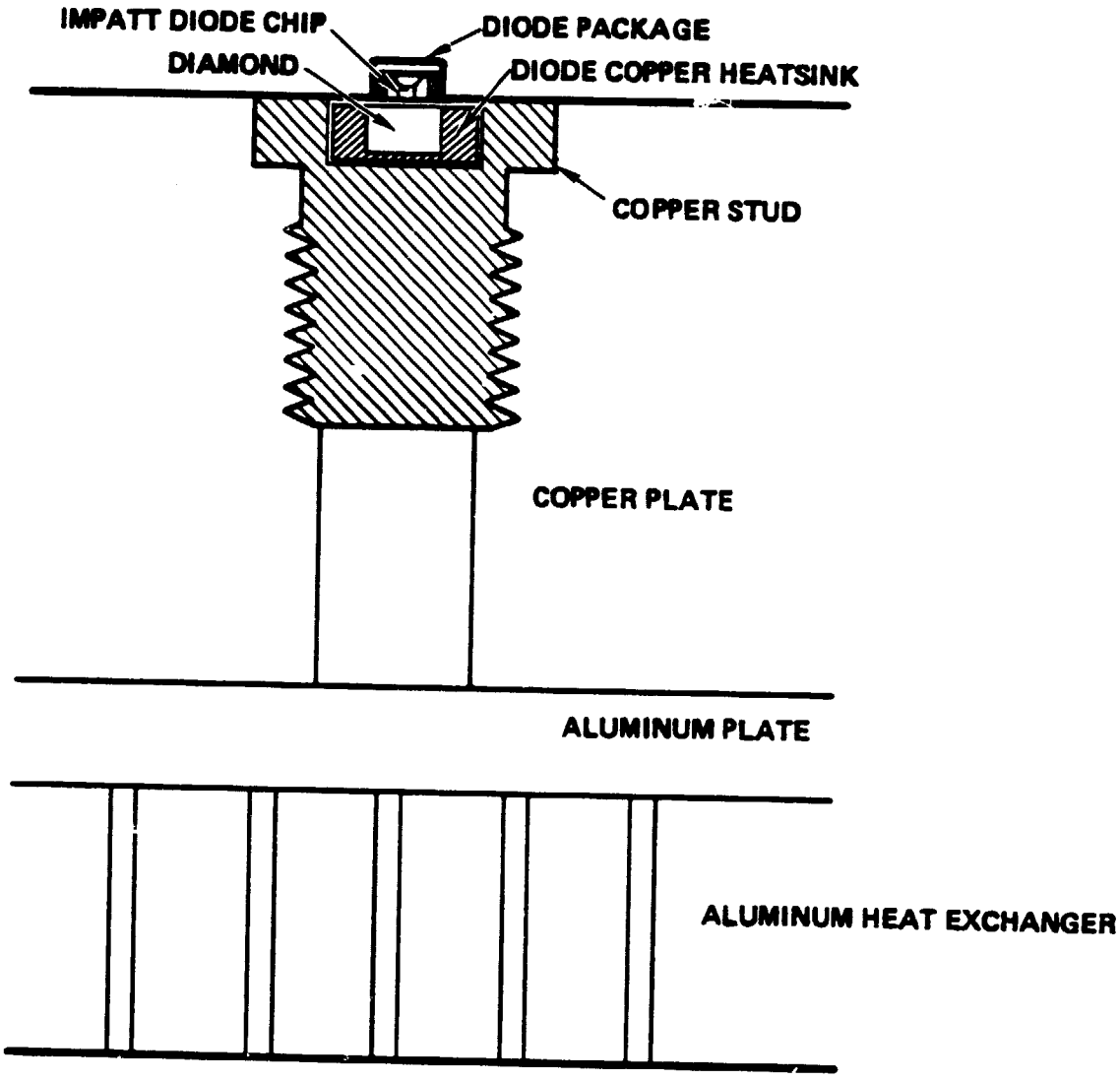


FIGURE 7-19. THERMAL INTERFACES BETWEEN THE IMPATT DIODE AND THE HEAT EXCHANGER

Driver Amplifier. The thermal model for the driver amplifier is shown in Figure 7-20. The thermal resistance of the IMPATT diode package was measured to be 12.26° C/W. The IMPATT diode operated at 53.64 V and 0.33 A, and generated 2 W of rf power. This yields a net dissipated power of 15.7 W. This amount of heat is dissipated at the diode junction and at the diode stud/copper base interface. However, the amount of heat dissipated into the heat exchanger is from 13 diodes, which, from Figure 7-14 is calculated to be 185.36 W. If the ambient temperature were assumed to be 25° C, then the junction temperature of the diode is given by

$$T_j = 25 + (185.36 \times 0.0577) + (15.36 \times 0.207) + (15.36 \times 0.0638) + (15.36 \times 12.26)$$

$$= 228.26° C$$

Power Combiner

The thermal model for the power combiner is shown in Figure 7-21. The thermal resistances from the diode to the stud is again taken to be 12° C/W. The DC power to the diode is taken to be an average of 16.12 W. Assuming an rf power of 2 W per diode (before combining), then the power dissipated as heat is 14.12 W. This gives a ΔT of 169.44° C. The thermal resistance from the stud to the copper base was calculated to be 0.0624° C/W. Thus the ΔT between the stud and the copper base is (170 x 0.0624)° C, or 10.6° C. Here, 170 W is the heat dissipated by the twelve diodes in the combiner. For the copper base/heat exchanger interface, ΔT is calculated to be (170 x 0.0936)° C, or 15.91° C. Here, 0.0936° C/W is the combiner base thermal resistance. Finally, the rise in temperature through the heat exchanger is

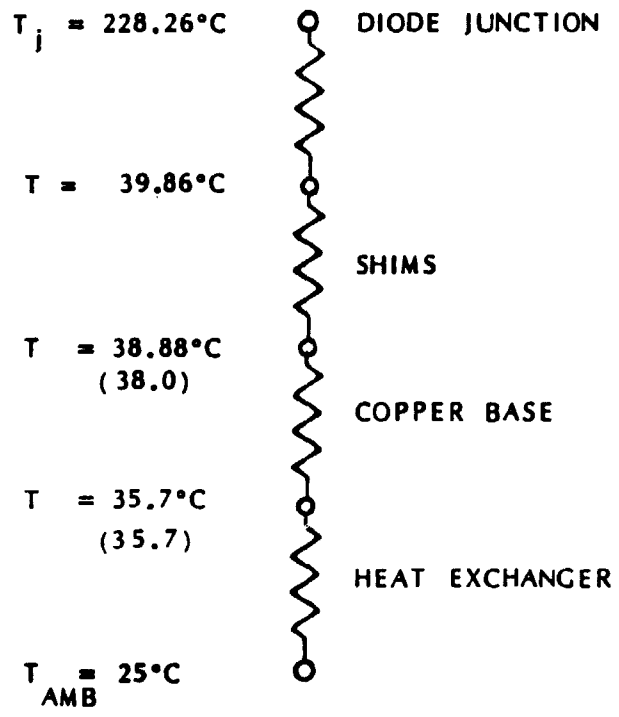


FIGURE 7-20. DRIVER TEMPERATURE DISTRIBUTION (COMBINER ON)

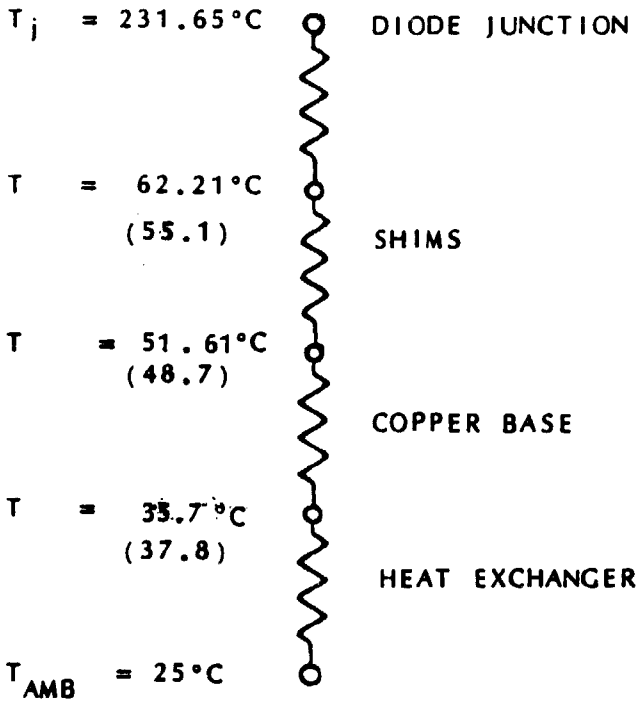


FIGURE 7-21. COMBINER TEMPERATURE DISTRIBUTION (DRIVER ON)

again taken to be 10.7°C. The junction temperature of the IMPATT diode is therefore equal to

$$T_j = 25 + 10.7 + 15.91 + 10.6 + 169.44° C$$

$$= 231.65 ° C$$

Having calculated the IMPATT diode junction temperature, the MTTF per diode can be determined from Figure 7-18. The failure rate per diode at T_j = 230° C is 1.72×10^{-6} per hour. If the failure of one diode constitutes a total failure for the amplifier, then each diode must be considered as a separate and distinct term in the summation of equation 7-9. Table 7-4 summarizes the failure rates for all the components in the amplifier. Table 7-5 capsulizes the failure rates at the LRU (Lowest Replaceable Unit) level, showing an overall failure rate of 37.83×10^{-6} per hour. This translates into an MTTF of 26,434 hours at 25°C ambient. One must bear in mind that in actual operation, the ambient temperature will vary between -20°C and 65°C (as an example). Secondly, the forced air cooling unit may not have the most efficient thermal design. Thirdly, the failure of one diode in the combiner typically results in between 1 and 2 dB of output power degradation, which might not be considered a total failure. All these considerations will have the effect of raising the MTTF by a significant amount, and thereby resulting in a higher reliability estimate for the POC amplifier.

COMPONENT	TOTAL FAILURE RATE ($\times 10^{-6}$ HRS^{-1})	COMPONENT	TOTAL FAILURE RATE ($\times 10^{-6}$ HRS^{-1})
RF COMPONENTS		F_1, F_2, F_4 = VN88AD (SILICONE)	1.72
IMPATT DIODE (DRIVER STAGE)	1.72	F_3 = 2N 4091	0.0001
IMPATT DIODE (COMBINER)	24.48	Q_1 = 2N222A	0.0000348
ISOLATORS	1.44	LM117HV REGULATOR	0.625
MULTICHANNEL RESGULATOR BOX		5K POTENTIOMETER	0.0025
LM117HV REGULATOR	7.50	560 RESISTOR	0.00067
50 POTENTIOMETER	0.30	0.1 F CERAMIC CAP	0.041
5.6 RESISTOR	0.021	1 F 20 V CAP	0.0085
0.1 F CERAMIC CAP	0.492	C1 = 47 F, 6 VDC	0.0425
C1 = 100 F	0.0122	C2 = 0.1 F, 50 VDC	0.0005
MODULATOR BOX		C3 = 0.1 F, 50 VDC	0.0062
R1 = 100 1/4 W	0.00068	C4 = 47 F, 6 VDC	0.084
R2 = 20 1/4 W	0.00091	C5 = 10 F, 75 VDC	0.0413
R3 = 68 1/4 W	0.00184	C6 = 10 F, 75 VDC	0.0413
R4 = 10 3 W	0.00085	Z1 = 5.1 V	0.02115
R5,R6,R7 = 200 1 W	0.0032	Z2 = 4.7 V	0.000351
R8 = 50 POTENTIOMETER	0.025	Z3 = 40 V	0.093
R9 = 5.6 1/2 W	0.00178		
R10 = 36 1/4 W	0.00068		
R11 = 2.2 K 1/2 W	0.00067		

TABLE 7-4. SUMMARY OF COMPONENTS FAILURE RATES

COMPONENT	FAILURE RATE ($\times 10^{-6}$ HRS^{-1})
DRIVER MODULE	1.72
COMBINER MODULE	24.48
ISOLATOR	1.44
REGULATOR MODULE	8.32
MODULATOR	1.87
	37.83

TABLE 7-5. FAILURE RATES AT THE LRU LEVEL

8. CONCLUSION AND RECOMMENDATION

The completion of the 30 GHz IMPATT amplifier program has resulted in the development of a two-stage IMPATT amplifier capable of 20 W of CW output and a 1 dB bandwidth of 265 MHz. Not only did the amplifier meet or exceed the performance requirements called for by the contract, additional development work was carried out during the program which resulted in the demonstration of TDMA burst mode operation for the 30 GHz amplifier. Specifically, the following key technologies were accomplished in the program:

- Developed reproducible 30 GHz silicon double-drift IMPATT diodes capable of $\geq$ 2.5 W output power and approximately 13% DC-to-rf conversion efficiency.

- Developed a 12 diode Kurokawa combiner which is capable of operating in the stable amplifier mode (no output in the absence of input). This allows the combiner output to be pulsed without added circuit complexity such as multichannel pulse modulators.

- Developed a low cost current pulse modulator which can switch the output power of a single-diode driver amplifier on and off with 20 ns rise and fall times.

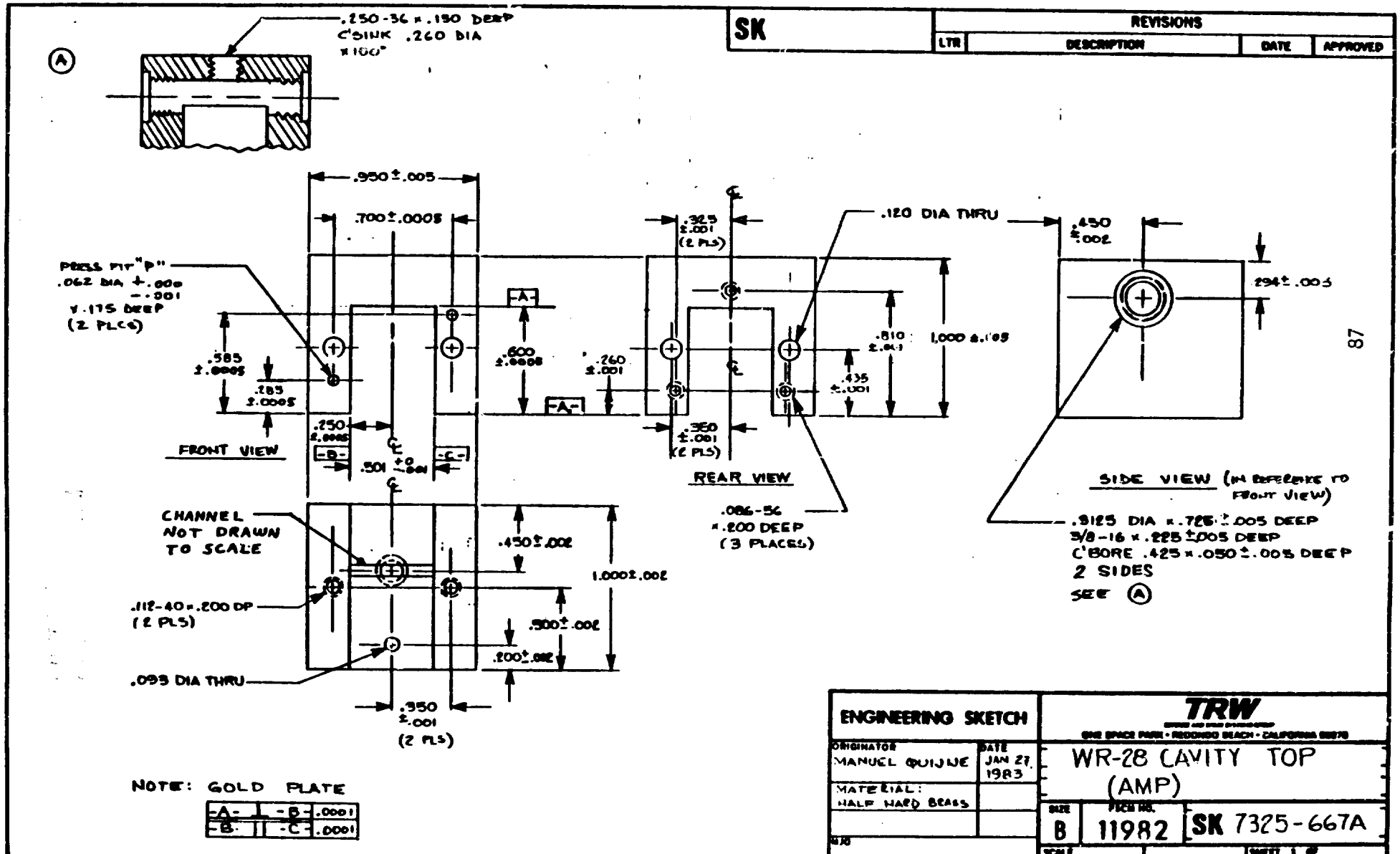
- Developed low loss, broadband circulators with 0.2 dB insertion loss over 7 GHz bandwidth.

Future growth of the amplifier performance will largely be in the area of output power. This will be accomplished by the development of higher power diodes and by more advanced power combining approaches such as using a radial line combiner. Chip level combining is still possible, but is deemed unlikely to beccme a mature technology within the next three years. In addition to

output power improvement, there will also be some secondary improvements in DC-to-rf efficiency, which results from improvement in the IMPATT diode itself. An assessment of these future technology improvements is presented in Appendix B.

As a result of this POC amplifier development, three additional development areas were identified. Firstly, the amplifier must be amenable to low cost manufacturing. Because of the high output power requirement on the power combiner, the low cost manufacturing aspects can only be addressed by looking at methods for low cost fabrication, such as numerical-controlled (NC) machining and die casting, etc.---methods which do not change the inherent circuit design. On the other hand, the driver stage can be made extremely low cost, as compared with the present waveguide configuration, by using MIC technology. TRW currently has developed a Q-band (44 GHz) microstrip oscillator capable of 200 mW output power. Such a microstrip oscillator can be developed at 30 GHz for low cost manufacturing. Secondly, the amplifier must have high reliability, which translates into low life cycle cost. The power combiner already posseses the advantage of graceful degradation, so that the combiner itself will not be considered totally inoperable if one or two diodes failed. On the other hand, the driver is a single-diode unit not subject to soft failure. In othr words, the failure of a single-diode driver would result in a catastrophic failure of the entire amplifier. This necessitates the incorporation of a redundant driver. The easiest way to realize redundancy is to put two driver amplifier chains in parallel and connect them at the output via a ferrite switch. TRW has developed latching ferrite switches operating between 27.5 and 30 GHz, with 0.4 dB insertion loss, 35 dB isolation, and 1 μs switching speed. Thirdly, since the amplifier will operate with an angle-modulated input signal, it is important to determine the capacity of the amplifier to handle data rates as high as 110 MBPS. This can be accomplished by performing a Bit-Error-Rate (BER) test on the amplifier. More detailed discussions on these issues can be found in Appendix C which is a reproduction of Task VIII Report entitled "Requirements Document and Development Plan".

APPENDIX A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REVISIONS
LTR
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.700 ±.0005
PRESS FIT "P" .062 DIA +.000 -.001 x .175 DEEP (2 PLCS)
.585 ±.0005
.285 ±.0005
.600 ±.0005
FRONT VIEW
.250 ±.0005
-B-
.501 +0 -.004
-C-
-A-
.325 ±.001 (2 PLS)
.120 DIA THRU
.260 ±.001
.810 ±.001
1.000 ±.005
.435 ±.001
.360 ±.001 (2 PLS)
REAR VIEW
.086-56 x .200 DEEP (3 PLACES)
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.294 ±.005
SIDE VIEW (IN REFERENCE TO FRONT VIEW)
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3/8-16 x .225 ±.005 DEEP
C'BORE .425 x .050 ±.005 DEEP
2 SIDES
SEE A
CHANNEL NOT DRAWN TO SCALE
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1.000 ±.002
.112-40 x .200 DP (2 PLS)
.500 ±.002
.200 ±.002
.099 DIA THRU
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NOTE: GOLD PLATE
-A- | -B- .0001
-B- | -C- .0001
87
ENGINEERING SKETCH
ORIGINATOR MANUEL QUIJUE
DATE JAN 27, 1983
MATERIAL: HALF HARD BRASS
TRW
ONE SPACE PARK · REDONDO BEACH · CALIFORNIA
WR-28 CAVITY TOP (AMP)
SIZE B
FSCM NO. 11982
SK 7325-667A
SCALE
SHEET 1 OF

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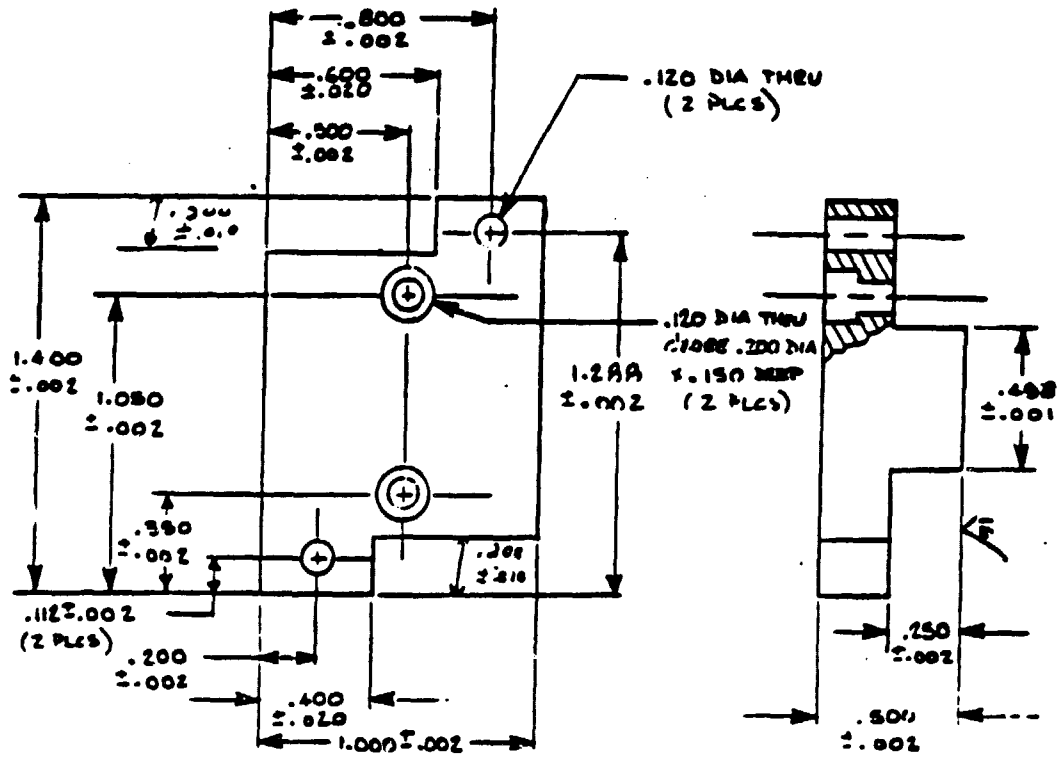

NOTE: 1. GOLD PLATE

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ORIGINATOR M. QUIJIJE C. STRAWBRIDGE	DATE Jan 26, 1982	WR-22 CAVITY BOTTOM
MATERIAL: TeCu		
X61431, X51790		
ALSO	SIZE A	FSCM NO. 11982 SK-C415-870
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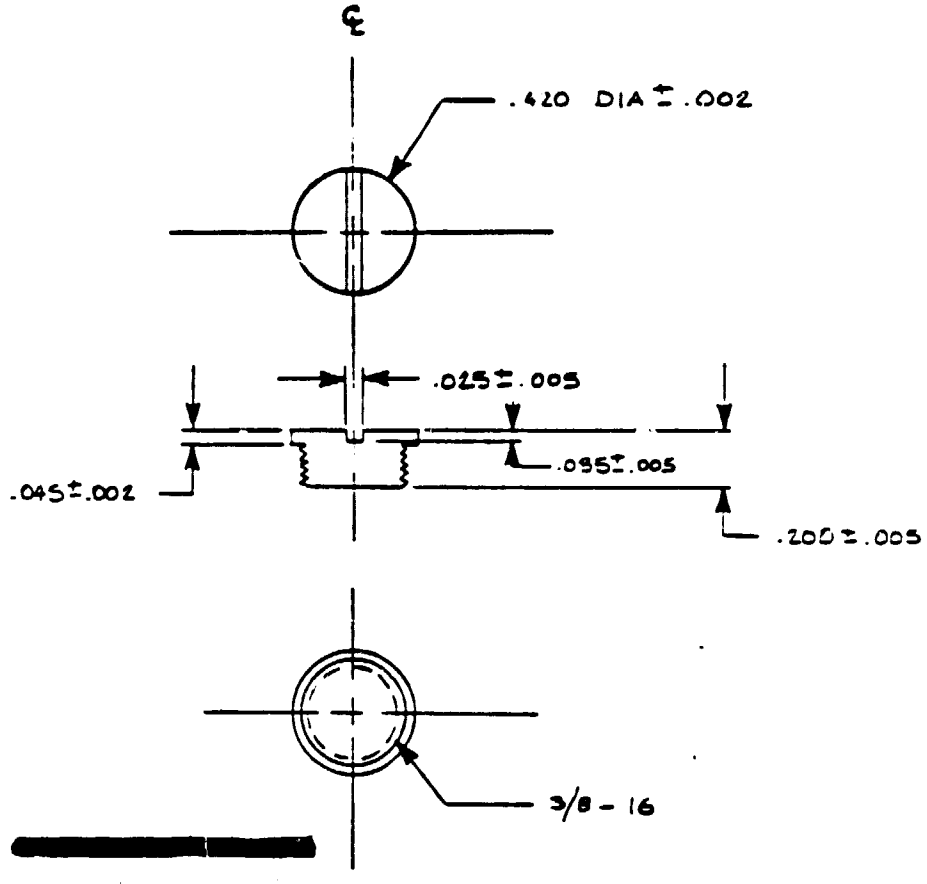

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ENGINEERING SKETCH

TRW
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR	DATE
MANUEL QUIJIJE X61431, X51790	MAY 11, 1981
MATERIAL: HALF HARD BRASS	
MFG	

WR-22 CAVITY ~~STUD~~ PLUGS

SIZE	DRAWING NO.	
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SYSTEMS GRP REV. 8/79

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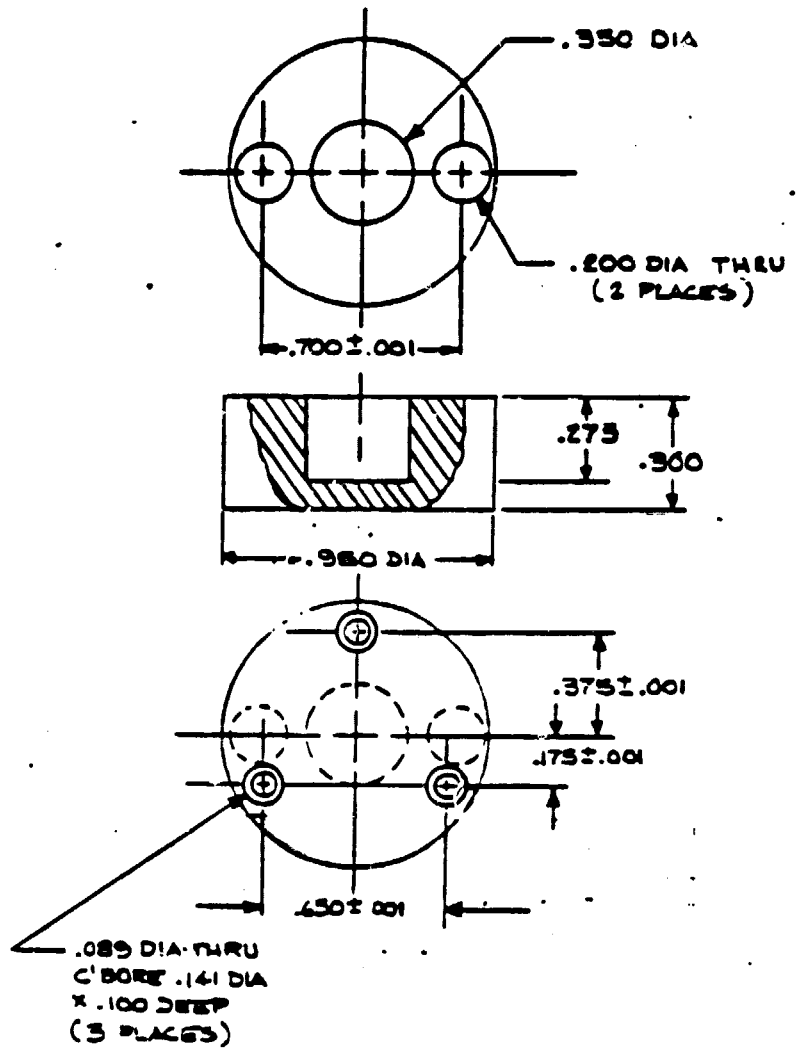

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MATERIAL: HALF HARD BRASS		
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SK 7325-670

SK	REVISIONS			
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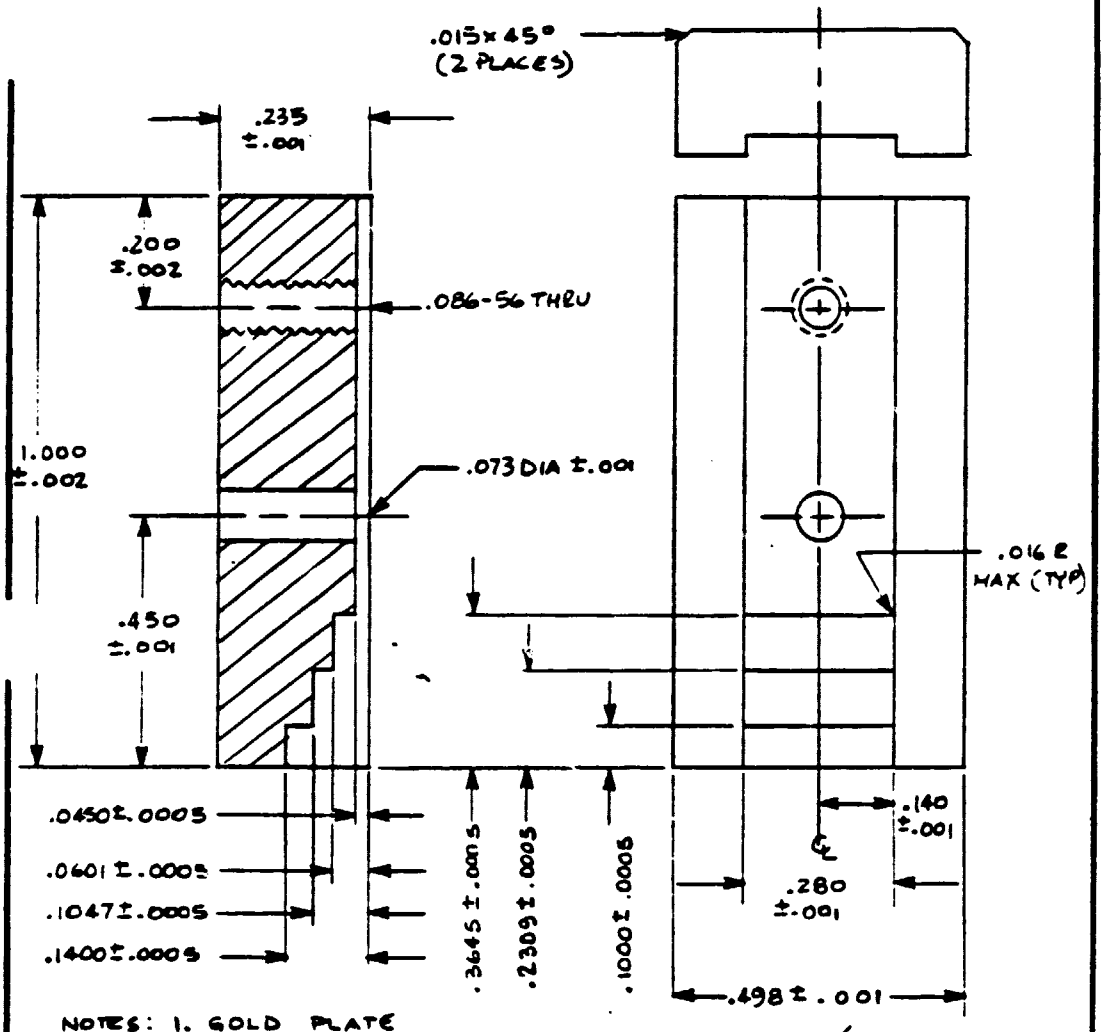

NOTES: 1. GOLD PLATE
2. ALL EDGES AND CORNERS SHARP, SURFACES 16 FINISH

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MATERIAL: 1/2 HARD BRASS		SIZE: A	FSCM NO.: 11982
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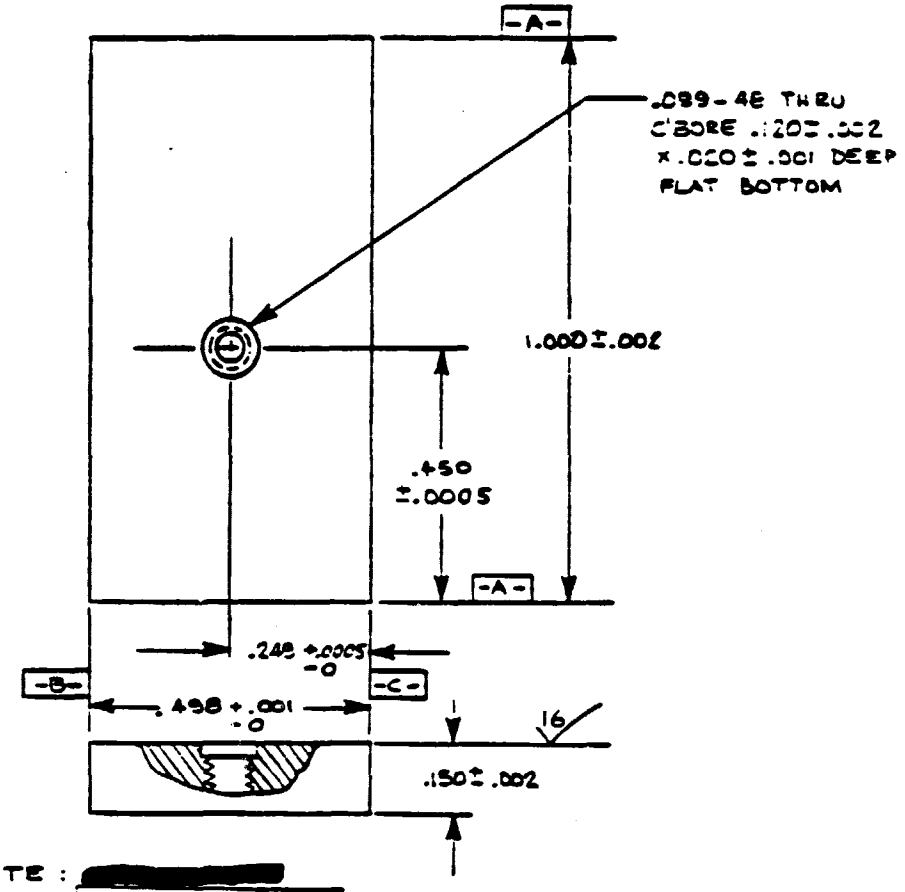

NOTE : [redacted]

-A-	-B-	.0001
-B-	-C-	.0001

ENGINEERING SKETCH

TRW

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR	DATE
ROY E BEELT	NOV 14 1979
MATERIAL Te Cu	
MFR	

WR-22 DIODE HEATSINK (STUD)

SIZE	FSCM NO.	
A	11982	SK 7325-266

SCALE | SHEET 1 OF

SK

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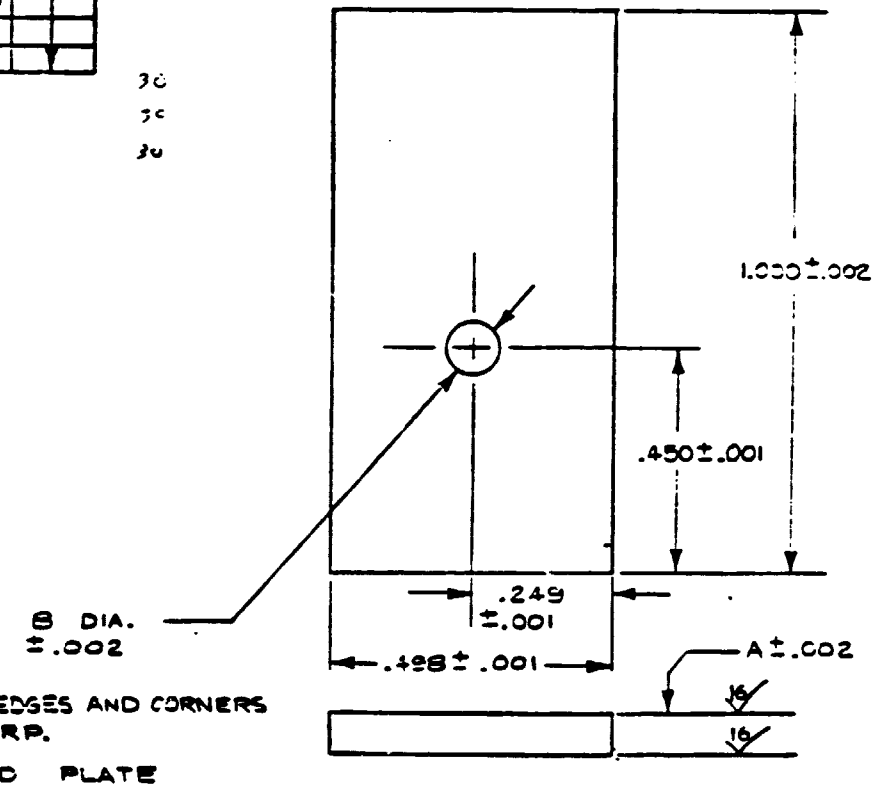

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GOLD PLATE

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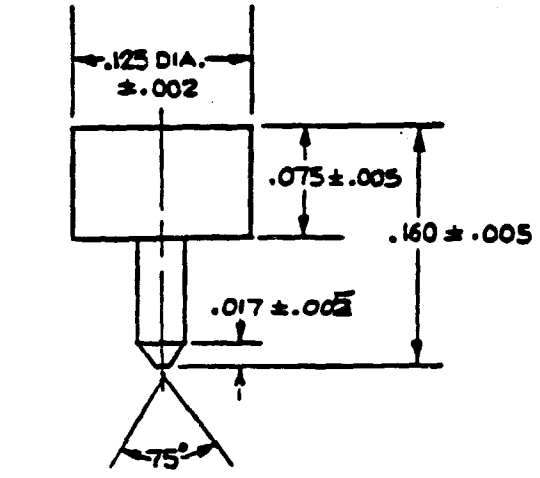

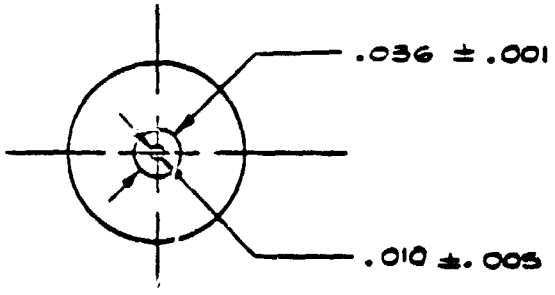

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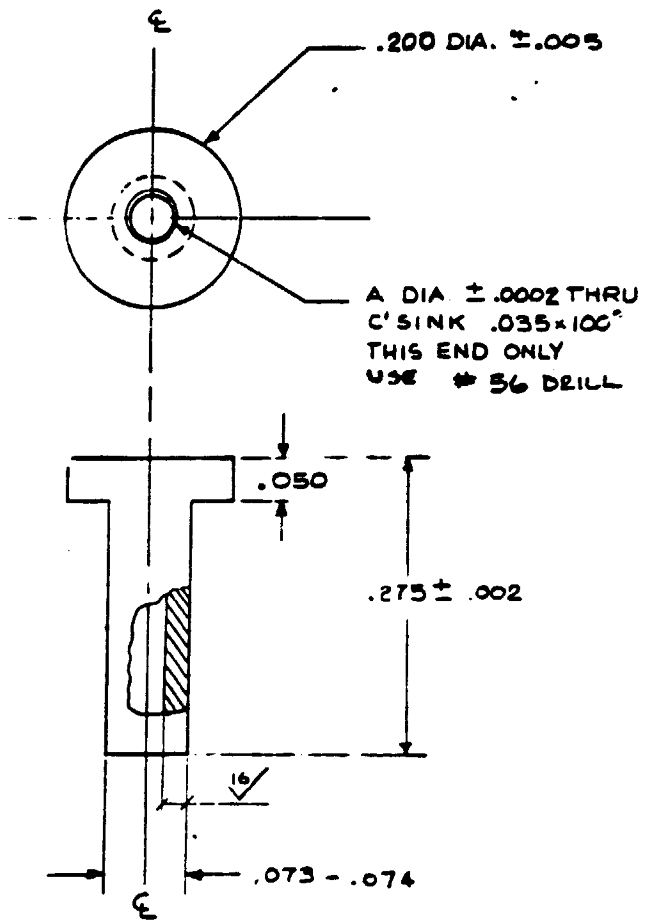
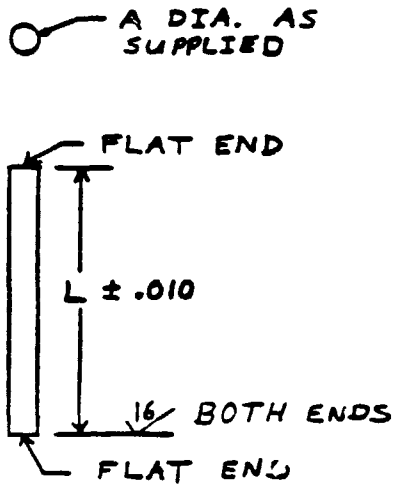


ENGINEERING SKETCH	TRW — ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
ORIGINATOR: MANUEL QUIJIJE / R. STEADIGEWAY — DATE: [illegible]	EWR-22 BIAS CHOKE (FERRITE)
MATERIAL: MF-124 ECCOSORB	SIZE: A — FSCM NO. 11982 — SK 7325-602
MJO	SCALE — SHEET 1 OF

SK

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

DASH NO.	A	L	QTY.
-001		.400	
-002			
-003			
-004			
-005			
-006			
-007			
-008			
-009			
-010			
-011			
-012			
-013			
-014			
-015			
-016			
-017			
-018			
-019			
-020			
-021			
-022			
-023			
-024			
-025			



NOTES:

1. DELTRONICS GAGE PIN TO BE GROUND TO THE PROPER LENGTH.
2. DEBURR AND LAP BOTH ENDS.
3. 3 BIAS PINS PER GAGE PIN.
4. GOLD PLATE ~ 10 μ IN.

ENGINEERING SKETCH

ORIGINATOR	DATE
R. STRANGEWAY M. QUITTJE	03/26/82
X61431 OR X51790	
MATERIAL: GAGE PIN	
MJO	

TRW
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

BIAS PINS

SIZE	FSCM NO.	
A	11982	SK-C415-975

SCALE — SHEET 1 OF 1

SK

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

DASH NR	- A -
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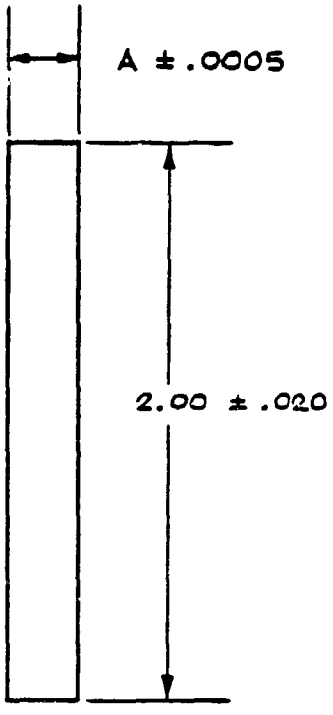
-002	.120
-003	.146
-004	.186
-005	.221
-006	.417



NOTE: 1. POLISH BOTH SURFACES WITH STEEL WOOL.
2. TO BE FLAT

ENGINEERING SKETCH

TRW
DEFENSE AND SPACE SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR	DATE
ROY EBERT	JAN 23 1980
MATERIAL .002 THK BeCu	
AUD	

W/G SHORT
BeCu COVER

SIZE	FSCM NO.	
A	11982	SK 7325-287

SCALE | SHEET 1 OF

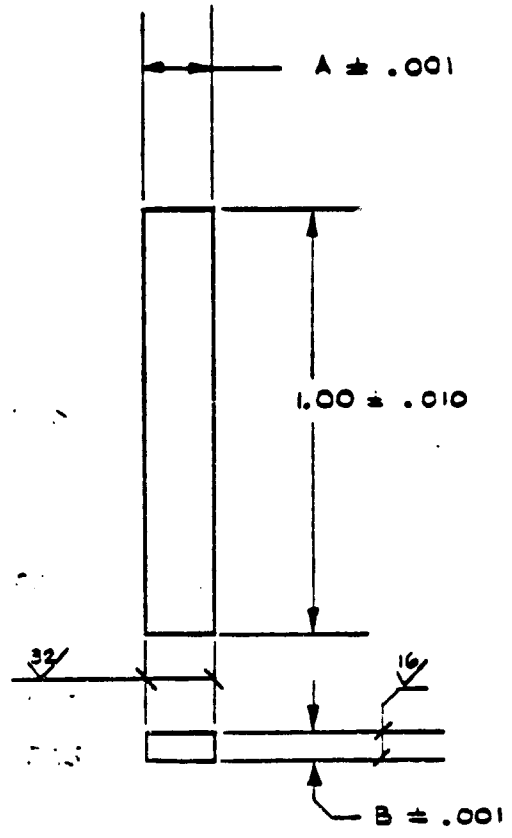
SYSTEMS 523 REV. 9-77

ORIGINAL PAGE IS
OF POOR QUALITY

SK

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

DASH NO	A	B
-001	.096	.041
-002	.096	.016
-003	.096	.006
-004	.118	.052
-005	.118	.016
-006	.118	.006
-007	.144	.065
-008	.144	.016
-009	.144	.028
-010	.219	.103
-011	.219	.031
-012	.219	.016
-013	.415	.160
-014	.415	.020
-015	.415	.025
-016	.219	.011
-017	.219	.006
-018	.219	.003
-019	.219	.026
-020	.219	.036



NOTE: 1. POLISH ALL SURFACES WITH STEEL WOOL
2. SHARP EDGES AND CORNERS

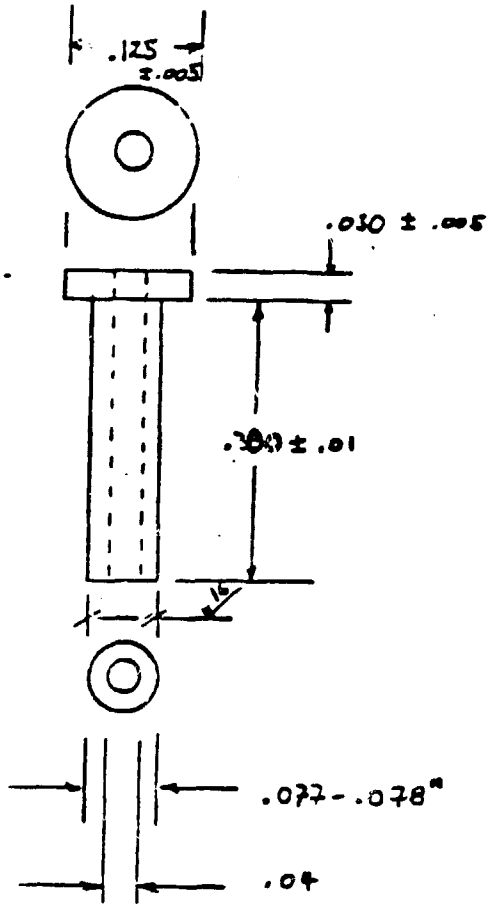
ENGINEERING SKETCH		TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR ROY EBERT	DATE JAN 23 1980	W/G SHORT BODY	
MATERIAL HALF HARD BRASS			
		SIZE A	FSCM NO. 11982
MJO		SCALE	SHEET 1 OF

SK 7325-286

SYSTEMS 333 REV. 8-77

SK

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



ENGINEERING SKETCH

TRW
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR	DATE
Erale Holmes	1/12/93
Material	
MF-124	

Eccosorb Loads

SIZE	FSCM NO.	
A	11982	SK C415-1138-001

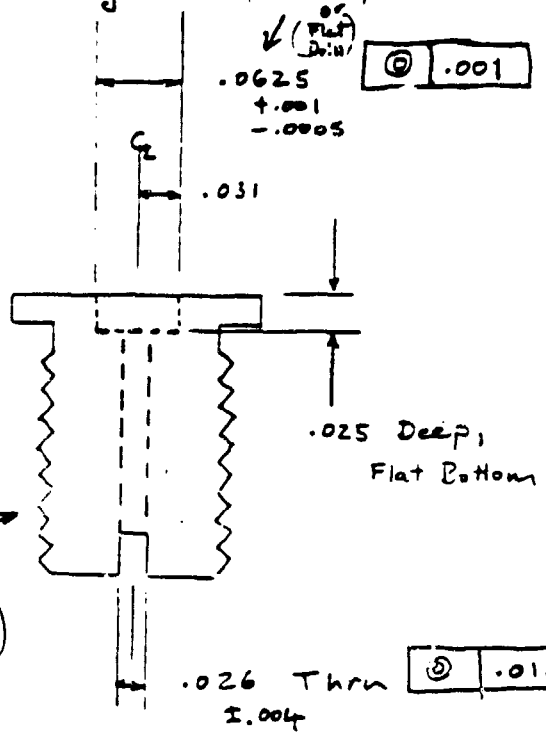
SCALE | SHEET 1 OF

ORIGINAL PAGE IS
OF POOR QUALITY

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

Steps:

1. Knock Ceramic Mesa off Stud
2. Center Thru Hole with Starting Drill (1/16 Mill)
3. Drill Thru Hole
4. Carbide End Mill Works Well to make Flat Bottomed Diode Well

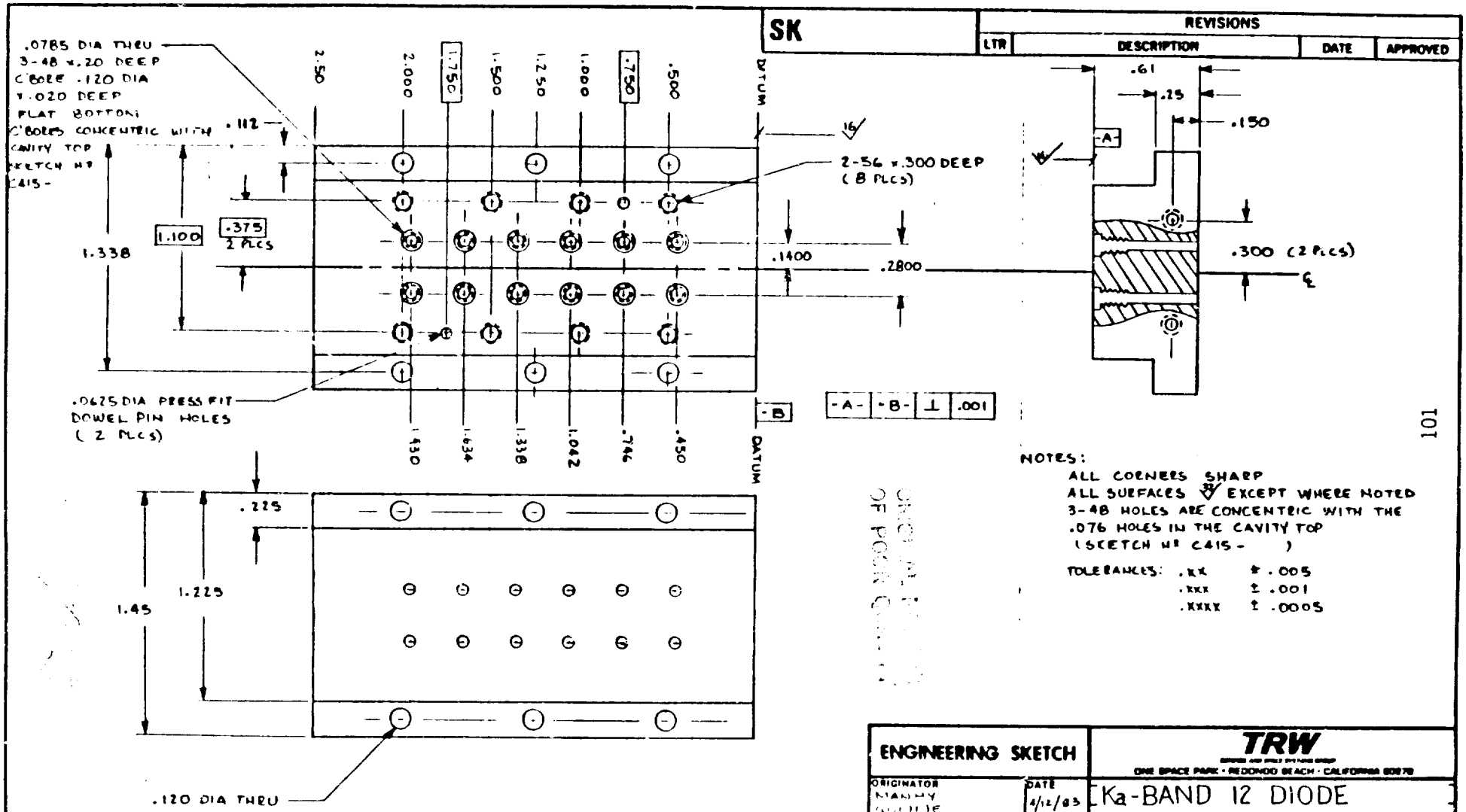


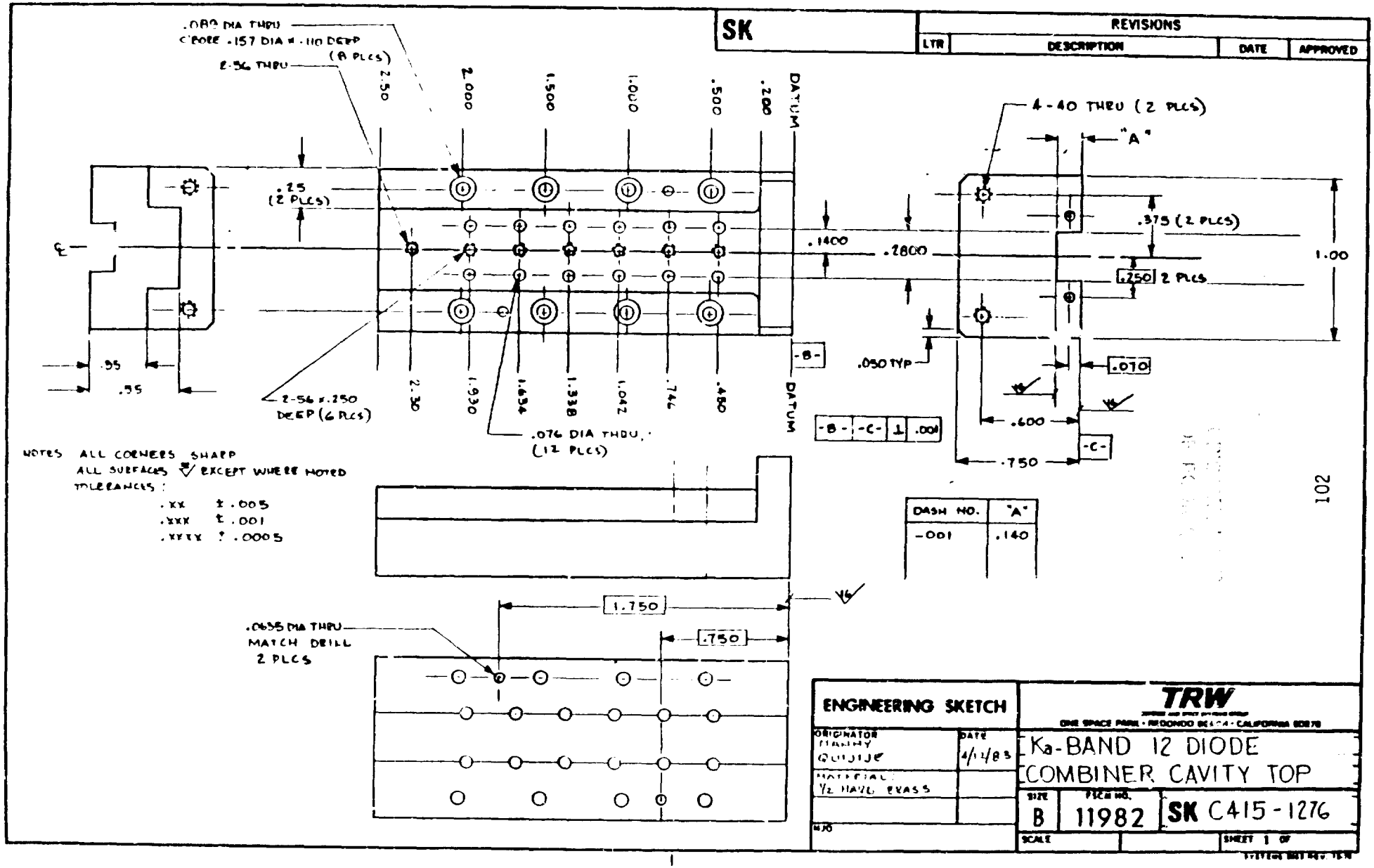
(μA) MA/COM # 422-41423
CASE STYLE 138

May hold threads in lathe collet - should meet ⌀ tolerances this way.

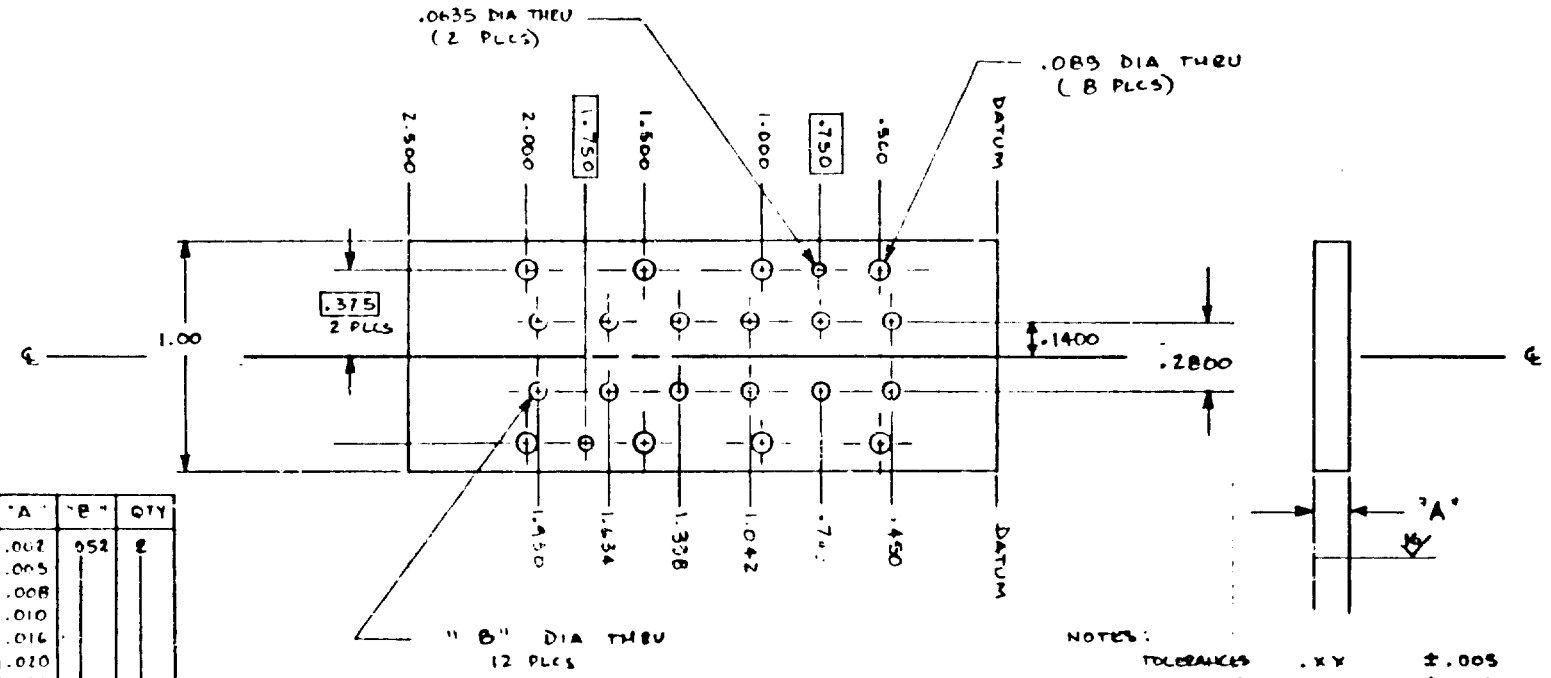
(.XXX = ±.001)

ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	Hole Location In Diode Stud	
E. Holmes	5/27/87		
X 61431			
		SIZE A · FSCM NO. 11982 · SK	
BLDG		SCALE	SHEET 1 OF


SK
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
.0785 DIA THRU
3-48 x.20 DEEP
C'BORE .120 DIA
x.020 DEEP
FLAT BOTTOM
C'BORES CONCENTRIC WITH
CAVITY TOP
SKETCH Nº
C415-
.112
1.338
1.100
.375
2 PLCS
2.50
2.000
1.750
1.500
1.250
1.000
.750
.500
DATUM
1.430
1.634
1.338
1.042
.746
.450
DATUM
2-56 x.300 DEEP
(8 PLCS)
.1400
.2800
.0625 DIA PRESS FIT
DOWEL PIN HOLES
(2 PLCS)
-A- -B- ⊥ .001
.61
.25
.150
-A-
.300 (2 PLCS)
.225
1.45
1.225
.120 DIA THRU
NOTES:
ALL CORNERS SHARP
ALL SURFACES 32 EXCEPT WHERE NOTED
3-48 HOLES ARE CONCENTRIC WITH THE
.076 HOLES IN THE CAVITY TOP
(SKETCH Nº C415-)
TOLERANCES: .XX ± .005
.XXX ± .001
.XXXX ± .0005
101
ENGINEERING SKETCH
ORIGINATOR
MANNY
DATE
4/12/83
MATERIAL:
TUNGSTEN COPPER
M/O
TRW
ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278
Ka-BAND 12 DIODE
COMBINER CAVITY BOTTOM
SIZE
B
FSCM NO.
11982
SK C415-1277
SCALE
SHEET 1 OF


SK
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
.080 DIA THRU
C'BORE .157 DIA x .110 DEEP
(8 PLCS)
2-56 THRU
2.500
2.000
1.500
1.000
.500
.200
DATUM
.25
(2 PLCS)
.1400
.2800
4-40 THRU (2 PLCS)
"A"
.375 (2 PLCS)
.250 2 PLCS
1.00
.55
.55
2-56 x .250
DEEP (6 PLCS)
2.350
1.930
1.634
1.338
1.042
.746
.450
DATUM
-B-
.076 DIA THRU,
(12 PLCS)
.050 TYP
-B- -C- ⊥ .001
.070
.600
-C-
.750
NOTES ALL CORNERS SHARP
ALL SURFACES 63 EXCEPT WHERE NOTED
TOLERANCES:
.XX ± .005
.XXX ± .001
.XXXX ± .0005
DASH NO. | "A"
-001 | .140
1.750
.750
.0635 DIA THRU
MATCH DRILL
2 PLCS
ENGINEERING SKETCH
TRW
ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278
ORIGINATOR
TIMOTHY QUIJIJE
DATE
4/14/83
MATERIAL
½ HARD BRASS
Ka-BAND 12 DIODE
COMBINER CAVITY TOP
SIZE
B
PICA NO.
11982
SK C415-1276
SCALE
SHEET 1 OF
102

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



NOTES:

TOLERANCES

.XX	±.005
.XXX	±.001
.XXXX	±.00-5

DASH NO	"A"	"B"	QTY
-001	.002	.052	2
-002	.005		
-003	.008		
-004	.010		
-005	.016		
-006	.020		
-007	.032		
-008	.035		
-009	.040		
-010	.045		
-011	.050		
-012	.002	.076	
-013	.005		
-014	.008		
-015	.010		
-016	.016		
-017	.020		
-018	.032		
-019	.035		
-020	.040		
-021	.045		
-022	.050		
-023	.042		
-024	.033		

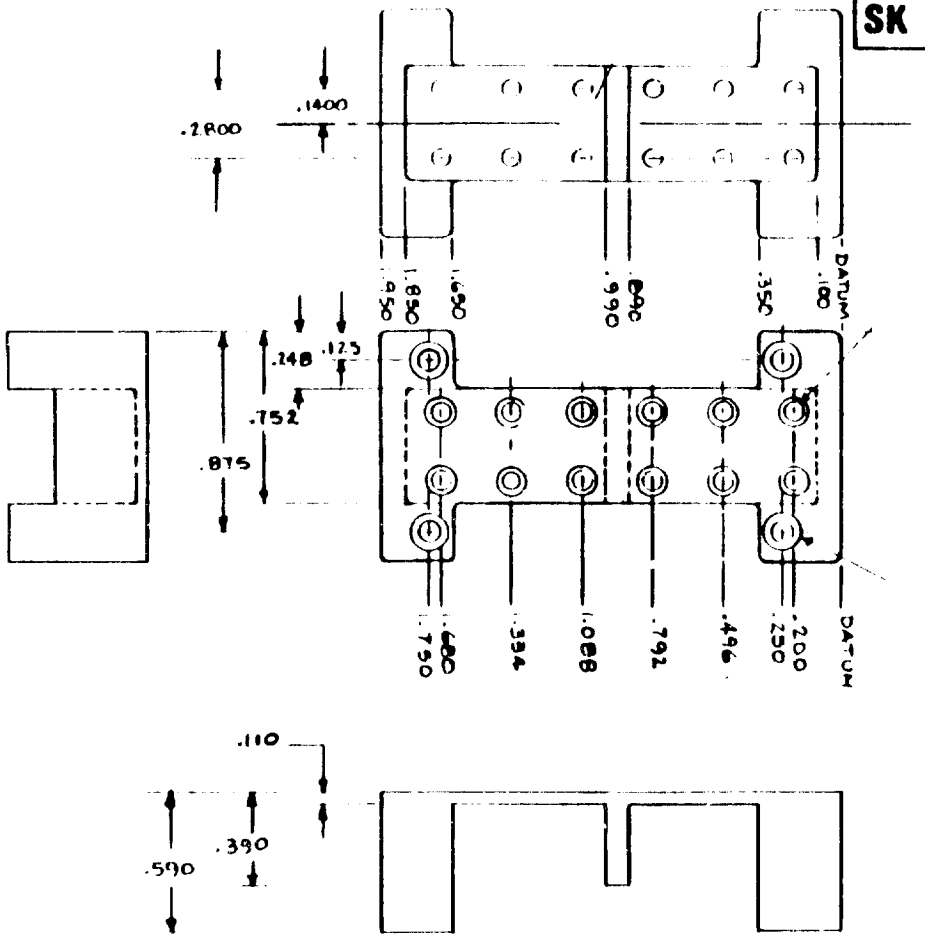
DASH NO	"A"	"B"	QTY
-025	.125	.076	2
-026	.150		
-027	.200		
-028	.250		

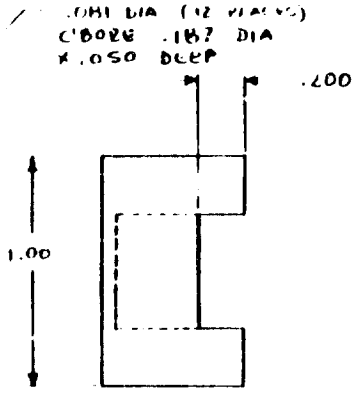
ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278
ORIGINATOR [illegible]	DATE 4/12/85	Ka-BAND 12 DIODE COMBINER SHIM PLATES
MATERIAL: 1/2 HARD BRASS		SIZE B · PICM NO. 11982 · SK C415-1278
MJO		SCALE · SHEET 1 OF

103

SK

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





.089 DIA THRU
C'BORE .157 DIA X .110 DEEP
(4 PLACES)

TOLERANCES
.XX ±.005
.XXX ±.001
.XXXX ±.0005

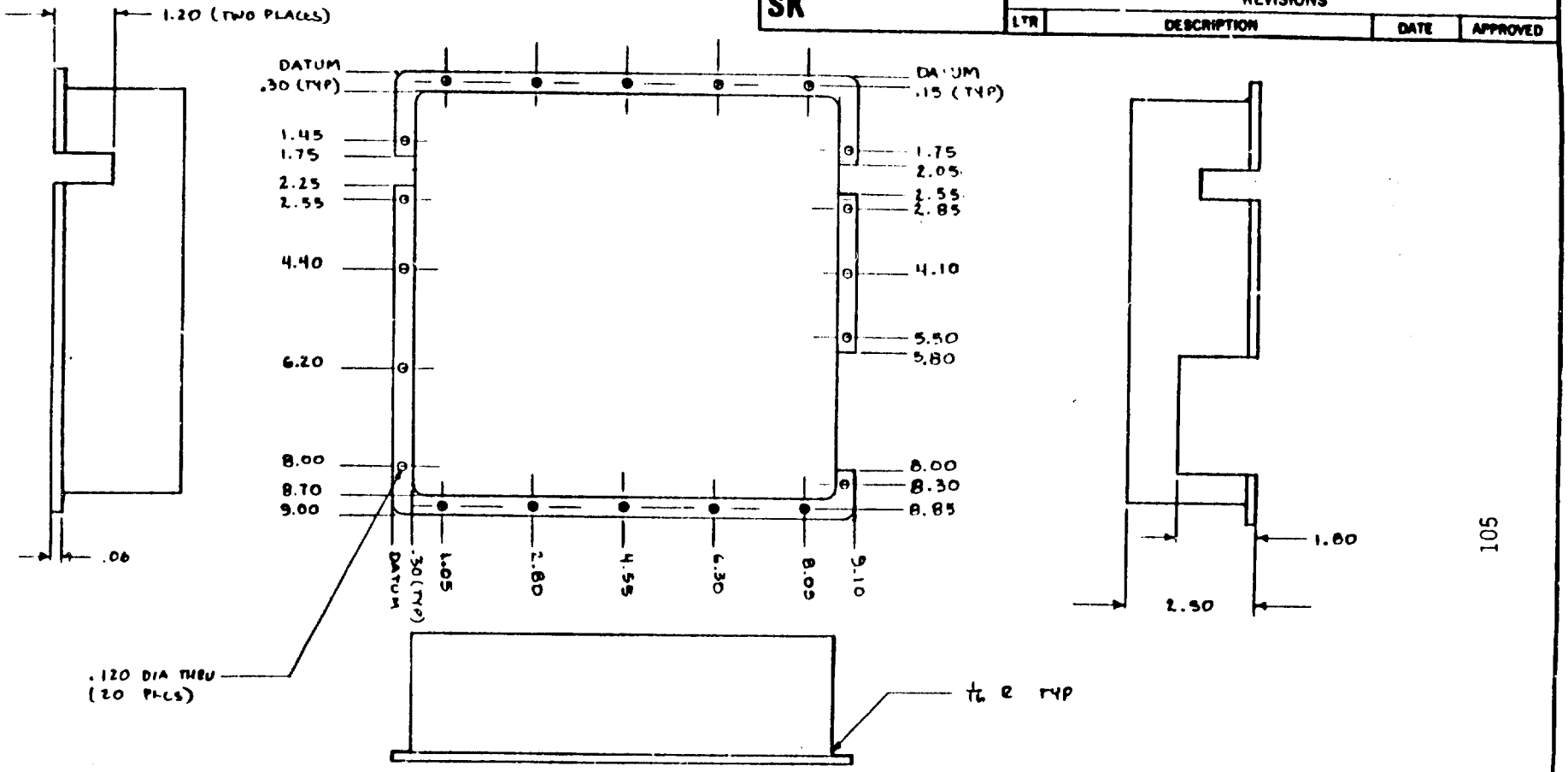
104

ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278	
ORIGINATOR MANNY QUIJIJE	DATE APRIL 4 1984	COMBINER TOP CONNECTOR	
MATERIAL [illegible]		SIZE B	PECM NO. 11982
TYPE GEE		SCALE	SHEET 1 OF
MFG			

SK (414-1559

SK

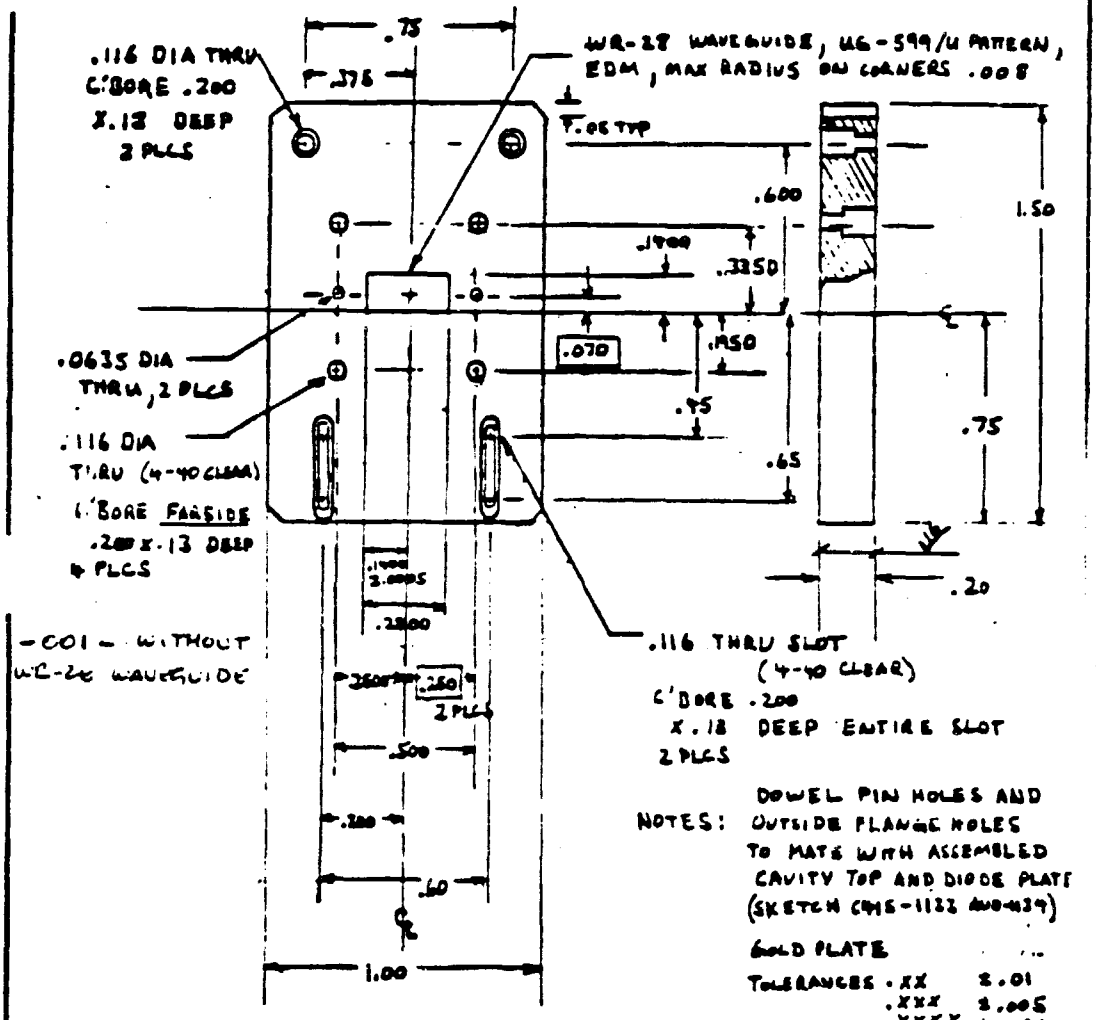
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



105

ENGINEERING SKETCH		TRW ONE SPACE PARK · REDONDO BEACH · CALIFORNIA 90278	
ORIGINATOR MANNY QUIJIJE	DATE 9/14/84	30 GHz SSA COVER	
MATERIAL ALUMINUM .060 THICK.		SIZE B	PSCM NO. 11982 SKC414-
MJQ		SCALE	SHEET 1 OF

SK C415-1136	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

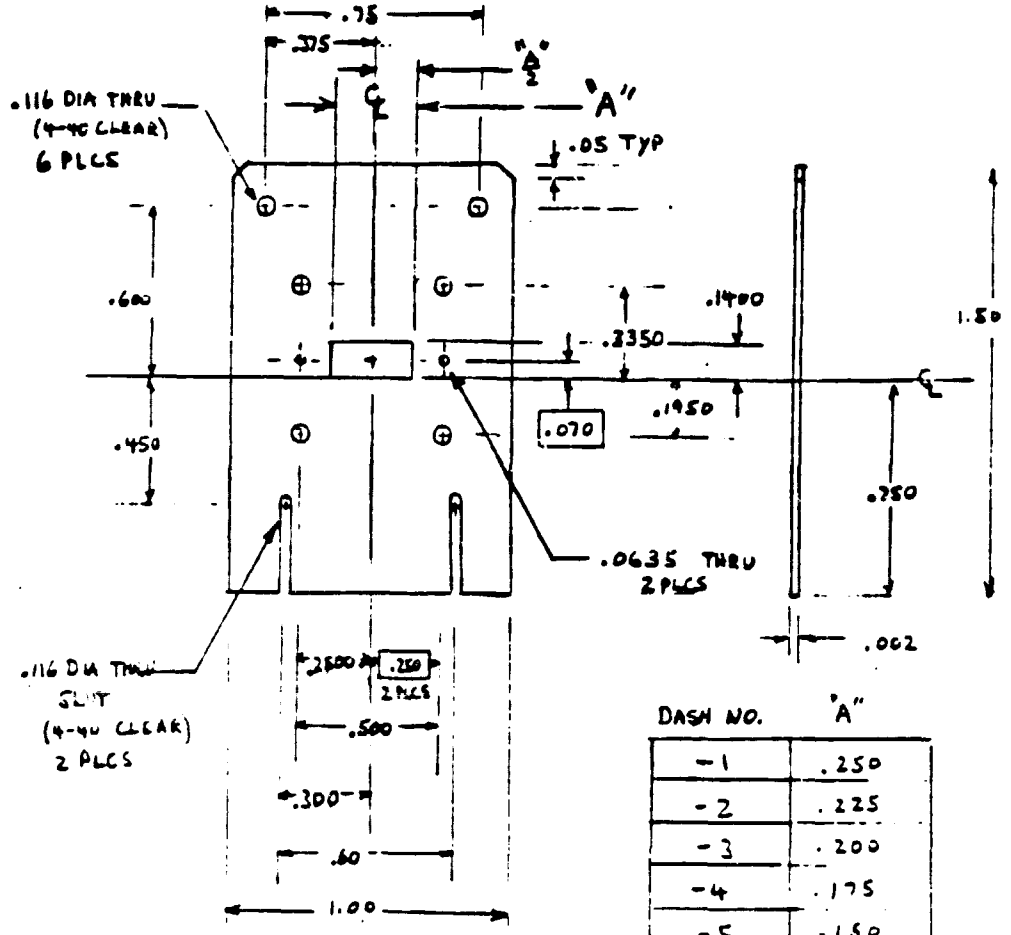


NOTES:
1. DOWEL PIN HOLES AND OUTSIDE FLANGE HOLES TO MATE WITH ASSEMBLED CAVITY TOP AND DIODE PLATE (SKETCH CH15-1133 AND-1134)
2. GOLD PLATE

TOLERANCES .XX ±.01
.XXX ±.005
.XXXX ±.001

ENGINEERING SKETCH	TRW ONE SPACE PARK · REDONDO BEACH, CALIFORNIA	
ORIGINATOR: M. QUIJIJE	DATE: 11/8/82	.12 DIODE COMBINER - ADAPTER PLATE
MATERIAL: 1/2 HARD BRASS		SIZE: A · FSCM NO.: 11982 · SK C415-1136
NUMBER		SCALE · SHEET 4 OF 6

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



DASH NO.	"A"
-1	.250
-2	.225
-3	.200
-4	.175
-5	.150
-6	.125
-7	.100

NOTES

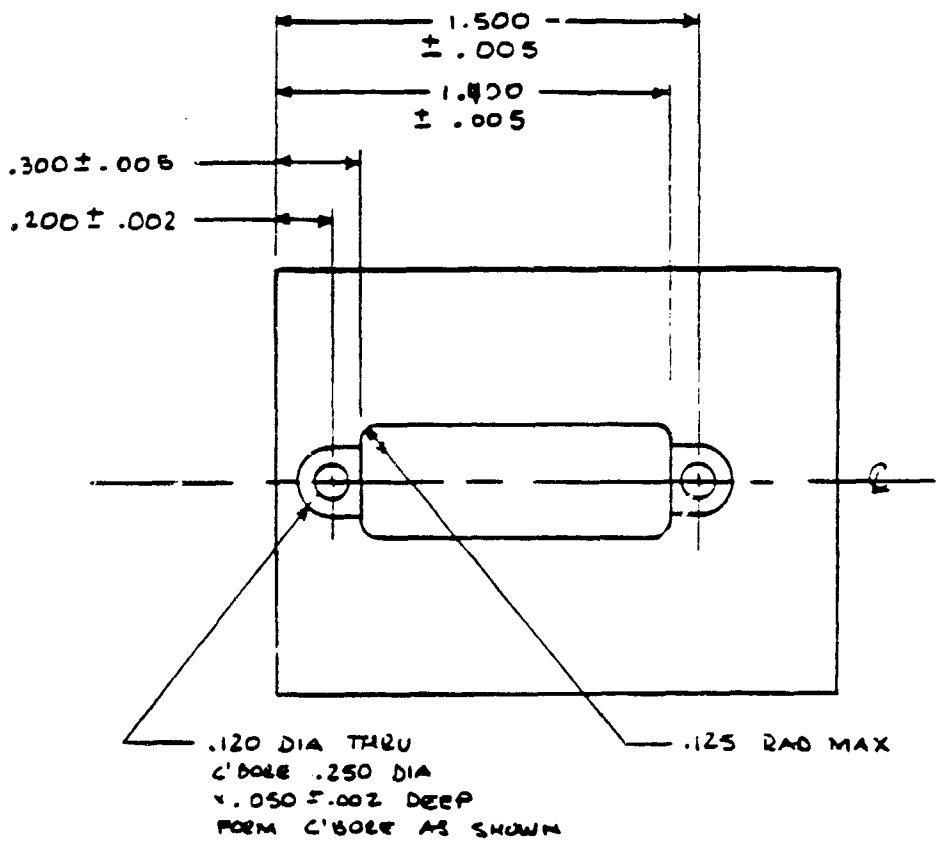
1. HOLES CONCENTRIC WITH FLANGE AND FLANGE ADAPTER Ⓜ .002 (SK C415-1136)
2. GOLD PLATE

TOLERANCES .XX ± .01 , .XXX ± .005 , .XXXX ± .001

ENGINEERING SKETCH	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR: M. QUIJIJE	DATE: 11/8/82	12 DIODE COMBINER COUPLING IRIS
Material: BERYLLIUM COPPER SHIM STOCK MJQ		SIZE: A · PSCM NO.: 11982 · SK C415-1137-
		SCALE · SHEET 5 OF 6

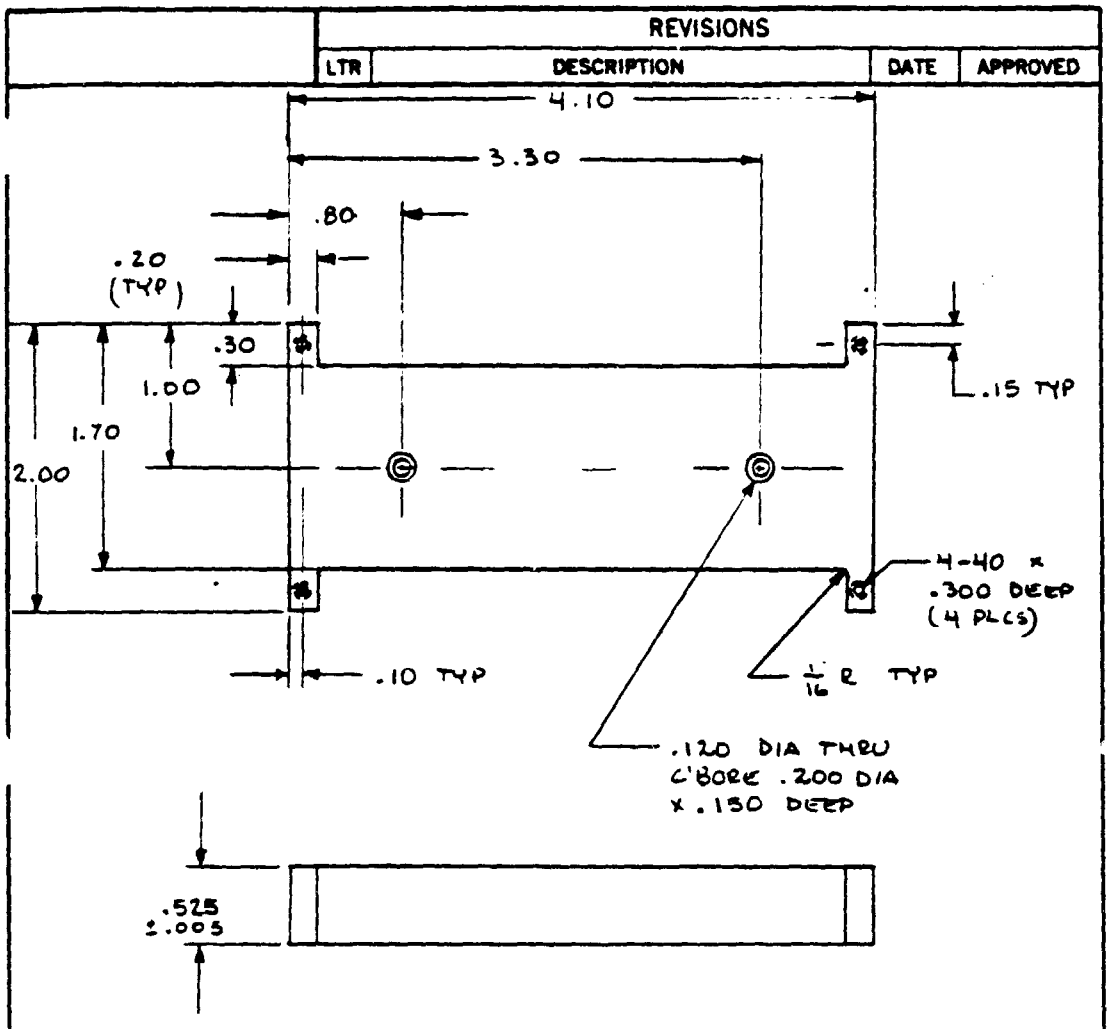
ORIG
OF P

	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



ORIGINATOR	DATE	TRW ONE SPACE PARK, REDONDO BEACH, CALIF 90278
		MODIFY Box (REGULATOR BOX
JN		SIZE A · CODE IDENT NO. 11982
		SCALE · SHEET 1 OF

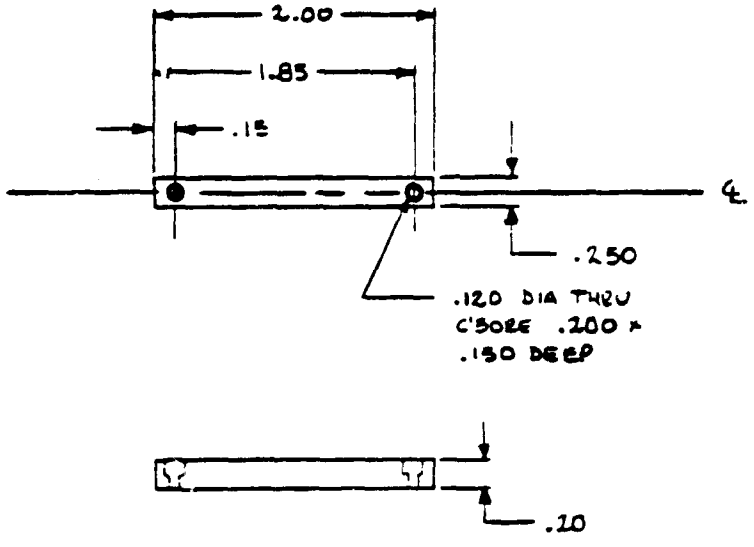
SYSTEMS 523 REV. 12-62



ORIGINATOR: MANNY QUIJIJE	DATE: 5/14/84	TRW ONE SPACE PARK, REDONDO BEACH, CALIF 90278
MATERIAL: ALUMINUM		30 GHz 55A CIRCULATOR BRACKET
		SIZE: A; CODE IDENT NO.: 11982; C414-
JN		SCALE; SHEET 1 OF

SYSTEMS 523 REV. 12-82

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TRW
ONE SPACE PARK, REDONDO BEACH, CALIF. 90278

ORIGINATOR Manny Quijje	DATE 5/14/85
MATERIAL ALUMINUM	
JN	

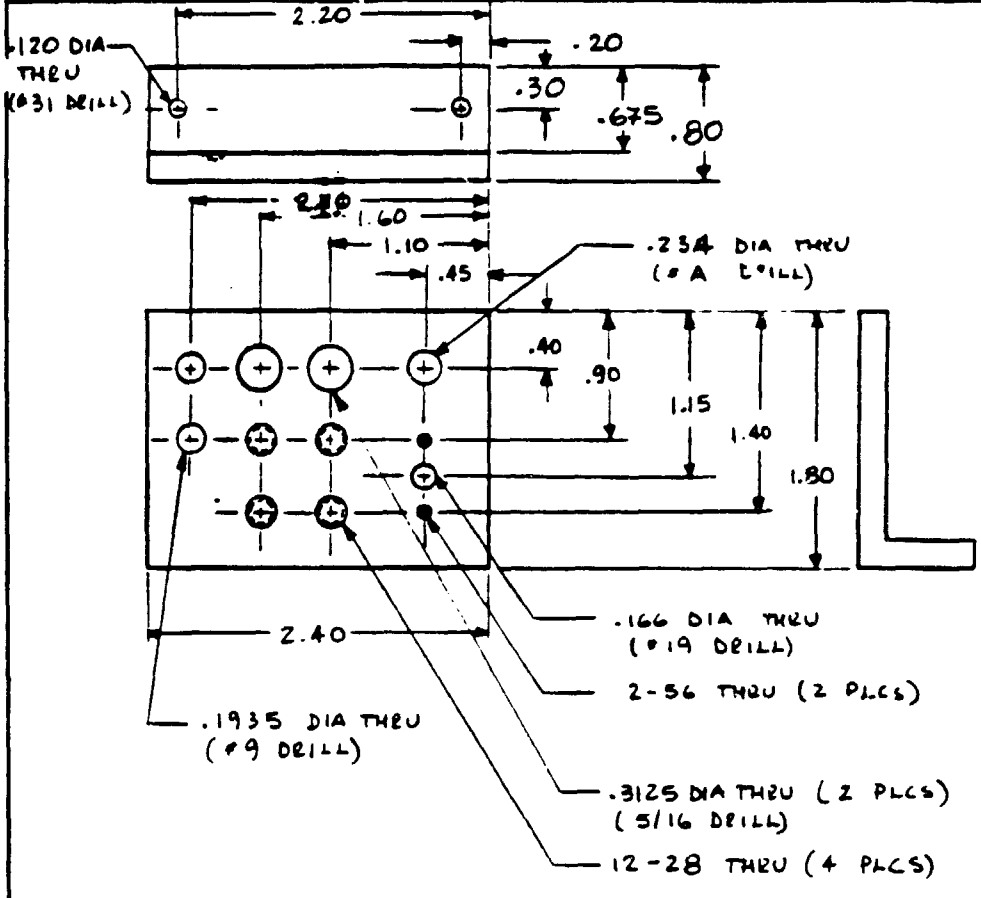
30 GHz SSA CIRCULATOR
BRACKET (TOP BAR)

SIZE	CODE IDENT NO.
A	11982

SCALE | SHEET 1 OF

SYS/ENG 523 REV. 12-82

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



ORIGINATOR: DANNY QUIJIJE	DATE: APRIL 30, 1984
MATERIAL: AL.	
JN	

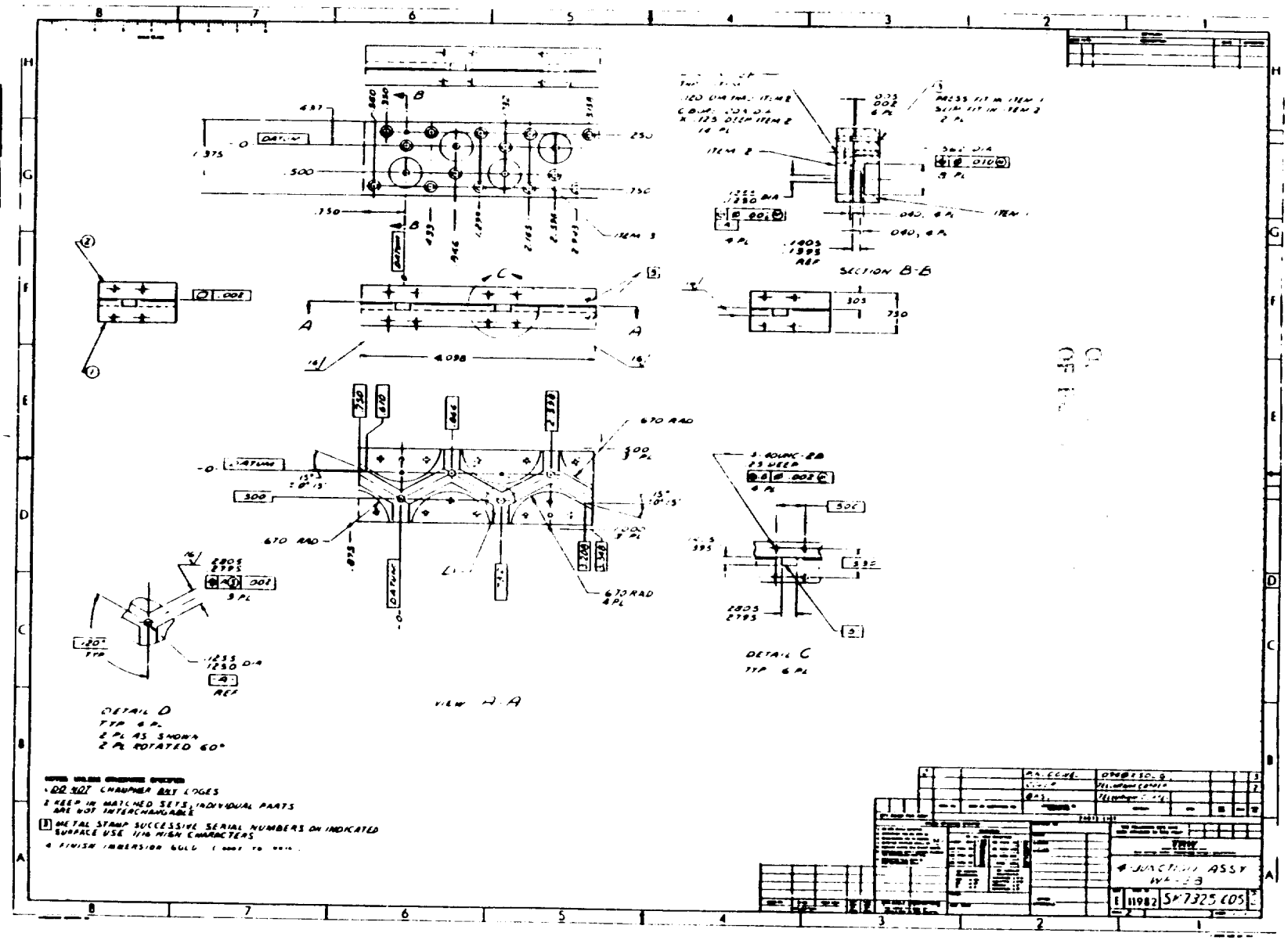
TRW
ONE SPACE PARK, REDONDO BEACH, CALIF 90278

30 GHz SSA DC CONNECTOR BRACKET

SIZE	CODE IDENT NO.
A	11982

SCALE | SHEET 1 OF

SYSTEMS 523 REV. 12-82


SECTION B-B
DETAIL C
TYP 6 PL
DETAIL D
TYP 4 PL
2 PL AS SHOWN
2 PL ROTATED 60°
VIEW A-A
4 JUNCTION ASSY
SK7325-605

APPENDIX B

30 GHZ SOLID STATE AMPLIFIER

FOR LOW COST LOW DATA RATE GROUND TERMINALS

TASK X REPORT

TECHNOLOGY ASSESSMENT

One Space Park, Redondo Beach
California 90278

July 1984

Prepared for:

National Aeronautics and Space Administration
Lewis Research Center
21000 Brookpark Road
Cleveland, Ohio 44135

30 GHz SOLID STATE AMPLIFIER

1. Introduction

A review is presented of the important design factors governing the power and efficiency of 30 GHz solid state amplifier in order to estimate the amplifier performance that might be expected in 1987. The key factors involved are the electronic conversion efficiency of the diode, the performance limitations imposed by the diode package parasitic impedances and the thermal characteristics of the diode. Another consideration discussed briefly is the possibility of utilizing arrays of diode chips to increase the power levels. However, circuit level power combining is still considered to be the most realistic approach to achieving higher power.

It should be emphasized that while some of the anticipated improvements in performance will result simply from a straight-forward extrapolation of existing technology, some are based on speculative ideas which may be difficult or impossible to achieve. Further, it is not possible to anticipate "break-throughs" in material technology and device designs, or the modes of device operation. However, while a precise assessment of 1987 technology may not be feasible, the assessment can be used to provide at least a lower bound to the improvements expected and an upper bound beyond which higher powers cannot be expected realistically.

2. Basic Power Output Equation

The important parameters that determine the output power of an IMPATT dide are:

η_c = electronic conversion efficiency

η_{ckt} = external circuit efficiency

η_d = diode circuit efficiency

ΔT = increase in diode junction temperature (°C)

θ = thermal resistance of the diode (°C/W)

In terms of these parameters, the power output of the diode, P_o, is given by

$$P_o = \eta_{ckt} \left(\frac{\eta_d \eta_c}{1 - \eta_d \eta_c} \right) \left(\frac{\Delta T}{\theta} \right)$$

Each of these factors is discussed below and a range of expected values of P_o is calculted.

3. Electronic Conversion Efficiency

For low cost and reproducibility considerations, it is anticipated that the double-drift flat profile silicon IMPATT diode will be used. Large signal computer simulation for double-drift flat profile indicated that c-to-RF conversion efficiency between 12 and 14% can be achieved, and this is not expected to change drastically for the next three years. For double-drift Read profile based on GaAs, efficiency of as high as 20% can be projected for 1987. However, this type of IMPATT diode tends to be more expensive to fabricate and to have a much lower yield than silicon IMPATT. It is therefore not attractive for low cost applications.

4. Diode Package Parasitic Impedances

It is well known that diode package parasitic impedances play a major role in affecting the performance of negative resistance oscillators and amplifiers. This problem has been thoroughly examined in the case of tunnel diodes [1] and the analysis developed applies equally well to the IMPATT diode. Figures 1 and 2 are of particular interest for this discussion. Figure 1 is useful in providing an insight into the effect of L_s on the effective impedance of the diode and the maximum practical diode area. Figure 2 is useful to demonstrate the important role of R_s in degrading the power output of the diode as an oscillator.

a. Effect of Lead Inductance

Figure 2 shows that an external circuit consisting of an equivalent inductance L and a load resistance R_L is required to tune the diode. Actually R_L consists of two parts: a resistance corresponding to the coupled-in external load and a resistance associated with losses in the external circuit. It should be noted that the lower the impedance of the diode, the lower will be the required value of L. Unfortunately, because of their small volume, low L circuits have higher values of loss resistance. In effect, the circuit efficiency, η_{ckt}, will decrease as the diode impedance decreases. In practice, it has been established that reasonable values of η_{ckt} results when the diode reactive impedance is greater than about 5 ohms. It is believed that the circuit efficiency will drop rapidly at the lower impedance values. Circuit efficiencies ranging from 0.9 to 0.95 are expected in practical circuits.

If in Figure 1a we neglect the effect of R_j and R_s on the reactive part of the diode impedance we can show that the area of the diode chip, A, is related to the diode impedance x_d, the case capacitance C_c, the

series inductance, L_s, and the angular frequency ω by

$$A = \frac{1}{\frac{\omega \varepsilon}{d} \quad \frac{X_d}{1 - \omega C_c X_p} + \omega L_s}$$

where d is the depletion width of the diode and ξ is the permittivity of GaAs.

Figure 3 shows a plot of the area required to maintain a 10 ohm reactive diode impedance as a function of the lead inductance, with C as a parameter. It is seen that large inductances and case capacitances lower the required diode area. This means, of course, that less power will be available from the diode as compared with the ideal diode with no parasitics. In 30 GHz diodes, typical values of L and C are 0.2×10^{-9} H and 0.1×10^{-12} F, respectively. This results in a reduced area of about 75% from the ideal case. With further refinements in diode packaging technology it may be possible to achieve approximately a 10% increase in the area and therefore a 10% increase in the output power.

b. Effect of Diode Series Resistance

The series resistance R_s, shown in Figure 1 and 2 is the combined resistance of the ohmic contacts, the spreading resistance and the contact resistances of the diode. Since all of the RF current must pass through this resistance, it degrades the power capabilities.

As shown by Barber and Bertram, the power loss in the series resistor is

$$P_R = \frac{V_1^2}{2R_{eq}^2} \quad R_s \quad (1 + w^2 C^2 R_{eq}^2)$$

where $\frac{V_1^2}{2R_{eq}}$ is the power generated, P_G, in the negative resistance. The useful output power, P_o, is

$$P_o = P_G \left(1 - \frac{R_s}{R_{eq}} - R_s w^2 C^2 R_{eq} \right)$$

Since $P_o = n_d P_G$, where n_d is the diode circuit efficiency, we have

$$n_d = 1 - \frac{R_s}{R_{eq}} (1 + Q_e)^2$$

or

$$n_d = 1 - \frac{1}{Q_e Q_d} (1 + Q_e)^2$$

where $Q_e = wCR_{eq}$, the electronic diode Q and $Q_d = (wCR_s)^{-1}$, the diode chip Q. Figure 4 is a plot of this equation showing the diode circuit efficiency as a function of the diode chip Q with the electronic diode Q as a parameters.

For infinite values of Q_d, the efficiency approaches unity. With careful device design and fabrication, circuit efficiency values of approximately 95% should be achievable.

5. Diode Thermal Properties

Two critical parameters that effect the output power of an IMPATT diode are ΔT, the increase in junction temperature that occurs when DC power is dissipated within the diode, and θ, the thermal resistance, which is a measure of the diodes ability to conduct heat away from the diode chip. ΔT is typically limited to about 200°C. Operating at values above this could drastically reduce the mean time before failure. Until a considerable amount of research on diode

reliability has demonstrated the feasibility of higher temperature operation, conservative values of ΔT ranging from 200°C to about 275°C should be assumed.

The value of the thermal resistance is dependent on the spreading resistance which is given approximately by

$$\theta = \frac{1}{\pi r K_\eta} + \frac{L_s}{\pi r^2 K_s} + \frac{L_m}{\pi r^2 K_m}$$

where r is the radius of the diode, L_s and L_m are the lengths of the semiconductor contact region and metal contact regions, respectively, and K_n, K_s, and K_m are, respectively the thermal conductivities of the heat sink, the semiconductor contact material and the metal region. Figure 5 is a plot of this equation for copper and diamond heat sinks. For the range of areas expected for the 30 GHz diode, a thermal resistance of between 11.0 and 12.0 W/°C is expected using the diamond heat sink.

Another structure which can potentially further reduce the thermal resistance of IMPATT diode is the so-called ring diode structure as shown schematically in Figure 6. In this structure, the heat dissipation is spread out over an annular area instead of concentrated under a circular disc, thereby resulting in significant reduction in thermal resistance.

A comparison of the thermal resistance of ring and solid disk diodes versus diameter ratio is shown in Figure 7 for equal areas [2]. The diameter ratio (b/c) is the ratio of the inside diameter of the ring (b) over the outside diameter (c). The larger the diameter ratio, the lower the thermal resistance of the ring diode (R_R) as compared to the solid disk (R_D). Ring diodes are thermally superior to solid disk diodes for diameter ratios greater than 0.1.

To reduce the thermal resistance from 12° to 8° C/W, the ratio $R_R / R_D = 0.66$. From Figure 7, this corresponds to a diameter ratio of $b/c = 0.8$. Therefore, ring IMPATT diodes with an aspect ratio of $b/(c-b) = 4$ will reduce the thermal resistance to the required value.

6. Power From Single Mesa Devices (Diamond Heat Sink)

Using the power output equation discussed in Paragraph 2 and assuming first a conservative set of parameters and then an optimistic set, the power available from 1987 diodes is estimated below.

Parameter	Conservative 1987 Value	Optimistic 1987 Value
η_c	0.14	0.20
η_d	0.90	0.95
η_{CKT}	0.90	0.95
ΔT	250° C	250°C
θ	10° C/W (R_d)	6.6° C/W (R_R)
P_{out}	3.5 W	8.9 W

These results show that single mesa diode oscillator/amplifiers have power outputs ranging from about 3.5 Watts at least, to about 9 Watts at most.

7. Chip-Level Power Combiners

An attractive concept to attain high power levels from IMPATT diodes is to connect together, both electrically and mechanically, two or more diode chips. For example, two chips can be connected electrically in series, but thermally in parallel. The two chips can be made twice the normal size area so that the diode reactance remains

equal to that of the optimum single chip diode. A major problem lies in the control of the parasitic reactances discussed in paragraph 4. It is impossible to interconnect the diode chips without introducing additional lead inductances. As discussed, added inductances will modify the diode impedance so that the expected factor of four improvement cannot be achieved. In addition, the two chip device tends to be prone to subharmonic oscillate or bias circuit oscillate. Nevertheless, it may prove fruitful to explore techniques for chip-level combining. It may, for example, be possible to use millimeter wve diode fabrication techniques to minimize theeffect of the parasitic impedances at 30 GHz. If successful, diodes ranging in powr from 7 to 16 Watts may be feasible. However, it is important to note that provisions must be provided to remove the additional heat generated within the diode.

8. Circuit Level Power Combining

As mentioned in the Introduction, circuit level combining remains to be the most promising approach to achieving high output power levels. Two techniques are presently available which would allow for between two-fold to three-fold increase in the currently achieved 20 W output power. The first approach uses a 3-dB hybrid coupler or magic-tee to combine two 20 W modules to achieve close to 40 W output powers, as shown in Figure 8. This approach is straightforward and involves little risk. The second approach utilizes dual-diode modules capable of 4 W output power as basic building blocks and, by combining them via a 16-way radial line divider/combiner structure, total output power in excess of 50 W can be achieved. Figure 9 shows a schematic of such a combining concept.

9. Reliability and Low Cost Considerations

As a result of a study effort of the 30/20 GHz communication system sponsored by NASA Lewis Research Center, certain revised

requirements for the solid state amplifier emerged. In the present design, the amplifier consists of a single-diode driver module followed by a 12-diode power combiner. While the latter is capable of graceful degradation, the driver module does not possess any soft fail charcteristics. Furthermore, the 20 mW input power is not typical of what can be generated by an upconverter in the real system, which is more likely to be around -10 dBm. In order to address these issues, a driver amplifier development was proposed by TRW, which consists of the following requirements:

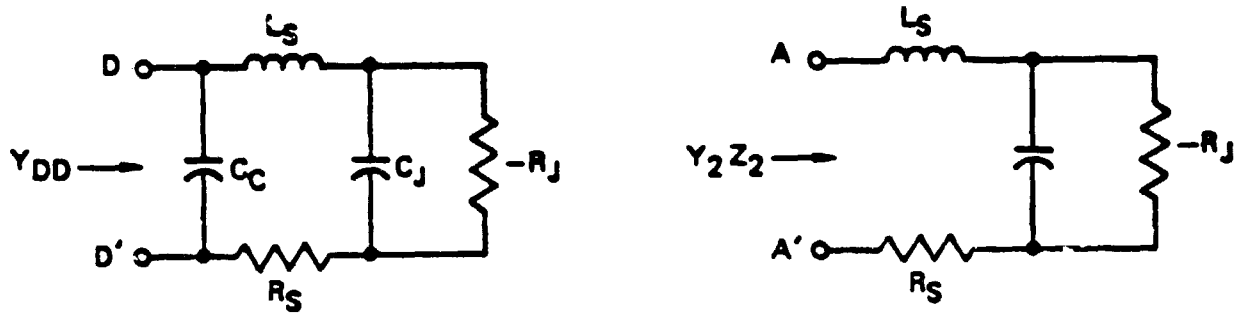
- 2.5 W (34 dBm) output power capability
- 4+ dB gain (- 10 dBm input drive)
- Microstrip Integrated Circuit (MIC) design for low cost
- Build-in redundancy to increase reliability

The detailed development plan for this low cost driver can be found in Appendix A.

References

[1] "Microwave Semiconductor Devices and their Circuit Applications," H. A. Watson, Editor McGraw-Hill Book Company, 1969, Chapter 14 "Tunnel Diode Circuits" by M. R. Barber and W. J. Bertram

[2] G. T. Culbertson and H. L. Stover, IEE Electron Devices, E D-19, 1972, pp. 986.



(a) (b)

Figure 1. (a) Equivalent circuit of packaged diode showing negative resistance and capacitance of the junction. (b) Equivalent circuit of packaged diode with the case capacitance omitted

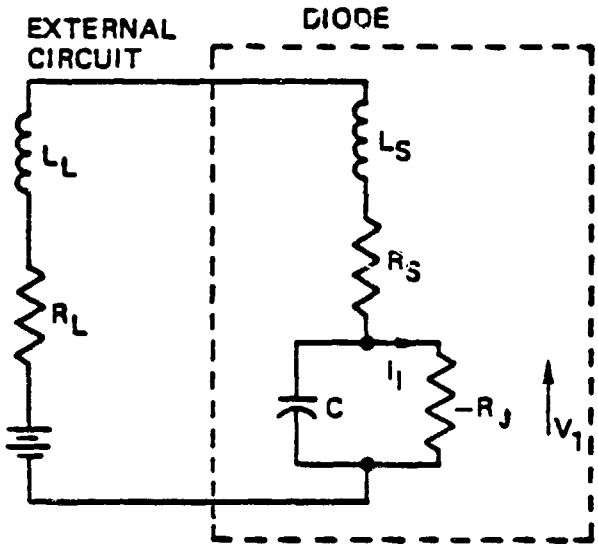


Figure 2. Sinusoidal oscillator circuit (after Watson)

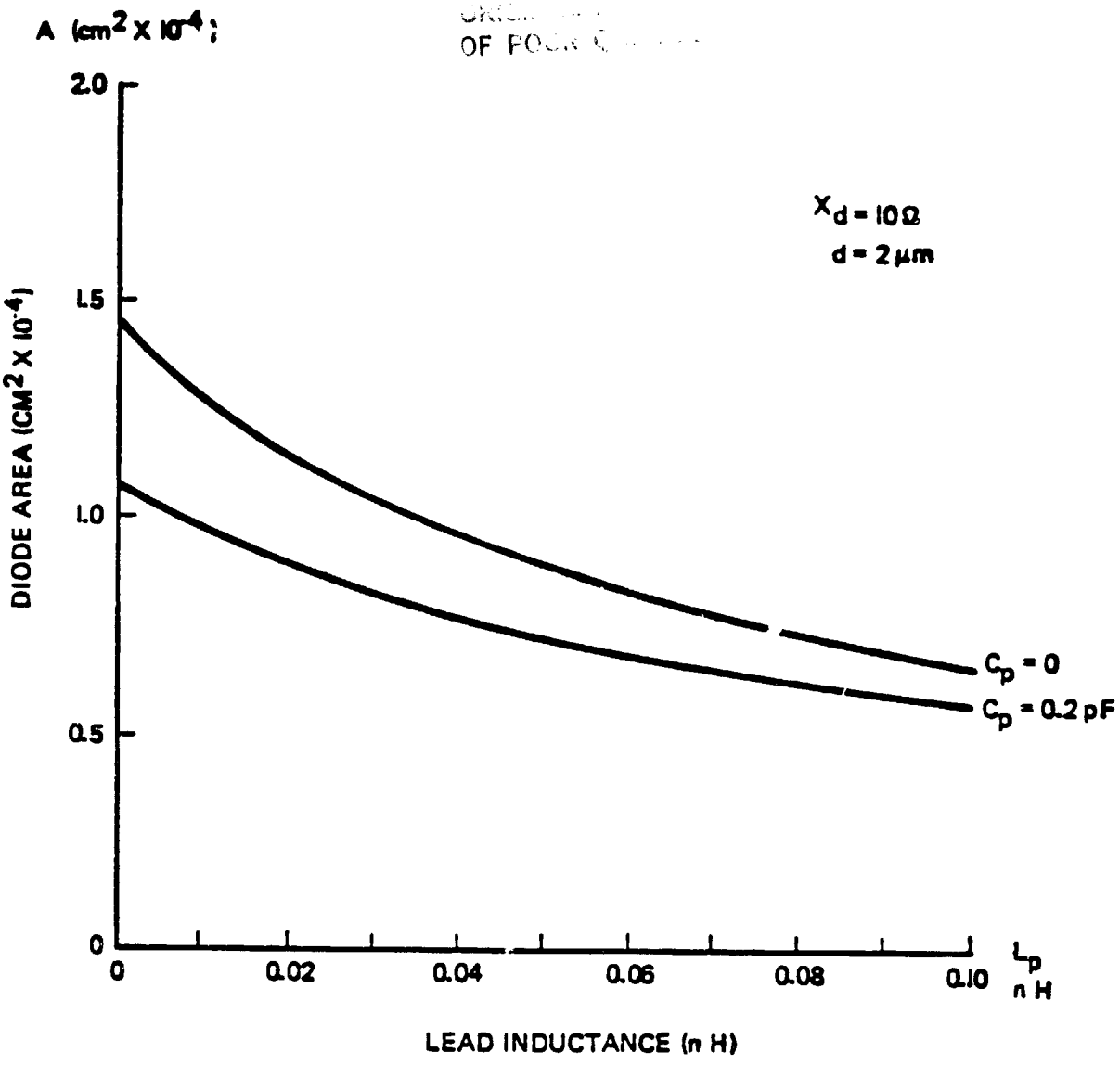


Figure 3. Diode area required to provide X_d = 10 ohm as a function of lead inductance

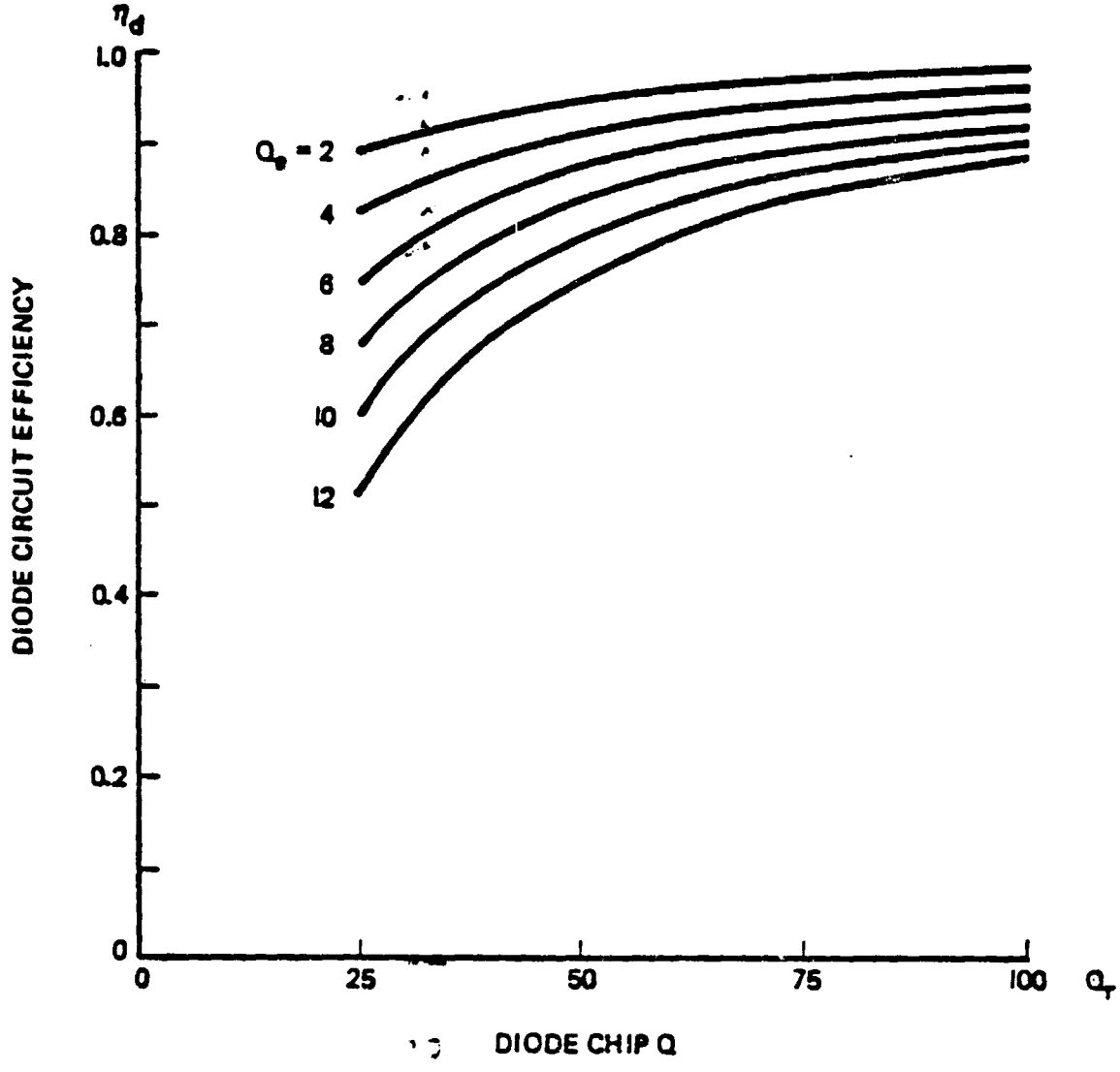


Figure 4. Diode circuit efficiency as a function of diode chip Q with diode electronic Q as a parameter

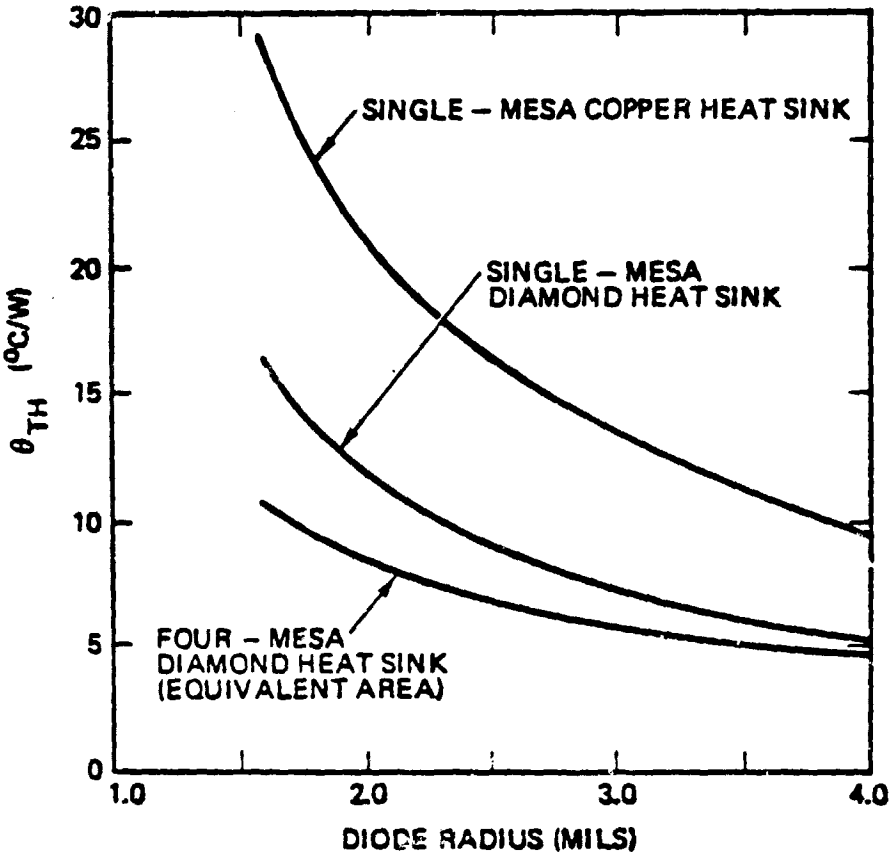


Figure 5. Calculated thermal resistance for a typical single mesa IMPATT diode with copper and diamond heatsink

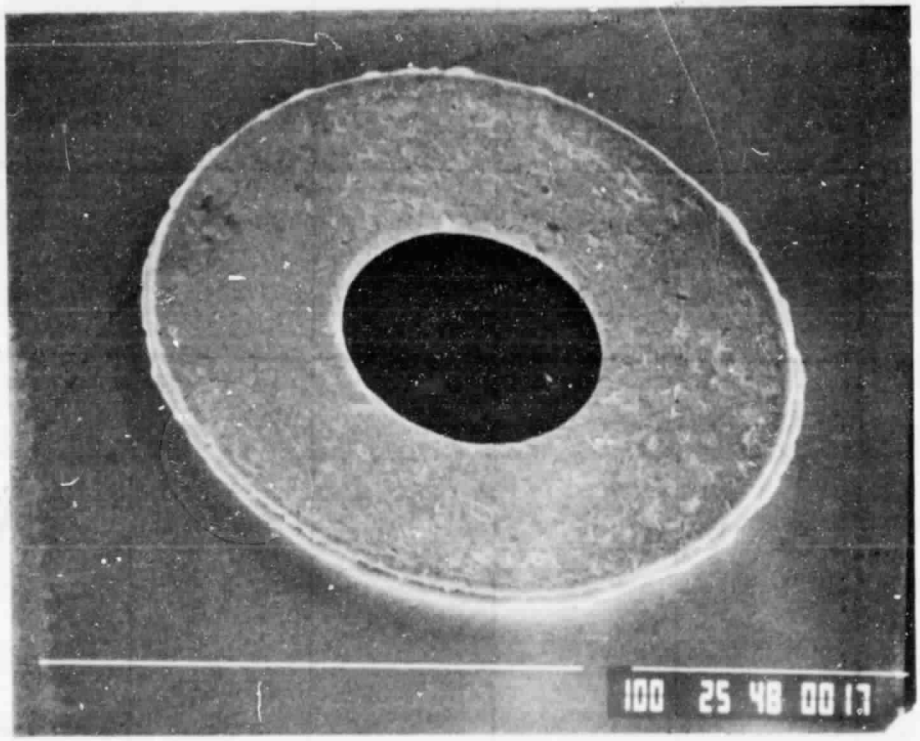


Figure 6. SEM photograph of ring diode structure

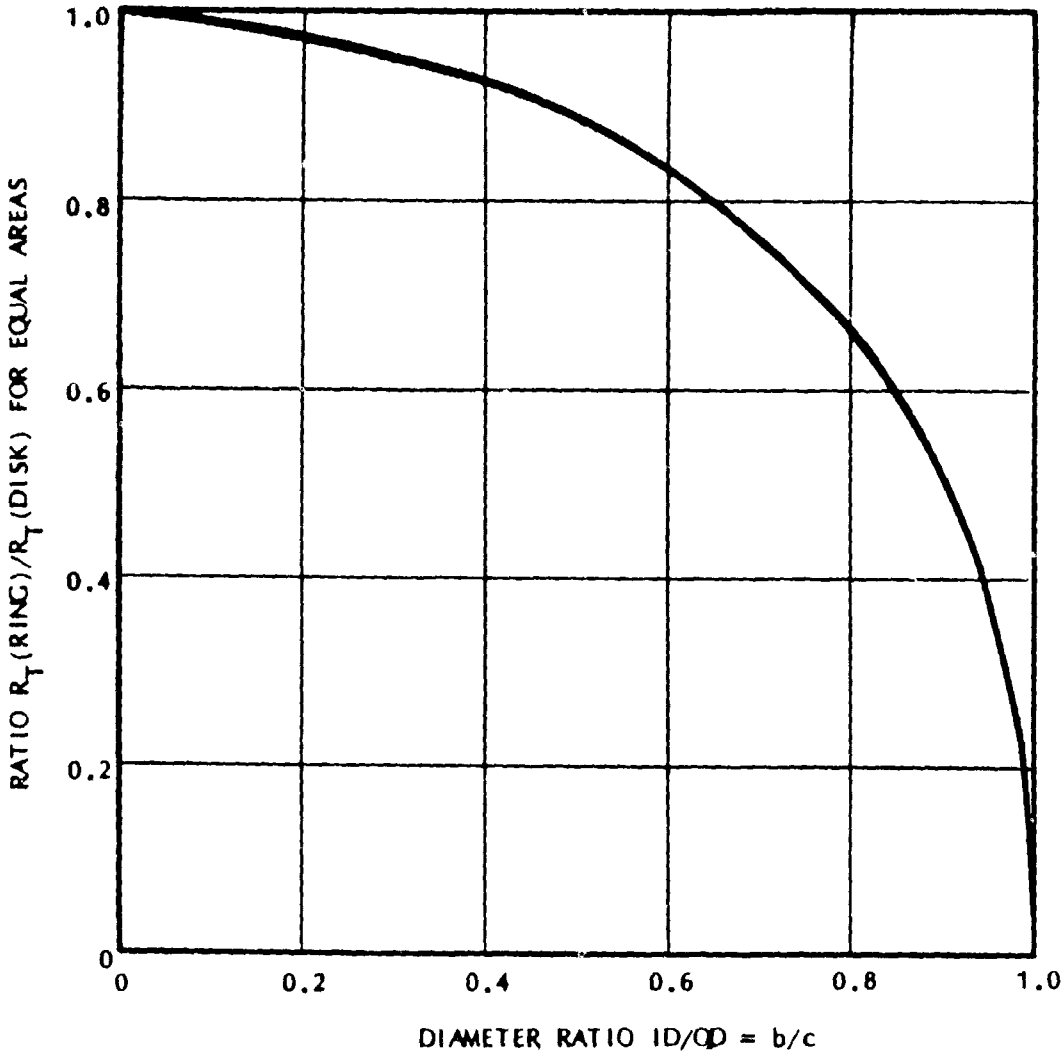


Figure 7. Thermal spreading resistance of ring geometry normalized to that of disk geometry with equal area [from (2)]

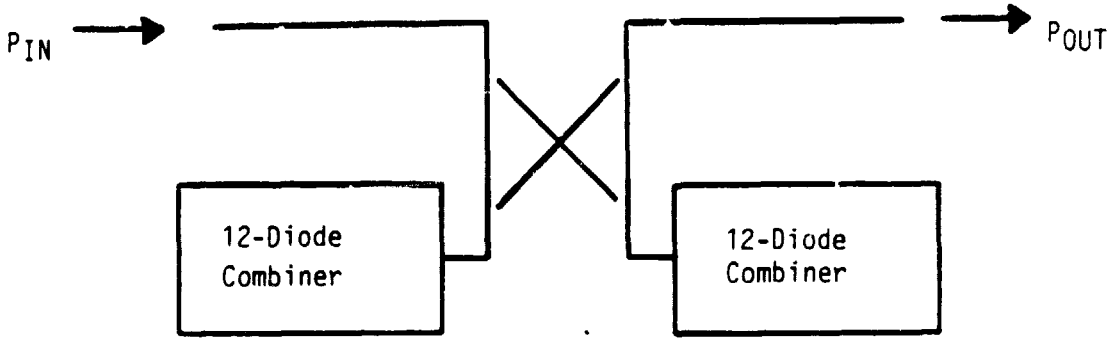


Figure 8. Power combining using 3-dB hybrid coupler

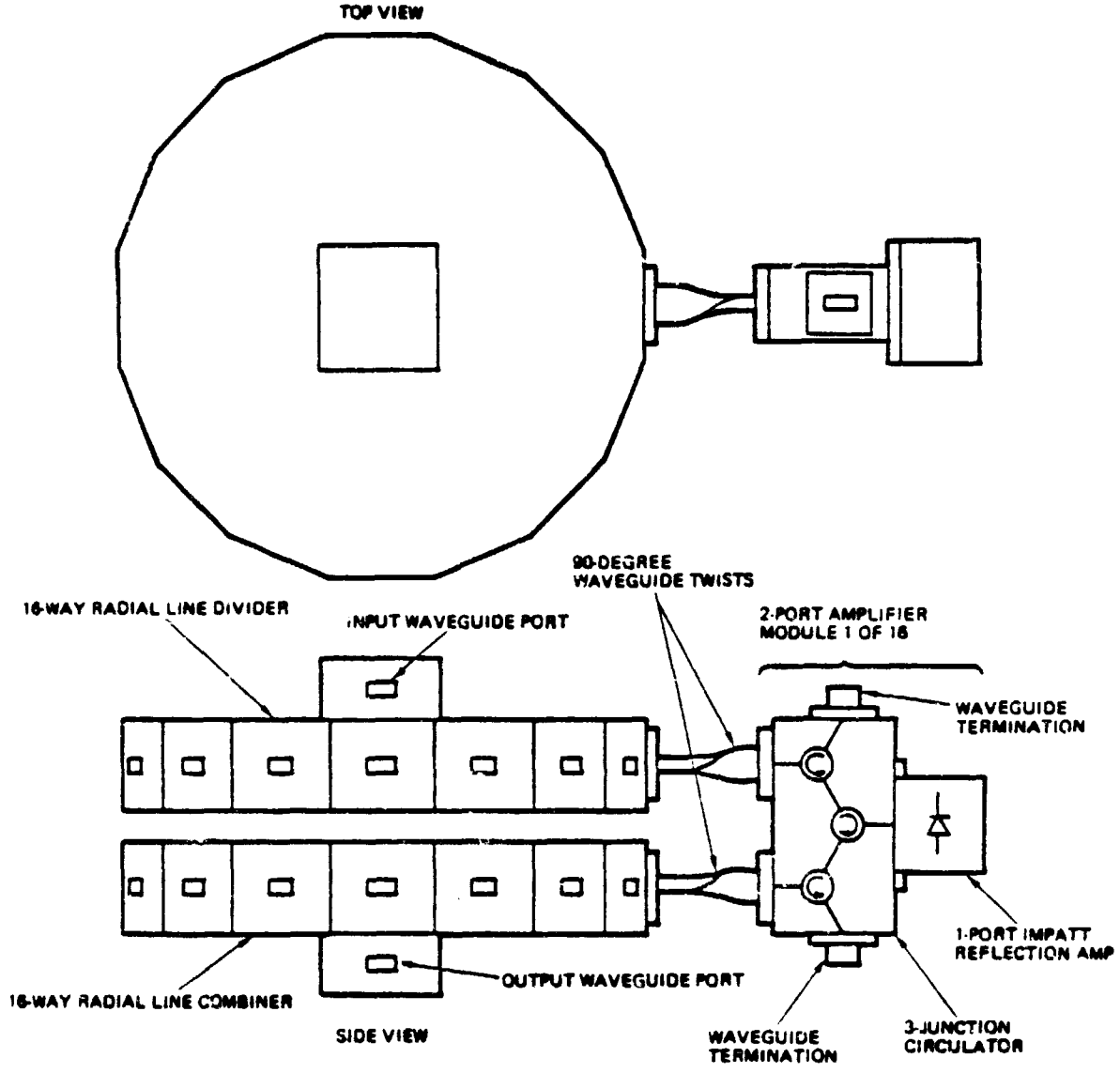


Figure 9. Radial Line Power Combiner Conceptual Design

APPENDIX C

30 GHz SOLID STATE AMPLIFIER

FOR LOW COST LOW DATA RATE GROUND TERMINALS

TASK VIII REPORT

Requirements Document and Development Plan

for a

Low Cost 30 GHz Solid State Amplifier

For a Low Data Rate Ground Terminal

One Space Park, Redondo Beach

California 90278

August 1984

Prepared for

National Aeronautics and Space Administration
Lewis Research Center
21000 Brookpark Road
Cleveland, Ohio 44135

1. REQUIREMENTS DOCUMENT

During the course of this POC model development program, a concurrent study program[1] was also underway at TRW from June 1982 to June 1983 to:

- Develop ground terminal design and cost information to aid system planners in selecting performance parameters for satellite communication systems providing customer premise services
- Develop for specific classes of terminals their manufacturing, installation, and operating costs
- Define the technology developments required and generate a technology plan for low cost LDR ground terminals

Two major constraints were imposed on the overall low cost low data rate ground terminal design, namely:

- Antenna Diameter: 2.8 meter maximum
- High Power Amplifier Output : 20 watts maximum

Based on these constraints, the following general requirements for the solid state HPA were arrived.

- The solid state HPA must be operated in the TDMA burst mode.
- While the power combiner output stage is capable of soft fail characteristics, the single-diode driver amplifier must be replaced by a redundant configuration.

- The metal casing should be mounted on a track permitting rotation of the feed without the necessity of disconnecting critical microwave components or severely complicating the alignment of the feed assembly.

Specific requirements for the TDMA solid state amplifier is given in Table 1.

Table 1. Transmitter/Amplifier Specifications

SATURATED POWER OUTPUT	20 WATTS; SWITCHING TIME 2 μ SEC
BURST RATE	6.875, 27.5, OR 110 MBPS
BANDWIDTH	1.2 X DATA RATE; 2 X DATA RATE FOR MINI STATION
MODULATION	SQPSK; DBPSK FOR MINI STATION
CARRIER SUPPRESSION	> 30 dB
AMPLITUDE IMBALANCE	±0.2 dB
PHASE IMBALANCE	±2.5°
RISE TIME	<600 PSEC; 6 μ SEC FOR MINI STATION
DATA SLEW	<100 PSEC; 1 μ SEC FOR MINI STATION
DATA ASYMMETRY	<100 PSEC: 1 μ SEC FOR MINI STATION
TEMPERATURE	INSTALLATION DEPENDENT
HUMIDITY	100%

2. DEVELOPMENT PLAN

This section presents a development plan for a 30 GHz solid state amplifier engineering model for a low data rate ground terminal to support an experimental program scheduled for a 1987 launch. This engineering model will meet the performance requirements as presented in Table 1. In addition to meeting those requirements, the engineering model will also embody a design

which is amenable to low cost production in quantities of up to about 250. The salient features of this development plan are as follows:

- Based on the electrical design of the POC amplifier, we will examine low cost production approaches to produce the waveguide components, namely, multijunction circulator assembly, single-diode driver assembly, multidiode power combiner assembly. The detailed piece parts for the assemblies are shown in the mechanical drawing under Appendix A.

- A microstrip integrated circuit (MIC) driver amplifier will be developed. This MIC driver will have redundancy and will be extremely low cost due to the MIC design.

- The production costs for 50 and 250 units of such an engineering model, as well as the delta cost to check out one additional unit, will be proposed to address the performance requirements which were not present in the POC development program.

- A detailed schedule and development cost.

The following sections present detailed discussions on each of the above tasks.

2.1 LOW COST PRODUCTION OF WAVEGUIDE COMPONENTS

2.1.1. INTRODUCTION

As the performance requirements are achieved through careful prototype and development model engineering, consideration of volume producibility must be an ongoing activity. Not only is reproducibility of performance essential but also the design must anticipate the introduction of manufacturing techniques compatible with high volume and low cost. The amplifier design

basically consists of the current regulator electronic circuitry and the millimeter wave waveguide components. The current regulators lend themselves to mass production printed circuit board techniques, and the assembly can be very repeatable and low cost. By contrast, the millimeter wave waveguide components require delicate precision machining operations which, in small quantities, can be costly. The major discussion will therefore focus on various waveguide component fabrication techniques which are candidates for quantity production with low cost as the primary objective.

2.1.2 PRINTED CIRCUIT BOARDS

TRW's planned approach to the production design of the regulator printed circuit boards will use surface-mounted chip resistors and capacitors and small outline packaged semiconductors on fiberglass/epoxy printed circuit multilayer boards. The boards will be designed for compatibility with automated assembly and test equipment. The elimination of trimming with variable resistors will be a major goal of the production design. The advantages of minimum size, mature technology, and low labor content in this approach will all contribute to minimum cost.

2.1.3 PRECISION MILLIMETER WAVE WAVEGUIDE COMPONENT FABRICATION

For quantity production, TRW has investigated a number of methods to fabricate precision millimeter wave wavguide components. The tradeoffs between performance, cost, and yield have been considered. Fabrication techniques available for the proposed program and future medium scale production include:

- Numerically-controlled machining
- Electroforming
- Electron-discharge machining
- Centerless grinding
- Screw machining
- Investment casting
- Die casting.

Each method has its own advantages and disadvantages, depending on the quantity and type of machined part.

Numerically-Controlled Machining (NCM)

Numerically-controlled machining involves running a machining center from a preprogrammed tape. TRW is now automatically generating these tapes from the CAD data base. This method is cost effective for small production runs (<100). For large quantity production runs (over 1000) this method is not well suited because it is relatively slow and expensive. NCM is the method by which the circulator housing, the N-way combiner, and the diode modules are machined for prototype and small quantity development model work. It provides excellent surface finish and tolerance control, and is therefore the primary vehicle by which design feasibility is demonstrated.

Electroforming

Electroforming is a technique in which a mandrel is made in the shape of the required inside dimensions of the piece to be fabricated. Copper is then plated around the mandrel until the piece has sufficient wall thickness for the necessary secondary machining. The mandrel is then etched away from the inside and the final outside dimensions are machined, usually on an NCM machine. This process is used where tight tolerances are required on an inside dimension which cannot be machined in any other way. This method is expensive and is a high risk approach from which the yield would be variable. It is also not cost effective since parts which do not meet performance

specifications would have to be scrapped with no opportunity for rework. In certain designs which could use die cast mandrels, if the quantities were high enough to justify a dedicated automated electroforming facility, this method might be viable.

Electron Discharge Machining (EDM)

The EDM machining technique is used to machine a small opening or cavity into a part which is too small for conventional machining. An electrode is made in the shape of the inside cavity and an electrical current issued to burn away the metal from inside the machined piece. This method might be useful for machining the stepped waveguide section in the amplifier assembly. EDM is expensive and time consuming and is therefore not considered a primary candidate at this point.

Point Centerless Grinding

Centerless grinding will be used to machine the diameters of ferrite and ceramic pieces used in the waveguide circulator assemblies. Because the process is highly controllable, very close tolerances can be realized. This method will be used to machine the circulator ferrite junction diameter, because of the requirement for tolerance control.

Screw Machining

Automatic screw machines will be used to produce piece parts which can be machined entirely on a lathe. Setup costs for the screw machine are a significant consideration, but a circulator junction transformer which costs $30 in small quantities will cost less than $0.50 in 10,000 piece quantities when produced on a screw machine.

Investment Casting

Investment casting involves fabricating a metal mold of the desired piece and making a wax copy of the piece. Several individual wax pieces are assembled into a wax tree, and the entire assembly is dipped into a ceramic slurry which coats the wax replica. After hardening, the assembly is baked to remove the wax and to strengthen the ceramic. Metal is then poured into the mold, forming that piece. Depending on the amount of finishing required, machining the finished investment cast part can be less expensive than one made by conventional machining. The cost of the IMPATT amplifier module body, for example, drops from approximately $400 for a single machined piece to approximately $80 for a machined, investment casting piece in quantities of a few hundred.

The tooling for investment casting typically costs $3K with a typical lead time of six weeks. This low tooling cost can be quickly absorbed in a volume run. Unlike die casting, which usually requires draft or tapers on the part to allow the part to be withdrawn, an investment cast piece can be made identical to the prototype design, keeping engineering and development costs down. The major drawback to investment casting is the amount of labor and the many processing steps, making investment casting labor intensive. For waveguide component fabrication, investment casting would be cost effective in most designs only up to a few hundred units.

Die Casting

The major disadvantage of die casting is the initial setup costs. Tooling for die casting costs about $10K to $25K, and lead time is about ten weeks. Also, because the die cast part has to be withdrawn from the tooling once it has cooled, tapers or draft must be usually be designed into the part. Thus, the part can be slightly different from the ideal engineering form. Also, the tool must often be modified after the initial parts are evaluated. This can affect performance beyond acceptable limits. As a result, a dimensional sen-

sitivity analysis and tests should be conducted for each design. This approach holds promise for large quantities at low cost. TRW is now evaluating some die castings of small millimeter wave components without draft with good results.

2.1.4 WAVEGUIDE COMPONENT MATERIALS AND FINISHES

An important consideration is material cost. Primary candidate metals to be considered are copper, brass, zinc, and aluminum. Cost of these raw materials must be equated against other parameters such as weight, electrical conductivity, thermal conductivity, machinability, and castability. The cost differential between materials is a negligible factor whether made from copper, brass, zinc, or aluminum. Gold plating of parts is necessary where corrosion resistance is a factor based on the environmental constraints of a particular unit. In general, aluminum is the typical choice primarily because of its low weight properties and acceptable thermal and electrical properties. The cost advantage of one metal over another is not a significant factor as the material cost represents a very small percentage of total cost, typically less than 5 percent.

2.1.5 ASSEMBLY

A primary cost reduction of millimeter wave components must come from minimizing the skilled labor intensive tasks associated with assembly, alignment, and test of these components. This is by far the major cost element. From TRW's many years of developing and manufacturing a wide variety of millimeter wave IMPATT amplifiers it has become quite evident that, for amplifier types which are not produced in quantity, assembly, and test, labor can be the overwhelming cost element for these amplifiers. Engineering or prototype units which are not produced in quantity generally require highly-skilled personnel to assemble, align, and test. Engineer and/or associate engineer levels are normally required for these operations. This is because mature test procedures, factory test sets, and trained assembly and test

technicians are too expensive for a few units. The per unit production cost of these amplifiers can be significantly reduced by applying labor-saving automation to amplifier fabrication, assembly, alignment, and testing.

Engineering the amplifier circuit design with the objective of eliminating most or all of the tuning elements is a task which must be performed prior to manufacturing in volume. This effort can contribute to greatly reducing the amount of labor required for amplifier production. Each tuning element or circuit adjustment present on the production design increases the amount of labor and the skill level required. For example, the design of the IMPATT amplifier modules is based on a coaxially-coupled reduced-height waveguide circuit. This circuit is shown in Figure 2.1-1 in a prototype configuration which incorporates a number of tuning mechanisms: the waveguide backshort position, coaxial choke position, and coaxial shim thickness and internal diameters.

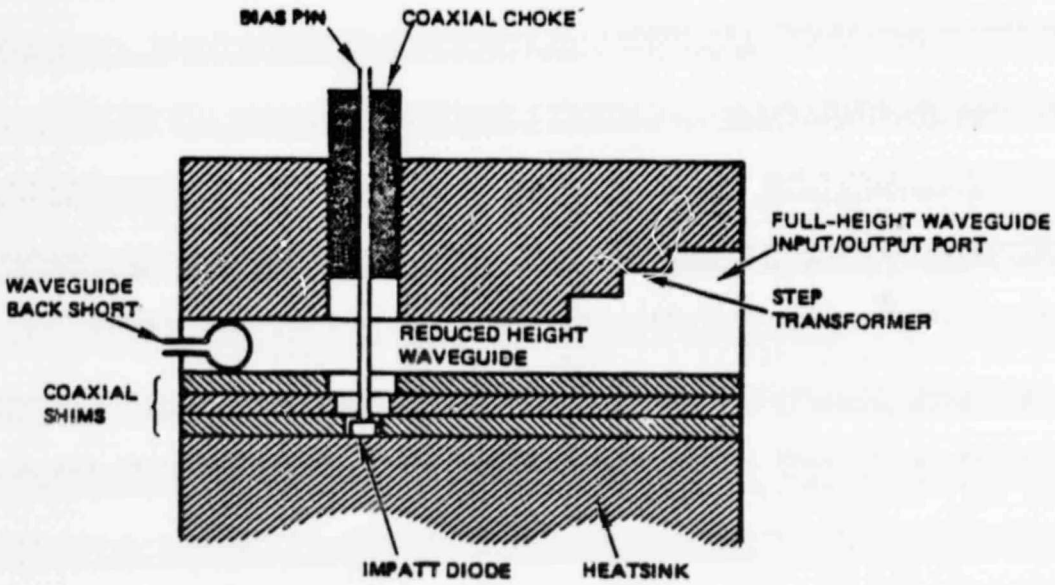


Figure 2.1-1. Schematic of Prototype Configuration Coaxially-Coupled, Reduced-Height Waveguide Circuit for IMPATT Diodes

Figure 2.1-2 illustrates an exploded view of the prototype configuration waveguide circuit. Because of diode lot-to-diode lot RF impedance characteristics, this circuit contains tuning features to compensate for these subtle differences. For a given lot of diodes (around 2000 diodes per lot), the shim dimensions and choke location are fixed. The backshort position is the only variable adjustment element for centering the frequency response.

Although seemingly complicated, these adjustments are actually a simple fundamental approach which provides the flexibility necessary to accommodate diode variations. The alternate approach would be to fix these variables and impose strict requirements on the diodes or perform an external matching function on diodes already embedded within circuits. Imposing a tight diode specification reduces diode yield and thus drives the diode cost upward to unacceptable levels. This is an important consideration since a large number of diodes are used in the amplifier, and the diode cost is the dominant cost factor in the cost of the amplifier. External matching is possible, but it is a very labor intensive activity which is not cost effective. The approach chosen improves diode yield and therefore reduce cost, making the solid state amplifier a viable competitor for TWTAs.

2.1.6 PRODUCTION CONFIGURATIONS

The production configuration of the circuit is fabricated by investment casting a one-piece housing as shown in Figure 2.1-3. This reduces the assembly from 10 to 4 items. The main housing, including the transformer section will be investment cast as a single item. This limits tuning flexibility but with properly screened diodes form a mature production facility expected by 1987, performance will not be sacrificed and a high yield of amplifiers will be obtained.

The proposed amplifier circuit design is manufacturable at low cost and by minimizing the need for variable tuning within the circuit itself, labor content is minimized.

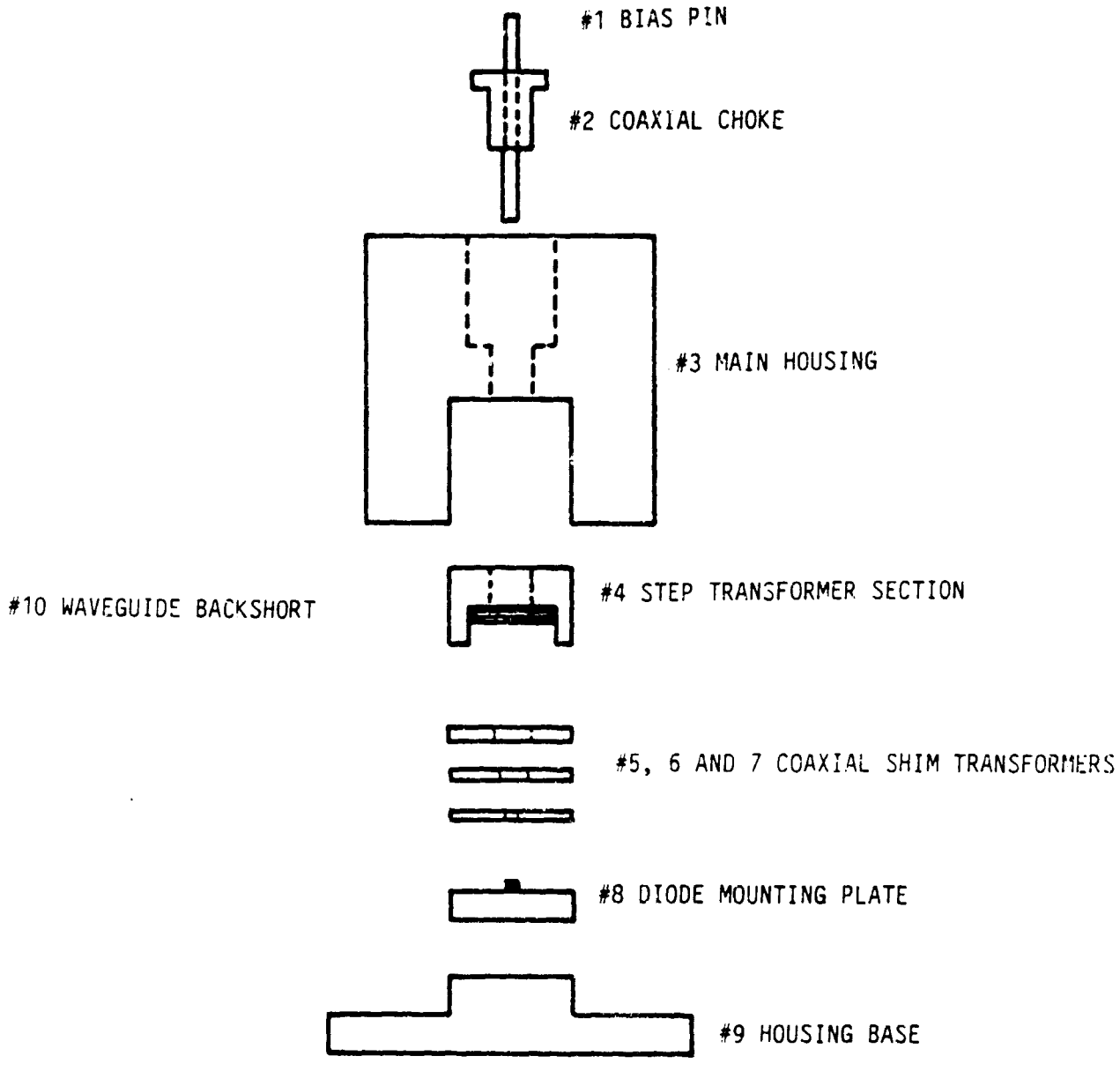


Figure 2.1-2. Exploded View of Waveguide Amplifier Circuit Prototype Configuration

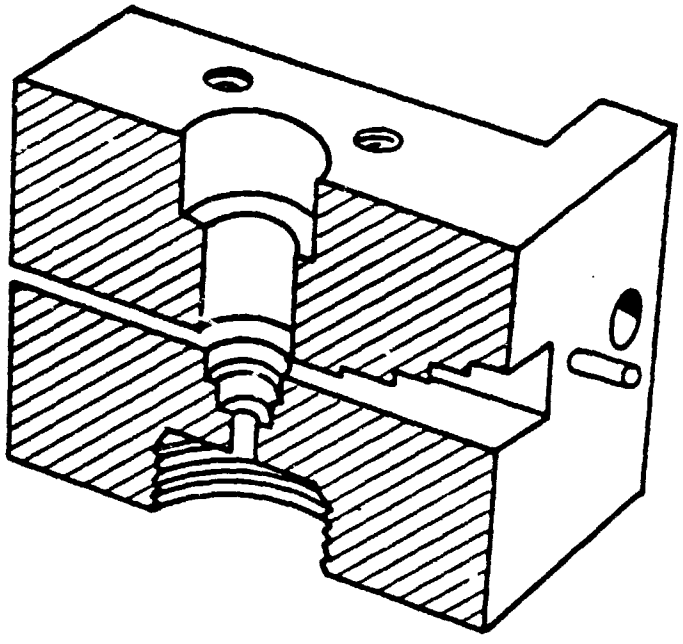


Figure 2.1-3 Production Waveguide Amplifier Housing Cutaway

The design for TRW's circulator has already been engineered to eliminate all tuning adjustments. This effort has been highly successful. The outstanding wideband and low loss performance of TRW's microwave and millimeter wave band circulators is well recognized throughout the industry. This performance is achieved in a design for which there are absolutely no tuning adjustments. TRW's circulator is an excellent example of the result of a very successful effort to take a microwave component which previously required a great deal of labor for alignment, and to subsequently eliminate the entire alignment and tuning operation. This assembly will be die cast and finish machined in two halves as shown in Figure 2.1-4.

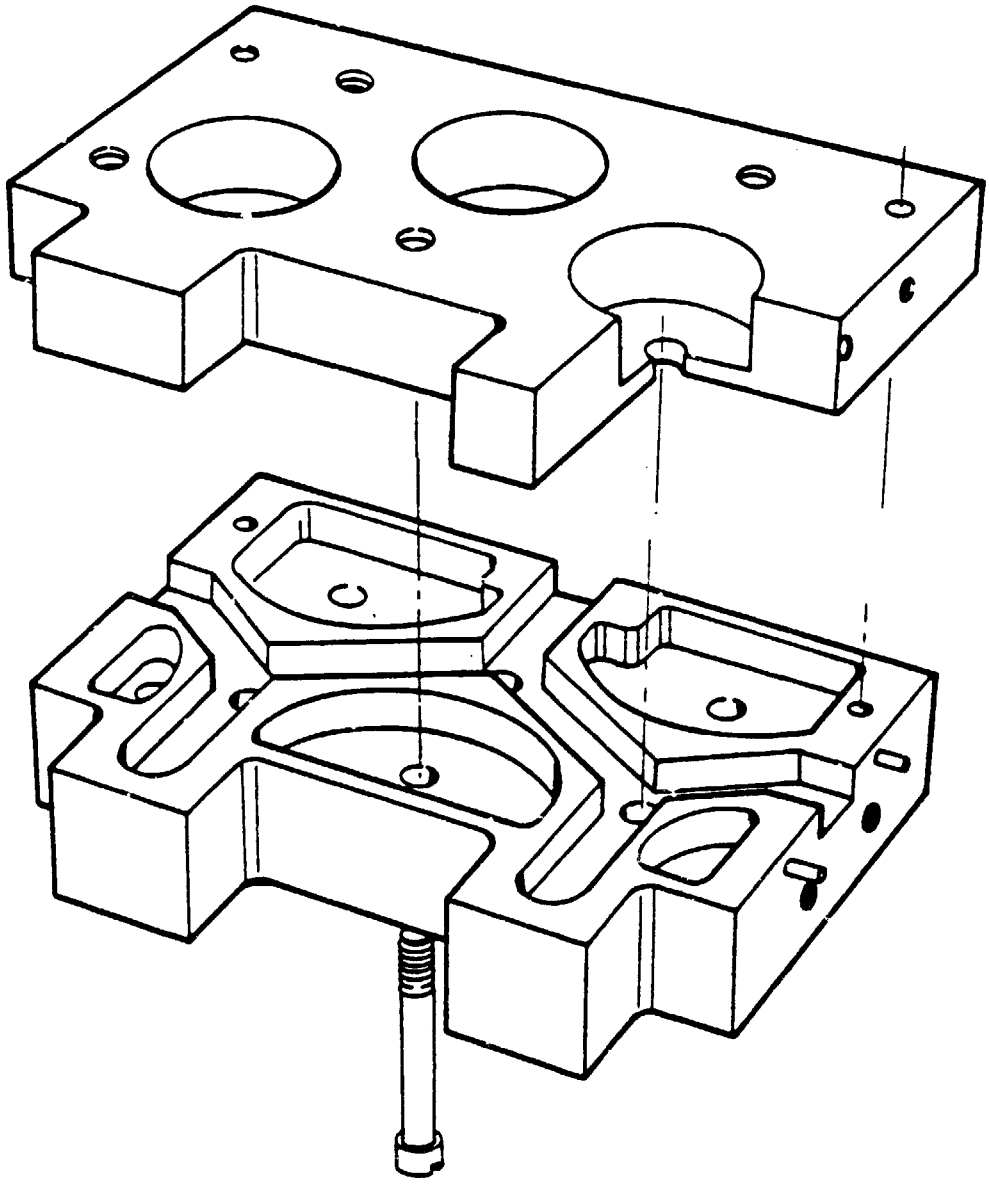


Figure 2.1-4 Production Circulator Housing Design
Example Shows Three-Junction Circulator

2.2 MIC DRIVER DEVELOPMENT

With the recent advances of millimeter-wave integrated circuits at TRW, novel circuits can be developed using microstrip transmission media to achieve medium output power and low cost for many system applications. The use of the integrated circuit is especially attractive for the driver stage of the 30 GHz engineering model development. To achieve these objectives, TRW proposes to develop a low cost 30 GHz microstrip IMPATT amplifier with redundancy, capable of 2.5 W CW output power and over 44 dB gain.

2.2.1 PROPOSED APPROACH

Using TRW's microstrip circulators and microstrip single-diode IMPATT oscillators/amplifiers as the building blocks, the proposed amplifier will be built as shown in Figure 2.2-1. At the amplifier input, the signal is split into two branches by a 3-dB divider. Each divided signal is amplifioed by two identical amplification chains consisting of three amplifier stages. A single-pole double-throw ferrite switch is placed at the output for amplification chain selection. This redundant arrangement is to increase the overall system reliability.

The amplifier design is based upon the injection locking amplification mode, in which the amplifiers act like oscillators. All the diodes are TRW silicon IMPATTs rated at 2.5 W CW in a waveguide circuit. The two driver stages are single-diode oscillators to deliver 150 mW at its output with 35 dB gain. Wideband, low loss (0.6 dB/path typical) TRW microstrip circulators will be used to achieve isolation between the inputand output port of the IMPATT amplifier. The driver is followed by a final stage amplifier to reach the goal of 34.4 dBm power with 12.6 dB gain. The proper design of the final stage is dictated by careful consideration of the output power capability of the IMPATT diodes, the tradeoff between gain and bandwidth, the power output of the driver and DC power consumption. It will be a 4-diode combiner using

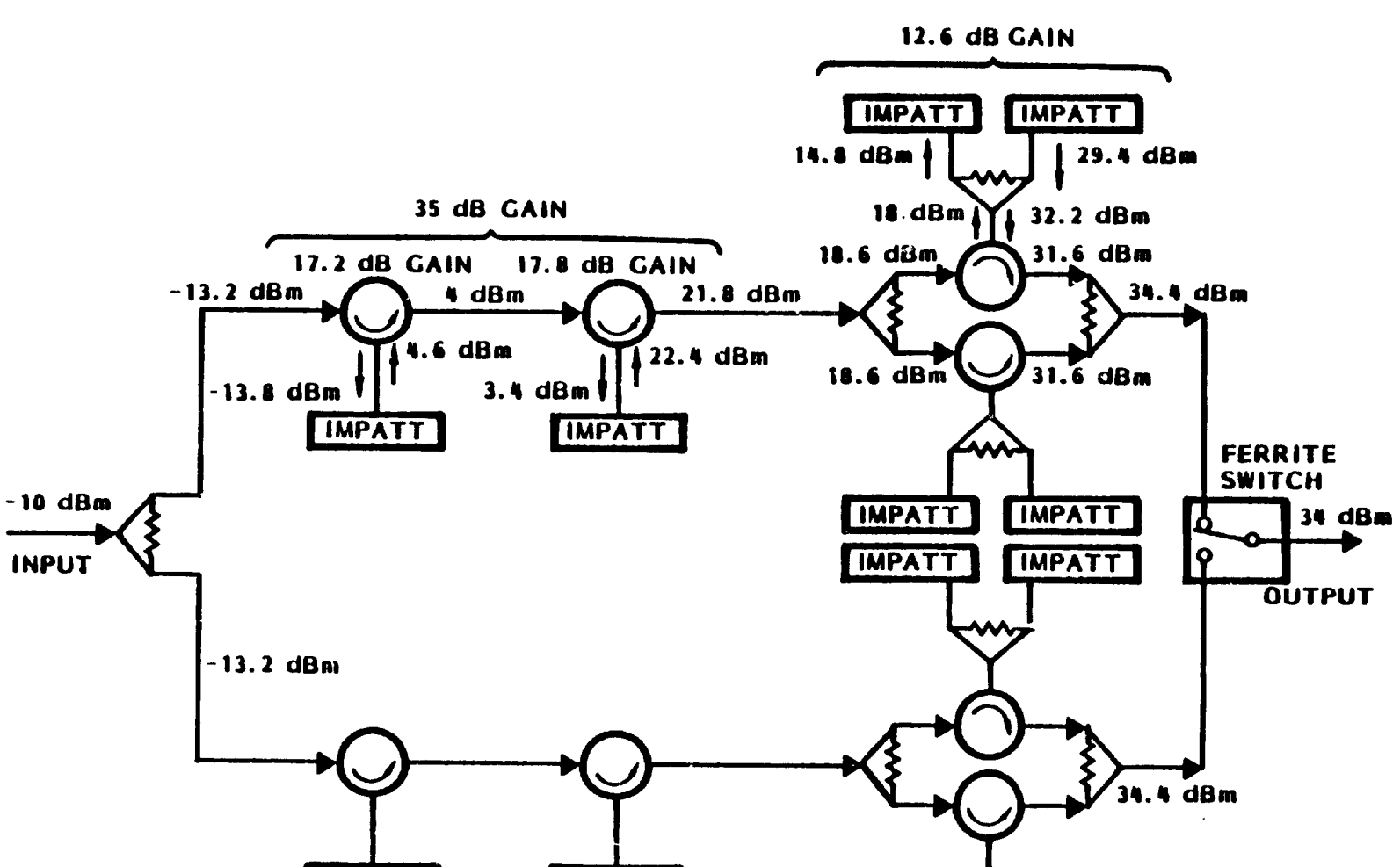


Figure 2.2-1. Amplifier functional block diagram

3-dB dividers as the input/output diplexing mechanism. To obtain 2.75 W (34.4 dBm) power output, the overall gain of the final stage should be close to 12.6 dB with an added power of 2.6 W. The 2.5-W IMPATT diode is capable of generating 1 w of output power in the microstrip circuit. Our system design only requires an output power of 870 mW (29.4 dBm) from each diode to produce an added power of 2.5 W in the 4-=diode combiner. The power combining efficiency is approximately equal to 80%. Assuming 0.4 dB insertion loss at the ferrite switch, an output power of 2.5 W (34 dBm) will be achieved from the amplifier.

The thermal design problems of the overall amplifier are expected to be minimal. The heat generating components, mostly originated from the IMPATT diodes of the amplifiers, are to be well separated from one another to allow efficient heat spreading. It is planned to cool the amplifier by heat conduction. In the event that heat conduction proves to be inadequate or difficult to implement effectively, thermal radiation can be used as a supplementary method for cooling.

The proposed specifications are as follows:

Power Output:	2.5 W, CW
Overall Gain:	44 dB, 3 stages
Bandwidth:	500 MHz
Size:	Less than 6 in^3 excluding power supplies
Center Frequency:	30 GHz

The details of the major building components are discussed below.

2.2.3 MICROSTRIP CIRCULATOR

TRW has developed a microstrip circulator operating at Q-band frequencies near 45 GHz. This circulator boasts of 20-dB isolation over 3-GHz bandwidth and less than 1 dB insertion loss.

The TRW microstrip circulator has many unique features. It uses C-48 material for the ferritre disk and Duroid 5880 for the substgrate. As many millimeter-wave integrated circuits utilized Duroid 5880 as a substrate, a "ring" matching structure is avoided, thereby reducing interface losses and simplifying the design. The design uses tangential coupling to achieve good impedance matching.

As shown in Figure 2.2-2 the microstrip circulator boasts of 20 dB isolation over 3 GHz bandwidth with an average insertion loss of less than 1 dB. Return loss is better than shown as there is considerable contribution from the microstrip-to-waveguide transitions. A view of the test unit is contained in Figure 2.2-3. This circulator design can be readily scaled down the frequency to 30 GHz for our amplifier design. The estimated insertion loss at this frequency is about 0.6 dB.

2.2-4. Microstrip IMPATT Oscillator/Amplifier

Recognizing the need for low-cost millimeter-wave solid-state sources for system applications, TRW has recently engaged in the development of compact MIC IMPATT oscillators/amplifiers. One such effort has led to a design of a 44-GHz microstrip IMPATT oscillator/amplifier. This oscillator consists of a circuit pattern on Duroid substrate as shown in Figure 2.2-4. A matching circuit was designed for the low diode impedance to match the high line impedance. Figure 2.2-5 shows the output power and frequency of the microstrip oscillator measured as a function of bias current. Output powr of 200 mW has been achieved at 44 GHz. An injection-locked experiment was also conducted and Figure A6 shows the locking bandwidth as a function of locking gain. Over 1.5% locking bandwidth was achieved for a locking gain of 19 dB. With this background, 30 GHz microstrip single-diode IMPATT modules can be easily developed.

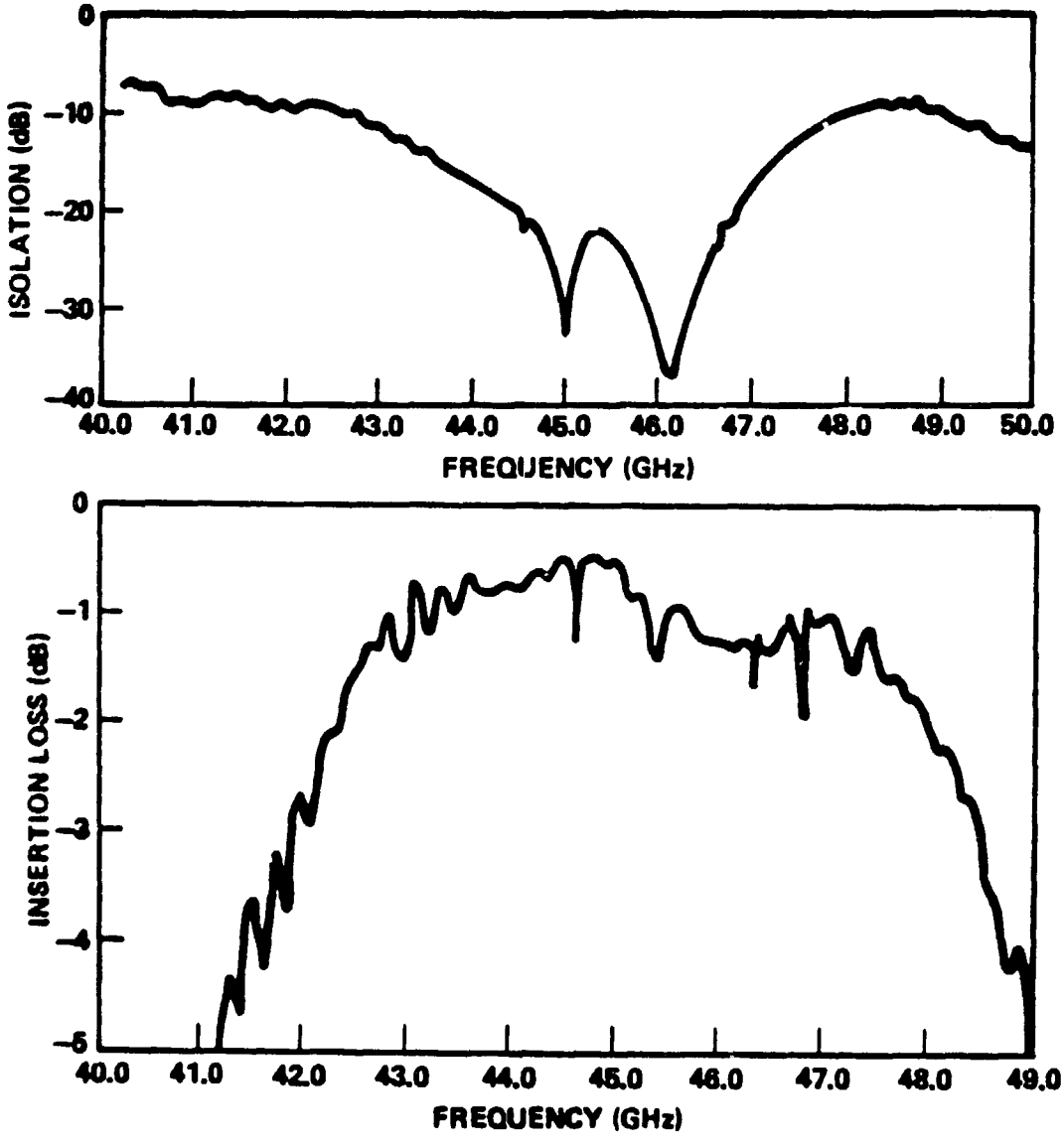


Figure 2.2-2 MIC Circulator Insertion Loss and Isolation

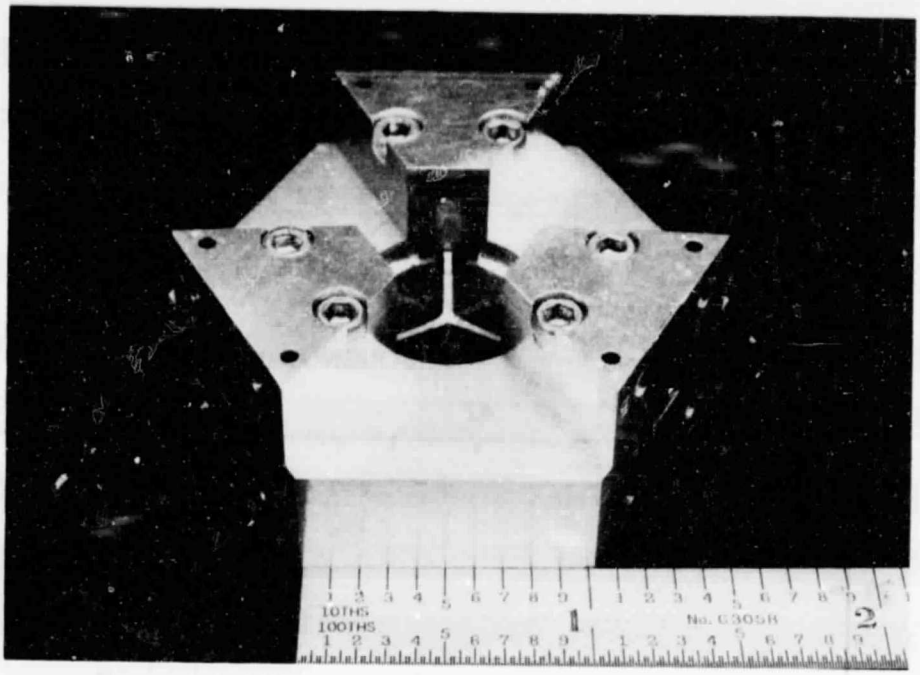


Figure 2.2-3 MIC Circulator Test Fixture

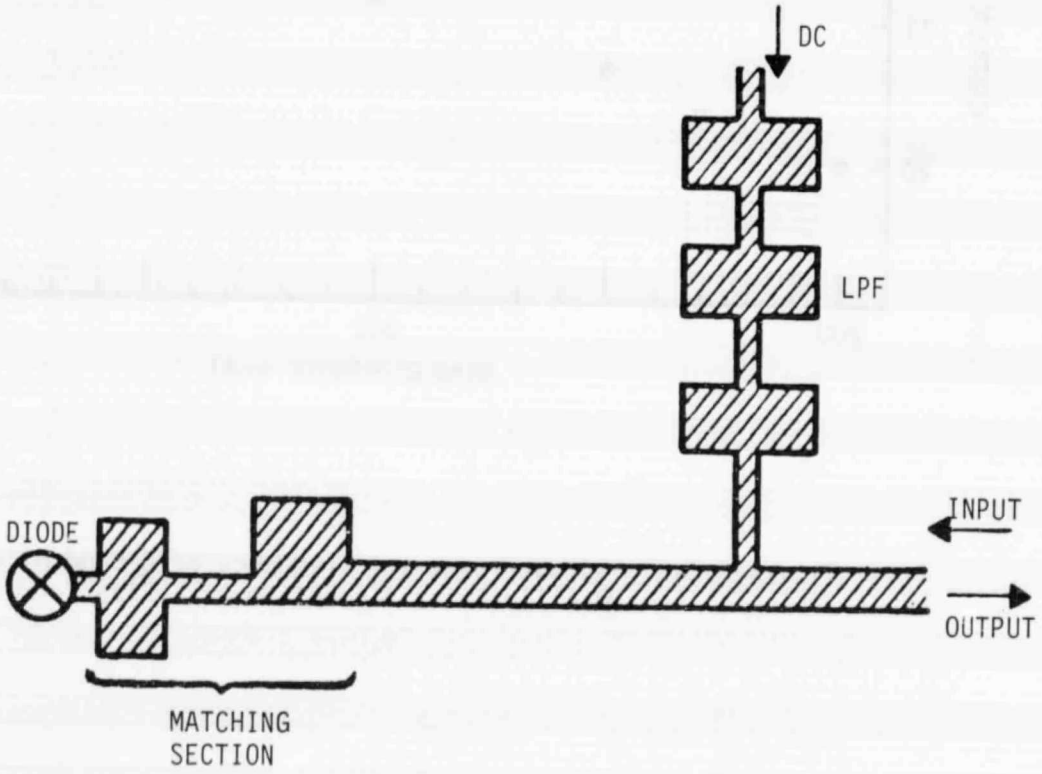


Figure 2.2-4 Circuit Layout of Microstrip Injention Locked Amplifier

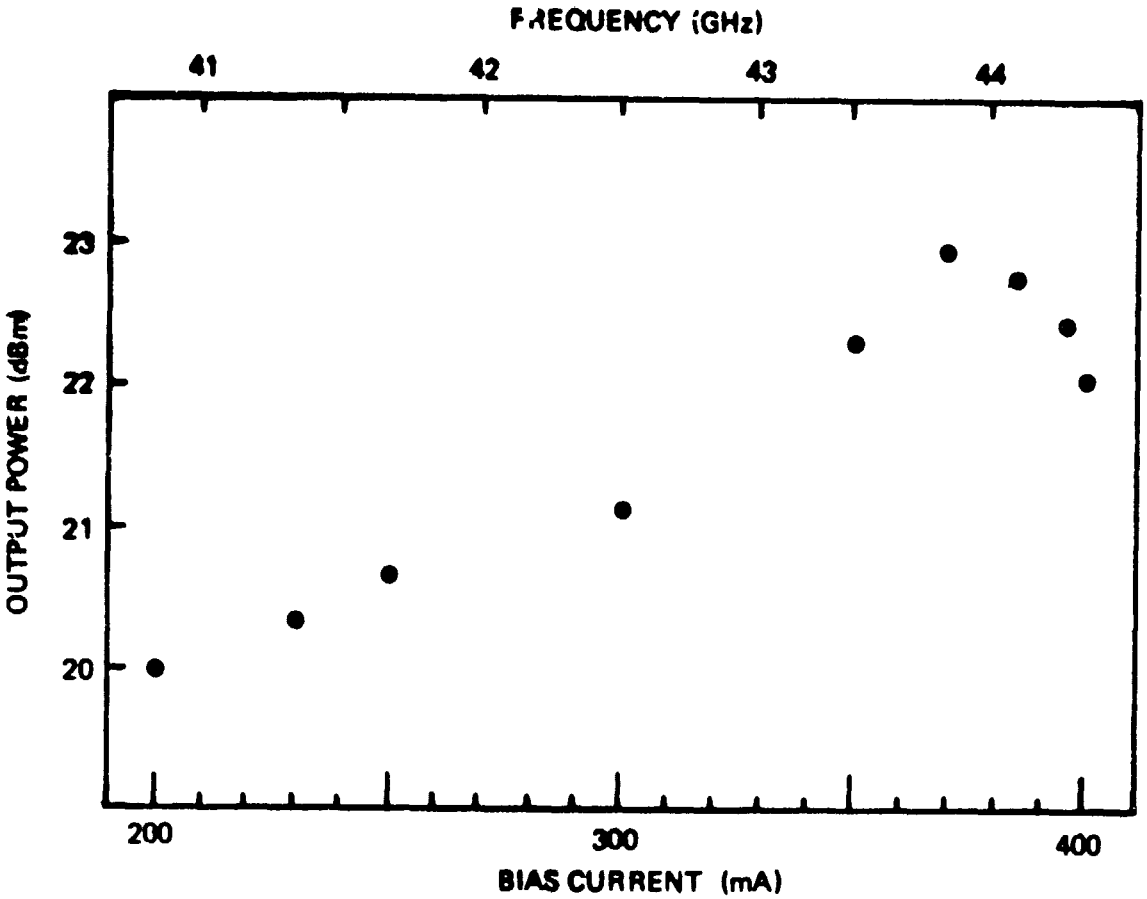


Figure 2.2-5 Output Power and Frequency of Q-Band Microstrip Oscillator as a Function of a Bias Current

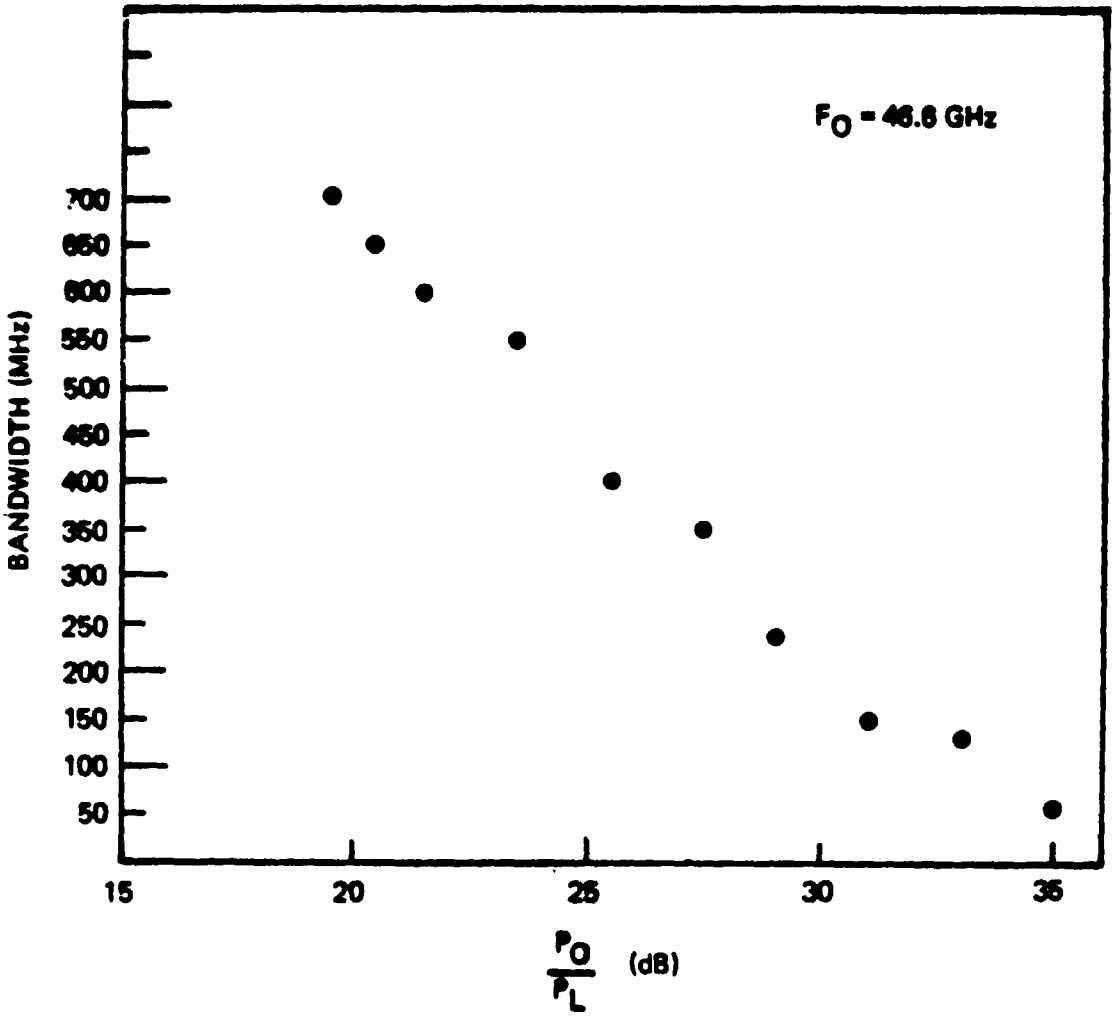


Figure 2.2-6 Injection-Locking Bandwidth as a Function of Power Gain

2.2.5 TRW Waveguide Ferrite Switch

TRW has developed a low loss ferrite switch operating at 27.5 to 30 GHz. This switch can be optimized and used for this program. The TRW switch performance is summarized below.

- Operating Frequency Range: 27.5-30 GHz
- Insertion Loss: < 0.4 dB
- Isolation: > 35 dB
- VSWR: 1.2:1
- Switching Speed: 1 μs
- Simple structural construction, high producibility.
- Impervious to shock and vibration.
- Latching type with low switching power requirement in the microJoule range.

2.3 BIT-ERROR-RATE MEASUREMENT

As part of the 30/20 GHz satellite communication system, the 30 GHz amplifier will ultimately be used in digital networks supporting an overall traffic load of approximately 3 Gbps. Low data rate (LDR) ground terminals in this system, of which the amplifier forms an integral part, will likely have average composite data rates of 64 kbps, 1.5 Mbps, and 32 Mbps. At the present time, the performance goals for the solid state amplifier are specified in terms of standard parameters such as power output, bandwidth, amplitude flatness, phase linearity and noise figure. However, in order to fully and accurately characterize the performance of an RF channel carrying digitally modulated signals, some technique beyond measuring the above parameters is useful. The most common and powerful method forevaluating the entire communications system as well as any individual component of the RF channel is through bit error rate measurement.

A BER test system was developed and employed at TRW to perform BER

measurements on a 3ϭ GHz, 5-W injection-locked CW IMPOATT amplifier. The system essentially compares the digital input signal with the digital output signal and effectively notes the difference in terms of a bit count. Any discrepancies are noted as a bit error. The system can evaluate signals either in the bi-phase shift keying (BPSK) up to a data rate of 100 Mbps or quadriphase shift keying (QPSK) up to 200 Mbps. We believe that, with minor modifications to accommodate a lower carrier frequency, this system is readily applicable for evaluation of the 30 GHz amplifier.

2.3.1 SYSTEM DESCRIPTION

A BER test system was developed and employed at TRW to perform BER measurements on a 38 GHz, 5 W injection locked IMPATT amplifier. The modulation technique employed was quadrature phase shift keying (QPSK) at a data rate of 100 million bits per second (100MBPS) per channel. QPSK has four possible phase states and therefore it can carry the information provided by two independent binary data streams or channels. The two channels are designated I (for in-phase) and Q (for quadrature) and adding the data rates for the two channels gives a composite data rate of 200 MBPS. This also gives the minimum RF channel bandwidth required to pas the first complete lobe of the modulated spectrum, in this case 200 MHz. For the 30 GHz solid state amplifier, although the design goal for the bandwidth is only 50 MHz, it is estimated that the actual bandwidth can be as high as 250 MHz or more. Therefore, the present system should be readily applicable.

Figure 2.3-1 is a functional block diagram of the complete BER test setup. In the following sections, the various building blocks of the system will be discussed in detail.

2.3.1.1 Data Generator

The I and Q data streams are generated by four functional blocks, namely, (a) a 200 MHz reference oscillator, (b) a ÷ 2 frequency divider, (c) a Tau-

Tron MN-301 pseudorandom noise (PRN) generator for the I data stream and another one for the Q data stream, and (d) a data reclocking circuit. The 200 MHz reference oscillator is a stable crystal oscillator that when divided by two and filtered serves as the 100 MHz system clock establishing the per channel data rate of 100 MBPS. The clock signal drives the two Tau-Tron

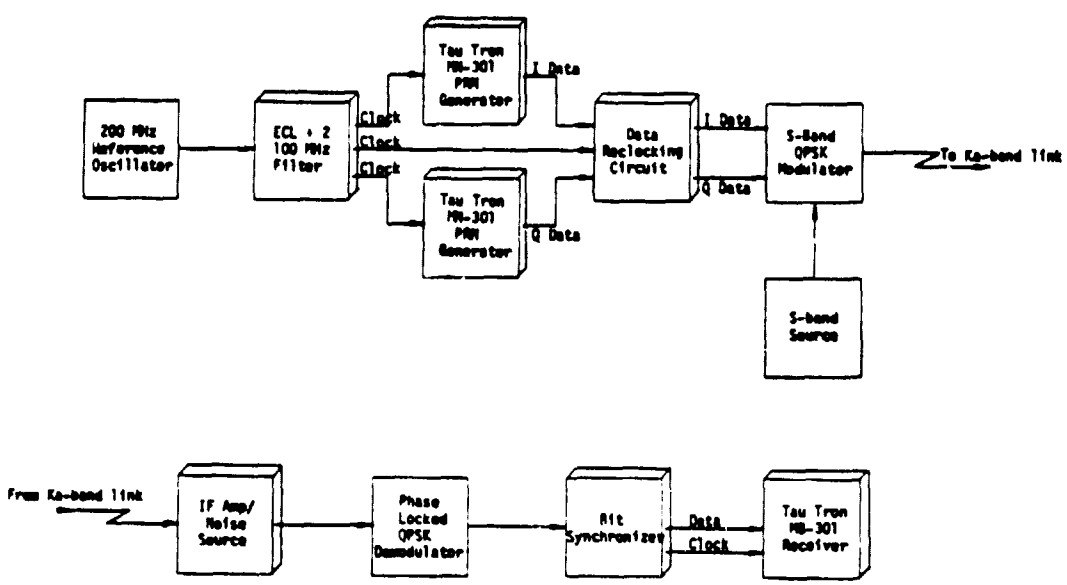


Figure 2.3-1 Functional Block Diagram of Complete BER Test Setup

MN-301 PRN generators which generate the PRN data streams. It is possible to set the two generators to different patterns ensuring minimal correlation between channels. To understand the function of the PRN generators, let us not that the entire premise of a BER measurement is that of comparing the output of the system to that of its input on a bit-by-bit basis and noticing whether, or how many, bits were changed (from a "1" to a "0" or vice versa). Certain bit sequences are better than others for this application because of the possibility of pattern sensitivities in various pieces of the hardware, particularly the modulator, the demodulator, or the bit synchronizer. To avoid undesirable consequences of possible pattern sensitivities, a pseudo-random noise bit pattern generator is employed as an input data source. In

addition to the favorable statistical properties of a PRN code, it is possible to program the receiver with the same code as that used in the transmitter and

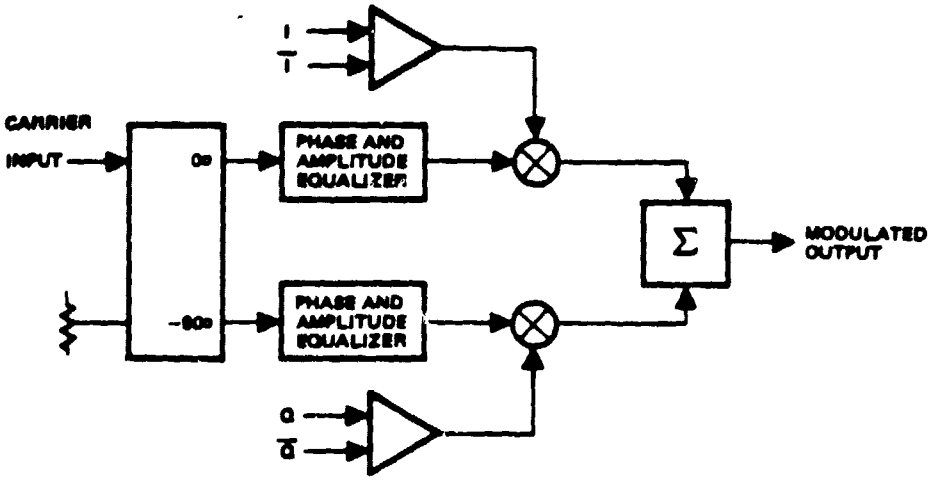


Figure 2.3-2. QPSK Modulator

therefore eliminate the need of a second communication channel to serve as a reference for the measurement. The data reclocking circuit removes any asymmetry from the data bits and also provides a one-half bit delay to the Q channel data., This skew between the channels ensures the only one of the bi-phase switches in the QPSK modulator will be required to switch at a time. This provides slightly improved performance.

2.3.1.2 QPSK Modulator

The QPSK modulator is a standard parallel configuration as shown in Figure 2.3-2. The 2.144 GHYz carrier is split into two equal amplitude quadrature channels by a 90 degree hybrid. Each of the two channels is then biphase (0 degrees to 180 degrees) modulated by the input data. The output of

the two modulators is in-phase power combined to generate the quadriphase modulated output signal. All of the modulator components are standard commercial items with the exception of the data amplifiers. The data amplifiers are a TRW design which utilizes microwave transistors in order to obtain switching speeds compatible with high data rate transmission. The biphase modulators are standard commercial double-balanced mixers. Phase and amplitude adjustments are accomplished y means of compensation circuits, which have adjustable phase and amplitude characteristics. The complete QPSK modulator is assembled in a machined aluminum housing using SMA connectors and flex cable for RF component interconnects.

2.3.1.3 Ka-band Link

In order to evaluate the BER performance of the 30 GHz amplifier, the QPSK modulator output must be allowed to pass through a Ka-band transceiving link, with the 30 GHz amplifier being the unit under test (UUT) in the link. Figure 2.3-3 is a block diagram of the Ka-band upconverter/downconverter unit. A Hewlett-Packard synthesizer is used as a stable local oscilator source for both the up and down conversion processes. This ensures coherency between input and output signals without undue complexity. The 14 GHz amplifier are commercially available items. The times two multipliers and mixers are commercially available from Spacek Labs. The output filter, which selects the upper sideband upconverted signal is either commercially available or can be designed and fabricated at TRW.

2.3.1.4 IF Amp/Noise Source

In order to simulate the noise that the signal would experience in an actual transmission through the atmosphere, a broadband noise generator is used to create an effective E_b / N_o at the demodulator input by reactively summing the broadband noise withthe modulated carrier prior to demodulation. The noise source shown in Figure 2.3-4 generates noise by amplifying thermal noise by 64 dB and bandlimiting it to 600 MHz. The E_b / N_o is determined from

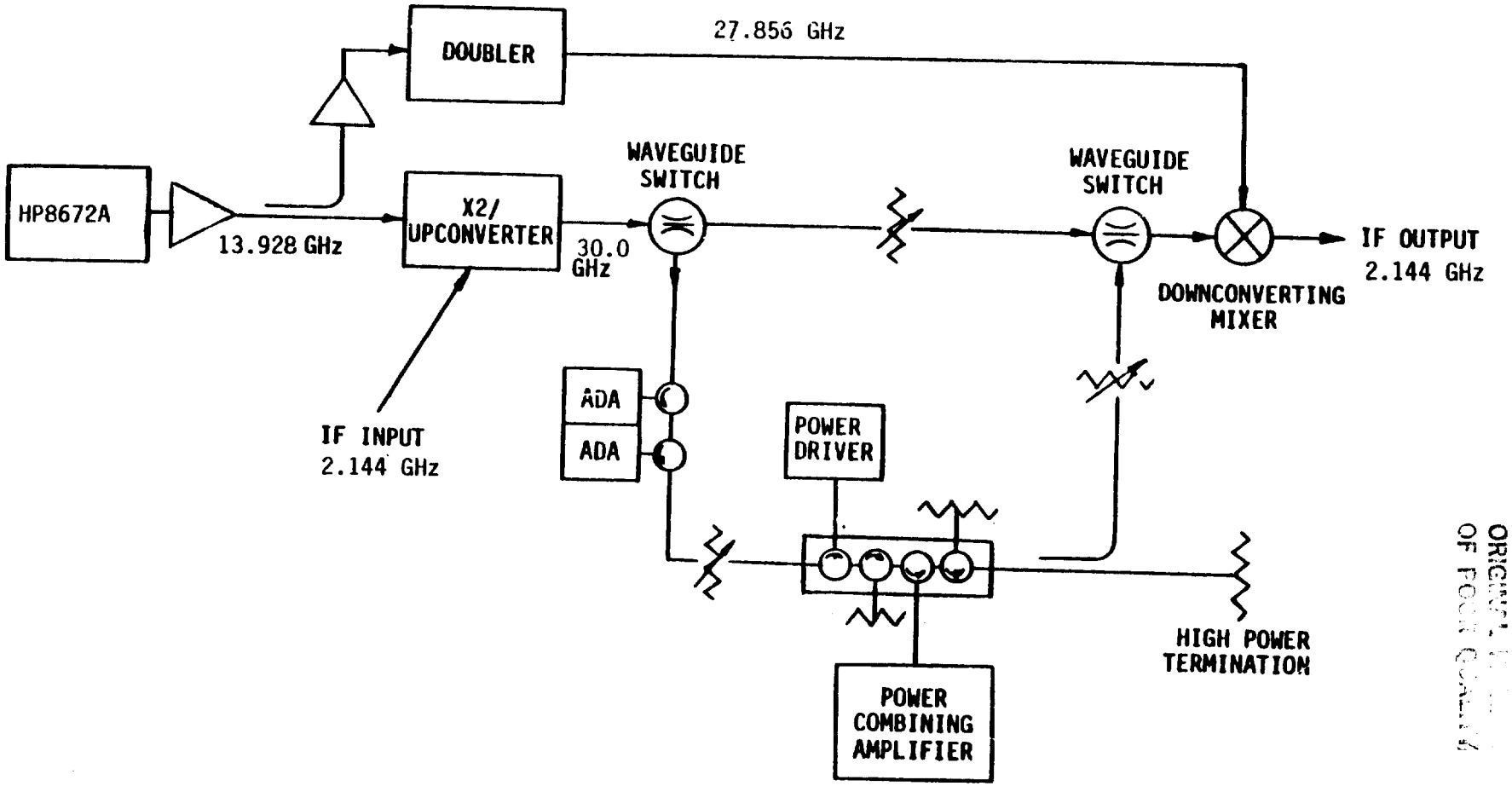


Figure 2.3-3 Ka-Band Link for 30 GHz BER Test System

the received modulated signal power, noise power spectral density, and detection filter bandwidth.

2.3.1.5 Phase-locked QPSK Demodulator

The demodulator extracts the data from the received signal by multiplying the incoming modulated signal by the recovered carrier. The demodulator is a standard data demodulator using a carrir recovery loop with decision feedback (also known as a modulation-wipeoff carrir recovery loop). The demodulator, shown in Figure 2.3-5 consists of three basic circuits: a quadrature demodulator, a QPSK remodulator, and a phase-locked carrier recovery loop. The modulated input signal is first split into I and Q components by an in-phase power divider. The two signals are then phase-detected by a pair of double balanced mixers. The LO input to the mixers is the recovered carrier which has been power divided by a 90 degree hybrid. If the recovered carrier is coherent with the modulated carrier, then the IF outputs from the mixers represent the phase differences between the LO and the modulated carrier and therefore the baseband data. The baseband data is next amplified and then power divided three ways to provide outputs to the bit synchronizer, the remodulator section, and front panel test points.

The demodulated baseband signals are then used to remodulate the locally generated carrier. If the recovered carrier is coherent with the modulated carrier, then the original QPSK modulated signal and the remodulasted QPSK signal will be identical in phase. The remodulated QPSK signal is fed to the phase detector and is the reference with which a sample of the incoming signal is compared. A VCXO error signal is generated within the phase detector which corresponds to the phase difference between the modulated and remodulated signals. A delay line is necessary to delay the modulated signal for a period of time equal to the delay of the demodulation/remodulation process. In addition to the necessary loop filters and amplifiers, the phase-locked loop contains sweep circuitry for automatic signal aquisition.

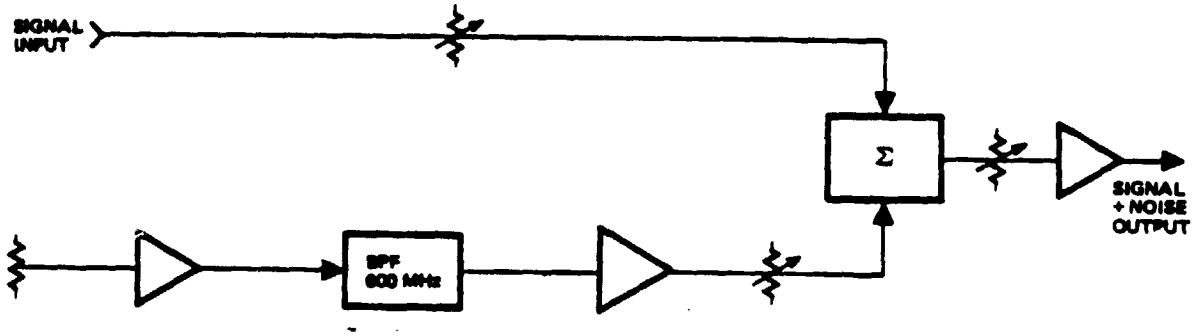


Figure 2.3-4 IF Noise Source

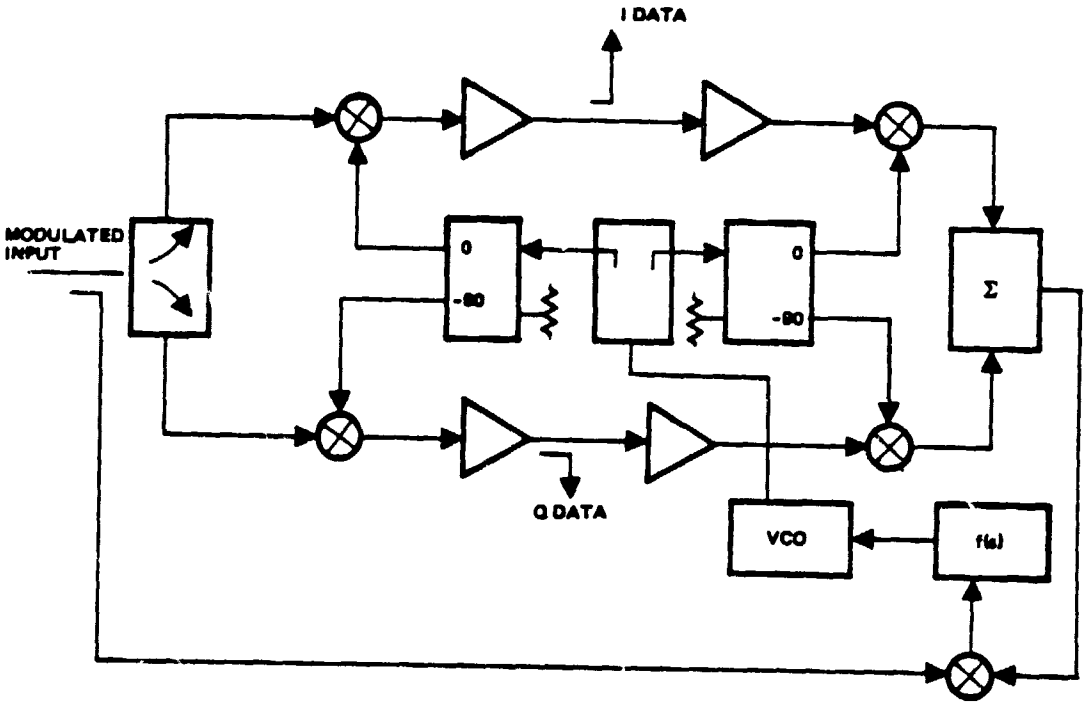


Figure 2.3-5 I-Q Quadriphase Demodulator

2.3.1.6 Bit Synchronizer

The bit synchronizer performs two functions: clock recovery and bit decision, i.e., a best estimate of the digital data on a bit-by-bit basis. The bit synchronizer accepts the output data from the demodulator, which is a composite of signal and noise, determines the data state, and outputs this decision. A block diagram of the bit synchronzer is shown in Figure 2.3-6.

2.3.1.7 Tau-Tron Receiver

The Tau-Tron MB-301 receiver accepts the clock and data signals from the bit synchronizer and compares the incoming data stream to the internally generated PRN sequence. The receiver allows the internally generated code to "slip past" the input signal until pattern correlation is detected. At this point the receiver begins counting bit-by-bit discrepancies and displays the result as an error count.

2.3.2 SAMPLE MEASUREMENT

To illustrate the type of measurement data one can obtain from the BER test system, we devote this section to the discussion of the data package obtained for the 38 GHz 5 W solid state amplifier.

The Ka-band link is shown in Figure 2.3-7. As a preparatory step before the actual BER test, the Ka-band link was adjusted for the flattest obtainable amplitude and phase response from IF input to IF output. Figure 2.3-8 shows the measured response at 2.1 GHz. Next, proper operation and alignment of each element in the BER test system was verified with the use of a spectrum analyzer and a high speed oscilloscope. Figure 2.3-9 shows the spectrum occupancy of the 100 Mbps pseudo random noise (PRN) output of the Tau-Tron PRN generator. The output spectrum of the QPSK modulator is shown in Figure 2.3-10, while Figure 2.3-11 illustrates carrier suppression by changing the frequency resolution of the spectrum analyzer. The output spectrum of the phase locked QPSK demodulator is shown in Figure 2.3-12. Cursory comparison with Figure 2.3-9 shows little degradation to the signal within the most important first two lobes of the spectrum.

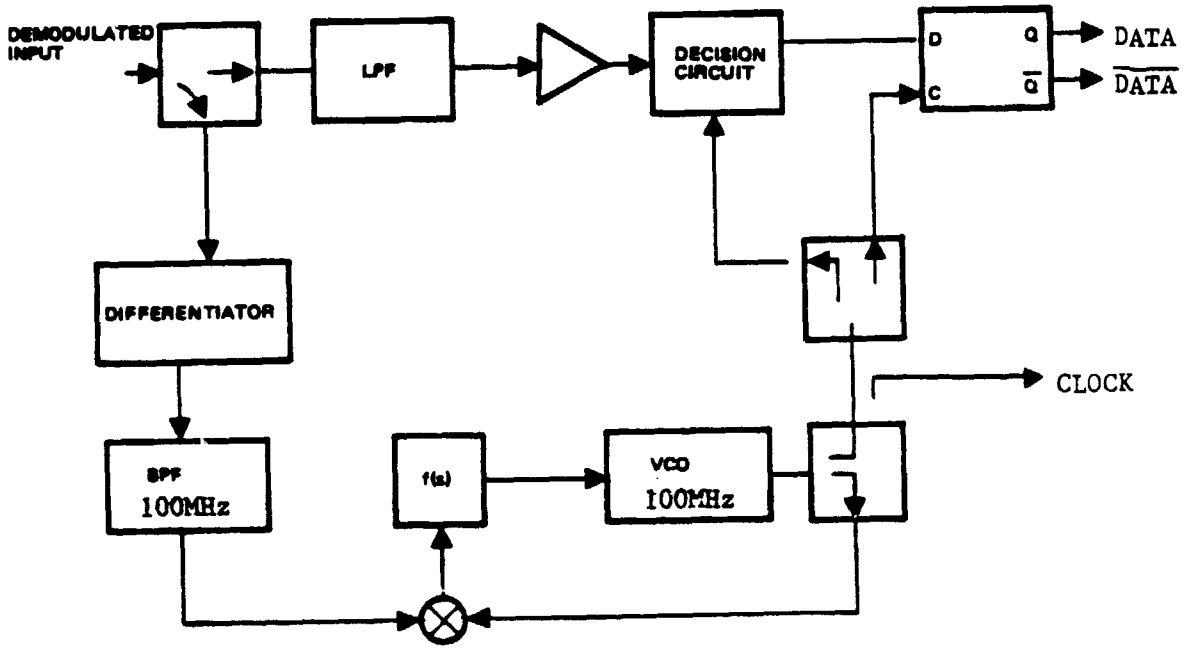


Figure 2.3-6 Bit Synchronizer

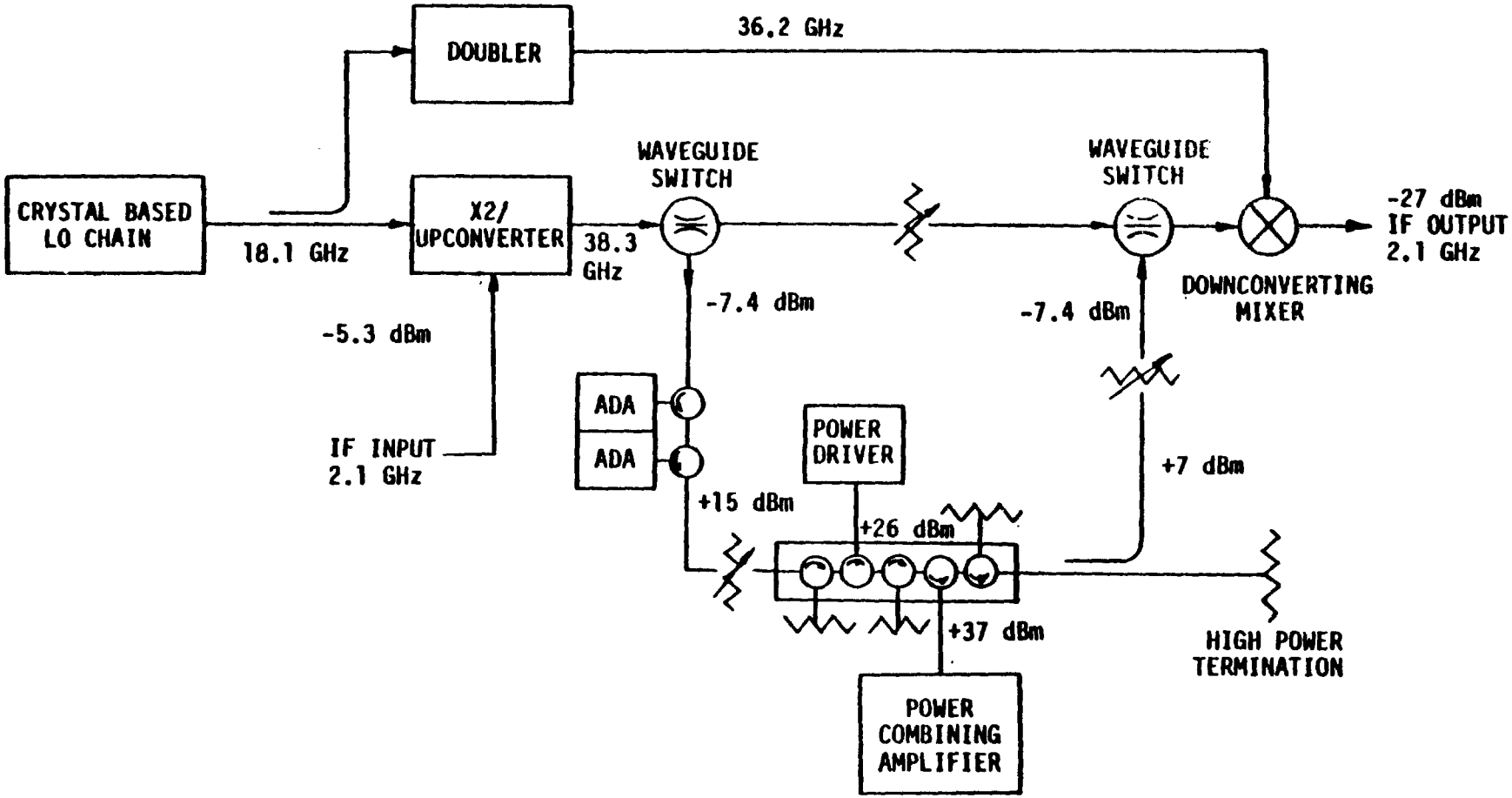


Figure 2.3-7 Ka-Band Link and Power Combining Amplifier

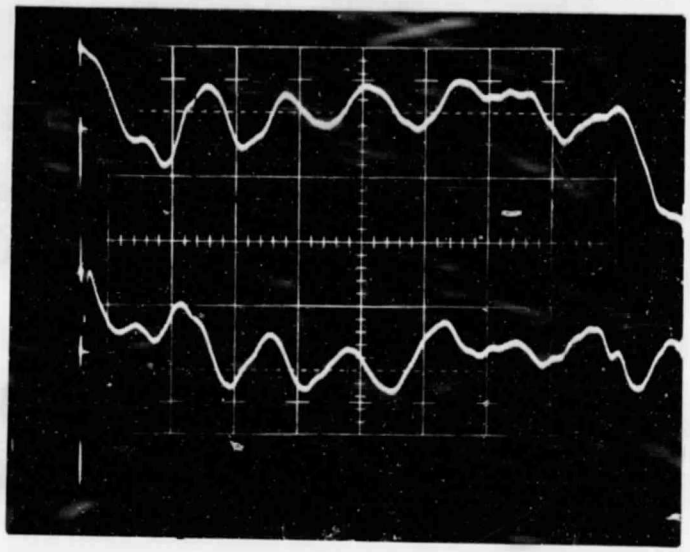


Figure 2.3-8 Amplitude (1 dB/div) at Top and Phase (5°/div) Response for Ka-Band Terminal

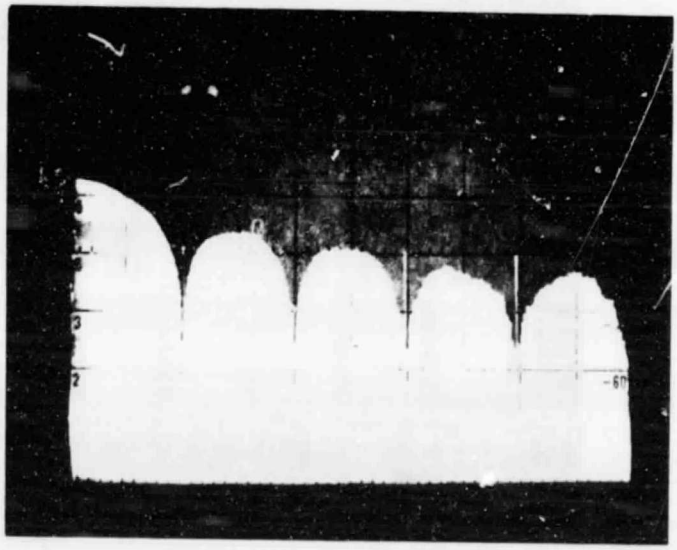


Figure 2.3-9 Output Spectrum of Tau-Tron PRN Generator (50 MHz/div)

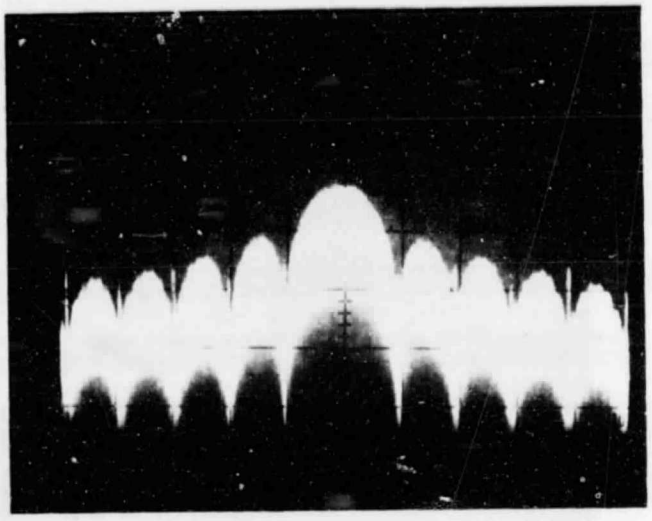


Figure 2.3-10 Output Spectrum of QPSK Modulator Centered at 2.144 GHz (100 MHz/div)

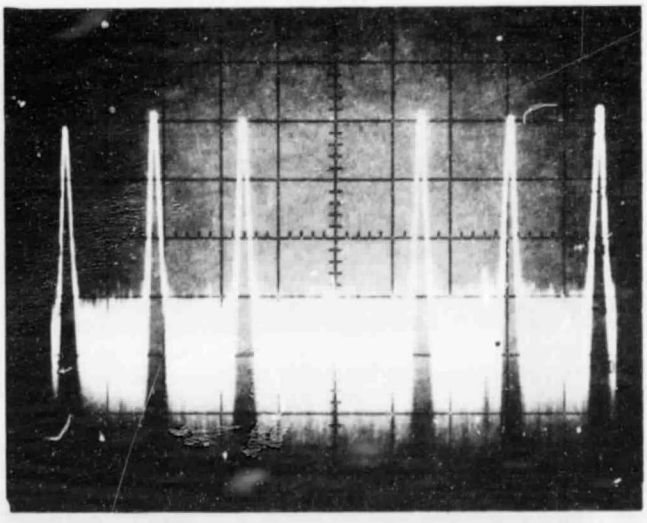


Figure 2.3-11 Output of QPSK Modulator Showing Data Sidebands and Carrier Suppression of 50 dB, Unmodulated Carrier at 0 dB Level (500 KHz/div)

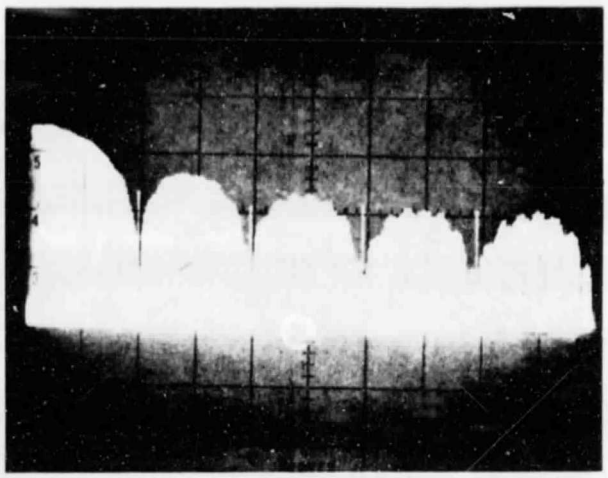


Figure 2.3-12 Output Spectrum of QPSK Demodulator (50 MHz/div)

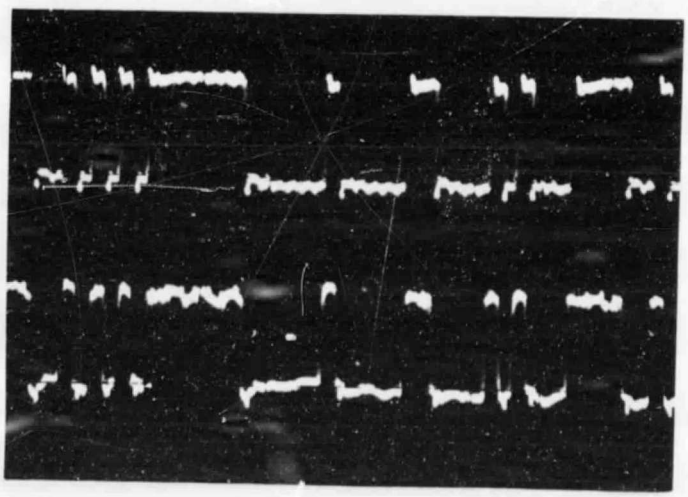


Figure 2.3-13 Tau-Tron Generator Output (Top) 1 V/div; QPSK Demodulator Output (Bottom) 0.1 V/div.

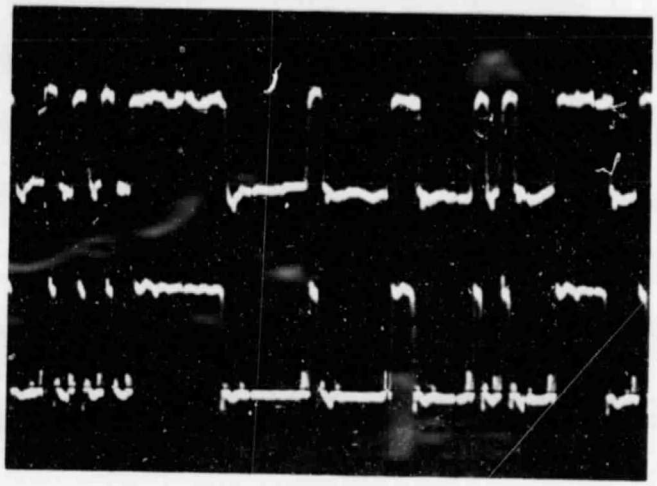


Figure 2.3-14 QPSK Demodulator Output (Top) 0.1 V/div; BIT Synchronizer Output (Bottom) 1 V/div

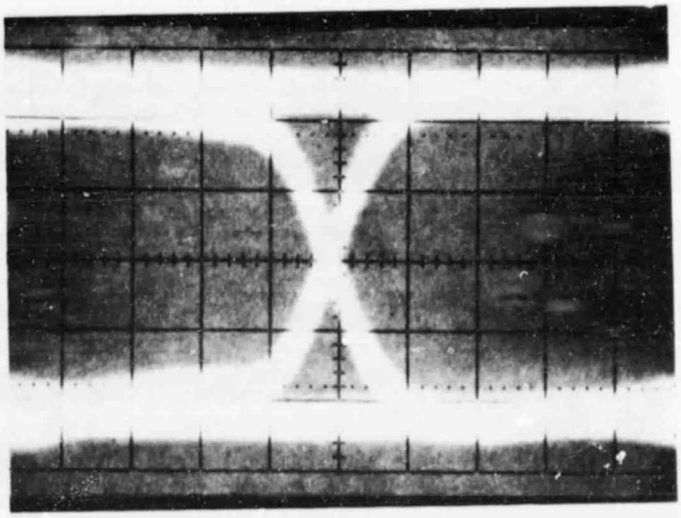


Figure 2.3-15 Eye Pattern at QPSK Demodulator Output Showing ± 200 ps Assymetry; Horizontal Scale: 1 nsec/div.

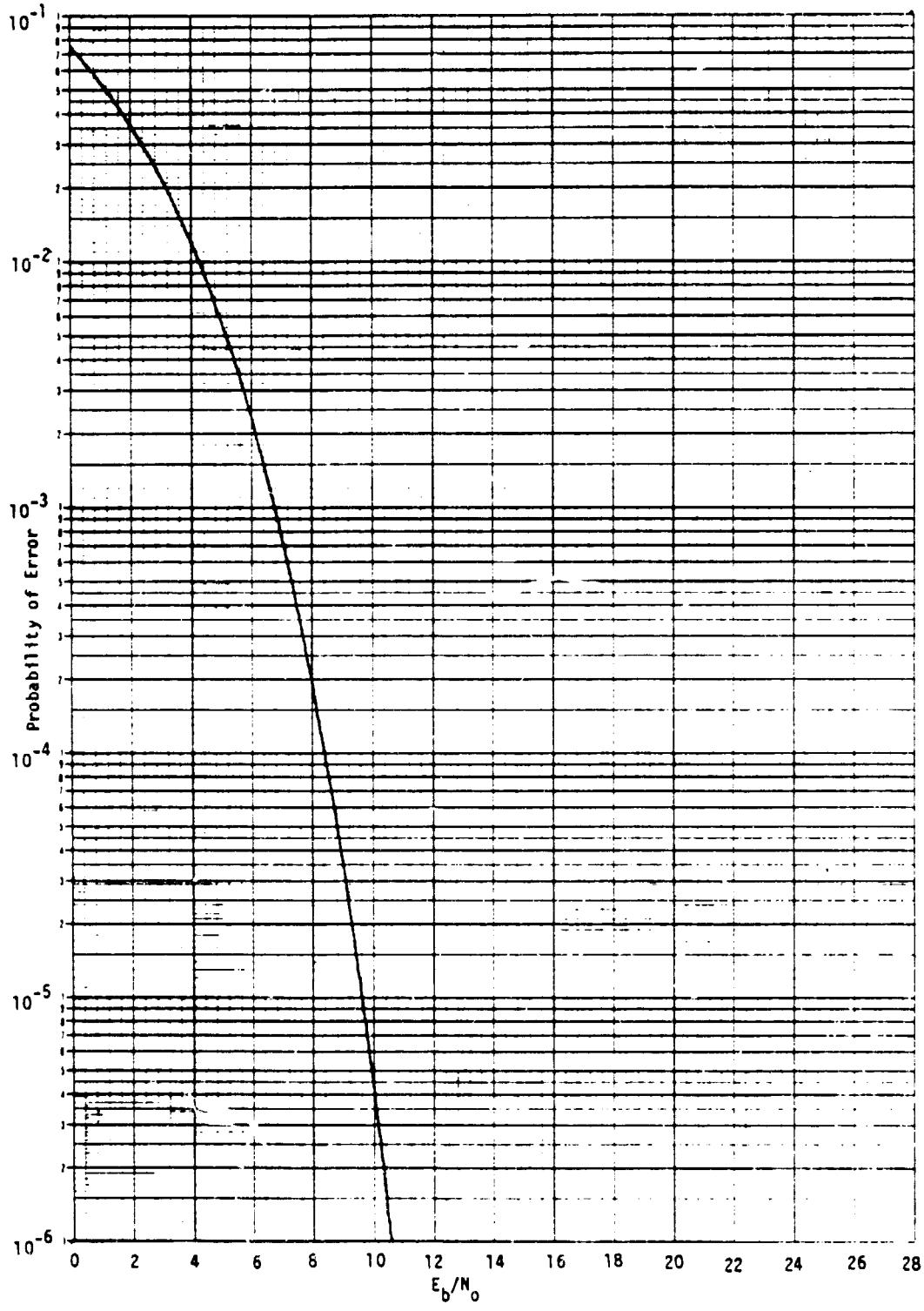


Figure 2.3-16 Ideal Probability of Error vs. E_b/N_o

Time domain photographs of the PRN bit stream at the output of the Tau-Tron generator, the QPSK demodulator and of the bit synchronizer are shown in Figure 2.3-13 and 2.3-14. The eye pattern shown in Figure 2.3-15 is useful in determining the asymmetry of the demodulated signal. The pattern is the sum of all of the bits in the 127-bit PRN sequence. The width of the pattern at zero crossing represents the total asymmetry throughout the entire sequence and includes the effects of any pattern sensitivity. Total asymmetry is ±200 ps for the QPSK signal shown.

The purpose of a BER test is to measure probability of error (P_E) as a function of energy per bit to noise ratio (E_b/N_0), the digital system equivalent of signal to noise ratio. Figure 2.3-16 is a plot of P vs. E /N for a perfect QPSK system. This is the reference against which other systems are measured.

The energy per bit to noise ratio can be defined as the carrier power to noise power plus a correction factor. The correction factor is necessary to take into account the difference between the noise bandwidth (B_N) and the signal or data bandwidth (DBW).

In equation form, these quantities are:

$$\frac{E_b}{N_o} = \frac{C}{N_T} + CF \qquad CF = 10 \log_{10} \frac{B_N}{DBW}$$

The setup shown in Figure 2.3-17 was used to measure the noise spectral density of the IF amp/noise source. From this, the equivalent noise bandwidth (B_N) may be determined.

A plot of the noise spectral density for the noise source is presented in Figure 2.3-18. Also indicated is the equivalent noise bandwidth. From this,

the equivalent noise bandwidth B_N may be determined. From Figure 2.3-18 B_N = 515 MHz. For 100 MBPS/channel QPSK, the data bandwidth DBW = 200 MHz. Therefore, the correction factor is:

$$CF = 10 \log_{10} \frac{B_N}{DBW} = 10 \log_{10} \frac{515}{200} = 4.11 \text{ dB}$$

$$CF = 4.11 \text{ dB}$$

Probability of error vs E_b/N_o is plotted in Figure 2.3-19 for the cases of Ka-band terminal, Ka-band terminal plus power driver (injection locked), and Ka-band terminal plus power driver plus power combining amplifier (injection locked). Table 2.3-1 summarizes the degradation in BER for each element in the system. The degrdation attributable to the power combining amplifier was 0.2 dB or less over the range of 10^{-2} to 10^{-6} BER. The power levels at each stage of the amplifier are identified in Figure 2.3-20. Knowing these power (hence gain) levels and that the Q_{ext} for the combiner is 30, the locking bandwidth for the combiner was calculated to be approximately 400 MHz. This is roughly two times the composite data bandwidth of 200 MHz. Figure 2.3-21 is a pictorial ilustration of the progress of a sinusoidal signal as it passes through the BER test system.

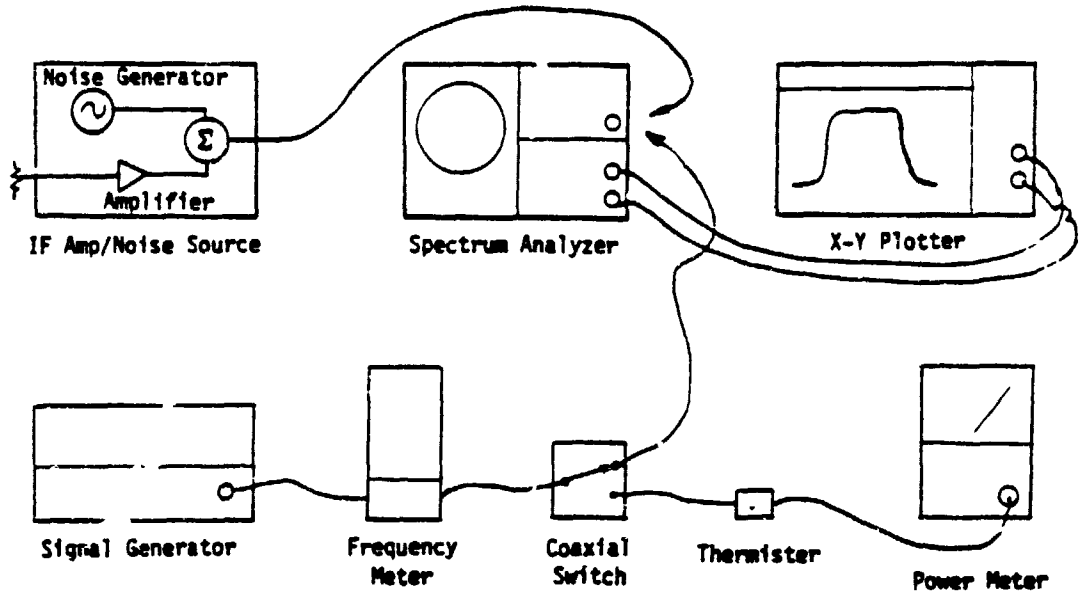


Figure 2.3-17 Setup to Measure Noise Spectrum Density of IF Amplifier

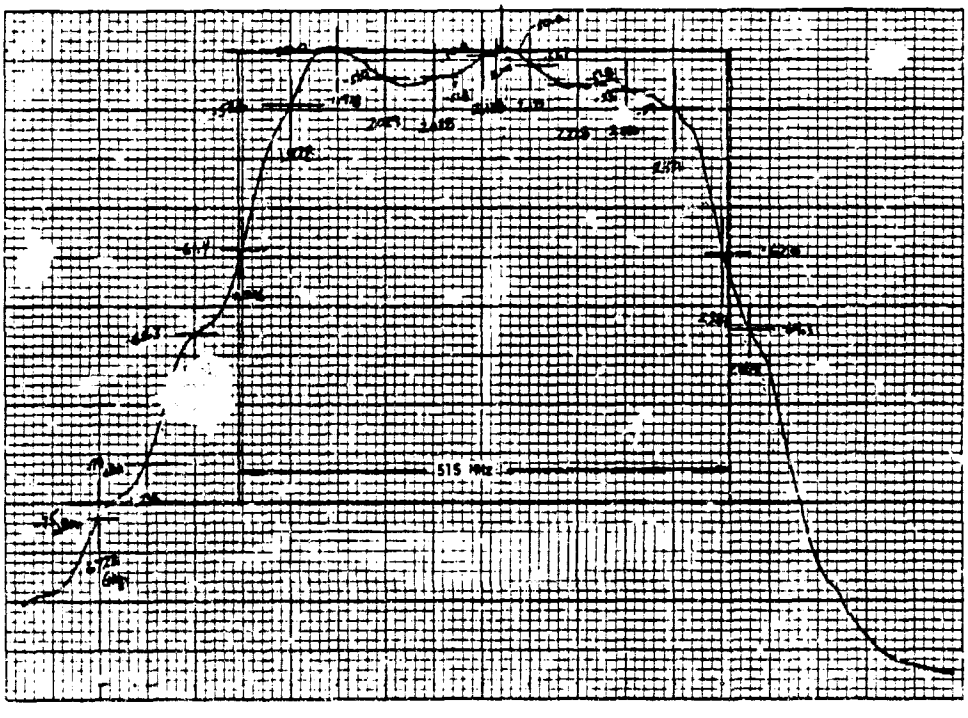


Figure 2.3-18 Noise Spectral Density of IF Amp/Noise Source

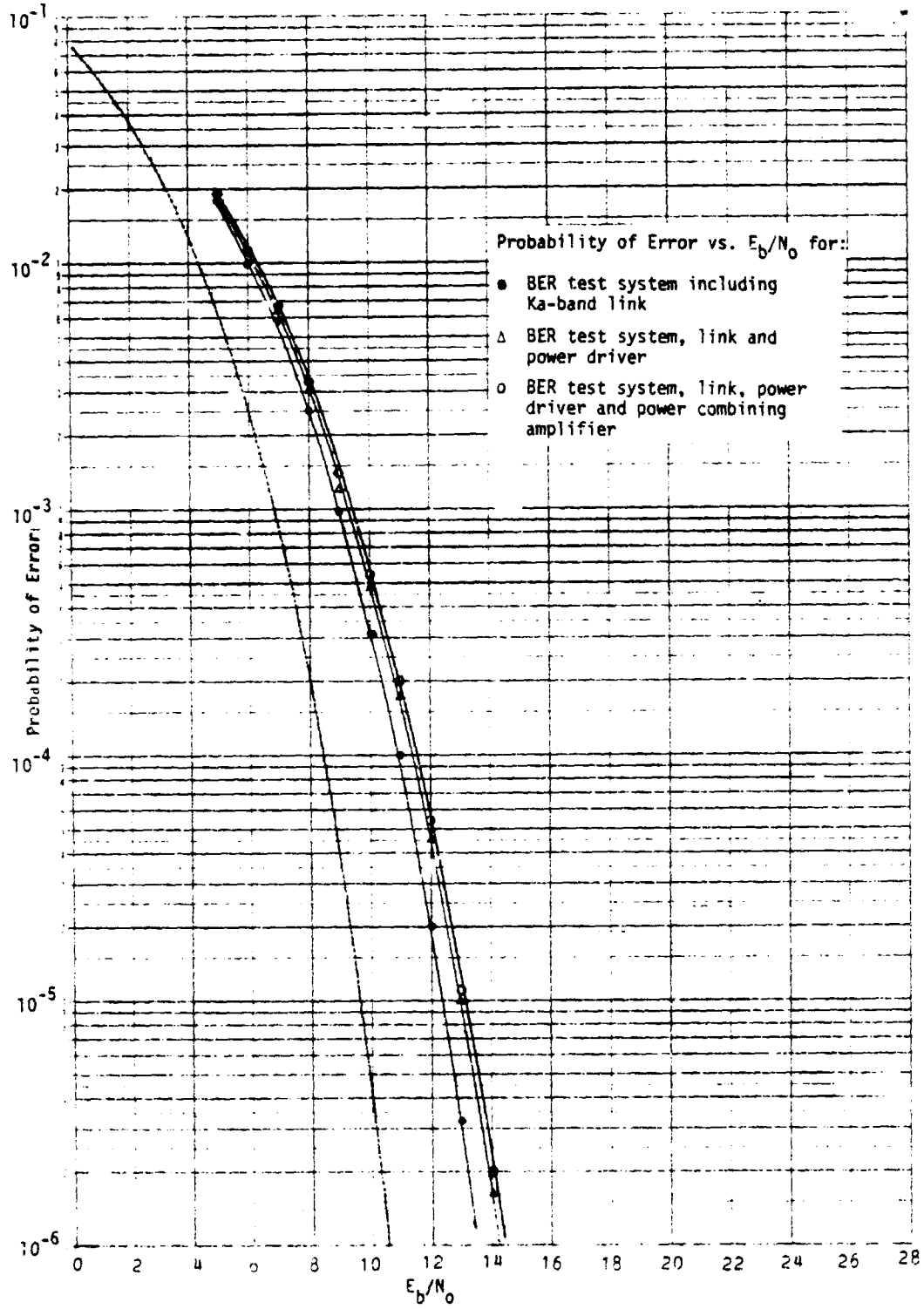


Figure 2.3-19 Composite BER Test Data

Table 2.3-1 Power Combining Amplifier BER Performance

BER	Degradation from Ideal (dB)		
	Test System	Power Driver	Combiner
10^{-2}	1.7	0.1	0.1
10^{-3}	2.3	0.3	0.1
10^{-4}	2.6	0.4	0.2
10^{-5}	2.8	0.7	0.1
10^{-6}	3.1	0.7	0.2

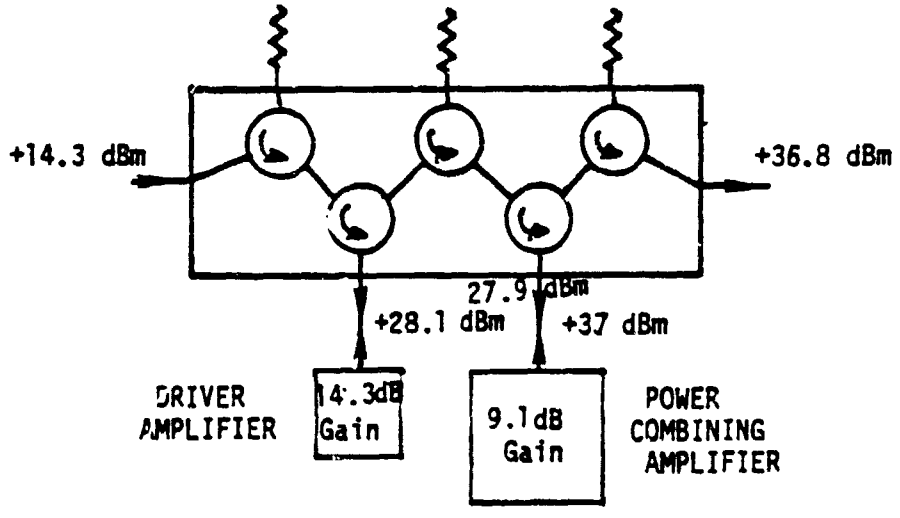


Figure 2.3-20 Amplifier Power Levels for Each Stage

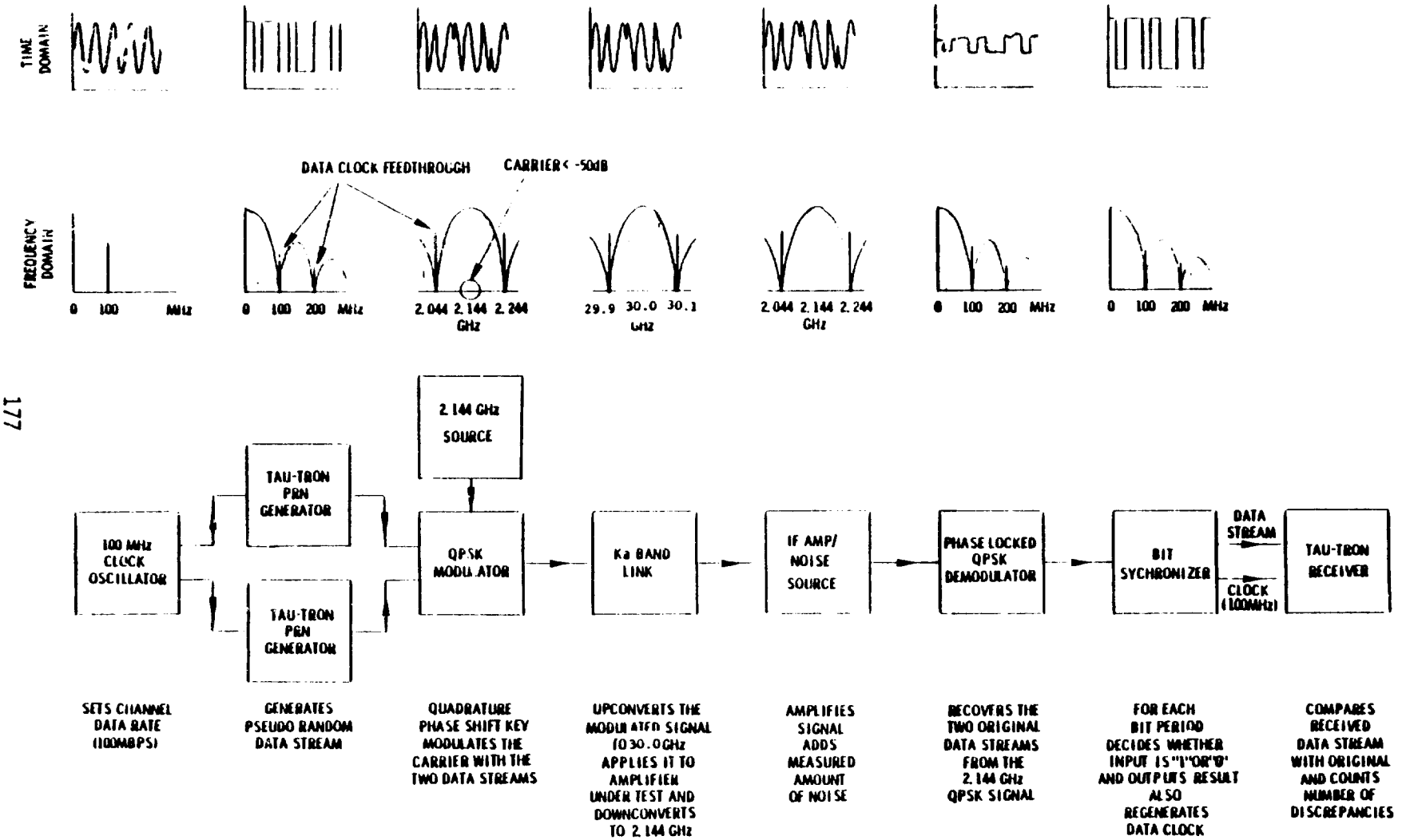


Figure 2.3-21. Progress of Signal through the BER Test System

2.4 PRODUCTION COSTS

The production costs for a 30 GHz 20W SSA unit in quantities of 50 and 250 are given in the preliminary estimates below, based on 1984 dollars. The estimates assume an advanced engineering model (as opposed to a POC model) that meets all electrical and environmental requirements for field tests. The estimated cost for setting up the investment casting equipment is $30 K.

Table 2.4-1 Production Cost Estimates

Part	No. of Pieces/Unit	Cost/Piece for 50 Units	Total per Unit	Cost/Piece for 250 Units	Total Per Unit
IC Regulator	13	$40.00	$520.00	$32.60	$424.00
Transistor	13	1.70	22.00	1.40	18.00
Diode, Zener	13	5.00	65.00	4.00	52.00
Diode, Switching	13	8.40	109.00	6.80	88.00
Resistors	156	0.33	52.00	0.27	42.00
Resistors, Variable	26	22.00	572.00	17.80	463.00
Thermistor	1	21.60	22.00	17.50	18.00
Capacitors	13	1.00	13.00	0.82	11.00
Four-Junction Circulator	1	185.00	185.00	150.00	150.00
One Diode Module	1	85.00	85.00	68.50	69.00
Twelve Diode Module	1	250.00	250.00	200.00	200.00
PIN Assemblies	13	8.60	120.00	7.00	91.00
Housing	1	1,025.00	1,025.00	830.00	830.00
Cover	1	85.00	85.00	68.00	68.00
Connectors	3	43.00	129.00	35.00	105.00
Switches	2	75.00	150.00	60.00	120.00
Magnets	8	8.00	64.00	5.50	44.00
Ferrites	16	4.90	78.00	4.00	64.00
Backshorts	2	1.90	3.80	1.50	3.00
Waveguide Runs	2	19.00	38.00	15.00	30.00
Power Supply/ Converter	1	1,230.00	1,230.00	1,000.00	1,000.00
IMPATT Diodes	25	490.00	12,250.00	400.00	10,000.00
PC Boards	4	185.00	740.00	150.00	600.00
Material Burden/ Attrition			4,452.00		3,623.00
Assembly Labor, (Burdened)			2,200.00		2,200.00
Test Labor (Burdened)			2,400.00		1,900.00
Unit Cost			$26,860.00		$22,213.00
Profit @ 15%			$4,029.00		$3,332.00
Total Unit Price			$30,889.00		$25,545.00

2.5 DEVELOPMENT SCHEDULE AND COST

TRW proposes a 24-month engineering development effort, a schedule of which is shown in Table 2.5.1. The total estimated development cost is $1.2M. In this effort, TRW will perform the following tasks:

1) Establish low cost rf and mechanical designs for the waveguide components such that they are amenable to volume production.

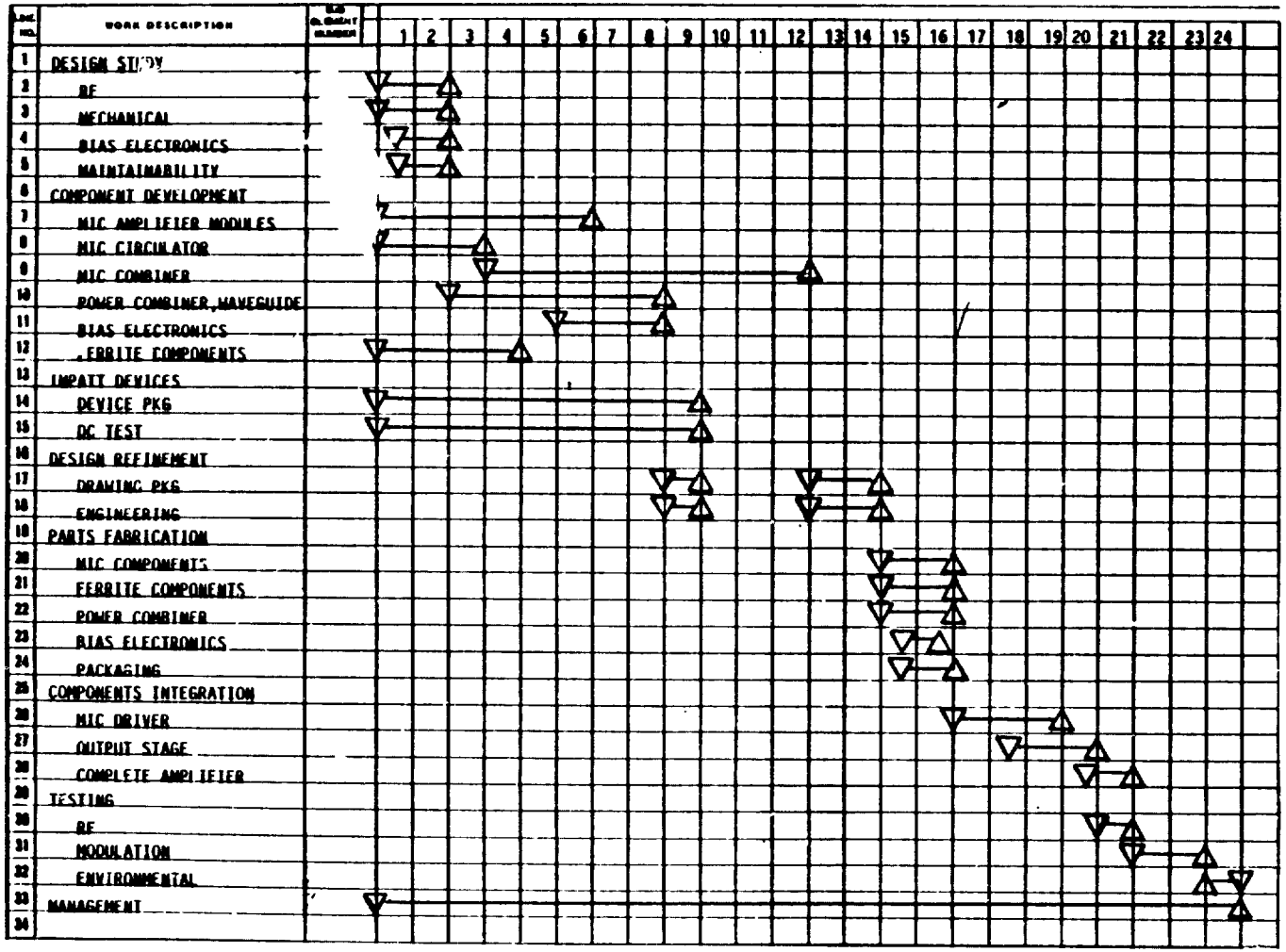
2) Develop low cost MIC driver (with redundancy).

3) Establisn low cost manufacture techniques such as investment casting.

4) Integrate and test complete amplifier in terms of a) rf characteristics, b) modulation characteristics, and c) environmental characteristics.

5) Deliver to NASA one Advanced Development Model (ADM) with associated drawing package.

Table 2.5-1. Development Schedule



3. REFERENCE

1. 30/20 GHz Low Data Rate Ground Terminal Design Study, Final Report, NASA Lewis Research Center Document Number 3-6-T-9-F2.