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Ball Aerospace Systems Division

System Engineering Report

CR-171-835
C.1

REPORT NO. _____ DATE 12/21/84

PROJECT
NASA/JSC

TITLE SPACEBORNE DISTRIBUTED SAR ANTENNA

PREPARED BY	DATE	APPROVED BY	DATE
Dan McKenna	12/28/84	H. Haddad	12/28/84

SCOPE/TEXT:(ATTACH ADDITIONAL SHEETS AS REQUIRED)

DISTRIBUTION

TABLE OF CONTENTS

I. INTRODUCTION

This report will summarize the development and testing of the MSAR C-Band array panel. From initial concepts through test completion, this paper will discuss each element of the antenna system individually as well as collectively.

Textual descriptions together with test data are both used to enable a clear understanding of the antenna system performance. And, in most instances, textual references are made to a particular photo, figure, or graph.

In general, test data has confirmed or exceeded expectations. Of particular note, excellent cross polarization isolation was achieved with a unique field cancelling geometry.

We are presently prepared to implement distributed amplifiers into this antenna system.

II. DEVELOPMENT

A number of concepts were investigated during the development stage to determine an optimum antenna design. The primary criteria during this phase was reduction of cross polarization or polarization isolation. Of course efficiency, radiation patterns, and impedance matching were also considered.

Initially, single patches were constructed on .047 inch PTFE to verify the correct patch size for its respective resonant frequency. Linear scaling was used to optimize patch operations at f_o. Efficiency experiments with .040 inch Rohacell and 2 bonded layers of .005 inch G-10 indicated that appreciable insertion loss existed with the composite substrate. Therefore, it was decided that PTFE would be used exclusively.

Next, individual single polarization columns were developed to determine the proper patch dimensions and spacing to minimize cross pole. The polarization feeds were integrated into a single column and dimensions again readjusted to minimize x-pole: -17dB of polarization isolation was measured for this iteration.

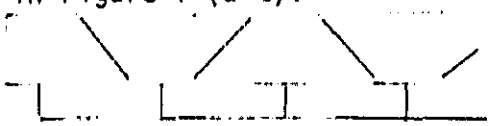
In order to ascertain the feasibility of achieving -19 dB sidelobes, a 12-way Taylor taper power divider was built and connected to a 12 patch linear array. In Table 1 we list the measured sidelobe performance of this power divider.

Table 1

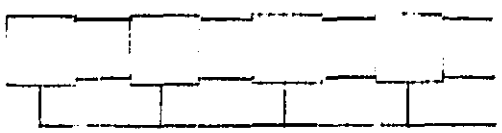
Measured Sidelobes Performance for a Taylor Taper Power Divider

Frequency	First Sidelobe
5.25 ghz	-18dB
5.30 ghz	-19dB
5.35 ghz	-17dB

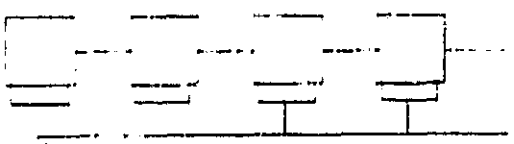
Throughout the lengthy development phase, many different and unique models were designed and tested. Only a few will be mentioned here and test data will not be provided in this paper. However, it should be noted that each model was conceived to optimize cross polarization between ports. A few of these concepts are shown in Figure 1 (a-e).



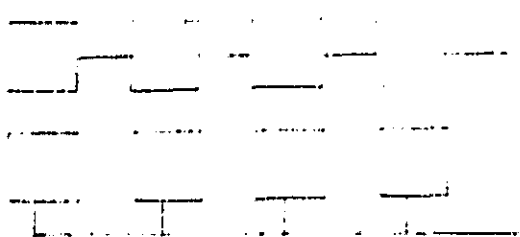
(a) E Plane Cross Pole Cancels Patch to Patch



(b) No Cross Pole Excited in E Plane



(c) Similar to Above, Other Port



(d) Separate Columns for Each Polarization
Unworkable due to Spacing Requirements
for Elevation Beam Steering

(e) Franklin Antenna (Vertical Polarization Did Not Work)

Figure 1 Various Series Fed Antenna Concepts

The final version, which will be discussed in the next section, fed both series arrays (horizontal and vertical polarization) 180 degrees out of phase. The cross pole for port 1 cancelled with a single row while port 2 required the addition of an inverted row back-to-back with the original.

III. ANTENNA

The final antenna panel is a 12 x 18 patch array (row and column). It is fed by pins through the substrate to the power divider board (the antenna and power divider are back to back). The panel is etched on .047 inch PTFE with an ε_r=2.50. Actual dimensions are approximately 26.5 inches wide by 19 inches high.

The array is fed at the center of each row in a vertical fashion. The horizontal polarization is fed in series (electrically in parallel except for series line loss) while the vertical polarization is fed in parallel.

By feeding the horizontal polarization at the center and out of phase to each side, field cancellation yields the desired cross pole. Likewise, the vertical polarization's cross pole is reduced by inverting one row and feeding it 180 degrees out of phase. Measured cross polarization as a function of frequency, polarization, and pattern cut (Az or El) can be seen in Table 2.

Copies of the test patterns are arranged as follows:

Frequency (GHz)	Polarization	Figure
5.275	Vertical	2
5.275	Horizontal	3
5.300	Vertical	4
5.300	Horizontal	5
5.325	Vertical	6
5.325	Horizontal	7
5.350	Vertical	8
5.350	Horizontal	9

It appears, as evidenced by occasional non-symmetric sidelobes, that a slight phasing error exists. These errors are caused by the final integrated power divider pin interconnection(s) between antenna and power divider, and slight changes in the relative dielectric constant ε_r of the array in the final version of fabrication (that is relative to the iterations before the current one).

Gain measurements over frequency for the two polarizations, horizontal and vertical, are shown in Figures 10 and 11, respectively.

Table 2

AVERAGE FIRST SIDELOBE LEVEL

5.275 GHz	Az	X-Pole	El	X-Pole
Hor	-11.6 dB	-31.9	-16.9 dB	-25.2
Vert	- 9.7 dB	-28.7	-16.2 dB	-32.7
5.30 GHz	**Az**		**El**	
Hor	-13.0 dB	-31.8	-17.0 dB	-25.6
Vert	-12.4 dB	-30.3	-17.3 dB	-36.7
5.325 GHz	**Az**		**El**	
Hor	-15.2 dB	-32.3	-16.8 dB	-29.6
Vert	-13.2 dB	-31.4	-18.1 dB	-35.2
5.350 GHz	**Az**		**El**	
Hor	-14.3 dB	-30.2	-17.7 dB	-32.5
Vert	-10.9 dB	-28.9	-17.7 dB	-33.8
5.375 GHz	**Az**		**El**	
Hor	-12.8 dB	-29.4	-19.9 dB	-30.0
Vert	Not Measured		Not Measured	

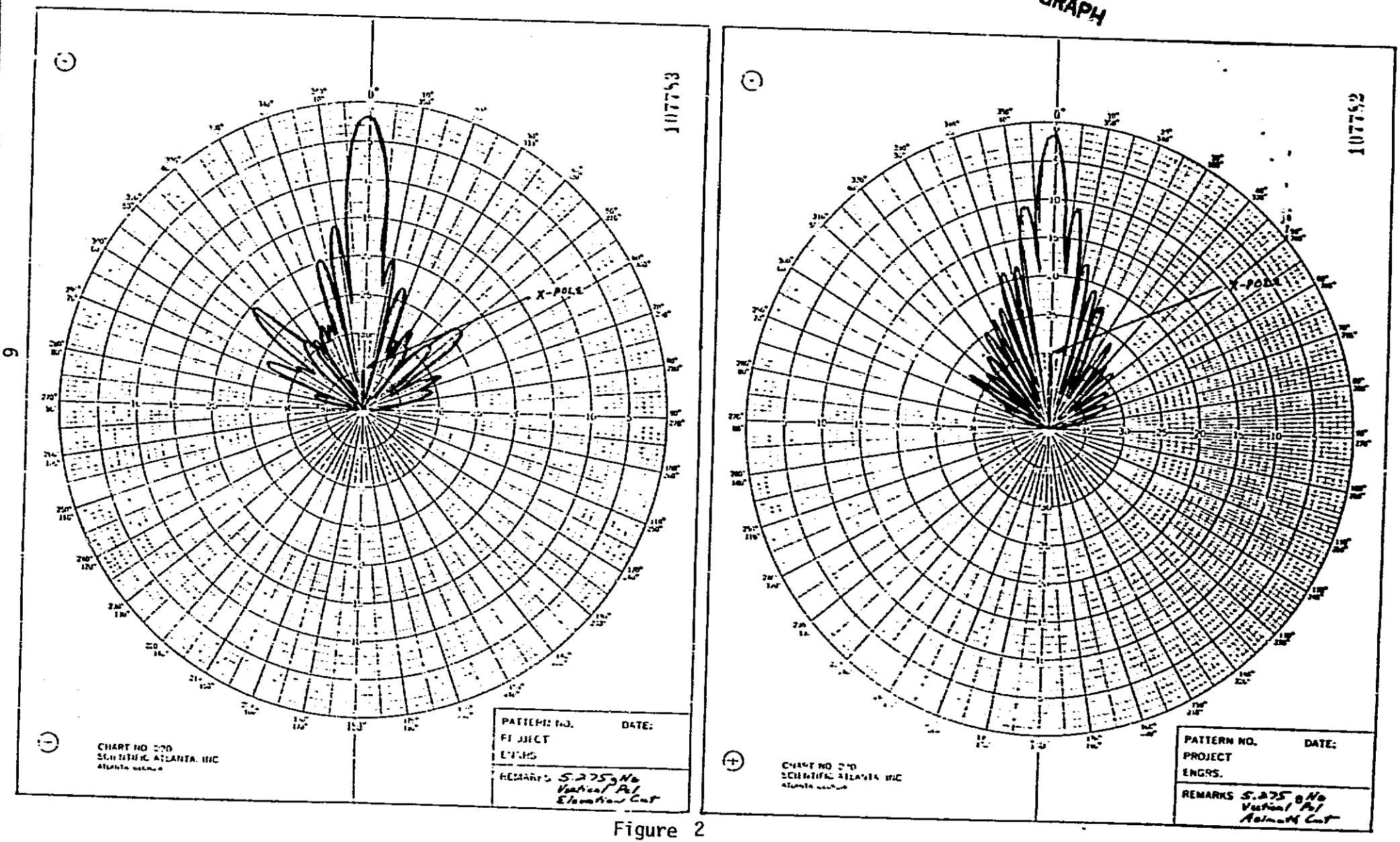
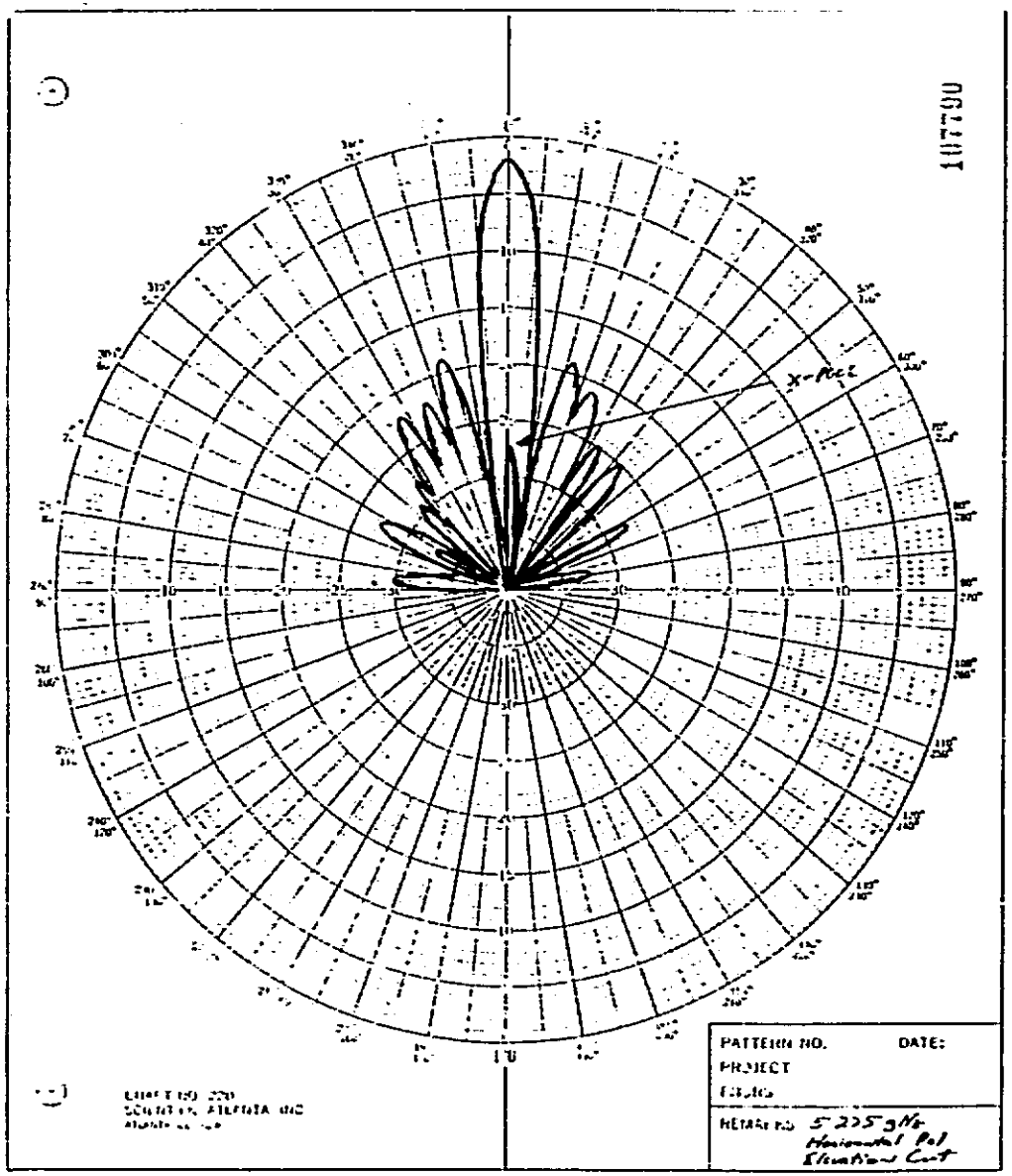


Figure 2



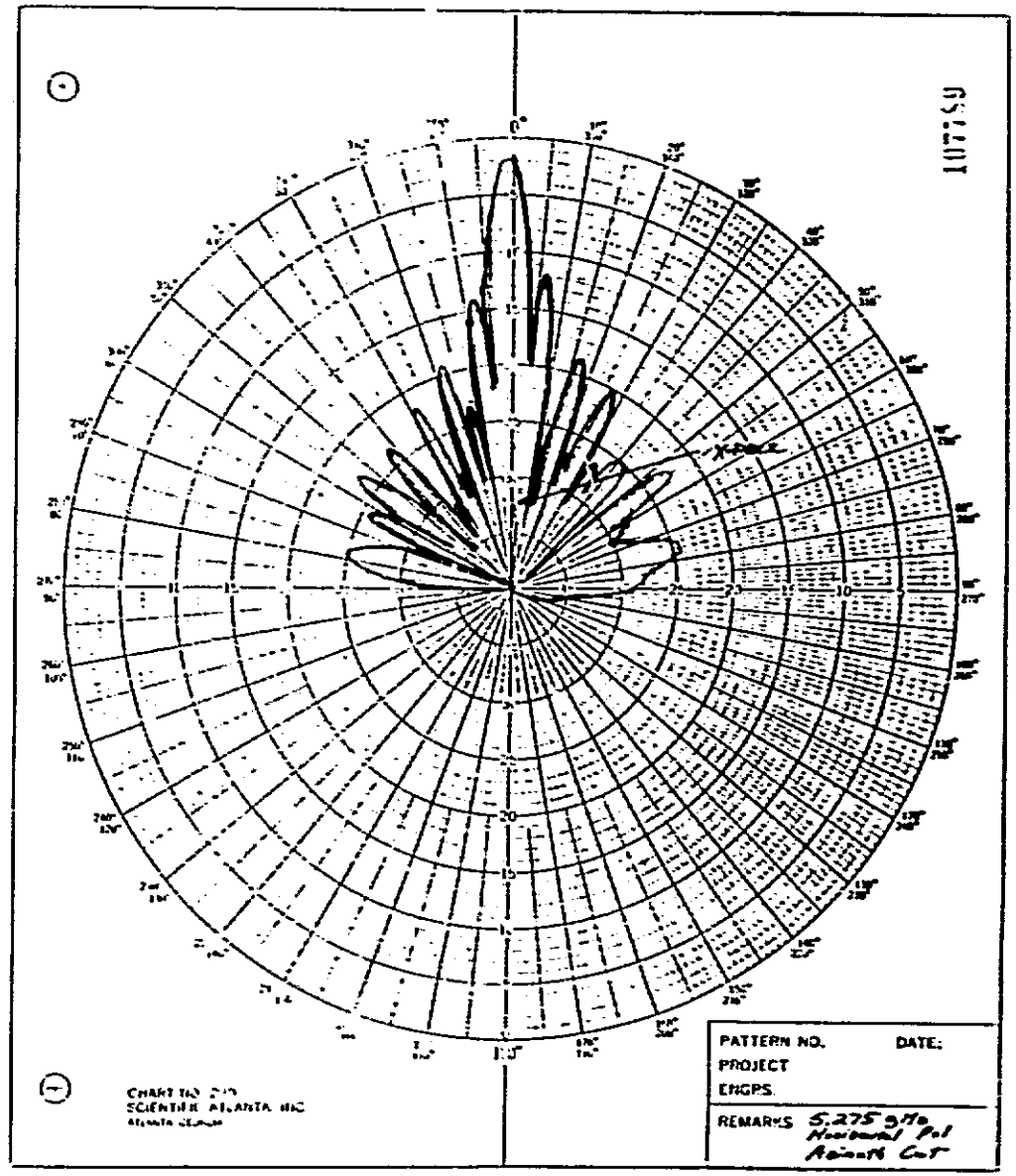


Figure 3

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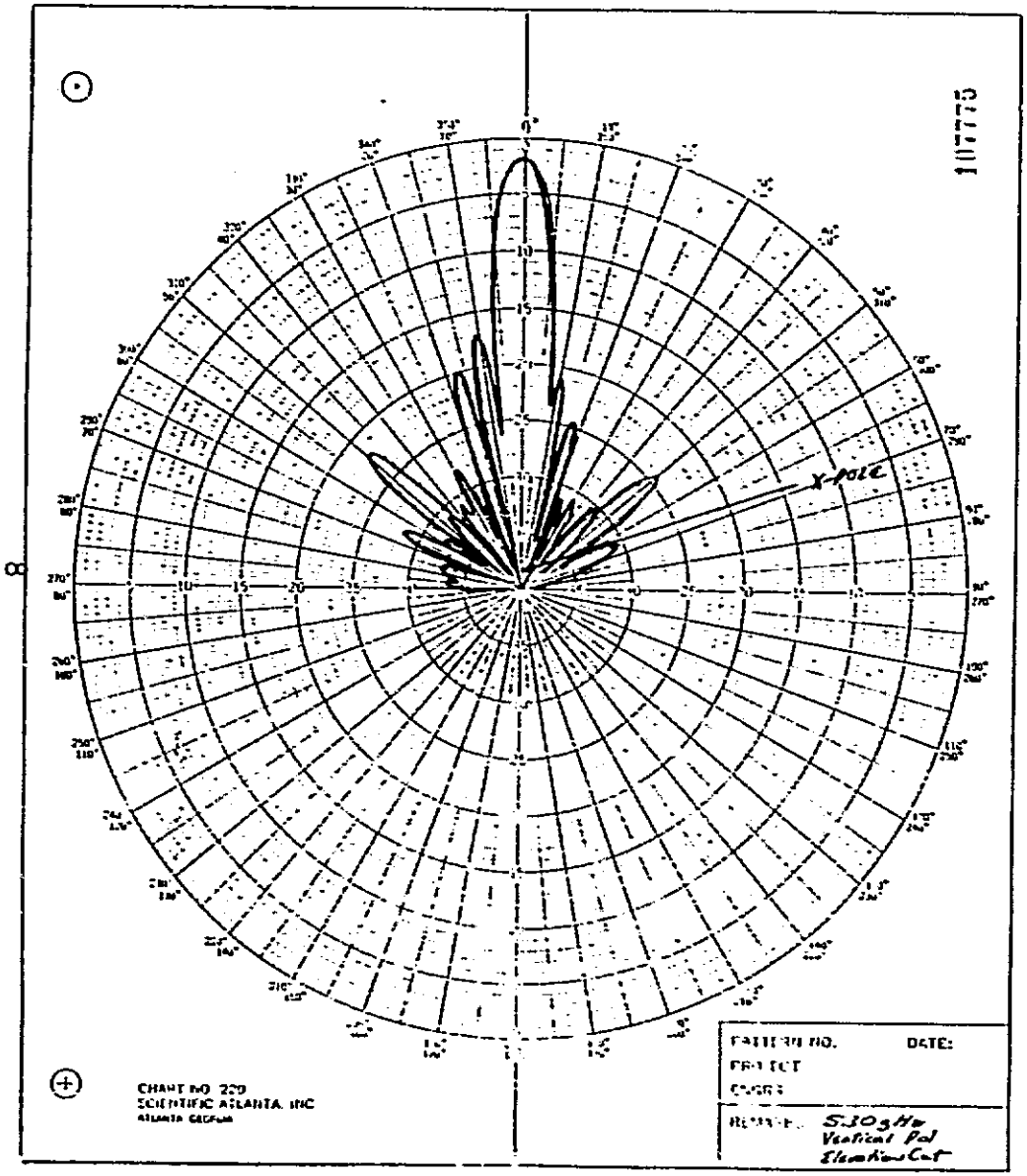


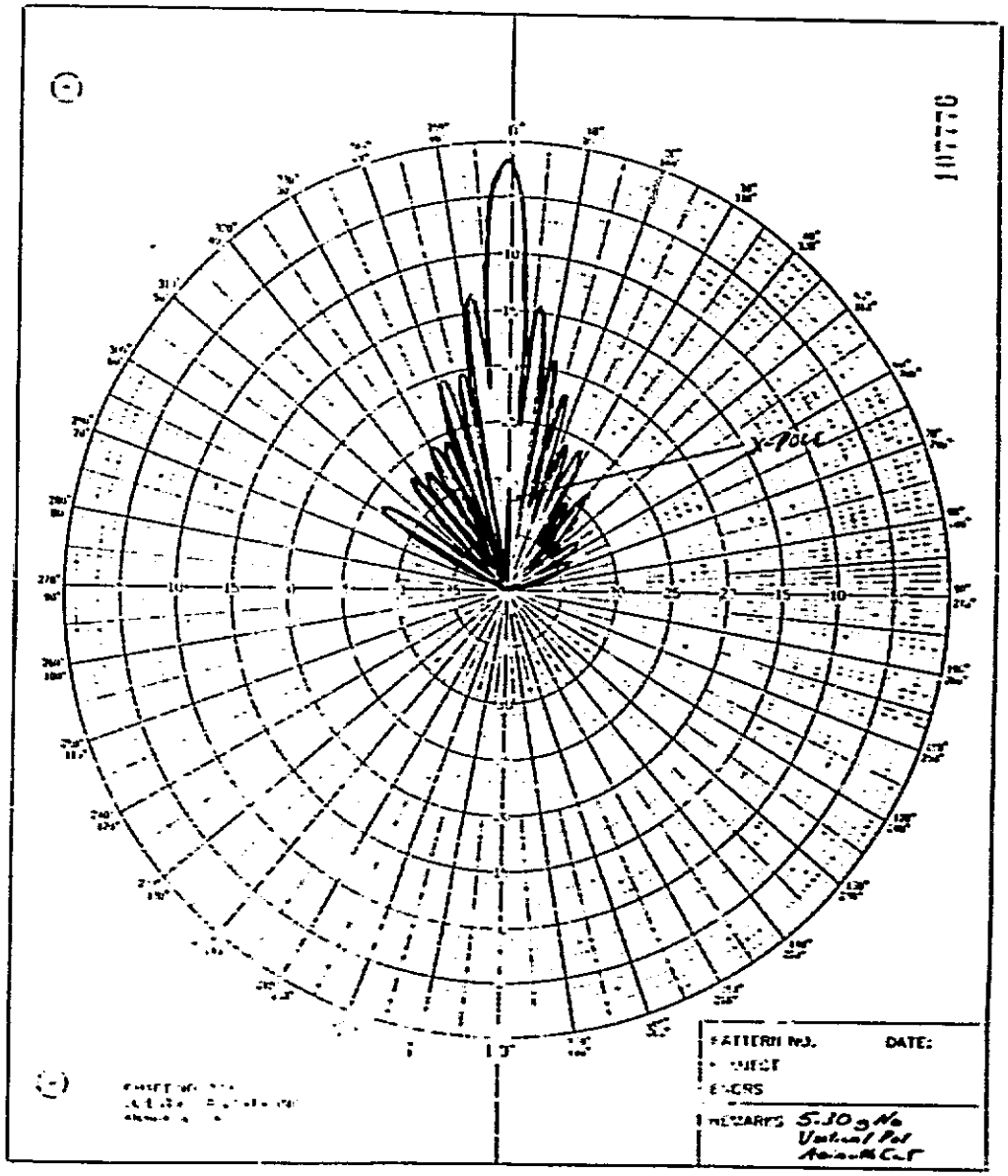


Figure 4

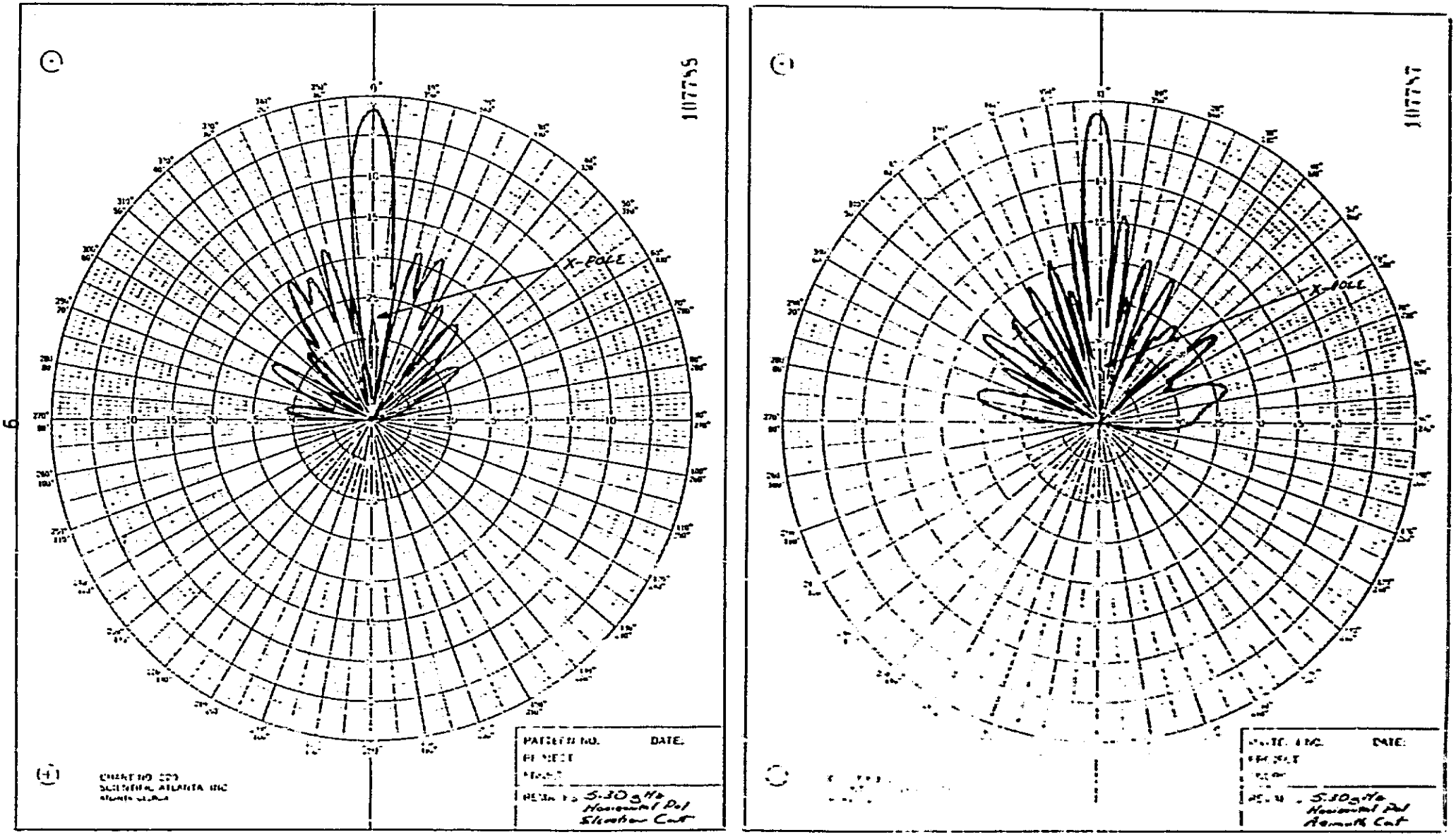
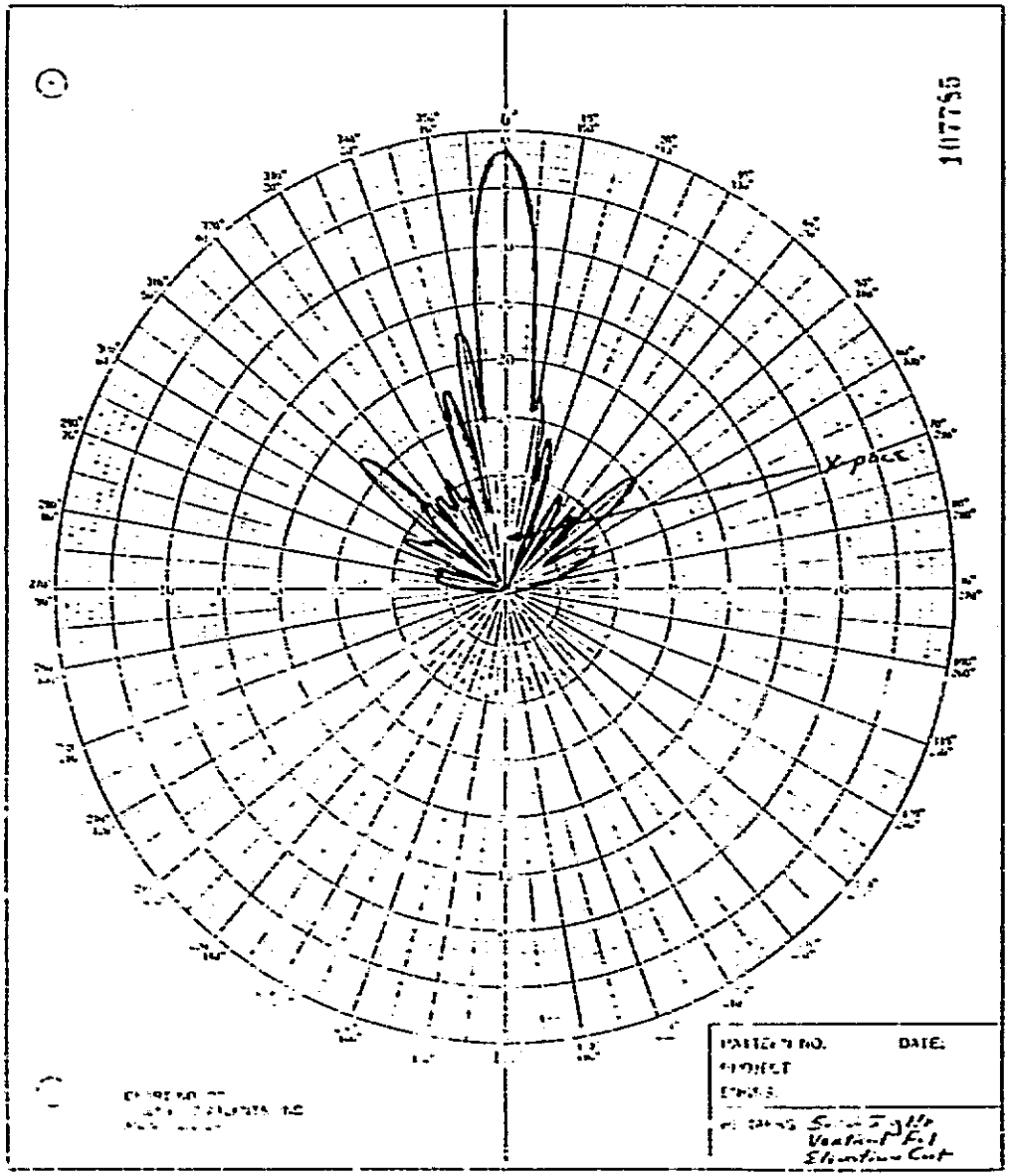
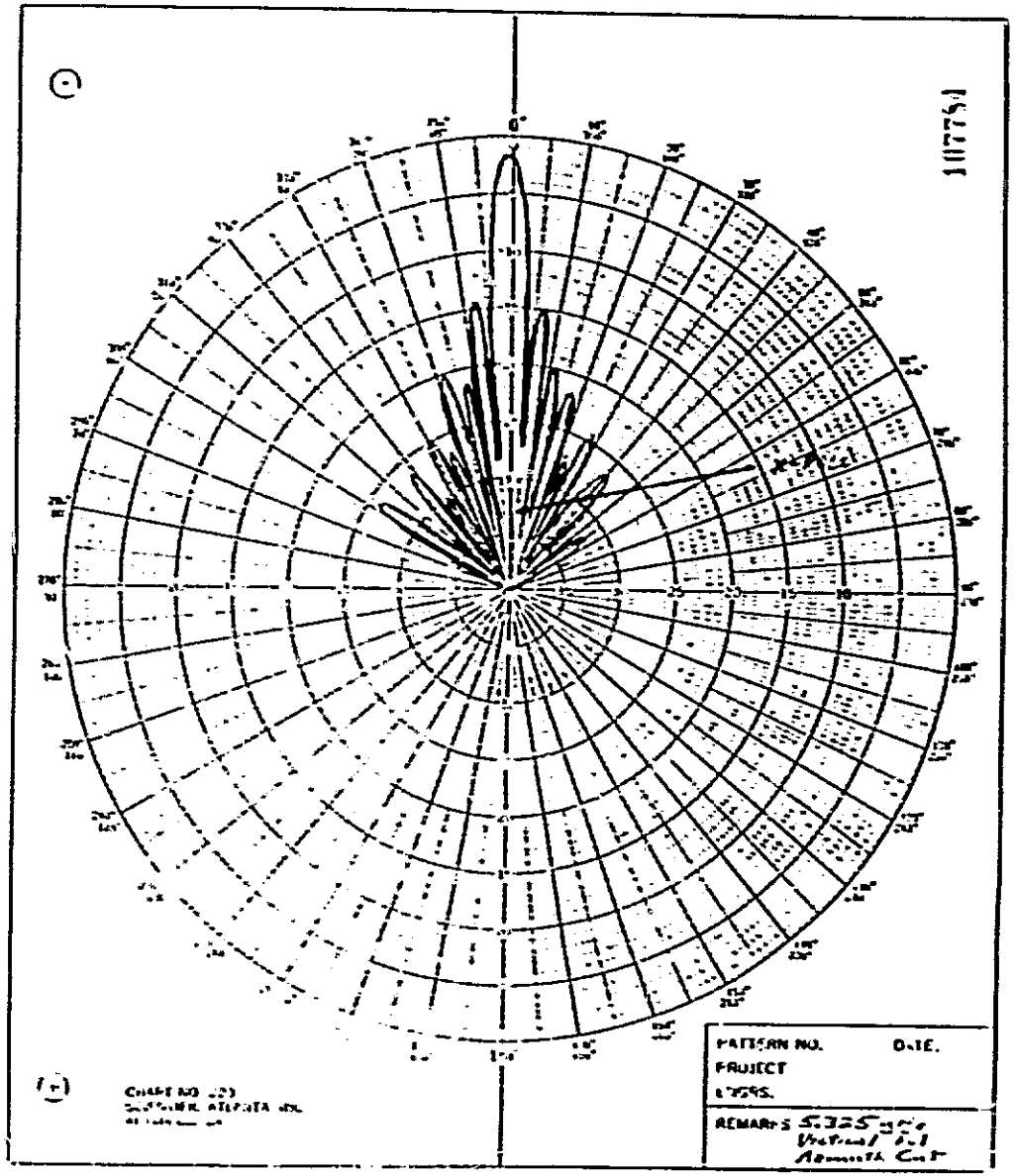


Figure 5





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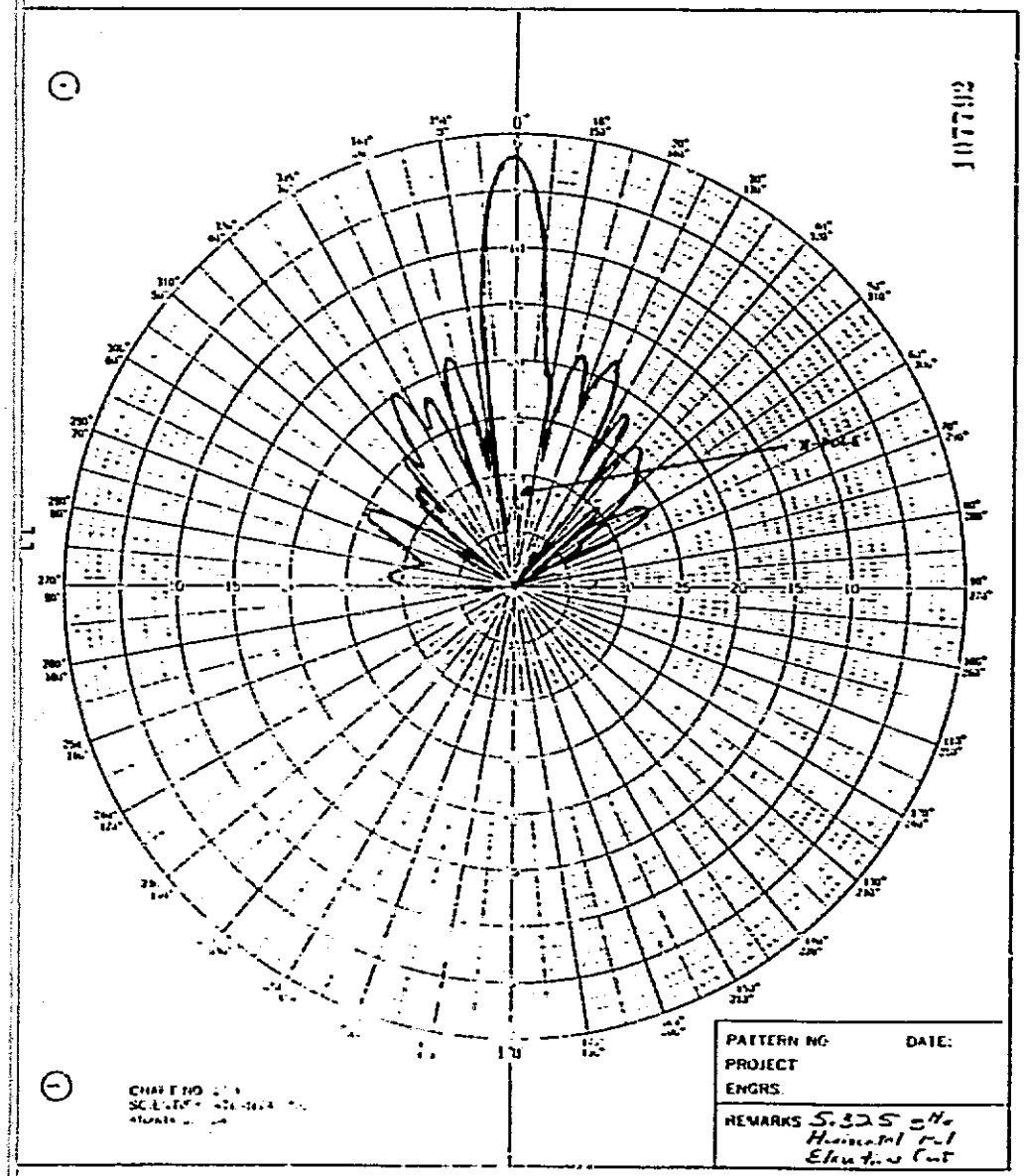

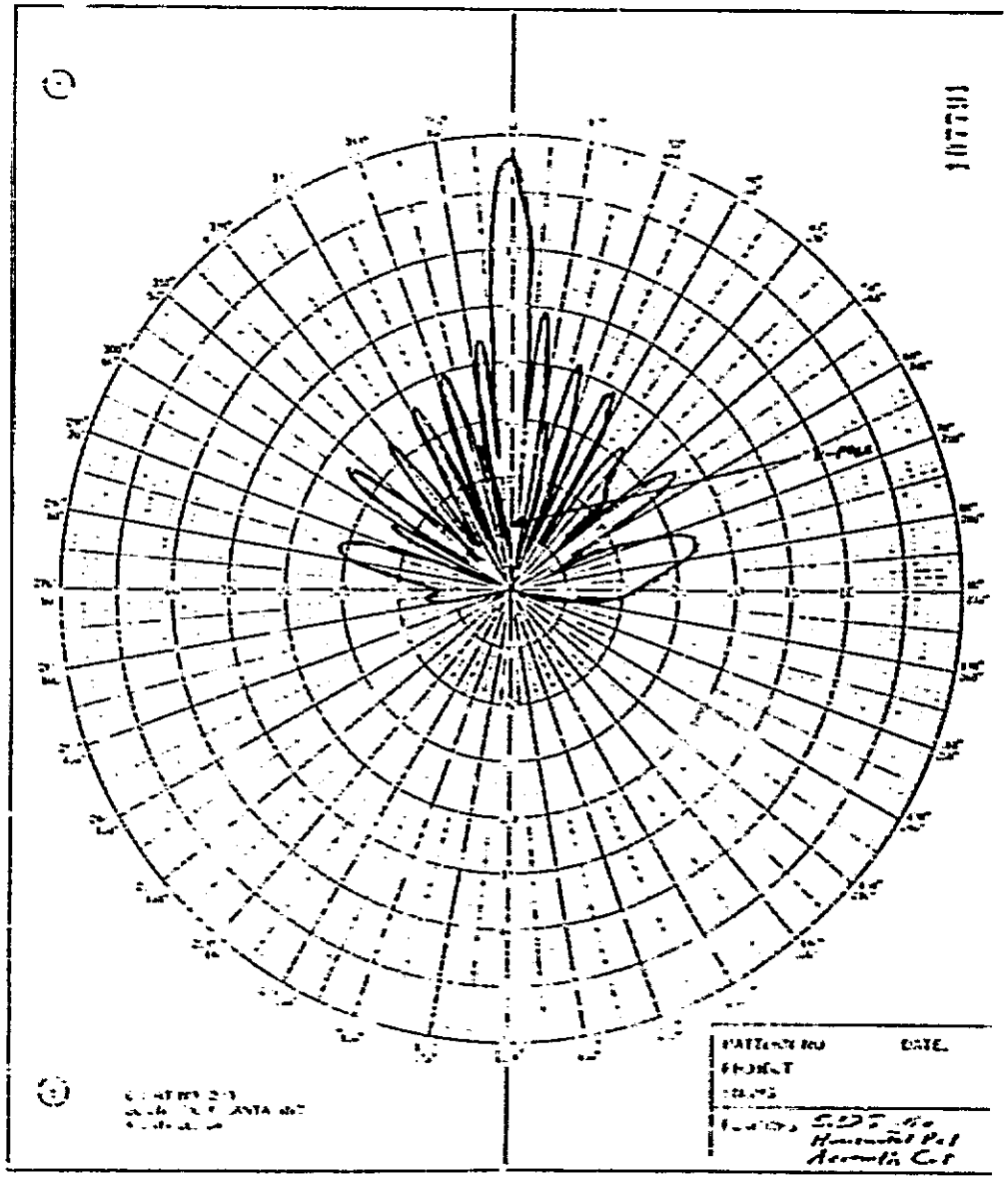

Figure 7

Figure

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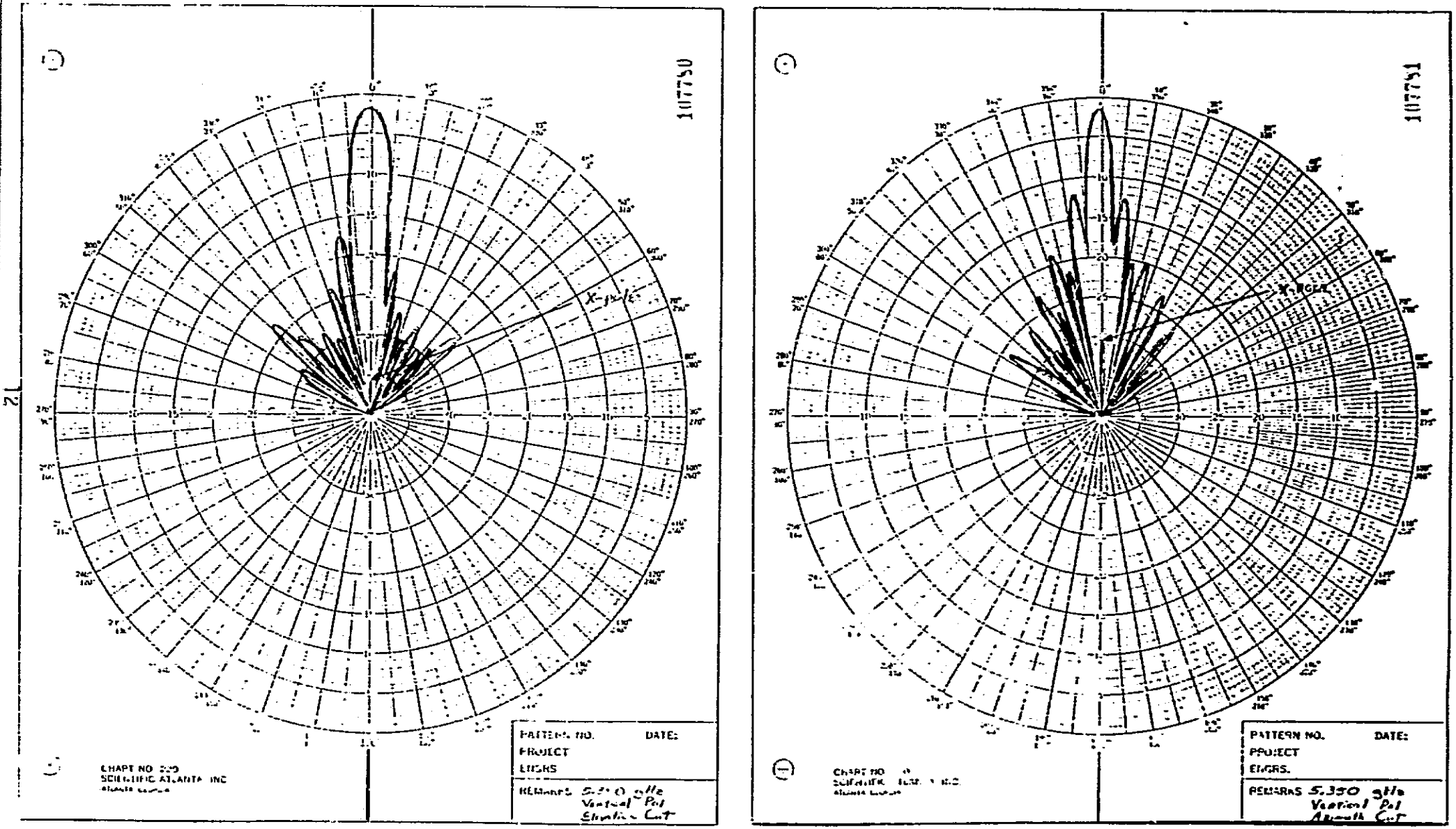


Figure 8

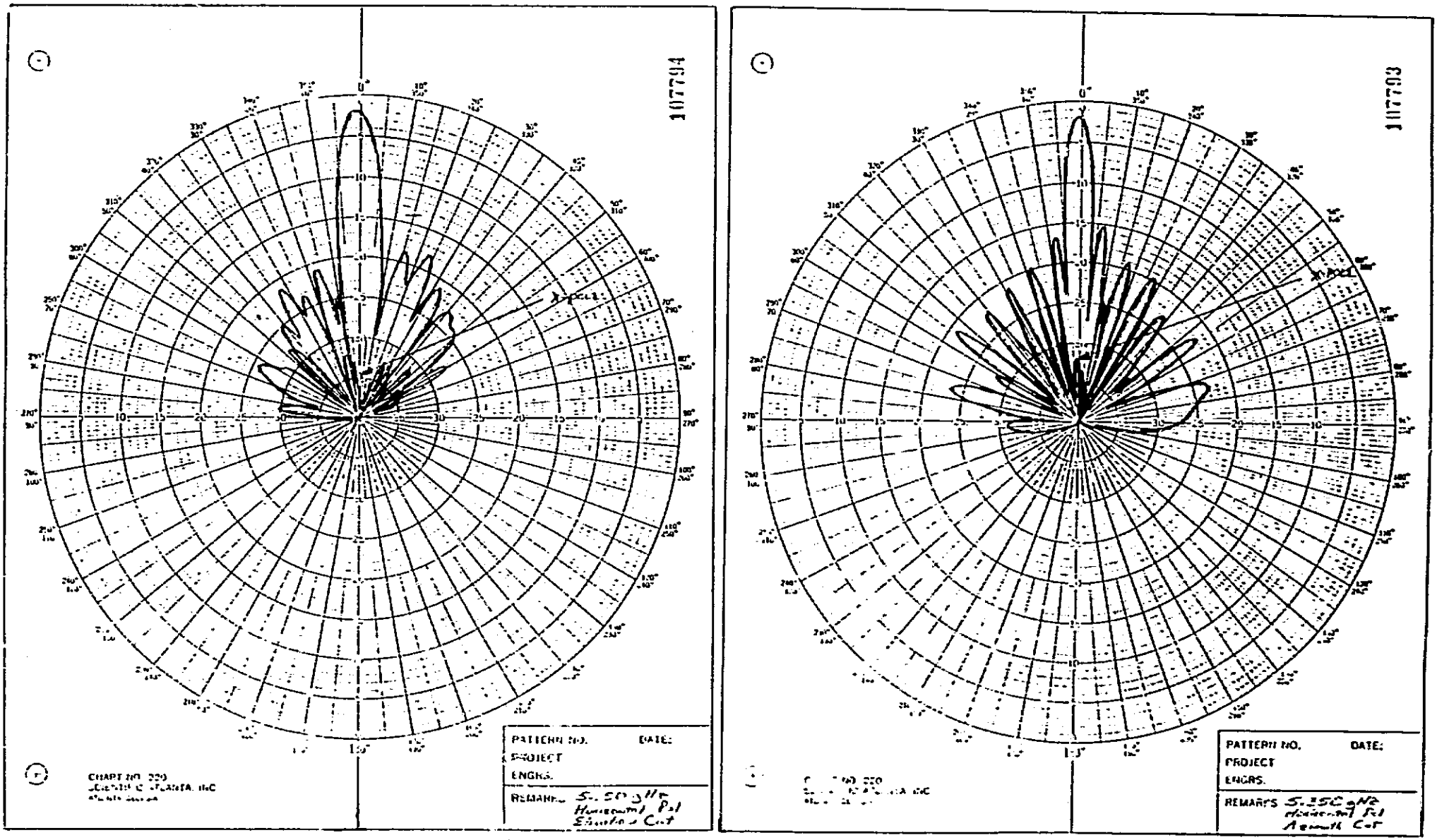
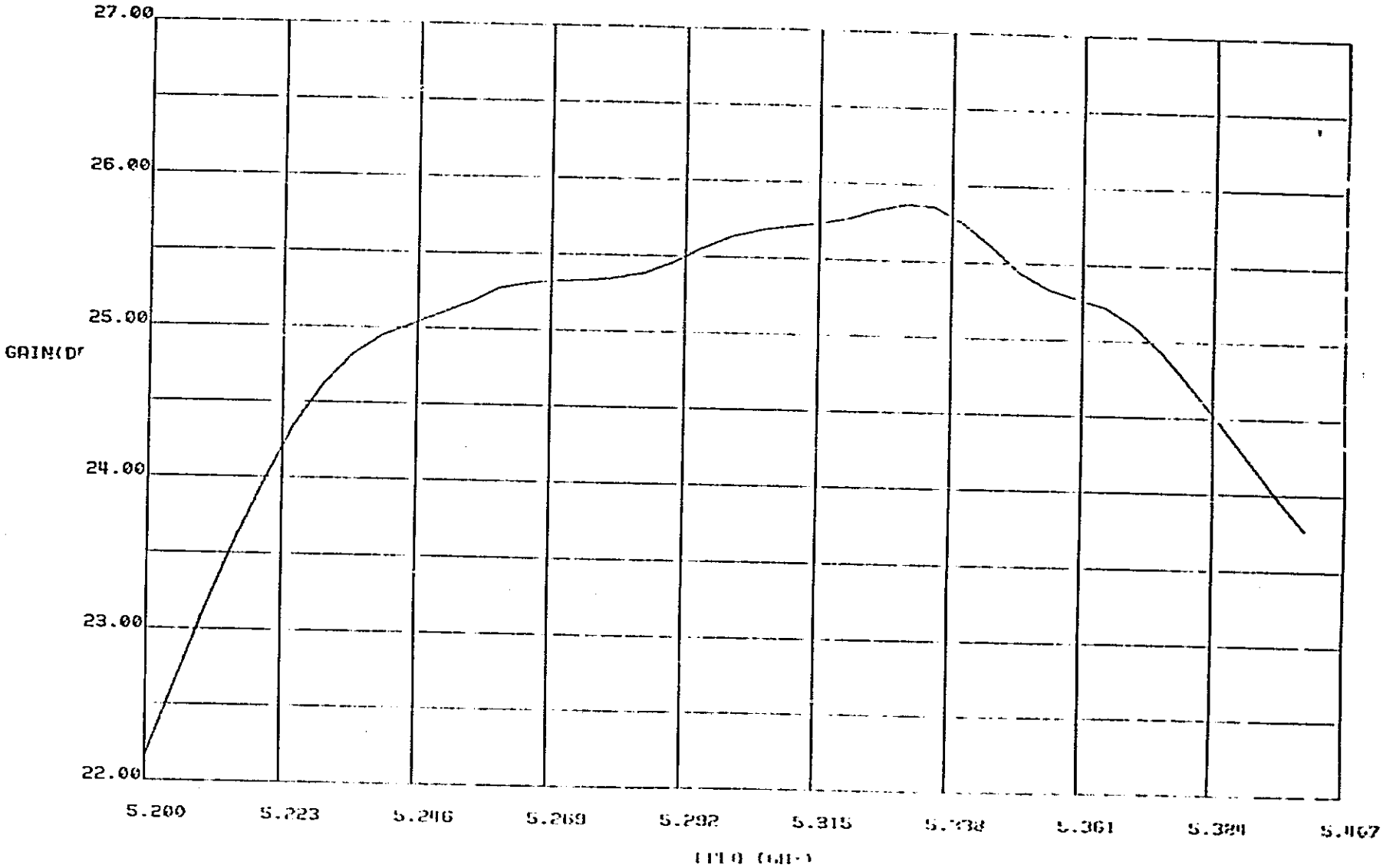
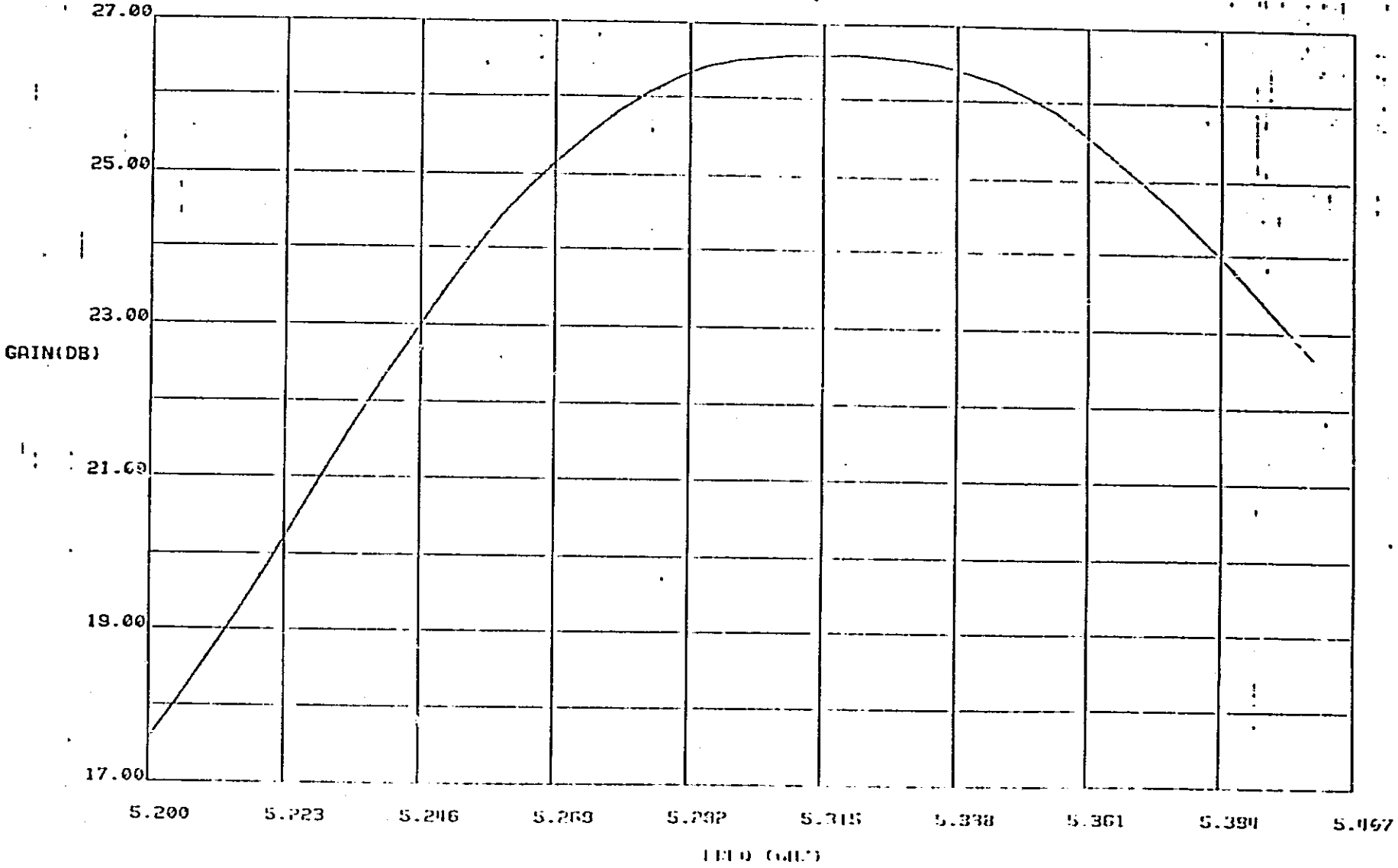


Figure 9



Horizontal Polarization
Port 1

Figure 10



Vertical Polization
Port 2

Figure 11

IV. POWER DIVIDER

Power dividers were designed to separately feed the input ports of the array -- horizontal and vertical polarizations. Port 1, horizontally polarized, provides 12 in-phase feeds to the 12 series fed patch rows. The vertically polarized port 2 establishes feed phases that alternate 0 and 180 degrees in order to properly phase the inverted patch rows (for cross pole cancellation).

Each power divider (port 1/port 2) is configured to deliver a Taylor amplitude distribution in the elevation plane. This in turn develops sidelobes that roll off monotonically. An amplitude taper was designed to enable the first sidelobes to be a minimum of -18dB below the main lobe. In contrast, the azimuth plane is uniformly illuminated and can only achieve a maximum of -13dB for its respective first sidelobes. (Neglecting the inherent taper due to the series feed arrangement)

During fabrication, a number of factors affected power divider test measurements: connector quality, connector soldering, board material, and external connector torque (cables to automatic network analyzer). In addition, the quality, S_{11} and S_{21} of the 50 ohm loads played an important role in the repeatability of test data. However, with careful fabrication using quality connectors/board material coupled with exacting test procedures, data repeatability was carried out to within .2dB in amplitude and 1 degree in phase.

Since the complete power divider is symmetric, i.e., one side is a mirror image of the other, only one side was initially built/tested for each port. When test results indicated nominal performance, the entire power divider was fabricated (See Figure 21). Note that the feed line (from the connector) for port 2 is displaced by 90 degrees (approximately 370 mils) to maintain proper patch row phasing. Port 1 is fed symmetrically.

The desired relative amplitudes, referenced to the innermost patch row (array centerline), as well as the measured data are listed in Tables 3, 4, and 5.

Table 3

Calculated Power Divider Amplitude Distribution

Port	Amplitude (dB)
A	0
B	-.63
C	-1.79
D	-3.26
E	-4.58
F	-5.12

Table 4

Port 1, Horizontal Polarization, Test Data

Port	Amplitude (S_{21})(dB)	Amplitude (dB)	%	Phase(deg)	Phase (deg)
A	6.41	0.00	22.86	57.5	0.00
B	7.20	-.79	19.05	57.2	-.30
C	8.55	-2.14	13.96	53.3	-4.20
D	9.94	-3.53	10.14	56.9	-.60
E	11.32	-4.91	7.38	55.3	-2.20
F	12.35	-5.94	5.82	53.1	-4.40

Insertion loss = -1.01 dB

Table 5

Port 2, Vertical Polarization, Test Data

Port	Amplitude (S_{21})(dB)	Amplitude (dB)	%	Phase(deg)	Phase (deg)
A	6.71	0	21.33	-10.8	178.8
B	6.95	-.24	20.18	168.0	
C	7.75	-1.04	16.79	-8.9	177.5
D	9.43	-2.72	11.40	168.6	
E	10.70	-3.99	8.51	-10.3	180.8
F	11.33	-4.62	7.36	170.5	

Insertion loss = -.68 dB

VI. PHASE SHIFTER

The phase shifter circuitry was generated using the CALMA CAD system. The circuit consists of 3 phase shifters (45^{o}, 90^{o}, and 180^{o}) with 90^{o} quadrature hybrids and one (22.5^{o}) with a loaded line design. These phase shifters along with dc bias lines are etched on a .032" thick PTFE substrate. The pin diodes are hermetically sealed to insure operation under a variety of conditions: the high vibration environment of shuttle lift off and landing, space vacuum, temperature effects, and ground humidity.

Test data indicates a worst case insertion loss of about 2.5 dB at 5.30 GHz (Figure 12). Test connectors and feed lines account for approximately .5 dB loss; thus actual insertion losses are on the order of 2.0 dB. The pin diodes are responsible for most of this loss. Figure 13 shows the return losses for each bit.

Phase analysis shows all the bits are accurate within $\pm 2^{o}$ over the frequency band of 5.26 to 5.34 GHz.

In Figures 14 through 17, we show the measured phases (over frequency) for each of the bits, 22.5^{o}, 45^{o}, 90^{o} and 180^{o}, respectively.

Ball Stripline ANTENNAS

PROJECT NO. 3845 PROGRAM PEACEKEEPER TRIBAND ANTENNA SYSTEM
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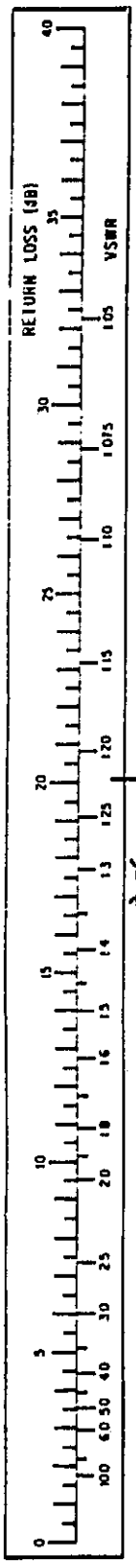

☐ RETURN LOSS; ☒ INSERTION LOSS; ☐ PHASE CHART

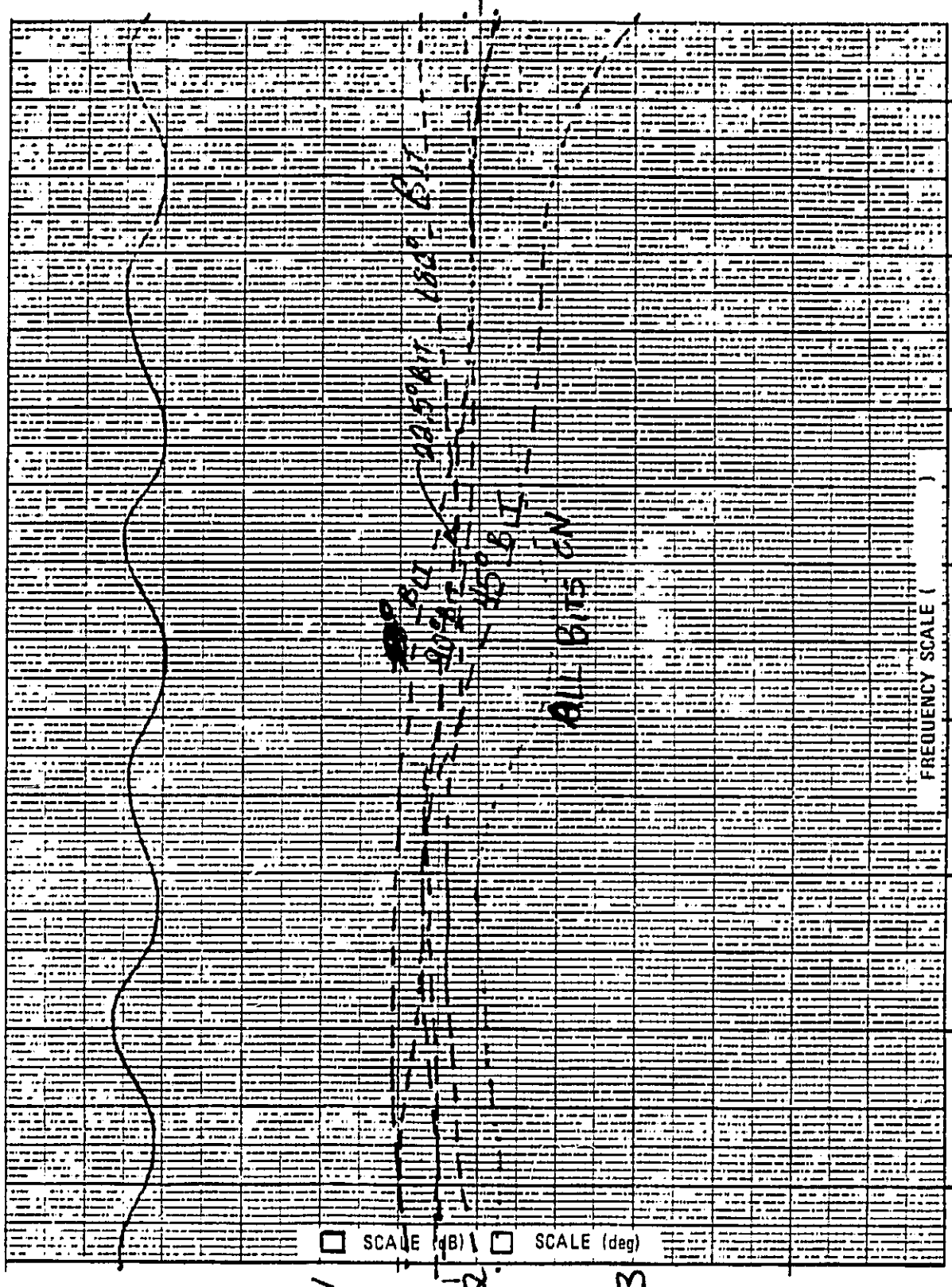

Figure 12

BALL AEROSPACE SYSTEMS DIVISION

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ANTENNAS

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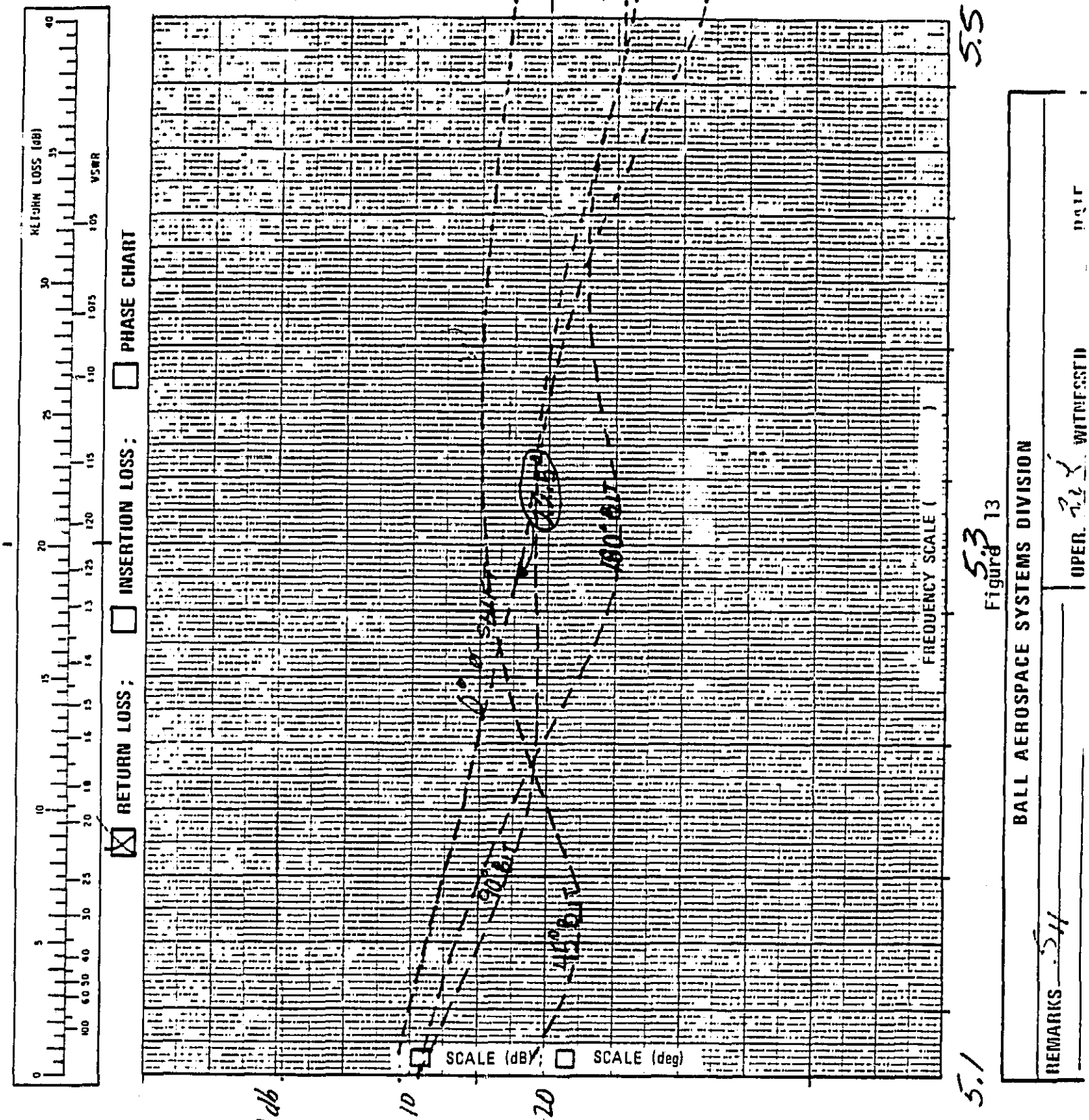
TEST TYPE: ☐ QUALIFICATION ☐ ACCEPTANCE ☐ OTHER
FREQUENCY RANGE _____ SHEET _____ OF _____



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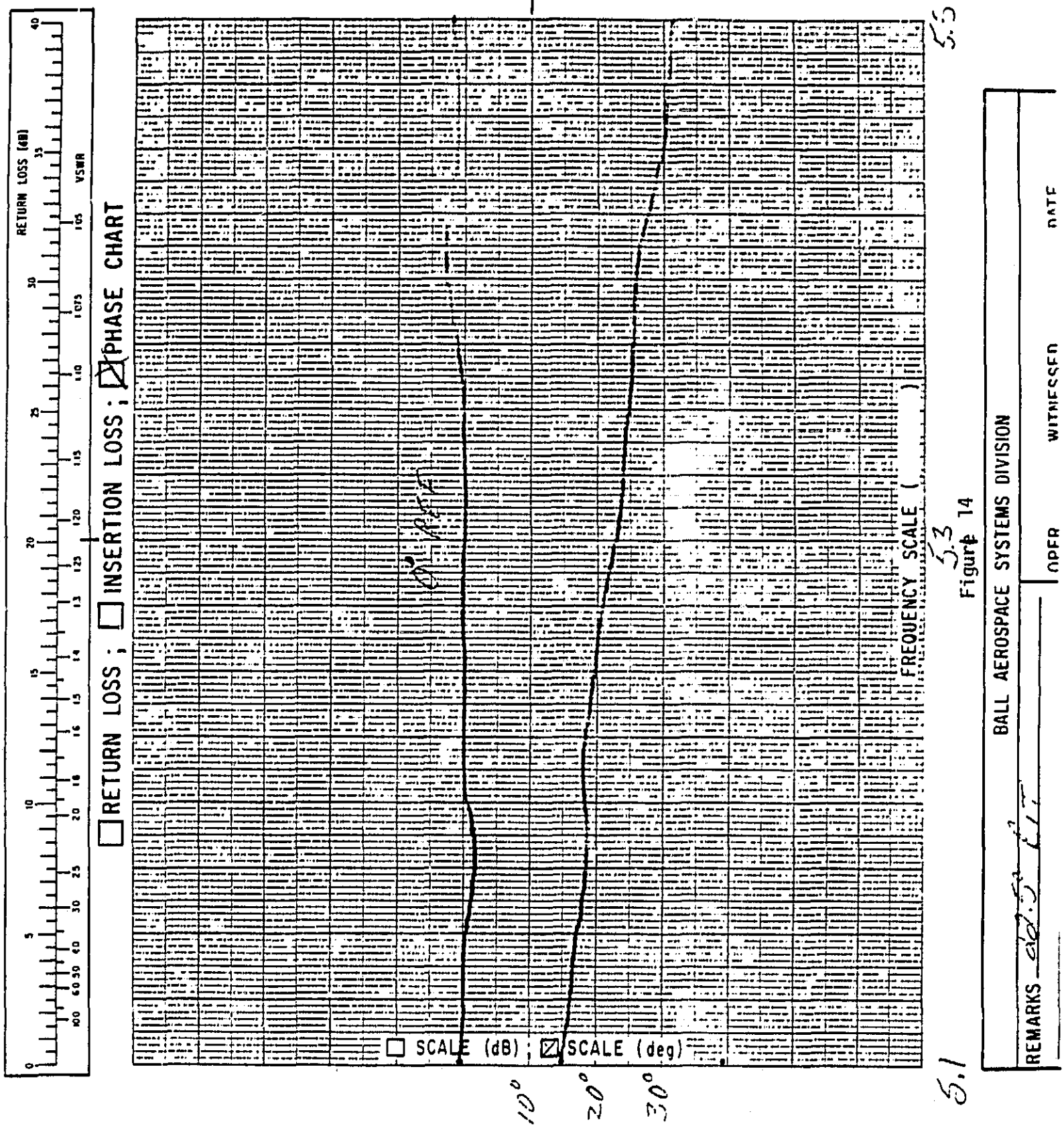

Figure 14

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Ball Strip Antennas

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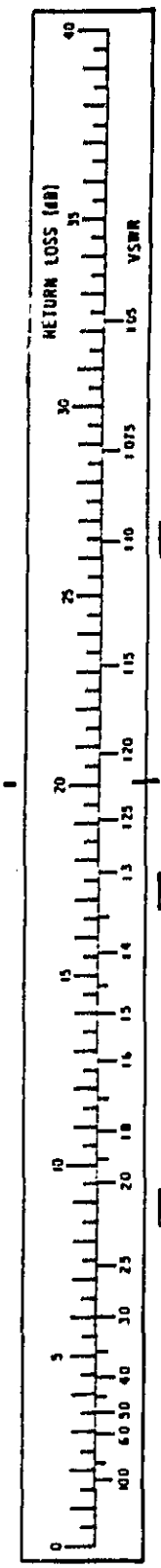
PART NO. _____ MODEL NO. _____ SERIAL NO. _____

TEST TYPE: ☐ DEVELOPMENT ☐ PRE ☐ FINAL

FREQUENCY RANGE _____ SHEET ____ OF ____



☐ RETURN LOSS ; ☐ INSERTION LOSS ; ☒ PHASE CHART

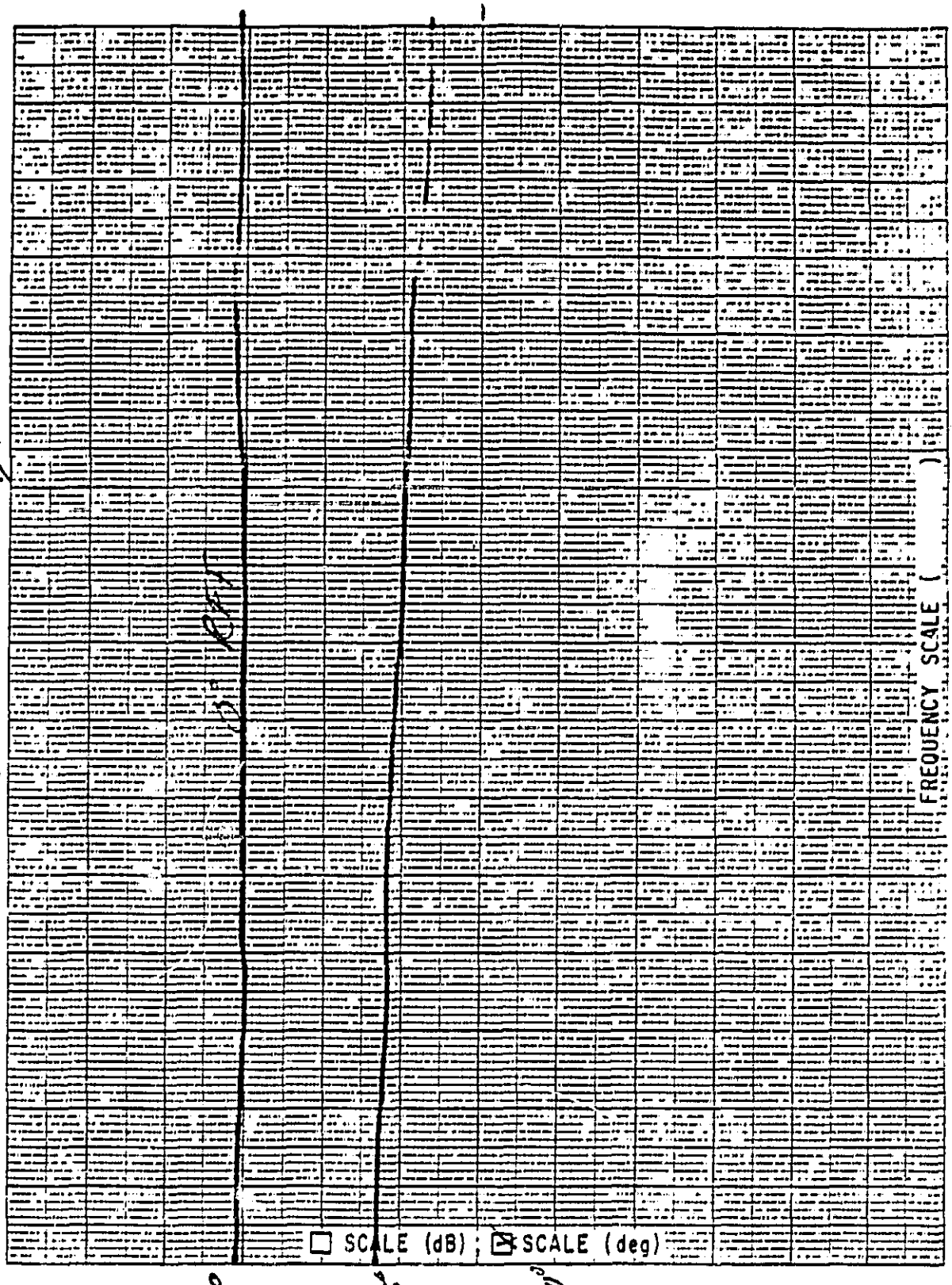


Figure 15

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Ball Strip 12 ANTENNAS

PROJECT NO. _____ PROGRAM _____
PART NO. _____ MODEL NO. _____ SERIAL NO. _____
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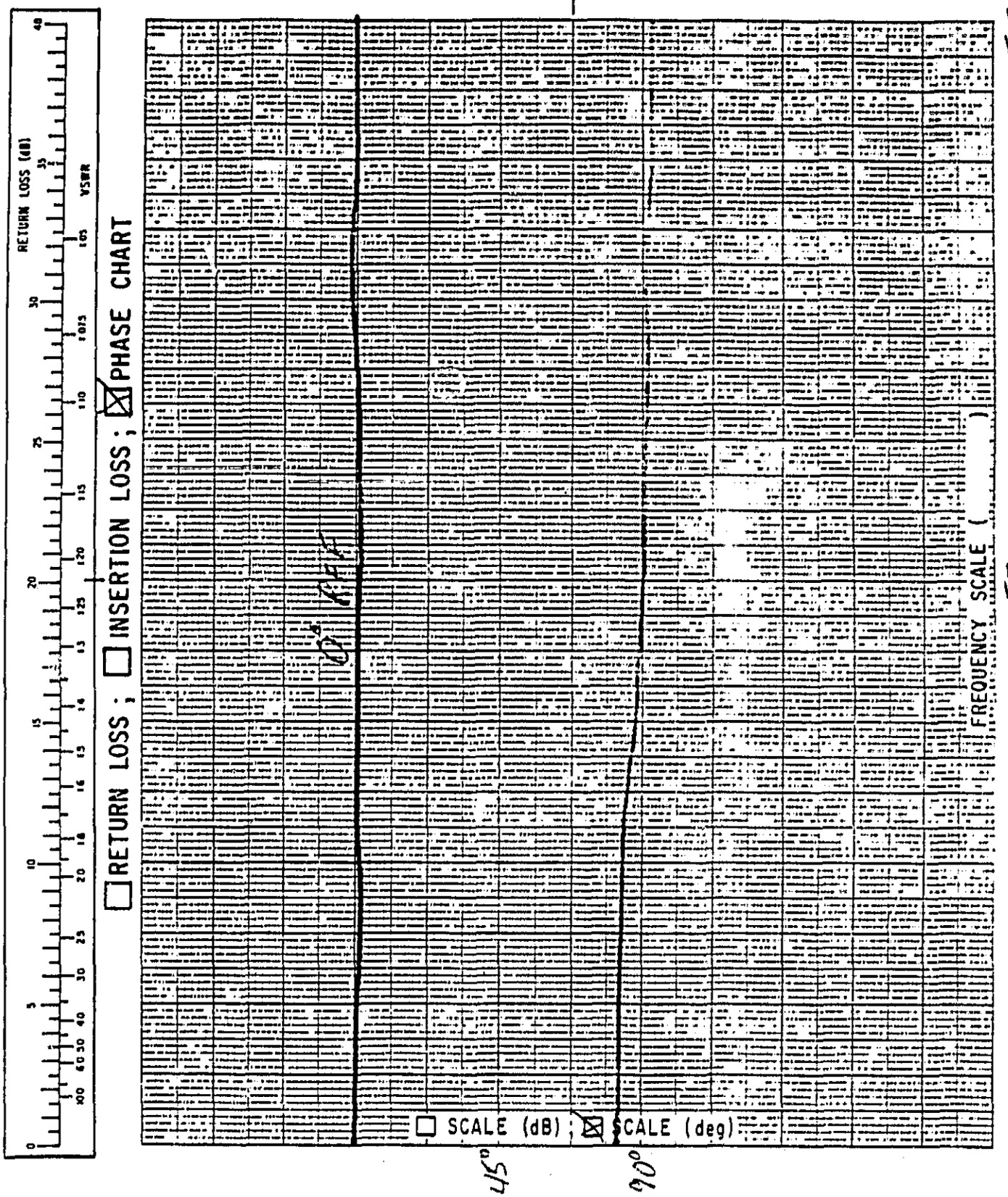
FREQUENCY RANGE _____ SHEET ____ OF ____



5.5
5.3
Figure 16
5.1

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REMARKS

Bi-stripline ANTENNAS

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PART NO. _____ MODEL NO. _____ SERIAL NO. _____
TEST TYPE: ☐ DEVELOPMENT ☐ PRE ☐ FINAL
FREQUENCY RANGE _____ SHEET ____ OF ____

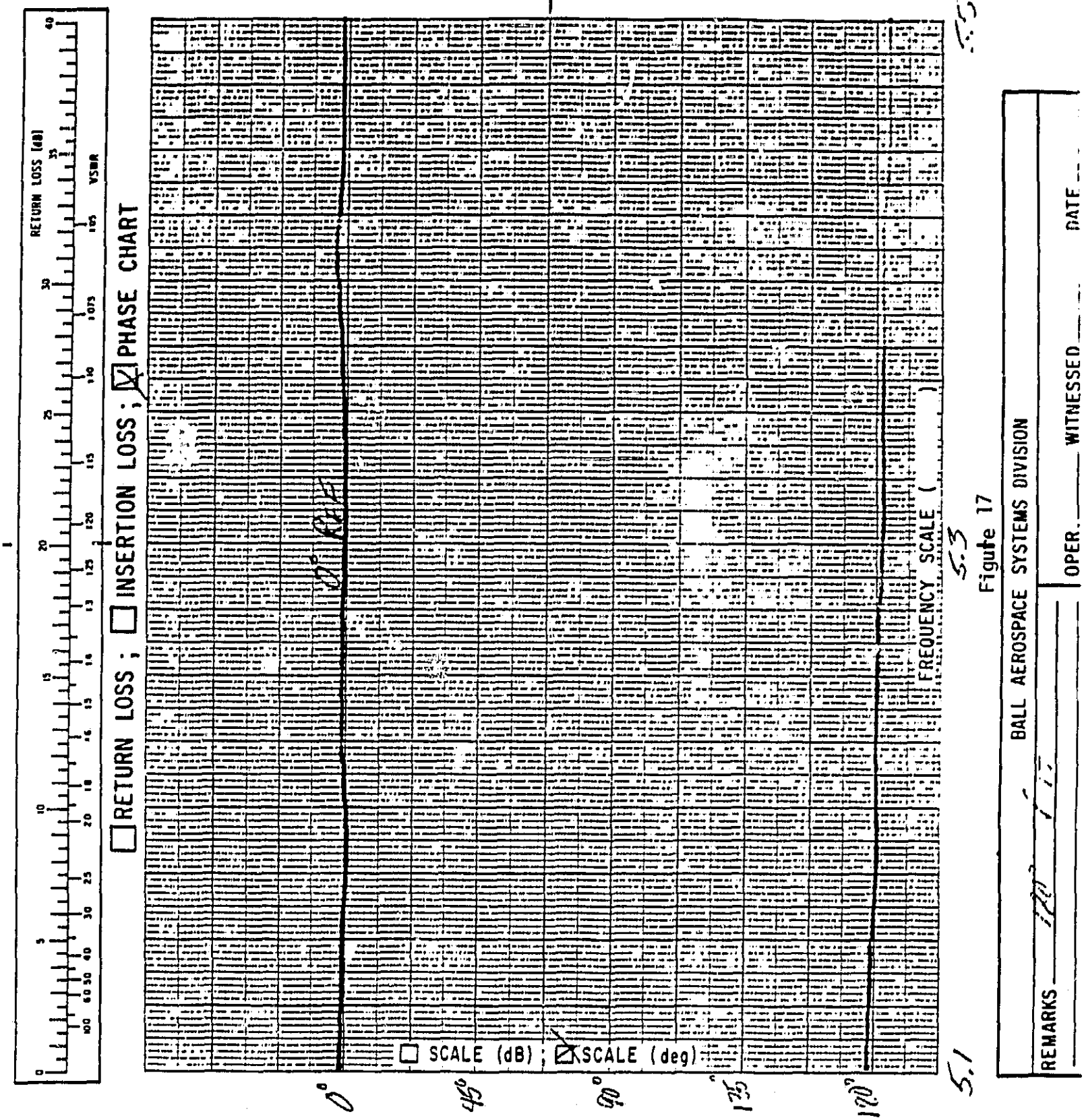

Figure 17

BALL AEROSPACE SYSTEMS DIVISION

OPER. _____ WITNESSED _____ DATE _____

REMARKS _____

VII. INTEGRATION

In this section we will discuss the integrated antenna/power divider performance. Input impedance and isolation measurements were performed; these test plots are shown in Figures 18 and 19 respectively. The VSWR for both polarizations is within 1.9:1 for the band 5.26 to 5.35 GHz. Port-to-Port isolation is below -50 dB for the same frequency band.

Photographs of the array, power divider, and phase shifter are shown in Figures 20-22 respectively. Also, the circuit layout for the combination of the phase shifter and power divider is shown in Figure 23.

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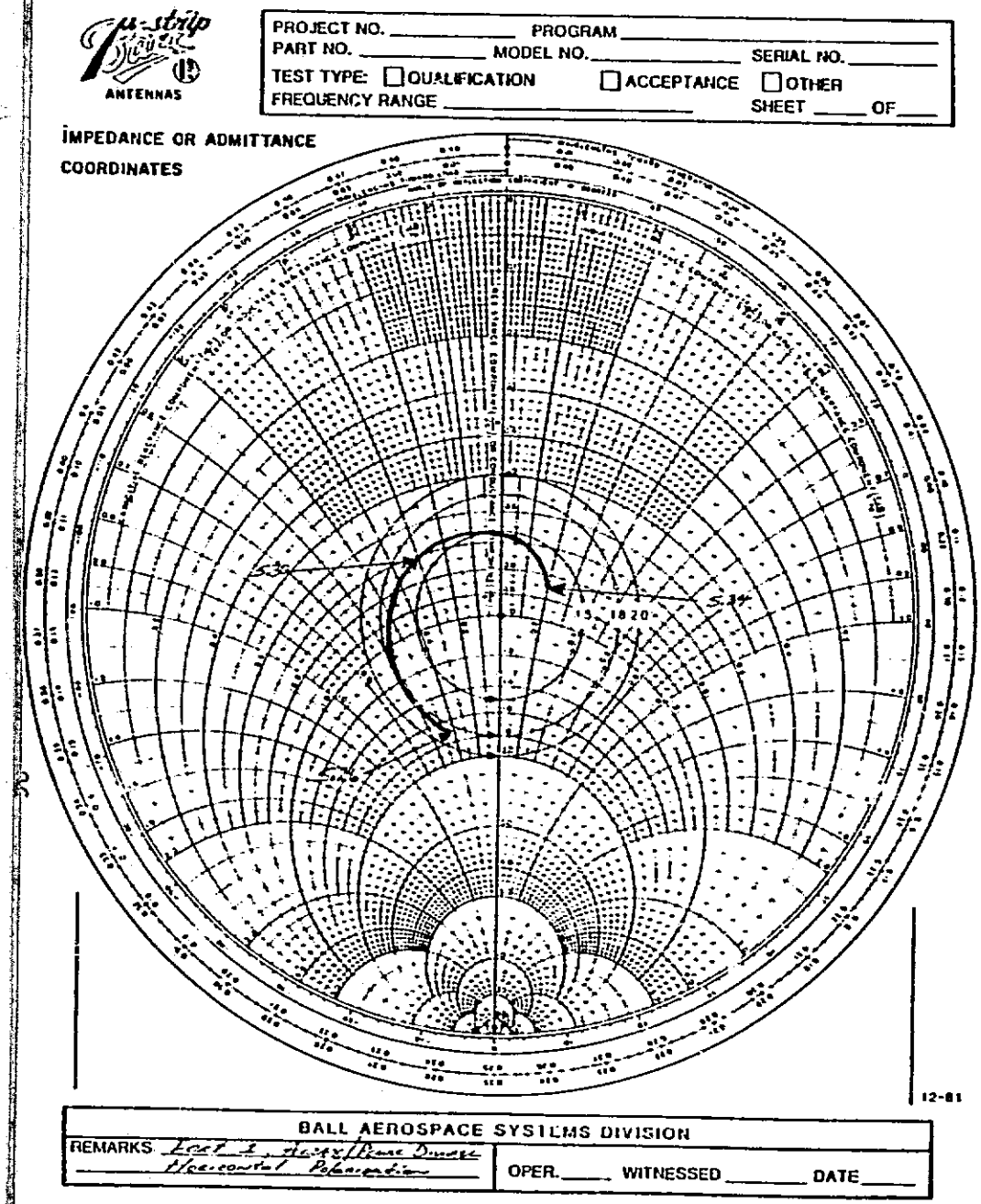

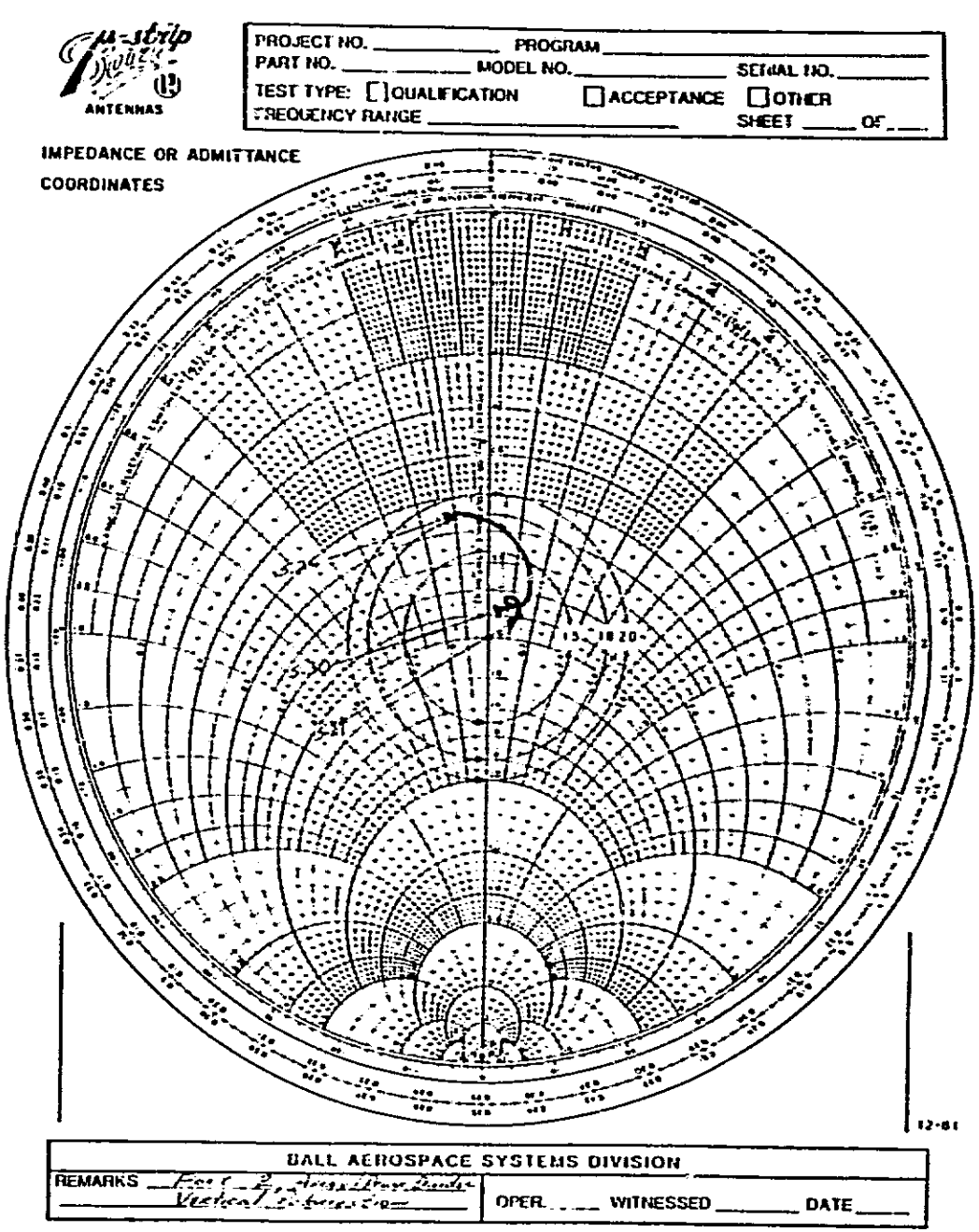

Figure 18

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Ball Stripline Patch ANTENNAS

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FREQUENCY RANGE 5200 - 5400 MHz SHEET ____ OF ____

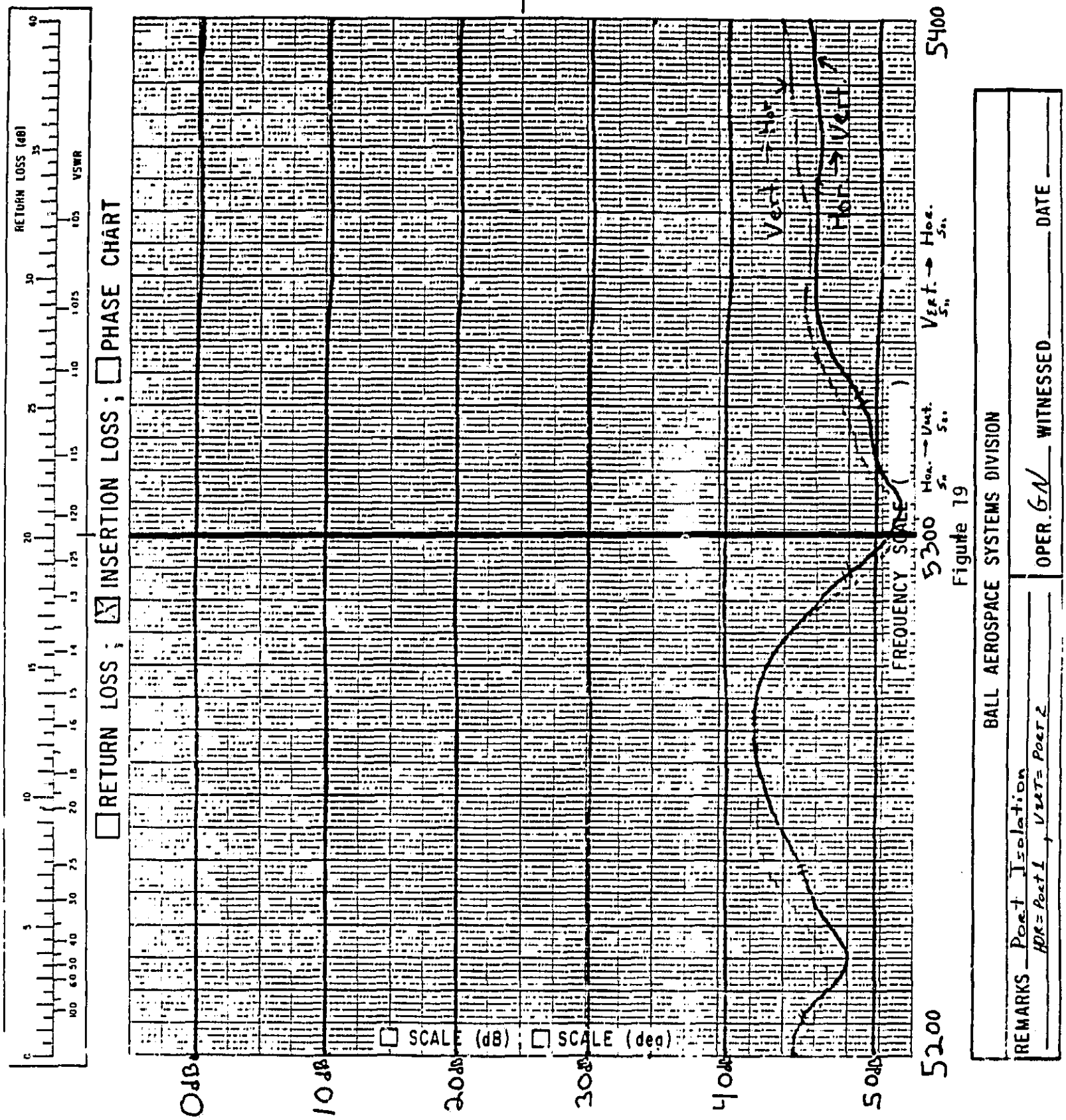

Figure 19

BALL AEROSPACE SYSTEMS DIVISION

REMARKS Port Isolation
HOR = Port 1, VERT = Port 2

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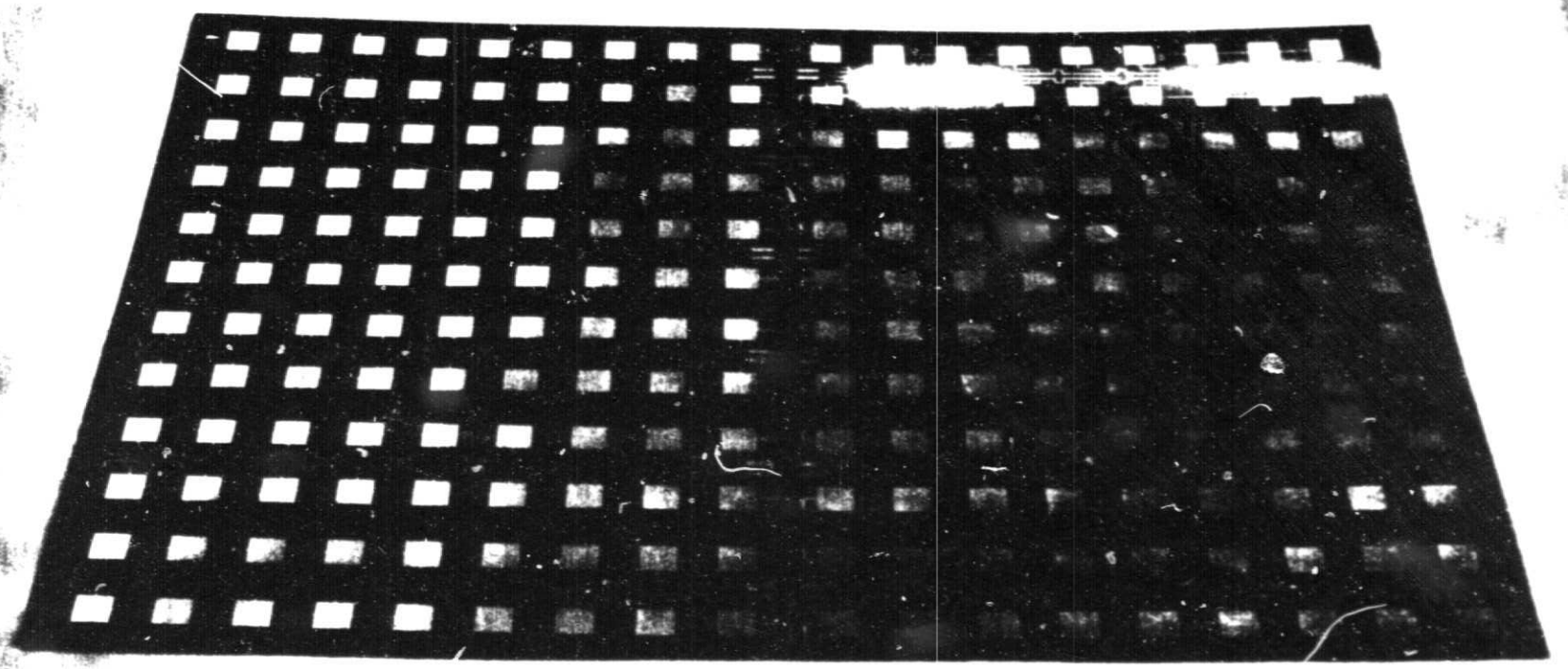

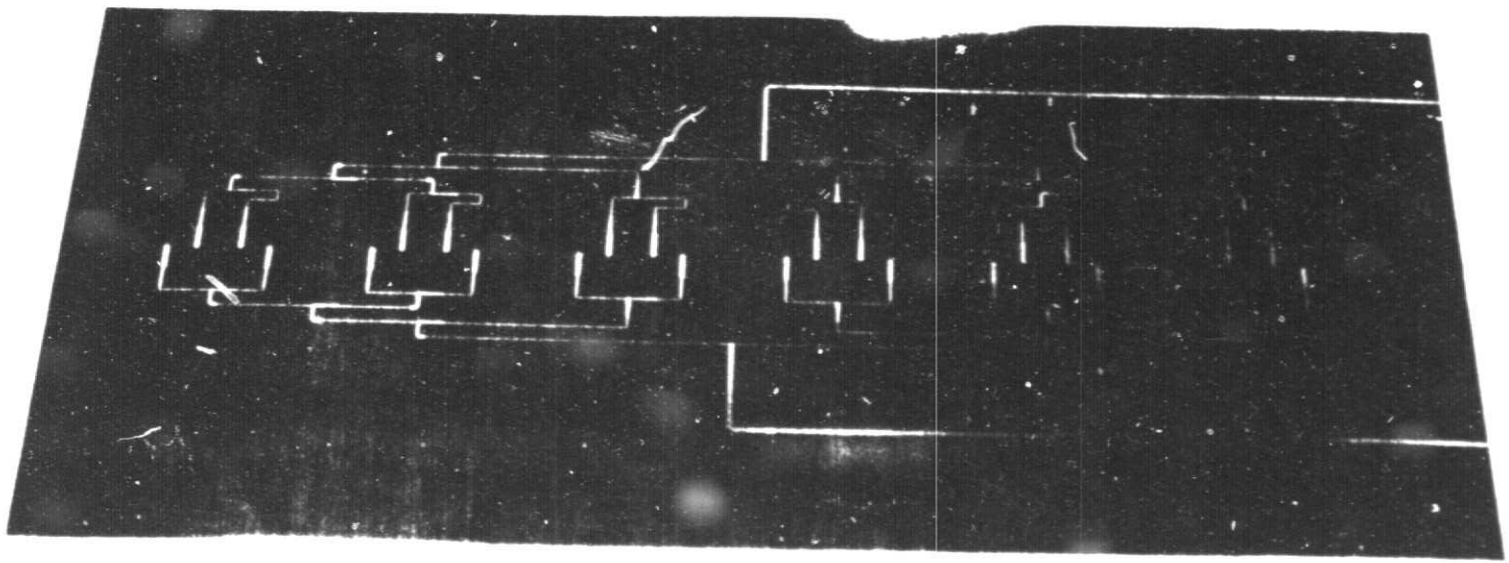

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BLACK AND WHITE PHOTOGRAPH

Figure 22

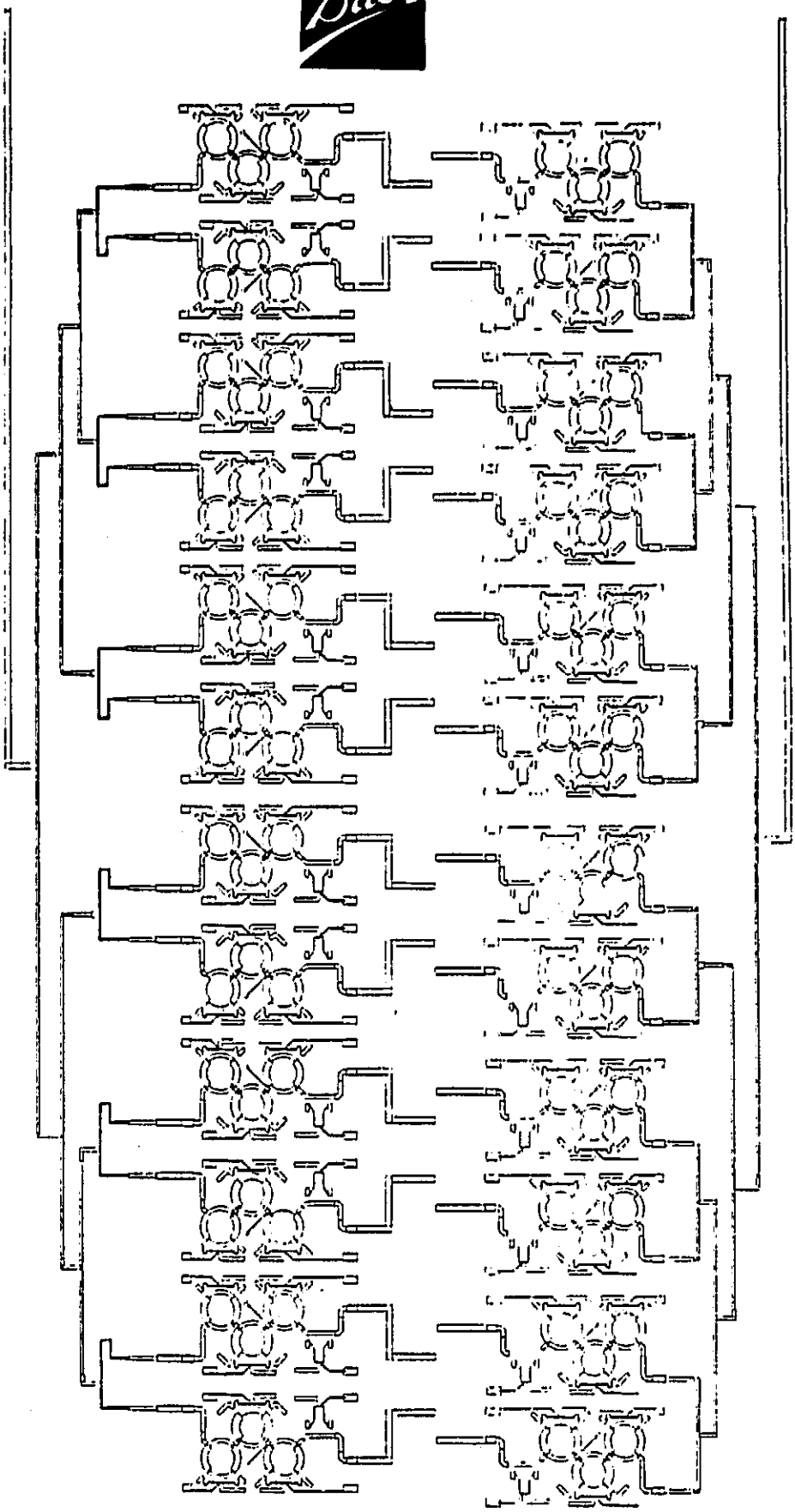

Figure 23

VII. CONCLUSION

The antenna/power divider system and phase shifter performed quite satisfactorily. A few parameters, cross polarization and port-to-port isolation for example, were exceptional. A bandwidth of 75 MHz to 100 MHz can be adequately achieved with this type of antenna design. Presently, the total measured losses in the 4-bit phase shifter, using hermetically sealed PIN diodes, is on the order of 2 dB. However, we expect this loss to drop to 1.5 dB with some judicious design of the various bits in the phase shifter.

Currently, we are preparing to integrate transmit/receive (T/R) amplifiers into the phase shifter and power divider board. The fabrication and testing of this active antenna array should provide some understanding into their implementation in future spaceborne radar and communication systems.

Active arrays, in general, can deliver high power without associated feedline power breakdown problems. A distributed amplification system achieves better sensitivities (in receiving weak signal levels) than does a centralized system which has higher losses as well as higher effective noise temperatures. In the event of modular failure, active array performance degrades gracefully. Hardware implementation, however, is generally more complex.