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ABSTRACT

Recent advances in silicon solar cell processing have led to attainment of conversion efficiency approaching 20%. In this paper we review the basic cell design investigated at Spire and indicate features of greatest importance to achievement of 20% efficiency. We discuss in detail experiments to separately optimize high efficiency design features in test structures and discuss the integration of these features in a high efficiency cell. In this work, ion implantation has been used to achieve optimal concentrations of emitter dopant and junction depth. The optimization reflects the trade-off between high sheet conductivity, necessary for high fill factor, and heavy doping effects, which must be minimized for high open circuit voltage. A second important aspect of our design experiments is the development of a passivation process to minimize front surface recombination velocity. We indicate the manner in which a thin SiO_2 layer may be used for this purpose, without increasing reflection losses, if the antireflection coating is properly designed. We also present details of processing intended to reduce recombination at the contact/Si interface. Data on cell performance (including CZ and ribbon) and analysis of loss mechanisms are presented. We conclude with a discussion of the ultimate performance that may be achievable with this type of processing.

INTRODUCTION

The attainment of 20% conversion efficiency in flat-plate Si solar cells is presently the goal of the National Photovoltaics Program (1). To this end, we have been conducting research on the ion implanted Si cell. This work recently led to the achievement of conversion efficiency of 18%, and efficiency approaching 20% appears possible in the near future (2,3). In this paper, we review the results to date with emphasis on cell processing aspects, and we indicate the device design and cell processing techniques that appear necessary for achievement of the national goal.

The high efficiency cell process to be discussed is based on the use of high lifetime float zone Si. This material was selected owing to superior minority carrier lifetime over a broad resistivity range. One promising alternative is the use of Czochralski silicon, which will be feasible if modest diffusion length (~200μm) can be achieved in low resistivity wafers. Many aspects of the techniques to be presented are applicable to polycrystalline material as well, with conversion efficiency commensurate with the diffusion length in such material. We will report in this paper on the application of some of our processing techniques to sheet materials.

The junction formation technique to be discussed is based on ion implantation and thermal annealing. As was shown in a recent paper, the ion implantation process allows one to reproducibily adjust the emitter dopant concentration to near optimal values (4). In addition, the thermal anneal process can provide a passivating surface oxide if oxygen is admitted to the gas stream. The versatility of this junction formation technique has made possible rapid progress in emitter design.

In order to gain a better understanding of the loss mechanisms operating in our developmental cells, we have used a solar cell modelling code developed at Brown University by one of the authors (5). The results of the modelling will be provided where appropriate throughout this discussion. The one-dimensional model is described in detail in reference 5, and will only briefly be described here.

The modelling code evaluates the analytic solution of the inhomogeneous diffusion equation which we assume governs minority carrier transport in the quasi-neutral emitter and base of the solar cell. The quasi-neutral regions are assumed to terminate at the space-charge region on one side, and at a minority carrier mirror (characterized by a surface recombination velocity) at the other side. The analytic solution for the sum of the diffusion current and a space-charge region light-generated current is integrated over the solar spectrum to obtain short circuit current (J_{SC}). Open circuit voltage (V_{OC}) and efficiency. In addition, provisions have been made for front surface reflection loss, shadow loss, reflection from a back surface mirror, and light-trapping (6).

The equilibrium minority carrier concentrations are calculated using Fermi statistics. The rigid band approximation is used to calculate the effects of band gap narrowing. Position dependence of doping, mobility, and lifetime are not included in this model and this limits the agreement between calculated and measured spectral response for short wavelengths. Nevertheless, we are able to achieve reasonable agreement with most other measurement data.

In the next section, we discuss the selection and characterization of the silicon used in our work. We follow this with a discussion of emitter design and fabrication, including the importance of surface passivation and ohmic contact design. The results of this work indicate the significance of high base minority carrier lifetime, and we report on new results from an investigation of the effects of cell processing on diffusion length. We conclude with a description of the cell design that we are pursuing for attainment of 20% conversion efficiency.

SELECTION OF SILICON

It is well known that fabrication of superior silicon cells based on conventional p/n junction designs requires silicon of the highest minority carrier lifetime (7). Development of a particular design and process sequence requires knowledge of the post-process lifetime; such data are of particular importance to the selection of base resistivity. For this reason, we investigated post-process lifetime of a variety of float zone slices.

Back surface field (BSF) cells were fabricated using a simple baseline process (2) from float zone slices obtained from Wacker and elsewhere. No antireflection (AR) coatings were used. Figure 1 replicates diffusion length data obtained by the method of Stokes and Chu (9) from quantum efficiency (QE) measurements of completed cells. The triangular data points indicate Wacker WASO-S slices. The square data points are Czochralski slices. Cell data is indicated in Table 1. It can be seen that AM1 conversion efficiency is about 10-11% for the WASO-S material of each resistivity. In order to determine how efficiency might be improved, we examined loss mechanisms in detail. In this way we were able to make significant improvements to the baseline process.

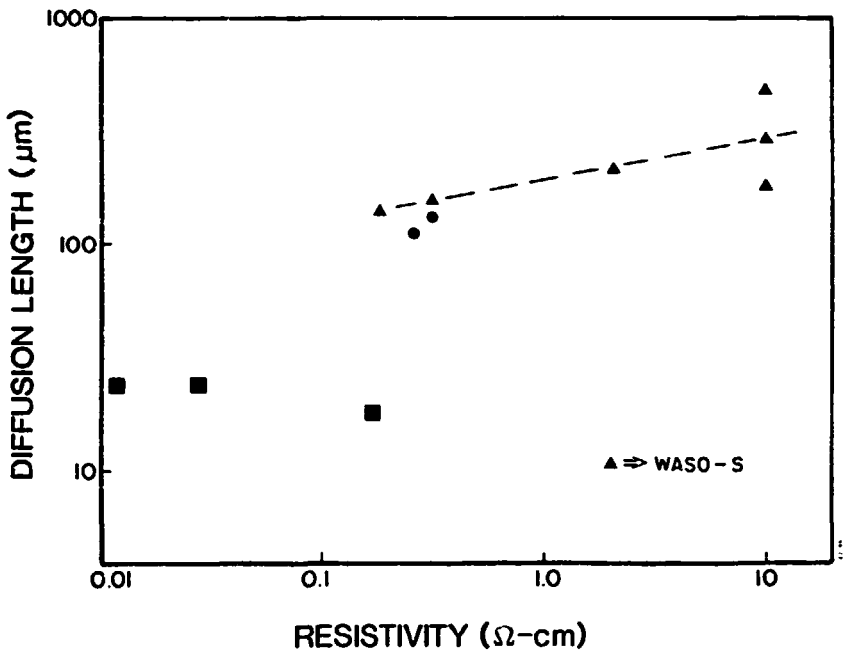

FIGURE 1. DIFFUSION LENGTH AS A FUNCTION OF RESISTIVITY. The dotted line indicates the functional dependence of L_D upon N_A that is assumed in our theoretical calculations.

TABLE I. CELL PERFORMANCE DATA FOR Si EVALUATION EXPERIMENT

GROUP	GRADE	RES. (Ωcm)	L_D (μm)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	EFF (%)
A	CZ	0.17	18	585 (003)	18.5 (0.6)	77.7 (2.7)	8.4 (0.5)
B	FZ	0.26	109	598 001)	22.3 (0.1)	79.0 (0.7)	'0.5 (0.1)
C	WASO-S (FZ)	0.18	139	597 (002)	22.3 (0.1)	77.3 (1.4)	10.4 (0.2)
D	WASO-S (FZ)	0.33	154	599 (001)	22.8 (0.1)	78.2 (1.0)	10.7 (0.1)
E	WASO-S (FZ)	2.1	212	583 (001)	23.4 (0.1)	78.9 (0.3)	10.8 (0.1)
F	WASO-S (FZ)	10	462	571 (001)	24.4 (0.1)	77.4 (0.3)	10.8 (0.1)
G	WASO-S (FZ)	10	227	563 (004)	24.1 (0.2)	77.1 (0.4)	10.5 (0.2)
H	FZ	0.32	129	597 (001)	22.8 (0.1)	78.9 (0.5)	10.7 (0.1)
I	CZ	0.027	—	530 (036)	12.0 (0.1)	54.6 (16.8)	3.8 (0.7)
J	CZ	0.012	—	364 (079)	7.6 (.02)	53.2 (1.8)	1.5 (0.4)

NOTES: Area = 4 cm^2, T = 28°C, L_D derived from quantum efficiency curves (9). Standard deviation shown in parenthesis.

Careful inspection of Table 1 indicates a large variation in fill factor (FF) for lower resistivities; this variation increases with decreasing resistivity. An examination of the dark I-V curves for representative cells, shown in Figure 2, indicates that leakage current increases as resistivity decrease.. Through experimentation, we determined that this leakage current arises at the edges of the solar cells, which in our process are cut from the original wafers with a diamond wheel dicing saw. Etching of the edges to remove the saw damage removes this leakage path but also removes some active junction area. The deleterious effects on J_{SC} that edge etching causes can be minimized by either use of mesa etching defined by photolithography, or by using an ion implantation mask similarly defined so as to restrict the junction from kerf areas. Both methods were found to reduce the leakage current to negligible levels. For large-area cells in which edge leakage current is small compared to the diode forward current, this type of processing will probably be unnecessary.

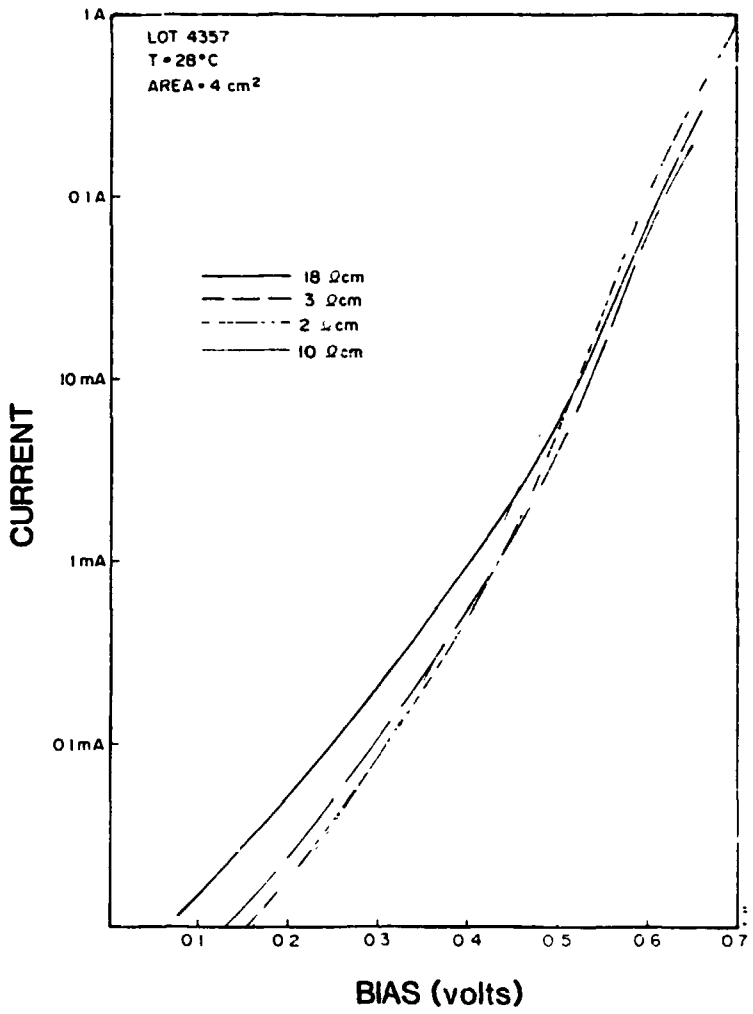

FIGURE 2. DARK I-V FOR REPRESENTATIVE CELLS OF VARIOUS RESISTIVITIES.

Figure 3 illustrates a comparison of measured external quantum efficiency (QE) data to the results of cell modelling, for a representative cell from group G in Table 1. Good qualitative agreement is obtained. Exact fitting was not attempted for two reasons: first, the absolute error in the QE data is not precisely known and second, the code cannot model position dependent parameters that are believed to be important in the emitter. Integration of the model QE data, however, yields good agreement with measured J_{SC}, and this is shown as a function of resistivity in Figure 4 with front surface recombination velocity as a parameter. In Figure 5 we present a comparison of the measured V_{OC} data to the calculated values with band gap narrowing (ΔEg) as a parameter. The modelling suggests that for low resistivity Si, band gap narrowing and surface recombination velocity dominate V_{OC}.

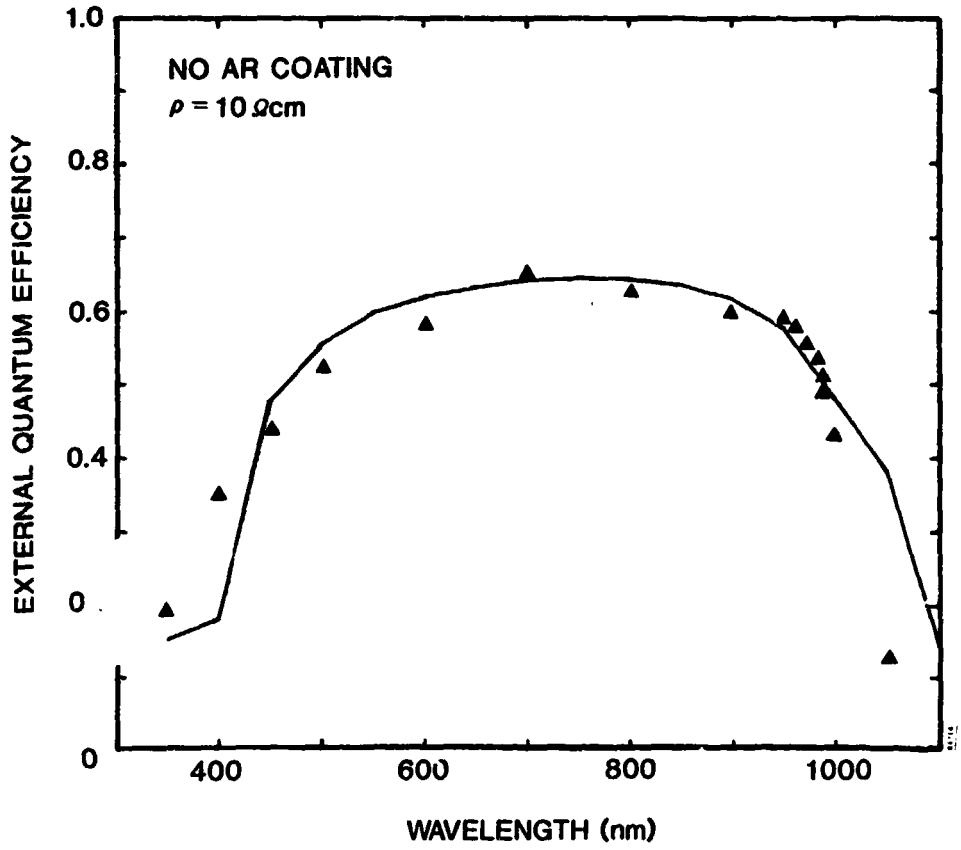

FIGURE 3. COMPARISON OF QUANTUM EFFICIENCY DATA TO MODEL CALCULATIONS FOR A CELL FROM GROUP G, TABLE 1.

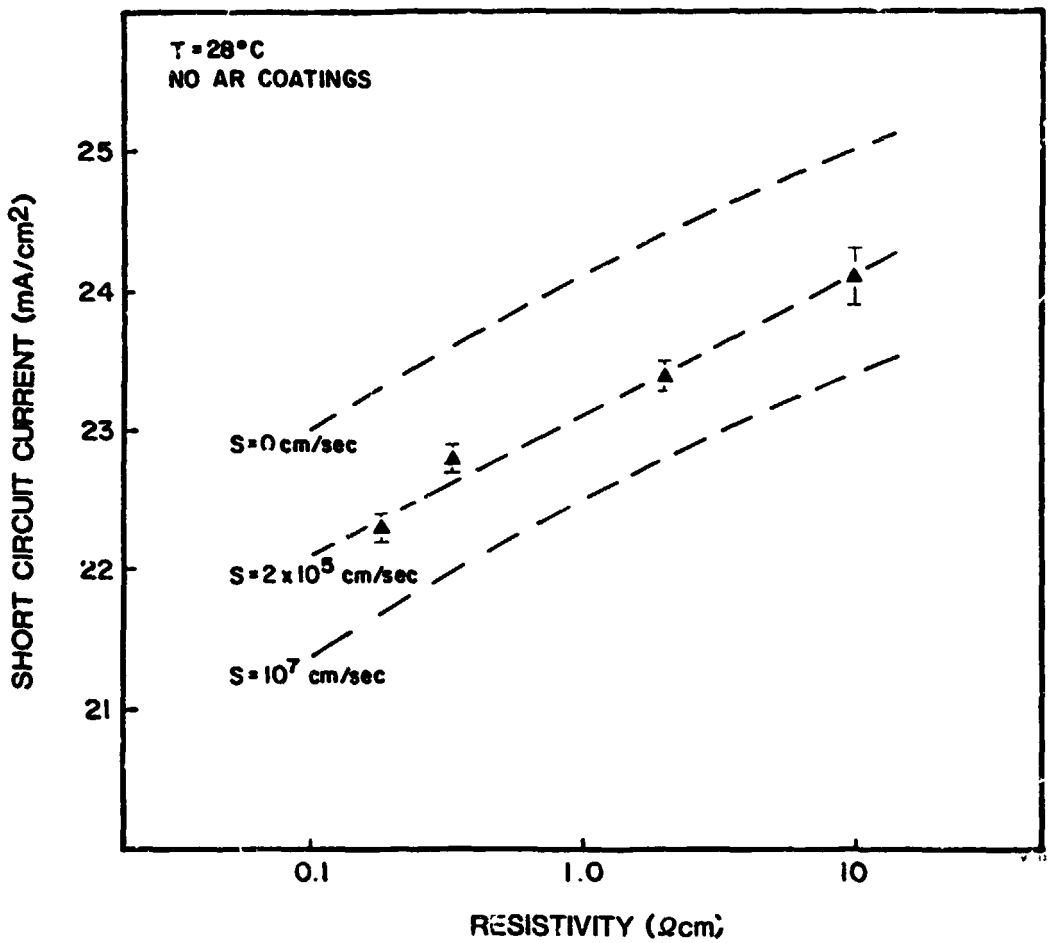

FIGURE 4. COMPARISON OF MEASURED AND CALCULATED J_{SC} AS A FUNCTION OF BASE ACCEPTOR CONCENTRATON.

We elected to work with cells of conventional thickness, even though calculations have shown that thin cells have theoretical advantages if minority carrier mirrors and light-trapping can be achieved (10). Our choice avoided the extraordinary care that handling thin (~50 μm) cells requires. The modelling of cells with conventional thickness (~400 μm) indicated that best efficiency would be obtained from low resistivity Si, provided that the emitter saturation current could be reduced, thus indicating the importance of pursuing research on emitter design.

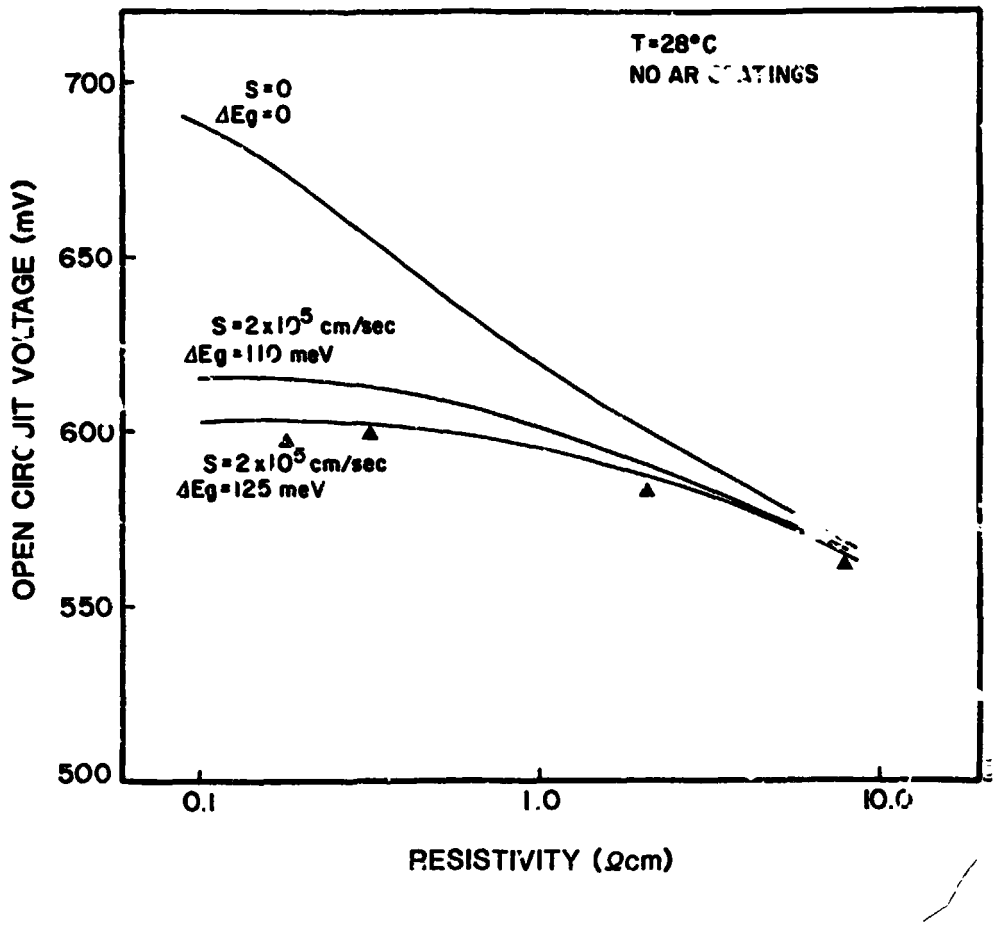

FIGURE 5. COMPARISON OF MEASURED V_{OC} DATA TO MODEL CALCULATIONS.

EMITTER EFFECTS

In a recent paper, we analyzed the importance of reduction of peak emitter dopant concentration, and it was shown that a very wide range of doping concentrations can be achieved with ion implantation (4). In Figure 6, we reproduce data that indicate that optimal QE at 350 nm is obtained for either arsenic or phosphorus emitter dopant concentrations of about $2x10^{19}$ cm^{-3}. V_{OC} appears to have a peak in this range as well, as shown in Figure 7. Unfortunately, the actual emitter concentration for which the maximum V_{OC} is obtained is obscured by low base diffusion length; i.e. in the neighborhood of the optimal donor concentration, the V_{OC} is base-limited. We will return to this point in a later section.

Figures 6 and 7 indicate that there is an advantage to passivating the front surface when shallow (~0.2μm) junctions are employed. Our experience indicates that as the junction is made deeper, the beneficial effects of passivation diminish; however, we have not conducted controlled experiments on this aspect.

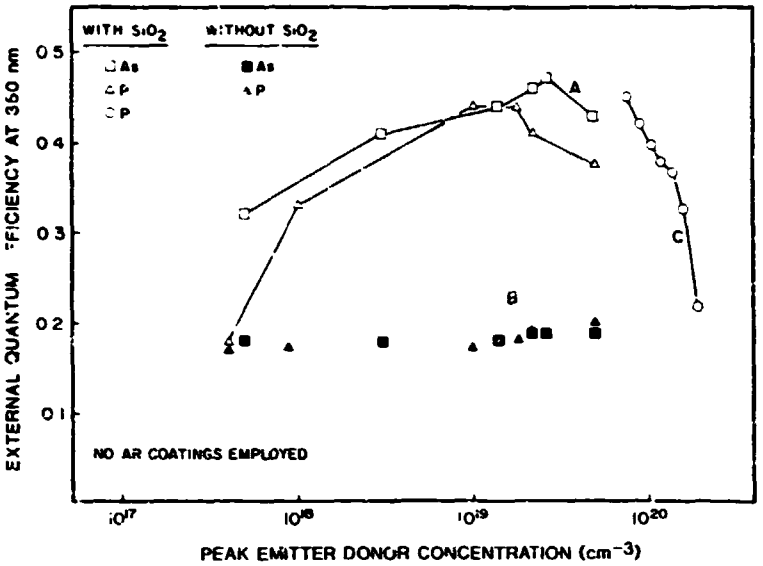

FIGURE 6. QUANTUM EFFICIENCY AT 350 nm. (A) Passivated As and P implanted emitters in 0.2 ohm-cm Si, (B) Non-passivated As and P implanted emitters in 0.2 ohm-cm Si, and (C) Passivated P implanted emitters in 0.3 ohm-cm Si.

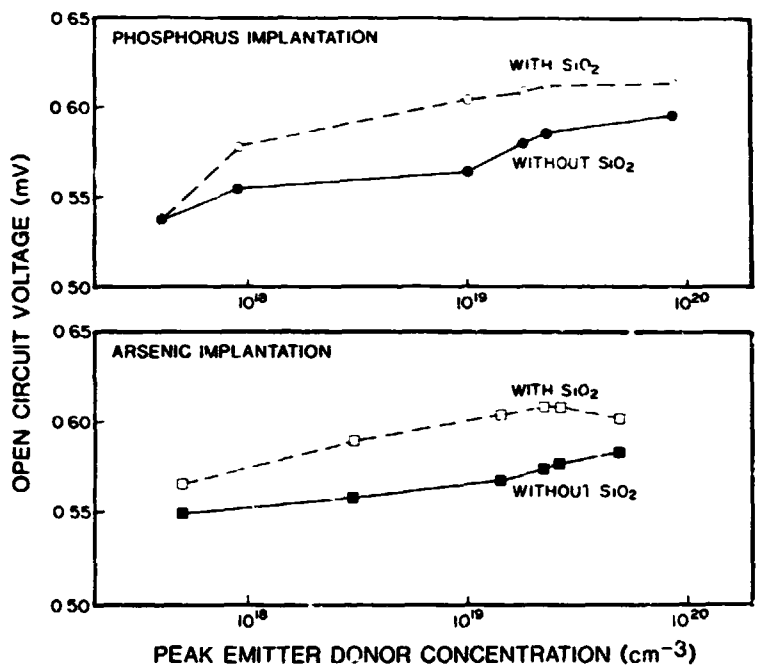

FIGURE 7. V_{OC} AS A FUNCTION OF N_D, WITH AND WITHOUT SiO_2 PASSIVATION.

Surface preparation can often affect the attributes of the ion-implanted emitter. In a later section, we describe the use of texture-etching to reduce reflectivity and enhance absorption. This etching, however, increases the front surface area, which necessitates a change in the ion implantation dose. To identify the optimal ion implantation dose for such an etched surface, we fabricated texture-etched solar cells with a range of doses. Details of this experiment are reported in reference 2. Figure 8 replicates the V_{oc} data for cells having SiO_2 passivation and for the same cells with SiO_2 removed. It can be seen from Figure 8 that the removal of the SiO_2 has a strong effect on V_{oc}.

There would seem to be three factors that control minority-carrier transport in the emitters of both the textured and polished devices: deleterious surface recombination, deleterious recombination and/or energy gap narrowing resulting from heavy doping effects, and advantageous minority-carrier reflection by the field resulting from the gradient of the doping. When SiO_2 surface passivation is present, the optimal ion implantation dose is approximately $5x10^{15}$ ions/cm^2 for a textured surface. Use of higher doses would seem to introduce deleterious heavy doping effects in the emitter which cause an increase in the saturation current. The existence of enhanced recombination in the near surface region is suggested by spectral response measurements that show that blue response decreases as the doping is increased (Figure 6). For lighter implantation doses, a loss in minority-carrier reflection occurs, owing to the reduction in the gradient of the doping near the surface. This reduction in doping perhaps allows an increase in carrier recombination at the front contact, and so V_{oc} decreases as the concentration is decreased. For the case in which the SiO_2 passivation is removed, the recombination at the surface exerts a strong influence on V_{oc}. In such a case, an increase in the peak dopant concentration that results from increase of dose increases the reflection of minority carriers, but the improvement is limited.

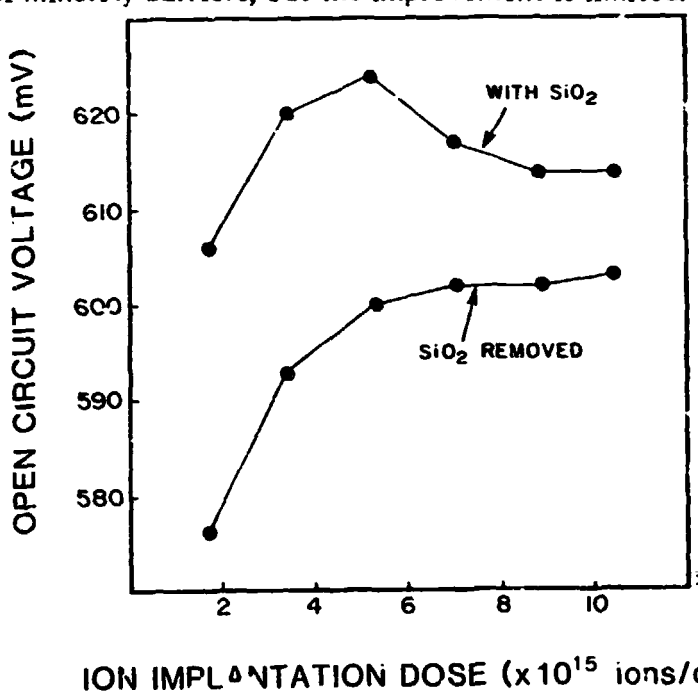

FIGURE 8. OPEN-CIRCUIT VOLTAGE AS A FUNCTION OF ION-IMPLANTATION DOSE FOR TEXTURE-ETCHED CELLS. The dose shown is the total dose measured by the implanter and is not corrected for the texture present on the target.

The optimization and theoretical analysis of our junction formation process applied to a textured surface requires knowledge of the resultant doping profile formed by the above implantation parameters on the {111} surfaces of the pyramids. For diffused junctions, one may perhaps assume that the junction profile replicates that which is formed on a standard {111} surface. It is not clear, however, that the depth distribution of implanted ions is equivalent to that obtained in an ordinary polished wafer, owing to scattering effects that may differ in the two cases. A further difference between diffusion and ion implantation is the increase in surface area mentioned above that obtains when texture is present. This increase requires a corresponding increase in ion dose.

For the above reasons, measurement of the dopant profile would be desirable. Unfortunately, the textured surface is not easily profiled using conventional techniques such as secondary ion mass spectroscopy, owing to obvious difficulties with depth calibration. For this reason, we conducted an experiment based upon ion implantation of a polished (111) wafer, suitably oriented with respect to the ion beam, to simulate the implantation of the {111} facets of the pyramids. This experiment is described in greater detail in reference 12.

A polished control (100) wafer was first implanted with $^{31}P_+$ using the conventional geometry. The implantation energy was 5 keV and the dose was 2.5×10^{15} ions/cm^2. An experimental (111) wafer was then implanted with $^{31}P_+$ at 5 keV to a dose of 5.2×10^{15} ions/cm^2, with the (111) surface oriented at an angle of 54.7° with respect to the ion beam to replicate the orientation of the facets of the textured surface. The specific dose, which includes an area correction related to the implantation angle, was 3×10^{15} ions/cm^2. Both wafers were then annealed in flowing dry N_2 using a three step process: 550°C-2hr., 850°C-15 min., 550°C-2hr. with ramping between steps. Dry oxygen was admitted to the gas stream during the 850°C step to grow the thin oxide necessary for passivation.

Spreading resistance analysis was obtained for both wafers, and is shown in Figure 9. The analysis indicates that the profiles are without detectable difference. This is not surprising, since the implantation parameters for polished and textured wafers were separately optimized for high cell performance. The value of the peak dopant concentration obtained in this experiment has been used in the modelling which follows in the next section.

To further refine our solar cell emitters, we have been investigating the role of recombination at the front ohmic contact. To this end, we have been experimenting with the reduction of ohmic contact area, while keeping the shadow loss constant, as has been done elsewhere (13). Figure 10 illustrates two methods of implementing this technique. In method A, the opening in the passivating oxide through which contact is made is reduced in width so that the opening is more narrow than the grid line. In method B, the openings are small separate squares. Both techniques require photolithography and alignment; however, one method of producing type A contacts would be to make the grid lines as narrow as the desired openings in the oxide. The width of the lines might then be increased to the desired width by electroplating, thus obviating alignment.

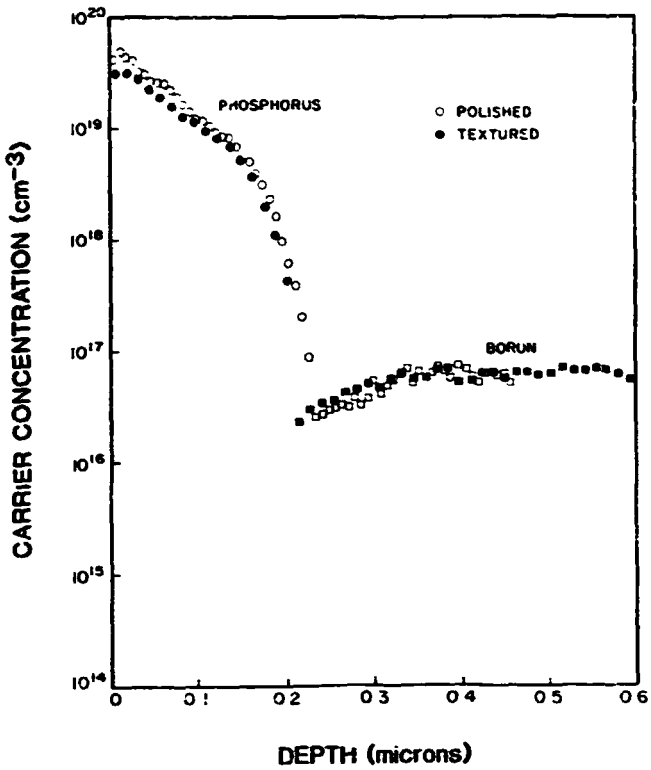

FIGURE 9. SPREADING RESISTANCE ANALYSIS OF A SIMULATED TEXTURED (111) WAFER AND A (100) CONTROL.

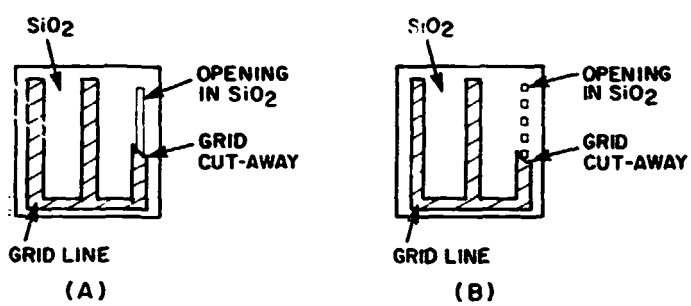

FIGURE 10. TWO METHODS OF REDUCING OHMIC CONTACT AREA.

Results with this type of processing are thus far inconclusive. In Figure 11 we replicate data from an experiment in which the ohmic contact area was varied as described above (4). Best results were achieved for reduced area, but the saturation current in these devices may arise mainly in the base, and so the optimal value of ohmic contact area may be obscurred. Further experiments are in progress and will be reported at a later time.

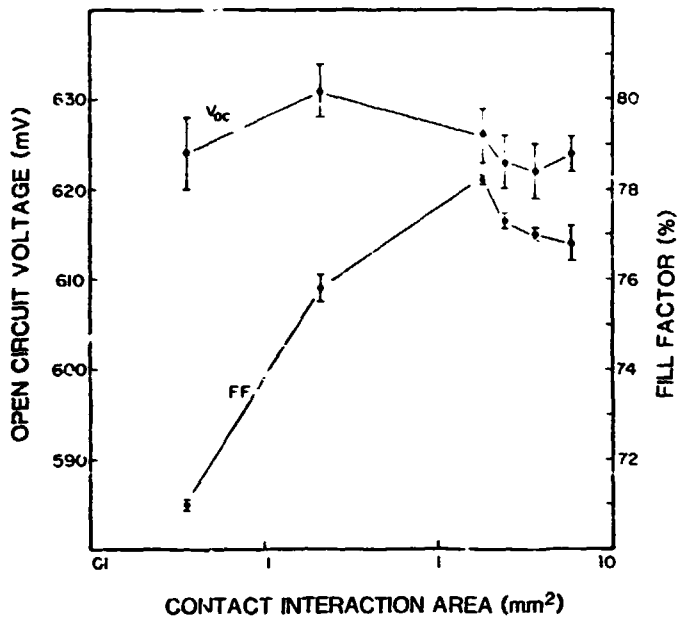

FIGURE 11. V_{OC} AND FF AS A FUNCTION OF OHMIC CONTACT AREA. (Base resistivity is 0.3 ohm-cm.)

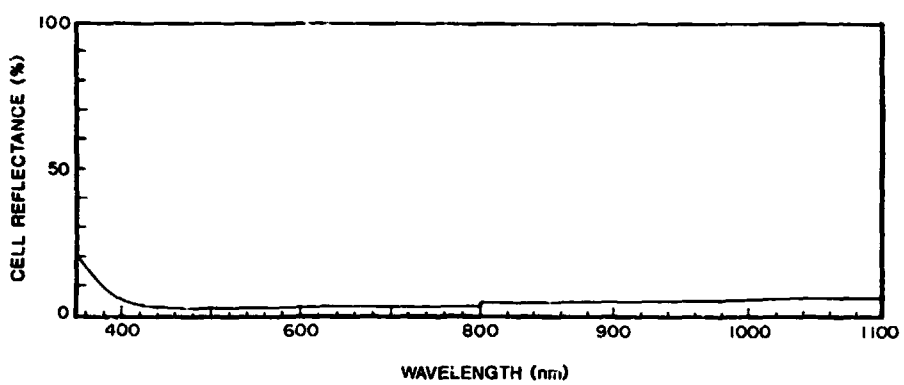

FIGURE 12. REFLECTION LOSS FOR A TEXTURED PASSIVATED SOLAR CELL.

Our results thus far on emitter design indicate the importance of both reduction of emitter dopant concentration and use of passivating oxide. This passivating oxide exerts a negligible influence on the reflection loss. To emphasize this point, we show in Figure 12 the measured reflectivity (courtesy of Dr. D. Arvizu, Sandia) from a textured solar cell. It can be seen that the reflection loss is indeed very small. The passivation can also be applied to sheet materials without severely affecting the AR coating. Recently we applied our emitter formation process to nonagon EFG ribbon. AM1 efficiency prior to AR coating was 9.7%. After evaporation of a single TiO_2 layer, efficiency increased to 13.2%, indicating a gain of 36%; higher gain would be possible with a more suitable AR coating (such as Ta_2O_5).

HIGH EFFICIENCY CELL DESIGN

Figure 13 illustrates the details of the solar cell structure yielding the highest efficiency to date. The texture-etched front surface is ion-implanted to form the emitter, as discussed in the previous section. The surface is provided with a thin layer of SiO_2 to reduce the front surface recombination velocity. An AR coating of Ta_2O_5 is applied on top of the SiO_2; the thickness of this layer is optimized to minimize the reflection resulting from the presence of the SiO_2. We have not reduced the ohmic contact area in this design.

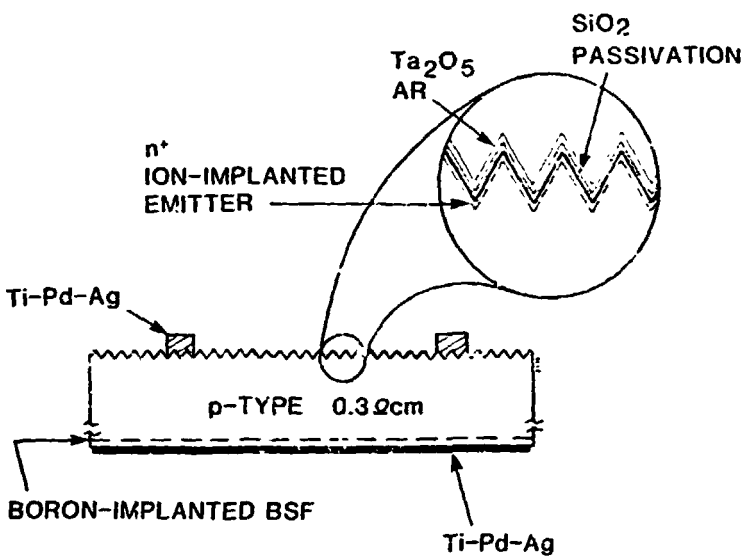

FIGURE 13. ILLUSTRATION OF THE SOLAR CELL STRUCTURE INVESTIGATED IN THIS WORK (not to scale).

Table 2 indicates the fabrication process for this cell design. The back surface is first implanted with $^{11}B^+$ and annealed to form a p^+ region. During the anneal, a thick surface oxide is grown to be used later for masking purposes. The resulting p^+ layer is about 1 m deep and has a peak concentration of 10^{20} cm^{-3}(14). Because the diffusion length is much less than the cell thickness, the p-p^+ junction is probably not effective as a back surface field (15); however, the p^+ region does aid the formation of a low resistance back contact.

TABLE 2. CELL FABRICATION PROCESS

Implant back	$^{11}B^+$ 50 keV, x 10^{15} ions/cm^2
Anneal/oxide	550°C -- 2 hrs. dry N_2 950°C -- 2 hrs. wet O_2
Pattern oxide	Acid etch
Texture	Hydroxide etch
Implant front	$^{31}P^+$ 5 keV, dose-variable
Anneal/oxidize	550°C -- 2 hrs. 850°C -- 15 min. 550°C -- 2 hrs.
Apply contacts	Evaporated Ti-Pd-Ag
Saw to size	2 cm x 2 cm
Plate contacts	Ag
Apply AR coating	Evaporated Ta_2O_5
Test	AM1, 100 mW/cm^2, 28°C

As discussed earlier, the surface oxide on the front was patterned to form an emitter ion implantation mask. The oxide mask defined the edges of the front phosphorus implant and so formed a planar emitter structure on each solar cell.

After patterning of the front oxide, the fronts of the wafers were texture-etched in a potassium hydroxide solution. Oxide on the back protected the boron implant from the etch. The fronts were then implanted with $^{31}P^+$ and annealed as described in the previous section. Evaporated Ti-Pd-Ag contacts were applied to both sides of the wafers and were patterned on the fronts using the photolithographic lift-off process. Electroplating was used to decrease the contact line resistance. The final step consisted of electron-beam evaporation of a Ta_2O_5 AR coating.

The resulting cells have been described in several recent publications (2, 16). Efficiency of up to 18% has been obtained, and the devices have been well characterized. We report here that an abbreviated form of the above process has been applied to Czochralski wafers supplied by Arco Solar Crystal Production. Efficiency of 16.8% was achieved (AM1, 28°C) and higher efficiency may be possible if the complete process is applied.

In Table 3, we summarize calculations of theoretical efficiency that indicate aspects of cell design that limit efficiency in the 18%-efficient FZ cells. The first entry in the table indicates the limit efficiency for a cell with width of 381 μm, made from 0.3 ohm-cm silicon. The only loss mechanism included in this calculation is Auger recombination (17); perfect light trapping and minority carrier mirrors are assumed (10). It is interesting that the upper limit to J_{SC} is 43.8 mA/cm^2, considerably higher than has been obtained in actual cells. Thus, considerable improvement is possible in J_{SC}. If neither light-trapping nor a back surface reflector (BSR) is present, the limit to J_{SC} is 42.2 mA/cm^2. Incorporation of actual reflection loss measured on a high efficiency cell (see Figure 12) indicates that J_{SC} can be as high as 40.6 mA/cm^2.

The diffusion length measured on our best cells is about 150 μm. Replacement of the Auger-limited diffusion length (~900μm) with the actual value reduces the J_{SC} to 36.9 mA/cm^2. Thus, a considerable amount of current is lost in our cells owing to bulk recombination. This loss can be overcome by increasing the diffusion length through more careful processing or by gettering. An alternative would comprise thinning the cell and adding a BSR.

The V_{OC} indicated for a 150μm diffusion length is 649 mV. The calculation of V_{OC} is extremely sensitive to the value of the effective masses, or in another formalism, to the value of the intrinsic concentration assumed. In our calculation, we used Fermi statistics with an effective density of states given by the average effective masses for electrons and holes (18). Owing to uncertainties in the effective masses, the effective density of states, and to heavy-doping effects in general, this calculation can be considered only as a rough estimate of the V_{OC}.

Inclusion of front surface recombination and bandgap narrowing reduces V_{OC} to values as low as 618 mV, if the data from reference 11 is used. By using a value for ΔE_g of 70 meV, we find good agreement with experiment. This may reflect the fact that our model assumes uniform doping, so 70 meV is perhaps an average value characterizing the heavily doped region near the surface and the lightly doped region beneath it. The shadow loss in our cells is approximately 3.5%; however, the reflection loss (already subtracted) includes reflection from the contact. Therefore, we only include a shadow loss of 2% in our calculation. Inclusion of the measured series resistance of 0.32 ohm-cm^2 (2) drops the FF to 81.6%. It can be seen that reasonable agreement with an experimental cell is attained.

The results in Table 3 reveal that a large amount of carriers are lost to bulk recombination. To quantify the effects of L_D on J_{SC}, we modelled the cell described above with L_D as a parameter. The result is shown in Figure 14. It can be seen that for the case of no BSR, increase in L_D to 200μm yields nearly 1mA/cm^2 gain. The addition of a BSR with reflectivity of 90% would increase J_{SC} to 36.6 mA/cm^2; increasing L_D to 200μm in that case would yield J_{SC} of over 37 mA/cm^2. In the next section we will describe experiments intended to raise L_D to over 200 μm.

TABLE 3. ANALYSIS OF LOSS MECHANISMS OF SPIRE'S HIGH EFFICIENCY SOLAR CELLS

	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	EFF (%)
Limit Efficiency of 0.3 Ωcm cell (Auger recomb. only)	713	43.8	84.7	26.5
No Light-Trapping	713	43.0	84.7	26.0
No BSR	712	42.2	84.7	25.5
Finite Reflection Loss	711	40.6	84.7	24.5
SRH Recombination (L_D=150μm)	649	36.9	83.6	20.0
Front Surface Recombination (S=2x10^4 cm/sec)	646	36.3	83.6	19.6
Bandgap Narrowing ΔEg				
(100 meV	618	36.3	83.0	18.6)
(80 meV	629	36.3	83.2	19.0)
70 meV	633	36.3	83.3	19.2
J_{oe} Penalty for Front Texture	625	36.3	83.3	18.9
Shadow Loss (2%)	624	35.6	83.3	18.5
Series R (0.32 ohm-cm^2)	624	35.6	81.6	18.1
Actual Data, Cell 22B	627	35.9	80.0	18.0

Notes: Calculations assume base width is 381 μm, T=28°C, Intensity = 100mW/cm^2, AM1.

In the event that efforts to raise L_D beyond 200 μm fail, one can consider thinning the base of the cell. A calculation of J_{SC} as a function of base width is shown in Figure 15, for the case of back surface reflectivity of 90%. For a cell with base width of 200μm, an increase in J_{SC} of about 0.5 mA/cm^2 is gained. If the cell is thinned and L_D is raised to 200 μm, J_{SC} of greater than 37 mA/cm^2 will be attained.

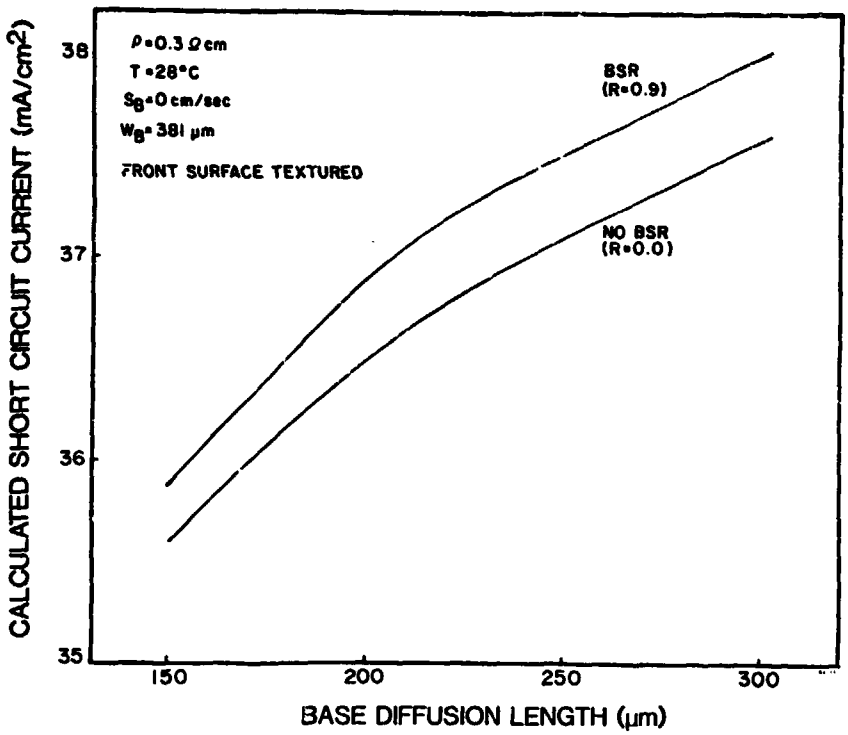

FIGURE 14. SHORT CIRCUIT CURRENT AS A FUNCTION OF DIFFUSION LENGTH.

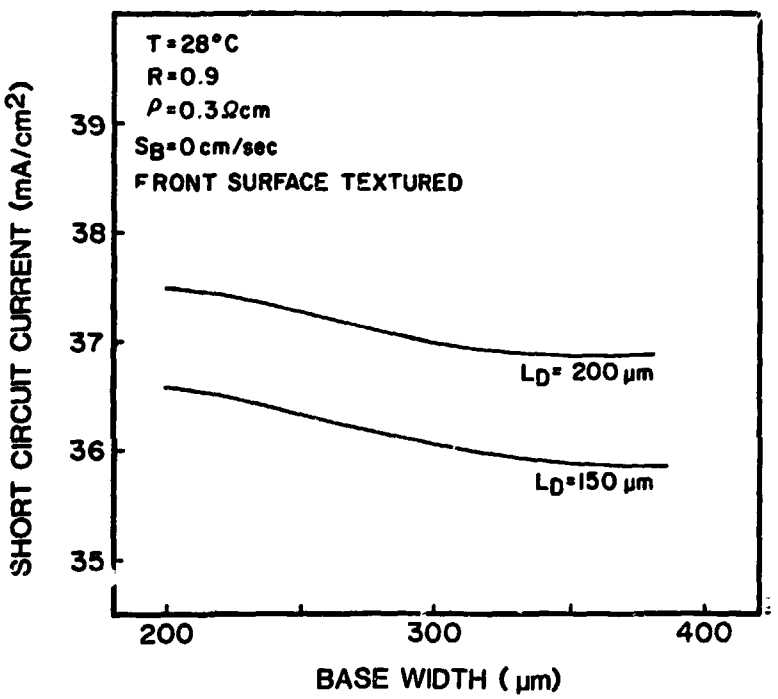

FIGURE 15. SHORT CIRCUIT CURRENT AS A FUNCTION OF CELL THICKNESS.

Improvements to L_D will also affect V_{OC}, although the gain is harder to quantify, owing to the large number of assumptions needed for calculation of V_{OC}. Nevertheless, V_{OC} as high as 660 mV is consistent with base resistivity of 0.3 ohm-cm and diffusion length of 200 μm, and experiments to reduce the ohmic contact area may reduce the emitter saturation current to negligible levels, thus enabling us to realize the base-limited V_{OC}. Similar results have already been demonstrated elsewhere (3).

EXPERIMENTS TO INCREASE J_{SC}

The preceding discussion has assumed that a BSR with reflectivity of 90% can be achieved. In fact we have developed such a BSR and in Figure 16 replicate experimental reflectance data from a polished AR-coated sample with Al evaporated on the back. The reflectivity of photons having energy less than the band gap, for which silicon is largely transparent, is greater than 90%. It is our assumption that the reflectivity of the BSR is as high for shorter wavelengths but the reflectance of photons with energy greater than the band gap has not been measured. However, the wavelengths that penetrate to the BSR are in general near the band edge, so the assumption is probably a good one.

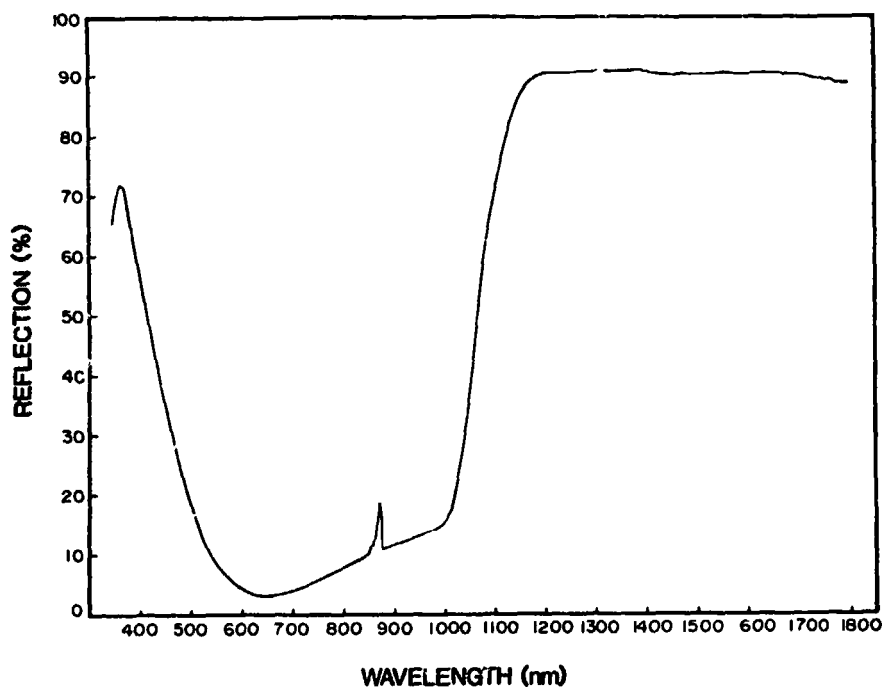

FIGURE 16. BSR REFLECTIVITY FOR AN AR-COATED CELL.

We have also examined the effect of our processing on cell lifetime. This was motivated by the anomalously low values of L_D that were obtained in a number of experiments, such as those reported in reference 4 and in earlier sections of this paper. In many of our emitter experiments, it was found that the base diffusion length had been degraded by the processing. We therefore devoted most of our attention to this problem. After a detailed examination of our furnace and gas lines, cleaning processes, annealing gases, and ramping, we identified our wet oxidation process to be a step that degrades lifetime. We have now eliminated wet oxidation from our sequence.

Recently we began experiments to increase diffusion length by gettering. The exact gettering processes that we are pursuing were taken from the literature and will be reported upon in a later publication. Owing to reservations about conducting an unusual process in our annealing tube, we used a sintering tube for the first gettering experiment. Since this tube is used for sintering solar cell contacts, it might be contaminated by Ti, Pd, or Ag. After a high temperature procedure in the sintering tube the wafers were fabricated into cells. It was found that L_D in control cells had degraded to about 100 μm, but L_D in the gettered cells increased to 170 μm. It is our conjecture that annealing in a clean tube may yield much higher values of L_D, and this is presently being tested.

CONCLUSIONS

Processing experiments have shown the importance of surface passivation, not only to V_{OC}, but also to J_{SC}. Analysis of loss mechanisms indicates that considerable improvement to J_{SC} may be obtained if diffusion length is increased. Improvement to V_{OC} is also possible by reducing emitter recombination. Many of these techniques can be applied with advantage to sheet materials. Certainly all of the above processing can be applied to CZ, with efficiency approaching that of FZ if gettering is successful in improving L_D. High efficiency can also be achieved with other sheet materials such as ribbon by using our junction formation and passivation techniques.

This work has indicated the manner in which the goal of 20% conversion efficiency may be achieved. Through process improvements such as gettering, thinning of the base, and addition of a BSR, J_{SC} of FZ cells may be increased to 38 mA/cm^2. Improvements to the emitter, including reduction of ohmic contact area, may increase V_{OC} to 660 mV. We have already achieved FF of greater than 0.8. If these features can be integrated in one cell, efficiency of 20% will be achieved. The application of this processing to present-day sheet Si will be an important step toward the DOE goal of 10% efficiency at \$90/m^2.

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CISZEK: Mark, do you have any thoughts on how you might be able to get reduced area contact to a wafer through an oxide?

SPITZER: I'll have to draw a slide of that. What's the Green secret? I don't have to draw that, I can explain it. What you do is you make a very fine-line grid. It would not be suitable for carrying the currents that you want, but it has the area of the opening in the oxide that I showed. And then you overplay it, you let the electroplating balloon the grid lines in their proper proportions; then you are left with grid lines that just touch a very small area along the surface. There is no alignment involved. The problem with that, I think, is the grid lines fall off; you have to be careful. I don't like it.

QUESTION: You can cross the lines, you make your slot and then cross your grid lines, you'll get a dot contact.

SPITZER: I was worried in doing that technique. I was worried about depositing the AR and having stripes on the wafer.

QUESTION: Mark, in your 18% efficient cell the surface dopant concentration was 3×10^{18}, or what?

SPITZER: In the 18% cell we think it was 3×10^{19}. So we used the same implant parameters for that experiment, where we measured the profile, as had been used on the 18% cells.

OLSON: Both in your work and Ajeet's you applied some of the things you learned to sheet materials, and I really think with some neat results. I think one interesting point to make is that your work on the good float-zone material is really a leading edge, and I think it is really important to have the high-efficiency work on this high-quality material lead the way. And it's clear that now you are beginning to apply it to work on low-cost sheet material.

SPITZER: I agree with that. And there is one other thing that we are working on, and that is to scale up the area of the cell. I think it also has to be applied to a fairly large-area device.

OLSON: It's there we are going to really learn what's really limiting the performance, and ultimately that might pay off.

SPITZER: I agree. I think we should stay with float-zone for a while.

JOHNSON: Mark, what was the sheet resistance of your emitter?

SPITZER: The baseline emitter that we started out was about 80 ohms per square and the one that is 3×10^{19} is about 200 ohms per square.

DAUD: Mark, could you tell me what the resistivity of the Czochralski silicon was that you got from ARCO?

SPITZER: Actually, I know what it is, but I don't have permission to disclose anything about the material, so you can ask one of the ARCO guys. But there is nothing crazy about it, its just ordinary stuff.