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MOSAIC INFRARED SENSOR FOR SPACE ASTRONOMY (MIRSSA)

PHASE I
INTERIM TECHNICAL REPORT

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SECTION 1
INTRODUCTION

This interim technical report summarizes the work performed on a NASA funded program to the Honeywell Electro-Optics Division for development of mosaic infrared detector/focal plane arrays for space astronomy. The technical monitor on this program is Dr. Nancy Boggios of Astrophysics Division at the NASA/headquarters. The principal investigator on this development program is Dr. Ashok Sood of the Honeywell Electro-Optics Division.

The objective of this program is to demonstrate the feasibility.

The Mosaic IR Sensor for Space Astronomy (MIRSSA) Program is a two year effort (Phase I & II) that is aimed at the development of PV HgCdTe detector arrays with the spectral response of up to 5 μm and silicon CCDs for low temperature applications.

Desired background-limited performance (BLIP) for space applications requires an extremely high R_oA product which can be achieved only by properly selecting the detector materials and the operating temperature. To determine these parameters, Honeywell has performed in Phase I a theoritical analysis and done measurements of HgCdTe PV detector arrays at various temperatures in both the SW and MW spectral bands. The results of the technical effort have demonstrated that high performance PV HgCdTe detectors can be fabricated for low temperature applications.

An additional requirement of Phase I specifies that Honeywell examine various CCD and other alternate device coupling schemes for low background space astronomy uses so as to assist in arriving at an optimal design for a CCD multiplexed readout.

In the past, Honeywell has characterized and analyzed CCDs for moderate to high temperature applications in the 2-5 μm band. Phase I of MIRSSA requires Honeywell to test these existing CCDs for low temperature space telescope applications.

SECTION 2
THEORETICAL TRADEOFFS AND CURRENT STATUS OF MW AND SW HgCdTe PV DETECTORS

Detection of IR radiation in the spectral bands of SW (1 to 3 μm) and MW (3 to 5 μm) for space astronomy poses a unique challenge to HgCdTe PV detector technology. This stems from the fact that the desired background-limited performance (BLIP) in the zodiacal background requires extremely high R_oA product ($10^{11} \sim 10^{12}$ Ω-cm^2) for the detector, which can be achieved only by properly selecting the detector materials and the operating temperature. To determine these parameters, we performed theoretical tradeoff analysis and measurements of existing HgCdTe PV detector arrays for both SW and MW spectral bands. It is concluded that HgCdTe PV detectors can meet the performance requirement for the space astronomy at the operating temperature of ~60 K for MW and ~100 K for SW detectors. This section presents the results of the analysis and the status of the HgCdTe detector performance. The last part of this section describes an ultra low-noise preamplifier which was developed under this program to measure the high impedance of the diodes.

2.1 Theoretical Tradeoffs for MW and SW Detectors

HgCdTe PV detectors operating at low temperatures (usually less than 120 K for MW or less than 200 K for SW detectors) are limited by noise originating dominantly from generation recombination (G-R) current in the diode space charge region. In the G-R dominant temperature range, the diode junction impedance at zero-bias is characterized by surface recombination velocity S_o at the surface of the space charge region formed around the junction periphery.*

Temperature dependence of the zero-bias impedance for a 4 mil x 4 mil detector (cutoff wavelength of 4.5 μm at 80 K) is calculated for three typical values of the surface recombination velocity as shown in Figure 2-1. Theoretical limit determined by the radioactive lifetime of the minority carrier in the base material is also shown in the figure as an upper limit. It can be observed from this figure that at 60 K the diode impedance becomes $10^{14} \sim 10^{16}$ Ω depending on the surface recombination velocity. Similar calculations were performed for a 4 mil x 4 mil SW detector (cutoff wavelength of 2.5 μm at 140 K) and the results are shown in Figure 2-2. Impedance of $10^{14} \sim 10^{16}$ Ω can be obtained at 100 K.

Another important consideration in designing the detector is the selection of cutoff wavelength. Dependence of the zero-bias impedance on the cutoff wavelength is examined at fixed temperatures (60 K for MW and 120 K for SW detectors) as shown in Figure 2-3 and Figure 2-4 for MW and SW detectors, respectively. If the cutoff wavelength is longer than 5 μm, the diffusion current becomes a significant contributor to the detector noise.

2.2 Current Status of HgCdTe PV Detector Performance

A number of existing MW and SW detectors were characterized in terms of the temperature dependence of R_o. Most of these arrays are 2 x 32 elements bilinear arrays with active area of 4.4 x 1.3 mil^2. The data will be discussed in the following subsections.

2.2.1 MW Arrays

Figure 2-5 shows temperature dependence of three typical elements from three arrays. The impedance reached the measure limit of ~10^{12} Ω at 80 K. The surface recombination velocity is

*NOTE: This is true for surface G-R dominant cases. If the G-R current originates and A the junction areas dominantly from the bulk space charge region, the characteristic parameter becomes depletion life time to which is equivalent to $(S_oP/A)^{-1}$ with P denoting the junction parameter.

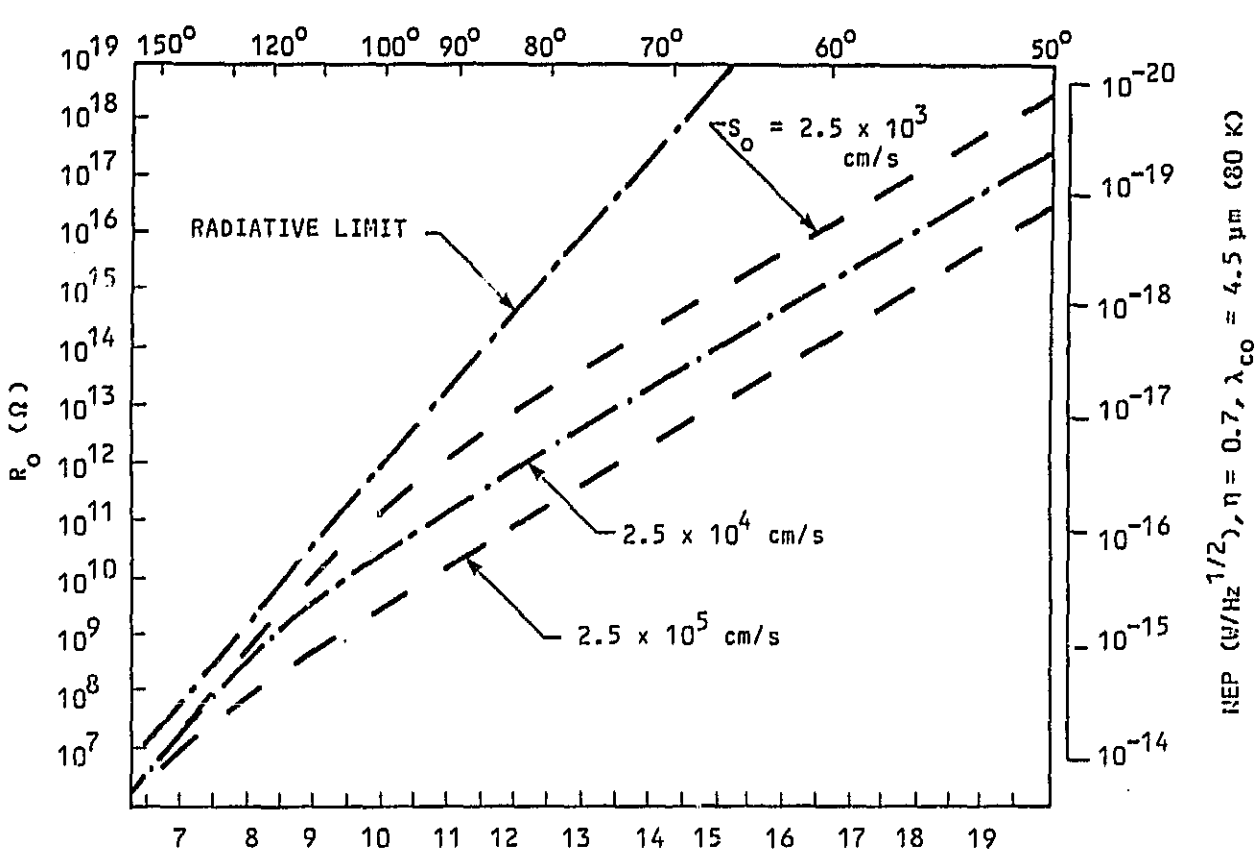


Figure 2-1. Temperature Dependence of R_o of a MW HgCdTe Photodiode Calculated for Various Surface Recombination Velocities. Relative Limit is the Theoretical Upper Limit of the Ro; Detector Area = 4 x 4 mil², Cutoff Wavelength = 4.5μ at 80K. The NEP Scale is Obtained From the R_oScale with 70% Quantum Efficiency and λ_{co} = 4.5 μm.

modeled as 1.5 x 10^4 cm/s for the typical diode of λ_{co} = 4.30μm. Figure 2-6 shows R_o versus cutoff wavelength measured at 80 K. The bars indicate maximum and minimum values of R_o in each array. The arrays with higher carrier concentration show a larger variation than the array with lower concentration. As indicated in the histogram of R_o in Figure 2-7, extremely uniform and high R_o values are achieved across the array by the lower concentration material. These observations are consistent with the characteristics of tunneling currents since the higher the carrier concentration, the greater the tunneling probability becomes due to narrower space charge width which in turn lowers the diode impedance.

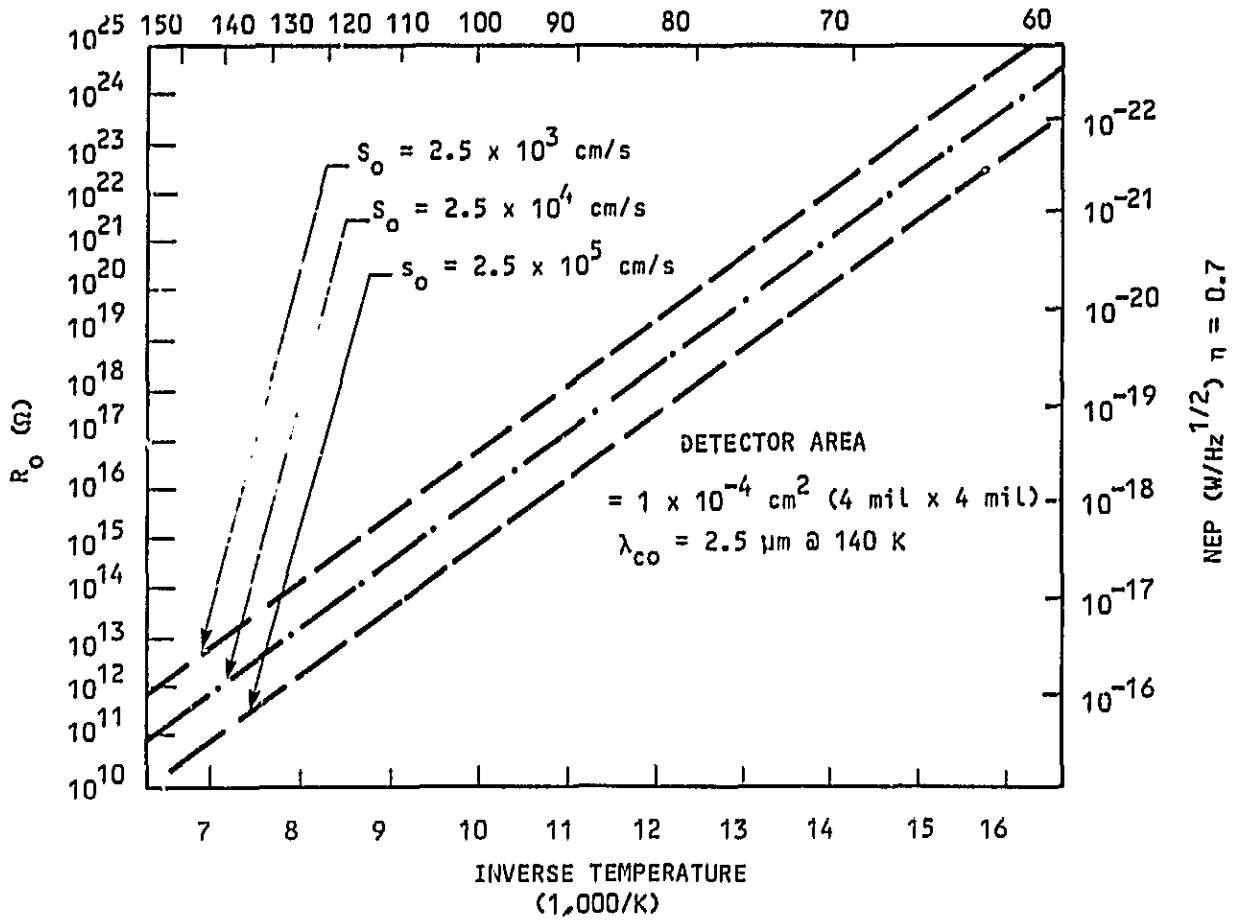


Figure 2-2. Temperature Dependence of R_o of a SW HgCdTe Photodiode Calculated for Various Surface recombination velocities; Detector Area = 4 x 4 mil^2, Cutoff Wavelength = 2.5μm at 140 K.

2.2.2 SW Arrays

Temperature dependance of typical three SW diodes is shown in Figure 2-8. Cutoff wavelength of these diodes at 200 K range from 2.37 μm to 2.44 μm. The R_o is limited by diffusion current above 200 K and below 170 K generation-recombination current becomes dominant limiting the diode impedance. Below 120 K the impedance measurement was impeded by the noise from preamplifier input circuit. The data at 140 K and 120 K were obtained with a newly built low-noise preamplifier, which is described in the next section.

2.3 Low-Noise Preamplifier Development for High Impedance Measurement.

To measure the high impedance of the diodes, an ultra low-noise preamplifier was built and used successfully to test both MW and SW diodes of up to 10^{14} Ω at low temperature. This new preamplifier has a feedback capacitor to measure the current, thereby eliminating the

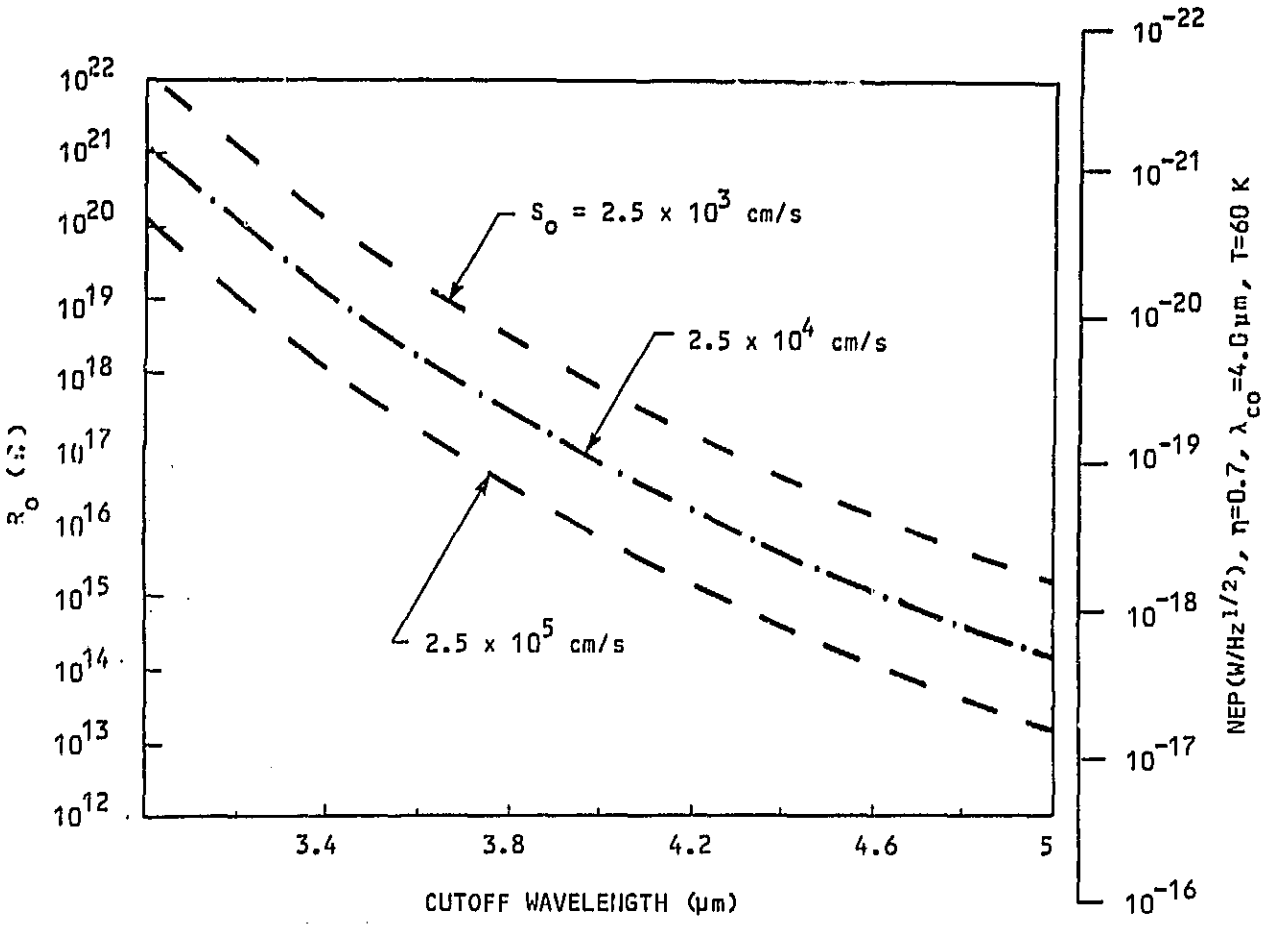


Figure 2-3. Calculated R_o vs Cutoff Wavelength at 60K for Three Values of Surface Recombination Velocity. The NEP Scale is a Conversion from the R_o Scale with Quantum Efficiency of 70% and λ_∞ = 4.0μm.

Johnson noise of the feedback resistor. A block diagram of the preamplifier circuits is shown in Figure 2-9. As is shown in Figure 2-10, the input noise of this preamplifier 1.5 x 10^{-5} A/Hz at 1 Hz at room temperature and can be reduced by a factor of 5 by lowering the temperature of the input stage to 150 K.

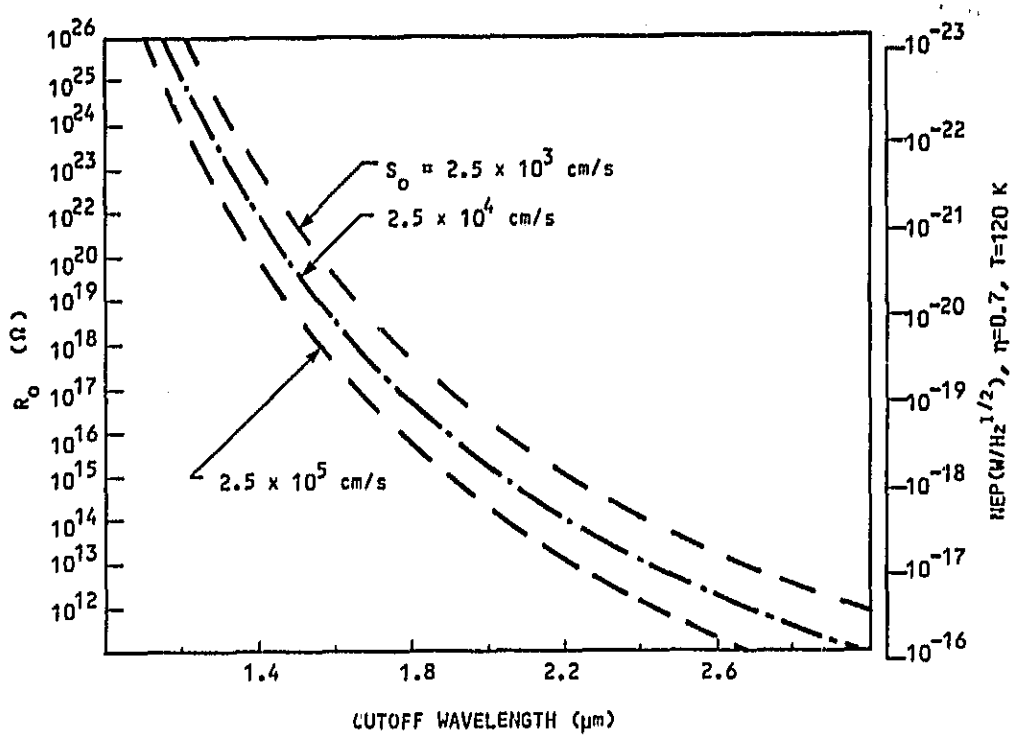


Figure 2-4. Calculated R_o vs Cutoff Wavelength at 120 K for Various Surface Recombination Velocities. The NEP Scale is a Conversion from the R_o Scale with 70% Quantum Efficiency and λ_∞ = 2.0 μm.

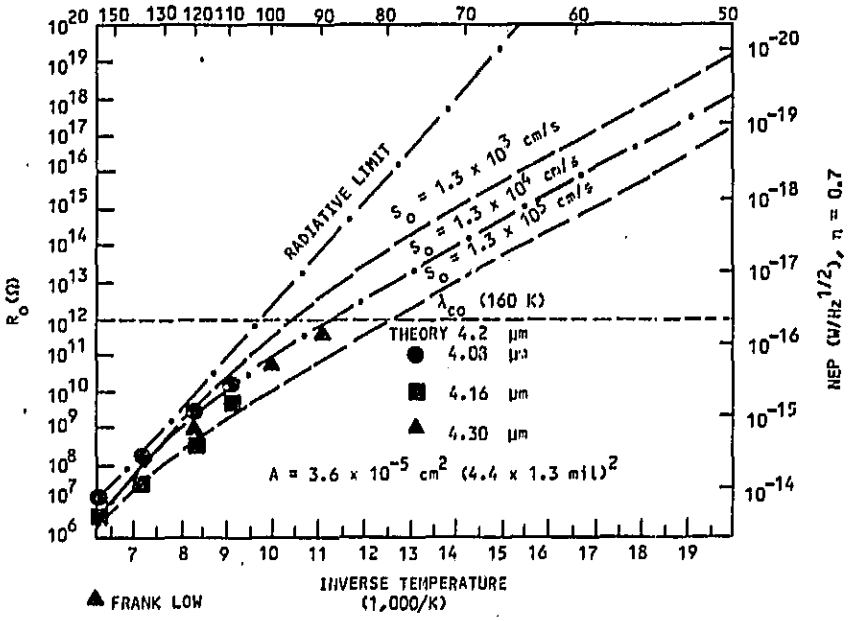


Figure 2-5. Measured Impedance vs Temperatures from Three MW Photodiodes. Measurement was Limited to 10^{12} Ω due to the Johnson Noise of the Feedback Resistor in the Preamplifier.

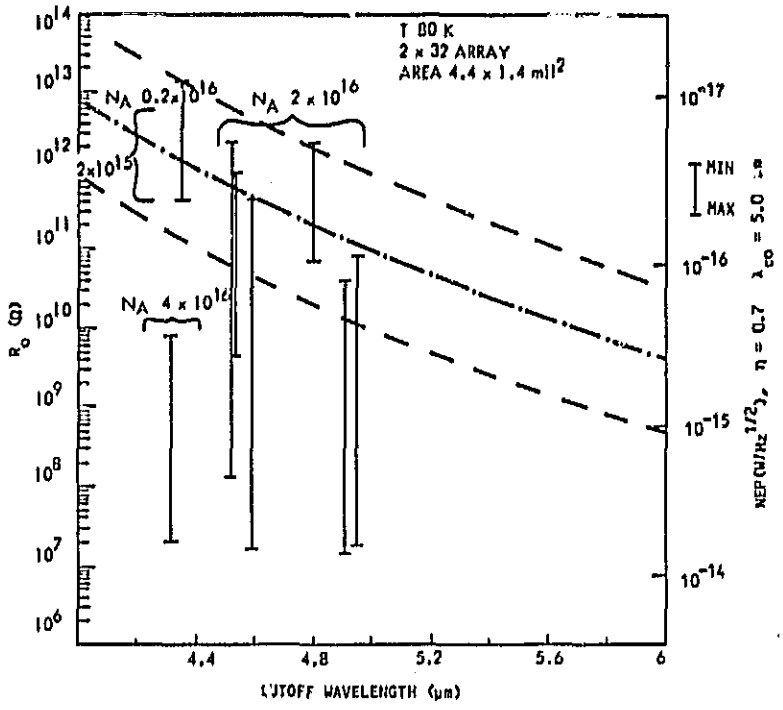


Figure 2-6. HgCdTe MW Array Data Shows Uniformity and Performance Improvement Obtained by Lowering Doping Level.

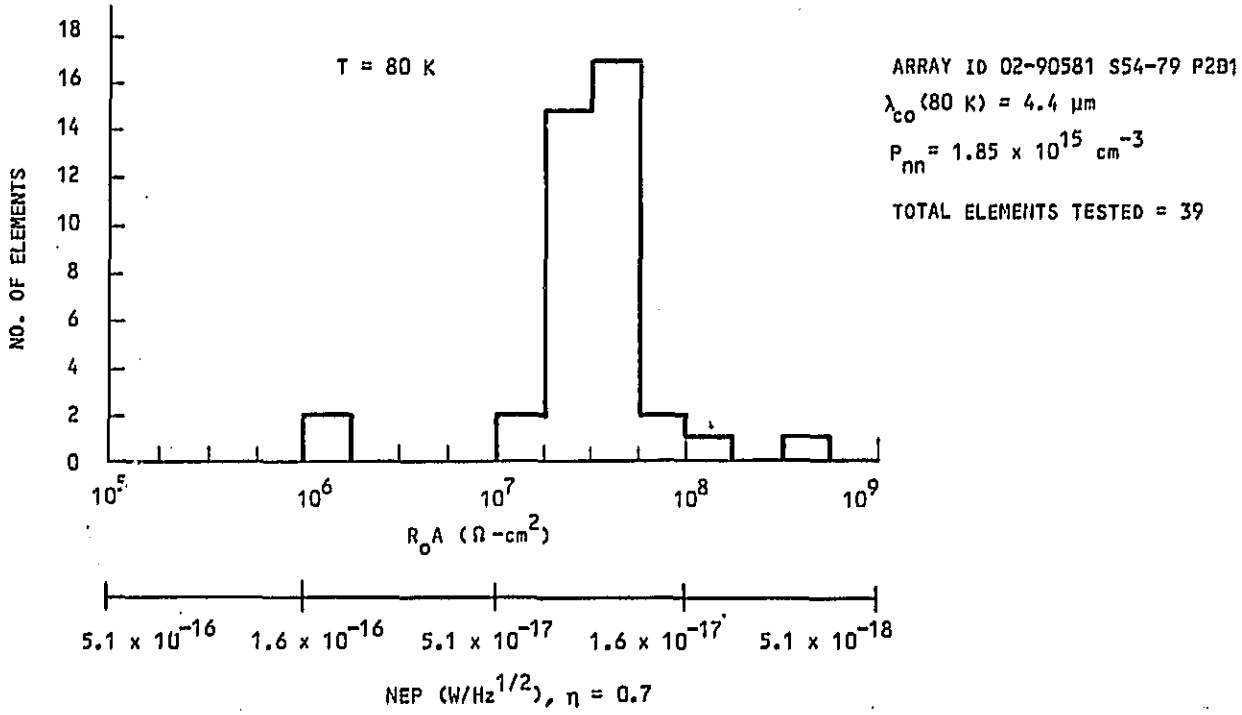


Figure 2-7. R_0A Distribution Shows Good MW Performance Uniformity has been Achieved at 80 K.

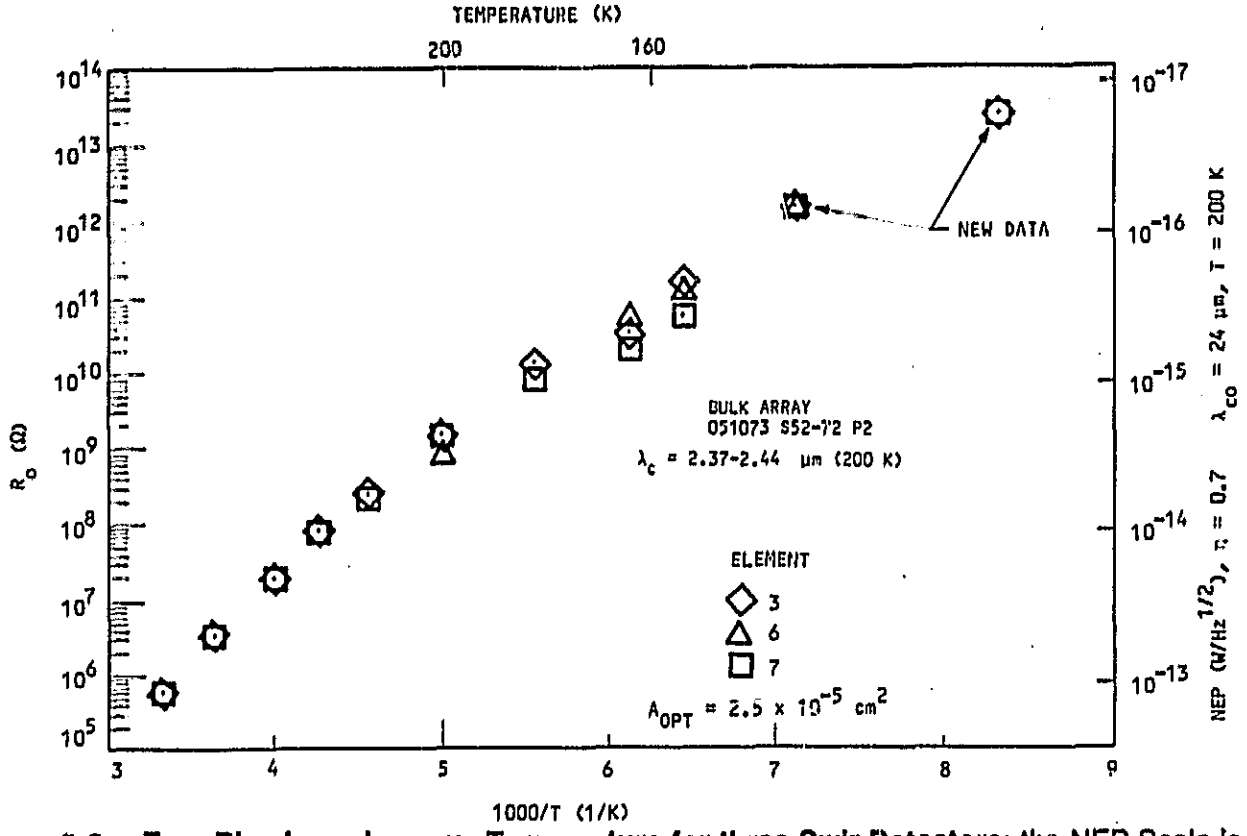
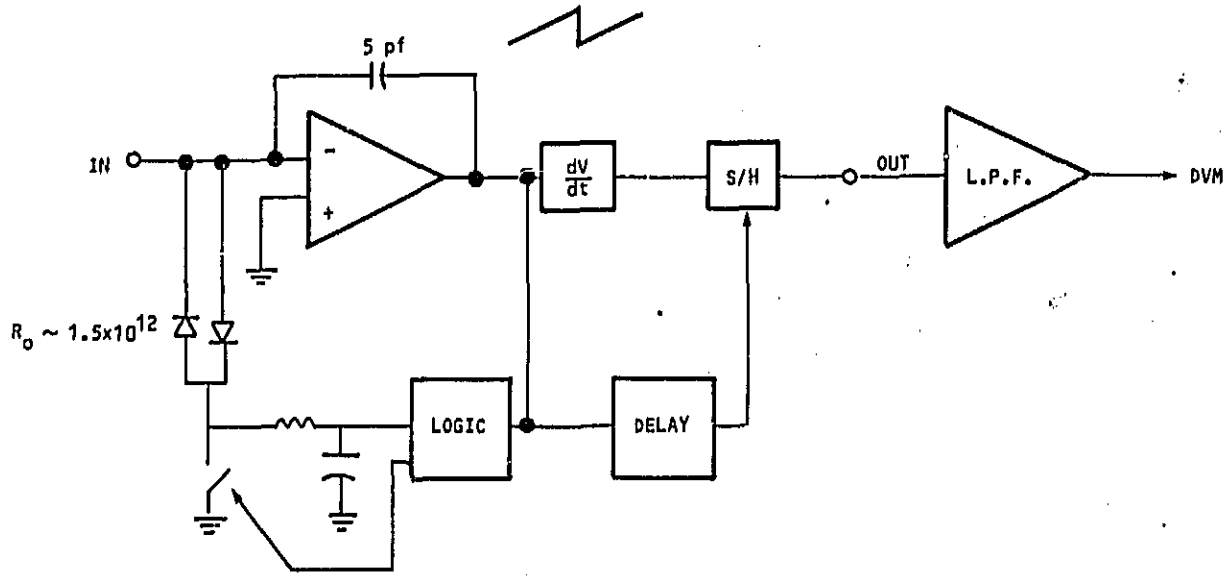


Figure 2-8. Zero Bias Impedance vs Temperature for three Swir Detectors; the NEP Scale is for 70% Quantum Efficiency and l_∞ = 2.40 mm, T = 200 K



- CAPACITIVE FEEDBACK ELIMINATES JOHNSON NOISE OF FEEDBACK RESISTOR.

Figure 2-9. Low Noise Preamplifier Schematic

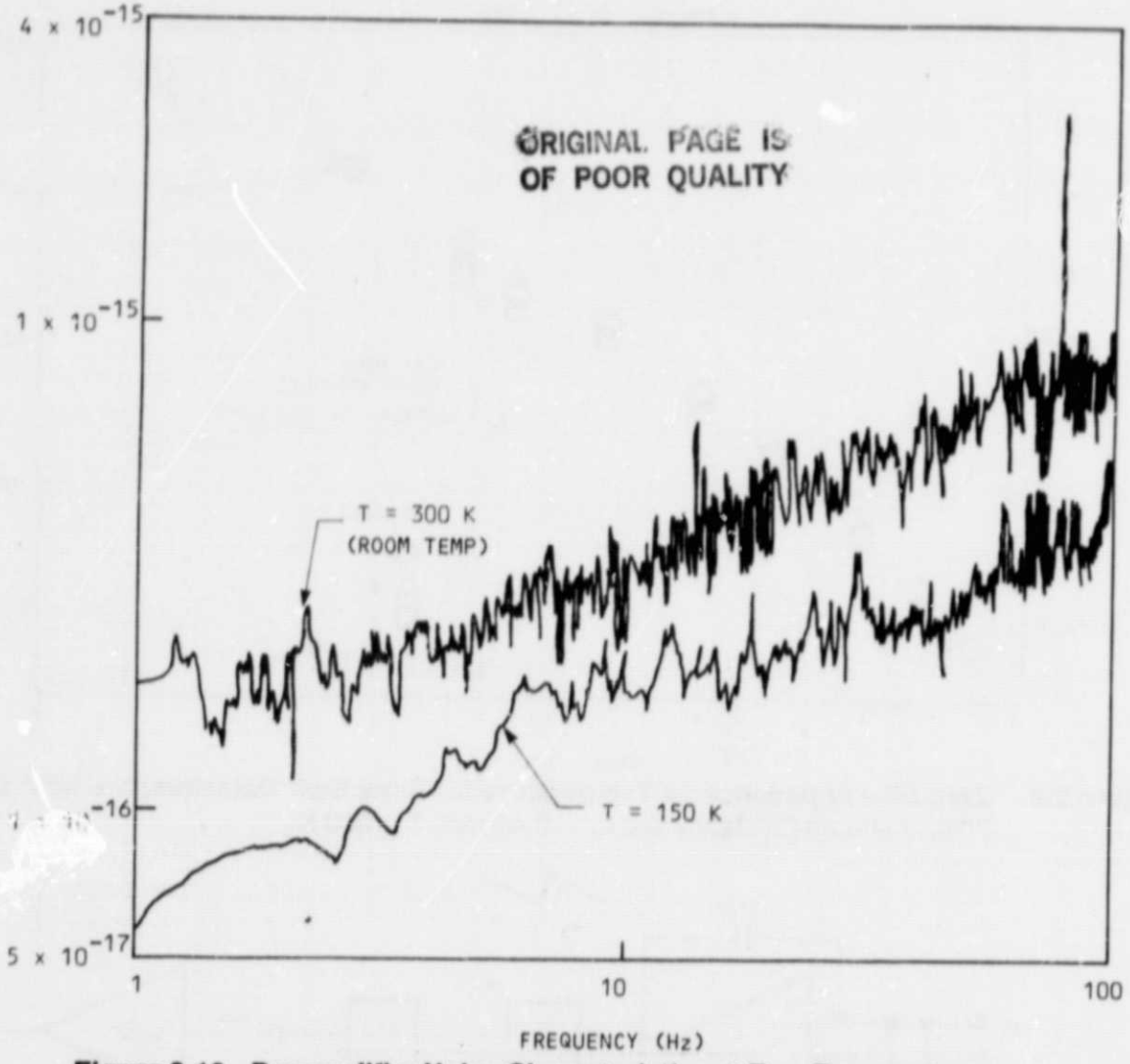


Figure 2-10. Preamplifier Noise Characteristics at Two Temperatures

SECTION 3
DETECTOR FABRICATION

This section outlines the fabrication techniques used, and discusses the device geometry for the arrays fabricated on this program.

The detectors are fabricated on p-type quench-anneal grown HgCdTe. All lapping and polishing is done on automatic equipment, which helps in uniformity of processing. Referring to Figure 3-1, the first steps in processing are lapping and polishing for flatness and thickness control. Final HgCdTe thickness is obtained by chemical etching. This etching step also serves to remove residual damage caused by the lapping and polishing. Once at final thickness, the surface of the HgCdTe has an anodic oxide grown on it. This oxide is removed just prior to ZnS insulator/passivation deposition, and is intended to provide a chemically clean surface. After ZnS deposition, the n^+ diode regions are formed by boron ion implantation through a photoresist mask. This step is followed by deposition of the gold common contact to the p-side. Contact holes are then etched through the ZnS layer for access to the n^+ regions, the HgCdTe in the dicing streets is delineated, and the indium bumps (for interconnection to the outside world) are formed by evaporation and lift off. The arrays are then diced, and bump interconnected to a circuit board.

The detectors were fabricated in a test structure format, which consists of a 4 x 4 element matrix as shown in Figure 3-2.

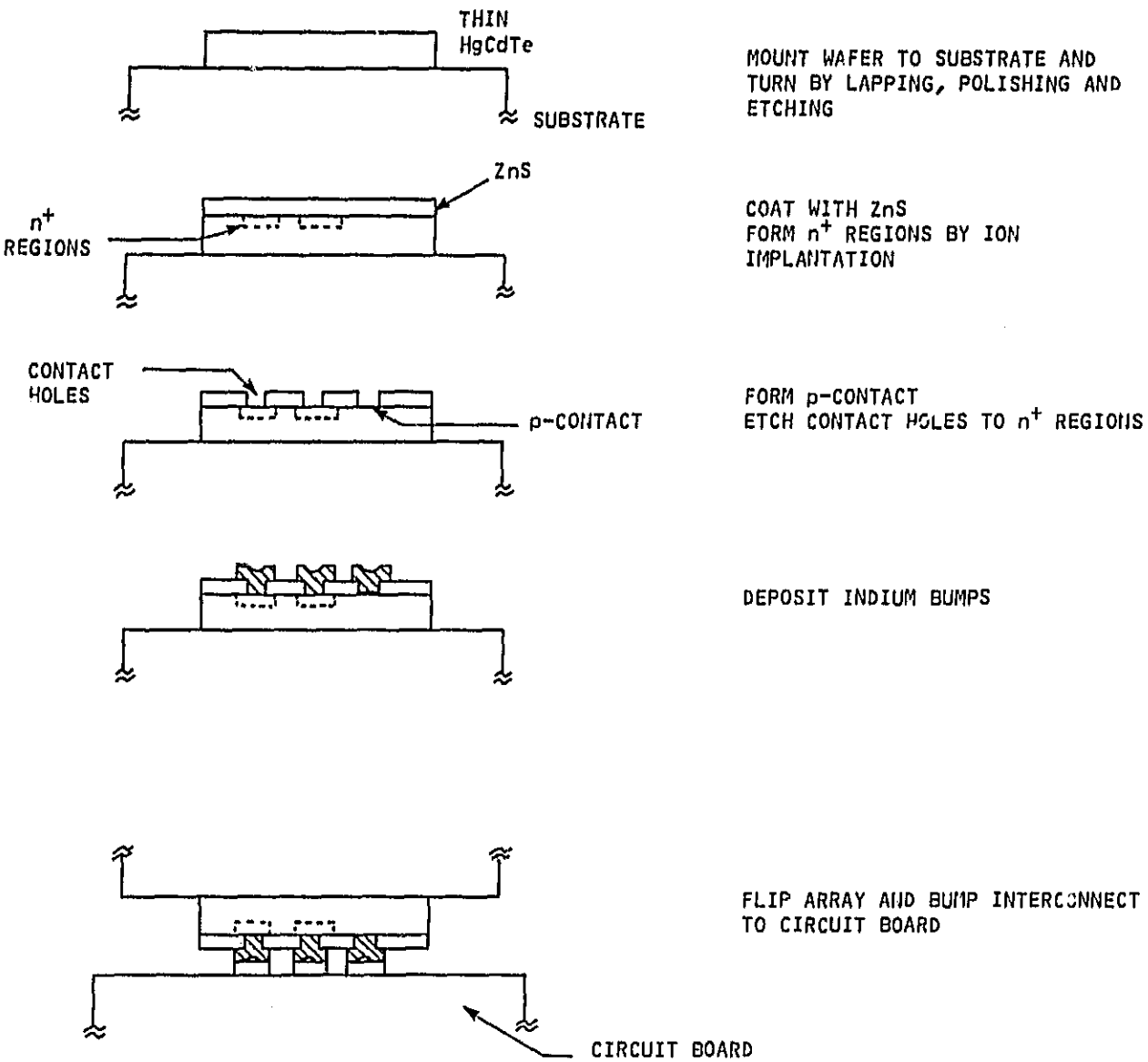


Figure 3-1. Schematic of Detector Fabrication Process

Figure 3-2. Test Array for use on MIRSSA

SECTION 4
CCD COUPLING ANALYSIS FOR SPACE FOCAL PLANES

Configuring a focal plane for space observation applications presents the designer with a unique set of requirements. The zodiacal background collected by large f/# telescopes can yield as little as one to two photons per second, at the detector site. Thus, a photon counter with long observation times would be most desireable. Yet, high density two dimensional array configuration precludes the use of most conventional forms of photon counters.

However, solid state photo-voltaic sensors are easily configured for high density focal planes. Use of conventional readout schemes, such as CID or CCD devices has allowed the number of elements in a focal plane to exceed 10^4. These large high density focal planes have been demonstrated routinely in tactical or terrestrial surveillence applications with moderately high background levels (10^{16} photons/cm^2 s). For space observation applications, with extremely low background levels, the detector impedance must be extremely large (10^{17} Ω) to minimize its thermal noise and approach background limited performance.

This specification on the sensor generates strength requirements on the coupling circuit necessary to read out the detector signal. Efficient coupling schemes for extremely low readout noise are necessary. Furthermore, for scenes encompassing bright objects, the dynamic range of the system must be large, and an antiblooming feature is necessary to avoid masking relevant imagery adjacent to the bright objects.

Finally, in optimized mosaic focal planes, each detector site occupies a space that is on the same order as the systems optical resolution. This size constraint eliminates most complex coupling structures best suited to these high impedance detectors.

During this study phase for low background coupling schemes, four input circuit designs were considered for a CCD multiplexed readout scheme. The four were chosen for simplicity of design and processing capability in large mosaic arrays. Each design was evaluated in terms of performance for space applications. The next section discusses the four designs and is followed by a section detailing the optimal design chosen for space telescope application.

4.1 CCD Input Coupling Schemes

Four coupling schemes were considered for the space astronomy focal planes and are shown in Figure 4-1. Each coupling circuit is simple enough to be configured into large mosaic focal planes. Direct source injection passes the detector current directly into the CCD input.

Direct gate coupling modulates the CCD input current by the open circuit voltage across the detector and has the advantage of adding current gain at the input. The last two schemes allow the detector current to be integrated onto the detector mode capacitance and then sampled by the CCD input. Sampled source injection is a destructive sampling process, whereby the integrated charge is transferred into the CCD once every sample. The resettable gate coupling scheme provides a non-destructive means of sampling the voltage on the detector capacitance.

This allows for multiple sampling during the integration time. However, voltage on the detector must be periodically reset to maintain the proper current gain for the configuration.

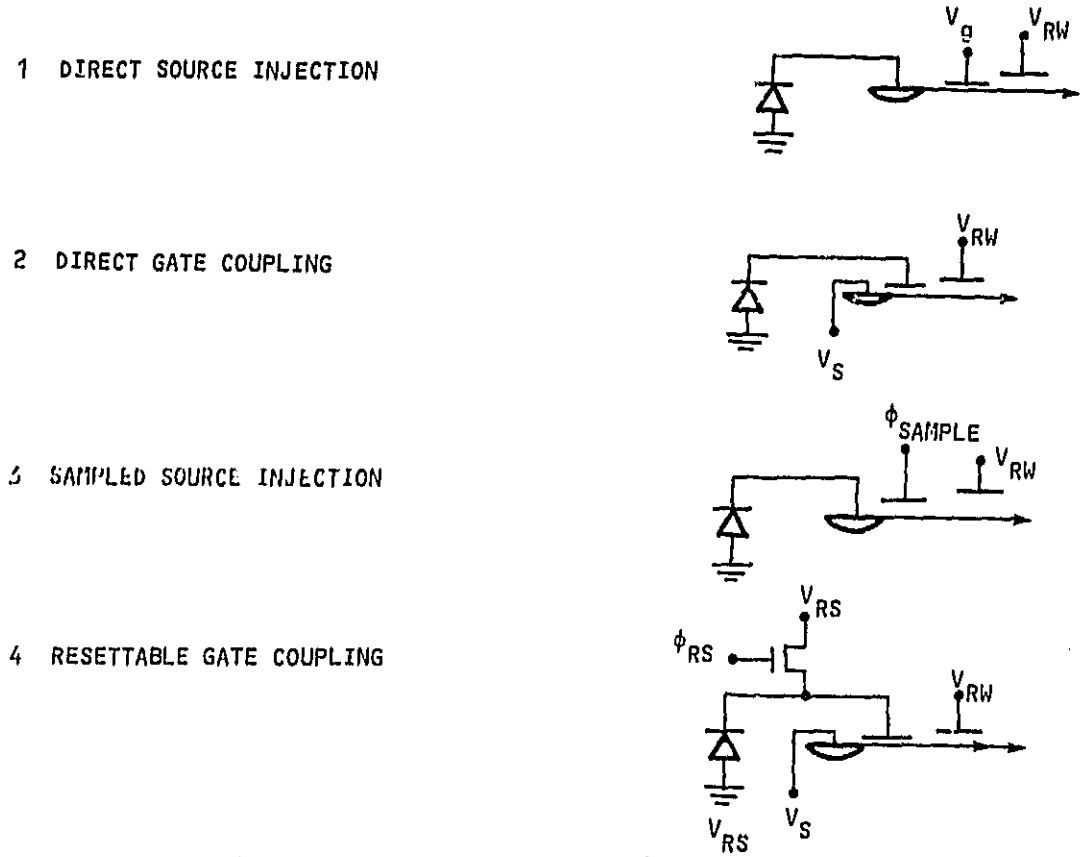


Figure 4-1. CCD Input Coupling Schemes

Relative performance summary of the four coupling schemes is given in Table 4-1.

Direct source injection is commonly used in focal planes where high background levels ($< 10^{13}$ photons/cm²s) are expected. In operation, a large input transconductance is required for good coupling efficiency. Since the CCD transconductance varies with the CCD input currently, an additional bias current would be

Table 4-1. RELATIVE PERFORMANCE OF COUPLING SCHEMES

COUPLING SCHEME	COMMENTS	NOISE FIGURE
Direct Source Injection	Requires Optical Bias Current for Good Coupling Efficiency	Poor Noise Figure at Low ϕ_n Limited by CCD Transfer Noise and Bias Shot Noise
Direct Gate Coupling	Requires Very Long Observation Times and Good Detector Uniformity	Modest Noise Figure Limited by CCD 1/f Noise
Sampled Source Injection	Eliminates CCD 1/f Noise but Adds KTC Reset Noise	Poor Noise Figure Limited by CCD Transfer Noise and KTC Noise
Resettable Gate Coupling	Nondestructive Readout Allows KTC Noise Removal by Differencing	Best Noise Figure Limited by CCD 1/f Noise

necessary for good coupling in focal planes designed for astronomical applications. The additional bias current could be introduced electrically or optically, but the added shot noise associated with the extra current would significantly compromise detector performance. Figure 4-2 illustrates the noise figure as a function of background flux for this configuration. For the low background region expected for space observation, the analysis leads to an unacceptable noise figure of 30 for the direct source injection method.

Direct gate coupling has the distinct advantage of providing a current gain at the input and thus reducing the requirement on the CCD related readout noise. The detector is operated in an open circuit configuration. Voltage developed across the detector as a result of photo-current I_η is applied to the integrating gate to modulate the CCD input current. For subthreshold operation, the current gain, A_I, can be expressed as

$$A_I = \frac{I_{CCD}}{Ng(I_{sat} + I_\eta)}$$

where Ng, I_{CCD}, and I_{sat} are the gate derating factor (1.6 to 2.0), CCD input current, and detector saturation current. A gain as high as 100 can be accommodated with this circuit.

Unfortunately, this configuration has a restricted frequency bandwidth with a cutoff specified by:

$$f_{co} = \frac{1}{2\,R_{oc}(C_d + C_g)}$$

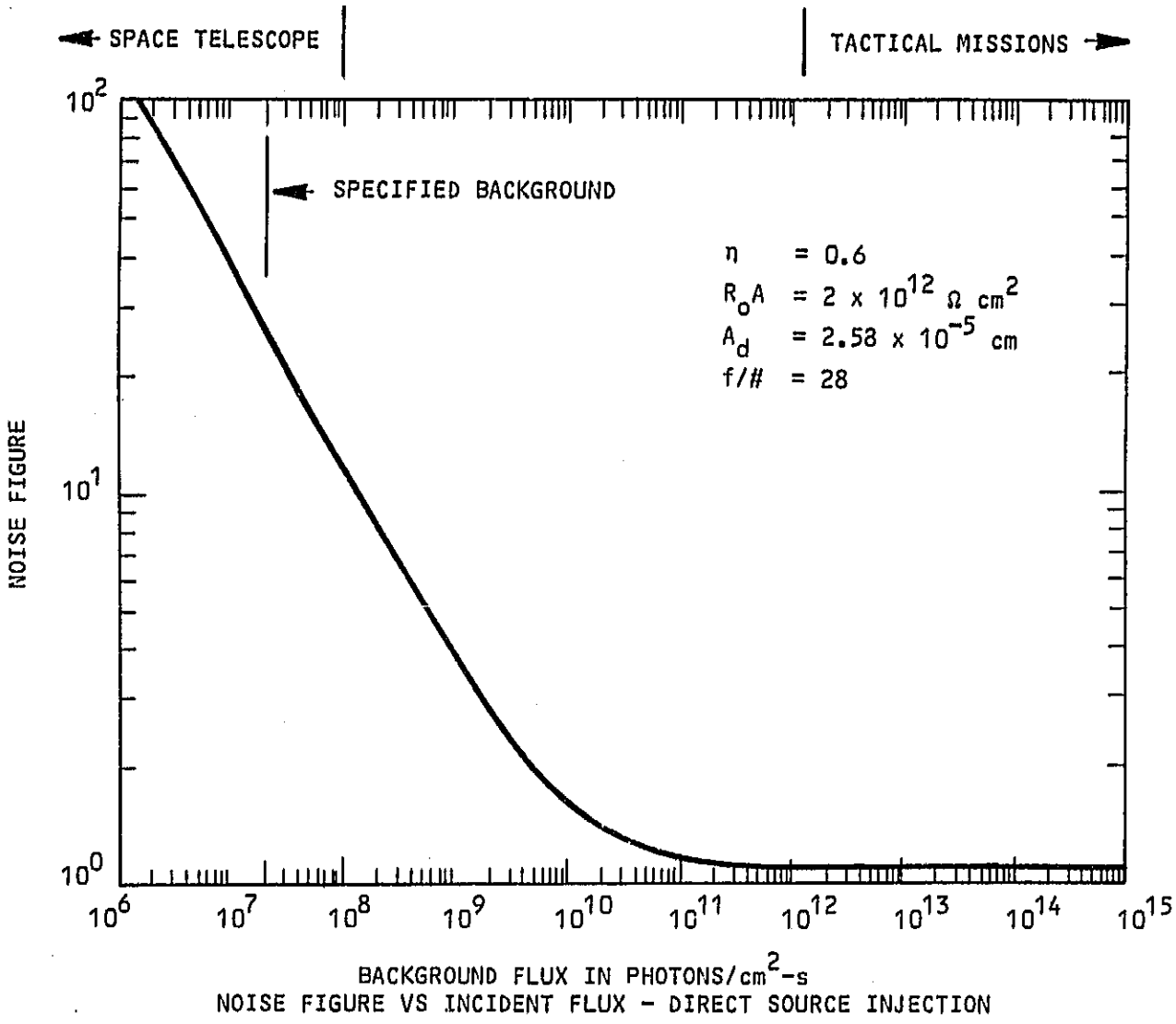
For large detector impedances necessary for low astronomical background levels, the cutoff occurs at less than 1.0 Hz. This alone is not prohibitive since long integration times are possible and dark current in the CCD is practically nonexistant at operating temperatures of 80 K or less. The limiting factor, however, will be the CCD input 1/f noise which severely impacts the noise figure for this system.

Sampled source injection eliminates the need for a bias charge. This is accomplished by waiting to inject charge into the CCD input until a sufficient amount of photo-current has been integrated on the detector capacitance mode. At the end of an integration cycle which can be several 100 seconds long, the control gate, 0_{sample} is clocked allowing the charge to flow rapidly into the input. This operation also resets the voltage on the detector capacitance. Because the input gate 0_{sample} is used as an analog switch and not as a modulating gate for the incoming current, the CCD input 1/f noise is virtually eliminated. Unfortunately, resetting of the capacitance potential by the input produces a reset noise whose rms value is determined by

$$i_{Reset} = \frac{KTC \neq}{ti} A_{rms}$$

Furthermore, this scheme has only unity gain, and therefore requires very low readout noise by the CCD. The result is a poor figure limited by the CCD readout and reset noises on the detector capacitance.

Resettable gate coupling (RGC) is capable of current gain while providing non-destructive sampling at the input. The current gain has the advantage of suppressing the readout noise of the CCD. Non-destructive sampling allows for a series of samples to be taken as the open-circuit voltage is developed across the detector capacitance, during each integration period. At the end of each integration period, the voltage is reset by a MOSFET. Although this process generates reset noise, it can be virtually eliminated by post processing using differencing of samples taken from within an integration period. In addition, differencing will also suppress the CCD input 1/f noise which would otherwise be very dominant. This significant reduction in noise is accomplished with only a factor of two loss in the signal as a result of differencing. Analysis has shown that a noise figure of about 2.0 is possible with the coupling scheme.



NOISE FIGURE VS INCIDENT FLUX - DIRECT SOURCE INJECTION

$$NF = \left[(2qI_{CCD} + \frac{2q^2}{t_i}(200^2) + \frac{4KT}{R_o})/2qI_{\emptyset}\right]^{1/2} + 0.2$$

Figure 4-2. Direct Source Coupled Noise Figure

On the basis of these unique features, Honeywell recommends the RGC coupling approach for low background space applications. A detailed description of this approach is presented in the next section.

4.2 Resettable Gate Coupled Analysis

A schematic of the RGC input structure is shown in Figure 4-3. The photo-voltaic detector is connected to the integrating gate of the CCD input. A switch placed across the detector is used to periodically reset the circuit before each sampling interval. In practice, the ideal switch shown in the schematic is replaced with MOSFET compatible with the CCD fabrication process.

In operation, the voltage on the integrating gate will behave as shown in Figure 4-4. Initially, the gate voltage is reset to V_{RS} and the detector returned to zero bias by the reset switch. At time t = 0, the switch is opened allowing the photocurrent, I_0, to begin charging the capacitance on the anode side of the detector. Just before the next reset, at t = T, the voltage on the capacitance is

$$Vg = V_{RS} + I_0 T/C.$$

For subthreshold operation, the CCD input current is expotentially modulated by Vg, according to

$$I_{CCD} = \frac{I_0 \exp q (Vg - V_{th})}{Ng KT}$$

where Ng is the gate derating factor which has been measured to range from 1.6 to 2.5 on Honeywell fabricated devices, and V_{th} is the threshold voltage of the input. This current is integrated into the potential well under the receiving gate, V_{RWO}. After a period, $t_i = T$, the accumulated charge packet is transferred into the CCD by the 0_T gate, where it is multiplexed with other input charge packets to form a serial data stream which is later converted to a voltage at the output.

For proper operation, the CCD integration period, T_i must be small to allow numerous samples of gate voltage during the detector sample interval, T. This permits the input to operate with a high enough current to supress the input circuit noise and CCD readout noise.

Post processing of the CCD data enables the original gate voltage signal to be recovered. Figure 4-5 illustrates the processing steps applied to the raw CCD output from a single input. For array operation, this is done in parallel for each input. First, a logarithmic amplifier is employed to compensate for the exponential gain of the CCD input circuit. Then, a matched filter followed by a summing operation performs the subtraction of samples within the sample interval.

The differencing maximises the output signal-to-noise ratio by removing the reset KTC noise and suppressing the CCD input 1/f noise. In addition, fixed offsets due to threshold voltage variations on the inputs are removed. The resulting value after differencing is related to the amplitude of the voltage ramp on the detector.

Calibration of the focal plane requires measurements of known background fluxes to compute both offset and gain compensation tables. These tables account for detector responsivity variations and are used to normalize the response from each detector in the focal plane.

The small signal equivalent circuit for the input structure is shown in Figure 4-6. Current from the detector is bandlimited by the RC network consisting of the detector resistance, R_0, and the capacitance, C, which includes the diffusion capacitance of the detector, the capacitance on the CCD gate, and any stray capacitance associated with the detector/CCD interconnect structure. The total detector noise on the CCD input gate is:

$$V_d^2 = [2qI\phi + 4\ kT/R_o] \frac{R_o^2}{1 + (\omega R_o C)^2}\ (V^2/Hz)$$

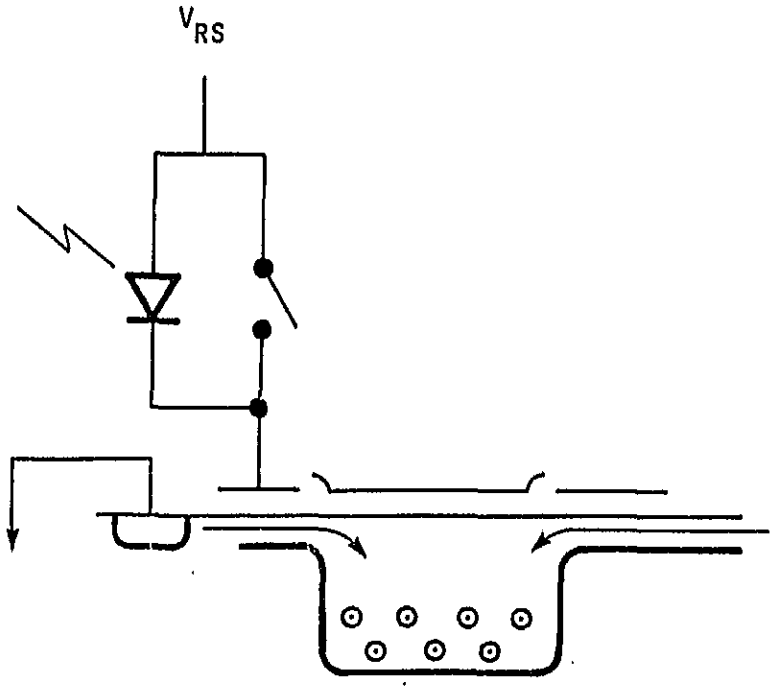


Figure 4-3. Schematic of RGC Input Circuit

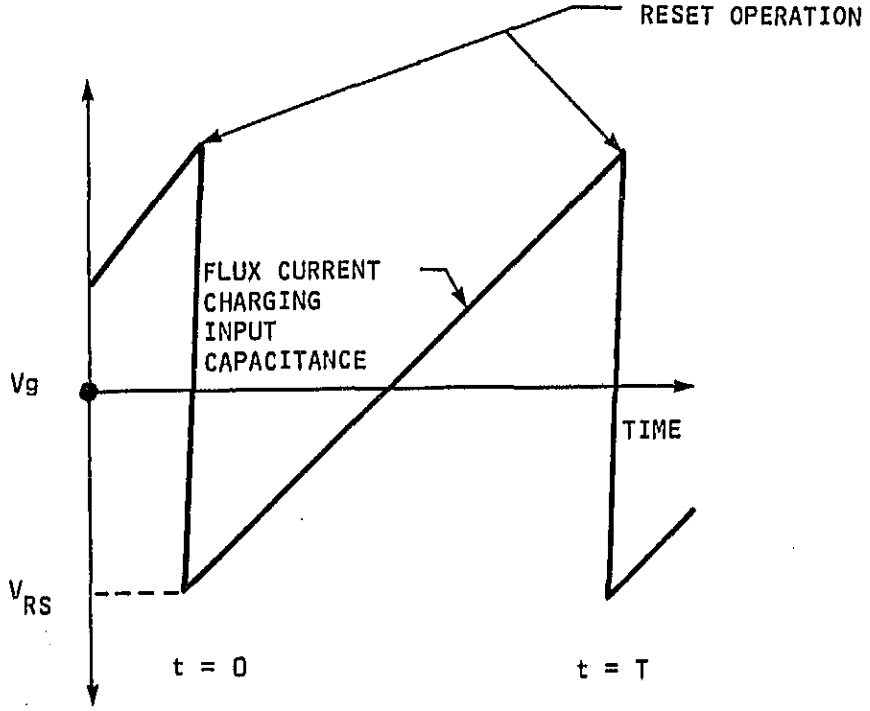


Figure 4-4. Resettable Gate Coupled Analysis - Gate Voltage Waveform

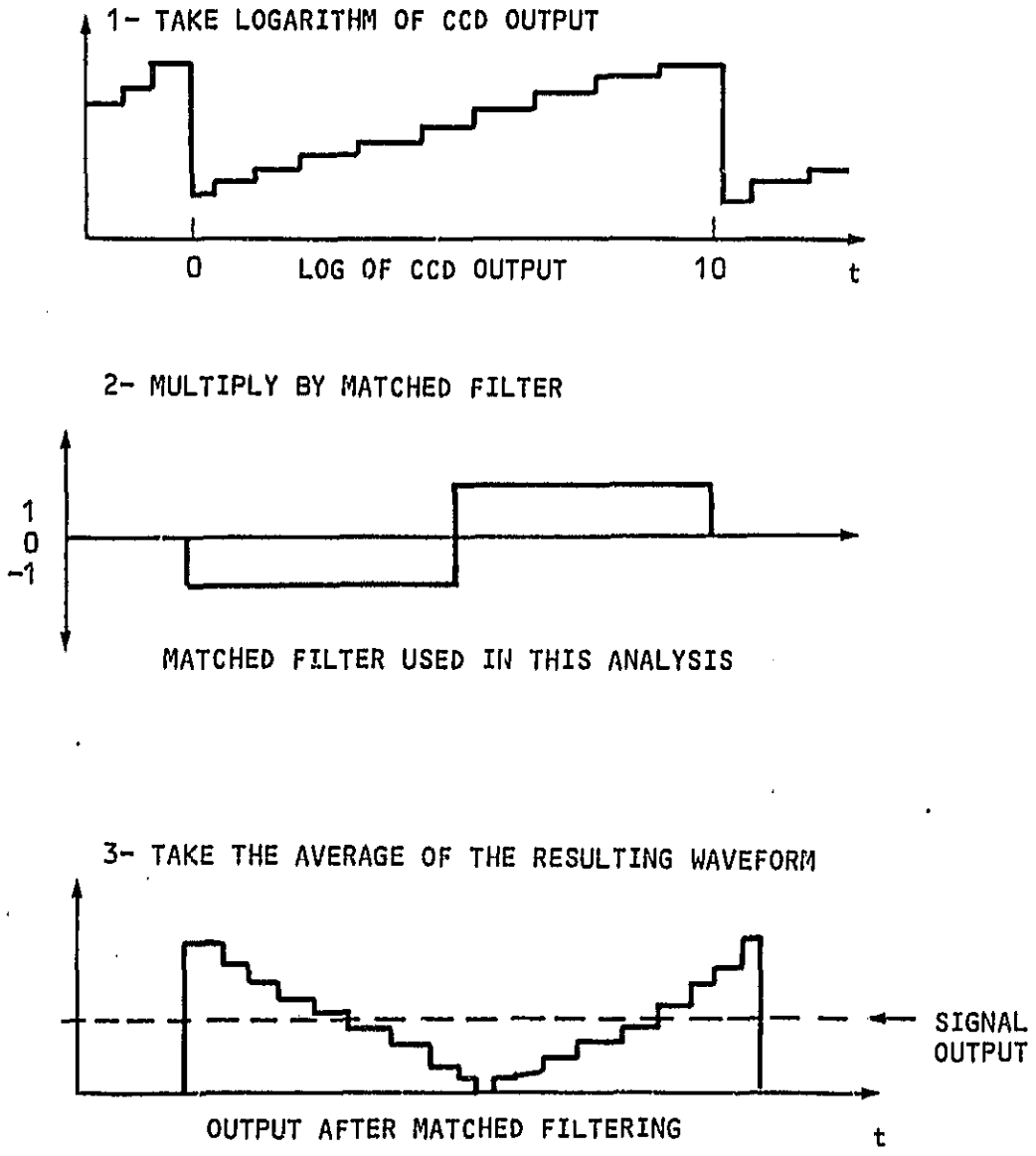


Figure 4-5. Matched Filtering Operation

where the first term is the photo-induced shot noise, and the second is the detector Johnson noise. Virtually, no detector 1/f noise is expected while operating a zero bias. The CCD noise referred to a voltage on the gates is:

$$V_{CCD}^2 = \frac{\delta kT}{C_{ox}^2 A_g f^{0.84}} + \frac{1}{g_{mg}^2} 2qI_{CCD} + \frac{2q^2}{t_i} (N_T)^2$$

The first term is the gate 1/f noise, where C_{OX} is the capacitance on the gate, Ag the area of the gate, and F a processing dependent parameter which has been measured to vary from 2.5 pfd to 250 pfd on Honeywell devices. The last two terms represent the input channel shot noise and the noise associated with transfer of charge along the CCD. The parameter, N_T represents the number of rms noise electrons generated

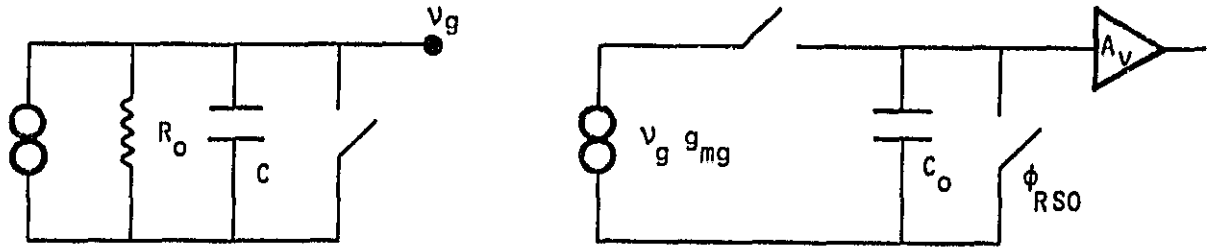


Figure 4-5. Small Signal Equivalent Circuit

during the transfer process. The transconductance,

$$g_{mg} = \frac{q\, I_{CCD}}{NgKT}$$

is related to the CCD operating current. The higher the CCD current, the more suppression of the two noise terms in the brackets. In normal operation this current is set by the CCD integration time, t_i and the charge capacity of the CCD.

A representative power spectrum of the various noise sources are shown in Figure 4-7 and Table 4-2 lists all the parameters required to generate the figure. The detector terms are rolling off because of the extremely low bandwidth of the voltage generated on the input gate.

The post processing matched filter operation modifies the noise spectrum in the figure by:

$$\left[\frac{\sin^2\left(\frac{\pi fT}{2}\right)}{\left(\frac{\pi fT}{2}\right)^2}\right] * \left[2\sin\left(\frac{\pi fT}{2}\right)\right]$$

where the first factor is due to the summing of sample over half the sample time T, the second factor is a result of differencing.

The calculated rms noise voltage for each component is listed in Table 4-3. The CCD 1/f noise dominates the photon shot noise. The next significant noise source is the detector Johnson noise. The total noise referred to the input gate is a 2.8 μV rms and a noise figure of 2.0 for the detector/CCD system is predicted. A signal of 62 μV is generated on the gate during a 10 minute sample period, but because of the differencing operation, this is reduced to 31 μV. The signal-to-noise ratio for the system is 11. This was calculated assuming a minimum flux of 7 x 10^7 photons/s-cm^2 collected by an f/28 optical system and incident upon a 2 mil x 2 mil detector.

The results are based on an ideal switch placed across the detector. In practice, this switch will be a MOS device that will introduce additional leakage current on the reset node and a source of voltage pick-up due to the reset clock. The leakage current can be minimized by using a minimum geometry source on the MOSFET switch and the pickup can be substantially reduced by using a screen gate adjacent to the source. Additional clock voltage pick-up on the input gate due to other CCD clocks must also be suppressed, by electrically shielding the detector array from clocks used on the CCD. This is done by fabricating the device with a blanket metal layer and tieing it to a dc potential.

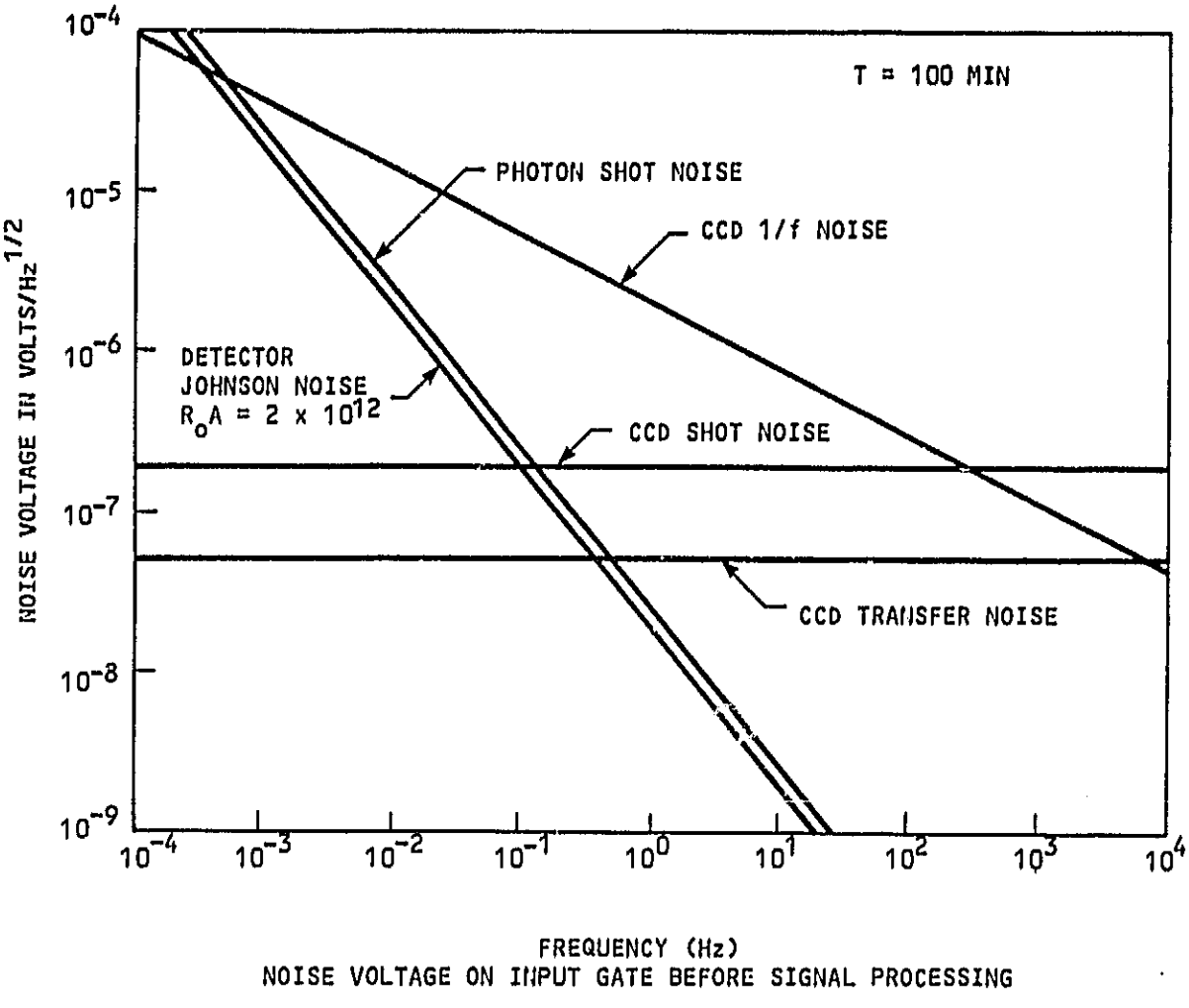


Figure 4-7. Noise Voltage on Input Gate Before Signal Processing

Table 4-2. LIST OF INPUT PARAMETERS USED BY NOISE MODEL

Flux = 7E7*P1/(4*28²+¹)	Incident flux
R_oA = 2E12	R_oA of diode
A_d = 2.58E-5	Detector area
C_d = 1.5E-12	Detector capacitance
C_{ox} = 6.28E-8	Oxide capacitance per cm²
μ = 1500	Mobility of carriers
T_{CCD} = 60	CCD operating temperature
N_{eff} = 0.60	Diode quantum efficiency
G_a = 4.0E-11	CCD 1/f noise parameter
N_g = 1.8	Gate n factor
Z_g = 3.0E-3	Integrating gate width
L_g = 6E-4	Integrating gate length
Q_e = 1.602E-19	Electron Charge Coulombs
K = 1.380662E-23	Boltzman Constant Joule/kelvin
$R_o = R_oA/A_d$	Detector zero bias resistance
$C_g = L_g*Z_g*C_{ox}$	CCD gate capacitance
$C_{stray} = C_g/2$	Stray capacitance
$C_{sum} = C_g + C_d + C_{stray}$	Total input capacitance
T_I = 1E-3	CCD integration time
$I_{CCD} = 5E6*Q_e/T_I$	CCD input current

Table 4-3. RESULTS OF NOISE ANALYSIS

System Parameters	
Observation Interval	10 Minutes
Photon Flux	7×10^7 Photons/(s, cm^2 Hemisphere)
Optical f#	28
Detector R_0A	2×10^{12} Ω-cm^2
Quantum Efficiency	60%
Signal and Noise After Signal Processing	
Photon Shot Noise	1.4 μVrms
Detector Johnson Noise	1.2 μVrms
CCD 1/f Noise (550 Å Gate Oxide)	2.1 μVrms
CCD Shot Noise	0.01 μVrms
CCD Transfer Noise	0.003 μVrms
Total Noise	2.80 μVrms
Signal Voltage	31.2 μV
Signal to Noise Ratio	11
System Noise Figure	2

SECTION 5
LOW TEMPERATURE CCD MEASUREMENTS

Low temperature operation of the FPA is required to obtain the high sensitivity potential of the photo-voltaic detectors. A practical lower limit for the operating temperature will be determined by the CCD performance. As temperature is reduced, the CCD transfer efficiency degrades and is accompanied by an increase in transfer noise. Of much less importance is the dark current level within the CCD, which fortunately decreases rapidly with lower operating temperatures. By employing the RGC CCD approach, with sufficient input current gain, the contribution of the transfer noise and dark current can be substantially reduced.

To study the temperature dependence of CCD performance, two types of Honeywell manufactured CCDs were selected and evaluated at temperatures ranging from 35 K to 300 K. Table 5-1 contains the pertinent design parameters for the two CCD types. The first device is a 128 bit, 2 phase buried channel device and the second is a 20 bit, 3 phase surface channel CCD. Functional CCD operation was observed on these CCDs down to 35 K, but their performance was limited by poor transfer efficiency.

CCD Dark Current

The dark current requirements for a CCD incorporated into a focal plane for space application, could require a dark current level of less than 1 fA/cm² if no pre-amplification of the detector signal is employed. Fortunately, Honeywell's approach, using the RGC input circuit does provide significant input gain thus relaxing the dark current requirements. Figure 5-1 shows that the measured dark current decreases exponentially with temperature on the 2178 device. The dark current was already less than 1 pA/cm² at 220 K and below our measurement capability. At temperatures $\leq$ 80 K the dark current is expected to be insignificant with our gate coupled approach.

CCD Transfer Efficiency & Transfer Noise

The integrity of a charge packet transferred through a CCD is effected by the efficiency of each transfer and the noise associated with the transfer process.

The small fraction of charge loss from each charge packet to the succeeding charge packet in the transfer process contributes a form of

Table 5-1. CCD Test Vehicles

CCD	Type	Register Length	Bit Length (μm)	Charge Capacity (Electrons)
2178	2-Phase Buried Channel	128 Bits	50	18×10^6
3027-R381	3-Phase Surface Channel	20 Bits	26	6×10^6

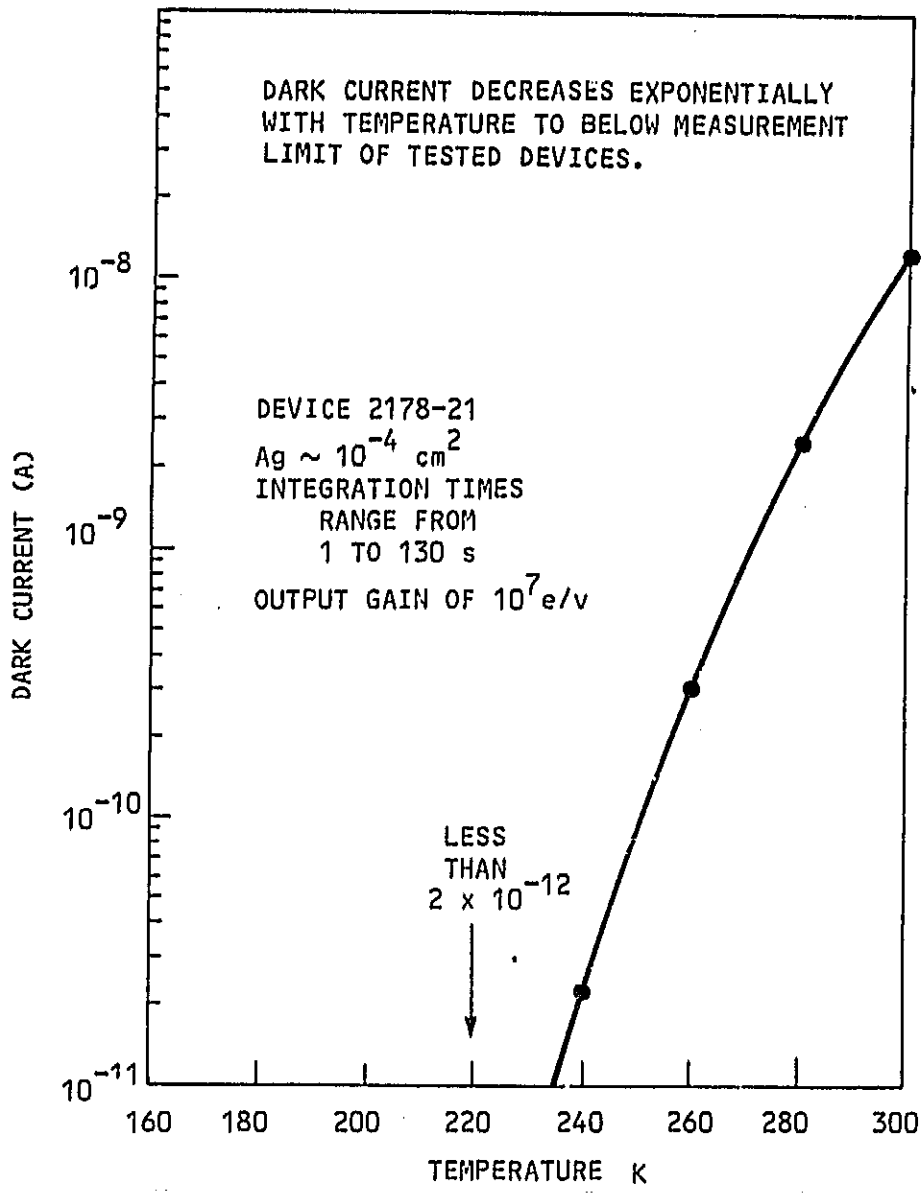


Figure 5-1. Dark Current Measurements

cross-talk in the multiplexed signals packets within the CCD and can limit overall system performance. Figures 5-2 and 5-3 illustrate the transfer efficiency of the two types of CCDs used in this study at four different temperatures. Similarly, the transfer noise can become the dominant readout noise in the focal plane and must be accounted for in modeling device performance.

The transfer efficiency and associated noise are dependent upon the trap density and trap time constants which are temperature dependent parameters and to some extent can be

Figure 5-2. Surface Channel Transfer Efficiency Data (No Fat Zero)

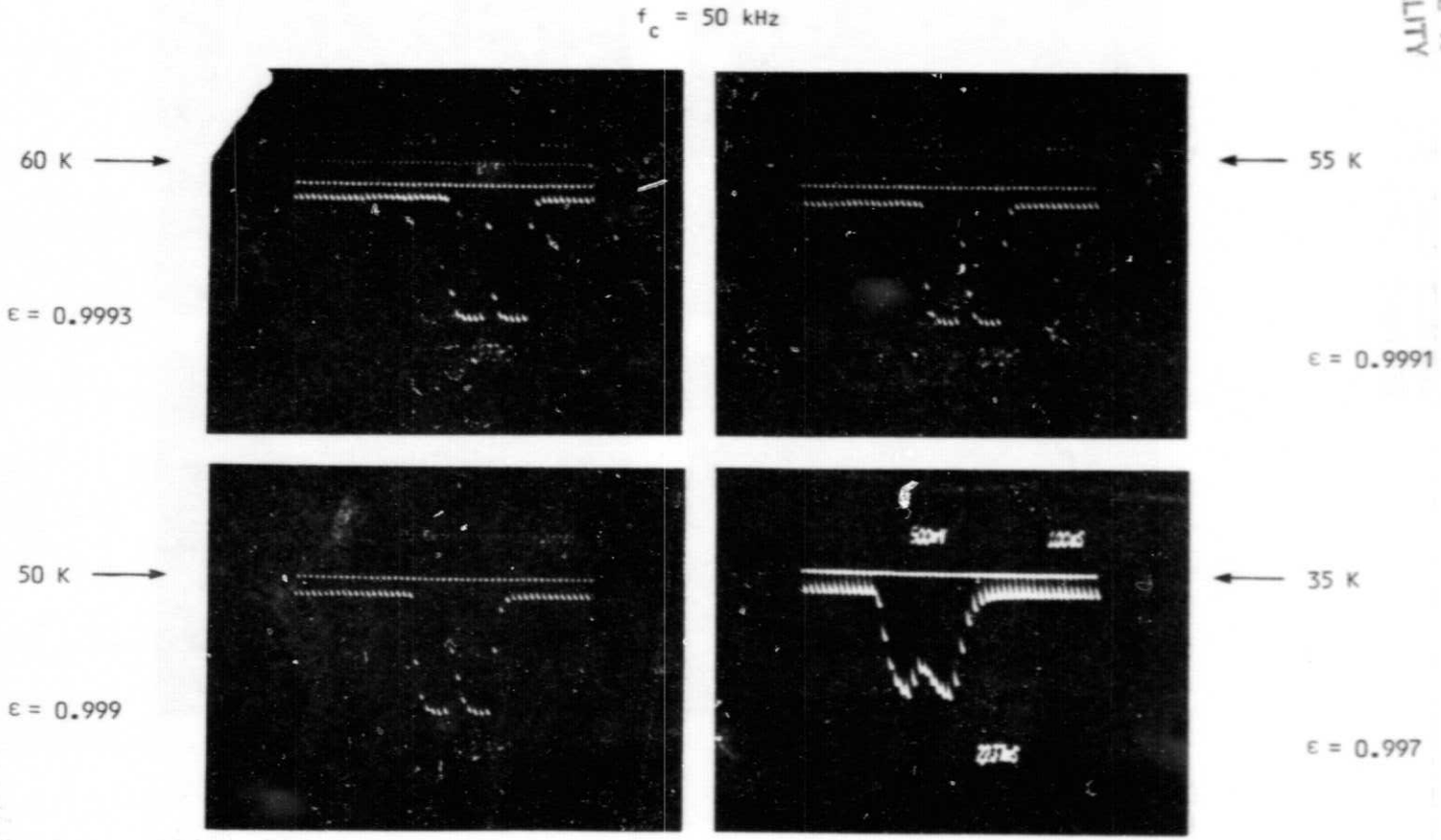


Figure 5-3. Buried Channel Transfer Efficiency Data (10% Fat Zero)

controlled through appropriate CCD processing. CCD design factors can also influence the transfer mechanisms, such as gate length, surface or buried channel, and the number of transfers per bit. Finally, proper operation of the CCD is used to optimize the transfer process. The data rate and clock waveforms are important as well as the use of a fat zero bias charge level in the register.

Figures 5-4 through 5-8 illustrate the dependence of the transfer efficiency on temperature, data rate, and bias charge for both the surface channel and buried channel CCD. A summary of the transfer efficiency measurement is shown in Table 5-2.

In addition to the systematic loss of charge from each charge packet, there exists random fluctuations in the loss affecting the size of the charge packets being transferred, which therefore introduce noise. This so-called transfer noise has a distinguishable spectral characteristic. This is because the loss of charge from one packet must show up as a corresponding increase in charge in succeeding packets which produce a correlation in the fluctuations in adjacent charge packets. The transfer noise spectrum has the form of:

$$S_T(f) \quad \alpha \quad \frac{4\eta\overline{\Delta Q_{tr}}^2}{q^2} f_C \,(1\text{-}cos\, 2\,\Pi f/fc)^{1}$$

where η is number of transfers, ΔQ_{tr}^2 is the variance of the charge per transfer, and f_c the clock rate for the CCD.

For performance modeling, the transfer noise in each packet is expressed in terms of RMS electrons;

$$N_T = \left[\frac{2\eta\overline{\Delta Q_{tr}}^2}{q =}\right]^{1/2}$$

Measurement of a two-phase, 128 bit buried channel CCD operating at 80 K is shown in Figure 5-9. For small charge packet size, less than 6 percent of the full well size, noise is dependent of the charge packet size. Above the 6 percent level, the transfer noise is independent of the charge packet size, and is above 1 x 10^3 rms noise electrons. For a charge capacity of 1.8 x 10^7 electrons a dynamic range of 1.8 x 10^4, or 85 dB is attainable with the CCD structure.

The dependence of N_T on the number of transfers shown in Figures 5-10 and 5-11. Since theoretical analysis would indicate that $N_T \alpha n^{0.5}$, this measurement 0.44 for the exponent is within reason. Typical measurements of the transfer noise as a function of temperature shown in Figure 5-12. Lowering the temperature from 80 K to 60 K causes the buried channel transfer noise to almost double to 2150 rms noise electrons.

For the 20 bit three phase surface channel device the characteristic transfer noise spectrum was not discernible above the flatband noise. Therefore, the measurement shown in Table 5-3 indicates an uper limit to the transfer noise. This data was generated by injected charge in a low noise fill and spill mode into parallel fat zero inputs, measuring the noise spectrum of a single selected channel and corresponding rms noise. The transfer noise increases as the temperature is decreased but not as fast as observed with the buried channel device. Also, it should be mentioned that this surface channel device has about 1/3 the charge capacity of the buried channel device and therefore its transfer noise must scale proportionally.

In conclusion, a set of CCD design recommendations for space FPA application has been generated based on the low temperature noise analysis and associated measurements:

1. K.K. Thornber & M.F. Tom Psett, IEEE Trans. Electron Devices, VOL ED-20 pp. 456, Apr. 1973

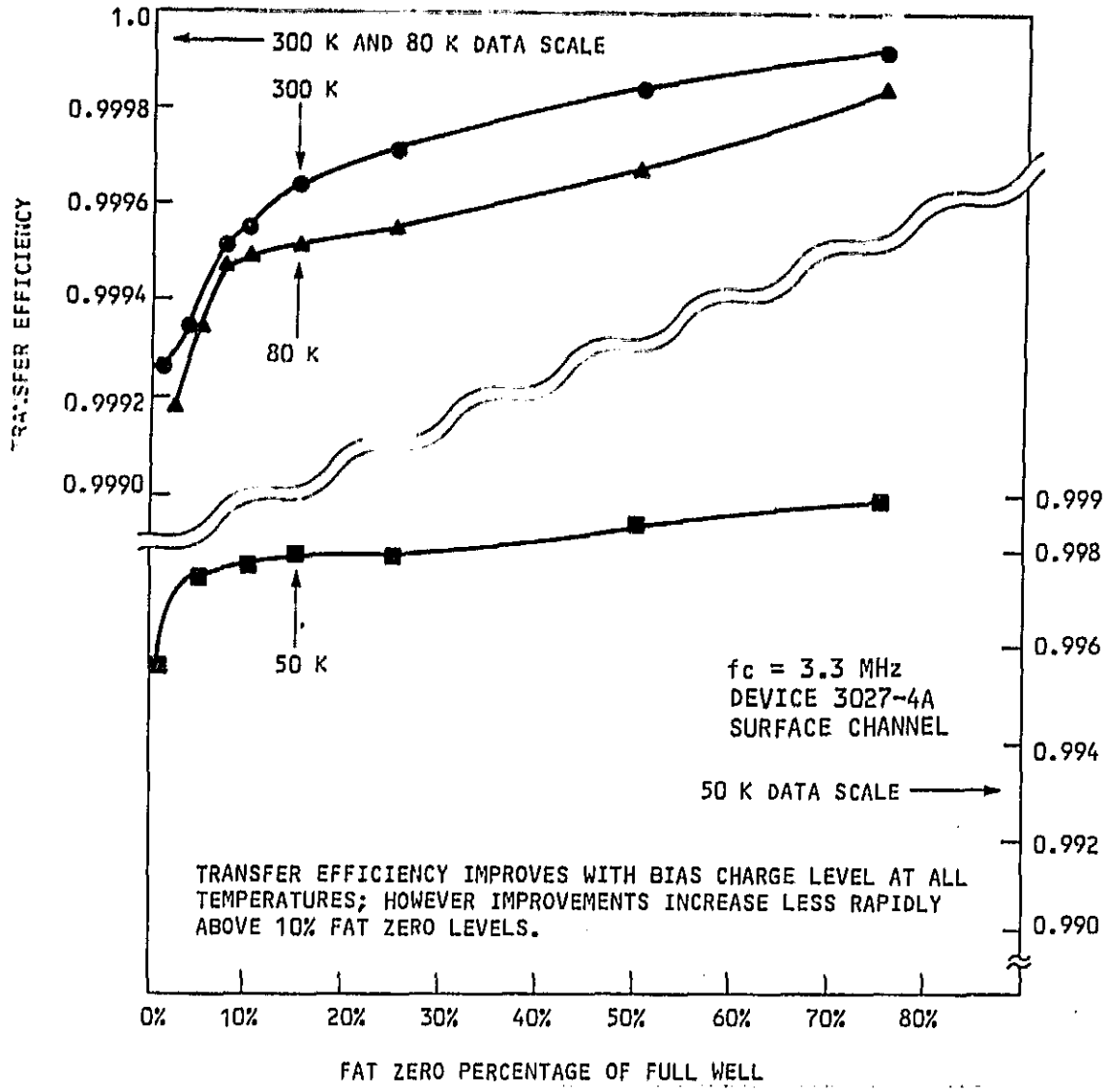


Figure 5-4. Surface Channel Transfer Efficiency: Fat Zero Dependence

- Minimize number of transfers
- Use minimum geometry gate sizes
- Use surface channel for operation below 50 K
- Use buried channel for operation above 80 K
- Use moderate readout rates (suggest <100 kHz)
- Maximum CCD charge to voltage output gain

Finally, an estimate of the transfer noise expected on a 64 x 64 staring array designed for space applications is shown in Table 5-3.

The estimate is obtained by properly scaling the measured transfer noise data which depends on the square root of the number of transfers and

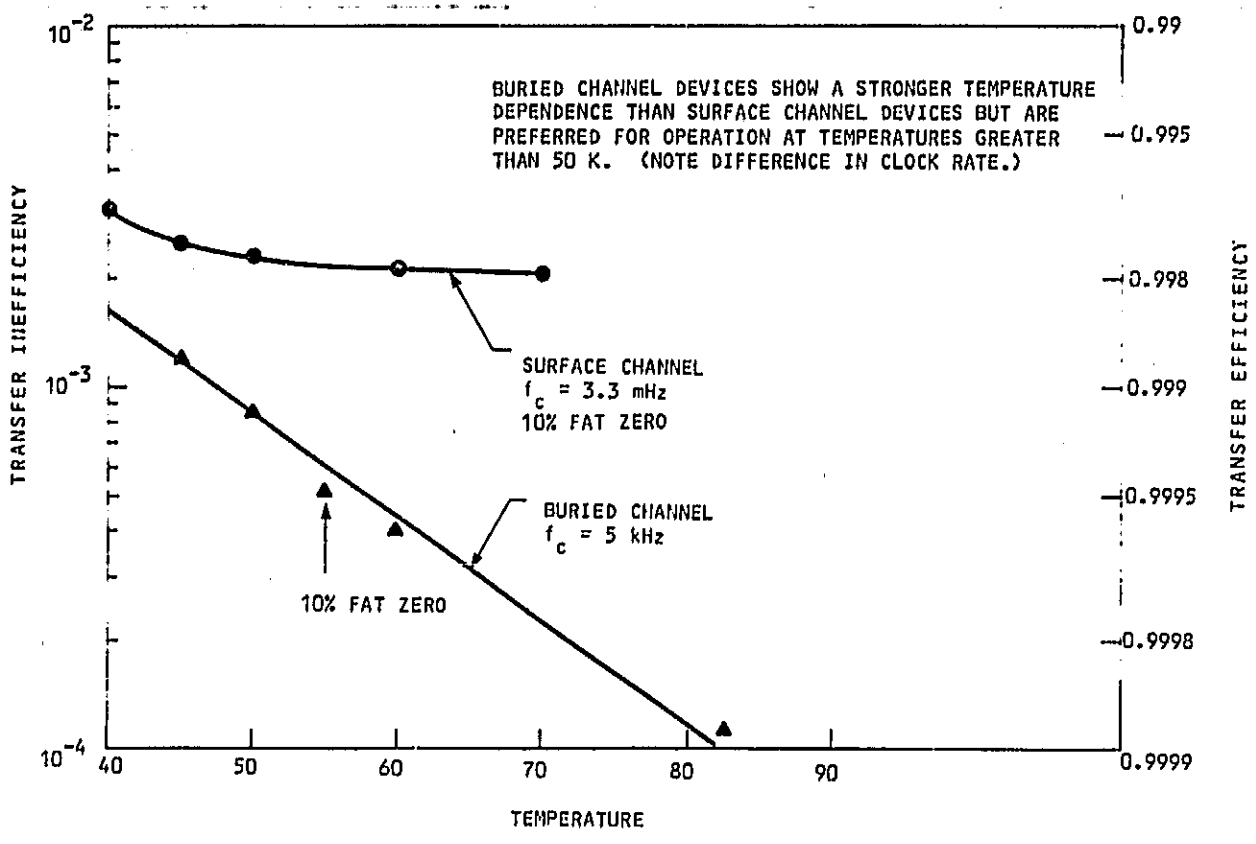
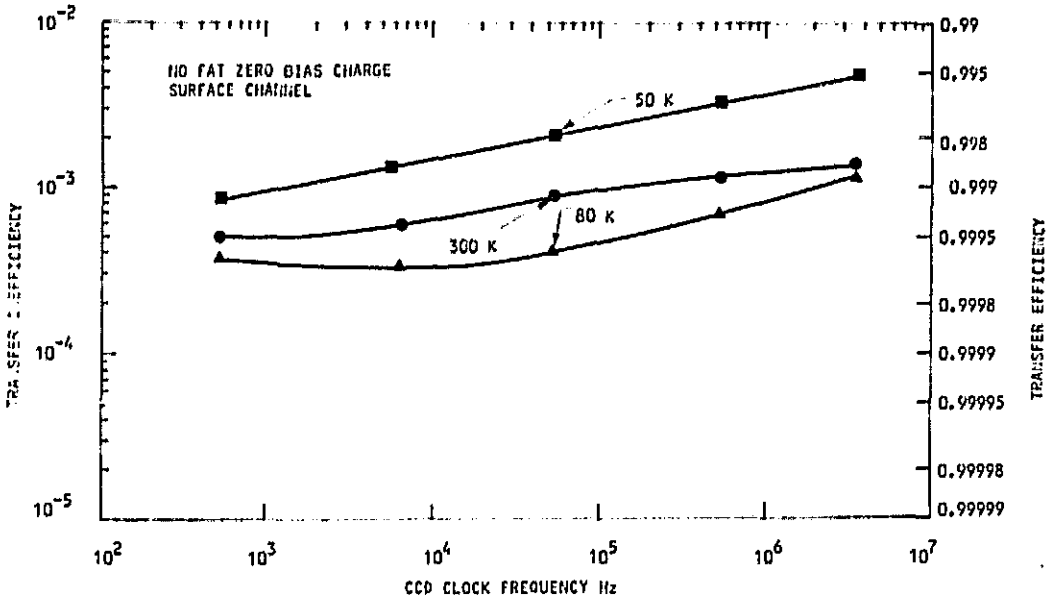


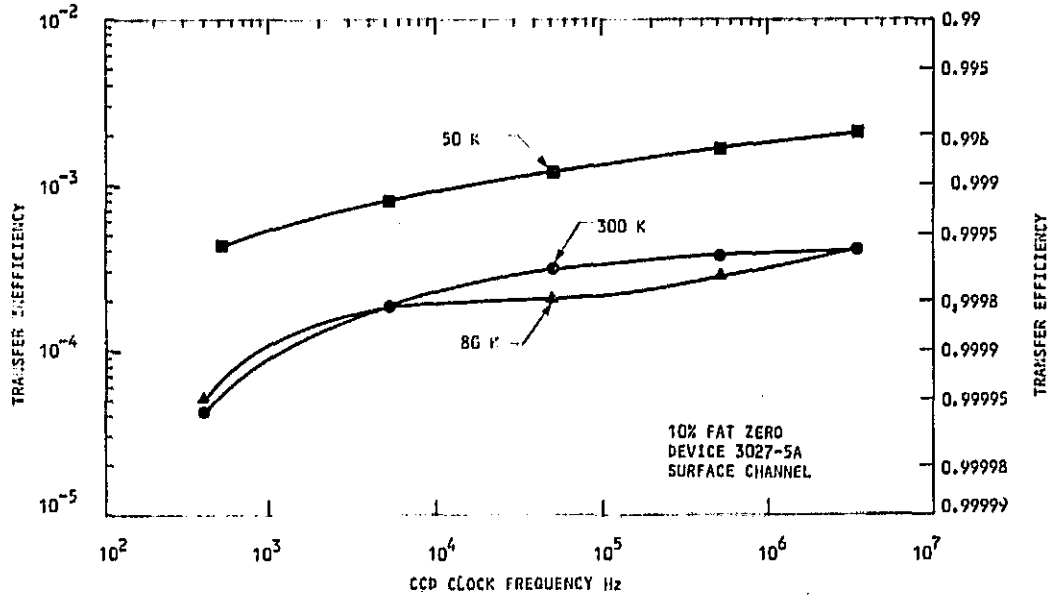
Figure 5-5. Transfer Efficiency Temperature Dependence

approximately the square root of its charge capacity. For the 64 x 64 array the maximum charge capacity is 1 x 10^6 electrons and the maximum number of bits that the signal must be transfered is 128. The analysis indicates that less than 600 rms noise electrons are generated at 60 K due to the readout process. By using preamplification of the signal at the CCD input, as intended with the proposed RGC approach, the noise level can be made virtually insignificant to the total noise of the system.



TRANSFER EFFICIENCY IS REDUCED FOR 50K OPERATION BUT CAN BE INCREASED THROUGH ADDITION OF A FAT ZERO BIAS CHARGE AND THROUGH REDUCTIONS IN CLOCK RATE

Figure 5-6. Transfer Efficiency Dependence on Frequency and Temperature



TRANSFER EFFICIENCY IS REDUCED FOR 50K OPERATION BUT CAN BE INCREASED THROUGH ADDITION OF A FAT ZERO BIAS CHARGE AND THROUGH REDUCTIONS IN CLOCK RATE

Figure 5-7. Transfer Efficiency Dependence on Frequency and Temperature

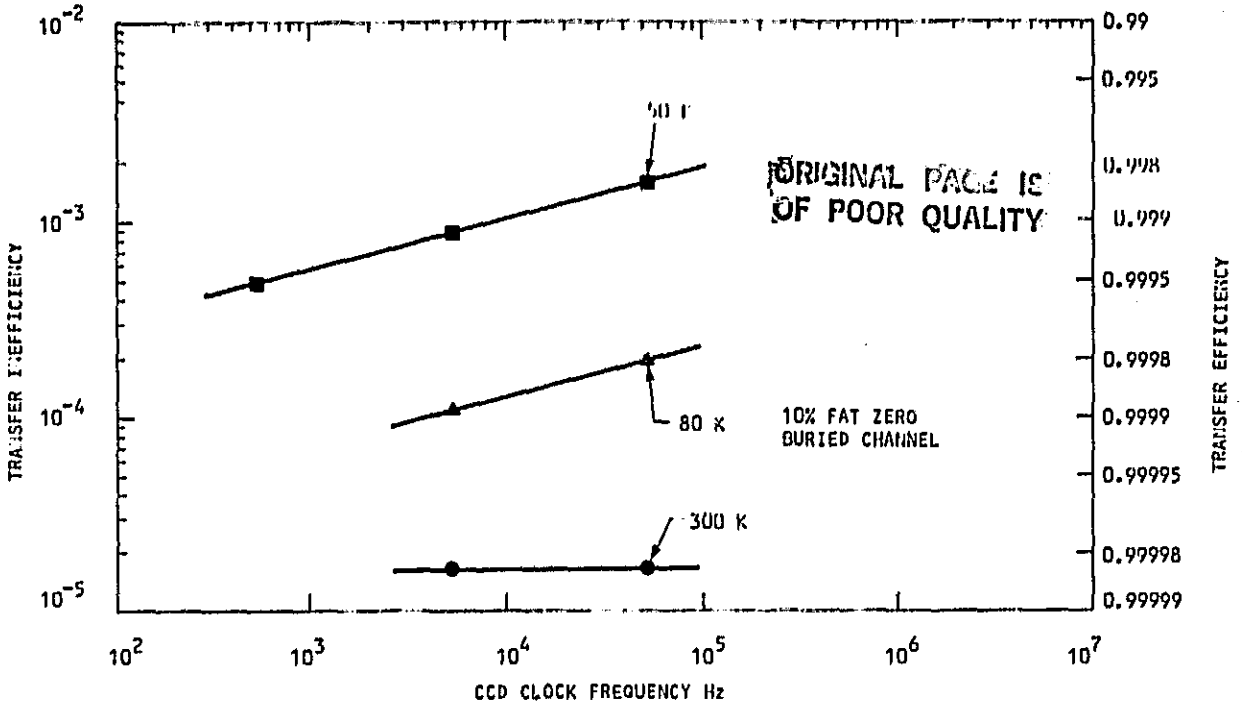


Figure 5-8. Transfer Efficiency Dependence on Frequency and Temperature

Table 5-2. TRANSFER EFFICIENCY DATA

Conclusions

- Functional CCD operation obtained down to 35 K
- Use of fat zero charge improves transfer efficiency at all temperatures
- Transfer efficiency for both surface and buried channel devices decreases with temperature below 80 K
- Buried channel devices are preferred for operation at 80 K and above
- Surface channel devices are preferred for operation at 50 K and below
- Best transfer efficiency at 50 K on tested devices is 0.9996 at

$$F_C = 500 \text{ Hz and } 10\% \text{ fat zero}$$

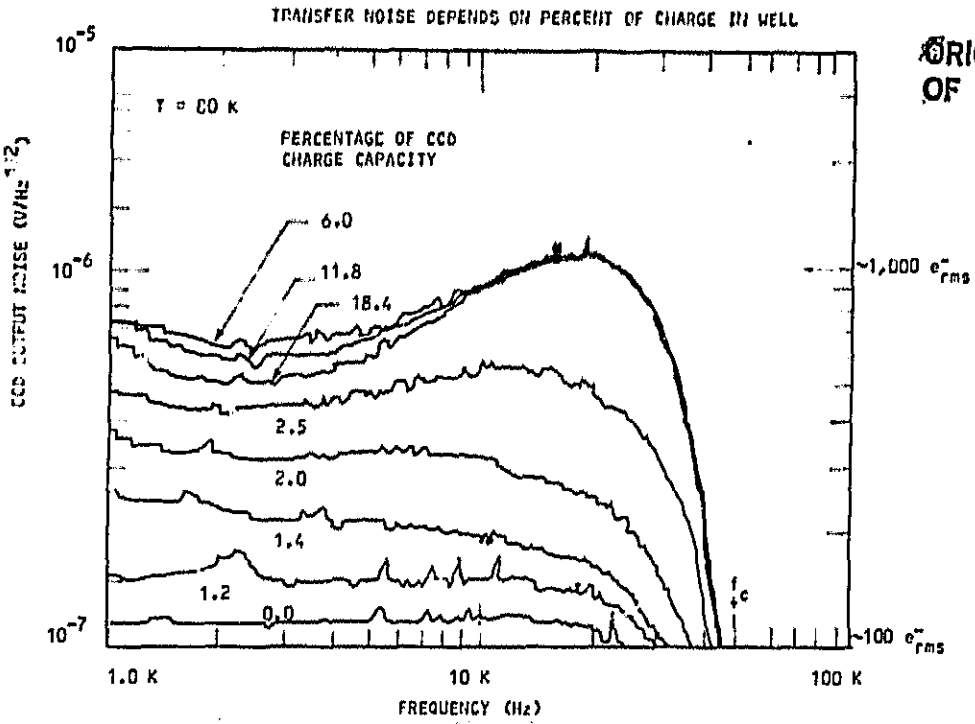


Figure 5-9. 2 ϕ 128 Bit Buried Channel CCD

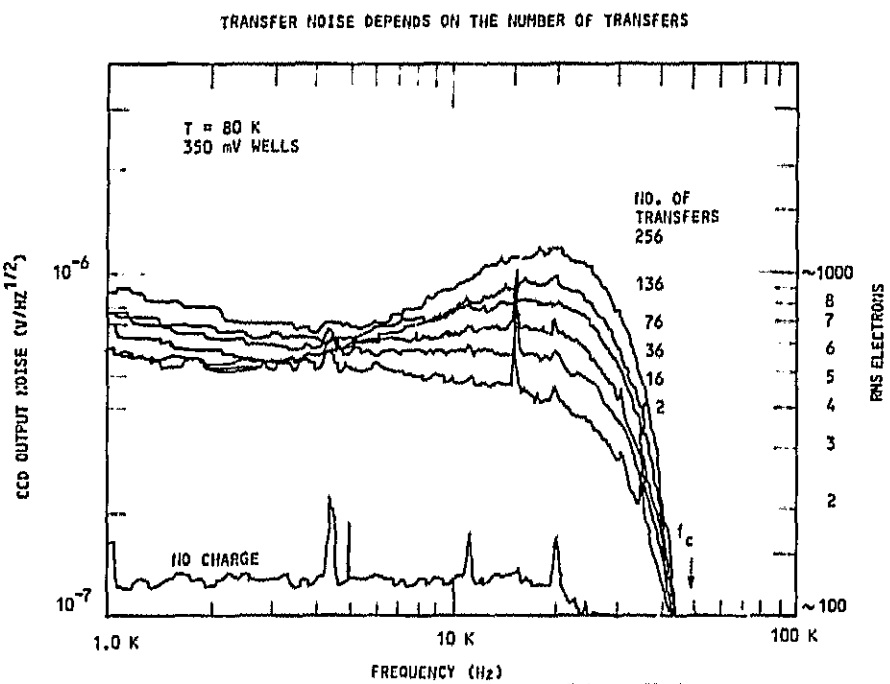


Figure 5-10. 2 ϕ Buried Channel CCD Transfer Noise

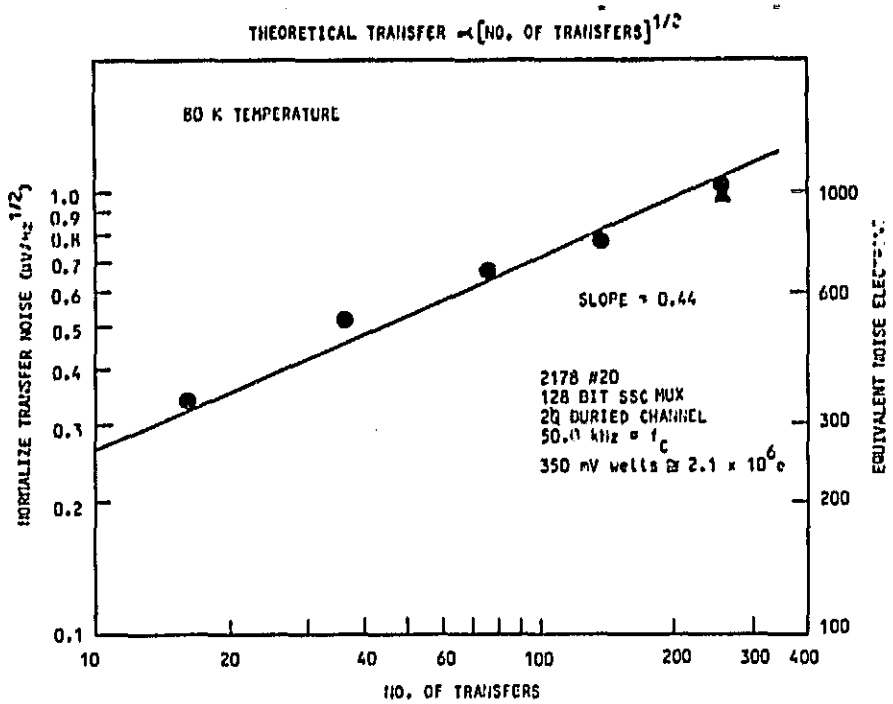


Figure 5-11. 2 ϕ Buried Channel Transfer Noise

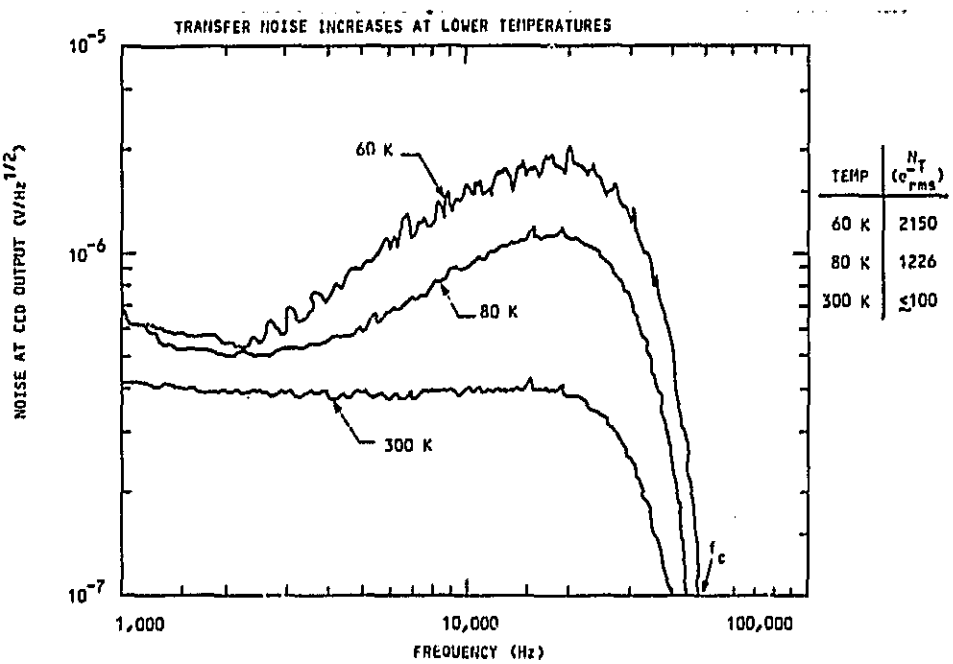


Figure 5-12. 128-Bit Buried Channel Transfer Noise

Table 5-3. NOISE MEASUREMENT OF 3027 CCD INDICATES UPPER LIMIT

Fill and Spill into Parallel Fat Zero Inputs (0.5V Wells)
Channel Frequency 55 kHz

Readout Noise (e_{RMS})

Channel	300 K	80 K	60 K	35 K
#1	390	395	-	-
#4	-	-	848	-
#5	-	-	-	1,420
#19	-	-	-	1,938
#20	455	570	875	-

Readout Noise Increases at Lower Temperatures

Table 5-4. ESTIMATE OF EXPECTED READOUT NOISE FOR A LOW BACKGROUND 64 x 64 STARING CCD

Maximum Number of Transfers: 128 Bits
Charge Capacity: 1 x 10^6 Electrons

	Temperature		
Channel Type	300 K	80 K	60 K
Surface Channel (Readout Noise)	205	257	394
Buried Channel (Xfer Noise)	100	289	507

These noise levels become insignificant when RGC input with current gain is used.