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THE SYSTEM OF EAS TIME ANALYSIS

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ABSTRACT

In studying the extensive air showers (EAS) it is important to have information for determining the EAS front shape, angle of incidence, disk thickness, particle distribution along the shower, on the delayed and EAS front advancing particles. The suggested system of the EAS time analysis allows one to determine the whole EAS longitudinal structure at the observation points. For this purpose the whole information from the detectors is continuously recorded in the memory with the memory cell switching in 5 ns, this enabling one to fix the moment of pulse input from the detector with an accuracy to ± 2.5 ns. Along with the "fast" memory, a "slow" memory with the cell switching in 1 μs is introduced in the system, this permitting one to observe relatively large time intervals with respect to the trigger (master) pulse with an appropriately lower accuracy (± 0.5 μs).

The methods of EAS structure analysis used at present are based on measuring the mutual delays between the operations of separate detectors or detector groups. One of the detectors switches on the time counter, and the other switches it off.

The suggested system principally differs from the existing ones by the fact that the information from each detector of the system is recorded continuously in the memory with memory cell switching in 5 ns.

At present, the system model connected to the EAS four detectors is tested on the PION installation.

As the memory capacity of each channel is limited, after filling all its cells (128 in the model) the further information is again recorded in the first cell, then in the second, and so on. Thus, every time moment in the channel memory there is an information on the particles striking the detector for the previous 128 x 5 = 640 ns.

After the input of the trigger, the output of which is determined by the experiment conditions, the memory cells switch for another 320 ns, the readout being feasible after that. The information about all the particles that passed through the system detectors before and after the trigger within ±320 ns is received by the computer. This time range may be extended by increasing the memory volume.

To extend the system possibilities, along with the "fast" memory a "slow" memory with cell switching in 1 μs is introduced in it (the time interval in the model is ±64 μs with respect to the trigger).

Apparatus. The signal from the scintillation detector photomultiplier (PMT) is fed to the amplifier-limiter A (fig.1) located in the close proximity to it, and then over the coaxial cable - to the memory block, where through the peaker P and shaper S is received by two shift registers Rg1 and Rg2.

Simultaneously, from the control unit CU the stable-frequency pulses are received, which in the phase inverter PI are separated into pulses of the same polarity, but out of phase by ½ period, that control the operation of Rg1 and Rg2 (K500UP141).

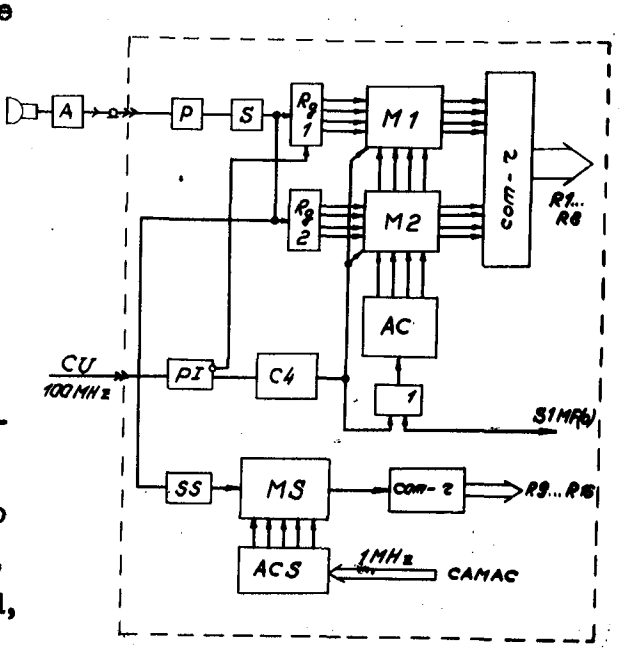

Fig.1. Block diagram of the time channel.

The real frequency of recording rises up to 200 MHz owing to register alternation. The recording from the registers in the memories M1 and M2 (K500PY145) of 64-bit capacity each is realized after filling the registers of 25 MHz frequency. (In the future, with appearance of more speedy microcircuits it will be possible to operate without shift registers and to record the information directly in the memory.) The record permitting pulses are received from the counter C4, and the simultaneous switching of M1 and M2 addresses - from the address counter AC.

The slow memory is organized analogously, but without shift registers. The address counter controlling the MS operation receives 1 MHz stable frequency pulses from the control unit.

The control unit (fig.2) is located in a separate module and is intended for the control of one crate memory blocks.

The quartz generator G produced 100 MHz pulses which are applied to the memory blocks through the key K and splitters. The fast shower master is received by the "stop" input of the control trigger CT. Having counted off 64 pulses of the generator G, the counter C64 closes the key K through the key K1, owing to which the information continues to be recorded in the memory cells for another 320 ns after the fast master input. If during 30 μs the main shower master is not received by the other CU input, then in 30 μs the fast master pulse will be applied to the CT "start" input. The key K

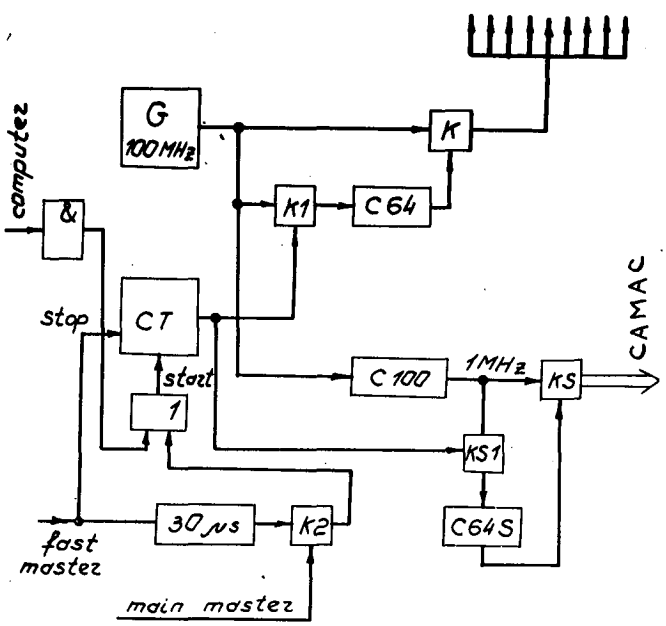

Fig.2. Control unit.

opens and the information from the detectors again starts to be recorded in the memory cells. And the main master input closes the key K2 and the CT remains in the "stop" position until from the computer a record permitting pulse is received that returns the CT to the "start" position.

The receipt of switch pulses to the slow memory is organized analogously. The keys KS and KS1 together with the counter C64S allow to generate 64 pulses more after the fast master input.

In reading, a fixed number of address switching pulses (64) from the computer is received by the same address counters. This allows one to start the readout from the cell in which the information was recorded at the most remote moment of time (-320 ns). The pulse number unambiguously reflects the information advance or delay time with respect to the master, this allowing one to operate without introducing the memory cell addresses and, particularly, the master address, into the computer.

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