HE 6.2-4

DATA ACQUISITION SYSTEM FOR PHASE-2 KGF PROTON DECAY EXPERIMENT

M.R. Krishnaswamy, M.G.K. Menon, N.K. Mondal,
V.S. Narashimham and B.V. Sreekantan
Tata Institute of Fundamental Research
Bombay-400 005, India

Y. Hayashi, N. Ito and Kawakami
Osaka City University
Osaka, Japan

S. Miyake
Institute for Cosmic Ray Research
University of Tokyo
Tokyo, Japan

Abstract

Phase-2 of KGF proton decay experiment using 4000 proportional counters will start operating from middle of 1985. The detection system in addition to measuring the time information to an accuracy of 200 n see also records ionization in the hit counters. It also monitors different characteristics of the counters like pulse height spectrum, pulse width spectrum and counting rate. In this paper we discuss this data acquisition system.

The detector comes under the category of fine-grain calorimeters, in which measurements are made on the ionization of charged particles as they traverse through the detector. This has a total of 375 tons of iron distributed uniformly over an area of 6m X 6m and height 6m. The detector comprises 60 layers of horizontally arranged iron plates (6mm thick) and proportional counters (of cross section 10cm X 10cm and 6m long). The alternate layers of proportional counters are arranged in an orthogonal pattern in order to get both the X and the Y coordinates of the tracks. The main detector is surrounded by a veto shield of proportional counters. This shield is located very close to the rock wall and consist of two layers of proportional counters with 2.54cm of iron in between. In addition to increasing the fiducial mass of the detector, this shield will be very useful to look for other interesting events like Kolar events.

The front end electronics consist of individual amplifier-discriminator chain for data read out and analog multiplexers for monitoring the pulse height. Analog pulses from individual counters are shaped to have uniform decay time constant using a R-C network and are fed to an amplifier of gain 80. The amplified pulses are then passed on

to a discriminator and also to an analog multiplexer. The width of the discriminator output is related logarithmically to the input pulse height and is a measure of ionization in the proportional counter.

The discriminator output pulses are then carried to a data acquisition card (DAC) using flat ribbon cable. There are a total of 60 DAC each one accepting discriminator signals from one complete layer (60 channel). In DAC, the width pulses are provided to the following circuits.

(1) A CMOS static RAM for temporary storage of the width information. These RAMs are being operated as a circular buffer and always contain the history of a channel of the previous 200microsec.

(2) A monoshot to generate fast pulses for trigger.

(3) A priority encoder and a digital multiplexer for monitoring the width pulses.

The fast trigger pulses from individual monoshot are passed on to a set of preprogrammed EPROMs. These EPROMs accept fast trigger pulses from individual channels as their address inputs and produce a set of outputs whenever a layer trigger logic is satisfied. At present three different trigger outputs are available from each layer (i.e. each DAC). These are layer 1-fold (an OR of all the channels in a layer), a layer 2-fold (a 2-fold coincidence among 6 adjacent channels in a layer) and a layer 3-fold (need coincidence of 3 or more adjacent channels). Using these layer trigger pulses a final trigger will be generated in a central trigger processor.

Read out of the stored width data is being done in parallel using eight Z-80 based microprocessors. Each of these microprocessors supervises data acquisition from 8 layers. After receiving a trigger interrupt from the trigger processor, the microprocessors will allow the DACs to continue writing data for a further 187.5 μsec before switching the RAMs to read mode. Since the cycle time of the RAMs is 200 μsec, by this technique 12.5 μsec of pretrigger history will also be available in addition to 187.5 μsec of post trigger history of a channel. Once the readout cycle begins, the microprocessors will transfer the stored width data from the individual RAMs to a central buffer memory. A host computer will finally transfer these data to a mass storage device in a proper format.