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Large-Area Thin-Film Modules

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Abstract

The low-cost potential of thin-film solar cells can only be fully realized if large-area modules can be made economically with good production yields. This paper deals with two of the critical challenges. A scheme is presented which allows the simple, economical realization of the long recognized, preferred module structure of monolithic integration. Another scheme reduces the impact of shorting defects and, as a result, increases the production yields. Analytical results demonstrating the utilization and advantages of such schemes will be discussed.

Introduction

Thin-film solar cells are actively being studied because of their potential as truly low-cost, large-scale, power-generation devices. As a result, there have been significant improvements in the performance of these cells in the last few years. More than 10% conversion efficiency has been reported for at least four material combinations: (CdZn)S/Cu_2S,[1] a-Si,[2] $CuInSe_2$/CdS,[3] and CdS/CdTe.[4] To fulfill the low-cost potential, however, it is not enough to use thin semiconductor films for device construction. Considerable efforts are required in every aspect of cell design and fabrication to ensure that these cells could be manufactured economically. This paper deals with two such aspects: the large area module design and the reduction of detrimental effects due to shorting defects.

Large-Area Module Design

Since solar cells are low-voltage, high-current devices, large-area cells needed for large-scale generation of electricity

cannot be produced by making large-area coatings. Some economic schemes for tapping the electrical output of the cells with minimum Joule losses have to be devised. This is not a trivial problem with thin-film cells, since the conductivity-limiting element is often the electrode layer buried under the thin active layers. Grid electrodes commonly used for bulk single-crystal or polycrystal cells cannot be used. In fact, even in cells whose structure allows the use of grid electrodes, pinhole problems (to be discussed later) make this approach undesirable. Instead, a monolithic integration design is preferred.

In a monolithic integration design, a large-area solar cell is divided into small area elements which are then connected in series. This has the benefit that the voltage rather than the current of the small area elements is added when a large-area cell is made, and it also reduces the current path. Both tend to reduce the Joule loss. The merits of such a design for large-area solar modules have long been recognized.[5-10] With techniques such as photolithography developed for integrated circuits, it is also obvious that, although the process will be rather expensive, the design is technically feasible. The challenge is to design a scheme and a process compatible with the large-scale manufacturing of solar modules at low cost.

Earlier, we presented such a scheme using a CdS/CdTe thin-film cell as an example.[11] This is done by dividing the transparent conductive ITO or SnO_2 coating (Fig. 1a) into electrically isolated, elongated stripes (Fig. 1b). Continuous CdS and CdTe layers are then coated (Fig. 1c), followed by a scribing process designed to expose some of the underlying conductive coating (Fig. 1d). A continuous top electrode layer is then coated, making contact to the exposed transparent conductive layer (Fig. 1e). A third scribing process separates the top electrode layer into stripes, completing the integration (Fig. 1f). Figure 2 shows the perspective view of a completed module.

This scheme using three scribing operations to complete the monolithic integration is attractive because it does not use the expensive photofabrication process. Furthermore, no masking is needed in any of the thin-film deposition processes, and only

one-dimensional registration is required during the scribing steps. The spacial relationship of the three scribe lines also relaxes the registration requirements making the scheme compatible with low-cost production processes.

Scribing can be done by a variety of methods. For the transparent conductive layer, laser scribing is desirable because of its speed and cleanliness, and because of the mechanical hardness of the layer. For the other two cases, however, the necessity to scribe the top layers without damaging the underlying transparent conductive layer and the potential for laser-induced degradation of electrical properties in the semiconducting layers make mechanical scribing more desirable. The CdS/CdTe cell is particularly suitable for mechanical scribing because these semiconductor layers are much softer than the SnO_2 or ITO layers.

Increasing the width of the individual cell elements reduces the fraction of wasted area due to integration but increases the current path and hence the Joule loss. The optimum cell width is therefore determined by seeking a compromise between these two factors. It is easy to show that the power loss due to these two mechanisms can be expressed by

$$P = J^2 R_{\square} L^3 (L + W)^{-1} + PW(L + W)^{-1} \qquad (1)$$

where J and P are the current and power density of the cell at the operating point, respectively; $R_{\square}$ is the sheet resistivity of the oxide layer, W is the width of the wasted region due to scribing, and L is the active width of the cell. Assuming $W << L$, the optimum width of the cell can be expressed by:

$$L = \frac{3}{2}\left(\frac{PW}{J^2 R_{\square}}\right)^{1/3} \qquad (2)$$

For a given kind of cell it is thus determined by the conductivity of the conducting oxide and the amount of area wasted for scribing. The calculated optimum element width and the corresponding

power loss are shown in Figs. 3 and 4 for a sample case of P = 10 mW/cm^2 and J = 18 mA/cm^2.

The Pinhole Problem

Another problem unique to thin-film cells is that of shorting pinholes. This problem arises because thin-film solar cells often use two continuous electrode layers separated from each other only by the semiconductors, which are just a few micrometers thick. Any defects in the semiconductor layers might result in a short between these electrodes, severely degrading the cell performance.

Randomly distributed pinholes can be described by the Poisson distribution:

$$P(x, A, N_d) = \frac{(A \cdot N_d)^x \exp(-A \cdot N_d)}{x!} \qquad (3)$$

where $P(x, A, N_d)$ gives the probability of finding defects in an area A with an average defect density N_d. Thus, the probability of finding a defect-free cell is:

$$P(0, A, N_d) = \exp(-A \cdot N_d) \qquad (4)$$

This probability is thus extremely area sensitive. For example, for a defect density of 0.001/cm^2, the probability of getting a defect-free 1-cm^2 cell is maybe as high as 99.9%, easily leading one to conclude that defect problems do not exist in this thin-film cell system. In fact, however, the probability of producing just a 1000-cm^2 cell is less than 37% (Table 1).

Table 1. Yields of Pinhole Free Cells

	Pinhole Density, cm^{-2}			
Area, cm^2	0.001	0.01	0.1	1
0.1	99.99	99.9	99	90.5
1	99.9	99	90.5	36.8
10	99	90.5	36.8	5×10^{-5}
100	90.5	36.8	5×10^{-5}	4×10^{-44}
1000	36.8	5×10^{-5}	4×10^{-44}	0

Since large-area cells have to be fabricated in a mass production environment, and care in manufacturing process control can only reduce defect density to a certain limit, it is desirable to devise a scheme that would reduce the detrimental effect of defects if they do exist. The scheme has to be compatible with low-cost processes also. The use of the monolithic integrated scheme accomplishes some of this mission. The area of the module is divided into many elements, which are then connected in series. A defect degrades only the element it resides on and not the whole cell; its effect is thus reduced.

The detrimental effect of defects can be further reduced by a cross-cutting scheme.[12] Basically, an integrated module is indiscriminately divided into many parallel subarrays by cutting, perpendicular to the direction of the scribes for integration, through all the thin-film coatings on the substrate (Fig. 5). The subarrays are electrically isolated from each other except at the two ends, where common electrodes connect them in parallel.

The beneficial effect of cross-cutting can be appreciated from a special example (Fig. 6). A module having 10 cells connected in a series is assumed to have 10 defects strategically placed such that there is a defect in each individual element. The whole module is inoperative because all the elements are shorted. Now if the module is cross-cut into 10 subarrays each containing just one defect, only 10% of the power output from the

module is lost because only one element in each subarray is shorted.

The effect of cross-cutting in a more general case can be analyzed as follows. We assume that all cells behave ideally with their I-V relationship given by

$$I = I_0(\exp \frac{eV}{nkT} - 1) - I_L \qquad (5)$$

where I_0 is the reverse saturation current, I_L is the light generated current, n is the diode factor, e is the electron charge, and k is the Boltzmann's constant. We also assume that all defects behave like perfectly conducting paths, rendering the cell elements on which they reside totally inoperative but not adding any series resistance to the rest of the array.

The defect density has to be in a reasonable range for the cross-cutting to be effective or meaningful. Too high a defect density necessitates cross-cutting the array into such fine divisions that it becomes impractical. It is easy to show that, with such reasonable defect density, for a module of area A consisting of N cells connected in series and divided into M subarrays, essentially none of the M subcells contain more than one defect. Thus a subarray with x defects behaves like one with (N - x) subcells in a series. The I-V relationship of such a subarray can be represented by

$$I = \frac{1}{M}(I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L) \qquad (6)$$

Since an array is constructed of M subarrays in parallel, the I-V relationship of the array is given by

$$I = \sum_{i=1}^{M} \frac{1}{M}(I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L) \qquad (7)$$

where the subscript i denotes the ith subarray.

In practical applications, many of these arrays are connected in parallel. The large number of subarrays involved justifies the use of probabilities and Eq. (7) is replaced by:

$$I = \sum_{x=0}^{\infty} P(x, M, N_d)\{I_0[\exp(\frac{eV}{(N - x)nkT}) - 1] - I_L\} \qquad (8)$$

where x is the probability for finding x defects in a subarray:

$$P(x, M, N_d) = \frac{1}{x!}(\frac{N_d \cdot A}{M})^x \exp(-\frac{N_d \cdot A}{M}) \qquad (9)$$

Given the values for the various constants in Eq. (8), the power output of the parallel assembly can be calculated and compared with that of a defect-free case ($x = 0$, $N_d = 0$).

Such calculations have been carried out using parameters for an idealized thin-film CdS/CdTe solar cell:[3] $I_L = 19$ mA/cm², $I_0 = 5.4 \times 10^{-10}$ A/cm², $n = 1.78$ under 75 mW/cm² of AM2 sunlight. In these calculations the array is assumed to consist of 60 cells in a series. Figures 7 and 8 show the calculated power loss and V_{oc}, respectively, as a function of cross-cutting for several $N_d \cdot A$ values. Figure 9 compares the power loss as a function of $N_d \cdot A$ between an undivided array and one which has been divided into 10 subarrays. The reduction of power loss is substantial, and this reduction is achieved through indiscriminative cross-cutting of the array.

The power loss can be further reduced by increasing cross-cutting, but the marginal benefit decreases. In practice the degree of cross-cutting is determined by a balance between the benefit and the added production costs as well as area lost due to cross-cutting.

Summary

Two simple schemes which improve the potential for low-cost production of large area thin-film solar cell modules have been presented. The analysis was carried out based on thin-film CdS/

CdTe solar cells but the schemes should be generally applicable to other thin-film cells as well.

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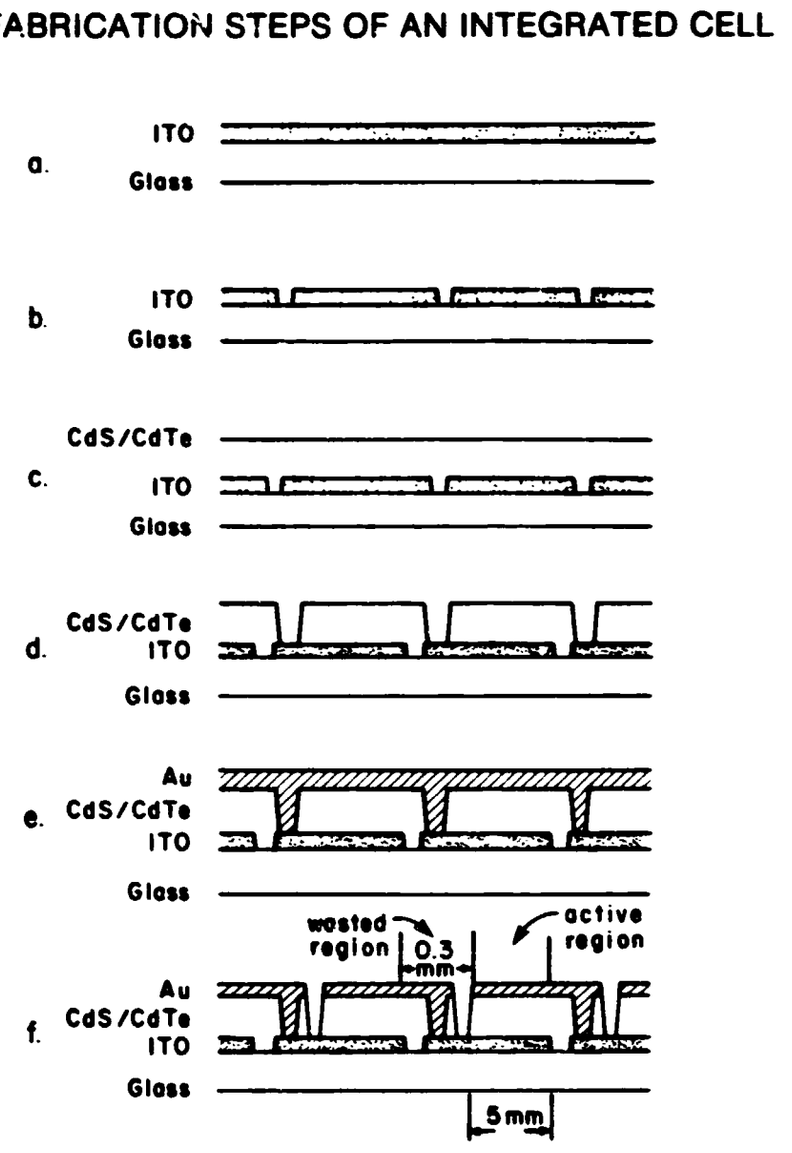

Figure 1. Fabrication steps of a monolithically integrated module.

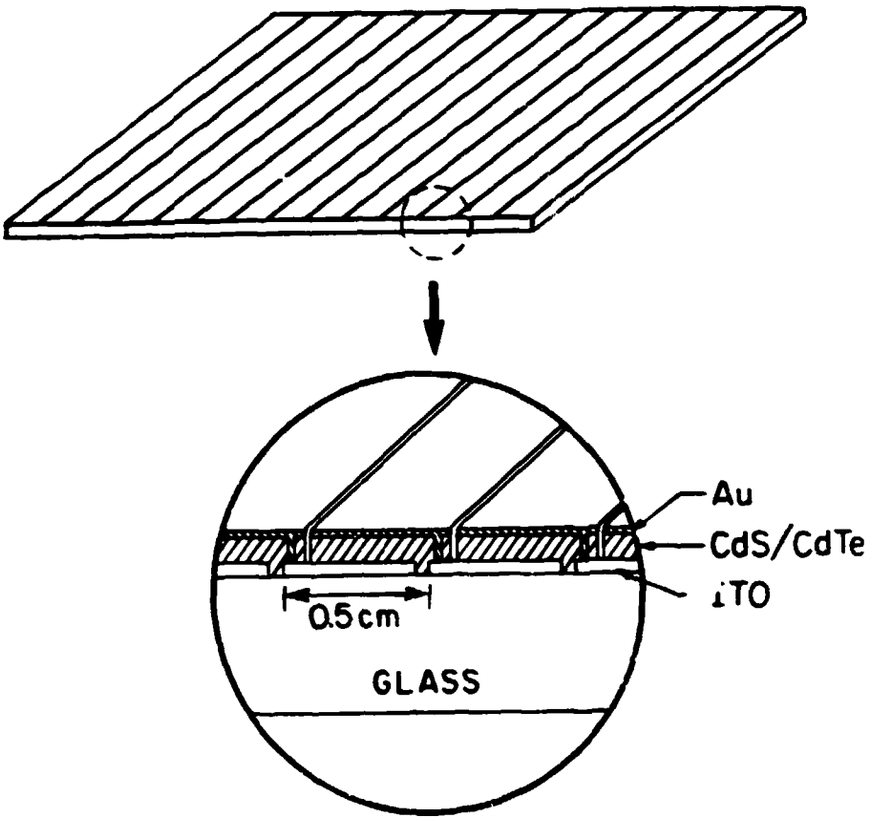

Figure 7. Perspective view of a monolithically integrated CdS/CdTe module.

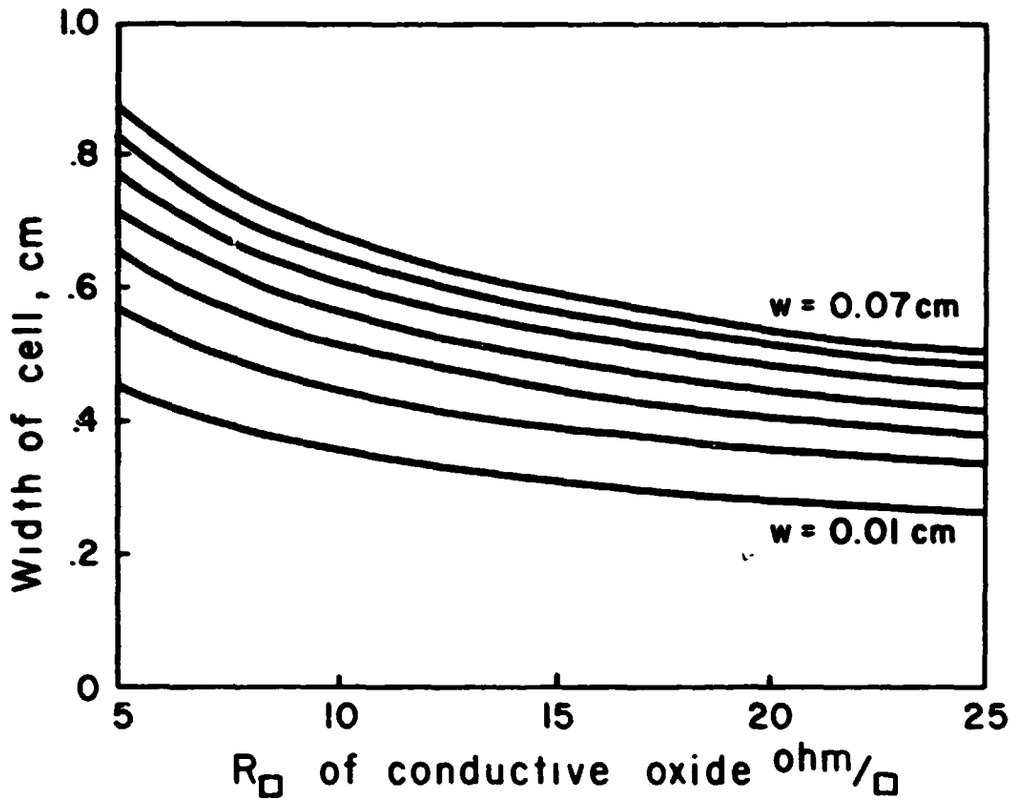

Figure 3. Dependence of the optimum cell width on the resistivity of the conductive oxide layer and the scribing waste.

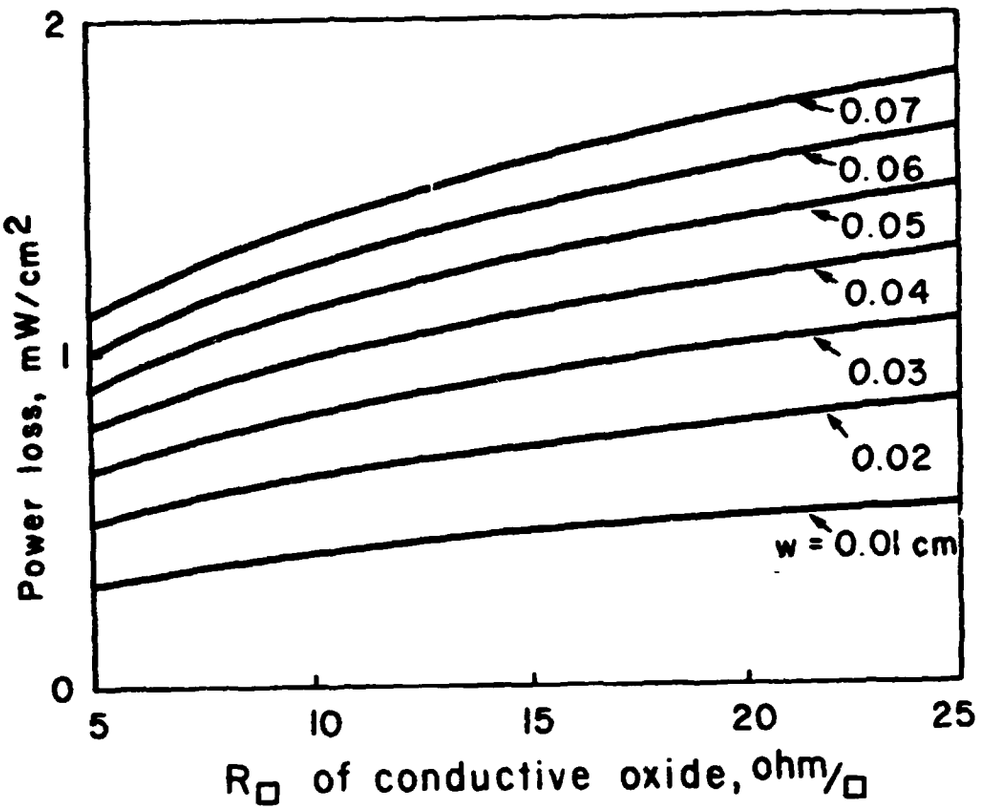

Figure 4. Dependence of the power loss at optimum cell width on the resistivity of conductive oxide and scribing waste.

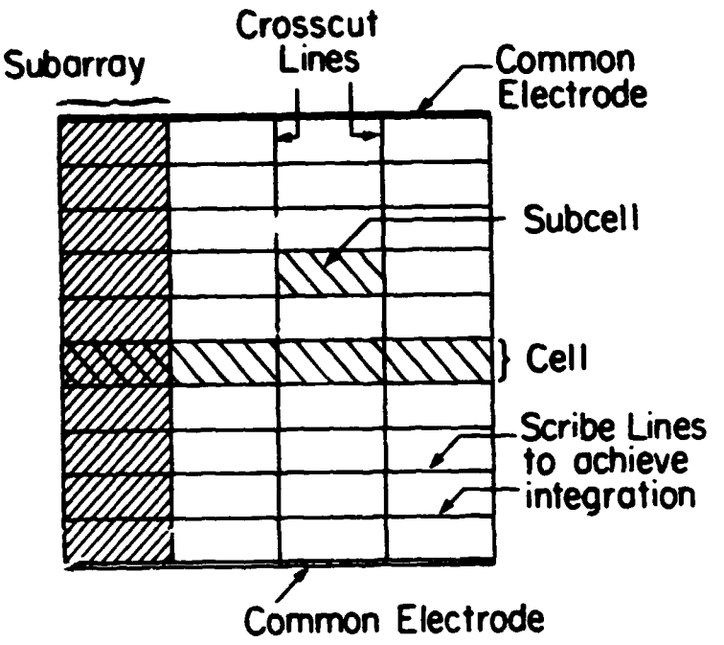

Figure 5. A monolithically integrated array with cross-cuts. The cross-cut lines are scribe lines cutting through all thin-film layers on the substrate.

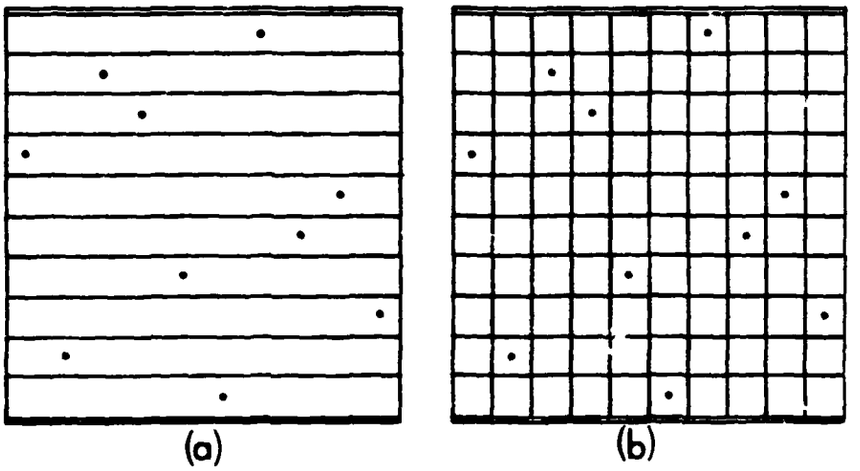

Figure 6. A special example showing the beneficial effect of cross-cutting. (a) Without cross-cutting, all cells in the array have one shorting defect. No output is expected from the array. (b) With cross-cutting, one cell in each subarray has a shorting defect. Only 10% of the power is lost due to defects.

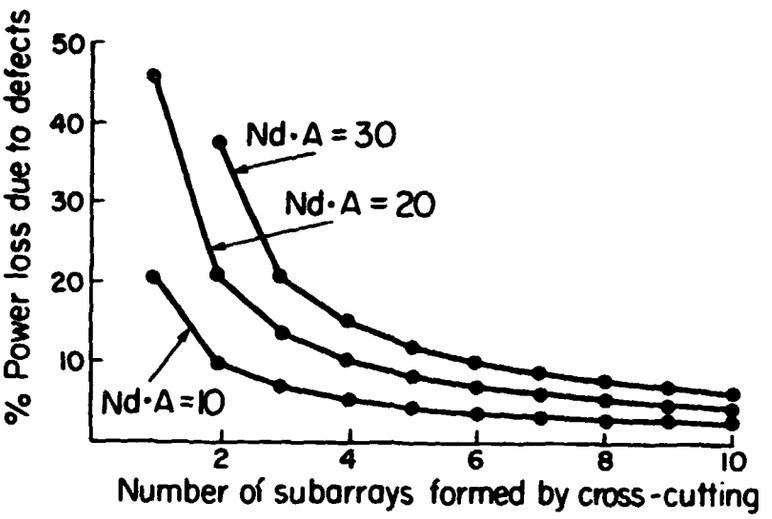

Figure 7. Effect of cross-cutting on the defect-induced power loss of an integrated array consisting of 60 cells in series.

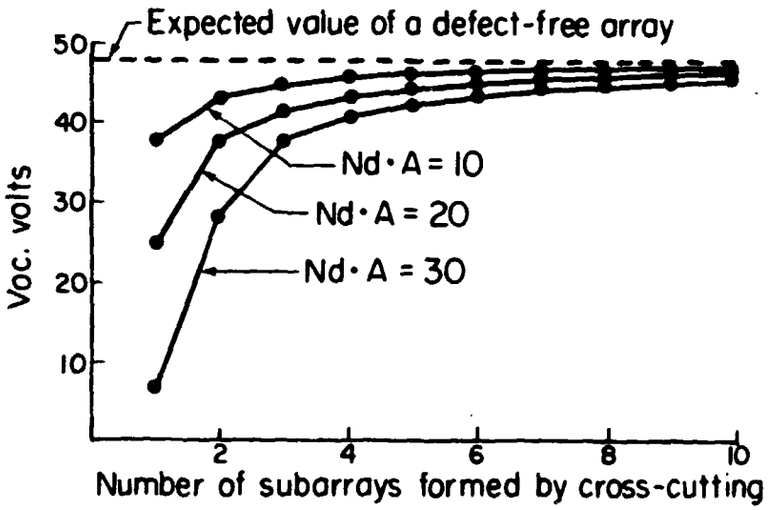

Figure 8. Effect of cross-cut on the voltage output of an integrated array consisting of 60 cells in series.

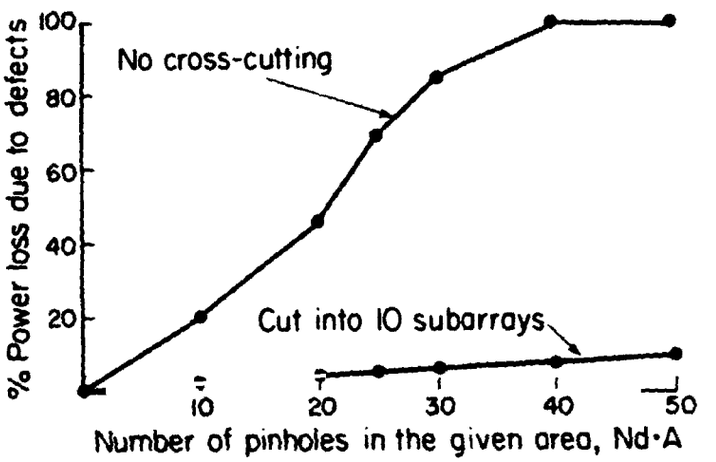

Figure 9. Percentage power loss due to shorting as a function of defect density for an array of 60 cells in series.

DISCUSSION

LESK: Are these shorts just through the cad sulfide, which is about a hundred times thinner than the cadmium telluride, or do you have to go all the way through both layers and short cold to the ITO?

TYAN: There are all kinds of different shorts. We are in the situation where we are not producing 1 ft^2 cells. We are in the laboratory, so our yield is pretty good, about 99%. We are not actually experiencing a large number of defects. What we are presenting here is a schome that will take care of defects when you make large-area modules. It doesn't really matter what kind of shorts you have.

LESK: Your cad telluride is quite conductive compared with intrinsic amorphous silicon. If you had a short just through the cad sulfide layer, it would make it look like a short all the way through, is that right?

TYAN: Cad sulfide is a semiconductor also. In the process we use the cad sulphide is rather insulated. So, even if we have a direct short between metal and cad sulfide, you still have some contact with resistance, which may or may not be enough when you try to make a module. We still have the shorting problem due to that contact. You can reduce the impact by doing this.

ROYAL: I noticed that there are very high temperatures in the process, where you have a substrate temperature of 600°C or so. Are there any problems in that area?

TYAN: That is the only way we know of making it.

BICKLER: It might be worth pointing out to people who contemplate using this process that Eastman Kodak has patented this design. Am I correct?

YERKES: Why don't you go ahead and make a 1 ft^2 array? What is holding you up? We've been hearing this from Kodak since 1982. Let's go ahead and do something!