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Bit Error Rate Testing of a Proof-of-Concept Model Baseband Processor

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BIT ERROR RATE TESTING OF A PROOF-OF-CONCEPT MODEL

BASEBAND PROCESSOR

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SUMMARY

Bit-error-rate tests were performed on a proof-of-concept baseband processor developed by Motorola Government Electronics Group, under the NASA 30/20 GHz Technology Development Program.

The BBP, which operates at an intermediate frequency in the C-Band, demodulates, demultiplexes, routes, remultiplexes, and remodulates digital message segments received from one ground station for retransmission to another. Test methods are discussed and test results are compared with the Contractor's test results.

E-2861

INTRODUCTION

In 1979, NASA initiated a Satellite Communications Program (refs. 1 and 2) to develop 30/20 GHz Satellite-Switched Time Division, Multiple Access (SS-TDMA) systems with multibeam and on-board processing capabilities. To develop and assess essential technology, NASA Lewis awarded a series of contracts in 1979 and 1980 for the development and production of proof-of-concept (POC) models of critical communications equipment. One of these contracts was for a POC model baseband processor (BBP) which is shown in figure 1. The BBP is intended for use on-board a SS-TDMA advanced communications satellite to route digital message traffic among antenna spot beams.

This report is an account of testing that was performed on the POC BBP at NASA Lewis, following its delivery in late 1983.

POC BASEBAND PROCESSOR AND TEST EQUIPMENT

The BBP is a special purpose processor intended for use on-board a SS-TDMA Communications Satellite (refs. 3 and 4). It will demodulate, demultiplex, route, remultiplex, and remodulate digital message traffic segments received from one ground station for retransmission to another. As needed to compensate for rain fade, the BBP can also provide for forward error correction (FEC).

When interfaced with an IF matrix switch, the BBP's high-bit-rate modems permit routing traffic between fixed and scanning antenna spot beams. Its low-bit-rate modems are used in conjunction with the narrow spot beam scanning antennas. During each successive frame period (approx 1 ms), a scanning antenna dwells briefly upon each ground spot assigned to it; each spot includes several ground stations. Each active ground station transmits, on one of several available frequency channels, a burst of message segments so timed as to arrive when the satellite's receive antenna dwells looking down at the originating spot. Bursts occur within preassigned time slots. Figure 2 illustrates TDMA spot, frequency channel, and terminal slot organization within a frame.

The BBP employs a store-and-forward message handling strategy, retransmitting message segments one or two frame periods after their arrival. As the satellite's downlink antenna beams scan spots, previously received uplink message segments are transmitted in a sequence so reordered as to arrive at their destination spots during their preassigned time slots. Uplink and downlink message segments continue to flow in the scheduled sequences and time slots for as long as needed to provide demand-assigned connection among ground stations. In this manner, collateral traffic occurs among many pairs of active ground stations until a major change in connectivity is required. A change in connectivity is accomplished by reprogramming of the on-board control registers of the BBP and the scanning beam antenna, from a master control earth terminal.

The POC BBP includes a representative set of uplink and downlink frequency channels; figure 3 shows a simplified block diagram. The baseband core of the POC model is the 4-input port to 4-output port digital routing switch and the associated set of input and output memories shown in figure 3. A set of input (one for each frequency channel) SMSK burst demodulators and output modulators (one per beam) provides for IF uplink and downlink connection to the baseband core. A 550 Mb/s demodulator receives uplink transmissions at a center (IF) frequency of 3456 MHz (bandwidth 830 MHz). It delivers two 275 Mb/s bit streams to the routing switch, one comprised of even-numbered bits and the other of odd bits. The 550 IF channel is space division multiplexed with the remaining uplink channels. A single 110 Mbps demodulator or up to four 27.5 Mbps demodulators share an allocated bandwidth of 166 MHz. The center frequency of the 110/27.5 allocated band is 3345 MHz. The 110/27.5 input memory receives the baseband data and delivers a reclocked data stream of 275 Mbps to the third routing switch input port. Similarly, a 55 Mbps FEC channel receives at an IF signal centered at 3511 MHz in a bandwidth of 166 MHz. The FEC input memory then delivers the reclocked 275 Mbps data stream to the fourth switch input. In addition, for development testing purposes, a set of input and output baseband channels is provided to by-pass the IF links. Control memories, not shown, provide for word-by-word programming of the baseband switch connections and for flagging the expected frame position of burst transmissions for each uplink demodulator.

Special Test Equipment (STE) is provided with the POC model; in figure 4 is shown a block diagram of the STE. It includes message source memory, modulators, IF burst switches, noise source, attenuators, summers, demodulators, and bit error rate test gear. As in the POC model, modems may be bypassed for special test purpose. Also included are a reference oscillator and a timing signal generator.

STE control memories, not shown, provide for continuous output of a frame of message data from the several channel source memories. Also, they coordinate burst switching and the comparison of received and transmitted message data as needed to provide a variety of Bit Error Rate (BER) statistical data.

Both STE and POC are programmed by a desktop computer that interfaces with all subsystems. It can write to and read from all STE/POC control and message data memories. It establishes all input control and message data for any given test configuration, and establishes power levels and signal-to-noise ratios; it also provides for semi-automatic measurements of channel BER. The computer is supported by a flexible disk drive, video display, printer, and plotter; a library of message and control data is provided on flexible disks.

TEST PROCEDURE

POC BBP testing at NASA Lewis consisted entirely of BER measurements. With the exception of a manual calibration procedure, these measurements are performed semi-automatically (ref. 5). Types of BER tests are connectivity, redundancy, baseline, IF power level variation, burst, adjacent channel interference, multichannel, and synchronization. The first two, connectivity and redundancy, are benchmark tests to be performed with Modems bypassed. Connectivity demonstrates zero BER for routing of baseband message data from input to output via several routes. Redundancy demonstrates that a zero BER is maintained when an alternative set of control memories is dynamically substituted during the BER test.

All other BER tests are performed with uplink Modems active. Baseline tests are performed at nominal IF power level; BER is measured both with and without the downlink modems active. In each of these tests, only one uplink channel is active and message data fills the entire frame. An exception is Baseline testing of the FEC channel where uncoded data fills only 50 percent of the uplink frame; for coded data, every frame contains only two 10-word messages.

IF power level variation tests are very similar to baseline tests, except that the downlink modems are by-passed and BER is measured at both higher and lower power levels. In both of these test procedures, the continuous message data in the uplink frame minimizes the requirement on the burst demodulator to acquire and phase-lock to the transmitted carrier frequency.

In the burst test procedures, uplink transmissions occupy a smaller portion of the uplink frame than they occupy in the baseline and power level variation series. Three duty cycles of frame message data represented by maximum, nominal, and minimum (97, 9, and 4 percent, respectively) are used in separate tests of each uplink channel to impose successively more severe demands on the capability of the burst demodulators to acquire and phase-lock to the uplink transmission. In these tests, only one uplink channel is active during each BER measurement.

In Multichannel tests, all uplink channels are active simultaneously, but BER is measured separately for each message. The Multichannel message data format is illustrated in figures 5 and 6. (The same format was used for the connectivity and redundancy tests, where both uplink and downlink modems were by-passed.)

The adjacent channel interference test procedure is designed to assess degradation of BER in one 27.5 Mb/s channel by applying one or two strong adjacent 27.5 Mb/s signals; spacing between channels is adjustable.

A synchronization test series is designed to verify that burst transmissions will be acquired by the burst demodulators if they arrive within ±60 ns of expected arrival time.

Execution of BER tests is quite simple. Testing is facilitated by automatic management of message data, control data, and test execution inputs and outputs required among the BBP, its STE, and the desktop computer based control systems. Required message and control data and test operations programs are stored on flexible disks. Operational procedures are well documented (ref. 5) and only a few manual operations are needed at the front panel switches of the STE/POC to obtain BER measurement results. Figure 7 shows a sample test procedure to test BER of the 27.5-A Mb/s channel for a maximum length burst message (97 percent duty cycle) at nominal input power to the uplink demodulator.

A documented calibration procedure is also performed periodically. It requires measurement of in-band signal and noise power at the front panel of the STE and of total in-band power at the demodulator input port. Correction factors are calculated and entered into the BER test program which controls the signal-to-noise ratio and the level of demodulator input power during automatic BER test.

The tests are organized by input of control and message data from flexible disk files to the STE and the BBP. Figures 5 and 6 illustrate the most complex test message array. A simpler example is a single message in a single uplink-downlink path, with a single message segment of ten 64-bit words. The message data is input to the STE message generator for transmission as the second through eleventh words of the uplink channel frame. The generator repeats this message continuously at the beginning of each frame. Included at the beginning of the message is a two word preamble that is designed to provide information needed by the uplink burst demodulator to acquire bit and word synchronization. Control data is input to BBP control memories that program, word-by-word, the demodulation, demultiplexing, routing, remultiplexing, and remodulation of the message segment. In addition, control data is supplied to the STE to control demodulation, BER counter circuits, and the automatic control of the uplink channel signal-to-noise-ratio and demodulator input power level as the automatic BER test program is executed. Also, a replica of the uplink message is set in STE memory for comparison with the eight word test message received at the BER counter.

TEST RESULTS

Three sets of BER tests have been performed on the POC model. The first and second sets (ref. 6) were done by Motorola engineers and the third set was done by NASA Lewis engineers. The first set was done at Motorola's plant just prior to shipment to NASA Lewis; it culminated a several month period of subsystems integration and adjustment, and constituted a proof-of-concept testing. The second set was a subset of the first; it was done at NASA Lewis, shortly after delivery, and was intended to demonstrate that the POC model was unimpaired after transport to NASA Lewis. In this report, this second set is sometimes identified by its date of occurrence, November 1983.

The third set of tests was undertaken to confirm the first set and, equally important, to provide familiarization with the hardware and operations that would be needed for integration of the POC BBP with a projected Communications Systems Simulator at NASA Lewis. The BER testing at NASA Lewis was performed over a 10 month period. Because of repeated problems with burst demodulators, testing was terminated before complete confirmation of prior test results. A principal difficulty was that the demodulators did not always lock to data transmissions. In some cases, after consultation with Motorola, relatively simple corrective adjustments were made by test engineers. On other occasions, adjustments and repairs at NASA Lewis were made by Motorola technical personnel. Ultimately, detailed examination of a modem pair at Motorola revealed problems that could not be corrected without factory rework. These problems produced phase errors in the demodulator quadrature mixers and bias voltage drifts in Modem LSI circuits. To assure that the BBP could be used as planned in a NASA Lewis communications systems simulator, Motorola recalled a subset of the modems for rework and subsequent refit to the BBP.

All of the BER test data presented here was obtained prior to recall of modems; it is compared with results of prior test sets.

Connectivity and Redundancy Tests

Table I shows the data for BB to BB BER tests on the 110 Mb/s channel for a message sample of 20 billion bits. This is typical of all channels with Modems by-passed and represents a benchmark performance of less than one per billion BER for baseband circuits. Similar tests are made with the multichannel message format shown in figures 5 and 6 to demonstrate routing via several important message paths, and also reordering of word sequences with zero errors; these are the connectivity and redundancy tests.

Baseline Tests

Figure 8 shows baseline test results at NASA Lewis for the odd-275 Mb/s uplink channel; both IF and BB downlink curves are shown. A comparison of results of baseline tests from POC system test results at Motorola, and like tests at NASA Lewis, is shown in table II. Results are shown as E_b/N_0 excess dB beyond the theoretical curve at BER equal to 10^{-6}. In all but three channels, the performance at NASA Lewis was degraded beyond the design goal of 2 dB.

Power Level Variation

In figures 9 through 14, the effect of power level variation on BER is shown for three uplink channels: the 275-odd, 27.5 B, and the uncoded 55 Mb/s channels. Curves from post delivery tests and NASA Lewis POC BER testing are presented. A complete comparison for all three test series and all channels is shown in table III. The performance goal was to be within 2 dB of the theoretical curve (ref. 6) at a BER of 10^{-6}. For 12 of the tests summarized in table III, task VIII results indicate this goal was met, while NASA results indicate excess degradation in a number of cases.

Burst Tests

Figures 15 through 22 show burst performance of uplink demodulators on 27 B, 55 uncoded and coded, and 110 Mb/s channels for the second and third sets of BER tests. Table IV shows a comparison of all three sets of burst test results. There, it is evident that all channel demodulators met the 2 dB goal during task VIII burst testing, but the 55 Mb/s and 27.5 D Mb/s did not meet the goal during post delivery burst testing. In 11 NASA burst tests, the 2 dB goal was not met.

Adjacent Channel Interference Tests

Preliminary BER tests of adjacent channel interference (ACI) are shown in figures 23 through 26. These tests were not completed because they require the use of the 27 B demodulator, whose performance degradation can be seen by comparing figures 23 and 24.

Synchronization Tests

The test results are summarized in table V. A comparison of BER curves at 10^{-6} was made on an uplink message shifted ± 72 ns (corresponding to an early or late arriving message at the demodulator) with an "on time" message reference curve measured in the baseline BER performance tests (see table II). The 110 Mbps and the 55 Mbps channels were the only channels tested for synchronization. The 550 channel was not fully functional in this mode (ref. 4), while the 27.5 B demodulator was unable to synchronize to the early/late messages at nominal input power levels. It was shown, however, that the 110 and 55 Mbps channels tested exhibited no degradation due to the ± 72 ns data shift.

Multichannel Tests

Results of multichannel tests are shown in figures 27 through 30, for the 27, 55, 110, and even -275 MB/s channels. Shown in all figures are the post delivery range of results, "A," and the results of later NASA tests, "B." At the time of the latter tests, as is apparent in figure 27, the shortburst BER performance of 27 B demodulator had already degraded by three orders of magnitude.

CONCLUDING REMARKS

POC baseband processor test results at NASA Lewis were mixed. Generally, the baseband control and message data circuits were error-free as expected, but there were frequent and persistent difficulties with burst demodulators. In some cases, test results at NASA show good agreement with results of formal proof-of-concept tests performed prior to delivery. Contrary to results of formal acceptance testing, there were a large number of demodulator burst test results that did not meet a 2 dB goal. (That is, E_b/N_0 was not within 2 dB of the theoretical curve, at 10^{-6} BER.) Performance of some of the demodulators ultimately became so degraded that they were unable consistently to acquire and lock-up to burst transmissions, particularly at the lower levels of input power. As a result of test experience at NASA Lewis, Motorola recalled a subset of the BBP modems for factory re-work, to make them suitable for use in a projected NASA Lewis communication system simulator.

REFERENCES

1. Sivo, J.N.: Advanced Communications Satellites. NASA TM-81599, 1980.

2. Bagwell, J.W.: A System for the Simulation and Evaluation of Satellite Communication Networks. Communication Satellite Systems Conference, 10th, AIAA, 1984, pp. 172-180.

3. 30/20 GHz Communications System Baseband Processor Subsystem, Task I Report. Motorola Inc., Jan. 1981. (NASA Contract NAS3-22502)

4. Sabourin, D.; and Attwood, S.: 30/20 GHz Communication Systems Baseband Processor Subsystem, Phase I. NASA CR-174632, 1984.

5. Operation Manual, 30/20 GHz Baseband Processor Integrated POC/STE System. Motorola 99-P08696W, Motorola Inc., May 1983.

6. Shaneyfelt, J.: Task VIII Baseband Processor Proof-of-Concept Testing and Analysis. Motorola Inc., Government Electronics Group, Nov. 1983.

TABLE I. - CONNECTIVITY TEST DATA

[Code gen ID: 3; 110 Mb/s channel.]

BER test		
errors=0	no. of bits=4.03E 09	BER=00.00E00
errors=0	no. of bits=4.03E 09	BER=00.00E00
errors=0	no. of bits=4.03E 09	BER=00.00E00
errors=0	no. of bits=4.03E 09	BER=00.00E00
errors=0	no. of bits=4.03E 09	BER=00.00E00

TABLE II. - BASELINE BER PERFORMANCE

[Continuous IF nominal power uplink/ baseband downlink: E/No @ 10^{-6} BER; (theoretical: 10.6; specified: 12.6 or less.)]

Channel	Pre-delivery system test (dB from theory)	NASA test (dB from theory)
275 even	1.3	2.0
275 odd	1.6	2.1
27.5 A	1.9	.7
27.5 B	1.1	2.5
27.5 C	1.5	.8
27.5 D	1.0	2.1
110	1.3	2.8
55	1.3	2.5

TABLE III. - SUMMARY OF I.F. POWER LEVEL VARIATION TESTS

[dB (E/N) from theoretical @ 10^{-6} BER crossing.]

Channel	Goal	Contract task VIII system test (ref. 5)	Accept. test at NASA Lewis	NASA test
275 even @ -25 dBm	2.0	1.8	1.1	2.2
275 even @ -30 dBm	↓	1.3	.8	2.0
275 even @ -35 dBm		1.8	1.4	1.9
275 odd @-25 dBm		1.7	1.0	2.4
275 odd @-30 dBm		1.6	1.4	2.2
275 odd @-35 dBm		2.1	2.9	2.8
27.5 A @-38 dBm		2.2	2.5	2.2
27.5 A @-43 dBm		2.0	1.9	1.1
27.5 A @-48 dBm		1.4	1.2	.9
27.5 B @-38 dBm		1.4	1.7	2.0
27.5 B @-43 dBm		1.1	1.4	2.4
27.5 B @-48 dBm		1.4	1.2	3.6
27.5 C @-38 dBm		2.7	2.7	2.4
27.5 C @-43 dBm		1.5	1.4	1.2
27.5 C @-48 dBm		1.4	1.0	.7
27.5 D @-38 dBm		1.2	2.0	1.6
27.5 D @-43 dBm		1.0	1.7	1.3
27.5 D @-48 dBm		.9	2.5	1.8
110 @-32 dBm		1.0	.9	1.6
110 @-37 dBm		1.3	.9	1.7
110 @-42 dBm		1.5	1.6	2.2
55 uncoded @-35 dBm		1.5	3.3	3.2
55 uncoded @-40 dBm		1.3	3.1	3.2
55 uncoded @-45 dBm		1.5	3.2	3.5
55 coded @-30 dBm, MCDA		1.8	2.8	2.9
55 coded @-45 dBm, MCDA		1.1	2.1	(a)
55 coded @-30 dBm, MCDB		1.9	2.8	2.6
55 coded @-45 dBm, MCDB	↓	1.0	2.1	(a)

[a]Coded tests were not performed at -45 dBm.

TABLE IV. - SINGLE CHANNEL SINGLE BURST TESTS

[dB (E/N) from theoretical @ 10^{-6} BER crossing.]

Channel/burst length	Goal	Contract task VIII system test	Accept. test at NASA Lewis	NASA test
275 even/max.	2.0	1.1	1.1	2.1
275 even/nom	↓	1.1	.8	2.0
275 even/min.	↓	2.0	1.7	2.6
275 odd/max	↓	2.0	1.2	2.2
27.5 A/max	↓	1.7	1.7	1.2
27.5 B/max	↓	1.6	1.7	2.4
27.5 B/nom	↓	1.3	1.7	2.5
27.5 B/min	↓	1.6	2.0	3.3
27.5 C/max	↓	1.6	1.4	1.2
27.5 D/max	↓	1.7	2.4	1.8
110/max	↓	1.1	.8	1.3
110/nom	↓	1.2	1.1	2.2
110/min	↓	1.6	1.3	2.4
55/max	↓	1.3	2.9	3.0
55/nom	↓	1.2	2.9	3.1
55/min	↓	1.5	3.2	3.4

TABLE V. - SUMMARY OF SYNCHRONIZATION TESTS

[Continuous IF nominal power uplink/baseband downlink: dB degradation @10-6 BER.]

Channel	Task VIII system test	NASA test
275 even-early message	Demod unlocked	Demod unlocked
275 even-late message	↓	↓
275 odd-early message	↓	↓
275 odd-late message	↓	↓
27.5 B-early message	0	↓
27.5 B-late message	0	↓
110-early message	0.2	0
110-late message	0.2	↓
55-early message	0	↓
55-late message	0	↓

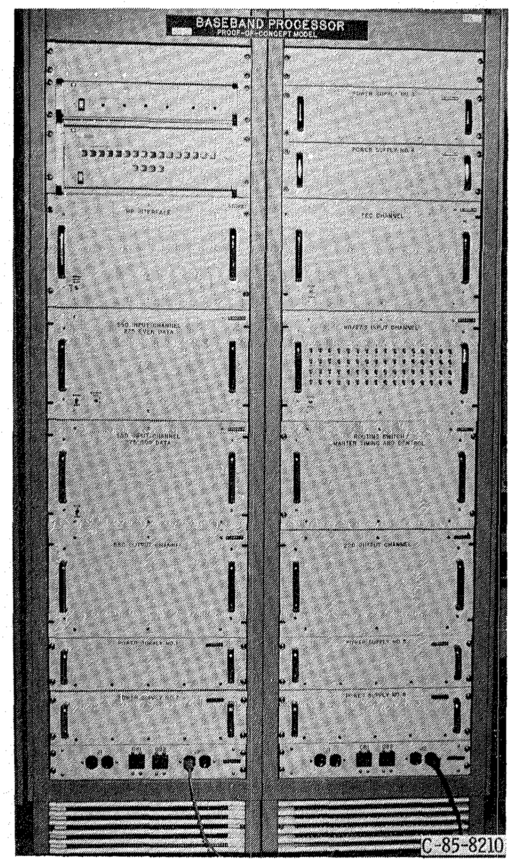


Figure 1. - Proof-of-concept model base band processor.

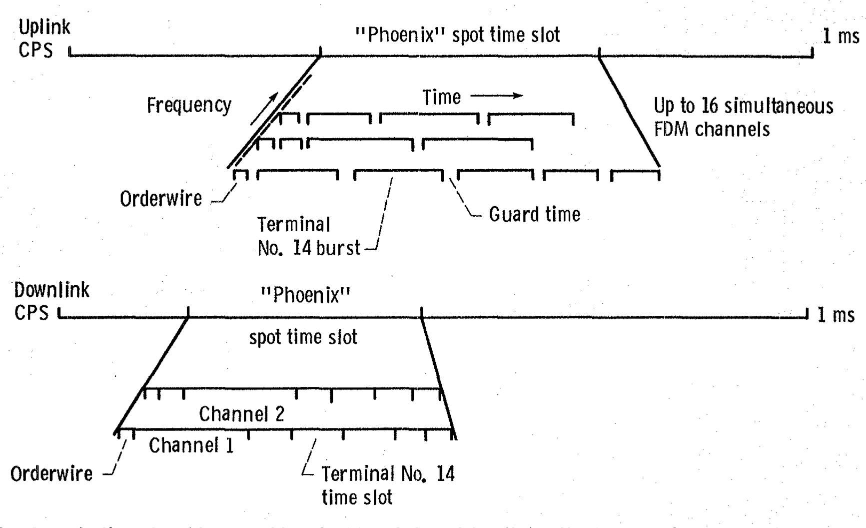


Figure 2. - Organization of spot beam and terminal burst time slots withing the frame period of a FDM/TDMA system.

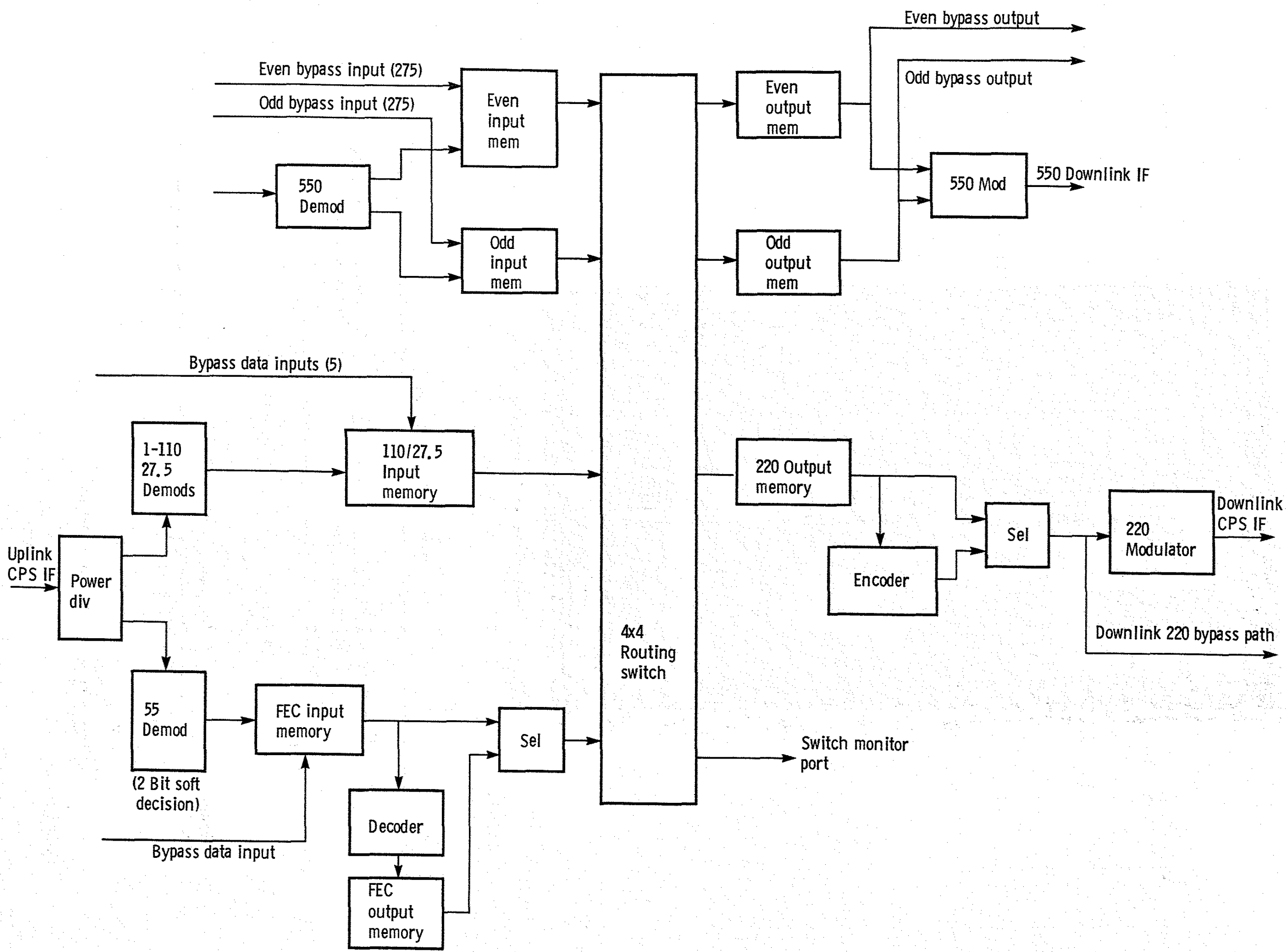


Figure 3. - Simplified block diagram of POC Baseband Processor.

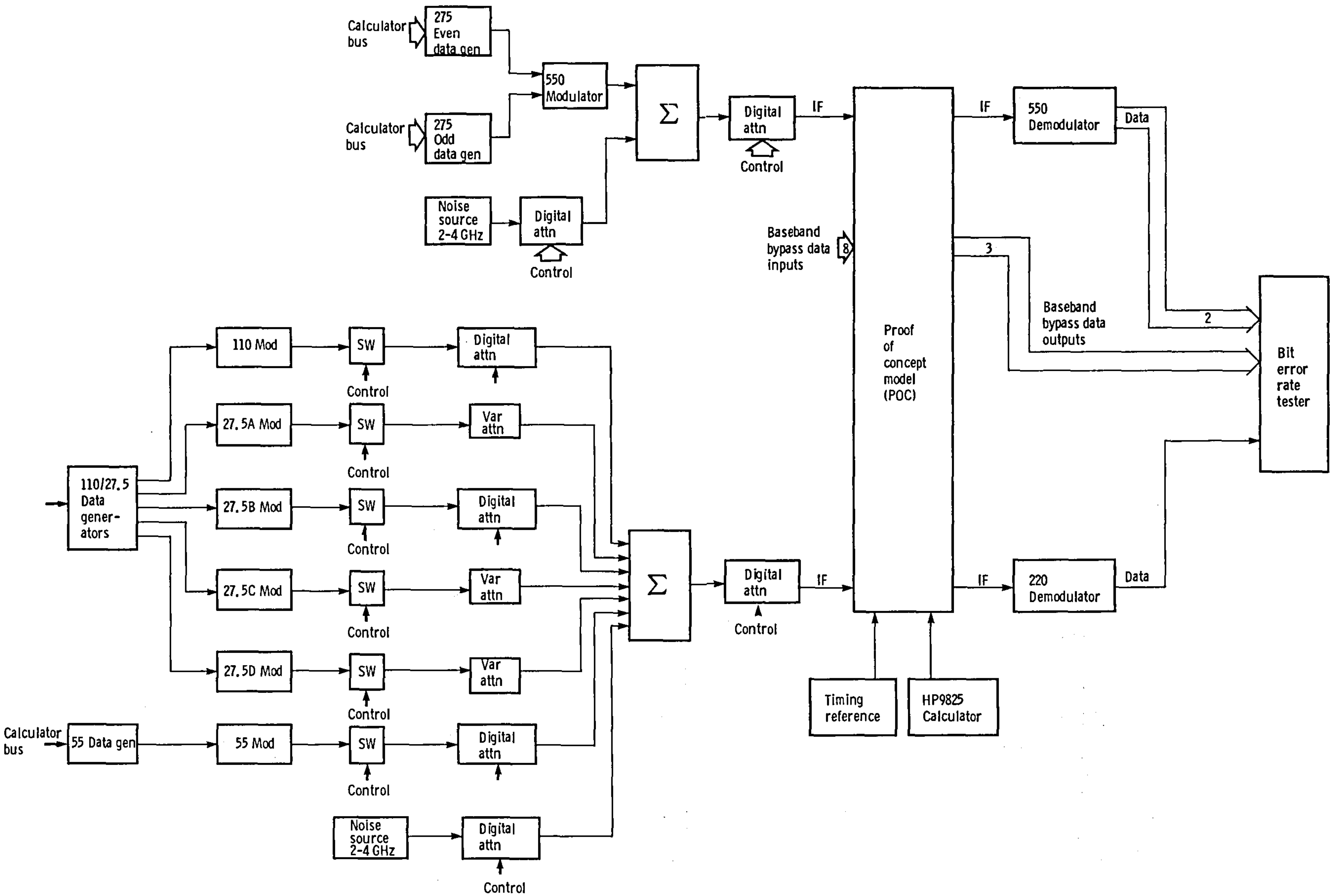
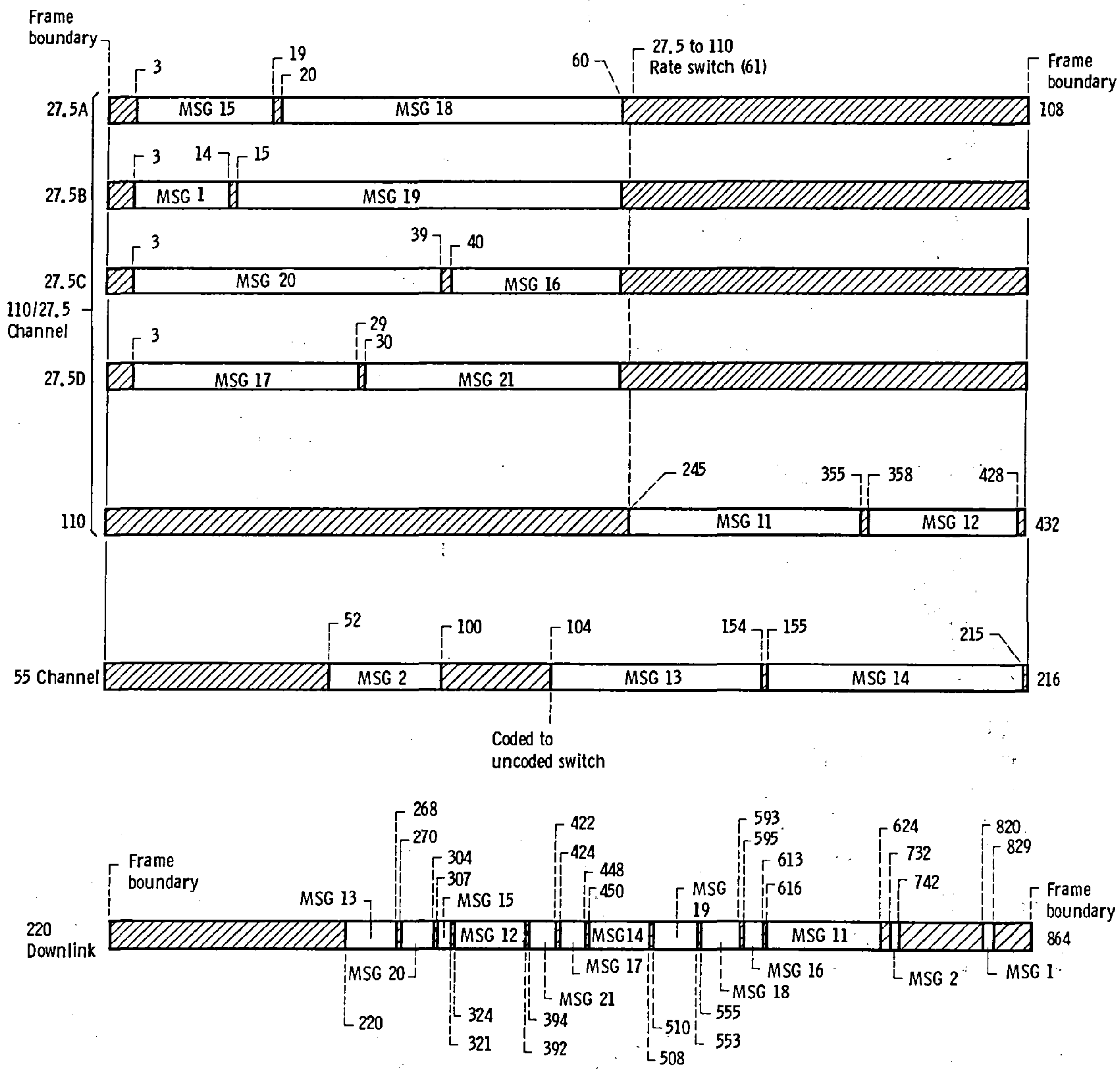


Figure 4. - Simplified block diagram of Special Test Equipment for POC Baseband Processor.



Notes:

(1) Shaded areas represent guard word areas

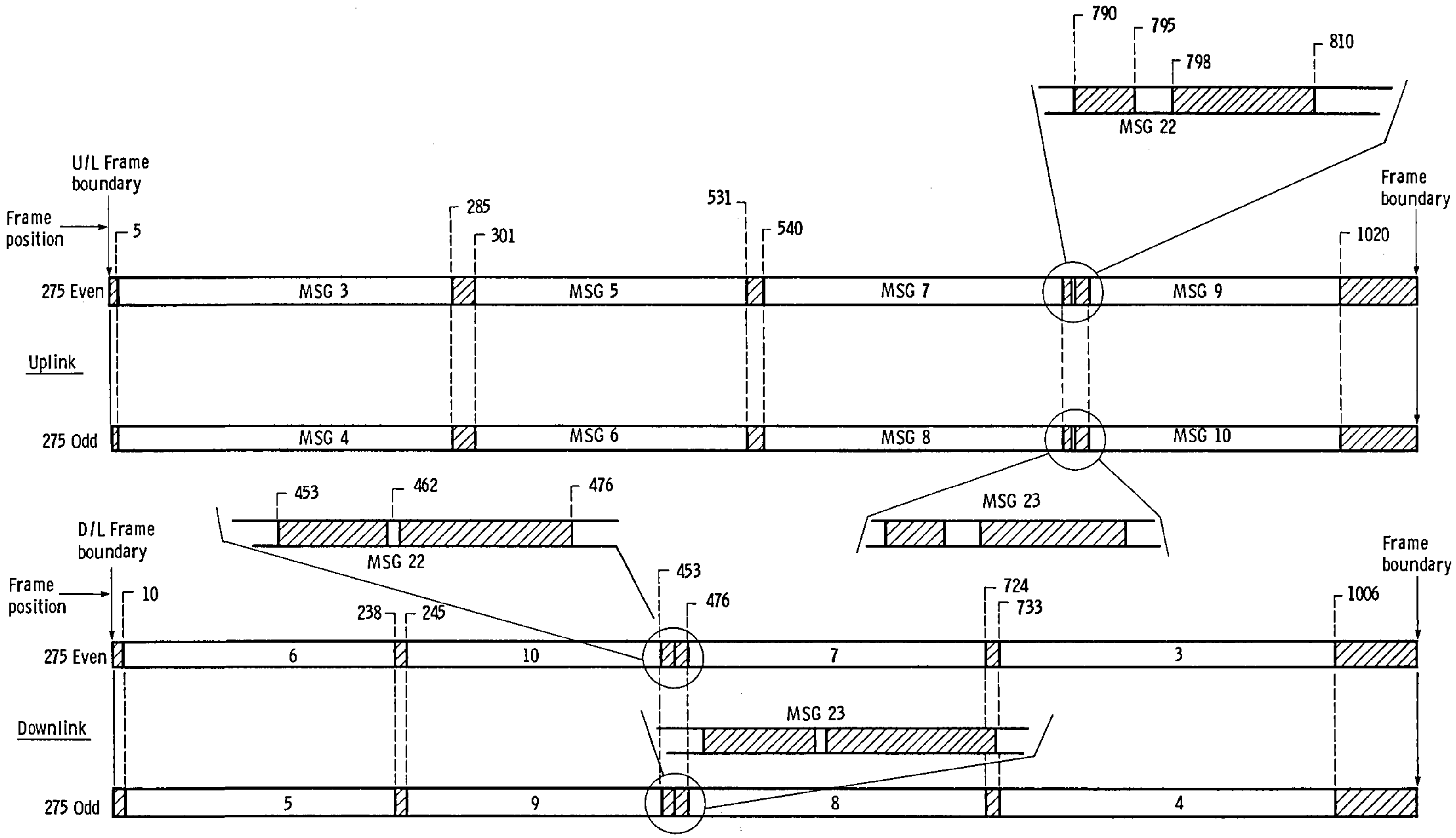
(2) Messages 1, 12, 14, 18, 20, and 21 are mapped into output memory with work order reserved to demonstrate word-by-word routing

(3) Message 2 is coded on uplink

(4) Messages 1 and 2 are coded on downlink

(5) Message length refers to number of words in full message w/preamble

Figure 5. - Multi-channel message format for testing low data rate channels of P. O. C. Baseband Processor.



Notes:

(1) Shaded areas represent guard word areas
(2) Messages 5, 6, 7, and 8 are mapped into the output memories with word order reversed to demonstrate word-by-word routing
(3) Messages on downlink appear two words shorter due to removal of uplink preamble (2 words)

Figure 6. - Multi-channel message format for testing high data rate channels of P. O. C. Baseband Processor.

Coded or Uncoded	U
Label for curve	275 ODD MAX

4.4.2.2.6 Attach paper to test data record. Label page A-6.

4.4.3 *27.5 Quad Demodulator.*

4.4.3.1 *27.5 A Burst BER.*

4.4.3.1.1 Select the following switch positions on the POC:

Drawer	Switch Position
110/27.5 Input	Demod

4.4.3.1.2 Select the switch positions on the front of the STE modulator drawer as follows:

Switch	Switch Position
Power On	ON
Control Source	REMOTE
CPS Noise	ON
Trunking Noise	OFF
CPS RF Output	ON
Trunking RF Output	OFF

4.4.3.1.3 Load the following files into the POC and STE using System Disk No. 6.

Utility	Filename
UPDATE	U27AM
PRESET	P27AM

4.4.3.1.4 With System Disk No. 6 in the disk drive perform a BER test on the 27.5 A uplink at IF and the 220 downlink at baseband with the following commands:

BER BURST	5
Save data on disk?	YES
Enter replica file?	R27AM
Enter BER path	3
Insert Disk with Data File. Continue (System Disk =25)	
Enter message ID	1
Setting BER control memory	
Enter E_b/N_o	5 to 16
Enter IF level	−43
Manual ATTEN entries	NO
Press Start/Status	

At completion of BER test data collection, press STOP and press EXEC (f_o) to exit BER.

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DRAWN	SIZE A	FSCM NO. 94990	DWG NO. 12-P02297W	REV A
ISSUED	SCALE		SHEET 32	

4.4.3.1.5 Plot the BER curve for the data record with the following commands:

Enter current date at the start of EXEC.

		(Default Value)
GRAPH BURST	5	
Enter curve no.	1	(1)
Enter E_b/N_o axis lower limit	4	(4)
Enter E_b/N_o axis upper limit	18	(18)
Enter E_b/N_o axis tic internal	1	(1)
Enter paper width (inches)	8.5	(8.5)
Enter paper length (inches)	11	(11)
Set up 8.5 x 11 inch paper		
Coded or Uncoded	U	
Label for curve	27.5 A MAX	

4.4.3.1.5 Attach paper to test data record. Label page A-7.

4.4.3.2 27.5B Burst BER

4.4.3.2.1 *Full Frame Message Length.*

4.4.3.2.1.1 Load the following files into the POC and STE using System Disk No. 7.

Utility	Filename
UPDATE	U27BM
PRESET	P27BM

4.4.3.2.1.2 With System Disk No. 7 in the disk drive perform a BER test on the 27.5 B uplink at IF and the 220 downlink at baseband with the following commands:

BER BURST	6
Save data on disk?	YES
Enter replica file?	R27BM
Enter BER path	3
Insert Disk with Data File. Continue (System Disk =25)	
Enter message ID	1
Setting BER control memory	
Enter E_b/N_o	5 to 16
Enter IF level	−43
Manual ATTN entries	NO
Press Start/Status	

At completion of BER test data collection, press STOP and press EXEC (f_o) to exit BER.

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DRAWN	SIZE A	FSCM NO. 94990	DWG NO. 12-P02297W	REV A
ISSUED	SCALE		SHEET 33	

Figure 7. - Sample operating instructions for automatic bit-error-rate testing.

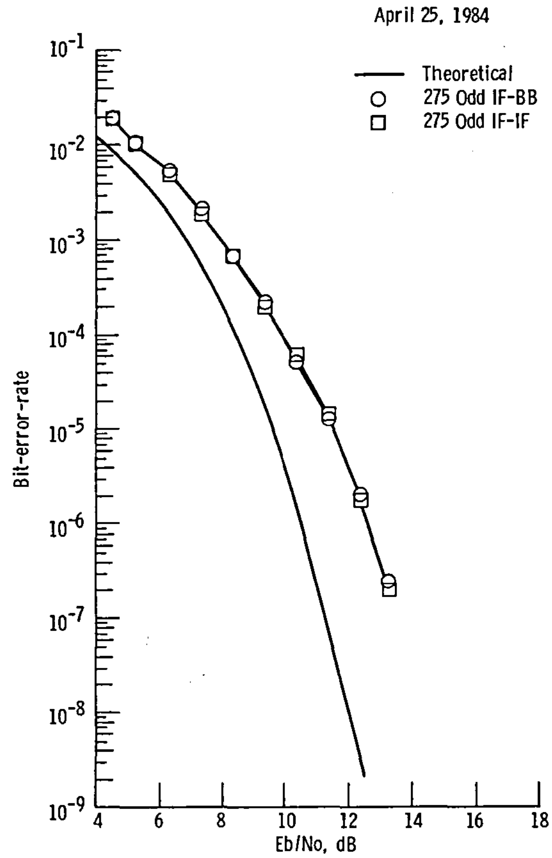

Figure 8. - Ber performance of 275 odd mb/s channel in baseline tests, April 1984.

Nov. 18, 1983

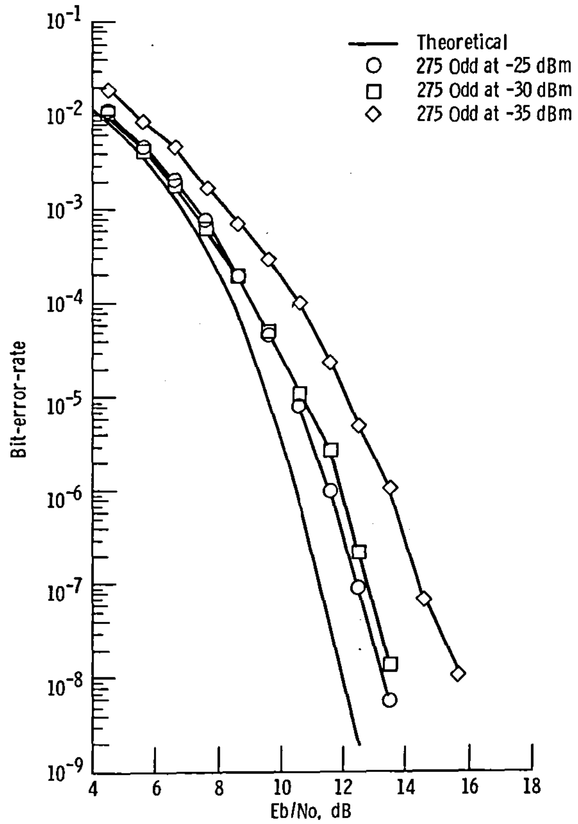

Figure 9. - 275 Odd channel ber performance in I. F. power level variation test, Nov. 1983.

May 22, 1984

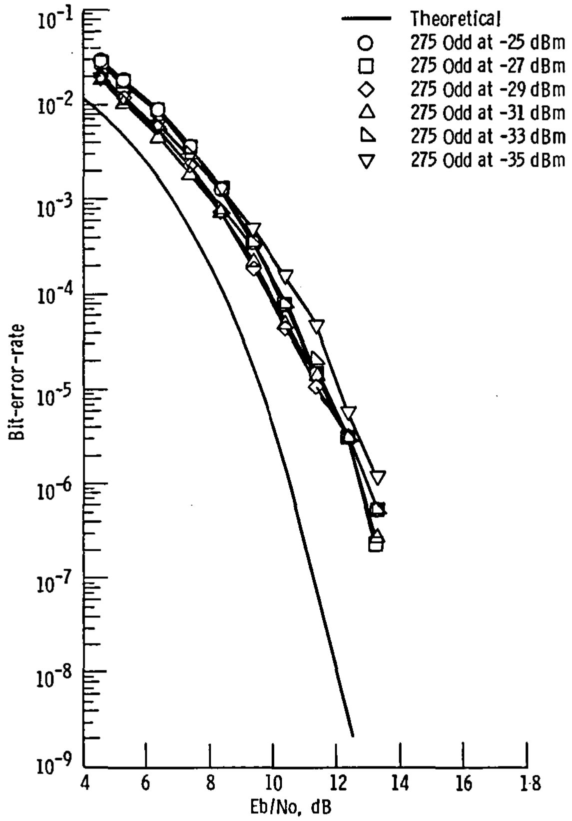

Figure 10. - 275 Odd channel ber performance in I. F. power level variation test, May 1984.

Nov. 18, 1983

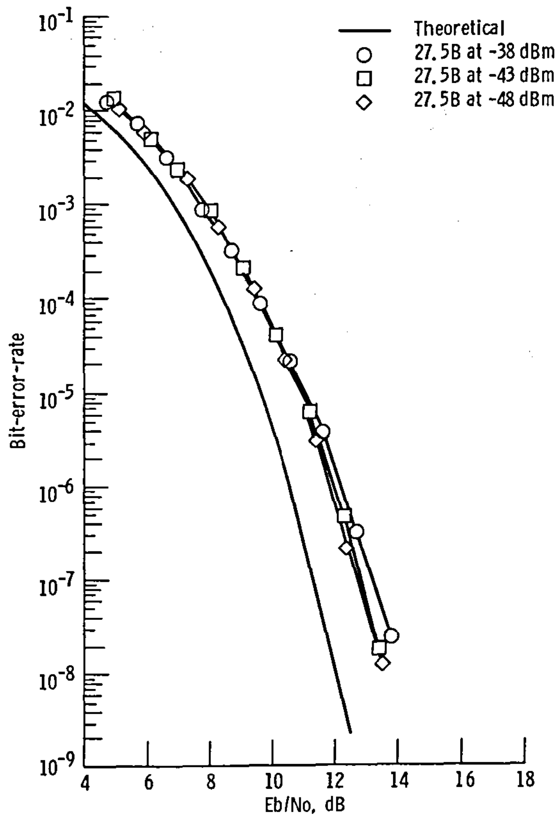

Figure 11. - 27.5B Channel ber performance in I. F. power level variation test, Nov. 1983.

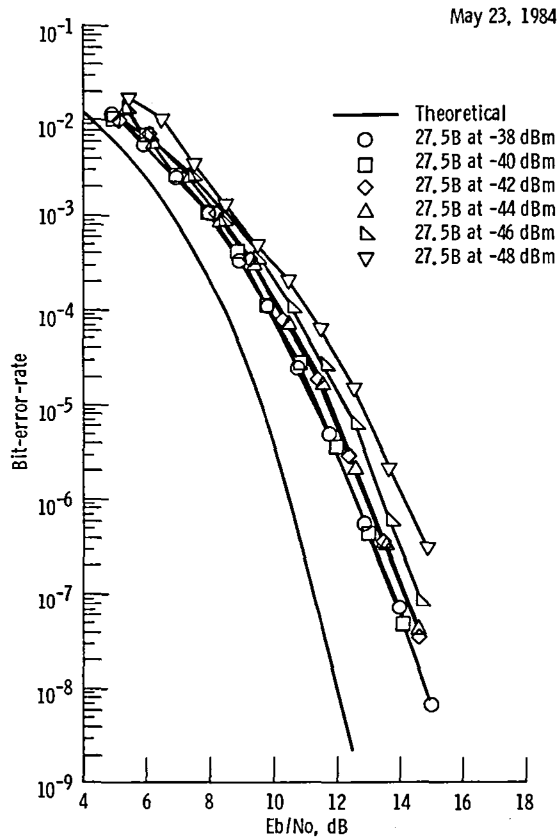

Figure 12. - 27.5B Channel ber performance in I. F. power level variation test, May 1984.

Nov. 22, 1983

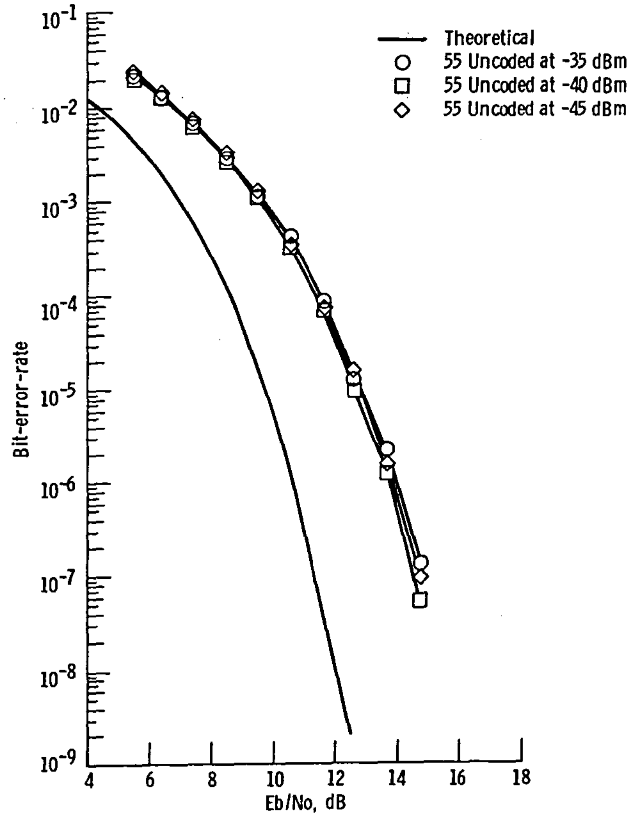

Figure 13. - 55 mb/s Channel ber performance in I. F. power level variation test, Nov. 1983.

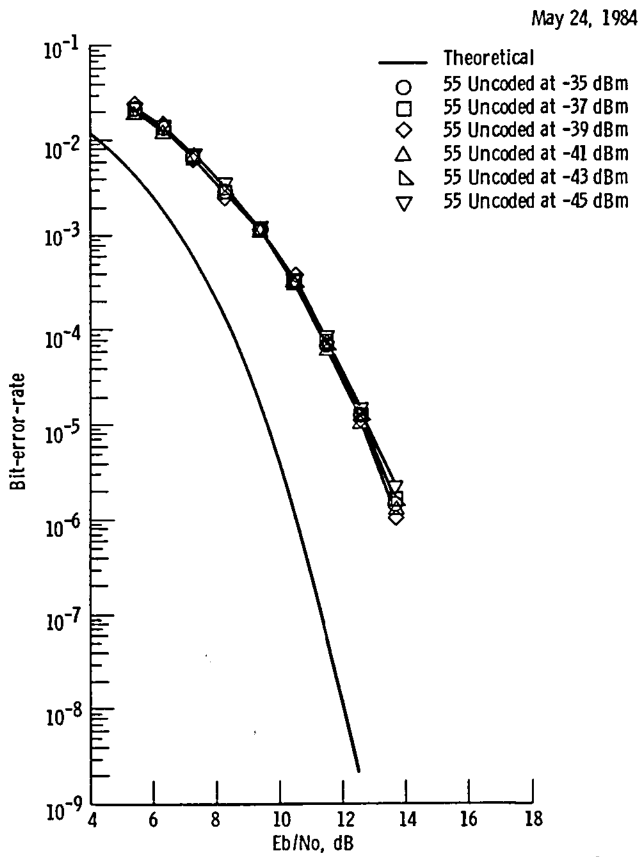

Figure 14. - 55 mb/s Uncoded ber performance in I. F. power level variation test, May 1984.

Nov. 18, 1983

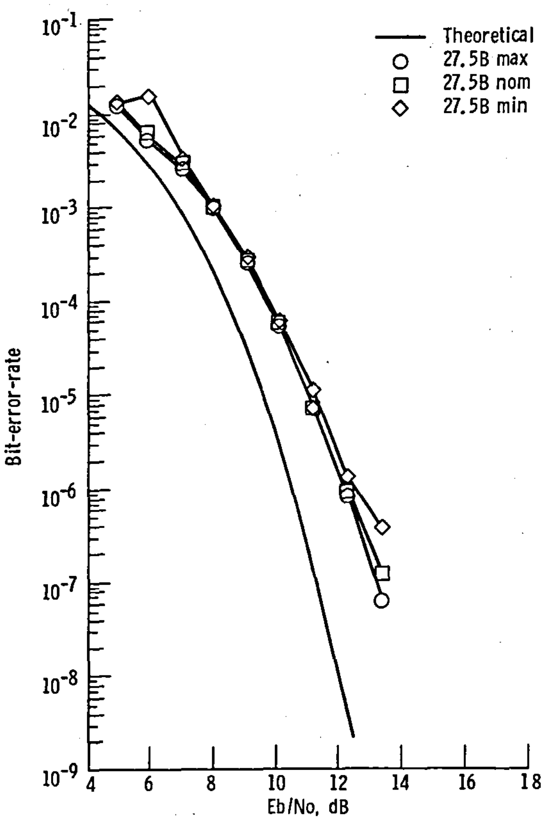

Figure 15. - 27.5B Channel ber performance in burst length variation test, Nov. 1983.

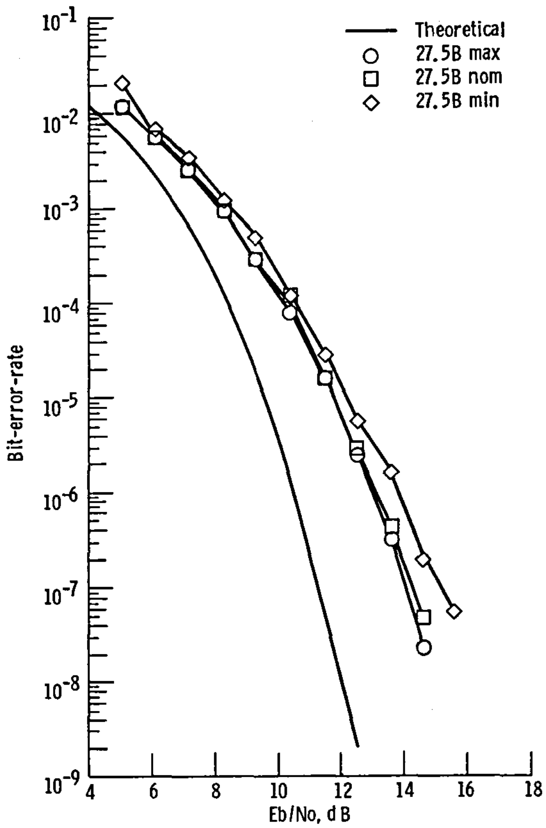

Figure 16. - 27.5B Channel ber performance in burst length variation test, May 1983.

Nov. 22, 1983

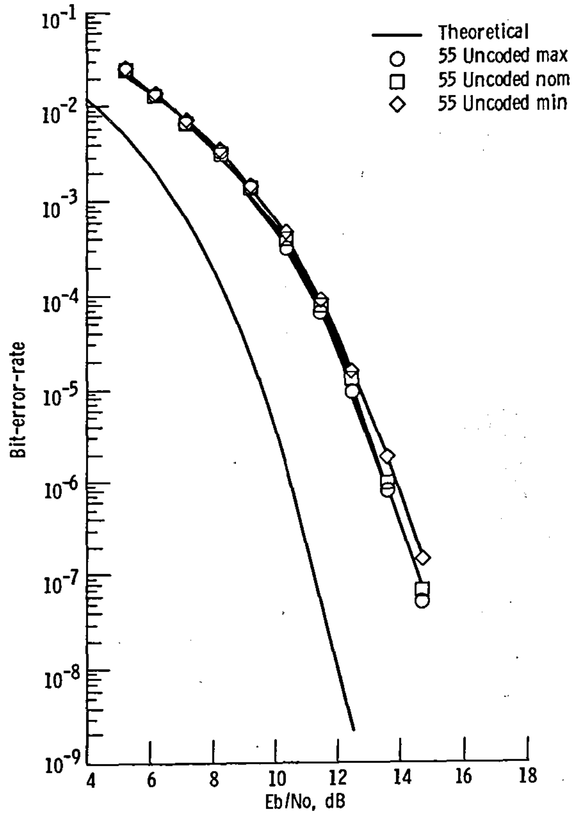

Figure 17. - 55 mb/s Uncoded ber performance in burst length variation test, Nov. 1983.

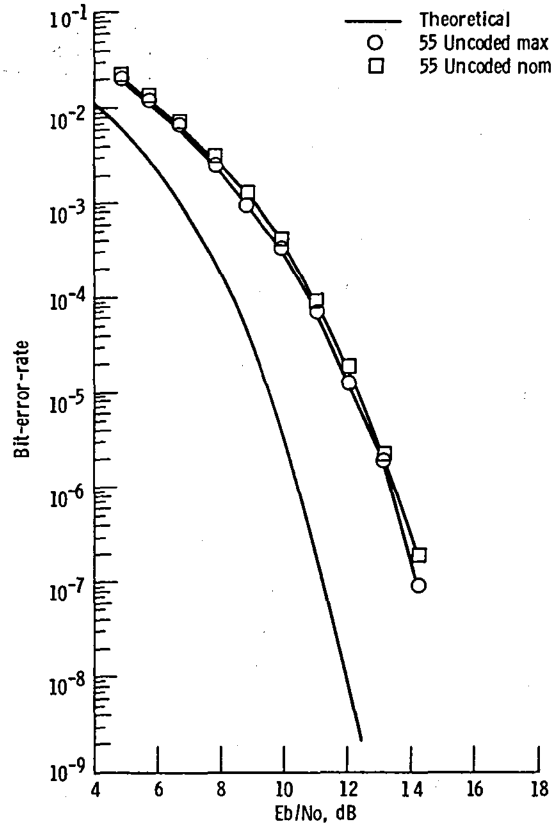

Figure 18. - 55 mb/s Uncoded ber performance in burst length variation test, May 1984.

Nov. 22, 1983

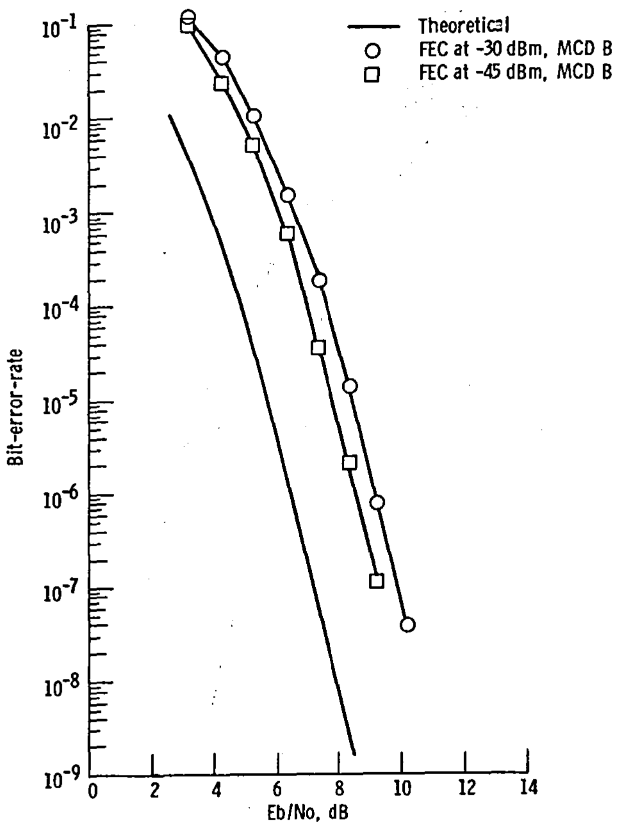

Figure 19. - 55 ms/s Coded ber performance Nov. 1983.

June 14, 1984

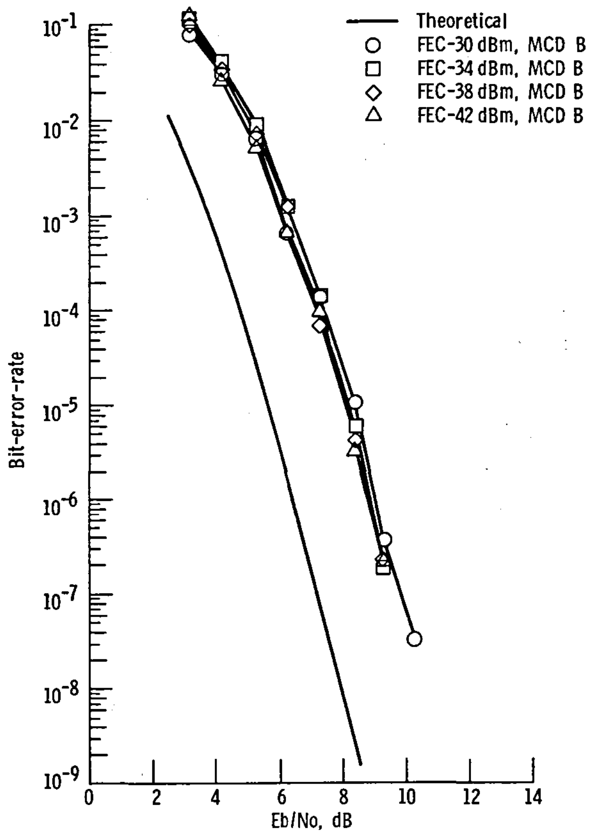

Figure 20. - 55 ms/s Coded ber performance, June 1984.

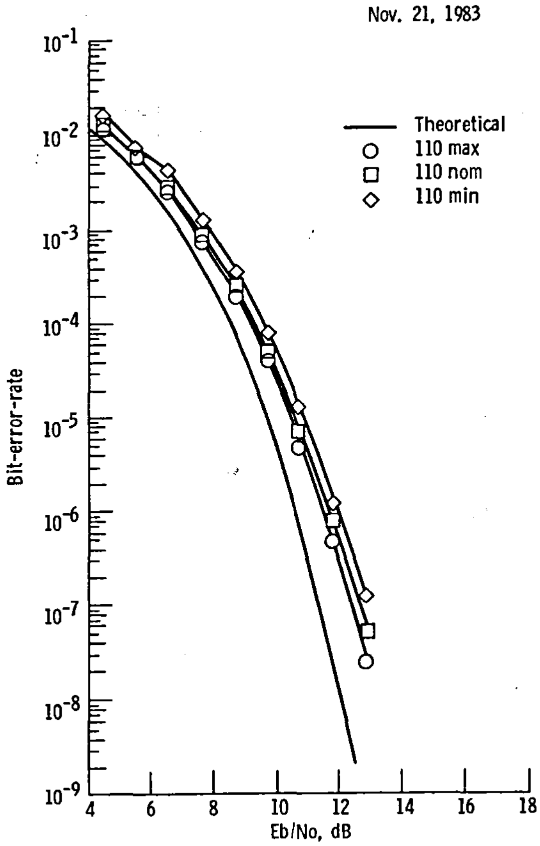

Figure 21. - 110 mb/s Channel ber performance in burst length variation test, Nov. 1983.

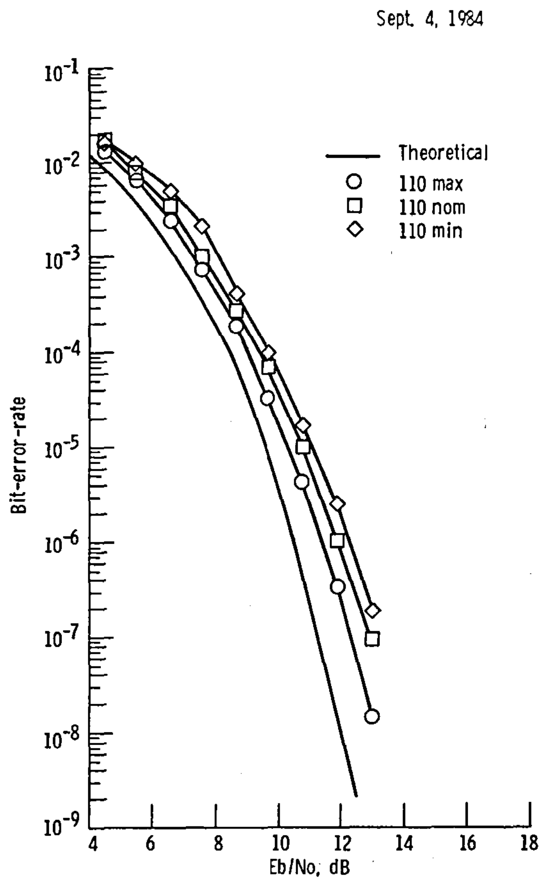

Figure 22. - 110 mb/s Channel ber performance in burst length variation test, Sept. 1984.

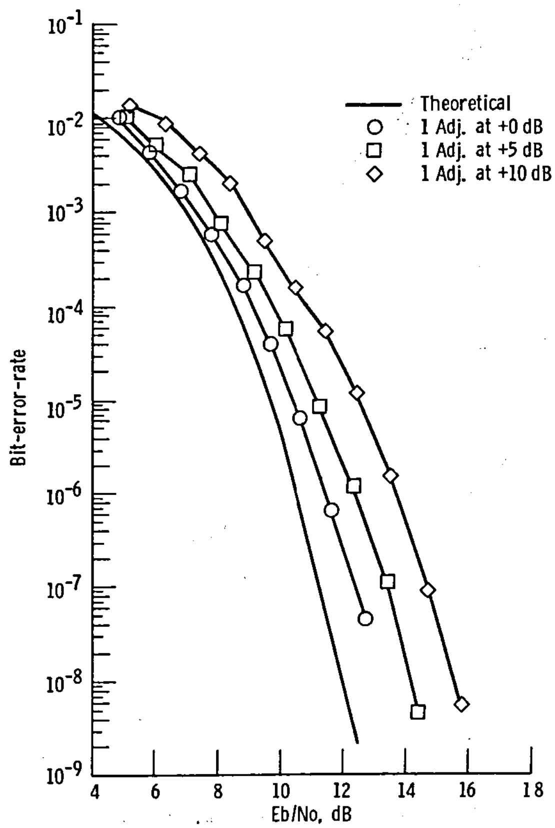

Figure 23. - 27.5B Channel ber performance, adjacent single interferor spaced at 1.5R, Nov. 1983.

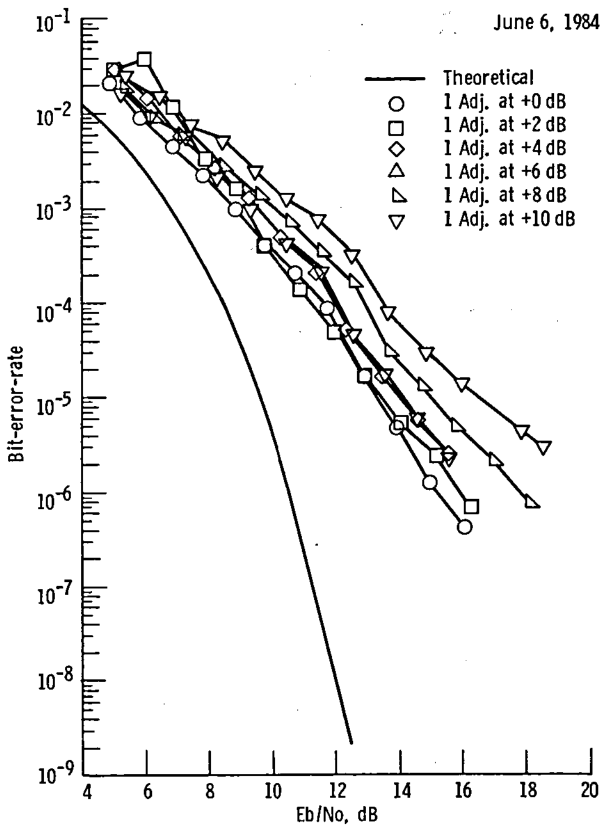

Figure 24. - 27.5B Channel ber performance, adjacent single interferor spaced at 1.5R, June 1984.

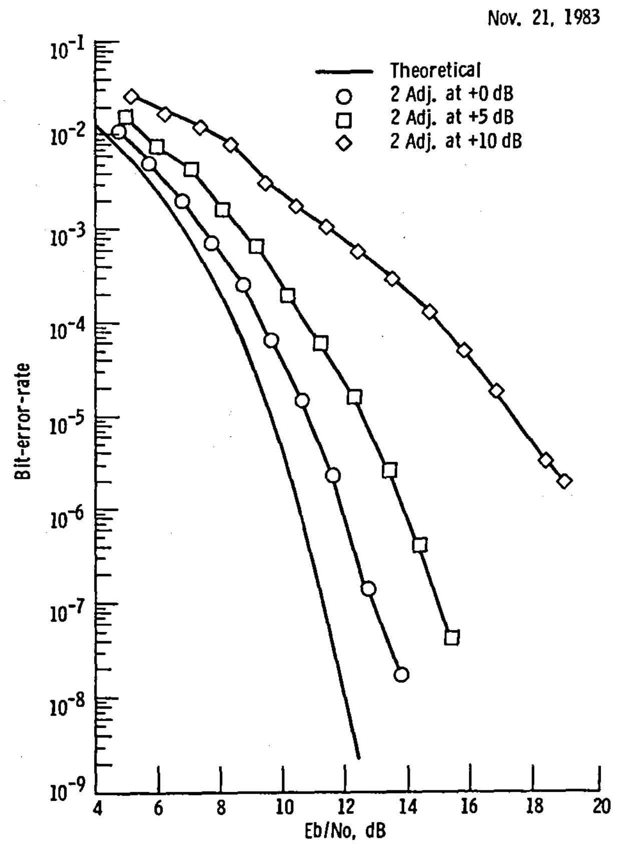

Figure 25. - 27.5B Channel ber performance, dual adjacent interferors spaced at 1.5R, Nov. 1983.

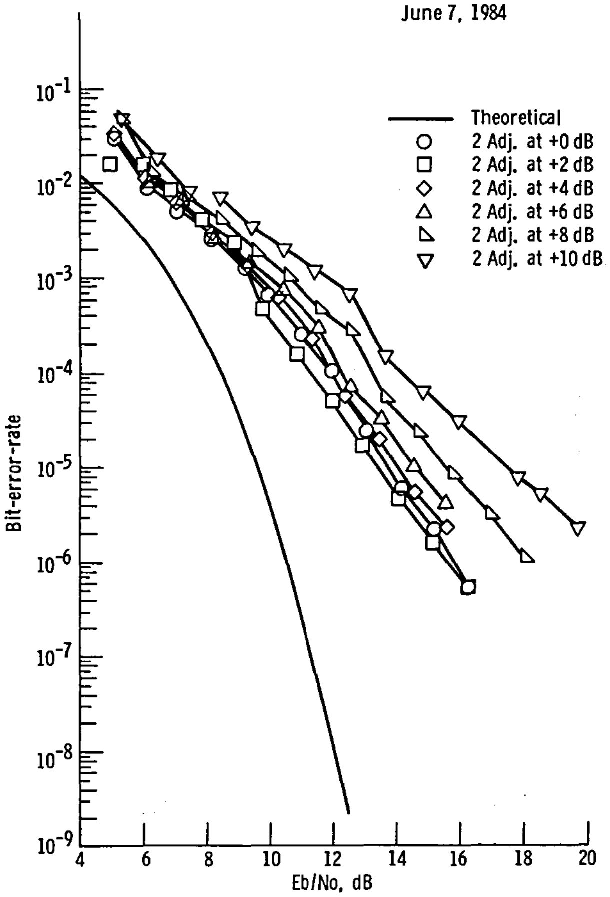

Figure 26. - 27.5B Channel ber performance, dual adjacent interferors spaced at 1.5R, June 1984.

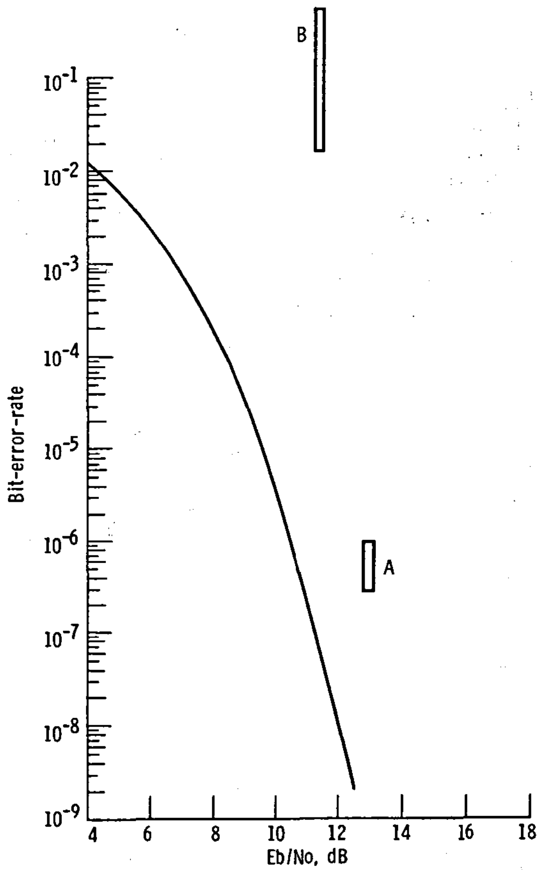

Figure 27. - Comparison of 27.5B mb/s channel ber performance in multi-channel tests on message #19 A: Nov. 1983 tests; B: Sept. 1984 tests.

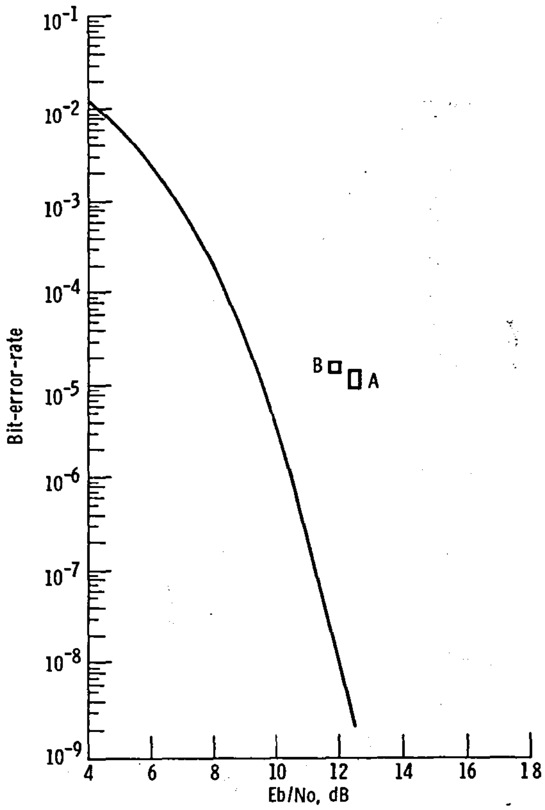

Figure 28. - Comparison of 55 mb/s channel ber performance in multi-channel tests; data combined from message #13 and #14 tests. A: Nov. 1983 tests; B: Sept. 1984 tests.

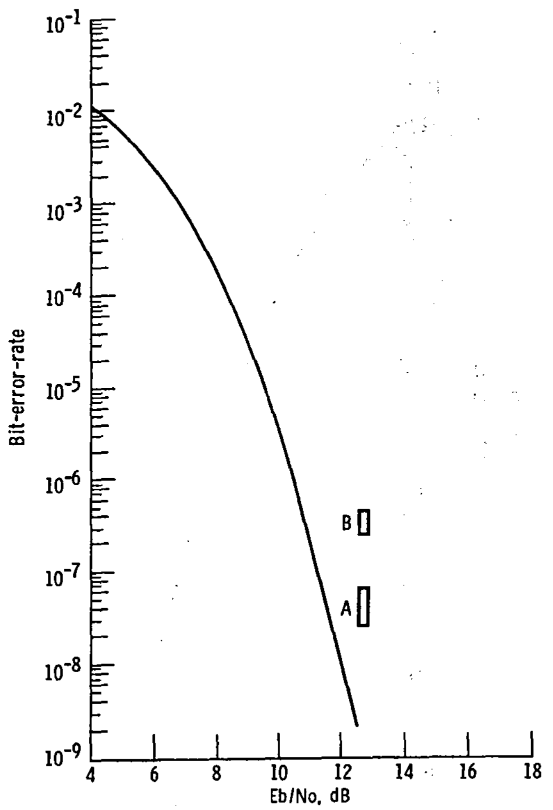

Figure 29. - Comparison of 110 mb/s channel ber performance in multi-channel tests; data from message #11 and #12 tests combined. A: Nov. 1983 tests; B: Sept. 1984 tests.

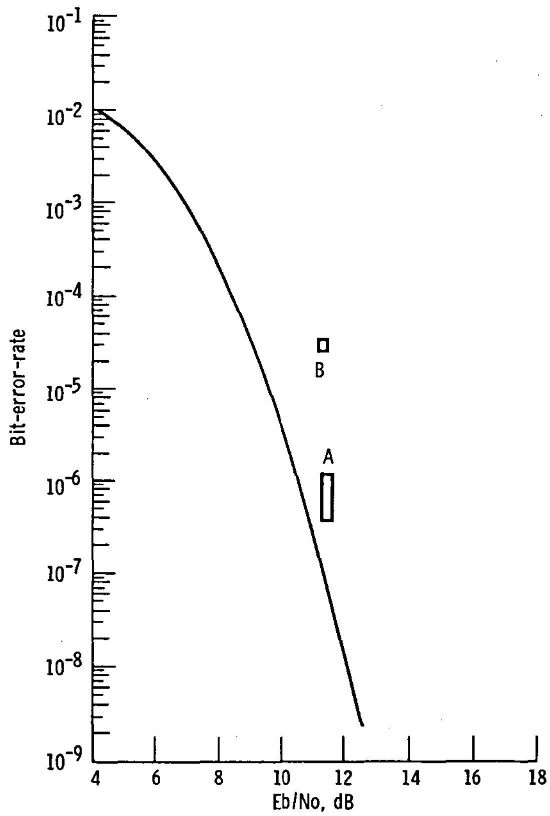

Figure 30. - Comparison of 275-E mb/s channel ber performance in multi-channel tests; data combined from message #3 and #7 tests. A: Nov. 1983 tests; B: Sept. 1984 tests.

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15. Supplementary Notes

16. Abstract

Bit-error-rate tests were performed on a proof-of-concept baseband processor developed by Motorola Government Electronics Group, under the NASA 30/20 GHz Technology Development Program. The BBP, which operates at an intermediate frequency in the C-Band, demodulates, demultiplexes, routes, remultiplexes, and remodulates digital message segments received from one ground station for retransmission to another. Test methods are discussed and test results are compared with the Contractor's test results.

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