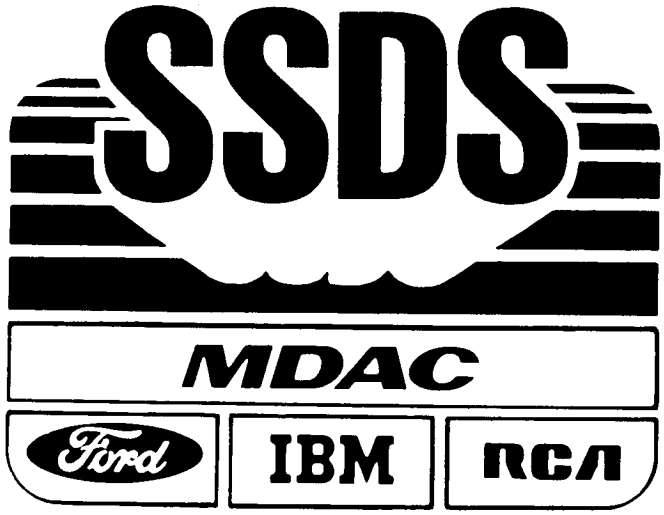
DECEMBER 1985

NASA CR-177839

MDC H1343A



(NASA-CR-177839) SPACE STATION DATA SYSTEM ANALYSIS/ARCHITECTURE STUDY. TASK 2: OPTIONS DEVELOPMENT DR-5. VOLUME 1: TECHNOLOGY OPTIONS (McDonnell-Douglas Astronautics Co.) 379 p HC A17/MF A01 G3/18

N86-20472

Unclas
04589

SPACE STATION DATA SYSTEM ANALYSIS/ARCHITECTURE STUDY

Task 2 – Options Development, DR-5
Volume I – Technology Options

MCDONNELL DOUGLAS CORPORATION

SPACE STATION DATA SYSTEM ANALYSIS/ARCHITECTURE STUDY

Task 2 – Options Development, DR-5
Volume I – Technology Options

DECEMBER 1985

MDC H1343A
REPLACES MDC H1940
DATED MAY 1985

MCDONNELL DOUGLAS ASTRONAUTICS COMPANY-HUNTINGTON BEACH
5301 Bolsa Avenue Huntington Beach, California 92647 (714) 896-3311

PREFACE

The McDonnell Douglas Astronautics Company has been engaged in a Space Station Data System Analysis/Architecture Study for the National Aeronautics and Space Administration, Goddard Space Flight Center. This study, which emphasized a system engineering design for a complete, end-to-end data system, was divided into six tasks:

Task 1. Functional Requirements Definition
Task 2. Options Development
Task 3. Trade Studies
Task 4. System Definitions
Task 5. Program Plan
Task 6. Study Maintenance

McDonnell Douglas was assisted by the Ford Aerospace and Communications Corporation, IBM Federal Systems Division and RCA in these Tasks. The Task inter-relationship and documentation flow are shown in Figure 1.

This report was prepared for the National Aeronautics and Space Administration Goddard Space Flight Center under Contract No. NAS5-28082

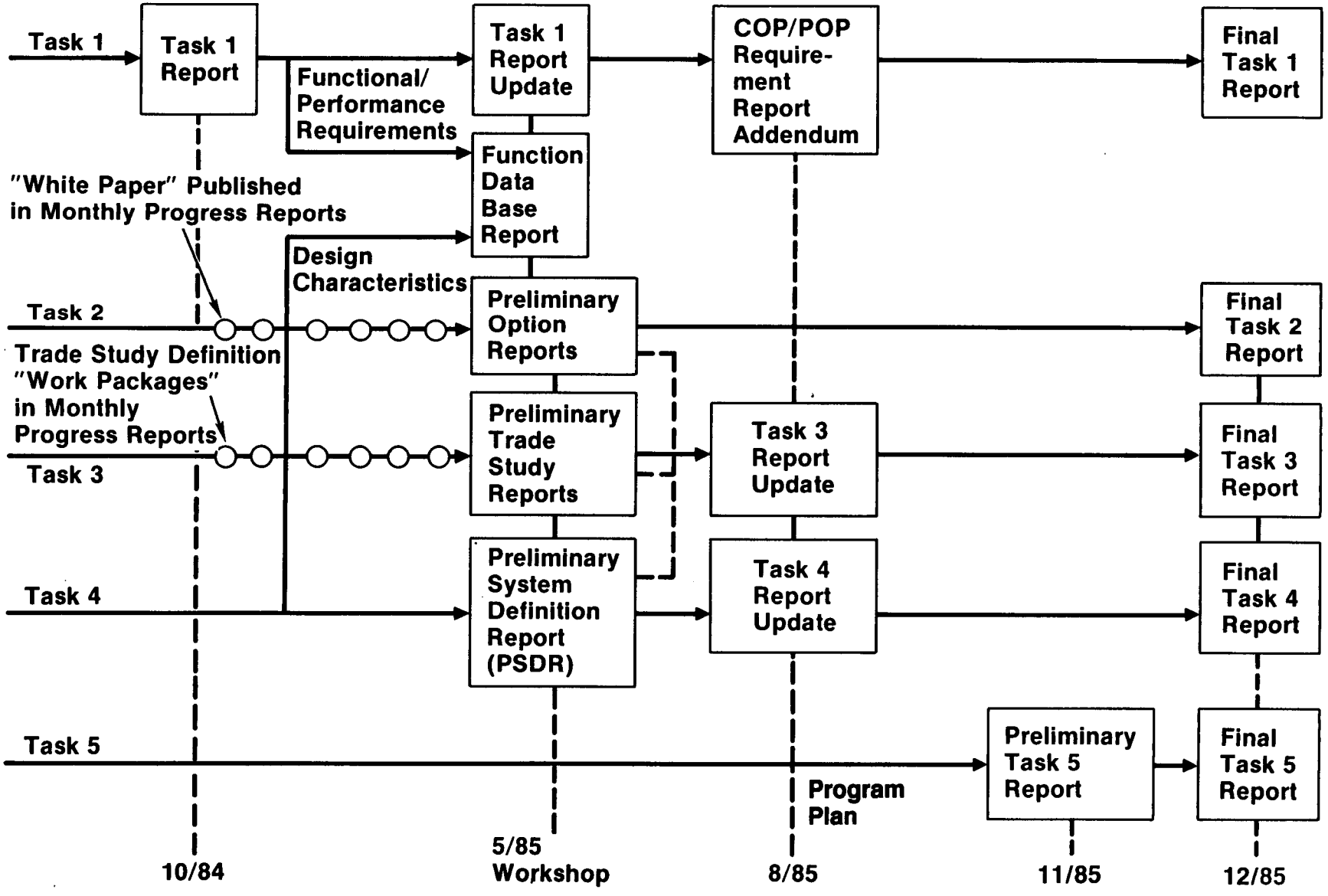
Questions regarding this report should be directed to:

Glen P. Love
Study Manager
McDonnell Douglas Astronautics Company
Huntington Beach, CA 92647
(714) 896-2292

Figure 1

VHG598

SSDS A/A DOCUMENTATION SCHEDULE



Task 2, Volume I
TABLE OF CONTENTS

GLOSSARY

A	Automatic
A&R	Automation and Robotics
A/A	Analysis/Architecture
A/D	Advanced Development
A/L	Airlock
A/N	Alphanumeric
AC&S	Attitude Control System
ACA	Attitude Control Assembly
ACO	Administrative Contracting Officer
ACS	Attitude Control and Stabilization
ACS/COM	Attitude Control System/Communications
ACTS	Advanced Communications Technology Satellite
AD	Ancillary Data
AD	Advanced Development
ADOP	Advanced Distributed Onboard Processor
ADP	Advanced Development Plan
AFOSR	Air Force Office of Scientific Research
AFP	Advanced Flexible Processor
AFRPL	Air Force Rocket Propulsion Laboratory
AGC	Automatic Gain Control
AGE	Attempt to Generalize
AI	Artificial Intelligence
AIE	Ada Integrated Environment
AIPS	Advanced Information Processing System
AL1	Air Lock One
ALS	Alternate Landing Site
ALS/N	Ada Language System/Navy
AMIC	Automated Management Information Center
ANSI	American National Standards Institute
AOS	Acquisition of Signal
AP	Automatic Programming
APD	Avalanche Photo Diode
APSE	Ada Programming Support Environment
ARC	Ames Research Center

ART	Automated Reasoning Tool
ASCII	American Standard Code for Information Exchange
ASE	Airborne Support Equipment
ASTROS	Advanced Star/Target Reference Optical Sensor
ATAC	Advanced Technology Advisory Committee
ATC	Air Traffic Control
ATP	Authority to Proceed
ATPS	Advanced Telemetry Processing System
ATS	Assembly Truss and Structure
AVMI	Automated Visual Maintenance Information
AWSI	Adoptive Wafer Scale Integration
B	Bridge
BARC	Block Adaptive Rate Controlled
BB	Breadboard
BER	Bit Error Rate
BIT	Built-in Test
BITE	Built-in Test Equipment
BIU	Buffer Interface Unit
BIU	Bus Interface Unit
BIU	Built-in Unit
BMD	Ballistic Missile Defense
BTU	British Thermal Unit
BW	Bandwidth
C	Constrained
C^2	Command and Control
C^3	Command, Control, and Communication
C^3I	Command, Control, Communication, and Intelligence
C&DH	Communications and Data Handling
C&T	Communication and Tracking Subsystem
C&T	Communications and Tracking
C&W	Control and Warning
C/L	Checklist
CA	Customer Accommodation
CAD	Computer-Aided Design
CAE	Computer-Aided Engineering
CAIS	Common APSE Interface Set
CAM	Computer-Aided Manufacturing

CAMAC	Computer Automatic Measurement and Control
CAP	Crew Activities Plan
CASB	Cost Accounting Standard Board
CASE	Common Application Service Elements
CATL	Controlled Aceptance Test Library
CBD	Commerce Business Daily
CBEMA	Computer and Business Equipment Manufacturing Association
CCA	Cluster Coding Algorithm
CCB	Contractor Control Board
CCB	Configuration Control Board
CCC	Change and Configuration Control
CCD	Charge-Coupled Device
CCITT	Consultive Committee for International Telegraph and Telephone
CCITT	Coordinating Committee for International Telephony and Telegraphy
CCMS	Checkout Control and Monitor System
CCR	Configuration Change Request
CCSDS	Consultative Committee for Space Data System
CCTV	Closed-Circuit Television
cd/M^2	Candelas per square Meter
CDG	Concept Development Group
CDMA	Code Division Multiple Access
CDOS	Customer Data Operations System
CDR	Critical Design Review
CDS	Control Data Subsystem
CE	Conducted Emission
CEI	Contract End-Item
CER	Cost Estimating Relationship
CFR	Code of Federal Regulations
CFS	Cambridge File Server
CG	Center of Gravity
CIE	Customer Interface Element
CIL	Critical Item List
CIU	Customer Interface Unit
CLAN	Core Local Area Network
CM	Configuration Management
CM	Center of Mass
CMDB	Configuration Management Data Base

CMG	Control Moment Gyro
CMOS	Complementary Metal-Oxide Semiconductor
CMS	Customer Mission Specialist
CMU	Carnegie-Mellon University
CO	Contracting Officer
COF	Component Origination Form
COL	Controlled Operations Library
COMM	Commercial Missions
COP	Co-orbital Platform
COPCC	Coorbit Platform Control Center
COPOCC	COP Operations Control Center
COTS	Commercial Off-the-Shelf Software
CPCI	Computer Program Configuration Item
CPU	Central Processing Unit
CQL	Channel Queue Limit
CR	Compression Ratio
CR	Change Request
CR&D	Contract Research and Development
CRC	Cyclic Redundancy Checks
CRF	Change Request Form
CRSS	Customer Requirements for Standard Services
CRT	Cathode Ray Tube
CS	Conducted Susceptibility
CSD	Contract Start Date
CSDL	Charles Stark Draper Laboratory
CSMA/CD/TS	Carrier-Sense Multiple with Access/Collision Detection and Time Slots
CSTL	Controlled System Test Library
CTA	Computer Technology Associates
CTE	Coefficient of Thermal Expansion
CUI	Common Usage Item
CVSD	Code Variable Slope Delta (Modulation)
CWG	Commonality Working Group
D&B	Docking and Berthing
DADS	Digital Audio Distribution System
DAIS	Digital Avionics Integration System
DAR	Defense Acquisition Regulation

DARPA	Defense Advanced Research Projects Agency
DB	Data Base
DBA	Data Base Administrator
DBML	Data Base Manipulation Language
DBMS	Data Base Management System
DCAS	Defense Contract Administrative Services
DCDS	Distributed Computer Design System
DCR	Data Change Request
DDBM	Distributed Data Base Management
DDC	Discipline Data Center
DDT&E	Design, Development, Testing, and Engineering
DEC	Digital Equipment Corp.
DES	Data Encryption Standard
DFD	Data Flow Diagram
DGE	Display Generation Equipment
DHC	Data Handling Center
DID	Data Item Description
DIF	Data Interchange Format
DMA	Direct Memory Access
DMS	Data Management System
DoD	Department of Defense
DOMSAT	Domestic Communications Satellite System
DOS	Distributed Operating System
DOT	Department of Transportation
DPCM	Differential Pulse Code Modulation
DPS	Data Processing System
DR	Discrepancy Report
DR	Data Requirement
DRAM	Dynamic Random-Access Memory
DRD	Design Requirement Document
DS&T	Development Simulation and Training
DSDB	Distributed System Data Base
DSDL	Data Storage Description Language
DSDS	Data System Dynamic Simulation
DSIT	Development, Simulation, Integration and Training
DSN	Deep-Space Network
DTC	Design to Cost

DTC/LCC	Design to Cost/Life Cycle Cost
DTG	Design To Grow
E/R	Entity/Relationship
EADI	Electronic Attitude Direction Indicator
ECC	Error Correction Codes
ECLSS	Environmental Control and Life-Support System
ECMA	European Computers Manufacturing Assoc.
ECP	Engineering Change Proposals
ECS	Environmental Control System
EDF	Engineering Data Function
EEE	Electrical, Electronic, and Electromechanical
EHF	Extremely High Frequency
EHSI	Electronic Horizontal Situation Indicator
EIA	Electronic Industry Association
EL	Electroluminescent
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMCFA	Electromagnetic Compatibility Frequency Analysis
EME	Earth Mean Equator
EMI	Electromagnetic Interference
EMR	Executive Management Review
EMS	Engineering Master Schedule
EMU	Extravehicular Mobility Unit
EMUDS	Extravehicular Maneuvering Unit Decontamination System
EO	Electro-optic
EOL	End of Life
EOS	Earth Observing System
EPA	Environmental Protection Agency
EPS	Electrical Power System
ERBE	Earth Radiation Budget Experiment
ERRP	Equipment Replacement and Refurbishing Plan
ESR	Engineering Support Request
ESTL	Electronic Systems Test Laboratory
EVA	Extravehicular Activity
F/T	Fault Tolerant
FACC	Ford Aerospace and Communications Corporation
FADS	Functionally Automated Database System

FAR	Federal Acquisition Regulation
FCA	Functional Configuration Audit
FCOS	Flight Computer Operating System
FCR	Flight Control Rooms
FDDI	Fiber Distributed Data Interface
FDF	Flight Dynamics Facility
FDMA	Frequency-Division Multiple Access
FEID	Flight Equipment Interface Device
FETMOS	Floating Gate Election Tunneling Metal Oxide Semiconductor
FF	Free Flier
FFT	Fast Fourier Transform
FIFO	First in First Out
FIPS	Federal Information Processing Standards
fl	foot lambert - Unit of Illumination
FM	Facility Management
FMEA	Failure Modes and Effects Analysis
FMECA	Failure Mode Effects and Criticality Analysis
FO	Fiber-Optics
FO/FS/R	Fail-Operational/Fail Safe/Restorable
FOC	Fiber-Optic Cable
FODB	Fiber-Optic Data Bus
FODS	Fiber Optic Demonstration System
FPR	Federal Procurement Regulation
FQR	Formal Qualification Review
FSD	Full-Scale Development
FSE	Flight Support Equipment
FSED	Full Scale Engineering Development
FSIM	Functional Simulator
FSW	Flight Software
FTA	Fault Tree Analysis
FTMP	Fault Tolerant Multi-Processor
FTSC	Fault Tolerant Space Computer
GaAs	Gallium Arsenide
GaAsP	Gallium Arsenic Phosphorus
GaInP	Gallium Indium Phosphorus
GaP	Gallium Phosphorous
GAPP	Geometric Arithmetic Parallel Processor

Gbps	Gigabits Per Second
GBSS	Ground Based Support System
GEO	Geosynchronous Earth Orbit
GEP	Gas Election Phosphor
GFC	Ground Forward Commands
GFE	Government-Furnished Equipment
GFP	Government-Furnished Property
GFY	Government Fiscal Year
GIDEP	Government/Industry Data Exchange Program
GMM	Geometric Math Model
GMS	Geostationary Meteorological Satellite
GMT	Greenwich Mean Time
GMW	Generic Maintenance Work Station
GN&C	Guidance, Navigation, and Control
GPC	General-Purpose Computer
GPP	General-Purpose Processor
GPS	Global Positioning System
GRO	Gamma Ray Observatory
GSC	Ground Service Center
GSE	ground Support Equipment
GSFC	(Robert H.) Goddard Space Flight Center
GTOSS	Generalized Tethered Object System Simulation
H/W	Hardware
HAL	High-Order Algorithmic Language
HDDR	Help Desk Discrepancy Report
HDDR	High Density Digital Recording
HEP	Heterogeneous Element Processor
HFE	Human Factors Engineering
HIPO	Hierarchical Input Process Output
HIRIS	High Resolution Imaging Spectrometer
HM1	Habitation Module One
HM	Habitation Module
HOL	High Order Language
HOS	High Order Systems
HPP	High Performance Processors
HRIS	High Resolution Imaging Spectrometer
I	Interactive

I/F	Interface
I/O	Input/Output
IBM	IBM Corporation
IC	Intercomputer
ICAM	Integrated Computer-Aided Manufacturing
ICB	Internal Contractor Board
ICD	Interface Control Document
ICOT	Institute (for new generation) Computer Technology
ICS	Interpretive Computer Simulation
ID	Interface Diagram
ID	Identification
IDM	Intelligent Database Machine
IDMS	Information and Data Management System
IEEE	Institute of Electrical and Electronic Engineers
IEMU	Integrated Extravehicular Mobility Unit
IF	Intermediate Frequency
IFIPS	International Federation of Industrial Processes Society
ILD	Injector Laser Diode
IMU	Inertial Measurement Unit
INS	Inertial Navigation System
IOC	Initial Operating Capability
IOP	Input/Output Processor
IPCF	Interprocess Communications Facility
IPC	Interprocesses Communication
IPL	Initial Program Load
IPR	Internal Problem Report
IPS	Instrument Pointing System
IR	Infrared
IR&D	Independent Research and Development
IRN	Interface Revision Notices
ISA	Inertial Sensor Assembly
ISA	Instruction Set Architecture
ISDN	Integration Services Digital Network
ISO	International Standards Organization
ITAC-0	Integration Trades and Analysis-Cycle 0
ITT	International Telegraph and Telephone
IV&V	Independent Validation and Verification

IVA	Intravehicular Activity
IWS	Intelligent Work Station
JPL	Jet Propulsion Laboratory
JSC	(Lyndon B.) Johnson Space Center
KAPSE	Kernal APSE
KEE	Knowledge Engineering Environment
KIPS	Knowledge Information Processing System
KOPS	Thousands of Operations Per Second
KSA	Ku-band, Single Access
KSC	(John F.) Kennedy Space Center
Kbps	Kilobits per second
Kipc	Thousand instructions per cycle
LAN	Local-Area Network
LaRC	Langley Research Center
LCC	Life-Cycle Cost
LCD	Liquid Crystal Display
LDEF	Long-Duration Exposure Facility
LDR	Large Deployable Reflector
LED	Light-Emitting Diode
LEO	Low Earth Orbit
LeRC	Lewis Research Center
LIDAR	Laser-Instrument Distance and Range
LIFO	Last In First Out
LIPS	Logical Inferences Per Second
LISP	List Processor
LisP	List Processor
LLC	Logical Link Control
LMI	LISP Machine Inc.
LN_2	Liquid Nitrogen
LNA	Low-noise Amplifier
LOE	Level of Effort
LOE	Low-earth Orbit Environments
LOS	Loss of Signal
LPC	Linear Predictive Coding
LPS	Launch Processing System
LRU	Line-Replaceable unit
LSA	Logistic Support Analysis

MMU	Manned Maneuvering Unit
MNOS	Metal-Nitride Oxide Semiconductor
MOC	Mission Operations Center
MOI	Moment of Inertia
MOL	Manned Orbiting Laboratory
MOS	Metal Oxide Semiconductor
MPAC	Multipurpose Application Console
MPS	Materials, Processing in Space
MPSR	Multi-purpose Support Rooms
MRMS	Mobile Remote Manipulator System
MRWG	Mission Requirements Working Group
MSFC	(George C.) Marshall Space Flight Center
MSI	Medium-Scale Integration
MSS	Multispectral Scanner
MTA	Man-Tended Approach
MTBF	Mean Time Between Failures
MTTR	Mean Time to Repair
MTU	Master Timing Unit
NASA	National Aeronautics and Space Administration
NASCOM	NASA Communications Network
NASPR	NASA Procurement Regulation
NBO	NASA Baseline
NBS	National Bureau of Standards
NCC	Network Control Center
NFSD	NASA FAR Supplement Directive
NGT	NASA Ground Terminals
NHB	NASA Handbook
NISDN	NASA Integrated System Data Network
NIU	Network Interface Unit
NL	National Language
NLPQ	National Language for Queuing Simulation
NMI	NASA Management Instruction
NMOS	N-Channel Metal-Oxide Semiconductor
NMR	N-Modular Redundant
NOS	Network Operating System
NS	Nassi-Schneidermann
NSA	National Security Administration

NSF	National Science Foundation
NSTS	National Space Transportation System
NTDS	Navy Tactical Data System
NTE	Not To Exceed
NTRL	NASA Technology Readiness Level
NTSC	National Television Standards Committee
Nd:YAG	Neodynium Yttrium Aluminum Garnet (laser type)
O&M	Operations and Maintenance
O/B	Onboard
OASCB	Orbiter Avionics Software Control Board
OCN	Operations and Control Network, Operational Control Networks
ODB	Operational Data Base
ODBMS	Onboard Data Base Management System
OEL	Operating Events List
OES	Operating Events Schedule
OID	Operations Instrumentation Data
OLTP	On Line Transaction Processing
OMCC	Operations Management and Control Center
OMV	Orbital Maneuvering Vehicle
ONR	Office of Naval Research
ORU	Orbital Replacement Unit
OS	Operating System
OSE	Orbit Support Equipment
OSI	Open Systems Interconnect
OSM	Orbital Service Module
OSSA	Office of Space Science and Applications
OSTA	Office of Space and Terrestrial Application
OSTDS	Office of Space Tracking and Data Systems
OTV	Orbital Transfer Vehicle
P&SA	Payload and Servicing Accommodations
P/L	Payload
PA	Product Assurance
PAM	Payload Assist Module
PASS	Primary Avionics Shuttle Software
PBX	Private Branch Exchange
PC	Personal Computer
PCA	Physical Configuration Audit

LSAR	Logistic Support Analysis Report
LSE	Language Sensity Editors
LSI	Large-scale Integration
LTV	LTV Aerospace and Defense Company, Vought Missiles Advanced Programs Division
LZPF	Level 0 Processing Facility
M	Manual
µP	Microprocessor
MA	Multiple Access
MA	Managing Activity
MAPSE	Minimum APSE
Mbps	Million Bits Per Second
MBPS	Million Bits Per Second
MCAIR	McDonnell Aircraft Company
MCC	Mission Control Center
MCC	Microelectronics and Computer Technology Corp.
MCDS	Management Communications and Data System
MCM	Military Computer Modules
MCNIU	Multi-compatible Network Interface Unit
MDAC-HB	McDonnell Douglas Astronautics Company-Huntington Beach
MDAC-STL	McDonnell Douglas Astronautics Company-St. Louis
MDB	Master Data Base
MDC	McDonnell Douglas Corporation
MDMC	McDonnell Douglas Microelectronics Center
MDRL	McDonnell Douglas Research Laboratory
MFLOP	Million Floating Point Operations
MHz	Million Hertz
MIMO	Multiple-Input Multiple-Output
MIPS	Million (machine) Instructions Per Second
MIT	Massachusetts Institute of Technology
MITT	Ministry of International Trade and Industry
MLA	Multispectral Linear Array
MMI	Man Machine Interface
MMPF	Microgravity and Materials Process Facility
MMS	Module Management System
MMS	Momentum Management System
MMU	Mass Memory Unit

PCA	Program Change Authorization
PCM	Pulse Code Modulation
PCR	Program Change Request
PDP	Plazma Display Panel
PDR	Preliminary Design Review
PDRD	Program Definition and Requirements Document
PDRSS	Payload Deployment and Retrieval System Simulation
PILS	Payload Integration Library System
PIN	Personal Identification Number
PLA	Programmable Logic Array
PLAN	Payload Local Area Network
PLSS	Payload Support Structure
PMAD	Power Management and Distribution
PMC	Permanently Manned Configuration
PN	Pseudonoise
POCC	Payload Operations Control Center
POP	Polar Orbiter Platform
POPCC	Polar Orbit Platform Control Center
POPOCC	POP Operations Control Center
PRISM	Prototype Inference System
PSA	Problem Statement Analyzer
PSA	Preliminary Safety Analysis
PSCN	Program Support Communications Network
PSL	Problem Statement Language
PTR	Problem Trouble Report
QA	Quality Assurance
R	Restricted
R&D	Research and Development
R&QA	Reliability and Quality Assurance
R/M/A	Reliability/Maintainability/Availability
R/T	Real Time
RAD	Unit of Radiation
RAM	Random Access Memory
RAP	Relational Associative Processor
RC	Ring Concentrator
RCA	RCA Corporation
RCS	Reaction Control System

RDB	relational Data Base
RDC	Regional Data Center
REM	Roentgen Equivalent (man)
RF	Radio Frequency
RFC	Regenerative Fuel Cell
RFI	Radio Frequency Interference
RFP	Request for Proposal
RGB	Red-Green-Blue
RID	Review Item Disposition
RID	Revision Item Description
RISC	Reduced Instruction Set Computer
RMS	Remote Manipulator System
RMSE	Root Mean Square Error
RNET	Reconfiguration Network
ROM	Read Only Memory
ROTV	Reuseable Orbit Transfer Vehicle
RPMS	Resource Planning and Management System
RS	Reed-Solomon
RSA	Rivest, Skamir and Adleman (encryption method)
RTX	Real Time Execution
S&E	Sensor and Effector
S/C	Spacecraft
S/W	Software
SA	Single Access
SA	Structured Analysis
SAAX	Science and Technology Mission
SAE	Society of Automotive Engineers
SAIL	Shuttle Avionics Integration Laboratory
SAIS	Science and Applications Information System
SAR	Synthetic Aperture Radar
SAS	Software Approval Sheet
SASE	Specific Application Service Elements
SATS	Station Accommodations Test Set
SBC	Single Board Computer
SC	Simulation Center
SCR	Software Change Request
SCR	Solar Cosmic Ray

SCS	Standard Customer Services
SDC	Systems Development Corporation
SDP	Subsystem Data Processor
SDR	System Design Review
SDTN	Space and Data Tracking Network
SE&I	Systems Engineering and Integration
SEI	Software Engineering Institute
SESAC	Space and Earth Scientific Advisory Committee
SESR	Sustaining Engineering System Improvement Request
SESS	Software Engineering Standard Subcommittee
SEU	Single Event Upset
SFDU	Standard Format Data Unit
SI	International System of Units
SIB	Simulation Interface Buffer
SIFT	Software Implemented Fault Tolerance
SIMP	Single Instruction Multi-Processor
SIRTF	Shuttle Infrared Telescope Facility
SLOC	Source Lines of Code
SMC	Standards Management Committee
SMT	Station Management
SNA	System Network Architecture
SNOS	Silicon Nitride Oxide Semiconductor
SNR	Signal to Noise Ratio
SOA	State Of Art
SOPC	Shuttle Operations and Planning Complex
SOS	Silicon On Saphire
SOW	Statement of Work
SPC	Stored Payload Commands
SPF	Software Production Facility
SPF	Single-Point Failure
SPR	Spacelab Problem Reports
SPR	Software Problem Report
SQA	Software Quality Assurance
SQAM	Software Quality Assessment and Measurement
SQL/DS	SEQUEL Data System
SRA	Support Requirements Analysis
SRAM	Static Random Access Memory

SRB	Software Review Board
SRC	Specimen Research Centrifuge
SREM	Software Requirements Engineering Methodology
SRI	Stanford Research Institute
SRM&QA	Safety, Reliability, Maintainability, and Quality Assurance
SRMS	Shuttle Remote Manipulator System
SRR	System Requirements Review
SS	Space Station
SSA	Structural Systems Analysis
SSA	S-band Single Access
SSCB	Space Station Control Board
SSCC	Station Station Communication Center
SSCR	Support Software Change Request
SSCS	Space Station communication system
SSCTS	Space Station communications and tracking system
SSDMS	Space Station data management system
SSDR	Support Software Discrepancy Report
SSDS	Space Station data system
SSE	Software Support Environment
SSEF	Software Support Environment Facility
SSIS	Space Station Information System
SSME	Space Shuttle Main Engine
SSO	Source Selection Official
SSOCC	Space Station Operations Control System
SSOCC	Space Station Operations Control Center
SSOL	Space Station Operation Language
SSON	Spacelab Software Operational Notes
SSOS	Space Station Operating System
SSP	Space Station Program
SSPE	Space Station Program Element
SSPO	Space Station Program Office
SSSC	Space Station Standard Computer
SSST	Space Station System Trainer
STAR	Self Test and Recovery (repair)
STARS	Software Technology for Adaptable and Reliable Software
STDN	Standard Number
STI	Standard Technical Institute

STO	Solar Terrestrial Observatory
STS	Space Transportation System
SUSS	Shuttle Upper Stage Systems
SYSREM	System Requirements Engineering Methodology
Si	Silicon
SubACS	Submarine Advanced Combat System
TAI	International Atomic Time
TBD	To Be Determined
TBU	Telemetry Buffer Unit
TC	Telecommand
TCP	Transmissions Control Protocols
TCS	Thermal Control System
TDASS	Tracking and Data Acquisition Satellite System
TDM	Technology Development Mission
TDMA	Time-Division Multiple Access
TDRS	Tracking and Data Relay Satellite
TDRSS	Tracking and Data Relay Satellite System
TFEL	Thin Film Electrolumenescent
THURIS	The Human Role in Space (study)
TI	Texas Instruments
TM	Technical Manual
TM	Thematic Mapper
TMDE	Test, Measurement, and Diagnostic Equipment
TMIS	Technical and Management Information System
TMP	Triple Multi-Processor
TMR	Triple Modular Redundancy
TMS	Thermal Management System
TPWG	Test Planning Working Group
TR	Technical Requirement
TRAC	Texas Reconfigurable Array Computer
TRIC	Transition Radiation and Ionization Calorimeter
TSC	Trade Study Control
TSIP	Technical Study Implementation Plan
TSP	Twisted Shielded Pair
TSS	Tethered Satellite System
TT&C	Telemetry, Tracking, and Communications
TTC	Telemetry Traffic Control

TTR	Timed Token Ring
TWT	Traveling-Wave Tube
U	Non-restrictive
UCC	Uniform Commercial Code
UDRE	User Design Review and Exercise
UIL	User Interface Language
UON	Unique Object Names
UPS	Uninterrupted Power Source
URN	Unique Record Name
UTBUN	Unique Telemetry Buffer Unit Name
UTC	Universal Coordinated Time
V&V	Validation and Verification
VAFB	Vandenberg Air Force Base
VAX	Virtual Address Exchange
VHSIC	Very High-Speed Integrated Circuit
VLSI	Very Large-Scale Integration
VLSIC	Very Large-Scale Integrated Circuit
VV&T	Validation, Verification and Testing
WAN	Wide Area Network
WBS	Work Breakdown Structure
WBSP	Wideband Signal Processor
WDM	Wavelength Division Multiplexing
WP	Work Package
WRO	Work Release Order
WS	Workstation
WSGT	White Sands Ground Terminal
WTR	Western Test Range
XDFS	XEROX Distributed File System
YAPS	Yet Another Production System
ZOE	Zone Of Exclusion
ZONC	Zone Of Non-Contact
ZnS	Zinc Sulfide

Volume I

TASK 2 - OPTIONS DEVELOPMENT

INTRODUCTION

The primary objective of Task 2 is the development of an information base that will support the conduct of trade studies (Task 3) and provide sufficient data to make key design/programmatic decisions (Tasks 4 & 5). This includes: (1) the establishment of option categories that are most likely to influence SSDS definition; (2) the identification of preferred options in each category; and (3) the characterization of these options with respect to performance attributes, constraints, cost and risk.

The definition of option categories was accomplished using hierarchial structures derived primarily from technology, system design, or programmatic perspectives. Technology option categories include advanced materials, processes and techniques that can be used to enhance the implementation of SSDS design structures. Design option categories include alternative structures, configurations and techniques that can be used to develop designs that are responsive to the SSDS requirements. Programmatic option categories include methods used to administrate/manage the development operation and maintenance of the SSDS. Programmatic options are important in that they tend to constrain design/technology decisions to cost-effective and timely solutions. It should be noted that with this method of option categorization, certain disciplines may be split across technology, design and programmatic areas. For example, software categories are included in all three. Technology oriented categories for software include such items as advanced tools and algorithms while design oriented categories include data base management and operating systems. Software development is addressed under programmatic options. The MDAC study team categorization approach and its structure is summarized in Table 1. It is intended to facilitate completeness, avoid replication, and support ease of use. The technology, design and programmatic options are each bound in separate volumes for ease of review. This draft is a collection of "white papers" each of which addresses a single option subject. This volume (I) addresses the generic approach and

TABLE 1

SSDS OPTIONS

VOLUME I	VOLUME II	VOLUME III
1.0 TECHNOLOGY OPTIONS	2.0 DESIGN OPTIONS	3.0 PROGRAMMATIC OPTIONS
1.1 Mass Storage	2.1 Software	3.1 Standardization/Commonality
1.2 Man/Machine Interface	2.1.1 Data Base Management	3.2 System Management
1.3 Data Processing Hardware	2.1.2 Resource Management	* 3.3 Deleted
1.4 Software	2.2 System Architecture	* 3.4 Deleted
1.4.1 Advanced Algorithms	2.2.2 Autonomy/Automation	3.5 System Development
1.4.2 High Order Languages	2.2.3 System Growth	3.5.1 Hardware Procurement
*1.4.3 Deleted	* 2.2.4 Deleted	3.5.2 Software Development
1.4.4 Advanced Tools	2.2.5 System Interfaces	3.5.3 System Integration Test & Verification
*1.5 Deleted	2.2.5.1 SSDS/Payload	
1.6 Artificial Intelligence	* 2.2.5.2 Deleted	
1.7 Communications	2.2.5.3 Man/Machine I/F (Workstations)	
1.7.1 Hard-Wired Communications	* 2.2.5.4 Deleted	
1.7.1.1 Network Media	2.3 System Security/Privacy	
1.7.1.2 Network I/F Devices	2.4 Time Management	
*1.7.2 Deleted	2.5 Communications	
	2.5.1 Space Communications	
	2.5.2 Wide Area Communications	
	2.5.3 Local Area Networking	
	2.6 Network Performance Assessment	

* These items have been deleted or incorporated into other sections.

methodology for the Technology Options listed in Table 1. Volumes II and III address the detailed options development for the Design and Programmatic Options, respectively.

The options which were identified within each major category are those considered most likely to influence SSDS design/programmatic decisions and/or enhance SSDS capabilities. This screening process is based on an assessment of the key driving requirements (Task 1) as well as the emerging architectural needs (Task 4). The level of option characterization varies across the different categories depending on study needs and perceived criticality. Some categories are much easier to characterize in terms of quantitative parameters than others. For example, most technology options are more conducive to quantitative measurement (i.e., size, power, reliability, capacity, throughput, cost, etc.), however, the characterization of these categories must include projected capabilities for both IOC and growth phases.

TASK APPROACH

The Task 2 options development activity was initiated early in the study to: (1) facilitate data gathering in high-technology areas that require long-lead-time efforts; (2) provide supporting design and technology perspective to Task 1 activities; and (3) support an early extraction of design/development drivers. However, options development should be done within the context of a system design structure that is derived from a comprehensive understanding of the requirements. This provides a firm basis for focusing options development on the more critical architectural needs. To accommodate the evolving needs of the study from requirements definition to the initial phases of system design while allowing early data gathering efforts to be initiated, required a highly adaptive approach.

This section will describe the following steps that define the task methodology and approach. The key steps include:

1. Establish an early baseline options list structure.
2. Establish a prioritized options list structure.
3. Identify options in high-priority categories.
4. Characterize options.
5. Document option categories.
6. Review and validation.

Early in the study a baseline options list structure was developed. The intent was to create a broad hierarchial framework that would not preclude potential solutions merely by omission. This required a somewhat independent and innovative viewpoint that did not introduce pre-conceived biases. This "baseline" structure also provided a highly visible mechanism to force conscious decisions as to the applicability and criticality of the various option categories. The top-level outline of this "baseline" structure has been retained even though study needs have dictated changes at the lower levels.

A "prioritized" options list structure was then derived form the "baseline" that recognized the needs of Tasks 3 & 4 in terms of their schedule, areas of emphasis, and key characterization parameters. This required significant interaction with these tasks to insure that a sufficient options data base will be available at the appropriate time. This is an evolving and continuing process that provides the basis for "bounding" and time phasing task 2 activities.

Initially, representative options were identified within the baseline options list structure to illustrate the intent of each category. This supported the refinement of the structure and supported the prioritization process. Once efforts were initiated for a high-priority category, the list of options was refined and screened to focus on driving requirements and evolving architectural needs. This process is essentially a coarse filter applied to a broad spectrum of alternatives to derive a "manageable" subset that can support key design decision extraction or provide the basis for a detailed trade study.

Once a refined set of options had been established for a prioritized category, option characterization and data gathering efforts were initiated. The characterization parameters vary significantly for different categories and were established/coordinated based on study needs (Tasks 3 & 4). Data gathering was based on a multitude of input sources including the following:

- Literature Searches
- Team-wide Expertise
- Technical Conferences
- NASA System and Technology Study Documentation
- Industry/Government Standards
- Team Research and Development
- NASA R&D and Testbed Activities
- Personal contacts with NASA, Industry and DoD Experts
- Review of Major DoD Initiatives (VHSIC, Ada/APSE, STARS, DARPA activities, etc.)
- Academia Programs

A key factor in characterizing technology options is the need to include realistic projections of capabilities that are likely to exist for IOC and future growth potential. This provides the foundation to develop SSDS designs that: (1) minimize the "technology gap" for initial development; (2) accommodate technological growth during the life time of the Space Station; and (3) support planned transitions to more autonomous/automated operations. In addition, such projections will play a key role in overall technology assessments that will result in specific recommendations for SSDS technology development and/or enhancement. Related technology development programs currently in process or planned for the near future will be of particular interest and provides valuable near-term insight. Long-term projections are more difficult and uncertain but are no less important because of their influence on growth and technology accommodation planning.

All major option categories have been documented in the form of preliminary "white papers" and included in the monthly progress reports for NASA review and comment. This form of documentation is based on a generic format that

included the identification of key driving requirements, a brief description of the options, option characterization and projected capabilities. We used this method of documentation and review to accomplish the following objectives:

a. Facilitate Team coordination and review.

b. Solicit contributions from all available sources including related NASA activities.

c. Identify areas of deficiency for which specialized support may be required.

d. Provide a mechanism to support early NASA review and allow maximum visibility.

Most option categories have been documented and submitted to NASA for review. The material provided in this appendix is a compilation of these preliminary "white papers" incorporating those NASA comments received prior to April 1, 1985.

SUMMARY

The preliminary task 2 (options development) documentation included in this Appendix has been organized using the outline and numbering scheme of the options list structure provided in Table 1. However, some sections have been deleted or incorporated within other sections during the course of the study and are so identified. This documentation was previously provided to NASA in the form of individual "white papers" (monthly progress reports) for preliminary review. The material contained in Volumes I, II, and III of this report represents a partial update to the preliminary "white papers". That is, attempts have been made to update sections to reflect those NASA review comments that were received in time for incorporation. This material is still considered to be preliminary in nature and will be updated prior to the formal Task 2 submittal.

1.0 TECHNOLOGY OPTIONS

1.1 MASS STORAGE

This section describes the technology options for mass storage and includes the major categories of (1) on-line storage (space), (2) on-line storage (ground), and (3) off-line storage (archive). On-line storage is divided into space/ground categories because of significant differences in both the driving requirements and the applicable technologies. As used here, "on-line storage" refers to devices that provide on-line computer access to mass storage capabilities without direct human intervention. "Off-line storage" implies some level of long-term data archiving, generally requiring intermediate processes before data can be stored or retrieved. Not included in this section is the memory storage that is considered to be an integral part of a processing element. However, memory devices may be included as an option if they provide sufficient shareable resources to be considered as "mass storage."

1.1.1 On-Line Storage (Space)

1.1.1.1 Description. This category includes the onboard storage technology that is potentially applicable in one or more of the following areas:

a. High speed/capacity buffering of downlink data to accommodate link bandwith and availability.
b. Rapid access storage for on-board data base management capability.
c. Recording capability for media that can be transported to space or to ground via Shuttle Transport System (STS).
d. High speed, moderate capacity devices that can be used for temporary storage, caches, or other specialized needs.

The onboard operational environment imposes additional unique requirements for mass storage systems. This includes space radiation, electro-magnetic interference, reliability, and constraints on physical size, weight, and power consumption. The option characteristics developed in this section reflect the importance of these environments (i.e. size, weight, power, radiation hardness, etc.).

Of particular importance is the radiation environment. While most mass storage media (i.e. magnetic tape, optical disk, magnetic disk, magnetic bubble) are inherently hard for anticipated levels, required support electronics might be more susceptable and need to be designed for radiation hardness or shielded in order to insure data quality.

The radiation environment consists of cosmic rays, the Van Allen Belt, and other sources of charged particles that significantly influence the selection of space qualified mass storage devices. This enviroment will result in total dose and single event (SEU) phenomena that can cause performance degradation, failure or logic "upset" in commercial components. This environment varies considerably with platform altitude and inclination and is statistical in nature due to the variations in proton flux of solar flares. The total dose environment is highest for a polar orbit (POP). The total dose per year is expected to be between 2000 and 25,000 Rads/year depending on solar conditions. Therefore, a reasonable total dose specification would be approximately 100,000 Rads for equipment expected to operate for 10 years. Lower levels of total dose may be specified if natural or intentional shielding is provided.

Heavy ions and energetic protons can cause upset of single locations in electronic circuitry, most notably in memory devices. These upsets are expected to become more critical as the feature size of the devices decrease and the complexity of the device increase. The degree to which these single event errors can be tolerated depends largely of the criticality of the application. For most mass storage applications, design/cost tradeoffs will determine the appropriate mechanism for operation in this enviroment (i.e. decreased component/media susceptability, error detection and correction coding, etc.). Expected upset rates can be calculated and designed around with reasonable confidence. Refer to section 3.5.1 for details on the space radiation environment model and appropriate alternatives for hardware space qualification.

The options described in this category are not restricted to current space qualified technology and includes those areas where such technology development has been initiated or significant potential is indicated for future development. The options in this category include:

- Magnetic Tape
- Magnetic Disk
- Optical Disk
- Bubble Memory
- Semiconductor

1.1.1.2 Option Characterization

1.1.1.2.1 Magnetic Tape (HDDR)

"High Density Digital Recording" (HDDR) is an option because it provides data storage at high density and at high speed on the magnetic tape media. These are characteristics appropriate for certain SSDS onboard mass storage requirements (i.e. buffering, etc.).

Magnetic tape systems have been used extensively as spaceborne mass storage systems. They were originally, in space applications, used for analog data storage, but recent advancements have made magnetic tape a good candidate for on-line mass storage of digital data where high capacity and high data transfer rates are required.

Digital data is stored on magnetic tape in one of two ways. Longitudinal recording is where the tape is passed over a fixed head that contains several data tracks. Benefits from longitudinal recording include long head/tape life, and less maintenance. The second method, rotary recording, involves passing the magnetic tape over a rotating head, thus storing data diagonally across the tape. This allows the tape to move at a slow speed, but achieve a high head to tape speed. The rotary recording technology promises higher data transfer rates and greater areal density on the media. Both techniques are mature and have a lower development risk then bubble memories or optical disk if current efforts in these areas continue. Both of these methods involve moving parts, therefore the reliability of the magnetic tape system is less then that of a solid state device like bubble memory. While the magnetic tape media itself is radiation hard (10^7 rads total dose), the control and logic circuits need to be designed to meet the environmental conditions of the on-orbit portion of the SSDS.

Magnetic tapes' performance characteristics include high transfer rate, high storage capacity, media reuseability, and proven space maturity. These characteristics make magnetic tape a candidate for buffering of uplink/ downlink data. An example of magnetic tapes' buffering capability was demonstrated on STS mission 41-G in October 1984. One of the mission goals was to use the SIR-B shuttle imaging radar to map a large part of the earths surface. Because there was a lack of a full time TDRSS link, an Odetics magnetic tape recorder was used to record the data, then replay it later when the TDRSS link was available. What data they could not transmit during the mission was brought back to earth on several reels of the magnetic tape. Because the magnetic tape device is sequential access, it is slow in random accessing of data, thus it probably will not be used in a data base application or in other applications where fast random access to the data is needed.

Some state of the art and future magnetic tape mass storage devices can be compared in figure 1.1-1.

	Odetics DDS-6000-EC	Ampex AHBR-17001	RCA 20 Mbit/s	Ampex SHBR-12
Total Storage (Gbits)	66	5	10	1000
Transfer Rate (Mbits/s)	50	105	20	340
Bit Error Rate	$1*10^{-6}$	$1*10^{-6}$**	$5*10^{-7}$	$1*10^{-6}$**
Recording Method	longitudinal	longitudinal	longitudinal	rotary
Shock & Vibration	Space Qual	Flight Qual	Space Qual*	Flight Qual*
Radiation Hardness				
Operating Temp. ^{o}C		5 to 50		
Power (max. watts)	280	1350	85	600
Weight (lbs)	154	225	81	200
Volume (inches cubed)	9080	10,450	2882	6150
Recurring Cost (dollars)	2,000,000	169,000	750,000	350,000
Production Start	1980	1984	1986	1987

* These units are being designed to meet these specifications
** No error correction, $1*10^{-8}$ with error correction

Figure 1.1-1: Magnetic tape recorder specifications

1.1.1.2.2 Magnetic Disk

Magnetic disk is a random access, read/write, digital data storage device that was first introduced in 1956 by IBM. Improvements such as thin film heads, Winchester methods, and improved disk surface materials have increased the

capacity of the magnetic disks by over a factor of 5000 since 1956. While other magnetic disk technologies (hard disk) have been flight qualified, their capabilities and physical characteristics are not as attractive as the newer Winchester disk drives. The Miltope RD-160 is a currently available, flight qualified, Winchester disk, that will store 1.07 Gbits of data, which the United States Army will use onboard aircraft for the ASAS program.

The ability to randomly access the data, and unlimited read/write are the magnetic disks' main advantages. A desirable characteristic of the Winchester technology is its ability to store a large amount of data in a small, light weight unit, thus making it a good candidate for space applications. As with magnetic tape, the magnetic disk media is inherently tolerant to radiation, but the logic and control circuits will need to be designed for the on orbit enviromental constraints. Also, as with magnetic tape, the magnetic disk system is made up of moving parts, thus the system is not as reliable as solid state devices. The magnetic disk is a candidate for use onboard the space station in a data base management system. Magnetic disk is also a candidate for use as temporary storage and in other specialized needs.

Some state of the art and future magnetic disk (Winchester technology) devices can be compared in figure 1.1-2.

	Miltope RD 160	Megavault Memories MV300
Total Storage (Gbits)	1.07	2.64
Transfer Rate (Mbits/s)	1.2	9.67
Bit Error Rate	$1*10^{-10}$	10^{-13}
Access Time	26 msec	18 msec
MTBF	10,000 Hr	12,000 Hr
Shock & Vibration	flight qual.	lab qual.
Radiation Hardness	EMP surviable	No Spec.
Operating Temp. ^{o}C	-10 to 55	10 to 46
Power (max. watts)	125	250
Weight (lbs)	35	30
Volume (inches cubed)	1764	580
Recurring cost	$25,000	$4200
Production Start	1984	1984

Figure 1.1-2: Magnetic disk specifications

1.1.1.2.3 Optical Disk

Optical disk is currently a random access, write once, unlimited read digital data storage device. It is an emerging technology that has matured rapidly since the first units were developed in the late 1970's. As of November 1984 the first commercial units are being delivered.

The optical disk system works much like the magnetic disk device. The media, a spinning disk coated with laser light sensitive material, is written and read with a laser light source. To write, the laser beam is focused onto the disk surface at an intensity high enough to cause a change in the disk surface. Depending on the technology used this change will either be a pit or a bubble. Currently this is a non-reversable process, but research has indicated that erasability is possible. To read, the laser at a lower power is focused onto the media. With the presence of a pit or a bubble the light will be reflected, thereby indicating a binary one.

The storage of large amounts of data, high data transfer rates, and rapid access to stored data are the main characteristics of optical disk. This would make optical disk a good candidate for storage of manuals, procedures and software. If erasable techniques can be matured optical disk would also be a candidate for data buffering and data base applications.

Currently there are no flight/space qualified optical disk devices being produced, but several companies have ongoing development efforts to make such a device. These companies include Miltope, RCA, and Lockheed Electronics Company. Both RCA and Lockheed are trying to develop an eraseable capability. The specifications for some of the proposed systems are given in Figure 1.1-3.

	RCA Dura Disk	RCA Optical Disk Buffer	Lockheed Optical Disk
Capacity (bits)	$5X10^{10}$/14" disk	10^{12}/system	$2X10^{9}$/5 1/4" disk
# of disks	1	12	1
Transfer Rate(bits/sec)	$4X10^{7}$	$1X10^{9}$	
Erasable	No	Yes	Yes
Weight (lbs)	150	700	
Power (watts)	300 (peak)	500 (ave)	
Volume (cubic inches)	5544	61,000	

Figure 1.1-3: Specifications of proposed optical disk systems

1.1.1.2.4 Bubble Memory

Bubble memories have been under development since 1967 when they were first developed in Bell Laboratories and with the first one Mbit bubble memory component introduced in 1979 by Intel Corporation. Bubble memory works by storing data on a thin magnetic material, typically garnet, that is positioned between two permanent magnets. The data is stored as magnetic cylinders arrayed in continuous loops. When the power is removed from the system the permanent magnets hold the magnetic cylinders in place. This gives bubble memories the characteristic of being a non-volatile, solid state mass storage device. Because current bubble systems use the non-radiation hard VMOS technology in some of their support chips, these bubble devices may be unacceptable for use in space applications. However, the USAF has recently issued a RFP to produce a space qualified, 4 Mbit bubble memory chip by 1987. Also, there are other USAF programs aimed at developing a radiation hard, space qualified chip set to support the bubble device. Temperature sensitivity is a another potential problem, but compensation techniques are being developed that increase the device operating temperature range.

Bubble memories have many applications, and many designs have already been developed that incorporate the bubble memory as the main data storage device. Some of these designs include a health maintenance monitor and a video image storage device. The versatile bubble memory can be configured to save power, or to provide fast data transfer rates, depending on the application. The problem is a lack of companies that manufacture the bubble memories, therefore, many of these good designs have remained on paper. Intel and Motorola are the only major domestic companies that remain in the bubble memory race that originally included big names such as Rockwell, Texas Instruments, and National Semiconductor. Also, development has not proceeded as planned. Intel had announced that a four Mbit bubble memory subsystem would be available in 1982, but as of Nov. 1984 they have only delivered prototype components. When size power and weight are considered, the bubble memory is a candidate for space applications where storage of up to 100 Mbits is needed. Specifications for some bubble memories are given in figure 1.1-4.

	Intel BPK 70A-5	Motorola MBM2011A	Intel 4 Mbit
Total Storage (Mbits)	1	1	4
Transfer Rate (Mbits/s)	.1	.1	.2
Bit Error Rate	$1*10^{-16}$	$1*10^{-11}$	$1*10^{-14}$
Access Time (average)	48 msec	11.5 msec	160 msec (worst case)
MTBF	40 years	> 10 years	> 30 years
Shock & Vibration	flight	flight	flight
Radiation Hardness			
Operating Temp. ^{o}C	-20 to 85	0 to 70	0 to 70
Power (max watts)	6.72		
Weight (lbs)*	.2	.2	.2
Volume (inches^3)*	6	6	6
Recurring Cost (ROM)	$200	$200	$400
Production Start	1979	1985	1984

* Also includes the support electronics

Figure 1.1-4: Bubble memory specifications

1.1.1.2.5 Semiconductor

Continued improvements in very large scale integrated (VLSI) technology make certain semiconductor technologies candidates for some low to moderate capacity mass storage applications. In this section we will consider only those technologies that are inherently non-volatile or have sufficiently low power requirements that backup battery power supplies could provide effective non-volatile capability. The applicable non-volatile technologies include:

1. Metal-Nitride-Oxide-Semiconductor Memory
2. Floating-Gate, Electron Tunneling, Metal-Oxide-Semiconductor

The applicable volatile technologies include:

1. Gallium Arsenide Memory
2. Complementry-Metal-Oxide-Semiconductor Memory

1.1.1.2.5.1 Non-Volatile Semiconductor

Metal-Nitride-Oxide-Semiconductor (MNOS) memory is an option for on-line (space) mass storage. The MNOS transistor permits stored data alterability simultaneously with stored data nonvolatility. It also provides a small-area structure and fabrication compatibility with high density, integrated circuit technologies.

McDonnell Douglas Microelectronics Center, (MDMC) has been working for some time to apply the MNOS memory technology to space solid state data recorder applications. MDMC's work has centered around utilizing MNOS in Adaptive Wafer Scale Integration (AWSI) techniques. AWSI is a concept which employs electrically alterable, nonvolatile interconnect controller circuits processed into a semiconductor wafer to connect "arrays" of interconnected, operable circuits (also processed into the wafer) to a bus structure deposited on the wafer between the arrays. With this approach, AWSI can have important advantages relative to other high density electronic circuit approaches. Such advantages potentially include: repeated electronic reconfigurability of interconnected circuits, compatibility with a wide variety of semiconductor processes, ability to select for yield, improved reliability, self-healing and fault tolerance, all plus reduction in size and weight.

MDMC has developed a wafer with the characteristics in figure 1.1-5.A. By designing the wafers to be easily interconnected, systems of any size can be developed. The characteristics of a proposed system are seen in figure 1.1-5.B. Westinghouse and others are also involved with MNOS technology but MDMC is the only company trying to utilize the AWSI techniques.

Storage Capacity	$5X10^5$ bits
Transfer Rate	up to 1.5 Mbits/sec
Recurring Cost	$500/waffer
Power	.25 watts peak
Radiation Hardness	10^5 - 10^6 Rad (si) Total dose
Endurance	> 10^8 write/erase cycles
Weight	.025 lb
Year	1984

Figure 1.1-5.A: AWSI memory wafer developed by MDMC

Storage Capacity	$1X10^9$ bits/system	$1X10^6$ bits/wafer
Interconnected wafers	1000	
Transfer Rate	up to 2.7 Mbits/sec	
Recurring Cost	$250,000/system	
Power	25 watts peak (at a 2.7 Mbit/sec transfer rate)*	
Radiation Hardness	10^5 - 10^6 Rad (si) Total dose	
Weight	26 lb/system	
Year	1987	

* System power is proportionately related to the transfer rate

Figure 1.1-5.B: Proposed MDMC AWSI solid state mass storage system

Floating-Gate, Electron Tunneling, Metal-Oxide-Semiconductor (FETMOS) is an option for on-line (space) mass storage because it provides non-volatile, randomly accessable, high density data storage. The FETMOS memory cell stores data by trapping a charge on its floating (isolated) poly-oxide gate. The cell may be erased by back-biasing the substrate of the cell. In this manner data is stored and erased. Once data is stored it can typically be accessed in 200 nSec. The state of the art devices have a 64 Kbit capacity and consume around 1.25 watts (peak). The data transfer rate of a FETMOS memory system depends mainly on the on how the device is integrated into a particular memory system. A major drawback to the FETMOS memory is its low endurance of 10^4 to 10^6 write/erase cycles. This would make FETMOS memory unsuitable for applications where there is large turnover of data. The FETMOS structure has a radiation hardness of 10^6 rads(si) total dose. Some state of the art FETMOS memories can be seen in figure 1.1-5.C.

	Motorola MCM2864	Intel 2864-2
Total Storage (Kbits)	64	64
Read Access Time(nsec)	200	200
Endurance (write cycles)	10,000	10,000
Data Nonvolatility	10 years	10 years
Peak Operating Power	1 Watt	500 mWatt
Recurring Cost	Not Available	Not Available
Production Start	1986	

Figure 1.1-5.C: FETMOS memory specifications

1.1.1.2.5.2 Volatile Semiconductor

Among the volatile semiconductor memories GaAs and CMOS were selected as the most likely technologies to be considered due to their low power requirements, allowing for the possibility of using battery backup to provide the non-volatile capability.

Gallium Arsenide (GaAs) memory is an option for on-line (space) mass storage because of its radiation hardness, low power consumption, and high speed. The GaAs structure is extremely fast. It has been projected that 2-10 GHz logic and 40 GHz transistors will be possable using GaAs technology. Coupled with its high tolerance to radiation (> 10^7 rads (GaAs)) and its low power consumption (.5 microwatts/bit) the GaAs memory shows great promise as a space qualified memory. Currently there are several companies developing GaAs memory devices. Included among these are: McDonnell Douglas Microelectronics Center (MDMC), Rockwell, and Hughes. Current efforts are being applied to the development of a 4 Kbit memory chip. There is also an effort by MDMC to develop a space qualified, 16 Mbit GaAs memory system for use in a space platform in the 1988 time frame. This memory system would use 10 watts of power in its standby mode and have a 10 nsec access time. The only drawback to the GaAs memory is that it is an emerging technology, but given enough time it will become a major part in space qualified memory systems.

Complementary-Metal-Oxide-Semiconductor (CMOS) is an option for on-line (space) mass storage because of its fast access, low power requirements, and high density data storage. CMOS memory is the most mature of the solid state memories that have been investigated for use as on-line (space) mass storage. CMOS memories have had commercial success and are under continual development. One of the state of the art devices is the Harris HM-65262, a 16 Kbit static RAM chip. Harris is also developing a 64 Kbit static RAM chip that should be available by mid 1986. Also produced by Harris are hybrid modules capable of storing 256 Kbits of information, and after the 64 Kbit chip is developed they plan on integrating it into a 1 Mbit hybrid module. Typical performance characteristics for a 16 Kbit CMOS static ram chip are: 250 microwatts power consumption in the standby mode, 350 milliwatts power consumption when operating, and an access time of 55 nSec. The performance of a 256 Kbit module is: 2.5 milliwatts in standby, 150 milliwatts peak operating power, and a 170 nsec access time. Radiation hard CMOS memories are available and exhibit a total dose tolerance of 10^5 rads (si).

1.1.1.3 Projected Capabilities

Each mass storage option was researched to determine the trends in their various characteristics. One useful trend was the analysis of bits stored per square inch on the recording medium vs. year. Using the plot of this information, seen in figure 1.1-7, and a standard medium size, the total capacity per unit of medium (i.e. one reel of tape, one optical disk, etc.) can be derived. Other trends used include: Data rate vs. year, and weight/bit vs. year. Personal contacts with industry and government personnel were another source of information used in making the predictions. Using this information, the generic models of the mass storage options that can be developed and mature by 1992 were produced and can be seen in table 1.1-6. These generic models represent devices that can be built if designed with maximum capacity and bandwidth in mind. Tradeoffs can be made that downgrade the performance of the devices in order to gain benifits in the areas of power, weight, and volume.

	Total Capacity (bits)	Transfer Rate (Mbits/sec)	Access Time (msec)	Peak Power (watts)	Volume ($inch^3$)	Weight (lbs)
Magnetic Tape:	10^{12}/tape	500	NA	500	10,000	150
Magnetic Disk:	$3X10^9$/system	20	20(ave)	200	600	50
Optical Disk:	10^{12}/system	1000	166(ave)	500(ave)	61,000	700
Magnetic Bubble(1):	$16X10^6$/chip	.4	10(ave)	8	6	.2
Semiconductor(1):						
MNOS (AWSI)/wafer	$1.25X10^6$	NA(2)	10 usec(3)	.25	3	.025
FETMOS/chip	$256X10^3$	NA(2)	400 nsec(3)	8	.5	.05(4)
GaAs/chip	$16X10^3$	NA(2)	15 nsec(3)	6.4	.5	.05(4)
CMOS/chip	10^6	NA(2)	1 usec (3)	4	.5	.05(4)

Notes:

(1) Represents a building block that can be used for a TBD design (i.e. any capacity, any transfer rate depending on power, size, and weight constraints)

(2) Transfer rate will be dependent on how the device is integrated into a system

(3) Read access time

(4) Chip is packaged in a ceramic dual in-line package

Table 1.1-6: Generic models of 1992 mass storage devices

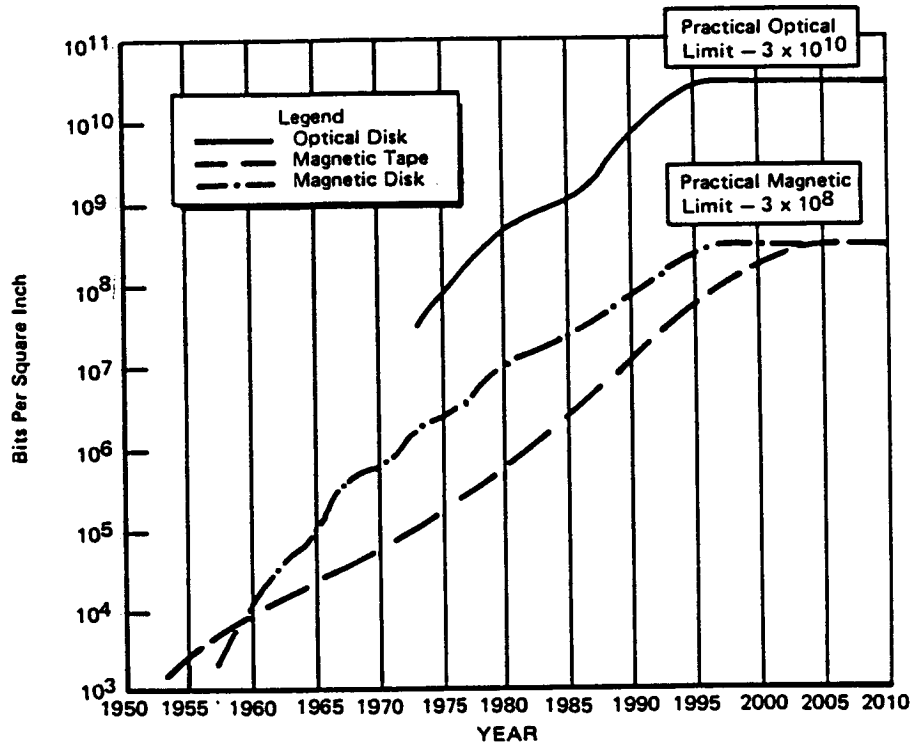


Figure 1.1-7. Projected Trend of Area Density Versus Year

1.1.1.3.1 Magnetic Tape

The generic model of a magnetic tape storage device presented in table 1.1-6 represents a machine that can be available by 1992 if designed with maximum capacity and bandwidth as the main objective. The improvements in the device will result mainly from new high energy tape that allows narrower head gaps which increase the density per track, and narrower head widths which allow more recording tracks. There are tradeoffs that can be made that affect the power consumption and weight of the device vs. the performance characteristics. Using a transfer rate tradeoff a machine with the characteristics in table 1.1-8 can be developed for use in missions not requiring a great deal of capacity or bandwidth. Another important tradeoff, which will affect power consumption, system life, weight, and complexity is the use of longitudinal recording vs. rotary recording. With the longitudinal recorder the benifit will be a device that is easier to maintain, but in order to get the higher data rates and data density additional recording tracks must be added, thus increasing the electronics part count considerably which in turn increases the system weight and power consumption. Rotary recording on the other hand gives the increased data rates and data density without a major increase in the electronics, but at the expense of head life, thus increasing the need for system maintenance.

Total Capacity	25 Gbits/tape
Transfer rate	200 Mbits/sec.
Power Consumption	100 watts (max)
Volume	3000 cubic inches
Weight	100 pounds
Recording Method	Rotary

Table 1.1-8: Characteristics of a medium capacity magnetic tape storage device

1.1.1.3.3 Optical Disk

Because of the newness of optical disk technology, the generic model shown in table 1.1-6 is based on actual development efforts rather then on historical trends. The device show will be eraseable and may be a critical element in the SSDS because it would greatly simplify the design of buffers and give the necessary capacity needed by some of the data stores. Current indications are that a device with the characteristics presented in table 1.1-6 can be developed and matured by 1992 if proper funding is supplied in a timely manner.

1.1.3.4 Magnetic Bubble

The current trends in magnetic bubble production indicate that by 1992 a 16 Mbit, space qualified bubble memory chip set will be available. Ongoing development effort also indicates that the temperature sensitivity problem should be solved with the use of compensation techniques.

1.1.1.3.5 Semiconductor

Semiconductor memory has a well defined learning curve for the various options. Development typically goes in factor of four increments every four years. Using this information, devices of the size shown in table 1.1-6 should be mature and available by 1992. The one exception might be the CMOS random access memory (RAM). The prediction of a 1 Mbit chip follows the established trends, but some experts in the field feel that only a 256 Kbit chip will be available. Even so, a 4 Mbit CMOS hybrid is a likely possibility.

GaAs memories are an area of particular interest because of the high speed and high tolerance to radiation that they exhibit. With proper funding a 64 kbit chip could be developed by 1992, but at current funding levels a 16 kbit chip will be available as shown in table 1.1-6.

The MNOS memory is being developed at the typical rate, and should be well suited to construct memory systems of 1 Gbit capacity before 1992.

1.1.1.4 Comparisons

Each option presented has characteristics that make it more favorable to some applications then the other options. To identify which options have the advantage in which applications requires that comparisons between the options be done. Preliminary relation of options to application can be seen in section 1.1.1.5. Final relation of the options to the applications will be done in a trade study (Task 3). A general comparison of the options performance characteristics can be seen in table 1.1-6. Other comparisons that are important for space applications include:

1. Cost vs. capacity
2. Weight vs. capacity
3. Volume vs. capacity

Each comparison will be done using the generic models developed in section 1.1.1.3. Not all comparisons will apply to all the options.

1.1.1.4.1 Cost vs. capacity

Using the cost/bit vs. year trends (figure 1.1-11) the costs were developed for the IOC generic devices presented in table 1.1-6. Table 1.1-9 contains the results of the cost analysis. Plotting this information in the form of dollars vs. capacity gives figure 1.1-12. It can then be seen that bubble memory is the cost effective option from 0 to $1X10^{11}$ bits. From $1X10^{11}$ on, Magnetic tape is the cost effective option. For capacities below $5X10^{8}$ MNOS is more cost effective than Magnetic disk. Optical disk was not included as not enough cost information was available to make accurate predictions.

Option	Cost per Bit (dollars)
Magnetic Tape	$7.5X10^{-7}$
Magnetic Disk	$3.7X10^{-6}$
Bubble	$6.25X10^{-6}$
MNOS	$3.12X10^{-5}$

Table 1.1-9: Cost per bit of 1992 generic options

1.1.1.4.2 Weight vs. capacity

By using the projected weights in table 1.1-6, a plot of weight vs. capacity was made and presented in figure 1.1-13. Table 1.1-10 gives the rankings, 1 being best, for storage less than 10^{9} bits and for storage greater than 10^{11} bits. For storage requirements from 10^{9} to 10^{11} it appears that several of the options, bubble, magnetic disk, MNOS, and magnetic tape all give about the same weight effectiveness.

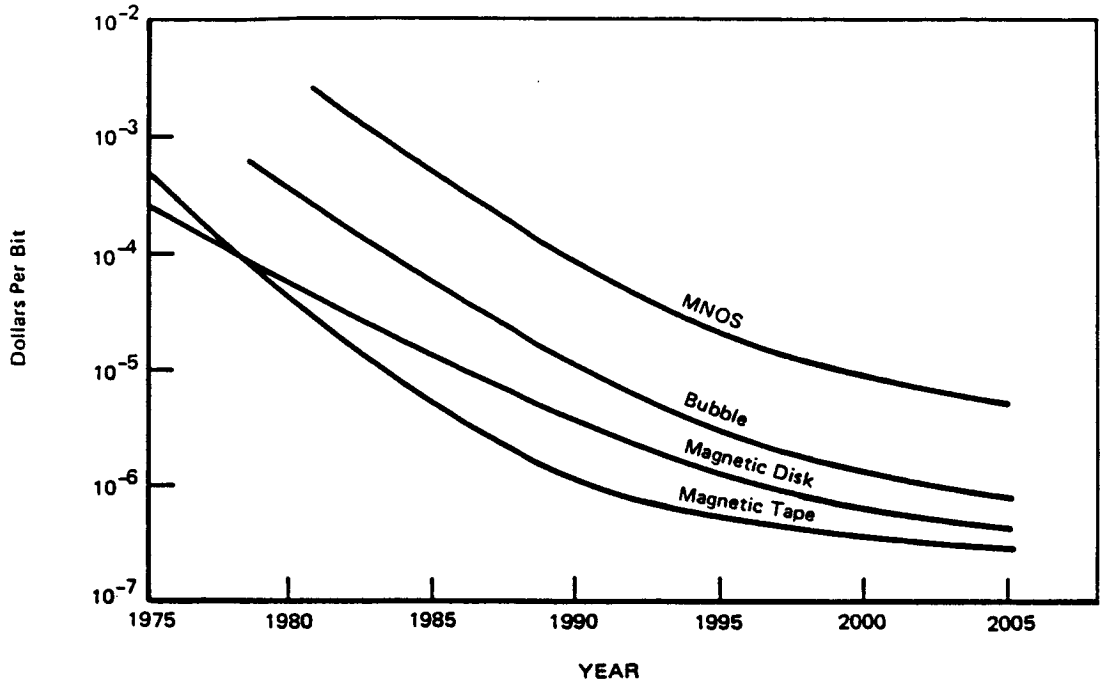


Figure 1.1-11. Cost Per Bit Versus Year

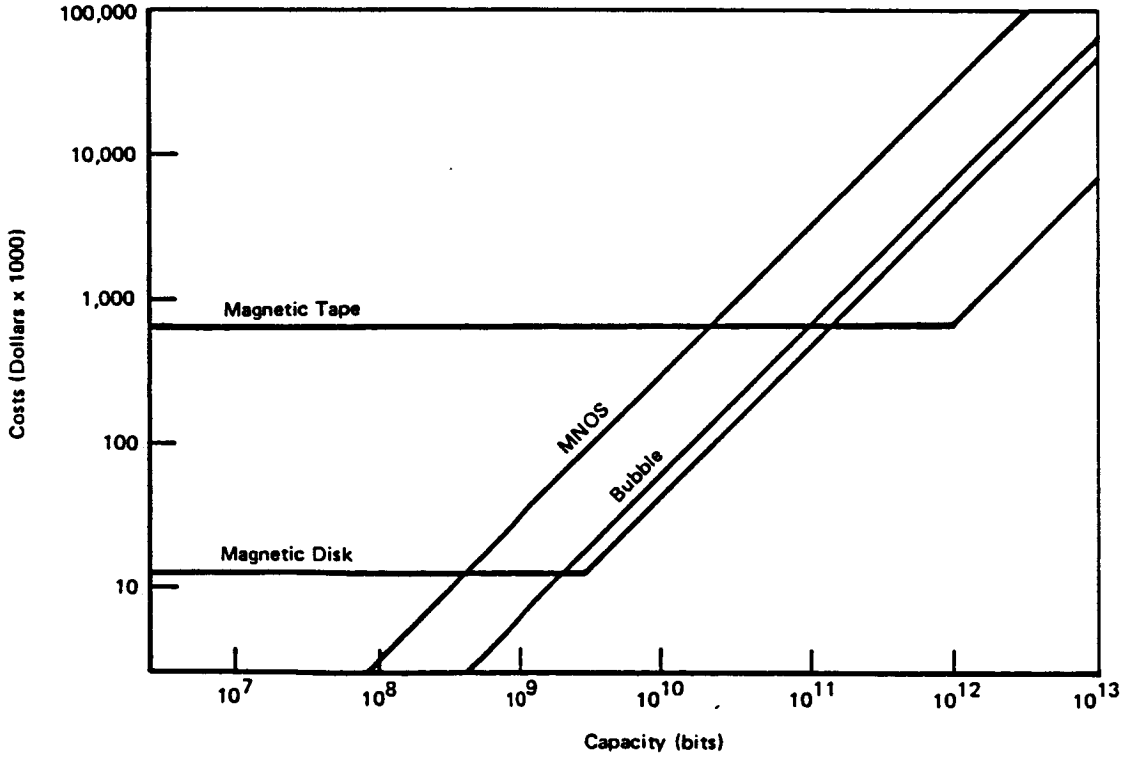


Figure 1.1-12. Cost Versus Capacity at 1992

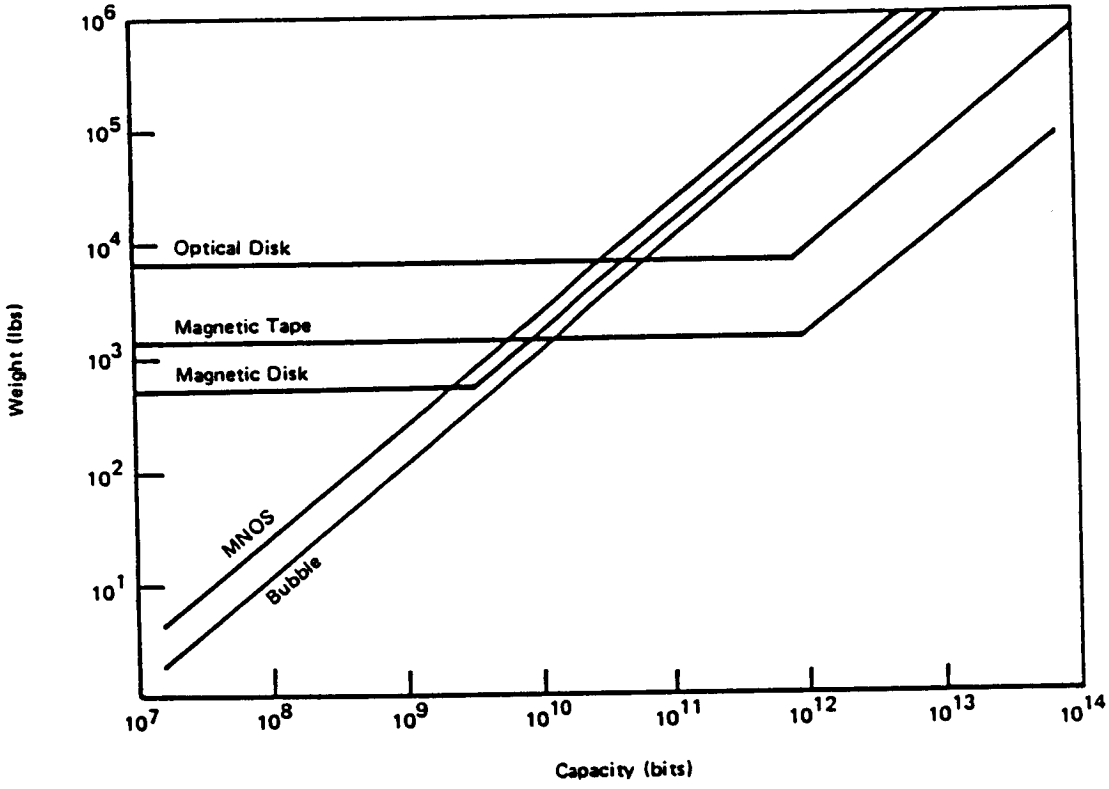


Figure 1.1-13. Weight Versus Capacity for 1992 Generic Devices

Ranking	Storage Capacity	
	$<10^9$	$>10^{11}$
1	Magnetic Bubble	Magnetic Tape
2	MNOS (AWSI)	Optical Disk
3	Magnetic Disk	Magnetic Bubble
4	Magnetic Tape	Magnetic Disk
5	Optical Disk	MNOS (AWSI)

Table 1.1-10: Rankings for weight effectiveness for mass storage options

1.1.1.4.3 Volume vs. capacity

By using the projected volumes from table 1.1-6 the plot for volume vs. capacity for the 1992 generic mass storage options was constructed and is shown in figure 1.1-16. From figure 1.1-16, the ranking shown in table 1.1-14 were developed for capacities less than 10^9 bits, capacities from 10^9 bits to 10^{11} bits, and capacities greater than 10^{11}.

Ranking	Storage Capacity		
	$< 10^9$	$10^9 - 10^{11}$	$> 10^{11}$
1	Magnetic Bubble	Magnetic Disk	Magnetic Tape
2	MNOS (AWSI)	Magnetic Bubble	Optical Disk
3	Magnetic Disk	Magnetic Tape	Magnetic Disk
4	Magnetic Tape	MNOS (AWSI)	Magnetic Bubble
5	Optical Disk	Optical Disk	MNOS (AWSI)

Table 1.1-14: Rankings for volume effectiveness for the mass storage options

1.1.1.5 Application

Using the information developed in 1.1.1.3 and 1.1.1.4 it is possible to make a preliminary relation of options to applications. The relation of the candidate options to particular applications can be seen in table 1.1-15. The task 3 trade study will do more extensive comparisons to make final relation of particular options to applications.

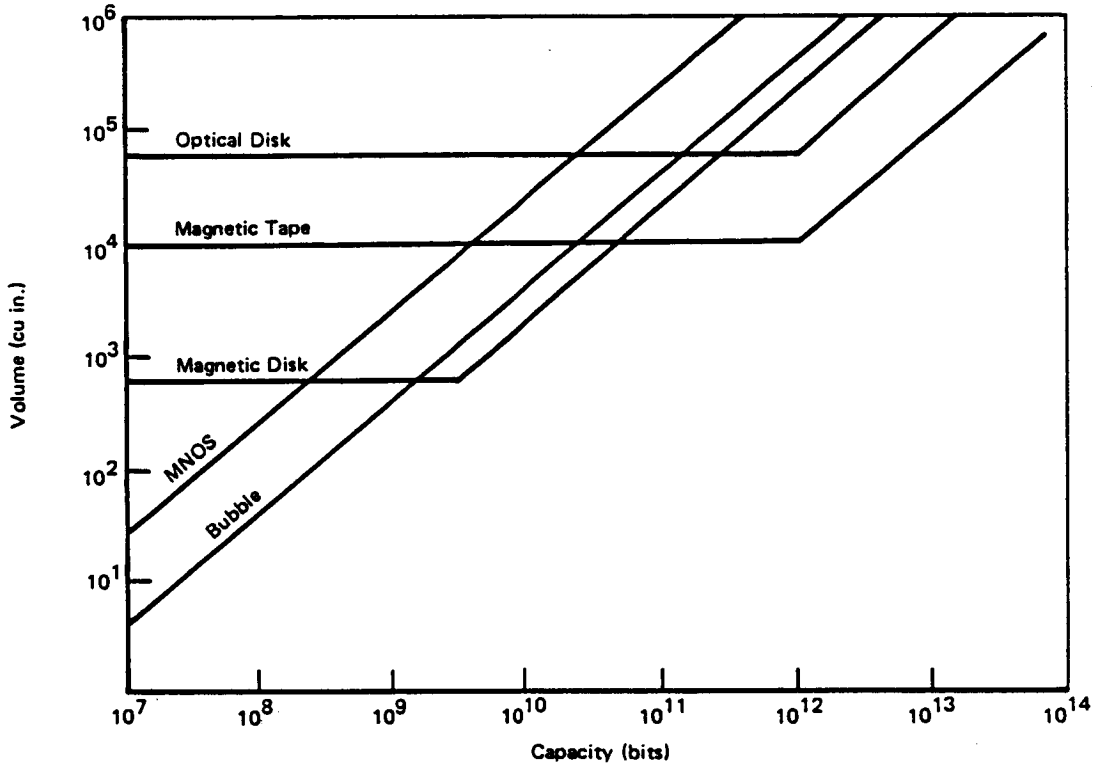


Figure 1.1-16. Volume Versus Capacity for 1992 Generic Options

	MAGNETIC TAPE	MAGNETIC TAPE	NON-ERASABLE OPTICAL DISK	ERASABLE OPTICAL DISK	MAGNETIC BUBBLE	SEMICONDUCTOR
ON-ORBIT BUFFERING	X	X		X	X	
ON-ORBIT DATABASE	X	X	X	X	X	X

Table 1.1-15 Preliminary relation of candidate options to application

1.1.2 On-Line Storage (Ground)

1.1.2.1 Description. This category includes the storage technology that is potentially applicable to the more global needs of the ground based portion of the SSDS. While a large variety of storage technologies will probably be used for a wide range of ground based applications, this section will focus on the more stressing requirements including the following:

a. Ground station buffering and/or contingency recording of TBD bits, TBD rate raw data.
b. One week storage of TBD bits of extracted customer data with a minumum of 12 hours of on-line data.
c. 0.5 seconds to 1 hour access storage for data base management of engineering and operational data.

The options in this category include the following:

- Magnetic Tape (HDDR)
- Magnetic Disk
- Optical Disk
- Optical Tape

1.1.2.2 Option Characterization

1.1.2.2.1 Magnetic Tape (HDDR)

"High Density Digital Recording" (HDDR) is an option because it has speed/density characteristics suited to meet some of the driving requirements of the ground based portion of the SSDS. Other recording methods, like the standard computer compatable units (6250, etc.), will be used in many less critical applications, and will not be described here.

With the newer magnetic tape recording technologies, data is recorded at high speed and high density on the magnetic tape media. Ampex has a prototype machine that will store $1x10^{12}$ bits on a 9200 foot reel of two inch wide magnetic tape at 340 Mbits/sec. The total physical volume of the tape is approximately 300 cubic inches, thus $3.33x10^{9}$ bits are stored per cubic inch. This characteristic, coupled with the data transfer rate of 340 Mbits/sec makes magnetic tape an attractive candidate for short term archiving. If the tape is stored in the proper environment the data quality can be maintained for a period greater than 25 years, thus making magnetic tape a good candidate for long term data archiving. Magnetic tape has also proven itself a candidate for use in data buffering applications. Comparisons of state of the art devices can be seen in table 1.1-17.

	Ampex HBR 3000i	Ampex SHBR 12	RCA HDMR-500	Honeywell HD 96
Total Storage(Gbits/tape)	5	1000	135	119
Transfer Rate (Mbits/s)	120	340	230	186
Bit Error Rate	1*10-8	1*10-6 *	1*10-6	1*10-6 *
Recording Method	longitudinal	rotary	longitudinal	longitudinal
Recurring Cost	$150,000	$350,000	$1,000,000	$175,000.
Media Cost	$300	$450	$450	$300
Production Start	1984	1987	1986	1984

* Without error correction

Table 1.1-17: Magnetic tape specifications

1.1.2.2.2 Magnetic Disk

Magnetic disk is a random access, read/write, digital data storage device that was first introduced in 1956 by IBM. With its large storage capacity and fast access times magnetic disk has become the main secondary storage device for both large and small computer systems. They are now in use storing the ever changing information of many large data base systems.

A major issue for large capacity magnetic disk devices is the use of fixed media or removable media. The advantage gained by the fixed media device is greater storage capacity, and the advantage of the removable media is the ability to archive data and physically transfer data to other locations. Using removable media magnetic disk drives for archival storage seems unlikely because the disks are mounted in a "pack" which makes inefficient use of physical storage space. The main use of the magnetic disk device could be in a data management system where the data is continually being updated.

Another issue is the lack of development being done on high performance magnetic disk drives for the high performance "supercomputers". This affects the SSDS in that a high performance device, that may be needed to accommodate a driving requirement, may not be available. The economic factors involved are the obvious reason for this. Most of the major development is being done on the magnetic disk drives that are used with the mini computers. Many of the developments made in this field can be transferred to the high performance machines, but more effort in the development of high performance disk drives has to be made if the full potential of these devices is to be realized. Some specifications for current state of the art high performance devices can be seen in table 1.1-18.

	IBM 3380	CDC 885-42	CDC 895-1
Total Storage (Gbits/sys)	20	8.3	19.2
Transfer Rate (Mbits/s)	24	38.3	24
Access Time (msec)	16	25	16
Recurring Cost	$90,000	$76,000	$94,000
Production Start	1984	1984	1984

* BER Information Not Available

Table 1.1-18: Magnetic disk specifications

1.1.2.2.3 Optical Disk

Optical disk is currently a random access, write once, unlimited read digital data storage device. It is a new technology, but has matured rapidly since the first units were developed in the late 1970's. As of Nov. 1984 production units are starting to be delivered.

An optical disk system consists of a laser source, a detector, optical system to direct the laser beam, the drive system and the optical disk. Writing to the disk is done by one of two means. The first method involves burning a hole through the top layer of the disk to uncover a reflective bottom layer. The second method involves heating the metal base of the disk, which creates a gas, which in turn forms a reflective bubble in the top layer of the disk. Each of these reflective spots represents a one and the lack of a reflective spot represents a zero, thus data is recorded on the disk. To read data the laser, at a lower power, is focused onto the disk. Any reflections are picked up by the detector and are interpreted as binary ones.

An RCA Jukebox system is already in place at NASA MSFC for use in the storage of satellite data. Likewise, a Storage Technology Corp. (STC) optical disk system is installed at the National Center for Atmospheric Research at Boulder, Co. for the storage of satellite data.

Companies such as Filenet Co. and Integrated Automation are involved in building optical disk jukeboxes around existing optical disk devices. These jukeboxes typically hold around 100 disks. There is a port that allows the insertion and removal of optical disks from the jukebox, thus there is potential for these jukeboxes to be used in storing both on-line and off-line data.

The characteristics of an optical disk system include: large storage capacity, fast data transfer rates, low bit error rates, low cost removable media, non-eraseability (which might be an advantage in long term data archiving). The optical disk media is space efficient as current technology allows storage of .25 Gbits per cubic inch. These characteristics make the optical disk system a good candidate for ground based, long term data archiving. If development on an unlimited read/write system is mature enough the optical disk system could be used for a ground based, data base information storage system where data needs to be updated constantly.

At present the optical disk is a write once technology, but development is now being done on a full read/write optical disk technology that also utilizes the magnetic properties of the disk surface. This technique is known as magneto-optical disk recording. The media is made of a material that is magnetically stable when cool, but unstable when heated. Initially the material has the same magnetic direction, thus the disk is blank. To write, the media is passed over a magnetic field that is in the opposite direction to the inital magnetic state of the material on the disk. Simultaneously, a laser heats the spot where data is to be written, thus allowing the material that was heated to take on the magnetic polarity of the external field. This is the manner in which data is written to the disk. To read data, the laser beam, at a lower power, is focused onto the disk. Because of the Kerr effect, the polarized vector of the reflected light will be rotated depending on the magnetic field of the material. This rotation can be detected by a photodiode arrangement. Erasure of the media is accomplished a track at a time by changing the external field back to the initial direction of the magnetic field of the disk, then heating the track with the laser. This results in the magnetic field of the track being set back to the original state. This method shows promise because it achieves the high storage capacity of optical disk, plus the eraseability of the magnetic disk. Although there are no units yet available, some companies feel that this technique has enough promise to fund further research and development.

Because high density optical disk is an emerging technology, the development risk is medium. Industry is putting a lot of money into the development of these devices, and if the read/write capability matures, they will begin to compete with the magnetic disk technology as a main secondary storage device. Some state of the art devices are compared in table 1.1-19.

	RCA JUKEBOX	STC 7600	SHUGART OPTIMEM 1000
Total Storage (Gbits/disk)	80 X 128 disks	32	8
Transfer Rate (Mbits/s)	50	30	5
Bit Error Rate	$1*10^{-8}$ *	$1*10^{-13}$ *	$1*10^{-12}$
Access Time	5.5 sec**	61.9 msec	100 msec
MTBF	2000 hrs		5000 hrs
Recurring Cost	$2,000,000 (ROM)	$130,000	$12,500
Media Life	> 10 years	> 10 years	> 10 years
Media Cost (per disk)	$500	$350	$350
Production Start	1982	1984	1984

* With error correction
** Includes time to retrieve and mount disk

Table 1.1-19: Optical disk specifications

1.1.2.2.4. Optical Tape

DOCdata from the Netherlands has a plan to store 600,000 Mbytes in one optical tape jukebox. The unit would consist of 100 optical tape cassettes, which hold 6000 Mbytes of information each, in a jukebox arrangement. Each cassette would hold 273 yards of the optical tape media, which is made of two transparent layers separated by a metal layer. The transparent layer furthest from the read/write head has preformed holes 4 um apart. The metal layer hides the holes until data is written to the tape. During writing the write laser would melt the metal into the hole.

The writing method utilizes a parallel array of several hundred gallium aluminum arsenide laser diodes. This presents a significant reliability problem in that it is estimated that 10% of the lasers will be defective without any way of replacement, which necessitates a 40% overhead correction coding method. Also, the wiring interface for the diode array is a major problem.

The operating concept sounds promising, but the technology is still too immature to fully assess its future potential and risk.

1.1.2.3 Projected Capabilities

The projected capabilities for the mass storage options were derived using analysis as described in section 1.1.1.3 and also using personal contacts. The objective was to develop generic models of the options that represent the highest capacity, highest speed devices that can be available by IOC. The generic models for on-line mass storage (ground) can be seen in table 1.1-20.

	Capacity Gbits	Transfer Rate Mbits/sec	Media cost dollars
Magnetic Tape	5000/tape	1000	500
Magnetic disk	35/device*	40	NA*
Optical disk	533/disk	100	30

* Fixed disk device

Table 1.1-20: Generic models for on-line mass storage (ground)

1.1.2.3.1 Magnetic Tape

Following the current trends, magnetic tape will have very good characteristics. The improvements in this option will result from a combination of new high energy tapes, and new head technology that will take advantage of the new tape and allow greater areal density and higher data transfer rates.

1.1.2.3.2 Magnetic Disk

The improvements in magnetic disk technology will come from new thin film heads, vertical recording techniques, and new methods of coating the disk surface. Recently, the rate of improvement in magnetic disk technology for main frame and super computer applications has slowed. This is a result of inadequate funding for the development of these devices. This area will have to be addressed before magnetic disk is ever to reach its potential.

1.1.2.3.3 Optical Disk

As important as the increased performance of the optical disk device in table 1.1-20 is that this optical disk device should be eraseable. Magneto-optical disk is the ways that this may come about, although a phase change method might also work.

1.1.2.4 Comparisons

Each option has characteristics that make it a better candidate for some applications then others. By making various comparisons the best option for each application can be chosen. Preliminary relation of the options to various applications can be seen in section 1.1.2.5. The general performance characteristics of the expected IOC options can be compared in table 1.1-20. Other applicable comparisons include:

1. Cost of the media

1.1.2.4.1 Cost of the Media

Using the projected media costs, it can be seen that eraseable optical disk is more cost effective than magnetic tape. This is illistrated in figure 1.1-22. The resulting media cost per bit is:

Magnetic Tape $\$10^{-10}$/bit
Optical Disk $\$5.6X10^{-11}$/bit

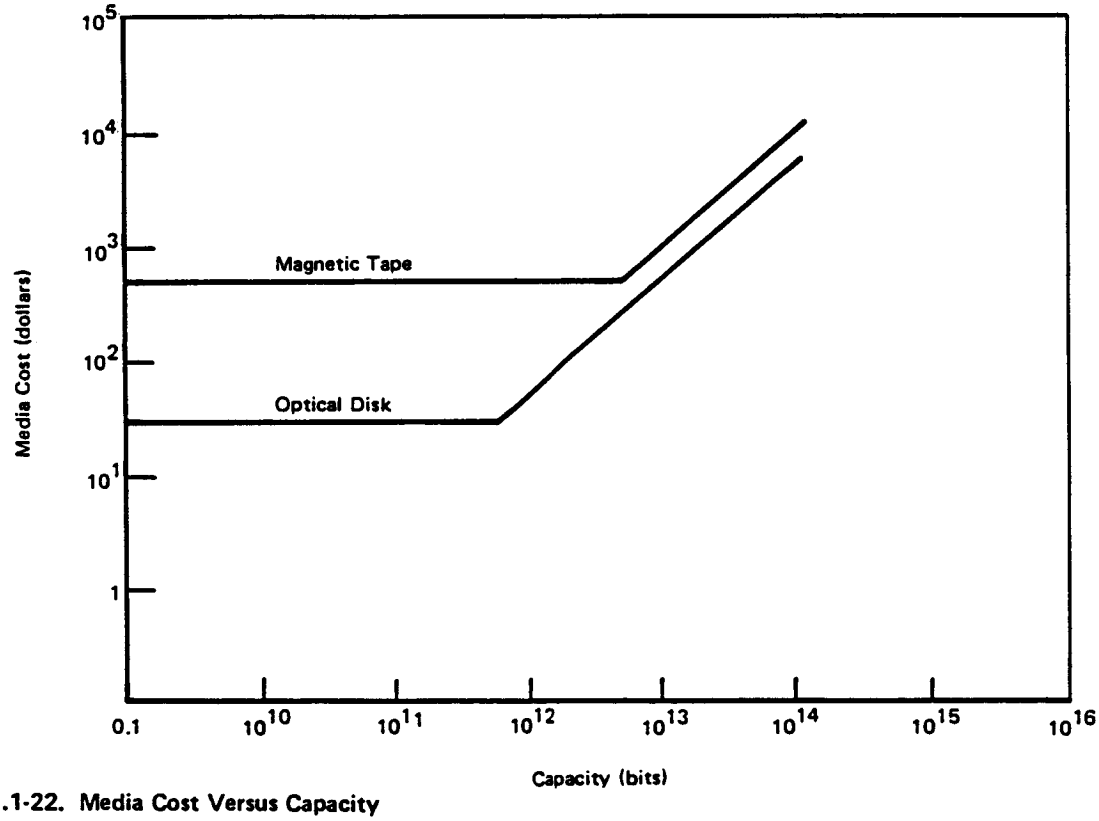


Figure 1.1-22. Media Cost Versus Capacity

1.1.2.5 Application

Using the information developed in 1.1.2.3 and 1.1.2.4 it is possible to make a preliminary relation of options to applications. The two driving applications that need to be considered are:

A. On-ground buffering
B. On-ground archiving

The preliminary relaton of the options to the applications is shown in table 1.1-21.

	MAGNETIC TAPE	MAGNETIC TAPE	NON-ERASABLE OPTICAL DISK	ERASABLE OPTICAL DISK	MAGNETIC BUBBLE	SEMICONDUCTOR
ON-GROUND BUFFERING	X	X		X	X	
ON-GROUND DATABASE	X	X	X	X		

Table 1.1-21 Preliminary relation of candidate options to ground storage applications

1.1.3 Off-Line Storage

1.1.3.1 Description

This category includes the storage technology best suited to meet the following off-line storage requirements:

1. Long term (> 2 years) archiving of engineering data
2. Storage of manuals, specifications, and procedures
3. Archieval of customer data for up to seven days, pending verification of receipt of each data set, with TBD time units access to the data.

The options in this category include the following:

1. Magnetic Tape
2. Optical Disk
3. Microfiche
4. Digitization techniques

1.1.3.2 Option Characterization

1.1.3.2.1 Magnetic Tape

See section 1.1.2.2.1 for characterization of magnetic tape.

1.1.3.2.2 Optical Disk

See section 1.1.2.2.3 for characterization of optical disk.

1.1.3.2.3 Microfiche

Microfiche is an option for the off-line storage of manuals, specifications, and procedures. Microfiche has been used for document storage since the 1940's with good results. Documents are stored by making a photo-reduced negative of the document. As many as 252 of these negatives can be arranged on a 4.1 inch by 5.86 inch card to make the master fiche. Copies of this master are easily and inexpensively made. Typically, the cost to produce the original fiche is around $10.00 and the cost to produce copies is 10 cents apiece. To compare data densities between microfiche and the other options, it is assumed that it takes a file of 400 Kbits to store an average A size document. Given that a single microfiche can store up to 252 A size documents, this equates to the storage of 100 Mbits of data per microfiche at an areal density of $4X10^6$ bits per square inch, which is in the neighborhood of the areal density of magnetic tape and magnetic disk.

The equipment to produce microfiche costs approximately $150,000 for a complete setup that can process about 900 documents per hour. The viewing equipment ranges from inexpensive (less than $500) microfiche readers to sophisticated computer retrieval and display systems. Image Systems Inc. (ISI) is a company that manufactures computer based microfiche systems. One of their systems, the ISI-4000 can store 780 microfiche cards in a carousel and access any document, on any fiche in under 3 seconds. The price for a basic ISI-400 is around $9000.

1.1.3.2.4 Digitization Techniques

Digitization techniques (converting paper data to digital data) is an option for off-line storage of manuals, specifications, and procedures. The basic digitization technique entails digitizing a document and storing the information on optical disk. Advantages gained from this technique include: centralized storage of up to date data, storage of non-textual images (i.e. engineering drawings, etc.), and fast access to the off-line data. Companies currently developing such digitization systems include Integrated Automation, and Filenet Corporation.

A typical scenario for the use of a digitization system is as follows. After producing an engineering drawing, an engineer would take it to a central document control station, where it would be fed through a document scanner. The document scanner would convert the drawing from its paper form to a digital file. This digital file would then be cataloged and stored on an optical disk that is contained in an automated jukebox. This jukebox would typically contain 100 optical disks. Disks may also be inserted and removed through a special port, thus allowing for off-line storage of the data in a library. Anybody needing to use the drawing may now call it up on a high resolution screen. If a hardcopy is desired it can be produced on a high quality laser printer. The advantages of the above scenario include: access to centrally stored, up to date drawings, computerized storage of images, and fast access to the data. Central storage of data is important because it allows everyone to have access to the same drawings, thus preventing the situation where somebody still has out of date information in their own filing cabinet.

The cost breakdown of a typical system is as follows:

Document entry station	$37,000
Optical disk jukebox	$100,000
Workstation	$15,000
High quality laser printer	$10,000

1.1.4 References

1. "The Multiple Format Data Handling Center Study", Control Data Corporation for NASA Contract No. NAS5-27691, November 1984.

2. "Space Platform End-to-End Data System Study", McDonnell Douglas Corporation for NASA Contract NAS8-33592, April 1981.

3. "Space Systems Technology Model", NASA, January 1984

4. "Memory Technology Survey", McDonnell Douglas Corporation for NASA Contract No. NAS5-25599, February 1981.

5. Bellmer and Davis, "Magnetic Bubble Memories: Technology and Application", Military Electronics/Countermeasures, August 1983.

6. "Non-Volatile Memories Rejuvenate as Bubble Prices Burst", Mini-Micro Systems, November 1983.

7. Dick Pierce, "Bubble Memories for Image Storage", Electronic Imaging, April 1984.

8. Robert Stermer, "A Spacecraft Mass Memory Design Using Self-Structured Magnetic Bubbles", NASA-LaRC, 1980.

9. Mike Cashman, "Solid State Memories Continue Pace", Digital Design, April 1984.

10. "Tinier Bubbles", Solutions, January/February 1984.

11. Grover Sims, "A Portable Physiological Data Recorder Using Magnetic Bubble Memory", Thesis, Air Force Institute of Technology, April 1983.

12. McLaughlin, "Large Disks: Greater Capacities, Greater Choices", Mini-Micro Systems, June 1983.

13. Robert Rosenberg, "Magnetic Mass Storage Densities Rise", Electronics Week, October 29, 1984.

14. Raymond Freeman, "The Future of Peripheral Data Storage", Mini-Micro Systems, February 1982.

15. Miller & Freese, "Recording Densities Push the Limits", Mini-Micro Systems, October 1983.

16. Edward Teja, "Disk Drives", EDN, June 28, 1984.

17. Norton & Losee, "Floppy-Disk Cartridge Challenges Winchesters", Mini-Micro Systems, February 1982.

18. Alan Bell, "Critical Issues in High-Density Magnetic and Optical Disk Storage", Laser Focus, August/September 1983.

19. Maarten De Haan, "Optical Memory Research Pays Off", Computer Design, October 1, 1984.

20. Mausd Mansuripur, "Disk Storage: Magneto-Optics Leads the Way", Photonics Spectra, October 1984.

21. Keith Jones, "DOCdata Plans to Made 6,000MByte Optical Tape Cassette", Mini-Micro Systems, June 1984.

22. David Davies, "Developments in Optical Disk Recording", Engineering Manager, November 1984.

23. Steve Moore, "The Mass Storage Squeeze", Datamation, October 1, 1984.

24. Alan Bell, "Optical Data Storage", Laser Focus, January 1983.

25. David Freedman, "Optical Disk: Promises and Problems", Mini-Micro Systems, October 1982.

26. Robert Hirshon, "Optical Storage Meets Increased Data Demands", Electronic Imaging, March 1984.

PERSONAL CONTACTS

1. Ken Wallgren NASA-HQ
2. Jack Hayes, NASA-Goddard
3. Gene Smith, NASA-Goddard
4. Paul Hayes, NASA-LaRC
5. Ed Caro, NASA-JPL
6. Doug Thomas, NASA-MSFC
7. Stu Cummins, USAF W-P
8. Russ Herndin, USAF ABLQ
9. Anthony Bartuska, RCA
10. Stephen M. Ravner, RCA
11. Oliver Bessette, RCA
12. Dennis Foti, Honeywell
13. Glen Call, Motorola
14. A. L. "Skip" White, Ampex
15. Bob Harper, Ampex
16. Steve Mednick, IBM
17. Hank Cote, STC
18. John Harper, STC
19. Dave DeYoung, STC
20. Bill Leuschel, STC
21. Ron Stewart, Miltope
22. Stan Domen, Intel
23. Larry Fujitani, Optimen
24. Rainer Zuleeg, MDMC
25. William Geideman, MDAC

26. Mark Fineberg, McAuto

27. Jim Blouin, McAuto

28. Bob Boggett, CDC

29. Jerry Muench, Odetics

30. Bill White, Thorn EMI technologies inc.

31. Loyde Miller, Harris Semiconductor

32. Mick DeDinsky, Harris Semiconductor

33. Bob Evens, Lockheed Electronics Co.

34. Charlie Adams, Integrated Automation

1.2 MAN/MACHINE INTERFACE

To take the fullest advantage of the capability of the onboard crew, the man/machine interface (MMI) equipment must embody several state-of-the-art technologies integrated into efficient, user friendly workstations, or MPACs (Multipurpose Application Consoles).

The Space Station RFP, and especially the Customer Requirements for Standard Services (CRSS) document impose several requirements on the MMI including presentation of video as well as color graphics and text information, portable workstations, and customer quick look capabilities. In addition, to enhance user friendliness, the use of standards shall be used as much as possible particularly in the areas of graphics and video presentation, and data system interfaces.

1.2.1 OUTPUT

1.2.1.1 Display

1.2.1.1.1 Description

Advanced electronic display media development holds one of the keys to effective integration of the space station crew workstation electronic systems. This is true whether they are employed in a large-area multimode display or in multifunction keyboards or touch-panels. Using display technology, the space station crew workstation can be decluttered by replacing single function instruments and switches with multimode, multifunction devices. Sperry will undertake a detailed assessment of advanced display media including the CRT and flat panel technologies for space station applications.

Before proceeding, the characteristics important to display media must be identified in order to make comparative judgements of the advantages, disadvantages and limitations of the various media. The characteristics deemed of importance are listed below.

Cost
Power Consumption
Size
Luminous Efficiency
Contrast Ratio
Resolution
Color Capability
Grey Scale
MTBF
Ruggedization Requirements
Highest Voltage
Temperature Range
Uniformity

The options to be considered for space station displays are as follows:

Plasma Display Panels
Cathode Ray Tube (CRT)
Light Emitting Diode Flat Panel
Liquid Crystal Flat Panel
Electroluminescent Flat Panel

CRT Technology

Before getting into the discussions of flat panel display media, let us look at the overall advantages and disadvantages of the two major display media types, i.e., CRT and flat panel.

The CRT has several inherent disadvantages which has led technology to the development of the flat panel. These are:

- Depth/Bulk
- Limited Life
- High Voltage
- Not directly Digital Compatible
- Possibility of Catastrophic Failure

The constraints of the CRT's electron optics determine the above disadvantages. High resolution with good edge focus necessitate relatively narrow deflection angles resulting in considerable depth and weight. This is a primary motivation for the development of alternate electronic displays such as the flat panel. Valuable space and weight savings can be obtained in the space station and other avionics applications when an appropriate flat panel display is developed. When the CRT is used at high beam current the phosphorus covering has a limited lifetime, in addition, a high voltage is required for the beam acceleration. Another disadvantage is that the CRT is not directly digitally compatible, although, this disadvantage can be considered minimal since the modern scanning techniques make the CRT readily addressable. In the past, the fear of catastrophic failure was of concern. This was primarily due to the poor design and now ruggedized CRTs have now reached the respectable MTBF of 3,000 to 5,000 hours. Further refinements will enhance this reliability, although not to the point of future solid-state flat panel displays.

Plasma Display Panels

Plasma display panels (PDPs) are by far the most popular of the commercial flat panel displays, accounting for nearly as large a market share as the other technologies combined. They are a well established technology and the basic characteristics and limitations are unlikely to change significantly in the foreseeable future. All PDPs utilize a noble gas (usually neon) that ionizes at a specific threshold voltage (V_{th}) and remains ionized at a lower sustaining voltage (V_{sus}). The usual plasma device consists of an array of individual cells arranged in a matrix form at the intersection of anode and cathode conductors which form electrodes on the surface of the glass plates used to contain the gas. One of the electrodes is made transparent for viewing the discharge. The discharge process is not very efficient, typically providing about 0.5 Lm/w.

PDPs may use one of four basic technologies: DC, AC, AC-DC hybrid, or Gas-Electron-Phosphor (GEP). Most produce an image directly by means of the glow of the noble gas (most DC, all AC, and all AC-DC hybrid). Gas-Electron-Phosphor (GEP displays, however, extract electrons from the

ionized gas and use them to excite CRT-type phosphors on the display screen. In similar fashion, some photoluminescent DC PDPs use invisible ultraviolet radiation from the ionized gas to excite phosphors.

Conventional DC plasma displays consist of electrodes sealed in a neon-filled glass envelope. At any area on the display where voltage exceeds V_{th}, a reddish-orange glow appears. A voltage of V_{sus} across the entire display maintains the glow, without providing sufficient voltage to excite any further glow at any other areas of the display. This gives plasma displays an inherent memory capability.

Two difficulties with DC plasma displays are the large number of drive circuits required (especially for an unformatted matrix) and contamination problems between the electrodes and the noble gas mixture. Another limitation of DC PDPs is that brightness is inversely proportional to area. Therefore, they cannot be much larger than a page in size and still retain sufficient brightness. Displays larger than this can be built only by connecting together a number of smaller displays.

AC plasma dominates the larger display field. This technology results from work at the University of Illinois to solve the contamination problems of DC plasma displays. The solution was to place the electrodes outside the glass envelope, out of contact with the gas mixture. Later refinements placed the electrodes back on the inside glass surfaces again, but this time protected from the gas mixture by a thin film, dielectric insulator. In addition to insulating the electrodes, the dielectric insulator creates a circuit element that provides a capacitive storage. As a result, once a picture element is turned on, it stays lit until it is turned off by an appropriate pulse sequence. This memory eliminates the need for display refresh. The overall quantity of electronics is the same as for DC plasma, since a driver is required for every row and column. But unlike DC plasma displays, brightness is independent of display area. Therefore, maximum size of AC plasma displays is limited only by manufacturing constraints and physical factors, such as the ability to manufacture large, fine electrode grids on glass, and the overall weight of the final product.

The third plasma technology, AC-DC hybrid, combines characteristics of AC and DC panels. These displays use a DC-based system that "primes" the gas, making it easier to turn on and address pixels. At the same time, a set of AC electrodes controls the display to achieve pixel memory. The gas-electron-phosphor technique uses a series of U-shaped cathodes running the height of the display that produce a cold-cathode glow discharge. There is an anode grid in front of the cathodes, criss-crossed by a matrix of row and column electrodes. When both a row and a column electrode are excited, an anode glow forms at their intersection. A video grid extracts electron beams from this glow and modulates their intensity. They are then accelerated through high-voltage spacers, striking and exciting CRT type phosphor dots on a face plate.

GEP technology re-introduces some of the problems of DC PDPs. Since it requires scanning, brightness is once again inversely proportional to the number of elements being scanned. Also, flicker once again becomes a consideration. However, these problems can be addressed just as they are addressed in a CRT; high quality phosphors can increase brightness, and long persistence phosphors can be used to reduce flicker. Also, GEP technology can accommodate color through the use of color CRT type phosphors.

Light Emitting Diode (LED) Displays

Light emitting diode technology is based on an electroluminescent phenomenon referred to as "carrier injection electroluminescence." In the presence of an electric field of proper polarity, loosely bound electrons on the n-doped side of an pn junction are injected across the diode junction region. Upon entering the p-doped region as minority carriers, they combine either by direct or indirect band gap transitions with majority carrier holes, thereby producing light.

This recombination can be either radiative or nonradiative. The primary objective in LED technology is to maximize the light output by increasing the probability of radiative recombination and decreasing the probability of nonradiative recombination. Primary success has been achieved in forming efficient light-emitting junctions in single crystalline solid-state compounds from group III and group V elements in the periodic table, these include: GaP

(green, yellow, orange and red emission), GaAsP (orange and red emission), and GaInP (yellow emission). Other less efficient compounds remain in a less developed state due to a combined lack of commercial interest and government support. GaN falls in this category, but is noteworthy because it has the potential for producing a full-color display. Military development efforts have resulted in LEDs having improved reliability, long life, and ruggedness.

A difficult technical problem has been developing techniques that improve LED efficiency, although substantial progress has been made in this area. Todays commercial LED devices typically require considerable more injected electrons for each photon that is emitted. Measured efficiency figures vary for the gallium-arsenide-phosphide range of LEDs, which are commonly used and commercially available type, and emit in the spectral range from red to green. As a ratio of GaP to GaAsP increases, the quantum efficiency rapidly falls off. But because of the increasing efficiency of the eye over this spectral range, the luminous efficiency remains very nearly constant. Thus a range of materials is available covering the spectral band from red to green, and all having an efficiency approaching 1 Lm/w.

Simple numeric 7-bar LED displays developed specifically for aircraft use are now commercially available and have been extensively tested under high brightness conditions. Red, yellow or green emitting bar chips have been used to form 4 mm-high numerals. Chips are mounted on a multilayer thick-film circuit which has a black dielectric layer on its top surface to increase contrast. The wire bonds to the LED chips are kept short to minimize reflections. It has been found necessary to use filters in front of the display to increase contrast. With this filter/display combination, excellent legibility has been reported in illumination levels up to 10 lux, with power consumption of less than 0.2w per character.

Attempts have been made to provide area arrays for aircraft use, but this presents altogether more formidable problems. Apart from the very serious problem presented by the low luminous efficiency of LEDs, the difficulty of fabricating an array of up to 10 elements at an economic cost generally implies monolithic structure. Unfortunately, monolithic arrays tend to be of lower efficiency than discrete chips. Limits to the size of matrix arrays are

set both by the problem of high-yield production of large arrays and also by the difficulty of providing the high-current, short-duration pulses necessary to drive matrices of more than about 64 x 64 elements. Thus it has been necessary to build up larger LED arrays in the form of a pattern of modules.

The primary development thrust on LEDs for use in military aircraft displays has been in green (5650A) GaP monolithic chip arrays suitable for forming the mosaic surfaces of two and four edge abuttable dot-matrix display modules. One quarter inch square, 64 pixels/inch monolithic chips that utilize a planar flip-chip solder reflow interconnection structure have been successfully demonstrated. The planar flip-chip structure, in addition to being well-suited to automated chip placement on and bonding to the underlying electrical interface ceramic, provides the display observer with a direct view of the light emitting diode junctions (i.e., through the transparent LED chip) that is not obscured by electrical leads or connections. The resulting structure has been demonstrated to provide luminance outputs suitable for sunlight legible graphic portrayal. The structure is also well-suited to the application of anti-reflective refractive index matching surface layers which initial testing indicates should permit a significant reduction in display surface/driver operating power when the technique is fully developed. Tests conducted on 1980 GaP monolithic LEDs resulted in average pixel luminance outputs of greater than 1,100 fl using the 0.5mA average LED drive current (at 2.75 volts) and 500 Hz refresh rate/0.5% pulse cycle drive condition employed in the 3 in x 4 in, 75 fl Multi-Mode Matrix Concept Demonstrator Display delivered in 1978. The power required to drive a 64 pixel/inch optically filtered 1 inch by 1 inch graphics LED module, having a typical 20 percent load pattern operating at a contrast ratio of 50 in a 10,000 fc viewing environment, is approximately one watt including drivers. The luminance improvement has resulted almost totally from improvement in materials and device processing techniques rather than from the optical enhancement processing techniques which are still in the last stages of development. Further development effort is still required to produce the same legibility at the maximum demonstrated resolution of 126 pixels/inch needed to match or exceed the resolution of current CRT displays used in aircraft for the portrayal of video information.

The construction of large display surfaces using standard 1 inch x 1 inch LED display modules offers a number of advantages over CRTs including (1) the ability to build displays satisfying a variety of different size and shape requirements using components with known display capabilities, (2) the fact that even though the number of individual displays needed for each military application is small, the number of modules needed is large enough to justify a high degree of production automation and (3) the interchangeability of modules results in a reduced logistics inventory requirement. The basic problem associated with modular display construction is the very tight mechanical tolerances that must be achieved to provide the intermodule alignments and spacings needed to give the appearance of a continuous display surface having equal pixel spacing throughout. Experience gained in the construction of two and four-edge abutted modular displays having 64 pixels/inch resolutions, has shown that the tolerances which must be met to produce modular LED displays at up to 125 pixels/inch resolution are feasible.

One very promising area for the application of the bright green monolithic LED modules (64 lines/inch) is in the form of full-surface display for programmable, multilegend switches. NASA-Langley and the Air Force have supported research in this application area which has led to the development highly reliable and unique graphic/alphanumeric switch technology. This new technology offers excellent potential for consolidation of workstation controls and presentation of backup display information.

Several development and evaluations have been performed on discrete tricolor LED arrays. These displays are fabricated by alternating red and green LEDs to form an X-Y array. They have been fabricated in several sizes, including 1 x 3 inch modules, and have edge abutted several modules to form a 3 x 4 inch tri-color display at 24 dots per inch. Three discrete colors are obtained as follows:

- Red - Red LED Lit only
- Green - Green LED Lit only
- Yellow - Red and Green Lit

24 dot per inch tri-color LED experiment displays have had excellent results. The basic problems of this approach in the workstation are high power consumption and high costs.

The Air Force, Canadian Government, and NASA-Langley have embarked on a program to develop tricolor LED technology in monolithic form (hopefully a less expensive approach) as a part of the Crew Station Technology program at Langley. The goals of the program are to achieve true monolithic tricolor LED modules with the increased resolution of 64 lines/inch, better uniformity in brightness and color, and lower production costs. It is envisioned that two major application areas may result: (1) direct use of tricolor LED modules in programmable multilegend, multifunction switches and keyboards and (2) medium-sized tricolor videographic displays through use of edge abutting of modules. Phase 1 of the program is nearing completion, the development of the tricolor monolithic modules, and Phase 2 will begin shortly, the development of a tricolor multilegend switch.

Liquid Crystal Displays (LCD)

According to Dr. Joseph Costelano, President of Stanford Resources, a research firm specializing in flat panel displays, by 1986 liquid crystal displays will replace plasma displays as the most popular flat panel graphics display. This will be due to the huge investments of a large number of Japanese companies and LCDs will account for over a third of the display sales in 1990. Most of these sales will be in the low end, low information market.

Commercial developments have concentrated on numeric displays, with liquid crystal displays replacing light emitting diode displays in the current watch and calculator markets because of their low power consumption and lower cost. Many varieties of LCDs are being developed in Japan, the U.S. and Europe, and display conferences have been replete with demonstrations of the new technologies. Recent applications of liquid crystal displays range from a 0.8 by 1.0 inch color television with a LC display of 240 by 320 picture elements, to a message board incorporating 1024, 2 inch by 2 inch liquid crystal pixels, suitable for store signs and message centers.

The Department of Defense efforts have concentrated on the development of video displays to present imagery such as graphics and alphanumerics. Optical projection and fiber optics expander techniques are currently being developed in order to increase resolution and enlarge display areas.

All liquid crystal display devices make use of the ability of liquid crystals to reflect or refract ambient light differently when acted upon by voltage and/or heat. The liquid display devices are therefore non-emissive and use electro-optic materials to modulate light by means of scattering, fire fringence, solarization, absorption, or combinations of these optical effects. Three main types of liquid crystal displays are most commonly used: Twisted-nematic field effect, active matrix, and smectic liquid crystal displays. Work on a dye-based phase-change phenomena shows promise for future displays.

Liquid crystals are basically organic liquids with very long molecules, so that over a fair range of temperatures the intermolecular forces cause the molecules to be aligned in an ordered structure. This structure gives rise to different physical characteristics including dielectric constant, refractive index, and magnetic susceptibility. With the application of an electrostatic field molecular alignment can be modified, which in turn alters the optical properties and appearance of the liquid crystal display.

Two modes of operation are available in the twisted-nematic field effect liquid crystal display: The field effect mode which uses light polarizers to provide contrast between the reflected and absorbed light and the dynamic scattering mode which uses light traps to provide contrast between the scattered light and specularly reflected light.

The twisted-nematic field effect liquid crystal display consists of two glass plates with rows and columns of transparent conductor lines. Sandwiched between the two plates is the liquid crystal mixture. The front glass plate has a transparent polarizing filter. The back glass plate has a reflecting polarizer, oriented at 90° to the polarizer on the front plate. When no current is applied to the conductors, the liquid molecules take up the orientation which is determined by the intermolecular forces within the liquid and also by any directional structure on the surface of the electrodes. This

orientation is a spiral shaped structure joining the two glass surfaces, giving the light a 90° twist. On applying an electrical current, the crystals line up and let light pass through uneffected. Cells with no current applied reflect ambient light, and appear light colored. The light passing through the face plate is polarized in one direction, then gets twisted 90° by the liquid crystal, allowing it to pass through the back-plate polarizer, which reflects it forward again. As it passes through the liquid crystal again, the light gets a second 90° twist, reorientating it to its original position and thus allowing it to pass out through the polarized face plate. Conversely, cells with current applied absorb ambient light, and appear dark. In this case, light is polarized in one direction by the front face plate, and passes through the aligned liquid crystal unaffected. When the light reaches the back plate, whose reflective polarizer is orientated 90° opposite that of the front plate, it is blocked. Therefore, light is not reflected back again, and the cells appear significantly darker than the surrounding cells.

A reflective display can be made using the dynamic scattering mode technique. This type of display eliminates the use of polarizers but uses light traps to provide contrast between scattered light and specularly reflected light. The dynamic scattering mode liquid crystal display must have external illumination for nighttime viewing.

In order to implement graphics, a multiplexing scheme allows addressing of a matrix of elements. One difficulty is the slow response time of the liquid crystal as they reorientate themselves. Extensive multiplexing compounds this problem and limits the area of the total conventional twisted-nematic field effect liquid crystal display.

Active matrix LCDs offer one solution to the above problem. This type of LCD uses an array of thin-film transistors as internal switches to turn each elements on and off. Higher information displays can be obtained due to the much faster switching times. However, difficulties in making defect free transistor arrays have limited this technology.

Thermally-addressed smectic LCDs use a liquid crystal material that requires both voltage and heat for activation. Therefore, instead of a conventional matrix of conductors, smectic displays use one plane for delivering voltage to

each cell, and the second plane for delivering heat. The key advantage of the technology is that once activated, the cells maintain their condition without refreshing. This simplifies the electronics, and provides for a much larger display. However, display time is slow and drivers required to handle the heating requirements are expensive.

Another liquid crystal mechanism which is important for potential application in the space station workstation is the cholesteric–nematic phase change display. A pleochroic or dichroic dye material is uniformly mixed with the host liquid crystal molecules. The appearance from the front surface of the crystal cell depends on the alignment of the dye molecules, and is colored in the cholesteric phase and transparent in the nematic phase. The phase change is brought about by an application of a voltage field which causes a complete change in the arrangement of the liquid crystal molecules. This is a much faster effect than in the twisted–nematic cell — Although. with the penalty of a voltage which is usually at least switch that of the twisted–nematic displays. A further advantage of this display is the improved angle of view compared with the twisted–nematic type.

Electroluminescent (EL) Displays

Several different techniques have been developed to utilize the phenomenon of field–excited luminance. In the past several years considerable progress has been made in overcoming some of the basic problems of this technology. Electroluminescent (EL) displays can be divided into AC and DC types corresponding to whether they are driven by AC or DC voltage. In each type, the devices may be fabricated with powder EL or thin–film EL materials.

The simple concept of exciting luminescence in phosphor powders by the application of an electric field was first put to practical use in AC–driven panels in which a ZnS phosphor powder was held in a plastic binder. This method has found widespread use in simple types of on/off displays, and also in aircraft for the lighting of cockpit instruments. Early examples of this type of panel has a poor reputation for life and luminance, but it later became possible to achieve lives of over 10,000 hours at luminances of 30 candelas per square meter (cd/m^2) or more.

Much research has been directed towards alphanumeric and matrix displays based on EL technology, but with the AC-excited powder-binder type of EL, the presence of half voltages on unaddressed elements causes a significant loss of contrast. Although, this has been largely overcome by coating the rear surface of the EL layer with an auxiliary material having a highly nonlinear current/voltage characteristic. The high voltages and low overall efficiency of this technique effectively rule it out of contention for aircraft use. An alternative of using an individual store or latch with each element has also been explored. Using the thin-film transistor technique luminances of 100 cd/m^2 have been obtained on 120 x 100 element panels.

in the early seventies, a development effort led by Sigmatron succeeded in fabricating AC thin-film EL devices with reasonable life brightness. Recently, researchers at Sharp Corp. have made a significant breakthrough in achieving medium high brightness and long life AC thin-film EL panels. The reliability of the devices not only depends on the quality of the polycrystalline manganese-doped ZnS layer, but also on the breakdown strength of the insulating layers sandwiching the ZnS layer. This EL mechanism is believed to be due to the electron impact excitation of the manganese ion. Since the light output of device is directly proportional to the charge flowing through the capacitative layers per pulse, the number of pulses per second and the voltage across the ZnS film, one expects to have higher efficiency if high dielectric constant and breakdown strength insulator films are used. The sharp voltage threshold, fast turn-on and turn-off response times, and high peak brightness make this device one of the attractive candidates for a refreshed matrix display.

In the thin film EL devices, a black layer acts as a light absorber, and since the layers in front of it can be made to be transparent, less than 0.5 to 1 percent of the light is reflected back. In a 10,000 foot-candle ambient light environment panels can achieve a contrast ratio in the range of 1.6 through 9.1 to 1 with 15 to 200 foot lamberts of panel brightness. This is an enormous advantage as compared with powdered phosphor, and means that, by comparison with earlier EL displays or with monochrome cathode ray tubes, adequate contrast can be obtained with much less panel brightness or luminance.

Unfortunately, in the case of thin-film EL display panels, the achievement of fairly good contrast ratios in a high ambient light environment may not be good enough for the cockpit.

Recently, a specially developed 6 inch TFEL panel (Tri-Service/NASA effort) was driven by an experimental raster (video) generator which produced an integrated EADI (electronic attitude director indicator) and EHSI (electronic horizontal situation indicator) flight display at 240 x 320 pixels at 60 Hz, Noninterlaced (Repeated Field). The displays produced were flicker free and showed good grey scale capability. The update rate of the symbology was approximately 20 Hz, which resulted in very smooth display animation. These initial tests will be followed by full laboratory evaluations and part-task simulator evaluations.

1.2.1.1.2 Option Characteristics

a) Performance Characteristics

CHARACTERISTIC	CRT	PLASMA	LED	LCD	EL
Cost	Good	Good	Poor	Good	Good
Power Consumption	Fair	Good	Poor	Excellent	Good
Volume	Poor	Good	Good	Excellent	Good
Luminous Efficiency	Excellent	Good	Good	Excellent	Good
Contrast Ratio	Excellent	Good	Good	Excellent	Good
Resolution	Excellent	Good	Good	Excellent	Good
Color Capability	Excellent	Good	Poor	Good	Good
Grey Scale	Excellent	Fair	Good	Excellent	Excellent
MTBF	Fair	Good	Good	Excellent	Good
Ruggedization	Fair	Good	Excellent	Good	Excellent
Uniformity	Excellent	Fair	Good	Excellent	Excellent
Highest Voltage	Poor	Fair	Excellent	Excellent	Fair
Temperature Range	Good	Good	Excellent	Good	Excellent

1.2.1.1.2 Option Characteristics

b) Programmatic Characteristics

CHARACTERISTIC	CRT	PLASMA	LED	LCD	EL
Cost	Good	Good	Poor	Good	Good
Schedule	Excellent	Fair (Color)	Poor (Color)	Fair (Color)	Fair (Color)
Availability	Excellent	Fair (Color)	Poor (Color)	Fair (Color)	Fair (Color)

1.2.1.1.2 Option Characteristics (Continued)

c) Risk Assessment

Option #1 - CRT

This is a level 6 technology readiness level; Prototype/ engineering model tested in relevant environment.

Option #2 - Plasma Display Panels

This is a level 4 technology readiness level; Critical function/characteristic demonstration.

Option #3 - Light Emitting Diode Displays

This is a level 4 technology readiness level; Critical function/characteristic demonstration.

Option #4 - Liquid Crystal Displays

This is a level 4 technology readiness level; Critical function/characteristic demonstration.

Option #5 - Electroluminescent Displays

This is a level 4 technology readiness level; Critical function/characteristic demonstration.

1.2.1.1.3 Projected Capabilities

a) CRT

	1987	1995	2000
Cost	Good	Good	Excellent
Power Consumption	Fair	Fair	Fair
Size	Poor	Poor	Poor
Luminous Efficiency	Excellent	Excellent	Excellent
Contrast Ratio	Excellent	Excellent	Excellent
Resolution	Excellent	Excellent	Excellent
Color Capability	Excellent	Excellent	Excellent
Grey Scale	Excellent	Excellent	Excellent
MTBF	Fair	Good	Excellent
Ruggedization	Fair	Good	Excellent
Uniformity	Excellent	Excellent	Excellent
Highest Voltage	Poor	Poor	Poor
Temperature Range	Good	Excellent	Excellent

1.2.1.1.3 Projected Capabilities

b) Plasma

	1987	1995	2000
Cost	Good	Good	Excellent
Power Consumption	Good	Good	Excellent
Size	Good	Excellent	Excellent
Luminous Efficiency	Good	Excellent	Excellent
Contrast Ratio	Good	Excellent	Excellent
Resolution	Good	Good	Excellent
Color Capability	Good	Good	Excellent
Grey Scale	Fair	Good	Excellent
MTBF	Good	Excellent	Excellent
Ruggedization	Good	Excellent	Excellent
Uniformity	Fair	Good	Excellent
Highest Voltage	Fair	Good	Good
Temperature Range	Good	Good	Excellent

1.2.1.1.3 Projected Capabilities

c) Light Emitting Diode Displays

	1987	1995	2000
Cost	Poor	Good	Good
Power Consumption	Poor	Poor	Good
Size	Good	Good	Excellent
Luminous Efficiency	Good	Good	Excellent
Contrast Ratio	Good	Excellent	Excellent
Resolution	Good	Good	Excellent
Color Capability	Poor	Poor	Good
Grey Scale	Good	Good	Excellent
MTBF	Good	Excellent	Excellent
Ruggedization	Excellent	Excellent	Excellent
Uniformity	Good	Good	Excellent
Highest Voltage	Excellent	Excellent	Excellent
Temperature Range	Excellent	Excellent	Excellent

1.2.1.1.3 Projected Capabilities

d) Liquid Crystal Displays

	1987	1995	2000
Cost	Good	Good	Excellent
Power Consumption	Excellent	Excellent	Excellent
Size	Excellent	Excellent	Excellent
Luminous Efficiency	Excellent	Excellent	Excellent
Contrast Ratio	Excellent	Excellent	Excellent
Resolution	Excellent	Excellent	Excellent
Color Capability	Good	Good	Excellent
Grey Scale	Excellent	Excellent	Excellent
MTBF	Excellent	Excellent	Excellent
Ruggedization	Good	Excellent	Excellent
Uniformity	Excellent	Excellent	Excellent
Highest Voltage	Poor	Good	Good
Temperature Range	Good	Good	Excellent

1.2.1.1.3 Projected Capabilities

e) Electroluminescent Displays

	1987	1995	2000
Cost	Good	Excellent	Excellent
Power Consumption	Good	Excellent	Excellent
Size	Good	Excellent	Excellent
Luminous Efficiency	Good	Good	Excellent
Contrast Ratio	Good	Excellent	Excellent
Resolution	Good	Good	Excellent
Color Capability	Good	Good	Excellent
Grey Scale	Excellent	Excellent	Excellent
MTBF	Good	Excellent	Excellent
Ruggedization	Excellent	Excellent	Excellent
Uniformity	Excellent	Excellent	Excellent
Highest Voltage	Fair	Good	Good
Temperature Range	Excellent	Excellent	Excellent

1.2.1.1.3 Projected Capabilities (Continued)

f) Key Drivers

CRT

CRT technology is mature but the main drivers for the space station will be a space qualified CRT. Work must be done on ruggedization and meeting the environmental constraints imposed by a space environment.

Plasma Display

Plasma technology is progressing satisfactorily. Problems such as slow update, contamination etc. are being resolved. The key driver to the use of a plasma display on the space station will be the development of a full color display.

Light Emitting Diode Display

Recent light emitting diode technology has improved the reliability, longevity and ruggedness of the LED display. The key to LED usefulness will be an improvement in efficiency, and the development of full color.

Liquid Crystal Display

The key drivers to a liquid crystal display will be the development of large full color display.

Electroluminescent Displays

The key drivers for a useful electroluminescent display is to increase the brightness and develop a large full color screen.

1.2.1.1.4 References

1) W. C. Scott, W. G. Horton, W. G. Manns, D. F. Weirauch, M. R. Namordi, F. Doerbeck and J. Gunther, "Flat Cathode-Ray-Tube Display," Texas Instruments, Dallas, TX.

2) M. Craford, "Recent Developments in Light-Emitting-Diode Technology," IEEE Transactions on Electron Devices, Vol. ED-24 No. 7, July 1977.

3) R. H. Bhargave, "Recent Advances in Visible LED's," IEEE Transactions on Electron Devices, Vol. ED-22, No. 9, September 1975.

4) "Recent Advances in Liquid Crystal Materials and Display Devices," IEEE Transactions on Electron Devices, Vol. ED-26, No. 8, August 1979.

5) A. Sobel, "Gas-Discharge Displays: The State-of-the-Art," IEEE Transactions on Electron Devices, Vol. ED-24, No. 7, July 1977.

6) M. DeJule, A. Sobel and J. MarKin, "A Gas-Electron-Phospher Flat Panel Display," Lucitron Inc., Northbrook, Ill.

7) G. Kramer, "Thin-Film-Transistor Switching Matrix for Flat-Panel Displays," IEEE Transactions on Electron Devices, Vol. ED-22, No. 9, September 1975.

8) "A Thin Film-Transistor-Controlled Liquid - Crystal Numeric Display," IEEE Transactions on Electron Devices, Vol. ED-26, No. 5, May 1979.

9) D. Syroid, Staff Engineer, Sperry Flight Systems.

1.2.1.2 Speech Synthesis

1.2.1.2.1 Description

Digital voice recording is the simplest way of producing speech electronically. Spoken words are converted to digital codes using an analog to digital converter and stored in a storage medium. The codes can then be retrieved in the proper order and converted to speech through the use of a digital to analog converter.

The most common means of encoding speech to digital signals is through pulse code modulation (PCM). Each amplitude of the speech signal is represented by a different digital code. A minimum length of 12 bits must be used in order to accommodate the range of amplitudes found in human speech. To preserve speech quality the speech must be sampled every 0.0001 of a second. It is interesting to note that this sampling rate of 10,000 time a second with a 12 bit digital code will require 120,000 bits of storage location every second. It becomes immediately obvious that tremendous storage requirements are needed.

In order to reduce the storage requirements for PCM, a method called coded variable-slope delta modulation (CVSD) can be used. This method uses a digital code to represent changes in amplitude for adjacent samples. Thus, the number of bits required in each code depends on the difference in amplitude between samples. As the number of samples increase, the encoding bit requirements decrease. Sample rates in CVSD systems generally exceed 16,000 bits/sec.

A recent development in limited vocabulary speech synthesis is time-domain encoding. The data stored represents speech waveforms that have been compressed as a function of time. A synthesizer then decompresses this data to form speech output. Only that data which the human ear uses to understand speech is stored, i.e., the frequencies produced and their power spectrum closely resemble the original waveform. Component frequencies are chosen so that the time-domain waveform can be represented by a small number of bits. Bit rates as low as 500 per second have been reported for some vocabularies.

Another concept, parametric encoding, generates speech by controlling an electronic synthesizer which produces complete words and phrases. The circuits actually simulate the functions of human anatomical features that produce speech. The most popular method of parametric encoding is a technique called linear prediction. Linear predictive coding (LPC) has been perfected to a point where it has become the best understood and most widely used method of speech systhesis.

Instead of storing words, the LPC systems separate words into sounds which constitute speech. Forty speech sounds called phonemes can be produced using sixteen vowels and twenty-four consonants. By using these forty phonemes, an LPC system can construct any word or phrase, although the synthesized speech is of poor quality. To improve speech quality, phonemes which are adapted to the speech environment in which they will be used (called allophomes) are used. These allophomes can be viewed as phonemes that have been conditioned to more accurately reproduce speech. Most systems use on the order of 128 allophomes and are linked together by a speech algorithm which provides parameter smoothing and adjustments in pitch and amplitude. The options to be considered here are Digital Voice recording and limited vocabulary output systems. Also to be considered are control action confirmation and data entry confirmation technology which can incorporate either of the above voice synthesis technologies.

In order to make comparative judgements of the advantages, disadvantages and limitations of the voice synthesis technology options, the following characteristics have been deemed important.

Cost
Power
Storage Requirements
Computational Loading
Total Word Capability
Response Time
Speech Quality

1.2.1.2.2. Option Characteristics

a) Performance Characteristics

CHARACTERISTIC	DIGITAL VOICE RECORDING	LIMITED VOCABULARY OUTPUT SYSTEMS	CONTROL ACTION CONFIRMATION	DATA ENTRY CONFIRMATION
1. Cost	Low Cost	Medium Cost	Medium Cost - Integration and system development will drive cost	Low Cost
2. Power	Medium	Medium	Medium Power	Medium Power
3. Storage Requirements	High	Medium	Storage requirements high due to complex software	Low storage requirements
4. Computational Loading	Low Computational Loading	Low Computational Loading	Medium Computational Loading	Low Computational Loading
5. Total Word Capability	Large capability incurs penalties in access time, response time and storage requirements	Large	Large	Limited to those words needed for data entry
6. Response Time	Response time will vary with word capability	Slow response time	Response time will vary with software complexity	Reat time response
7. Speech Quality	Excellent	Good	Digital voice recording or limited vocabulary system can be used	Digital voice recording or limited vocabulary system can be used

C-2

1.2.1.2.2. Option Characteristics

b) Programmatic Characteristics

CHARACTERISTIC	DIGITAL VOICE RECORDING	LIMITED VOCABULARY OUTPUT SYSTEMS	CONTROL ACTION CONFIRMATION	DATA ENTRY CONFIRMATION
1. Schedule	Technology is mature and no schedule impact is anticipated.	Technology is not mature but is available. No schedule impact anticipated if current systems are used.	Schedule impact will be in the area of system requirements, and software development.	Technology is mature and no schedule impact anticipated.
2. Cost	Low Cost	Medium Cost	Medium Cost	Low Cost
3. Availability	Technology available	Technology available	Technology available but only elementary systems in use.	Systems currently in use.

1.2.1.2.2 Option Characteristics (Continued)

c) RISK ASSESSMENT

Option #1 – Digital Voice Recording

This is a level 4 technology readiness level; critical function/characteristic demonstrated.

Option #2 – Limited Vocabulary Output System

This is a level 3 technology readiness level; conceptual design tested analytically or experimentally.

Option #3 – Control Action Confirmation

This is a level 3 technology readiness level; conceptual design tested analytically or experimentally.

Option #4 – Data Entry Confirmation

This is a level 6 technology level; prototype/engineering model tested in relevant environment.

1.2.1.2.3 Projected Capabilities

a) Digital Voice Recording

	1987	1995	2000
1. Cost	1. Excellent	1. Excellent	1. Excellent
2. Power	2. Good	2. Good	2. Excellent
3. Storage Requirements	3. Poor	3. Poor	3. Good[1]
4. Computational Loading	4. Excellent	4. Excellent	4. Excellent
5. Total Word Capability	5. Excellent[2]	5. Excellent[2]	5. Excellent[2]
6. Response Time	6. Good	6. Good	6. Excellent[3]
7. Speech Quality	7. Excellent	7. Excellent	7. Excellent

NOTE: 1. Assumes new methods in compacting digital data.

2. Capability is high if penalties in access time, response time and storage requirements are acceptable

3. Assumes faster peripheral storage devices.

1.2.1.2.3 Projected Capabilities

b) Limited Vocabulary Output Systems

	1987	1995	2000
1. Cost	Good	Excellent	Excellent
2. Power	Good	Good	Excellent
3. Storage Requirements	Good	Good	Good
4. Computation Loading	Good	Good	Excellent
5. Total Word Capability	Excellent	Excellent	Excellent
6. Response Time	Good	Good	Excellent
7. Speech Quality	Good	Good	Excellent

1.2.1.2.3 Projected Capabilities

c) Control Action Confirmation

	1987	1995	2000
1. Cost	Good	Excellent	Excellent
2. Power	Good	Good	Excellent
3. Storage Requirements	Poor	Good	Good
4. Computation Loading	Poor	Good	Good
5. Total Word Capability	Excellent	Excellent	Excellent
6. Response Time	Good	Good	Excellent
7. Speech Quality	Good	Good	Excellent

1.2.1.2.3 Projected Capabilities

d) Data Entry Confirmation

	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Good	Good	Excellent
3. Storage Requirements	Excellent	Excellent	Excellent
4. Computation Loading	Excellent	Excellent	Excellent
5. Total Word Capability	Excellent	Excellent	Excellent
6. Response Time	Excellent	Excellent	Excellent
7. Speech Quality	Excellent	Excellent	Excellent

1.2.1.2.3 Projected Capabilities (Continued)

e) Key Drivers

Digital Voice Recording

The key driver to improving the digital voice recording systems will be to reduce the large storage requirements and sampling rates. New and improved methods must be developed to encode digital speech information.

Limited Vocabulary Output System

The key driver for limited vocabulary output systems will be the reduction of the data rate. The lower bit rate will mean longer on-off signals resulting in superior bit reliability, lower power and reduced storage requirements.

Control Action Confirmation

The key to control action confirmation will be the system integration and complex software associated with coordinating voice synthesis with complex control action confirmations.

Data Entry Confirmation

Data entry confirmation is being used in may commercial applications. The technology is well developed and key drivers will be in the improvement of the voice synthesis techniques above.

1.2.1.2.4 References

1) "Desktop System Develops Voice," Electronics, pp. 228–229, February 10, 1983.

2) E. Teja, "Speech–development System Speeds Design Turnaround," EDN, pp. 100, March 31, 1983.

3) "Voice Board Controls Itself," Electronics, pp. 236–237, February 10, 1983.

4) "Linear Predictive Coding System Synthesizes Speech in Real Time," Computer Design, March 1983.

5) R. E. Crochiere, R. V. Cox, J. D. Johnston, "Real Time Speech Coding," IEEE Transactions on Communications, pp. 621–633, April 1982.

6) Michael Hutchins and Lee Dusek, "How Vocabulary is Generated Determines Speech Quality," Computer Design, pp. 89–93, February 1984.

1.2.2 INPUT CONTROLS

1.2.2.1 Manual

1.2.2.1.1 Description

Traditionally, cockpit input control devices have consisted of switches, push buttons and control columns interacting with software controlled systems. With the improvement in display technology the electronic display is considerably more versatile and offers the opportunity to greatly improve the transfer of information between the crew and space station systems and subsystems. In order to realize the maximum benefit from present display technologies, the workstation must be a place of highly efficient man/machine interrelationships and possess input control capabilities to promote crew effectiveness in all situations.

The following is the list of the current manual input control device options to be considered for use on the space station.

Keyboard
Touch Panel
Joystick
Light Pen
Graphics Tablet
Mouse
Trackball
Multifunction Switches

Keyboard

The keyboard is the oldest and most common method for display input. Commands are typed on an alpha-numeric keyboard and interpreted by a processor which controls display processing to the screen. Keyboards tend to consume space since the keys must be large and sufficiently spaced for ease of pressing without errors.

Touch Panel

There are two main types of touch panels in use today, optical type panels and resistance or capacitance panels. Rows of light emitters and receptors along the screen perimeter are used in the optical system. The touched location is determined by which beams are broken. The spacing of the optical components determines resolution, which is usually low and on the order of a 0.1 inch. The other type panels possess a resistive or capacitive characteristic when the finger touches the screen or may sense an acoustic echo from the touched position. These systems tend to have a higher resolution on the order of 0.01 inch. Problem areas in touch panel systems include this limited resolution, smearing of finger prints on the face plate and operator fatigue.

Joystick

The joystick consists of a spring-loaded rod which when tilted controls the direction and speed of a cursor as a function of the direction and angle of the rod. Rapid displacement with relatively high resolution are its main advantages.

Light Pen

The light pen consists of a stylus containing a photocell which produces an electronic signal when it is placed on the screen and detects light. The signal is sent to a processor and screen location determined. Problems associated with the light pen are operator fatigue and the extra software and hardware required to identify pen position.

Graphic Tablet

The most widely used of the graphic input tools is the graphic tablet. The position of a movable cursor unit is sensed as it moves over a flat surface. This surface has x and y wires embedded in the surface which emit electrical or acoustic signals as the cursor is moved over the surface. This data is then translated into digital coordinate data for transmission to a processor. The precision capabilities of the surface may exceed that of the manipulative capabilities of the operator due to the limited hand/eye coordination possessed by human operators.

Mouse

The mouse is a puck-like device which is rolled against a flat surface to provide cursor control. The main advantages of the device is the rapid cursor movement and they can be used on an ordinary desk top. Tracking errors may be induced by slippage or lifting the device. The use of a mouse in a zero g environment may be questionable.

Trackball

Trackballs are balls set in sockets and rolled in the palm of the hand. Cursor movement is in the direction of the roll at a rate proportional to rotationaly speed. Precise cursor positioning is possible because of the small cursor increments with respect to large angular ball displacements.

Multifunction Switches

Multifunction switch concept is based on discrete alphanumeric LED flat packs or liquid crystal display technology. Multifunction panels generally consist of three areas: a mode select area, scratch pad area and programmable-legend key area. Much work development work needs to be done in the data busing and software development areas. Also, much human factors work needs to be done to determine how to blend this new multifunction technology into a more automated workstation environment.

1.2.2.1.2 Option Characteristics

a) Performance Characteristics

CHARACTERISTIC	KEYBOARD	TOUCH PANEL	JOYSTICK	LIGHT PEN	GRAPHICS TABLET	MOUSE	TRACKBALL	MULTI-FUNCTION SWITCHES
1. Cost	Good	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	Fair[1]
2. Power	Good	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent
3. Space/Size/Weight	Good	Excellent	Excellent	Excellent	Good	Excellent	Excellent	Excellent
4. Vibration induced Errors	Good	Fair	Good	Good	Fair	Good	Good	Excellent
5. Reliability	Excellent	Excellent	Excellent	Good	Excellent	Excellent	Excellent	Good
6. User Friendly	Good	Excellent	Excellent	Good	Good	Excellent	Excellent	Excellent

NOTE: - 1. SYSTEM AND SOFTWARE DEVELOPMENT COSTS ARE HIGH WHEREAS ACTUAL HARDWARE COST IS LOW.

1.2.2.1.2 Option Characteristics

b) Programmatic Characteristics

CHARACTERISTIC	KEYBOARD	TOUCH PANEL	JOYSTICK	LIGHT PEN	GRAPHICS TABLET	MOUSE	TRACKBALL	MULTI-FUNCTION SWITCHES
1. Cost	Good	Excellent	Excellent	Excellent	Excellent	Excellent	Excellent	Fair
2. Schedule	No Schedule Impact	No Schedule Impact	No Schedule Impact	No Schedule Impact	No Schedule Impact	No Schedule Impact	No Schedule Impact	Schedule impact will be in the form of system & software development time.
3. Availability	Mature Technology	Mature Technology	Mature Technology	Mature Technology	Mature Technology	Mature Technology	Mature Technology	Technology is improving rapidly. Will be available for space station IOC/

1.2.2.1.2 Option Characteristics (Continued)

c) Risk Assessment

Option #1 - Keyboard

This is a level 7 technology readiness level - Engineering model tested in space.

Option #2 - Touch Panel

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #3 - Joystick

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #4 - Light Pen

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #5 - Graphic Tablet

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #6 - Mouse

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #7 - Trackball

This is a level 6 technology readiness level - Prototype/ Engineering model tested in relevant environment.

Option #8 - Multifunction Switches

This is a level 5 technology readiness level - Component/ Brassboard tested in relevant environment.

1.2.2.1.3 Projected Capabilities

a) Keyboard

CHARACTERISTIC	1987	1995	2000
1. Cost	Good	Excellent	Excellent
2. Power	Good	Good	Good
3. Space/Size/Weight	Good	Good	Good
4. Vibration induced Errors	Good	Good	Good
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Good	Good	Good

1.2.2.1.3 Projected Capabilities (Continued)

b) Touch Panel

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Fair	Fair	Fair
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Excellent	Excellent	Excellent

1.2.2.1.3 Projected Capabilities (Continued)

c) Joystick

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Good	Good	Good
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Excellent	Excellent	Excellent

1.2.2.1.3 Projected Capabilities (Continued)

d) Light Pen

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Good	Good	Good
5. Reliability	Good	Excellent	Excellent
6. User Friendly	Good	Good	Good

1.2.2.1.3 Projected Capabilities (Continued)

e) Graphics Tablet

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Good	Good	Good
4. Vibration induced Errors	Fair	Good	Good
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Good	Good	Good

1.2.2.1.3 Projected Capabilities (Continued)

f) Mouse

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Good	Good	Good
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Excellent	Excellent	Excellent

1.2.2.1.3 Projected Capabilities (Continued)

g) Trackball

CHARACTERISTIC	1987	1995	2000
1. Cost	Excellent	Excellent	Excellent
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Good	Good	Good
5. Reliability	Excellent	Excellent	Excellent
6. User Friendly	Excellent	Excellent	Excellent

1.2.2.1.3 Projected Capabilities (Continued)

h) Multifunction Switches

CHARACTERISTIC	1987	1995	2000
1. Cost	Fair	Good	Good
2. Power	Excellent	Excellent	Excellent
3. Space/Size/Weight	Excellent	Excellent	Excellent
4. Vibration induced Errors	Excellent	Excellent	Excellent
5. Reliability	Good	Good	Excellent
6. User Friendly	Excellent	Excellent	Excellent

1.2.2.1.3 Projected Capabilities (Continued)

i) Key Drivers

Keyboard

Keyboard technology is mature. The key drivers for space station keyboard use will be the reduction in size, weight, volume and meeting environmental space qualifications requirements.

Touch Panel

Touch panel technology is mature. Problems such as limited precision are limited by finger width and cannot be considered a driving force. All things considered, there is no key driver for touch panel technology.

Joystick

Joystick technology is mature with many applications. Meeting environmental space qualification is the only key driver associated with the use of joysticks on the space station and this presents no problem.

Light Pen

Light pen technology is mature with many applications. Meeting environmental space qualifications is the only key driver associated with use of light pens on the space station and this presents no problem.

Graphics Tablet

Graphics tablet technology is mature. Meeting environmental space qualifications is the only key driver associated with the use of graphics tablets on the space station and this presents no problem.

Mouse

Mouse technology is mature with many applications. Meeting environmental space qualifications is the only key driver associated with the use of a mouse on the space station and this presents no problem.

Trackball

Trackball technology is mature with many applications. Meeting environmental space qualifications is the only key driver associated with the use of a trackball on the space station and this presents no problem.

Multifunction Switches

Multifunction switches are well on the way to being a mature technology. The key driver to successful use of multifunction switches on the space station will be the system integration and software development task.

1.2.2.1.4 References

1) Dr. E. B. Davis and Dr. I. B. Peckham, "New Developments in Cockpit Human Interfaces," Royal Aircraft Establishment, Farnborough, Hampshire, England.

2) J. K. Krouse, "Selecting a Graphic-input Device for CAD/CAM," Machine Design, pp. 75-80, 1983.

3) "Positioning and Tracking Controls for the Human Operator," Measurement Systems, Inc., 121 Water Street, Norwalk, Connecticut 06854, USA.

1.2.2.2 SPEECH RECOGNITION

1.2.2.2.1 General Description

Speech recognition by computer controlled electronics is now receiving a great deal of attention from the commercial sector of the marketplace. Several companies in this country and in Japan have products that will recognize speech, however there is no product now available that will achieve the goal of understanding normal human conversation. Speech recognition is evolving with more capability but it is unlikely to expect dramatic leaps of technology in the near future.

Automatic speech recognizers are composed of sound analyzers followed by word classifiers. The sound analyzer usually performs bandpass filtering on the microphone derived signal and generates a time sequence of frequencies and amplitudes in digital form. The key differences between voice recognition systems are the nature of the subsequent analysis and the methods of classification of words.

The most elementary and widely used approach to utterance classification is to form a two-dimensional matrix of the utterance with time along one axis and frequency along the other. The dependant variable is amplitude. Reference matrices, which are generated for each word during talker training, are compared to the matrix of the unknown utterance. The correct utterance is found by computing a least squares difference to the reference matrices.

Frequently the computer will base an action upon a series of vocalized words. When a word or words have been identified the computer may repeat the vocal input by means of a speech synthesis device. A confirmation such as a switch closure may be required if a misinterpreted word can cause serious problems.

Less sophisticated systems require the speaker to pause between each word so the voice recognizer can clearly define the unknown utterance. In order to identify words in continuous speech, the voice recognizer must compare the reference templates to the continuous speech by sliding the template in time continuously in order to try for a match. This is very computation intensive.

Different speakers will pronounce words in quite different ways. Also a person under stress may speak differently. The less sophisticated systems will require a person to train the voice recognizer with a basic set of words. Another speaker will then be unable to use the voice system because his pronunciation will be different. A more advanced approach is to first isolate specific phoneme units in speech. These are elementary building blocks of speech. The successful algorithms for classification of continuous speech are often proprietary or are trade secrets. The analysis of whole phrases or sentences is aided by considering each word in context. Some words in a sequence may individually be temporarily unresolved. Yet comparing several words in sequence, the processor may identify each word correctly.

The sophisticated processing using phoneme units in general will lead to speaker independence and to recognition of continuous speech. Speech recognition systems vary in several respects.

Isolated word vs continuous speech

One speaker trained vs speaker independent

Limited vocabulary vs large vocabulary

Limited processing vs large processing requirements

There are systems available of commercial quality that cover a spectrum of capabilities. In general the high cost systems have more capability although there are good products that are available at relatively low cost for personal computers.

Therefore, we will specifically contrast a low performance system that is characterized by isolated word recognition, single speaker, limited vocabulary and a low processing requirement with a high performance system that can recognize words in continuous speech and is speaker independent with a large vocabulary and intensive processing.

The selection of a voice recognition system for a crew workstation is based upon the tasks to be done. The system design must detail the capabilities of speech recognition against the detailed work task involved and there must be a trade-off against alternate control mechanizations.

Voice control is not suitable for precise motion control; a joystick would be better. A much more capable system than is now available would be required to enter lists of data; a keyboard would be better. Voice may be particularly useful to select an item from a prepared list when the hands are busy with other tasks. For example, an EVA task might be able to utilize a low performance recognizer in conjunction with a helmet-mounted display to change pages of a menu.

1.2.2.2.2 Options Characteristics

a) Performance Characteristics

CHARACTERISTIC	SINGLE SPEAKER SYSTEM	SPEAKER INDEPENDANT SYSTEM
Cost	Excellent	Fair
Power	Excellent	Good
Space/Size/Weight	Excellent	Fair
Accuracy	Fair	Good
Reliability	Excellent	Good
User Friendly	Fair	Excellent

1.2.2.2.2 Options Characteristics

b) Programmatic Characteristics

CHARACTERISTIC	SINGLE SPEAKER SYSTEM	SPEAKER INDEPENDANT SYSTEM
Cost	Excellent	Fair
Schedule	No Schedule impact	Software Development impact
Availability	Readily available	Technology is continuing to improve

1.2.2.2.2 Option Characteristics

c) Risk Assessment

Option #1 - Single Speaker System

This is a level 6 technology readiness level Prototype/Engineering model tested in relevant environment.

Option #2 - Speaker Independent System

This is a level 3 technology readiness level conceptual design tested analytically or experimentally.

1.2.2.2.3 Projected Capabilities

a) Single Speaker System

CHARACTERISTIC	1987	1995	2000
Cost	Excellent	Excellent	Excellent
Power	Excellent	Excellent	Excellent
Space/Size/Weight	Excellent	Excellent	Excellent
Accuracy	Fair	Good	Excellent
Reliability	Excellent	Excellent	Excellent
User Friendly	Fair	Fair	Fair

1.2.2.2.3 Projected Capabilities (Continued)

b) Speaker Independant System

CHARACTERISTIC	1987	1995	2000
Cost	Fair	Fair	Fair
Power	Good	Good	Excellent
Space/Size/Weight	Fair	Fair	Good
Accuracy	Good	Good	Excellent
Reliability	Good	Good	Good
User Friendly	Excellent	Excellent	Excellent

1.2.2.2.4 References

1) G. White, "Speech Recognition: An Idea Whose Time is Coming."

2) A. M. Godwin and Dr. J. C. Ruth, "Voice Command, The Next Threshold in Cockpit Operation," General Dynamics, Fort Worth, Texas.

3) S. Ross and J. McAllister, "Practical and Continuous Speech Recognition," Computer Design, June 15, 1984.

1.3 DATA PROCESSING HARDWARE

By its very nature, the applicability of data processing (DP) hardware is broad and varied. This applicability includes: ground/space environments; general purpose to specialized capabilities; and a wide range of applications within the SSDS.

The overall subject of Data Processing will be addressed as five basic categories; (1) Fault tolerant (FT) computers, (2) Special purpose computers, (3) General purpose (GP) computers, (4) Flight computers, and (5) Advanced computer architectures.

Some sections address capabilities that are not expected to be included in the SSDS (i.e. signal processor, etc.) but are included to give insight into their potential impact on the SSDS.

The section on "advanced architectures" is included to identify potential growth options that may deviate from traditional architectures. While the scope of this category is broad, it is not intended to be a comprehensive survey of DP hardware that is currently available. Sufficient representative vendor data is included to establish the current state-of-the-art (SOA) and identify trends.

We have also included data from new projects that are expected to mature within the next few years as a key source of projection data.

The goal of this paper is to survey the DP options and provide characteristics and costs in sufficient detail to support associated Task 3 trade study. These options must be evaluated against not only the design requirements but also the key Space Station programmatic requirements of commonality, standardization, etc.

Special processors dedicated to network communications (i.e. BIU's, gateways, etc.) are covered in Section 1.7.1.2.

1.3.1 Fault Tolerant Computer Architecture

1.3.1.1 Description

Fault tolerance F/T is the survival attribute of a computer architecture and allows a system to recover automatically from fault-caused errors, and to eliminate faults without suffering an externally perceived failure.

Prior to 1960, fault tolerant/automated fault recovery concepts were not considered cost effective because redundant hardware and fault recovery mechanisms added considerably to system costs. Software techniques, i.e. instruction retry, error detection codes, etc. were implemented but the emphasis was on rapid fault isolation and repair in order to minimize system downtime. During the 1960's, however, application of computers to spacecraft control and telephone switching systems, where costs of computer failure were very high, led to further development and application of fault tolerant concepts and implementations. By the end of the 1960's nearly all of the basic forms of F/T architecture found in later designs triple modular redundancy (TMR), redundancy/compare, self-checking, and back-up sparing) had been explored and were being refined for more modern implementations. Special F/T architectures developed over the last decade are now being further developed and translated into LSI and VLSI technologies for commercial, military and space markets.

The intent of this section is to provide an overview of recent/current F/T architectures along with an indication of their performance characteristics. The discussion will be limited to hardware intensive F/T implementations; however details of their F/T mechanisms will not generally be provided. A comprehensive discussion of hardware and software F/T concepts and mechanisms is provided in Section 2.2.1.

The fault-tolerant (F/T) computer options to be considered have been categorized into two groups: commercial systems and systems developed/sponsored by NASA or DOD.

1.3.1.2 Option Characterization

1.3.1.2.1 Commercial Systems

With the significant reduction of hardware costs, hardware redundancy techniques are now being utilized in a large number of 'real time' applications under the pressure of consumer demands. The commercial market has therefore produced a broad line of F/T systems, with an emphasis on 'on line transaction processing' (OLTP). Leaders in this area are the Tandem 'Non-Stop' series and systems developed by Stratus and Synapse.

The Tandem approach to F/T in their 'Non-Stop' series was systematic, eliminating the master-slave relationships and utilizing replicated processors, dual access to I/O controllers, dual power systems, and dual paths to subsystems. Checkpointing is the key recovery mechanism for this product line. This technique involves periodically updating a back-up processor/ memory to provide a roll-back point in the event of failure. The approach is effective but does extract a 15% - 30% performance penalty. This system was one of the first to allow on-line repair, i.e. replacement of circuit cards, etc. without disturbing current applications.

The Stratus systems utilized the 'pair and spare' (quad replication) concept for processors and memories with redundant subsystems. If the outputs of each lock-stepped pair do not compare then the hot spare continues the operation. This approach is attractive since it requires no 'recovery' from a fault and requires no special F/T software programming. The basic system remains relatively inexpensive even with a maximum of 18 processors since off-the-shelf MC68000 and Z80A units are used.

The disadvantage of the 'pair and spare' approach is that expansion requires the additional volume, power, and expense of (quad) replication. The Synapse systems avoid this problem utilizing an 'N + 1' architectural approach in which only one additional processor is provided above the estimated workload

requirement. In this system multiple MC68000 processors are tightly coupled through a high speed bus to a common (shared) memory. The processors are self dispatched and pick up processing tasks from the common memory. Since tasking is dynamic, the additional processor provides the same F/T depth as a replicated '2N' system.

Table 1.3.1-1 summarizes the features, performance and intended usage of a representative sample of commercial systems. This table is not intended to imply a direct utility of these systems for Space Station but does, (primarily because of reduced hardware costs), demonstrate the increasing practicality of fault tolerance.

Table 1.3.1-1 (Page 1 of 2)

COMMERCIAL FAULT-TOLERANT SYSTEMS

COMPANY/SYSTEM	CPU TECHNOLOGY	MEMORY SYSTEM	PERFORMANCE/CPU (MIPS and TPS -	FT STRATEGY	CPU FAULT DETECTION
August Systems, Inc./ Can't Fail 300	Three Intel Corp 8086 based processors run identical code when in FT mode.	32K bytes per CPU on-board: up to 1M byte per CPU on Multibus.	Approximately 0.4 MIPS -up to 256 A/D points TPS not relevant.	CPUs: SIFT: analog front end: TMR	At start of each iteration three CPUs check state data and vote out odd processor.
Auragen Systems Corp/ System 4000	Up to 32 clusters of three Motorola 68010 each: clusters inter-connect over a high-speed duplex 32-bit bus.	Up to 8M bytes per cluster (1M byte/ board.	0.85 MIPS/cluster (company figure). Nominally 27 MIPS/ system at full expansion 1.5 TPS/CPU (estimate)	Queue and count	Self-detect via idle diagnostics and absence of "I'm alive" messages.
Autech Corp./ DAC-6000	Dual 68000-based Displaymaster and Decmaster. Zilog, Inc. Z80A-based process I/O modules.	64K bytes to 256K bytes per CPU, with parity battery backup on board CMOS static.	Decmaster supports up to 256 process points TPS not relevant.	Hot backup	Timeouts, cross diagnostics.
Computer Consoles, Inc./Power 55/5	Up to eight 68000-based CPUs with 68000-based disk and terminal controllers.	512K bytes to 4M bytes per CPU error checking and correction, battery backup. Each of two ICCs has 512K bytes.	Nominally 5.6 MIPs (0.7 per 68000). Two TPS/ CPU (ITOM estimate) due to multicopy database.	Checkpointing	ICC timeout transactions; bad ICCs detected by CPU voting scheme.
Hewlett-Packard Co./ Systemsate/1000	Two HP1000 Models 60 or 65 working in "hot backup" mode (16-bit microprogrammed).	256K bytes to 2M bytes per CPU. 1 parity bit/16 bits of data.	1 MIPS (200K floating point operation/sec mod 65). TPS not relevant.	Hot backup	Watchdog timer times out.
Parallel Computers Inc./Parallel 300	Two 68010's on a multi-bus.	Maximum 4M bytes/ processor.	0.7 MIPS	Hot backup	Hardware and software synchronization between CPUs.
Sequoia Systems/ No Name Yet	Up to 64 CPUs and 96 IOPs all 68010-based and self-checking.	2M bytes to 64M bytes with ECC (seven bits per bit word)	Sequoia claims up to 40 MIPS at full expansion	Automatic reassignment	Self-checking subsystem electrically disconnects.

Table 1.3.1-1 (Page 2 of 2)

COMMERCIAL FAULT-TOLERANT SYSTEMS

COMPANY/SYSTEM	CPU TECHNOLOGY	MEMORY SYSTEM	PERFORMANCE/CPU (MIPS and TPS	FT STRATEGY	CPU FAULT DETECTION
Stratus Computer Inc./ FT200, XA400, XA600	Self-checking CPUs based on Motorola 68000s. Each Processing Module can have duplexed CPU memory and controllers. Max. 32 Processing Modules on a ring-type local area network.	FT200; 8M bytes logical XA400 (16M bytes physical) XA600; 16M bytes logical (32M bytes physical)	0.7.2.0.3.0 MIPS 2.4 6 TPS for FT200, XA400, and XA600 respectively.	Pair and spare	Self-checking subsystem pulls out and generates red-light interrupt to operating system.
Synapse Computer Corp./ Synapse N + 1	Up to 28 68000-based CPUs and IOPs (I/O processors) working with a shared memory via a duplexed, high-speed 32-bit parallel bus.	16M bytes/system (1M byte boards), error checking and correction.	0.7 MIPS/CPU; system MIPS depend on how many CPUs configured, 2 TPS/CPU (1TOM estimate) if supported by enough I/O processors.	Checkpointing	Timeout mechanisms.
Tandem Computers, Inc./ NonStop I, II, TXP	Up to 16 CPUs on a duplexed, high-speed, 16-bit parallel bus. CPU is 16-bit microprogrammed.	8M bytes/CPU (2M bytes/ board), error checking and correction.	0.7, 0.8,, 2 MIPS; 1, 1.5 5 to 6 TPS for Nonstop I, II, and TXP, respectively.	Checkpointing	Absence of "I'm alive" message; each CPU must broadcast over Dynabus each second.
Tolerant Transaction Systems/Eternity	Two National Semiconductor Corp. 16000's in each system building block.	1M byte to 4M bytes per system building block.	1.5 MIPS/system building block (Tolerant estimate)	Checkpointing	Timeouts and "I'm alive" message.

1.3.1.2.2 NASA/DOD Sponsored Systems

A number of research and project specific F/T systems have been sponsored by NASA/DoD over the past several years. Table 1.3.1-2 list the more prominent examples along with their primary characteristics. These systems were developed primarily to forward particular concepts of architecture and reliability rather than to achieve particular performance characteristics. As noted earlier, hardware techniques are primarily utilized which renders the F/T mechanisms generally transparent to the application software and in fact impose relatively small (if any) processing overhead on the system. Performance characteristics (throughput, data formats, bus protocols etc) are therefore not important in these discussions since, in general, processors and memories can be upgraded without altering the F/T implementations. Brief details of some of the more significant systems are provided in the following.

o FTMP - Fault Tolerant Multi-Processor

The FTMP, initially developed for potential use in commercial aircraft, utilizes TMR techniques wherein three copies of the applications program are executed in a synchronized triad of processors and memories. The results are hardware voted to mask faults. The system processors and memories are interconnected to five redundant busses through special bus guardian circuits and are dynamically assigned to the processing triads as shown in Figure 1.3.1-1. The initial design goals for this system were 10^{-9} fails/hour over a 10 hour mission.

o AIPS - Advanced Information Processing System

AIPS is an extension of the FTMP concepts to a distributed system. A group of processing sites are connected through switching nodes to a redundant intercommunication structure that acts as a triply redundant bus. Each processing site may utilize an FTMP, or TMR processors, or a single non-redundant machine. A local clock is provided at each site to synchronize its processors however there is no inter-site synchonization. Hardware voting is provided throughout the system however voting across multiple sites is more difficult due to the lack of synchronization. Figure 1.3.1-2 shows the basic AIPS architecture concept.

Table 1.3.1-2
NASA/DoD Sponsored Fault Tolerant Technologies

SPONSOR/DEVELOPER	NAME	PRIMARY CHARACTERISTICS
NASA/CSDL	FTMP	Fault Tolerant Multiple Processor - TMR approach
NASA/CSDL	AIPS	Advanced Information Processing System. FTMP Concepts applied to distributed system.
NASA/CMU	C. Vmp (VLSI implemented of architecture)	Experimental Triplicated Processor Architecture - A Voted Multiple Processor
DoD	Pluribus	Fault Free Network Modes
NASA/JPL	STAR	Self-Testing and Repair. Reconfiguration with cold back-up unit under control of TMR Test & Repair processor.
NASA	Space Shuttle	4 Modular Redundant computers with voting. Fifth unit-non redundant back-up.

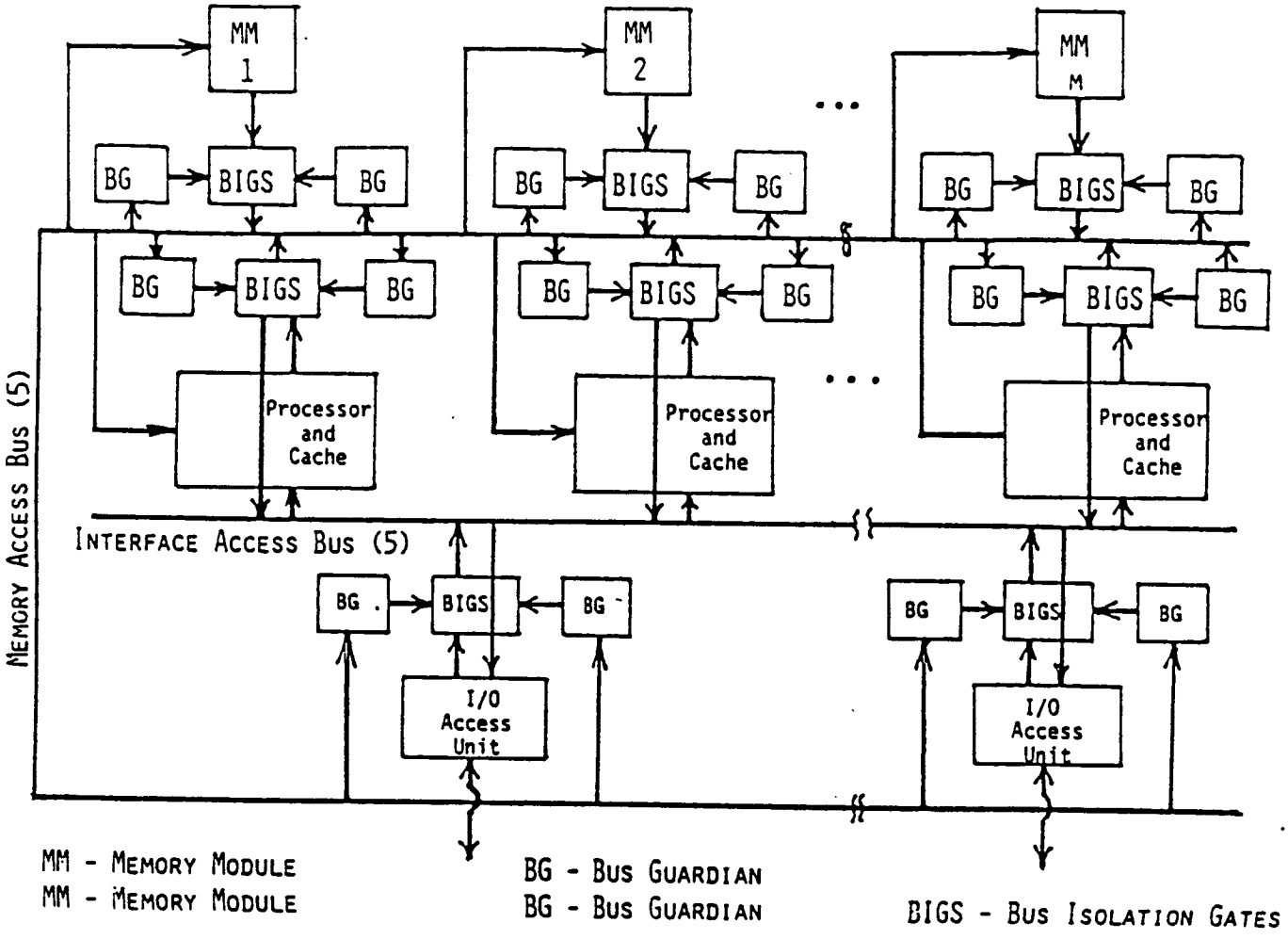


Figure 1.3.1-1 FTMP Architecture

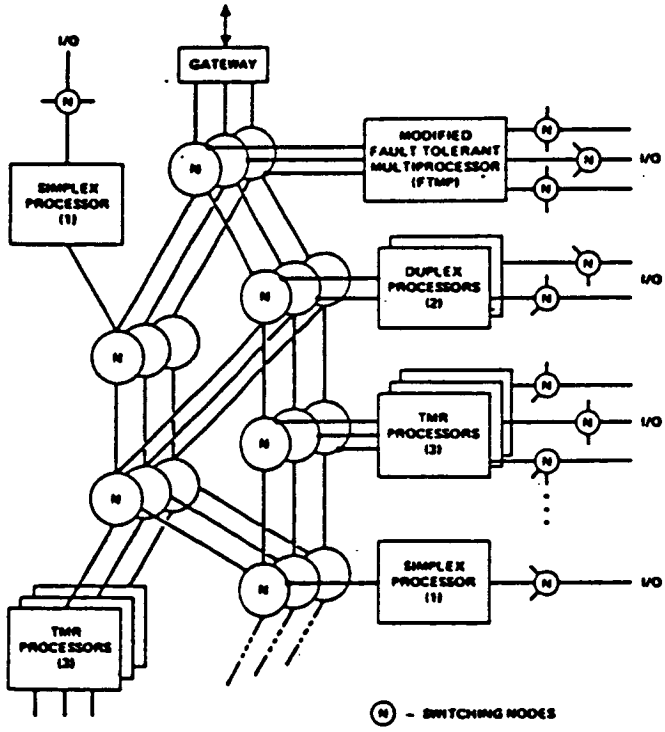


Figure 1.3.1-2 AIPS Architecture

o STAR - Self Test and Recovery

The JPL-STAR computer was developed for long un-maintained life during deep space missions and had the capability to detect, reconfigurate and recover from a hardware failure. The computer was subdivided into its functional units, i.e. processors, memories, and a Test & Repair processor. Only one unit of each type would be powered at a time because of the limited power resources; the backup units would be maintained as cold spares. Each unit was designed to detect and signal any internal fault. The tri-modular redundant (TMR) Test & Repair processor, would then replace the faulty unit.

o Shuttle Flight Control System

Perhaps the best known of the NASA sponsored architectures is the flight system currently in use on the NSTS Orbiter. This system utilizes five IBM AP-101 computers coupled with separate I/O processors in a four modular redundancy configuration. The fifth unit, utilizing a different coding of the flight program, is manually switched in as a separate, non-redundant computer if two of the primary units fail. Computer, memory, I/O, and inter-connecting bus redundancy is provided through-out the system to provide an over-all reliability such that:

- o no singly failure can affect the mission, and,
- o no second failure can endanger the crew.

1.3.1.3 Projected Capabilities

With increasingly lower hardware costs, F/T techniques become more practical across an increasingly larger applications set. These techniques must accommodate the natural system architectural and technological development paths. These paths are clearly moving toward VLSI and in many cases toward distributed implementations. VLSI designers are expected to sparingly allocate die real estate to F/T structures, therefore, replication will generally be continued as the mainstay of F/T systems. It is anticipated that the quad-redundant approaches, i.e. pair and spare, or pair shadowing, will predominate because of their self-checking capabilities and the potential to continue the processing essentially uninterrupted. Also, the AIPS concepts

are favorable to the Space Station environment since damage tolerance is available from the physical disbursement of functionally redundant components and sufficiently high bandwidth busses are now available. Once the hardware is established then the software concepts will be tailored to match. Coupled with increasingly reliable basic hardware and software products, F/T systems in everyday applications will exhibit reliabilities that exceed the goals of today's research.

1.3.1.4 References

1. D. Siewiorek, "Architecture of Fault Tolerant Computers," Computer, Vol. 17, Number 1, August, 1984, pp. 9-18.

2. O. Serlin, "Fault Tolerant Systems in Commercial Applications," Computer, Vol. 17, August 1984, pp. 19-30.

3. D. Rennek, "Architectures for Fault-Tolerant Spacecraft Computers," Proc IEEE, Vol. 66, pp. 1255-1268, October 1978.

4. R. Sedmack and H. Liebergot, "Fault-Tolerance of a General Purpose Computer Implemented by Very Large Scale Integration," "IEEE Trans. Comput," Vol. C-20, pp. 492-500, June 1980.

5. D. P. Siewiorek, et al, "A Case Study of C.mmp, Cm*, and C.Vmp: Part I - Experiences with Fault Tolerance in Multiprocessor Systems," Proc. IEEE, Vol. 6, No. 10, October 1978, pp. 1178-1199.

1.3.2 Special Purpose Computers

1.3.2.1 Description. This category includes processors that are primarily designed as an adjunct to a general processor (GP) host computer system and/or provide solutions to specialized problems. In general, special purpose computers achieve high performance at the expense of flexibility. In some cases, the required performance levels (throughput, response times, etc.) are achieved through the use of special purpose architectures and devices that are configured to match the problem domain. In other cases, such solutions represent cost-effective alternatives to general purpose approaches. Many of these options are a direct consequence of recent trends toward functional modularity and multiprocessing in the larger general purpose computer systems. The options in this category include:

- Signal Processors
- Array Processors
- Data Base Machines
- AI Processors
- Communications Processors
- Graphics Processors

1.3.2.2 Option Characterization.

1.3.2.2.1 Signal Processors

Signal processing is a broad generic term generally used to describe highly-specialized, real-time processing of "sensor" data such as filtering/smoothing, data compression, target detection, image correlation, spectrum analysis, etc. Typical sensors requiring such processing includes imaging/scanning electra-optics, sonar, and various types of radar. Signal processing algorithms are usually computationally simple, but because of the high data rates associated with evolving sensor technology, their implementation often requires a special-purpose architecture to provide sufficient throughput within reasonable size constraints (generally located in close proximity to the sensor). To achieve the necessary performance levels, signal processors exploit the application-specific features of a system, employ architectures that are matched to the flow of sensor data, and tend to use the latest SOA high-speed circuits. Because of the application dependency of signal processors, it is not meaningful to generalize their performance characteristics.

While signal processors are highly-specialized for specific applications, the degree of specialization (and, inversely, the degree of flexibility) can vary significantly. A performance versus flexibility trade-off analysis would have to consider a wide spectrum of implementation and packaging alternatives including the following:

- o Custom chip development
- o Programmable Logic Arrays (PLA's), Gate Arrays
- o "Hardwire" Logic with Available Circuits
- o Bit-slice, microcode
- o Programmable processor arrays
- o Etc.

One might anticipate that with the tremendous improvements in circuit technology (speed, memory density, etc.,), signal processors would tend to become more general purpose (flexibility, standardization, etc.) and, in fact, some have. However, new sensor requirements and design characteristics continue to stress signal processor technology with ever increasing data rates and required functionality. In response to evolving DoD system/sensor requirements, the very high speed integrated circuit (VHSIC) program is sponsoring high-speed, signal processing VLSI chip design, and fabrication techniques. The ultimate goal of VHSIC is to achieve pilot production in 1986 of processors with the following features:

- o >250,000 gates
- o Clock speeds >25 MHZ
- o Several million to billion operations/second
- o 0.5 μm dimensions
- o Radiation dose up to $10^{11}/cm^2$
- o Built-in-test at the chip level

These characteristics are to be obtained by scaling down integrated circuits, reducing channel length and oxide thickness, decreasing supply voltage, and developing new types of architecture and software. Also, it has been recognized that custom designs for a specific system tend to limit the market over which high technology costs can be amortized. This problem will be addressed by greater standardization and the increased use of programmable

devices. Many of these standard modules will be applicable to NASA signal processing needs. Table 1.3.2-1 summarizes VHSIC design approaches, typical chips, and some of their key characteristics.

1.3.2.2.2 Array Processors

Array processors, as defined here, are highly parallel architectures using relatively large, structured arrays of processing elements. Connected to a general purpose host processor, these processors provide fast solutions to problems involving large sets of data and repetitive mathematical (vector or matrix) functions, digital filtering and fast Fourier transforms FFT's. Historically, this has implied large-scale, single-instruction-multiple-data (SIMD) processors such as the ILLIAC IV or NASA's massively parallel processor (MPP). We will extend this definition to also include more flexible array structures such as the following research projects:

- Cedar System, University of Illinois
- Texas Reconfigurable Array Computer (TRAC), University of Texas
- Blue Chip, Configurable Highly Parallel Computer, Purdue University

Other multiple-instruction-multiple-data (MIMD) multiprocessor architectures, such as Denelcor's Heterogeneous Element Processor (HEP) and CDC's Advanced Flexible Processor (AFP) use smaller arrays with flexible interconnections and more powerful processing elements to provide similar capabilities (see Section 1.3.3). However, the current SOA technology in array processors is the NASA MPP summarized in Table 1.3.2-2.

A projection of the large scale array processor performance is shown in Figure 1.3.2-1.

Typical of many general and special purpose areas of processing, smaller scale array processors are being provided in circuit board configurations supporting a specific back plane. Sky Computers, for example, has introduced a 15MFLOP Warrior array processor on a 2 VME card configuration. Mercury Computer Systems has provided a similar 3 board package in their ZIP 3232, 15 MFLOP array processor. Both units execute a 1K complex FFT in approximately 3 msec. The ZIP units are designed with a 'data flow' architecture to provide hardware synchronization that is transparent to programmer. Another development in the array processor field is NCR's Geometric Arithmetic

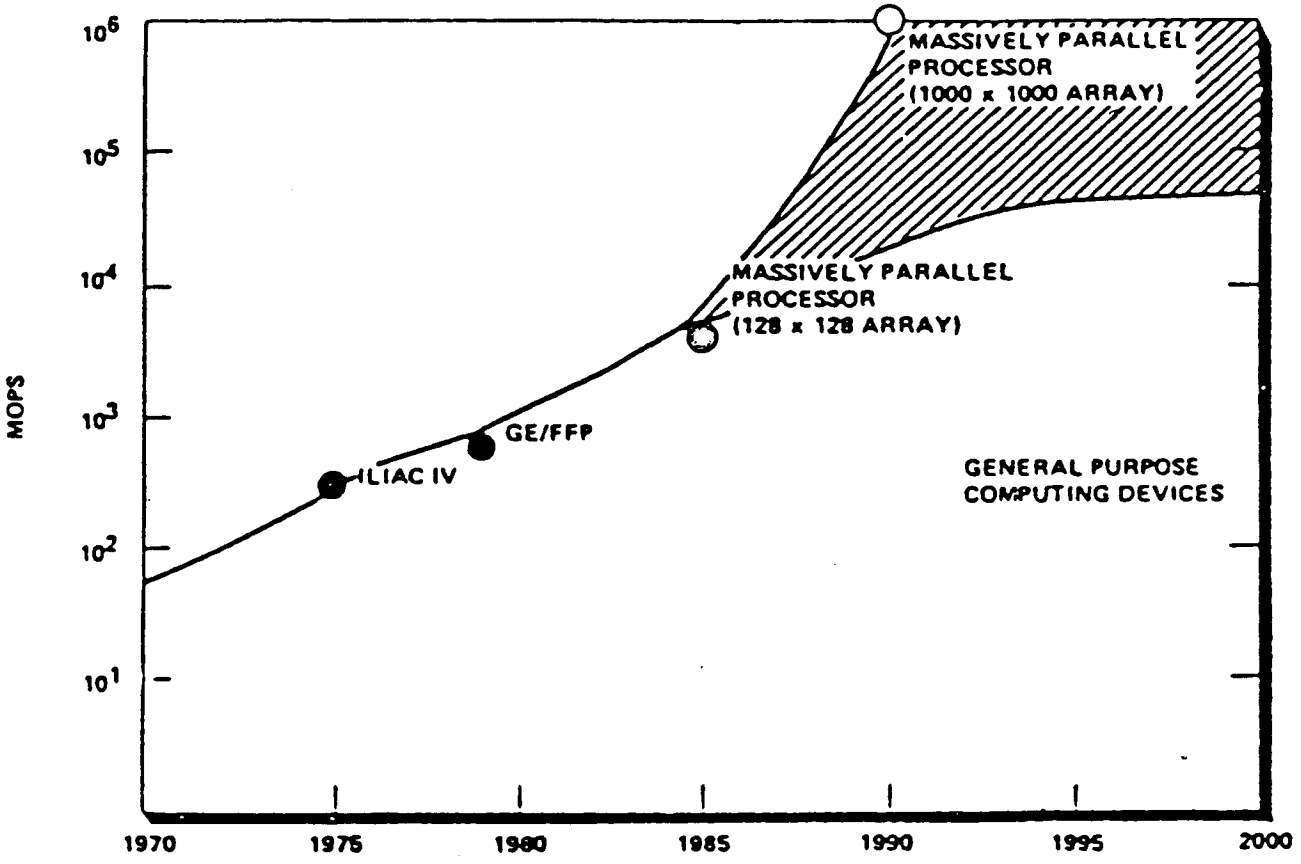


Figure 1.3.2-1 Array Processor Performance

Table 1.3.2-1 Phase I (1.25 μm) VHSIC Sponsored Technology Characteristics

DESIGN APPROACH	CHIP SET	GATE DENSITY (GATES/ mm2)	GATE POWER (μ/ GATE)	SPECIAL FEATURES
Custom-chip-based macrocell library	Parallel programmable pipeline Controller	480	30	Radiation hardness Responsive generic architecture
Standard and custom reconfigurable chips	Digital correlator Algebraic encoder/decoder Spread spectrum subsystem	400	2	Radiation hardness Electron-beam direct-write lithography Highly specialized chips
Master Image with macrocell library	Complex multiplier/ accumulator	570	100	Software strength Design approach
Programmable chip set	Data processor Array controller and sequencer Vector address generator Vector arithmetic logic unit Static RAM Multipath switch Device interface unit General buffer unit	390	37	Operational fabrication facility Design utility system
Standard chip set	Content addressable memory Window addressable memory Address generator Matrix switch 15-bit multiplier/ accumulator Microcontroller Four-port memory	TTL390 CMOS300	240 20	Innovative memory chips Versatile chip set
Standard chip set	Pipeline arithmetic unit Extended arithmetic unit Controller Gate array Static RAM Multiplier	1000	4	Highest speeds

Table 1.3.2-2 MPP CHARACTERISTICS

- o Architecture
  - Large scale, SIMD array processor
  - Consists of 4 major units; host computer, array control unit, array unit, staging memory
  - 16,384 processors (12.8 x 128 array)
  - 64 Mbytes staging memory
- o Performance
  - 6.5×10^9 fixed-point additions per second
  - 1.8×10^9 multiplies (8-bit) per second
  - Near real-time image processing applications
- o Physical
  - Dimensions = 74 x 88 x 28 inches
  - Weight = 2,500 lbs.
  - Cooling - Forced Air
  - Power = 20 KW
- o Available Support Software
  - Cross assemblers linker, loader, librarian
  - I/O services macro library
  - Control and debug services
  - Diagnostics
- o Programmatics
  - Delivered to NASA/GSFC in 1983
  - Cost 4-6M$

The commercially available Britton-Lee Intelligent Database Machine (IDM) series loosely fits the category of backend processors because it is designed to operate in support of one or more hosts. The IDM utilizes an architecture far from general purpose however. The company's largest unit, the IDM 500/2 consists of a database processor, data base accelerator, up to 6M bytes of memory, disk and tape controllers, and an interface to the host computer. The database accelerator has a three-stage instruction pipeline that can perform to 10 MIPS. The IDM is essentially a software implementation of a relational data base management system (DBMS) housed in special hardware. In operation, the IDM traverses binary-tree index structures to locate requested data similar to a software implementation; no special purpose parallel data search hardware is provided, however multiple queries can be simultaneously processed. Table 1.3.2-3 provides characteristics of this unit.

Table 1.3.2-3
BRITTEN-LEE INTELLIGENT DATA BASE MACHINE CHARACTERISTICS

o Storage Capacity	32×10^9 Bytes
o Data Model	Relational
o Max No. of Hosts	64
o Max. Memory	6 Mbytes
o Interfaces	RS232, IEEE-488 IBM Block Max., Ethernet
o Compatible Hosts	DEC VAX/PDP, IBM 43XX, 30XX, 370 IBM PC
o Physical - Weight - Dimensions	(without mass storage) 170 lbs. 17.5 x 19 x 26 inches
o Performance	10 MIPS database accelerator processor (MECL)
o Support Software	Host-resident query language Report generation facilities App. programming tools DBMS administration utilities
o Cost	$155K

1.3.2.2.3.2 Intelligent Controllers and Associative Memories

In the mid 1970's, associative (content addressable) concepts were introduced to backend attachments. The Relational Associative Processor (RAP) begun at the University of Toronto in 1974, was one of the first data base systems to incorporate parallel processing. RAP used an array of processing elements, each working on a portion of the total data base to provide direct hardware support for the normalized relational model.

The first commercially available implementation of associative memory techniques applied to a relational data base was the Synfobase by Corem International. This system is built around an Zilog Z80 with 64K bytes of RAM, up to 10M bytes of Winchester disk and 8K of associative memory. With a disk to associative memory transfer rate of 200K bytes/sec, a 10M byte disk can be 'associated' in under 1 minute. The 10M byte version of this system is available for approximately $10M.

The principal benefit of these approaches is reduced data base access time however associative memories are expensive and will be size limited which creates a data bottleneck in paging data in and out of memory.

1.3.2.2.3.3 Data Base Computers

Data base computers (or integrated data base machines) have succeeded intelligent controllers in the architecture evolution. These are complete systems which consist of general-purpose and special-purpose devices serving as functionally specialized processors. For example, such a system might consist of a general-purpose system processor, an associative processor for directory access, and intelligent mass storage controllers for data base processing. Examples of research in the area of data base computers include the Data Base Computer project at Ohio State University, RAP.2 at the University of Toronto, and INFOPLEX at MIT.

1.3.2.2.4 AI Processors

AI processors are a recent innovation that employ special hardware/firmware features and facilitate AI-based applications and development. These processors are based on AI languages such as list processors (LISP) that are traditionally used to develop AI programs. While such programs have been previously developed and executed on traditional mainframes/minicomputers, AI processors can offer enhanced speed and efficiency because they are "tuned" to the language structure and operating environment. Earlier versions tended to be dedicated, single-user environments. However, newer machines are beginning to emerge that offer modern operating system compatibility (i.e. UNIX), a wider choice of standard peripherals, and flexible networking capabilities (i.e. ETHERNET, etc.). The characteristics of currently available AI processors are summarized in Table 1.3.2-4.

TABLE 1.3.2-4
AI PROCESSOR CHARACTERISTICS

CHARACTERISTICS	XEROX 1132	SYMBOLIC S3670	LMI LAMBDA	TI-EXPLORER
System Architecture	Spec. ECL Processor and microcode to execute LISP.	Spec processor and microcode to execute on MIT CADR. Spec 36 bit bus	Spec processor and microcode to execute LISP. Based on MIT CADR Spec 32 bit bus. Opt UNIX 68010 co-processor	Spec processor and microcode to execute LISP. Based on MIT CADR. Spec 32 bit bus
Main Memory	2M bytes - 32 M bytes	2M bytes - 30M bytes	4M bytes	2M bytes - 16M bytes
Virtual Memory	32M bytes	15-16M bytes	128M bytes	128M bytes
Storage	80M bytes disk opt. to 315M bytes	167.5-474M bytes Streamer tape cassette	169/470M bytes rigid disk standard tapes	112M bytes disk opt. streamer tapes
Software Environment	INTERLISP with SMALLTALK	ZETALISP, ZMACS editor, INTERLISP, ADA, FORTRAN	ZETALISP, INTERLISP PROLOG ADA, ZMACS editor	Common LISP, ZMACS editor
Networking	10MHz ETHERNET Opt for ser/para ports.	10MHz ETHERNET Opt Serial Port	10MHz ETHERNET Opt Serial Port	10MHz ETHERNET Serial/Parallel port
Size	17 ft^3	31 ft^3	27 ft^3	3.4 ft^3
Weight	240 lbs	700-800 lbs	700 lbs	60 lbs
Cost	~$130K	~$100K	~$90K	~$50K

There is also development activity toward flight/space qualified AI machines. Ames Research Center for example is currently in joint venture with Symbolics to develop a flight qualified LISP processor. The first target is the Symbolics S3640 although the end result is expected to be a smaller, different machine. Also, a $6 Million contract was awarded by the Navy ESC to T.I. to develop a compact LISP machine utilizing a 2-micron CMOS VLSI processor. The computer will incorporate a 1.25 micron SRAM and will operate at speeds up to 40 MHz providing up to 10 times the processing power of today's units. Production of this unit is scheduled for 1987.

1.3.2.2.5 Communications Processors

This class of special purpose processors has an architecture designed specifically to support digital communications functions, i.e. modulation/demodulation, interleaving/de-interleaving, encoding/de-encoding, formatting and routing. These processors generally provide multi-channel support and therefore have a modular form with specialized bus configurations.

An example in this category is the Raytheon Wideband Signal Processor (WBSP) classified as a fault tolerant communications processor. Intended to operate as a peripheral to the Raytheon Fault Tolerant Space Computer (FTSC), the WBSP will handle all of the signal processing for a wide latitude of applications by tailoring its A/D, modulation, interleaving and encoding modules and algorithms. The WBSP provides 5 busses to interconnect these processor elements plus a FTSC interface controller to route demodulated data to the FTSC and accept data for modulation/transmission.

In the area of fault tolerance, the FTSC monitors the WBSP through data formats, i.e. trailers that contain sum checks, etc. In addition, special (spare) monitoring processors are used to duplicate functions of active processors on a time shared basis. Once a fault is detected, reconfiguration of the WBSP is managed by the FTSC.

Typically real time communications processors are not a standard configuration item; architectures must be tailored to the particular application and will depend on functions to be performed, I/O servicing and peak throughput (bit/sec). This would be particularly true of space station with its high (up to 600 mbit/sec rates. Performances in the range of 50-100 million operations per second (MOPS) are anticipated and will require new architectures, and new technologies.

1.3.2.2.6 Graphics Processors

With the increasing usage of computerized graphics for CAD/CAM, VLSI design, simulations, and mapping etc., special architectures and capabilities are being developed to provide essential tools for these applications. The key attributes of graphics systems are their screen resolution (pixel field formats), performance (screen update speed), and number of colors. Specialized features include editing, rotation, zooming, panning (scrolling), windowing, and color enhancement/selection. These systems typically are implemented as 'back-end' computers, off-loading the purely graphics oriented tasks from a host machine to a more efficient graphics machine.

The basic graphics system must accept commands and data from a host unit and/or interactively via keyboard, data tablet or joystick, perform the data/command transformations and generate the appropriate screen display. The basic functions are the command processing, graphics or drawing processing, display processing and scanning/raster processing.

The command processor accepts data and commands (display lists) from the host/user, transforms the data and interprets commands for the graphics processor. The graphics or drawing processor maintains the data base geometries of the display objects and performs the additional transformations to generate figures per data and commands. This data can be in the form of vector data/instructions that are passed on to the display processing function. The display processor performs the vector transformations to convert the vectors into specific pixel patterns modified as necessary by the format, orientation and color commands. This information is typically provided as coded bit maps in the video memory. This format provides a code word that defines a specific color via look-up tables in the video memory. The scanning/raster function reads the video memory and issues this color/intensity control data to the DAC circuitry that drives the CRT and provides RGB outputs for external display devices.

The recent trend has been to functionally partition the graphics units into multiprocessor designs for performance improvement. The Lexidata 8100/GS represents an early example of this approach, utilizing an MC68000 for the command and graphics processing and a separate high speed bipolar unit for the

display/raster/scanner processor. The improved LEX 90/35 operates more interactively with the host utilizing a 16 bit-slice graphics processor, transferring data from host at a 2M byte rate.

In this same trend, Synertek has a pair of NMOS LSI devices (graphics processor and raster/scanner) that can be assembled into a graphics controller for a 4096 X 4096 pixel display that is 32 planes deep. These devices, operable separately or in tandem, should find a home in midrange graphics workstations and desktop computers.

Characterization/costs of representative commercial units are shown in Table 1.3.2-5

Table 1.3.2-5
GRAPHICS MACHINES CHARACTERISTICS

Characteristics	Calcomp Vista Graphic 4500	Lexidata 90/35 Model 2	Chromatics CX 1500
Front End Processor	MC68000	MC68000	MC68000
Graphics Processor	AMD2903	AMD2900	bi-polar
Format	16/32	16	16/32
Array Processor	No	No	Yes
Resolution	1280 x 1024	1280 x 1024	1536 x 1152
Gray/Scale	8 bits	12 bits	24 bits
Double Buffer	Yes	Yes	Yes
Performance	125 nsec/pixel	375 nsec/pixel	50 nsec/pixel
Processor Clock Speed	N/A	12 MHz	N/A
Random Pixel Access	125 msec	375 msec	125 msec
Data Transfer	1 Mbyte/sec	1 Mbyte/sec	2 Mbyte/sec
Size			
Monitor	5.7 ft^3	TBS	3.4 ft^3
Engine	5 ft^3	1.5 ft^3	11.6 ft^3
Weight			
Man	70 lbs	TBS	N/A
Elec	110 lbs	45 lbs	N/A
Power	N/A	250-400W	750-1200W

1.3.2.2.6.1 Future Trends

Currently available 'raster/scan' commercial units typically have 1280 x 1024 pixel resolution, 256 to 16 million colors, and performance figures of 100M/sec pixel updates, and 60K random vectors/sec. This technology provides superior colors over 'vector refresh' techniques at a lower cost and is not subject to screen flicker under heavy processsing loads. The 'raster/scan' units are generally inferior in resolution and are not competitive in animation capabilities. True parallel processing architectures are also being pursued particularly to support the enormous performance requirements of 3-D modeling. The key issue in the parallel designs is task partitioning; the more popular approach currently is to assign each processor a discrete portion of the display screen.

There is also a trend to hardware transformation, wherein large scale integrated (LSI) circuitry is used to perform specific mathematical transformations, i.e. rotation, scaling, shading, etc. This approach is estimated to provide a X100 gain in performance over the standard software techniques. These developing units generally promise higher resolution, higher performance, animation, and 3-D modeling.

1.3.3 General Purpose Computers

1.3.3.1 Description. This category includes computers that are classified as general purpose in nature and have broad capabilities to support varied applications. The options in this category differ primarily in their range of performance capabilities and in their cost. While performance boundaries are continually changing and are not always clearly definable, the options in this category can be described in a relative manner by the following traditional classification:

- Supercomputers
- Mainframes
- Minicomputers
- Microcomputers
- Microprocessors

Performance capabilities for all of these options will continue to improve somewhat uniformly. Architectural innovations tend to be introduced at the high end (supercomputers) where users are continually striving for higher levels of performance. As these concepts mature, they tend to become incorporated in new products at the lower end thus boosting performance in all areas. The Intel 386 and Motorola 68020 are examples of new microprocessor products that are incorporating on-chip some of the more mature architectural innovations that previously existed only in much large, high-performance systems (i.e., multiprocessing, virtual memory, etc.). On the other hand, improvements in circuit design/density and packaging techniques are initially introduced at the low-performance end where the emphasis is on reduced cost, size and power. This is illustrated by new microprocessor products with over 200,000 transistors on a chip and featuring 32-bit architectures, cache memory, and multiple co-processors (10^6 transistors/chip expected in the near future). These VLSI packaging techniques and fabrication processes are now being applied to high-speed circuitry and will significantly improve performance/cost and performance/size ratios for all levels of performance.

In the past, selection of one of these options for a given application was relatively straightforward. The computer was selected that best met the performance requirements at the lowest cost. However, recent advances in local/remote area networking now provide cost-effective alternatives to centralized computer facilities. For many applications a Local Area Network (LAN) of minicomputers may be a better solution (i.e. cost, performance, reliability, etc.) than a large mainframe or supercomputer. From the user's point of view, the ability to use smaller, less expensive computers to do tasks previously only possible on large systems will continue to provide independence from central control.

The viability of the traditional "computer center" has been placed in jeopardy except for classes of service in which the center can continue to hold a cost-effective edge. For the near-term this will probably include "supercomputer" scientific applications and large data base utility applications where performance will continue to be attractive in a centralized facility.

1.3.3.2 Option Characterization. A summary of SOA characteristics for the general purpose computer options is provided in Table 1.3.3-1. The options are further described in the following sections.

Table 1.3.3-1
CURRENT GENERAL PURPOSE COMPUTER COMPARISON

	MICRO	MINI	MAINFRAME	SUPERCOMPUTERS
ARCHITECTURE	VARIABLE	VARIABLE	VARIABLE	VECTOR (ARRAY)
THROUGHPUT (MIPS)	.1 - .5	.5 - 3.5	3 - 30	30 - 100 (SCALAR) - 800 (VECTOR)
MAX. MEMORY (M WORDS)	.1 - 1	1 - 4	1 - 8	>64
WORD LENGTH (BITS)	4 - 32	16/32	48 - 64	64
TECHNOLOGY (LOGIC)	MOS (SOME BIPOLAR)	BIPOLAR	BIPOLAR ECL	ECL
ENVIRONMENT	SOME MIL-SPEC.	SOME MIL-SPEC & RUGGEDIZED	LAB	LAB
SIZE	CHIP(S)	MEDIUM	LARGE	LARGE
RELATIVE COST	VERY LOW	50 - 300K	<3M	5 - 15M

1.3.3.2.1 Supercomputers.

A supercomputer is "the cutting edge of computational computer technology at any instant in time." They are high-powered parallel processors with numerical processing throughput significantly greater than that of other general purpose computers. Supercomputers are designed mainly for executing programs with a high degree of parallelism (repetitive operations on different fields of data) and therefore require intricate programming to extract a fraction of their computing potential. Typical applications include weather system modeling, physical/mathematical sciences, nuclear fusion energy, weapon systems, and space sciences. These systems have undergone a slow evolution of experimentation with parallel architectures. Currently, the industry has settled on the "pipelined" vector type of architecture with future trends toward multiple processor architectures. (Note that array processors are covered in Section 1.3.2.)

At the end of 1983 there were only about 75 supercomputers in existence and most are located at national laboratories and universities. Increasingly, supercomputers are also becoming recognized in industry as a key to advancing engineering, manufacturing, and other commercial technologies. Two major manufacturers (CDC and CRAY Research) dominate the industry at the current time. However, new products have appeared or been announced from Denelcor (HEP), Fujitsu, Hitachi, and Nippon Electric Company, see Table 1.3.3-2.

The next significant increase in supercomputer performance will involve multiprocessor configurations and parallel structuring of the computations. However, the computing potential of parallel architectures will depend largely on the availability of algorithms and software which support efficient development and execution of such structures. There is a general lack of detailed knowledge of parallel problem structuring and parallel models of computation upon which to base development of application software. Significant gains can result from joint consideration of hardware, software, and applications in the implementation of parallel architectures.

Performance trends/projections for super computers are provided in Figure 1.3.3-1.

Table 1.3.3.-2

Super Computer & Super Computer Project Competition

Organization	Fujitsu	Hitachi	NEC	CRAY				CDC		Denelcor	Japan(MITI Project)	France (Min. de la Defense DRET projects)		
model	VP-200	S-810/20	SX-2	1M	X-MP	2	3	205	2XX	HEP-2		ISIS	MARIANNE	Not Named
announcement (or project start)	July 1982	Aug.1982	April 1983	Aug.1982	Aug.1982	none yet	none yet	June 1981	none yet	May 1983	(Jan.1981)	(1980)	(1980)	not yet started (will comb MARIANNE ISIS)
availability	Nov.1983	Nov.1983	March 1985	Sept. 1983	June 1983	mid 1984	1985/86	Feb. 1982	1986/87	1985/86	1989	1986/87	NA	
architecture[3]	vector IBM compatible	vector IBM compatible	vector	vector	vector multi-processor	vector multi-processor		vector	vector multi-processor	scalar[3]	vector multi-processor	vector	multi processor	vector multi processor
maximum performance (M FLOPS)[1]	500	630	1,300	250	630	1,000	NA	400	1,200-2,000	~~1,000~~ 4,000	10,000	200	NA	NA
maximum main memory size MB	256	256	256	32	32	NA	NA	64	256	~~2,000~~ 4,000	1,000	256	NA	NA
Technology • Logic (gate delay)	ECL (350 ps)	ECL (350 ps)	NA	ECL (551..7ns)	ECL (.5-1ns)	ECL	ECL GaAs	ECL (700 ps)	CMOS (0.5-1ns)	ECL ~~NA~~	JJ/GaAs (10-30 ps)	NA	NA	NA
• main memory	64K MOS static (55 ns)	16K MOS static (40 ns)	64K MOS static	16K MOS (70ns)	4K ECL (25ns)	MOS	MOS.	MOS (45 ns)	MOS	ECL/MOS	16K GaAs (10 ns)			
Input/Output • No.paths (total)	32	32	32	19	19	NA	NA	16	16	NA	NA	NA	NA	NA
• max data rate path (MB/sec)[2]	3	3	1.5	100	1,000			25	50-60					
• max aggregate data rate (MB/sec)[2]	900	1,100	1,350	550	1550	NA	NA	400	1,000	NA	1,500	1,200	NA	NA

[1] all 64 bit words
[1] M FLOPS = millions of floating point operations per second
[2] MB/Sec = millions of Bytes per second
[4] derived from 6-12 times Cray 1
[5] vector/options multiprocessor
NA : not available

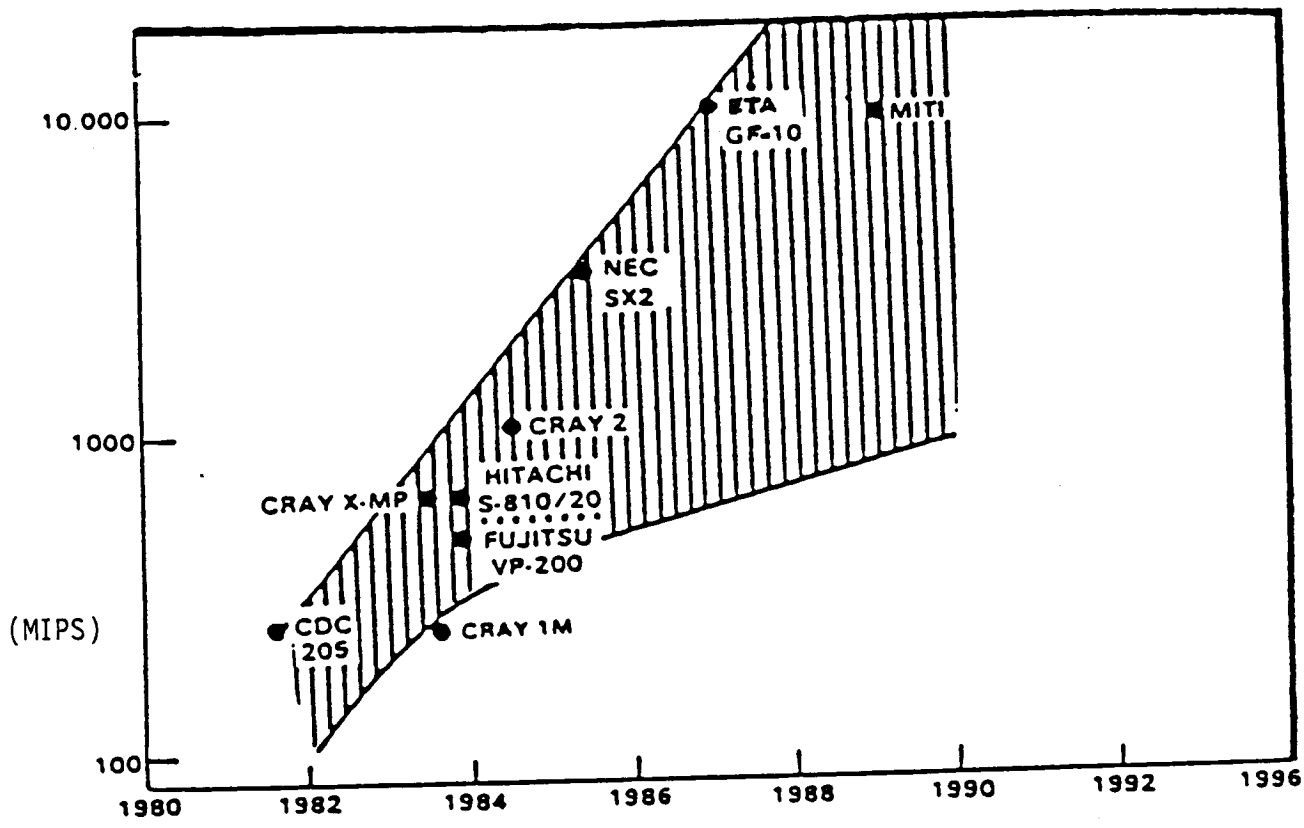


Figure 1.3.3-1

Supercomputer Performance (Pipeline)

(NASA Space Systems Technology Model)

1.3.3.2.2 Mainframes.

General purpose mainframes, contrasted to supercomputers, are better for data processing, where various computations and logical manipulations are performed on files, numbers and strings of characters. Mainframes have speeds within range of the supercomputers (in scalar mode), typically less than 20 MIPS, and have architectures that are more flexible variations of supercomputer architectures. While minicomputer and LAN technology have encroached on many previously mainframe dominated areas, centralized processing methods using large general purpose computers (batch, time sharing, and transaction processing) are likely to remain as cost-effective alternatives for some applications. This will include systems that require significant computational capability and/or the use of large complex data bases. Characteristics of representative computers in the mainframe class are provided in Table 1.3.3-3.

Mainframe computers can further be characterized by the following trends:

a. VLSI progress will drive size and cost down while performance continues to improve.

b. Systems are becoming more modular, with each module performing a single or small set of functions.

c. Modules will support or execute directly high-level language statements. Both interpreter and compiler versions of several languages are available.

d. They will contain multiple processors dedicated to specific system functions (i.e. I/O processors, file processor, application processors, special purpose adjunct processors, etc.)

1.3.3.2.3 Minicomputers.

In the realm of general purpose computers, the minicomputer has exhibited the most active growth profile. The major trend in minicomputers has been the proliferation of 32-bit architectures bordering on mainframe status, with the ability to support larger data bases and computer networking. Although most new minicomputers have the 32-bit architecture, others of similar performance

Table 1.3.3-3
MAIN-FRAME CHARACTERISTICS/COSTS

Vendor	IBM	NAS/Hitachi	CDC Cyber	Amdahl
Model	3081K	9080	180-860	5870
Processors/ Technology	2 Proc ECL	2 * ECL Arrays	2 ECL Arrays	2 ECL
Word Format	64	64	64	32
Throughput	10-14 MIPS	19-21 MIPS	22 MIPS	22-24 MIPS
INT Memory	96 Mbytes	64 Mbyte	128 Mbyte	128 Mbyte
Virtual Mem	2 Gbytes	2 Gbyte	2 Gbyte	4 Gbyte
Networking (Data Xfer)	3 Mbyte/sec per chan	3 Mbyte/sec per chan	3 Mbyte/sec per chan	3 Mbyte/sec
I/O Channels	24	48	24	32
Volume	375 ft^3	1160 ft^3	403 ft^3	1500 ft^3
Weight	22K lbs	25K lbs	10K lbs	7K lbs
Power	28KVA	50KVA	38KVA	39KVA
Cooling	Water	Air	Air	Air
Cost	$4-5M	$4.7M + Periph.	$4-5M	$3.5 - 4.0M

* Array Processor available to boost throughput to 28 MFLOPS

have multiple 16-bit processors (e.g. HP3000), 24-bit or 48-bit architectures (Harris). Minicomputers are unique in that they are not only expanding into the mainframe performance arena, but smaller systems are quickly finding a niche in the office automation environment. Improved communications and networking capabilities also permit the linking of many types of machines into powerful distributed environments.

The following characteristics further describe typical minicomputer trends.

a. Multiprogramming, multi-user, virtual memory type operating system environment.

b. Up to 16 Mbytes of main memory, Gbytes of virtual memory.

c. Support local/remote area network communications (DECNET, etc.).

d. Abundance of mainframe peripherals supported.

e. Floating point array processors (commercially available) can be added to enhance "number crunching" capability.

f. Many software packages available including development support environments, operating systems, data base management systems, and CAD/CAM capabilities.

g. Support real-time, on-line and interactive applications with software (OS) and interface hardware.

h. CPU based on bit-slice technology or proprietary circuits as opposed to microprocessor chip or chip set.

Characteristics/costs of representative high end products from the commercial market are listed in Table 1.3.3-4; performance trends/projections for minicomputers are provided in Figure 1.3.3-2.

Table 1.3.3-4
MINI-COMPUTER CHARACTERISTICS/COST

VENDOR	PERKIN ELMER	DATA GENERAL	DEC	H.P.	MODCOMP	PRIME
MODEL	3260	MV10000	VAX 8600	3000-SERIES 68	CLASSIC 32/85	9955
Throughput	3.4 MIPs	2.3 MIPs	4.4 MIPs	1.5 MIPs	2.4 MIPs	4.0 MIPs
Memory (Internal) Available	16M byte	21M byte	32M byte	8M byte	64M byte	16M bytes
Network Capability	40M byte/ sec	28M byte/ sec	77M bytes/ sec	20M byte/ sec	8M byte/ sec	9M byte/ sec
Technology	LSI TTL/MOS	VLSI AST	ELC Gate Arrays	ELC	VLSI TTL	ECL
Size	60 ft^3	55 ft^3	77 ft^3	34 ft^2	25 ft^3	60 ft^3
Weight	650 lbs	1189 lbs	1725 lbs	1100 lbs	600 lbs	1350 lbs
Power	5000 W	3400 W	6500 W Max	4400 W	2550 W	---
Cost	$300K - $350K	$400K	$570K	$220K	$190K	$450K

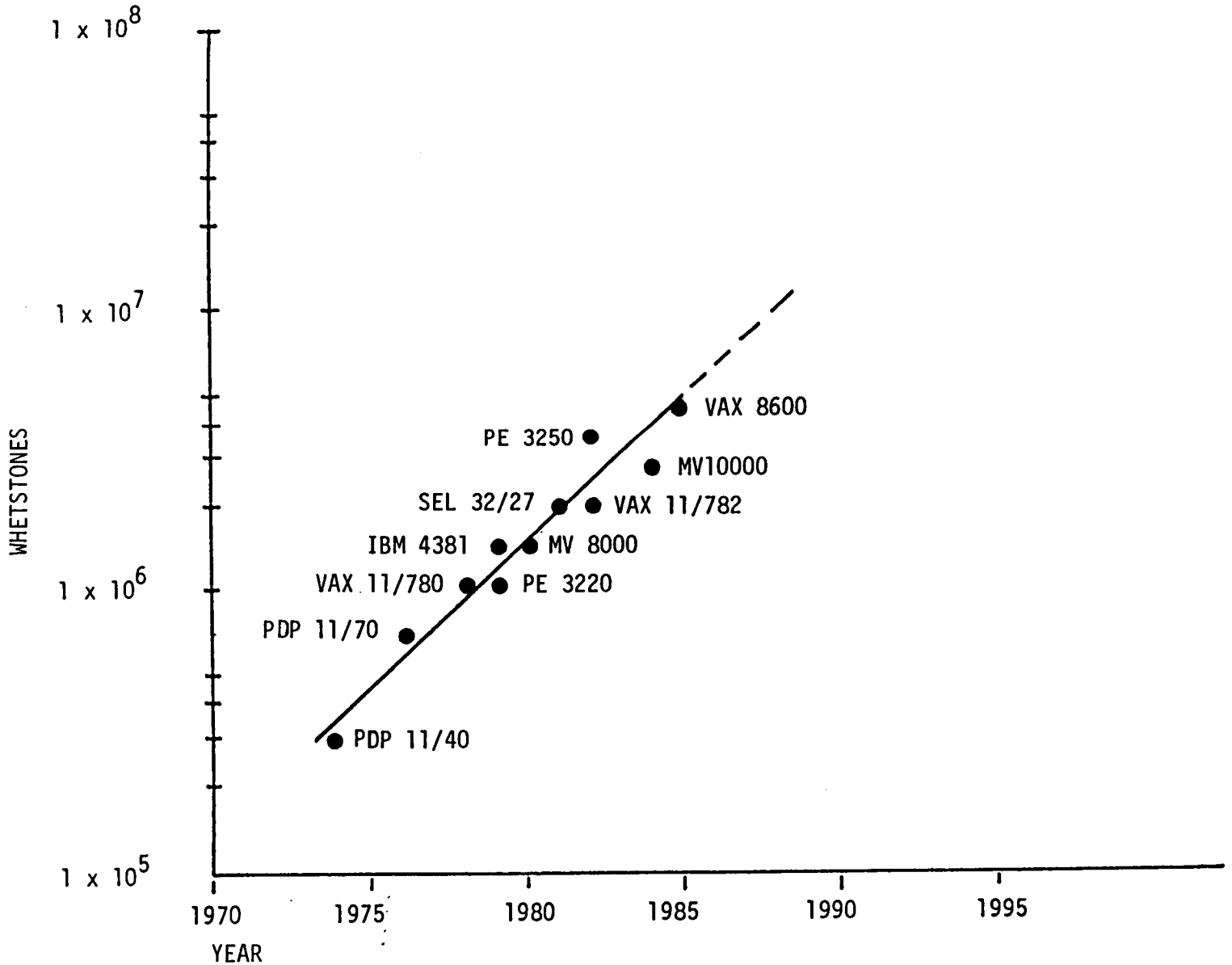


FIGURE 1.3.4-2 MINICOMPUTER PERFORMANCE TRENDS/PROJECTIONS

1.3.3.2.4 Microcomputers.

The distinction between minicomputers and microcomputers is becoming more obscure as improvements in architecture and VLSI technology expand microcomputer capabilities. Now there are systems and board-level microcomputers that rival minicomputers in capability, just as today's minicomputer rival early mainframes. Microcomputers use a microprocessor chip or chip set for their CPU. As a result, microcomputer capabilities will be driven by advances in microprocessor technology. For example, new chips will boost microcomputer performance to the 32-bit mini range at substantially lower cost. In addition, many of these systems are available with popular industry-standard software packages such as UNIX or PICK.

The Single Board Computer (SBC) is a modular microcomputer designed to be embedded in a larger system as the primary computational element or as an adjunct processor used to offload allocated functional responsibilities. The SBC's are powerful "building block" modules that are used for many specialized applications such as device controllers, message/network switching, data acquisition, automated testing, laboratory/industrial automation, work stations, etc. The SOA capability of an SBC is determined by the capability of the microprocesor, memory and I/O chips that can be mounted on standard circuit board. As 32-bit microprocessors and 256 Kbit memory chips become available, the SBC capability horizon has expanded well beyond the earlier "controller" type applications.

Microprocessor technology has also given rise to a variety of microcomputer systems that provide substantial capability at low cost. In general, this includes application oriented systems such as personal computers, word processors and business information systems where cost is the primary driver. It also includes systems that strive for cost-effective improvements in performance (throughput) and/or system reliability/maintainability through multiple processor architectures. While microprocessor technology now offers many mainframe features and capability, they cannot individually provide the computational power of the larger systems. This has resulted in new multiple microprocessor systems based on high-speed interconnection buses that offer

Table 1.3.3-5
MICRO-COMPUTER CHARACTERISTICS/COST

	H.P. 9000 (217)	STRATUS XA-600	CONVERGENT Mega-Frame
Processor	68000	68010 (Pair & Spare)	68010 (2)
Memory	8 M bytes	16 M bytes	7 M bytes
Performance	ν .5 MIPS	3 MIPS	.5 MIPS/Proc
Networking	1.3 Mbytes/sec per DMA	2.8 Mbytes/sec per channel	10 Mbits/sec
Volume	3 ft^3	26 ft^3	22 ft^3
Weight	18 lbs	600 lbs	520 lbs
Power	120 W	5KVA	2.7KVA
Cost	$9000	$325-350K	$50-60K

enhanced performance as well as fault-tolerance features (see Section 1.3.1). Such systems are often based on the SBC described above. Examples include Hewlett Packard's 9000 series supermicro (proprietary NMOS III technology), the Stratus Multiple Micro systems (68010 based fault tolerant systems), and Convergent Technology's Mega Frame (MC 68010 and Intel 186 chips with UNIX). Characteristics/cost of these units are provided in Table 1.3.3-5.

1.3.3.2.5 Microprocessors.

Microprocessors are single chip or chip set processors that have evolved rapidly from 4 and 8-bit "controllers" to today's 32-bit processors that provide many mainframe features. They are included here for completeness and as potential building blocks for future system "boxes" but are not, in themselves, considered to be an option. However, since their capabilities may significantly impact system level trends, we have characterized some of the more significant innovations that are likely to influence microprocessor-based system architectures. The implications of microprocessor technology on flight systems will be described in Section 1.3.4.

The SOA in microprocessor technology can best be illustrated by the new 32-bit generation including Motorola's MC68020, Zilog's Z80000, Intel's iAPX 386, Hewlett-Packard's HP FOCUS, Bell Laboratory's BELLMAC-32, and National Semiconductor's NS32032. Compared to their predecessors, they have more instructions, more registers, more extensive co-processor capability, higher operating speeds, and extended direct memory addressing. Table 1.3.3-6 provides a comparison of current 32-bit microprocessor characteristics. Other available features include the following:

- o Instruction cache memory
- o Virtual memory capability
- o Instructions to aid compilers and operating systems
- o On-chip multiple processors (floating point, memory management, etc.)
- o Coprocessor support and interfaces

Table 1.3.3-6 32-Bit Microprocessor Characteristics

Characteristics	HP FOCUS	NS32032	MC68020	Z80000	iAPX386
Chip Technology	NMOS III (Proprietary)	XMOS	HMOS	NMOS	HMOSIII
Power (Watts)	7	1	1.8	1	2.5
Clock Frequency (MHZ)	18	6 - 10	16	25	8
Data Word Size (Bits)	32/64	32	32	1/4/8/16/32	8/32
Instructions	230	86	65	180	111
Registers (Arithmetic/index/ General Purpose)	7/10/11	8/8/8	8/16/16	32/32/32	8/8/8
Direct Address (Bytes)	500M	16M	256M	32M	32M
DMA	Standard	Standard	Optional	Optional	Optional
First Delivery	1981	1983	1984	1984	1984
Second Sourcing	N/A	Yes	Yes	No	Yes

Of the new microprocessors described, the HP FOCUS and BELLMAC-32 are intended for use only in HP and Bell products and are not expected to be commercially available. Most of these microprocessors average about 150,000 transistors/ chip. The HP FOCUS is the exception with about 450,000 transistors.

The most innovative of the new microprocessor designs is Intel's iAPX 432. It is a 32-bit three-chip microprocessor set in which an object-oriented operating system is implemented in the chip circuitry. The 432 hardware, operating system and system programming language all support the concept of "objects" - variable length data structures (records, vectors, arrays, processes, etc.) that have a higher order than those typically implemented by traditional architectures. The following characterizes the key feature of this unique microprocessor.

- o A high-level instruction set designed to accommodate efficient translation of high level languages.
- o Operating system kernel in hardware (i.e. task scheduling, etc.)
- o Two-level multiprocessor bus structure.
- o Built-in security features to protect the integrity of objects and programs.
- o Virtual memory capability (segmentation).
- o Functional redundancy checking allows pairs of 432s to check one another and flag computational errors.
- o 200,000 instructions per second.
- o Ada orientation aimed at reducing programming costs.
- o Operating system features facilitate the sharing of workloads automatically and dynamically.

Intel announced intentions to provide a new cross-development system, Ada compilers, and development support under UNIX. Intel is expected to develop newer and faster revisions of the 432.

Application microprocessors are chips dedicated to specific applications that relieve the host CPU's processing burden and increase system throughput in computation - intensive applications. This is a rapidly emerging technology providing cost-effective alternatives for such complex applications as signal processing, voice synthesis, video display and modern processing. They are generally special-purpose architectures designed to efficiently execute specific algorithms such as FFTs, Linear Predictive Coding (LPC), etc. It is expected that application processors will continue to improve and be available for those applications that have high-quantity commercial market potential.

In response to Air Force initiatives to standardize computer instruction set architectures (ISA), many avionics suppliers are now producing MIL-STD-1750A computers (see Section 1.3.4). As a result, a number of suppliers are developing 1750-based microprocessors to further reduce size and power and enhance throughput/memory capability. Products expected to be available in the near-term include the following:

	Fairchild F9450	MDAC 281
Chip Technology	I^2L	CMOS-SOS
Throughput	700 KIPS	900 KIPS
Memory Addressing	64K direct, expendable to 1M word.	64K direct, expendable to 1 M word with MMU.
Floating Point on Chip	Yes	Yes
Packaging	Single Chip DIP	3-Chip on Thick Film Assembly.

These microprocessors are designed to meet military specifications and are inherently tolerant to relatively severe nuclear radiation environments. As these products become available they will be incorporated into the new flight computers. In addition, there is a new generation of 1750 microprocessors that will emerge from the VHSIC program and provide substantial improvements in processing speed (5-10 MIPS).

1.3.3.3 Projected Capabilities. It can be expected that the capabilities of all general purpose computer options will improve significantly in the future due to their broad commercial market. Even in the somewhat limited market occupied by supercomputers tremendous gains are likely to be achieved motivated by new commercial applications, Japanese initiatives, and national concerns for maintaining competitive leadership in high-technology computing. However, degree of improvement will not be uniform in all areas and will probably reflect the market expansion potential in each area. As shown in Table 1.3.3-7 microcomputers are expected to experience the highest growth rate and the mainframe market the lowest rate with a diminishing percentage of the total market.

The performance capabilities of all general purpose options will continue to increase with time, as depicted in Figure 1.3.3- , somewhat blurring option definitions. These performance increases are due to two mechanisms. First, these systems benefit through technology improvements, i.e., LSI/VLSI implementation of processors and memories. Secondly, vendors continue to expand downward, providing low cost versions of this high performance systems. New and more powerful microcomputers for example will soon dominate the low-end minicomputer market because of their significantly lower costs. Minicomputer vendors are now, in fact, incorporating software compatible microprocessors in many of their low-end products.

The trend in processing power has been roughly an order of magnitude increase as measured in MIPS every five years, based to a large extent on advancements in integrated circuit technologies. This trend will be difficult to maintain however since we are rapidly approaching the physical limit of gate speed in bi-polar and MOS technologies. A general move toward the high mobility of gallium arsenide is expected with additional techniques, i.e., LN_2 cooling to further increase mobility and implementation of innovative computer system architectures i.e., multiprocessor techniques. The resulting performances are, however, difficult to project over period exceeding a few years, particularly in the areas of supercomputers where only wild speculation can provide any estimates. The instructions per second which is now a poor measure of processing power will certainly be replaced or redefined to become

Table 1.3.3-7

MARKETING TRENDS

	1975	1980	1985	1990	1995
Microprocessors	9%	6%	20%	37%	55%
Word Processors (Personal Computers)	4%	6%	10%	13%	14%
Single Board Computers	3%	11%	13%	12%	9%
Minicomputers	10%	17%	21%	21%	17%
Mainframes	83%	60%	36%	17%	5%
Total Sales	$13B	$29B	$62B	$141B	$313B

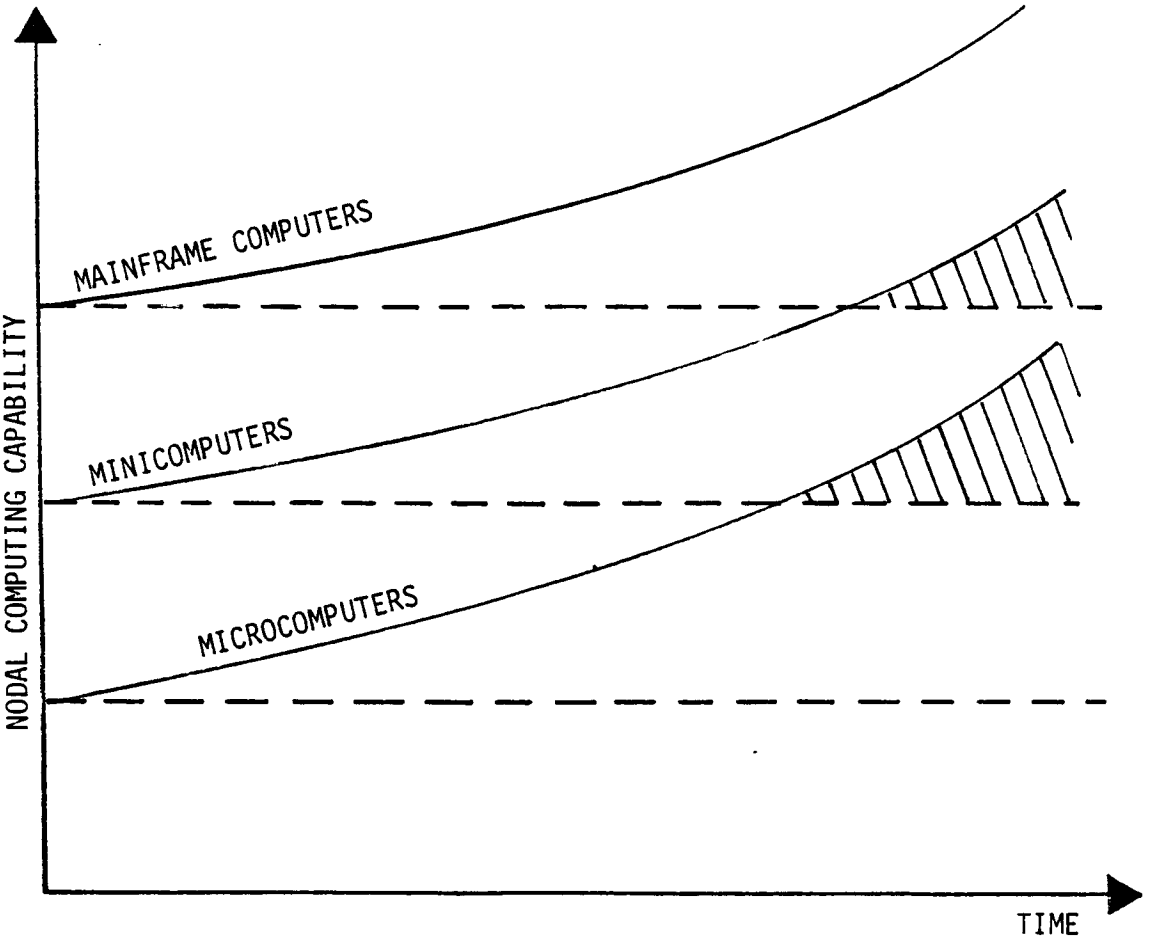


FIGURE 1.3.3-3

GROWTH OF NODAL ARCHITECTURE CAPABILITY

a more meaningful definition, particularly with the expected popularity of RISC architectures. Nevertheless it is of some interest to attempt to project where the more orderly micro's, mini's, and mainframes may reside on the performance scale at IOC. These categories, as shown in Figure 1.3.3-3 are expected to propagate upwards into the next performance region. Thus, the mainframes will cover a range of 100-500 MIPS, mini's will cover 50-150 MIPS and micro's will peak at 30-100 MIPS. The word format for these units will be 32 on the low end up to 64 bits and their internal memories will approach significant percentages of their virtual memory space.

1.3.4 Flight Computers

1.3.4.1 Description

This category includes options for computers that can be used on the SSP flight elements. While general purpose in nature, such computers will differ from those described in Section 1.3.3 due to the physical constraints (size, weight, power), operational environment, and reliability/availability/ maintainability requirements imposed by an orbiting Space Station or associated platforms. Historically, flight qualified computers have evolved into distinct classes based on the flight vehicle (satellite, missile, aircraft, etc.) and the operating environment (radiation, space/atmosphere, shock/vib.). These differences resulted in unique computer designs responsive to the specific vehicle/environment requirements: computers developed for space applications (satellites, deep space probes) tended to stress reliability, low power and small size, while sacrificing on-board performance capabilities. Aircraft computers, on the other hand, have abundant power, air cooling, moderate size constraints and adequate opportunity for maintenance resulting in relatively high-performance systems. These differences are further described in Table 1.3.4-1. The Space Station environmental requirements are actually a composite of those for space and aircraft. While the STS is a similar environment, there are still significant differences since Space Station computers need only be transported to orbit (not operational during launch) and they must tolerate long-term radiation effects (accumulative dose). Fortunately, many of the boundaries between

TABLE 1.3.4-1
FLIGHT COMPUTER REQUIREMENTS COMPARISON

REQUIREMENT	SPACE	AIRCRAFT	SPACE STATION
ENVIRONMENTAL	- HARD VACUUM (CONDUCTION COOLING) - LAUNCH S/V	- ENDOATMOSPHERIC (CONVECTION COOLING) - OP. S/V	- PRIMARILY IN PRES. VESSEL - TRANSPORTED TO ORBIT
PARTICLE RADIATION	- LONG TERM EFFECTS & RANDOM EVENTS - EXO. MOST STRESSING (EXCEPT EMP)	- ATM. ATTENUATION & MAN-RATED - SHORT TERM EFFECTS	- SPACE ENVIRONMENT
PHYSICAL CONSTRAINTS	- VERY LOW POWER (LOW PERFORMANCE) - LOW WEIGHT	- ABUNDANT POWER - MED. WEIGHT	- LOW POWER/WEIGHT
OPERATIONAL MODE	- REMOTELY OPERATED, HIGH AUTONOMOUS - NOT MAINTAINABLE	- MAN-IN-LOOP FOR OPERATION - PERIODIC MAINTENANCE	- LIMITED MAINTENANCE
PERFORMANCE	- LOW (HIGHLY CONSTRAINED BY WEIGHT/POWER REQ'MTS	- HIGHER AND OFTEN DISTRIBUTED (FEDERATED)	- HIGH
RELIABILITY	- HIGH, NO MAINTENANCE (REMOTELY OPERATED) - LITTLE HAZARD TO LIFE	- HIGH FOR CRITICAL FUNCTIONS (HUMAN SAFETY) - LOW FOR OTHERS (HUMAN INTERVENTION AS BACKUP)	- HYBRID
DEVELOPMENT SPAN	- 6-12 YEARS	- < 3 YEARS	- TBD

environment-specific flight applications are beginning to diminish and technology advances are changing many of the design trade-off decisions previously faced. As a result, new flight computer products are emerging that are designed to be applicable for both military aircraft and space applications.

One of the more significant drivers for this category is the requirement for operation in the space radiation environment over long periods of time. In the Space Station environment, it is necessary to consider the long-term degradation due to total dose of ionizing radiation, random logic upset due to cosmic ray and solar alpha incidence, and fluence pulse effects. Currently, qualified radiation hardened components are typically a limited variety of SSI technology, available in limited quantities, are very expensive, and require long lead times. In addition, the traditional radiation hardened memories have been the slower, heavier and larger varieties, i.e., core, plated wire, etc. Consequently, radiation hardened computers have suffered significant size, weight and performance penalties compared to their 'non-rad' counterparts. Qualification of LSI and VLSI components and memories will alleviate much of this problem.

In addition to operating in the Space Station environment, an on-board computer must also provide sufficient resources (throughput/memory) and networking capability to support distributed DMS concepts and future growth paths. While individual computer resource requirements are not defined, it is clear that high MIPS/cost and MIPS/size ratios are desirable and that higher network nodal capabilities will ease network design, minimize potential bottlenecks, and facilitate future growth. High-speed flexible networking capability is generally lacking in this category with MIL-STD-1553 (1 Mbit serial bus) as the prevailing standard. Efforts are currently in progress to develop a new MIL-STD. bus (network) with enhanced speed and flexibility.

The options in this category include the following:

- Mil.-standard ISA flight computers
- Mil.-spec. versions of commercial minicomputers
- NASA standard spacecraft computers
- New Space Station standard computer development

1.3.4.2 Option Characterization

1.3.4.2.1 MIL-STD ISA Flight Computers

Standard instruction set architectures have been used by the military for many years and have been supported by numerous commercial sources. In recent years, the Air Force has established the MIL-STD-1750A as their standard flight computer ISA. Due to the relatively large quantity marketplace that is emerging for Air Force applications, this initiative has been well-supported by the avionics industry. Nearly all flight computer suppliers now offer, or are developing, a 1750 flight computer. Most of these computers are implemented with today's bit-slice technology. However, new 1750 chips are currently being developed by Fairchild, MDAC and Mikros, as described in Section 1.3.3, and more powerful chips will emerge from the VHSIC program (Westinghouse and Texas Instruments). Because of this broad industry acceptance and the VHSIC emphasis, the 1750 has become the de facto standard for many non-Air Force applications as well. While actual experience with 1750 computers is still somewhat limited, the following potential benefits have been identified:

- o A growing base of support software, both GFE and vendor supplied.
- o Enforced portability of software including any machine language code (i.e. operating systems, etc.)
- o A good technology growth path supported by DoD, (i.e. VHSIC and DARPA program will focus on current military standards).
- o Many supplier sources to choose from.

However, it has also been observed that the same results can be achieved with the use of a standard high order language (HOL) such as Ada while allowing the introduction of more powerful and modern architectures. It has been argued that raising the level of standardization (i.e. from machine language to HOL) will further broaden the support software base well beyond the avionics community support.

The following characteristics are typical of today's MIL-STD-1750 computers

- o 16-bit architecture
- o Throughput = .5-1.0 MIPS (DAIS mix)
- o Memory addressing up to 1 Mword with memory management units

- o 32 and 48-bit floating point arithmetic
- o 16 GP registers
- o 16 level priority interrupts
- o Qualified To MIL-E-5400
- o Built-in timers and test capability
- o Logic Technology = Mostly Bipolar with some CMOS
- o Radiation tolerant
- o Typical size and power
  - 1 Ft^3 (ATR Mounted)
  - 50 Lbs.
  - <500 Watts (depending on memory type)
- o Cost <500K$
- o Available HOL's include Pascal and JOVIAL. Ada compiler in process

Table 1.3.4-2 from Defense Electronics, 1982, "Weighing 5000.5X", describes ongoing activities pursuing MIL-STD-1750.

1.3.4.2.2 MIL-Spec Versions of Commercial Minicomputers

A number of MIL-Spec. computers have been developed by avionics suppliers under licensing agreements with commercial minicomputer manufacturers. Noteable in this area are Norden (licensed to DEC) and Rolm (licensed to Data General). These products have been used in a variety of military applications including many flight programs. With the advent of the 16-bit Air Force standard (1750), the use of these current products in future flight applications will be limited. However, new 32-bit products have recently been introduced (proposed) that will (could) be qualified to airborne specifications (MIL-E-5400). This provides a 32-bit alternative to 1750 for some flight applications since a 32-bit standard (i.e. MIL-STD-1862) is not currently implemented. Table 1.3.4-3 characterizes these 32-bit mil-spec. minicomputers. In addition, a few vendors are producing "ruggedized" versions of minicomputers that don't meet full mil.-spec. requirements. Norden, for example has had experience ruggedizing DEC products with a final cost of approximately 2x the original product cost. The only other 32-bit flight computer currently available is the IBM AP101 series that has "dual" architecture capability, IBM 32-bit and MIL-STD-1750.

TABLE 1.3.4-2

Vendors and Agencies Actively Pursuing MIL-STD-1750A

VENDORS	VERSIONS
Control Data Corp.	Has 1-card change to convert Navy's AN/AYK-14 to MIL-STD-1750A -Up and running; was due to be verified by the Air Force in August 1982
Delco	1/2 ATR box (M362F), 32k words, Fire Control Computer for F-16 Multinational Staged Improvement Program (MSIP) -Not verified by the Air Force as meeting the standard -Has delivered flight hardware as sub-contractor to General Dynamics Repackaged version, 64k words, 940 kops, for LANTIRN -Verified as meeting the standard -Has delivered flight hardware as sub-contractor to Martin Marietta Updated version Magic 372, 64k words -Delivered the same as on the LANTIRN -Verified as meeting the standard 1 ATR box, 128k words is planned
Fairchild Semiconductor	Won competition to develop MIL-STD-1750A chip set for General Dynamics/Ft. Worth -To be used in F-16 MISP -Available in mid-1983 on a single card
General Electric	GE/Utica uses two MIL-STD-1750A computers in F-5G II radar -In cooperation with Tracor GE/Binghampton is developing company-funded MIL-STD-1750A
Honeywell	Subcontracted to Fairchild to develop architecture implementation for a MIL-STD-1750A chip set
Hughes Aircraft	Building company-funded MIL-STD-1750A radar processor -Intended for F-15 MSIP
IBM	Two working airborne versions (CP-2EX and AP-101E) -Both verified by the Air Force as meeting the standard Won competition for 1000 MIL-STD-1750A computers for the B-1B -Computers capable of both AP101D and 1750A ISAs -Subcontractor to Boeing
McDonnell-Douglas	Delivered first militarized airborne MIL-STD-1750 computer and support software -MIL-STD-1750A brassboard up and running Working on a radiation hard and non-hard version, with 1750A chip set
Mikros	Accepting orders for MKS1750, a fully-militarized, SOS/CMOS radiation-hardened, single-card MIL-STD-1750A computer -Board measures 20 sq. in., consumes 2W -200 kops with DAIS instruction mix -Available 4Q CY 82 Also sells MIL-STD-1750A software development station -Available 3Q CY 82
Rolm	Bidding a 1/2 ATR size MIL-STD-1750A computer on AFSATCOM Terminal Upgrade program
Singer Kearfott	Won Competition for F-111 Digital Update Weapons/Nav Computer -Will install in F-111D, F-111F, FB-111A -Brassboard up and running, based on SK-3121 machine
Sperry Univac	AN/AYK-15A airborne computer (Univac designation-U1625) updated to MIL-STD-1750A -Up and running in Air Force Avionics Laboratory Delivering MIL-STD-1750A computers to Sperry Systems for Modular Automatic Test Equipment (MATE) (Univac designation-U1630) contract -512k word minis interfacing with disk/mag. tape/line printer
Teledyne	Won competition for F-5G II mission computer with MIL-STD-1750A -1/2 ATR size, 17 pounds, 700 kops with DAIS mix, available now -Validated by the Air Force as meeting the standard -Cost: $43K each, with Reliability Improvement Warranty (RIW) of 5000 operating hours; but, cost is variable by quantity, data, and other considerations Also markets TDY-750 SDS software development system -Includes floppy and hard discs and fine printer -Available 4 months ARO
Texas Instruments	Building MIL-STD-1750A computer in VHSIC program -For Army application: fire-and-forget missile
Tracor	Built microprocessor MIL-STD-1750A for GE's F-5G II radar Developed MIL-STD-1750A rad-hardened chip set with RCA
Westinghouse	Uses two MIL-STD-1750A computers in enhanced improved AN/APG-66 radar -Will be installed in F-16 a/d B-1B (MSIP) Uses MIL-STD-1750 in Army's SGT YORK Division Air Defense System, as subcontractor to Ford Aerospace Building MIL-STD-1750A in CMOS for VHSIC program

TABLE 1.3.4-3
MIL.-SPEC. 32-BIT MINICOMPUTER CHARACTERISTICS

CHARACTERISTIC	NORDEN MIL-VAX-1	NORDEN MIL-VAX-2	ROLM HAWK-32	TMI (PROPOSED)
Instruction Set	VAX	VAX	D.G. ECLIPSE	MOD COMP 32/85
Throughput (Whetstones)	1 x 10^6	1.5 X 10^6	1.5 x 10^6	6 MIPs
Memory (internal)	4 M Bytes	8 M Bytes	8 M Bytes	8 M Bytes
Virtual Address Space	4 G Byte	4 G Byte	4 Gigabytes	4 G Words
Technology	AST Gate Array	CMOS 10K gate array	VLSI CMOS gate array	VLSI CMOS/SOS Logic Arrays
Volume	2 ft^3	.09 ft^3	1.4 ft^3	
Weight	170 lbs.	65 lbs.	90 lbs.	54 lbs.
Power	1200	400	400 watts	309 w
Networking Capability	UNI-Bus 1.5 Mbyte/sec	Q-Bus 1.5 Mbyte/sec	MCA Bus 4 Mbytes/sec	160 M Byte/sec
Available HOL	ADA, Pascal, FORTRAN	ADA, Pascal, FORTRAN	ADA, Pascal, FORTRAN	Pascal, FORTRAN
SW Development Environment	Good	Good	Good	Good
Cost	$400-450K	$200-250K	350K$	$265K **
Availability Date	Now	Mid '86	End of 1984	+ 3 yrs.

** Requires estimated $12.7M for development.

Significant advantages associated with this class of computers includes the following:

- o Extensive base of support software and tools already exist for minicomputers.
- o Software development can be accomplished on compatible commercial minicomputers.
- o New HOL's (i.e. ADA) and operating systems initially targeted to minicomputers.
- o Track evolution path of minicomputers.

1.3.4.2.3 NASA Standard Spacecraft Computers

This option consists of computers designed specifically to meet the stressing space-related requirements of past and current NASA missions. Included are computers developed separately through NASA-funded projects as well as some commercially developed computers that have been used in limited applications. The historical evolution of these spacecraft computers was heavily influenced by the overriding concern for system reliability and the need for extensive space qualification testing prior to flight. This influence led to a reliance on relatively simple, highly reliable, on-board systems and the allocation of more complex functions to maintainable ground complexes. The normal spacecraft severe size and power constraints further reinforced this approach, resulting in relatively low performance computers that significantly lag behind the state-of-the-art for both commercial and military computer technology. The capabilities of representative spacecraft computers currently under development, recently flown, or planned for future NASA missions are summarized in Table 1.3.4-4. These computers have been primarily designed for fault tolerant configurations to be used in long-term, unmanned spacecraft applications. A noteable exception is the IBM AP-101 series general purpose computer (GPC) used on-board the shuttle is a quad-redundant configuration. The GPC can be characterized as follows:

- o CPU - TTL, MSI/LSI
- o Memory - 65K, Core
- o Word Format - 32 bit
- o Floating Point Arithmetic
- o Throughput 450 KOPS
- o Weight - 59 lbs
- o Power - 350W
- o Cost - $500K

1.3.4.2.4 New Space Station Standard Computer Development

While the previous section described the option of using existing or in-development NASA standard spacecraft computers, this section describes the option to develop a new NASA standard computer specifically for the needs of space station. Due to the high costs associated with the initial development of a new computer, extensive qualification testing and low-quantity production, such an option is only likely if cost-effective alternatives do

Table 1.3.4-4

Spacecraft Computer Characteristics

COMPANY MODEL NO.	IBM NSSC-I	ITEK APPLIED TECHNOLOGY ATAC - 16MS	IBM NSSC-II	LITTON 4516 E (OBC)
FAULT-TOLERANT CONFIGURATION	2 CPUs 2 STINTS SHARED MEMORY	2 SINGLE STRING CPUs WITH CROSS-STRAPPED MEM, PS, I/O	2 SINGLE STRING CPUs EACH WITH FTM	2 SINGLE STRING CPUs WITH SHARED FTM
STATUS • DEVELOPMENT • SPACE QUAL • SPACE EXPERIENCE	QUALIFIED SMM-1980 ST-1982	QUAL MAY/JUNE 1981 (COMPANY FUNDED) GALILEO-1984	QUAL COMPLETE FOR NMOS STATIC RAM SEVERAL UNITS FAB/DELIVERED	UNDER CONTRACT (CLASSIFIED PROGRAM) QUAL IN LATE 1981. RGC AMeRV 1980. SPACE SEXTANT QUAL COMPLETE
WORD LENGTH • FIXED POINT (S/D) • FLOAT. POINT (E/M)	18 NO FLOAT PT	16/32 8/24 (?)	16/32/64 8/24 (FW)	16/32 8/24 (FW)
MEMORY • MAX ADDRESS • PART TYPE • ERROR CORR CODE	64 K x 18 CORE NONE	128 K x 16 CMOS (H5604) 6 BIT HAMMING	>198 KBYTES 16K x 1 DYNAMIC 6 BIT HAMMING	256 K x 16 CMOS (H6504) 6 BIT HAMMING
PHYSICALS • CONFIGURATION • POWER/WT	• 2 CPUs, 1 ON 16 K MEMORY (MAX) 8 K ON 31 W/17.4 LB	1 ATAC-16MS WITH 64 K x 22 MEM (CHASSIS CONFIGURED FOR DUAL PROCESSORS AND MORE MEMORY) 63 W/25 LB 28 VDC IN	1 OF 2 NSSC-IIs ON, EACH WITH 196 K x 22 FTM 130W/58 LB	1 OF 2 LC4516s ON 128 K x 22 FTM WITH 32 K OFF BATTERY BACKUP 77 W/26 LB 29 VDC IN
THROUGHPUT • FIXED POINT • FLOAT POINT	FIXED PT ADD-5 μSEC MUL-44 μSEC DIV-75 μSEC NO FLOAT PT	THROUGHPUT GIBSON MIX WITH FLOAT. PT 375-400 KIPS (MACHINE SLOWER THAN LITERATURE DUE TO DELAYS IN FTM)	THROUGHPUT 16 BIT FIXED PT 330 KIPS 32 BIT FIXED PT 185 KIPS FLOAT PT 40 KIPS FLOAT. PT ADD-NA MUL-38 μSEC + N DIV-56 μSEC + N	THROUGHPUT 16-BIT FIXED POINT GIBSON MIX-539 KIPS FIXED PT (50% R-R) ADD-1.6 μSEC MUL-5.2 μSEC FLOAT. PT ADD-10 + N μSEC MUL-23 + N μSEC DIV-32 + N μSEC
HIGH-ORDER LANGUAGE (APPLICATION PROGRAMS)	NONE	HAL-S FORTRAN BASIC	HAL-S FORTRAN	FORTRAN
PACKAGING AND PART TYPES	HYBRID, 40-PIN FLAT PACKS, 27 CHIP TYPES, 69 FLAT PACKS TOTAL TIL	FLAT PACKS ON ML PWB TTL, CMOS	HYBRID, 5 CHIPS PER CAN MAX, 20 DIFFERENT CHIP TYPES, 96 TOTAL CHIPS IN CPU, 18 DIFFERENT HYBRID TYPES TTL, NMOS	FLAT PACKS AND LEADLESS CARRIERS, RAM IC, ON ML PWB, ML BACKPLANE, 75 DIFFERENT IC TYPES TTL, CMOS
RELIABILITY (R) • FAULT-TOLERANT CONFIG • 2 YR (1752 HR) • UNPOWERED STANDBY SPARING ($\lambda_{UP} = 0.1\ \lambda_P$)	 0.96	CLASS B FAIL. RATES 64 K WORDS ACTIVE 8 K STANDBY CROSS-STRAPPED 0.999	 0.9987	CLASS B FAIL. RATES 96 K WORDS ACTIVE 32 K STANDBY 0.9804

NO FTM – FAULT TOLERANT MEMORY
FW – FIRMWARE
NA – NOT AVAILABLE
S/D – SINGLE/DOUBLE FIXED PT WORD
E/M – EXPONENT/MANTISSA FLOATING POINT WORD
N – NORMALIZE ML PWB MULTILAYER PRINTED BOARD

Table 1.3.4-4 Cont'd

Spacecraft Computer Characteristics

COMPANY MODEL NO.	NORTH AMERICAN ROCKWELL DF-224	RAYTHEON FAULT-TOLERANT SPACECRAFT COMPUTER (FTSC)	TELEDYNE MECA-43	CONTROL DATA CDC 469
FAULT-TOLERANT CONFIGURATION	STANDBY (UNPOWERED) MODULAR SPARING TMR BUSES AND CONTROL LINES	4 CPUs STANDBY MODULE SPARING AS IN DF-224	DUAL CPUs WITH CROSS-STRAPPED POWER CONVERTER, MEMORY, I/O	2 SINGLE-STRING CPUs
STATUS • DEVELOPMENT • SPACE QUAL • SPACE EXPERIENCE	QUAL COMPLETE CLASSIFIED PROGRAMS IN PRODUCTION IN SPACE	SAMSO ADVANCED DEV BREADBOARD/BRASS-BOARD STAGE	REPACKAGED AIRCRAFT COMPUTER, FIRST 2 SPACE CONTRACTS IN PROCUREMENT STAGE (CLASSIFIED PROGRAMS). USES EXISTING HYBRIDS	USED IN SEVERAL SPACE PROGRAMS OVER PAST YEARS (E.G., HEAO, CLASSIFIED PROGRAMS)
WORD LENGTH • FIXED PT (S/O) • FLOAT. PT (E/M)	24 NO FLOAT. PT	32 8/24	16/32 8/24	16/32 NO FLOAT. PT
MEMORY • MAX ADDRESS • PART TYPE • ERROR CORR CODE	64 K X 24 PLATED WIRE PARITY	96 K x 32 CMOS, CMOS-SOS	NA	32 K x 16 PLATED WIRE, CMOS, PARITY
PHYSICALS • CONFIG • QUAL OR IN DEVELOPMENT • POWER/WT	3 CPUs, 1 ON, 48 K x 24 MEMORY (MAX) 8 K ON, 3 IOUs, 1 ON 100 W/100 LB	1 CPU OPERATING 3 IN STANDBY 62 K x 32 MEMORY 60W/50-80 LB	1 CPU OPERATING 1 OFF (STANDBY) 8 K x 22 ON 56 K x 22 OFF 74W/49 LB	1 469 OPERATING 1 469 STANDBY 20W/20 LB
THROUGHPUT • FIXED PT • FLOAT. PT	THROUGHPUT (24 BITS) FIXED PT MIX < 350 KIPS ADD-1.8 μSEC MUL-8.0 μSEC DIV-23.4 μSEC	FIXED PT ADD-5.4 μSEC MUL-11 μSEC FLOAT. PT NA	THROUGHPUT GIBSON MIX-390 KIPS FIXED PT ADD-1.6 μSEC MUL-3.93 μSEC FLOAT PT ADD-7.08 - N μSEC MUL-11.32 - N μSEC DIV-17.92 - N μSEC	FIXED PT ADD 4.0 μSEC MULT 10.4 μSEC FLOAT. PT NOT IMPLEMENT IMPLEMENTED
HIGH ORDER LANGUAGE	NONE	NONE	JOVIAL	NONE
PACKAGING AND PART TYPES	16 CUSTOM PMOS LSI 6 HYBRIDS DIODE ARRAY PLATE WIRE MEM ML PWB ASSY	CMOS-SOS LSI TO BE DEVELOPED	72 HYBRIDS, 13 TYPES, ON ML PWB, LARGE HYBRIDS, > 30 CHIPS/HYBRID	CUSTOM PMOS LSI
RELIABILITY (R) • FAULT TOLERANT CONFIG • 2 YRS (1752 HR) • UNPOWERED STANDBY SPARING (λ_{UP} = 0.1 λ_P)	24 K WORDS ACTIVE 3 x 8 K STANDBY 2 STANDBY CPUs 2 IOUs STANDBY 0.97	0.95 FOR SYS CONTRACTURAL REQUIREMENT	POWER CONV, MEM, CPU, CROSS-STRAPPED 80 K ACTIVE, 8 K STANDBY 0.997	NA
MISCELLANEOUS • CLASS S/CLASS A PARTS PROGRAM EXPERIENCE • DERATING ELECT. ANALYSIS THERM. ANALYSIS	GOOD (MINUTEMAN) COMPLETE	NA INCOMPLETE	GOOD NA	GOOD (HEAO) -

not emerge from the commercial/military marketplaces. However, there are potential advantages for tailoring a new computer design to the specific application requirements of space station including the opportunity to "build-in" fault tolerance features, standard networking capabilities, and other performance enhancements. While such functions can be implemented in software, there are performance payoffs for incorporating these capabilities in hardware/firmware.

There are actually several alternative approaches to developing a new space station standard computer (SSSC) that can be reasonably considered. This includes the following:

1. Use commercially available μP chips.
2. Develop new custom chip set (VLSI)
3. Use bit-slice technology to emulate commercial processors.

A qualitative assessment of these approaches is summarized in Table 1.3.4-5.

Table 1.3.4-5
NEW COMPUTER DEVELOPMENT SUMMARY

	USE AVAILABLE μP CHIPS	DEVELOP NEW CHIP SET	BIT-SLICE EMULATION
o Performance Enhancement Potential	Low	High	Moderate
o Potential Size/Power	Good	Good	Moderate
o Potential Rad-Hardness	Currently very limited but potential improvement	Very Good	Good
o Growth Potential	Good. New incompatible chips can be replacements	Poor. New development required	Code Enhancements can be incorporated
o Risk Assessment			
- Performance	Low	Moderate	Low
- Cost	Low	High	Moderate
- Schedule	Low (If qualified)	High	Moderate
o Cost Assessment			
- Recurring	Low	High	Moderate
- Non-Recurring	Low	High	Moderate
- Support SW	Depends on μP	Depends on ISA	Depends on target
- Quantity Production	Low	High	Low

Approach 1 becomes increasingly attractive as more capabilities are provided on-chip. As new μP chips begin to look more like larger computer systems, new μP-based computers are becoming more cost-effective to design and develop and offer vast potential for reduced size and power. However, since these devices still have relatively low computational power, more reliance must be placed on concurrent architecture technology. This can introduce potential design complexity related to processor interconnection efficiency, data queueing, operating system overhead, and resource contention that must be addressed within the context of the Space Station application.

The major problem with this approach is the general lack of devices that are (or can be) qualified for a long-term space environment. Most currently available processors are based on NMOS technology and lack sufficient radiation - hardness. Bipolar products offer good immunity to total dose radiation, where MOS products have traditionally shown poor total dose characteristics to gamma radiation. As a result, current space/military applications using microprocessors rely heavily on bipolar devices such as TI's 9900 and on some available CMOS devices. However, recent studies on various INTEL products indicate that as circuit densities increase, improvement in the total dose characteristics becomes considerable. Where earlier NMOS products showed degradation in the low kilorad range, higher density HMOS II circuits have demonstrated performance without failure at levels exceeding 50 krads. However, the best near-term potential is probably offered by the emergence of new commercial products based on low-power CMOS technology. The availability of new SOA microprocessors that can be qualified to the space radiation environment is a major uncertainty due to the lack of test data on advanced products. Perhaps the most cost-effective source of rad-hard microprocessors will be those developed specifically for the military such as the Fairchild, MDAC, TI, and Westinghouse MIL-STD-1750 chips described in Section 1.3.3.

Approach 2 is probably warranted only if the development costs can be substantially shared with other government initiatives (i.e. VHSIC, DARPA, etc.) and if significant gains in performance can be achieved by incorporating advanced technologies at the chip level. This might include the use of new circuit technology (i.e. GaAs, CMOS/SOS, etc.) or innovative architectural concepts. While the Air Force currently has projects under way to develop

space-qualified GPU chip sets (RCA EPIC, Sandia, etc.), the extent to which NASA could influence these designs for space station specific requirements is not clear.

Approach 3 uses available bit-slice technology to emulate a target processor's instruction set, a technique commonly employed by military avionics suppliers as well as many commercial manufacturers. Typically, bit-slice devices can be selected that are high-speed and inherently rad-hard (bipolar, CMOS/SOS). By emulating a specific target processor, a new computer can capture the existing support software base and minimize support software development costs.

1.3.4.3 Projected Capabilities

Because of the relatively stringent requirements imposed by a space station environment and the limited production quantities involved, it is likely that future space station computer capabilities will be provided either by commercial and/or DoD initiatives to support the growing military market or as the result of NASA-sponsored development efforts (or some combination thereof). The projected capabilities described here will focus on the more visible trends in current and future military flight computers as summarized below:

a. An increased military presence in space will drive high-performance, small form factor, rad.-hard computer technology.
b. DoD-sponsored programs (i.e. VHSIC, DARPA, etc.) will have a significant "fallout" beneficial to space station computing needs as participants incorporate technology into commercial products. Also a direct product benefit if mil-standards are adopted, (i.e. MIL-STD-1750, etc.).
c. Because of a and b above, and other technology advances, commercial products will emerge based on common modules that are adaptable to both NASA and DoD applications. This trend is already apparent in many of the newer flight computers (e.g. TDY-750, AP101F, etc.)

Examples of applicable computer systems currently being developed by DoD contractors include Honeywell's Advanced Distributed Onboard Processor (ADOP) and CDC's Military Computer Modules (MCM). Both of these programs are

striving to provide high performance capabilities in a distributed networking environment, and both are being designed to incorporate evolving VHSIC technology.

Other examples of advanced military computer development includes VHSIC efforts by TI and Westinghouse as well as other contractor-funded efforts (e.g. MDAC 281, etc.)

Figure 1.3.4-1 shows the current and projected throughput capability million machine instruction per second (MIPS) for military flight computers. It is expected that any new computer development sponsored by NASA should be able to achieve similar results. Clearly, the VHSIC program will have a significant impact over the next ten years by improving speed and radiation tolerance while reducing size and power. In addition, GaAs will offer significant potential for future space applications due to its higher electron mobility and inherent radiation tolerance. New GaAs products are beginning to emerge and will become competitive in some areas in the late 80's. Development of more sophisticated circuits is under way in Japan and the U.S. (DARPA) and could result in mature GP computer modules in the early 1990's.

Early definitions of the Space Station architectures have generally identified a 'standard data processor' for use as a standard/common unit for replicated use by the Station sub-systems. It is of some benefit to project the potential characteristics of this processor as it currently exists and as projected to IOC and growth periods. This projection is shown in Table 1.3.4-6. As shown, the current generic performance is 0.5 - 1.0 MIPS which is expected to increase to the 100 - 200 MIPS range by 1997. As indicated earlier, the instructions per second measure is currently not a totally valid indication of performance particularly with the introduction of the reduced functionality instruction set (RISC) architectures however this projection is provided as a 'normalized' measure of performance. The memory and I/O capabilities listed are not considered to be any technology limit but rather are presented as capacities that complement the functional performance of the Subsystem Data Processor (SDP).

C-3

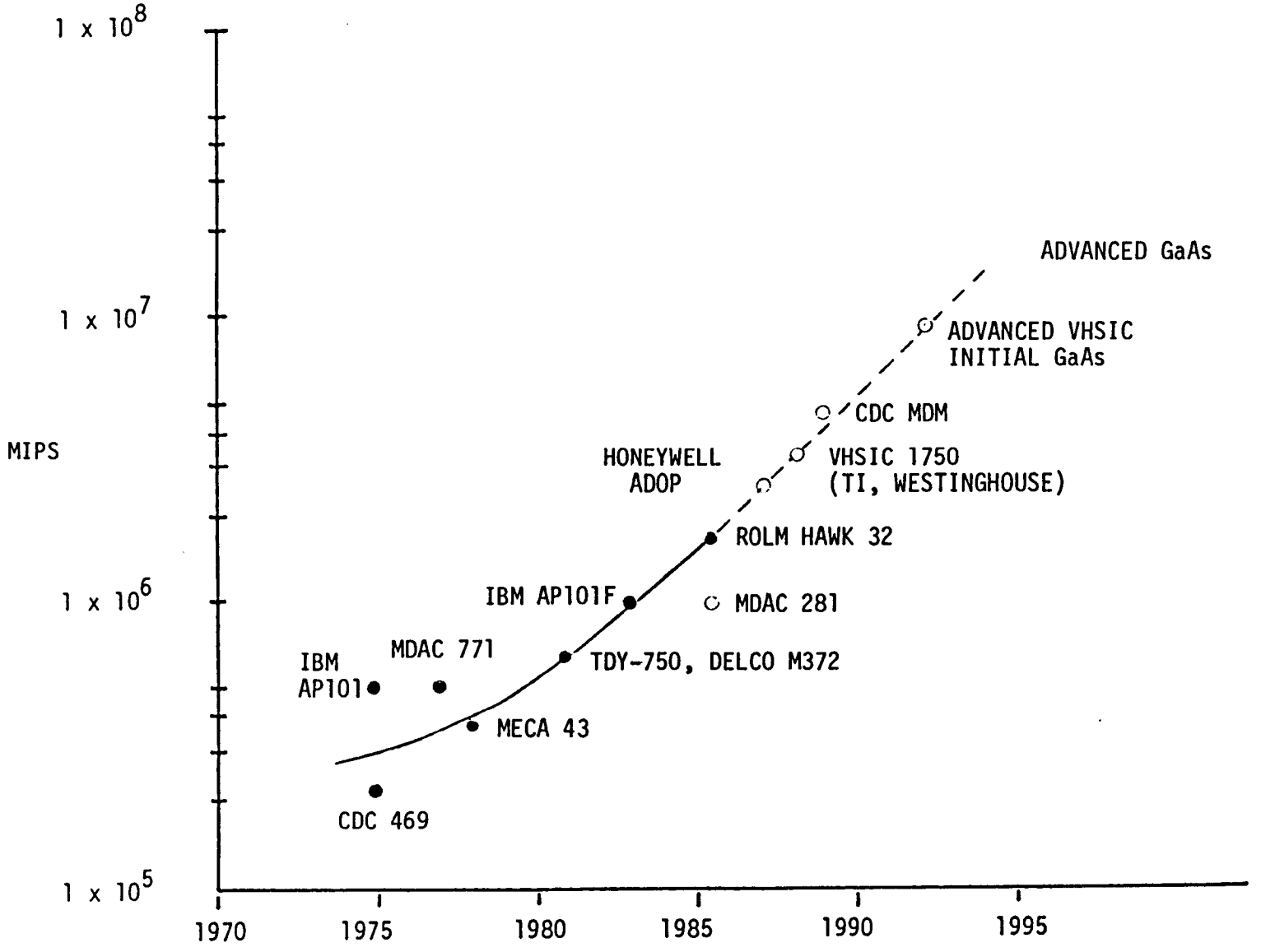


FIGURE 1.3.4-1 - MILITARY FLIGHT COMPUTER PERFORMANCE TRENDS/PROJECTIONS

Table 1.3.4-6
Generic Flight Computer Projections

	1985	1987-1989	1992	1997
Architecture	Uniprocessor 1750A	Main & Co-Processor	Main & Co-Processor	Multiprocessor
Technology	NMOS, CMOS	GaAs, CMOS, VHSIC (RISC)	GaAs, RISC	GaAs
Main Memory	64K-128K bytes	.5 - 1 Mbyte	25-30 MIPS	100-200 Mbytes
Performance	0.5 - 1 MIPS	3 - 5 MIPS	25-30 MIPS	100-200 MIPS
Networking	1-3 Mbytes/sec	5-10 Mbytes/sec	10-50 Mbytes	100 Mbytes
Size	1/2 ATR	2 CKT Cards	1-2 CKT Card	1-2 CKT Card
Power	< 250W	< 50W	< 20W	< 10W
Cost	< $5K	< $3K	< $3K	< $3K

1.3.5 Advanced Computer Architectures

1.3.5.1 Discussion

In the past decade there has been considerable momentum in both the commercial and academic arenas to explore and develop new architecture utilizing von Neumann and non-von Neumann concepts to meet the growing demands of real time applications and to support particular software concepts. The rapidly emerging reduced instruction set (RISC) concept is projected to become widely supported for the next several years in the general purpose, von Neumann configurations and there is still some effort in reducing the 'semantic gap' to more closely match architectures to HOL's. Systolic and data flow approaches are being widely pursued in non von Neumann development. There also has been considerable pressure particularly from NASA/DoD to develop standards to support either specific HOL's or specific object code in order to exploit software portability/re-useability. Perhaps the most concentrated research/development effort is directed by the well documented Japanese initiative to develop a 'fifth generation' machine by 1990.

Fruition of much of this development is heavily dependent on the VLSI technology. Tremendous advances have been made within the past few years such that 10^6 transistors on a single chip is now possible. The successful implementation of high performance, 32 bit architectures with cache and memory management produced at relatively low cost (see section 1.3.4)is testimony to this advancement. The Intel 432 project designed to implement Ada provided VLSI building block approach that also incorporated significant F/T capabilities. Also, NCR recently introduced their Geometric Arithmetic Parallel Processor (GAPP) that provides 72 single bit processors each with 128 bits of RAM on a single chip representing the first commercial systolic array processor chip.

These chips make possible the realization of extremely powerful machines through utilization of massively parallel techniques. The 'Cosmic Cube' project at CalTech, for example, utilizes an array of 64 standard processors with a special interconnection network and delivers 10% of the Cray I performance at 1% of the cost. The currently active VHSIC projects will boost the VLSI technology.

1.3.5.2 Options

For the purpose of discussion, the subjects addressed in the background section have separated into three categories: instruction set architectures, multiple processor architectures, functional language architectures, and the Japanese initiative. Each is discussed in some detail in the following sections.

1.3.5.2.1 Instruction Set Architectures

Instruction sets may vary in size; from large, redundant sets of minimal, or, reduced instructions sets, depending on the particular philosophy embraced. One such philosophy is that of the Reduced Instruction Set Computers (RISC) which employ primitive instruction sets utilizing simple hardware implementations. Recent architecture trends have provided increased instruction functionalities requiring multi-level decoding and additional clock cycles at the expense of more complex circuit and firmware designs. Improved performance of these designs relies on execution of fewer instructions for specific solutions plus continuing advancement in VLSI technologies. This approach is illustrated by the new 32-bit processors, i.e., Motorola 68020, National 32032, Zilog 80000. The proponents of RISC, however, argue that increased performance is more universally achieved through the use of simpler instructions with faster execution times. For sophisticated applications requiring complex operations, the performance benefit has not been clearly demonstrated; however, co-processor chips could be developed for these complex operations.

While the RISC concept is not new, relatively few architectures have been committed to hardware. This group, all experimental, includes:

MIPS - Stanford University
RISC-1 - U.C. Berkeley
IBM 801

RISC has recently been identified as an alternative approach for incorporating new technologies into near term microprocessor development. The reason is that these technologies, i.e., GaAs, have not matured sufficiently to support the 200,000 transistor/chip densities of the new 32-bit designs but support the 20,000 transistor/chip RISC design density. This development will be particularly attractive for space oriented projects since GaAS provides not only speed enhancement but radiation tolerance.

DARPA contracts for development of a GaAs RISC processor have been awarded for 1 year to MDAC, Tektronix/RCA and TI/CDC for a design plus sample hardware demonstration.

The MDAC design characteristics include:

- Stanford MIPS architecture
- 32-bit data path
- Fixed point processor with a floating point co-processor
- 16 Mword addressability
- 4 watts/chip
- ~ 20,000 transistors/chip
- 50 Mbps typical execution rate (fixed point)
- Pascal compiler

1.3.5.2.2 Multiple Processor Architecture

Much of the effort in this architectural category is being devoted to the correspondence between processors and attached components at nodes on a computer network, a tightly-coupled multiple processor, or a distributed computing environment. The physical matching of bandwidths between processors, memories, and physical linkages is greatly inhibited by the software overhead required for the interactive protocols and general management of the multiple resources. Although much was learned from the Cm* and C.mmp experiments at Carnegie-Mellon University, there is still much more to be developed for the computer network performance to match the total capability of the processors and their attached components. The COSMIC CUBE is one experiment in that direction.

Another ongoing experiment is ZMOB at the University of Maryland, which has 256 processors connected via a high-speed ring, so that a processor may communicate with any other in "unit time", where unit time is defined as the time it takes to send data once around the ring. ZMOB uses a functional language and progress is being made towards achieving a high degree of concurrency, and, thereby improved performance.

There are many computer networking and multiple processor experiments presently underway in various university and industry laboratories. Of course, the performance of tightly-coupled multiple processors depends heavily upon low-overhead communication software to reach the throughput capabilities of the hardware.

1.3.5.2.3 Functional Language Architecture

This class of architectures represent a departure from the classical von Neumann, synchronous, defined instruction cycle designs. Performance improvements are possible through the use of functional languages. Perhaps best documented in this classification is the Data Flow architecture. The data flow computer achieves fully asynchronous, parallel instruction execution through two basic principles of operation:

Asynchrony: An operation is performed only when all required operands are available.

Functionality: All operations are purely functional (i.e., no side-effects are produced).

Instead of execution control based on a program counter (von Neumann), data flow operators (instructors) compute whenever all required input operands are available. The output values from one operator flow directly to the inputs of the next operator(s) without memory storage. This approach eliminates shared memory bottlenecks of processor von-Neumann designs.

The principle of functional execution for data flow designs is that the operators cannot interact, thus synchronization is not required, eliminating the need for a central control.

The essence of data flow program execution is the interconnection and execution of functions. Conceptually, each data flow operator is allocated to a unique processing unit. The set of operators that the computer directly executes is the "base language". Functional, high order languages with compilers have been developed to translate the HOL's into the "base language" for execution. It is not yet known whether functional language architectures, such as data flow, can efficiently execute functional programs in comparison to von Neumann architectures and conventional language programs. The major issue in answering this question is the high level at which functional programs are written. Major open questions still exist in the categories of:

1) compiler techniques;
2) interconnection structure;
3) caching;
4) tree representations of lists;
5) granularity of parallelism; and
6) controlling parallelism.

Functional program architectures are currently under widespread, active experimentation to study the efficient execution of functional programs on multiprocessor systems. The announcement by NEC of a data flow processor chip is a welcomed hardware development, which will enhance the success of these experiments and facilitate broad spectrum projects to answer the important questions about functional language architectures.

1.3.5.2.4 Fifth Generation Architecture

Advances in Artificial Intelligence research and applications have been slowed by the lack of computer systems with adequate performance and memory capabilities. Such computer systems are anticipated as the next or 'fifth generation' machines which are expected to feature massively parallel architectures with tremendous capabilities for concurrent pattern recognition and performing logical inferences.

After a two-year preliminary investigation into the requirements and options of the next generation architectures, the Japanese, in April 1982, officially began their 'fifth generation' initiative, the most challenging and extensive computer project undertaken to date. Under the direction of their Institute for New Generation Computer Technology (ICOT) in combination with researchers from eight Japanese corporations, this initiative has the goal of developing a prototype 'fifth generation' computer system by 1990.

The project involves the unification of four separate areas of research: knowledge based expert systems, very high level programming languages, decentralized computing, and VLSE technology.

Three basic functions for the architecture have been identified:

a) intelligent interface machines corresponding to conventional I/O,

b) inference machines, corresponding to conventional CPU's, and

c) knowledge based management machines, corresponding to an integration of main and virtual memories.

These systems are expected to:

a) have a performance capability of 100M to 1G logical Inferences/sec (LIPS)

b) process natural languages such as English and Japanese

c) freely handle non-numerical data such as documents, graphics, images, and speech

The project research into the advanced architecture will address several options including:

- Logic-Programming Machines
- Functional Machines
- Relational-Algebra Machines
- Abstract-Data-Type Support Machines
- Data Flow Machines
- Innovative Von Neumann Machines

For the Logic-Programming machines, the research theme is the study and development of the necessary architectures to support inferences and a computational model based on predicate logic with a power of expression approximating natural languages. This research will involve development of languages and a processing system incorporating predicated logic, development of the basic technology (parallel systems and special-purpose mechanisms), and logic programming machine (with a development goal of 50M - 1G LIPS).

Research for the Data Flow machines will be oriented to parallel processing. The preliminary goal is a machine with 16 processors and a memory of 8M bytes. The final goal is a high speed machine wit 1000 - 10,000 processors, a memory of 1G - 10G bytes, and a performance of 1 - 10 LIPS.

1.3.5.3 References

1. D. P. Siewiorek, et al., "A Case Study of C.mmp, Cm*, and C.vmp: Part I - Experiences with Fault Tolerance in Multiprocessor Systems," Proc. IEEE, Vol. 66, No. 10, Oct. 1978, pp. 1178-1199.

2. N. Takahashi, and M. Amamiya, "A Data Flow Array System: Design and Analysis," Proc. Tenth Ann. Symp. Computer Architecture, 1982, pp. 243-250.

3. D. D. Gajski et al., "A Second Opinion on Data Flow Machines and Languages," Computer, Vol. 15, No. 2, February, 1982, pp. 58-69.

4. H. J. Siegel, "Interconnection Networks for SIMD Machines," Computer, Vol. 12, No. 12, June, 1979, pp. 57-65.

5. M. Satyanaranayan, "Commercial Multiprocessing Systems," Computer, Vol. 13, No. 5, May 1980, pp. 75-96.

6. D. A. Patterson and D. R. Ditzel, "The Case for the Reduced Instruction Set Computer," Computer Architecture News, Vol. 8, No. 6, October 1980, pp. 25-33.

7. M. Flynn, "Directions and issues in architecture and language: Language Architecture Machine," Computer, Vol. 13, No. 10, pps. 5-22, October, 1980.

1.4 SOFTWARE

1.4.1 Advanced Algorithms

1.4.1.1 Data Compression

There are numerous operational requirements for processing/transmitting remotely sensed imagery and for general science and engineering (GSE) data acquired as part of the Space Station program. The imagery data volume in particular, is expected to increase immensely as imaging systems of higher resolution and spectral bands are developed and deployed. The vast amount of mission data thus acquired in space applications poses a serious problem to the Space Station Data System (SSDS) in terms of data storage, processing complexities and response times for end-to-end data transmission. Consequently, the cost of archiving, transmitting and distributing large quantities of mission data becomes a significant SSDS design consideration, even with the currently projected improvements in applicable technology. To achieve real-time efficient transmission of mission data and to conserve communications channel bandwidth, data compression is usually considered as one of the most powerful tools available. Data compression algorithms tend to be application dependent and as such will probably not be a standard service provided by the SSDS. However, since they offer significant potential for impact on key SSDS drivers, they will be characterized to the extent necessary to assess this impact.

In addition to minimizing the storage cost, data compression provides the following potential benefits:

- Memory requirement for search terms may be reduced.
- Lower transfer time due to compressed data volume may result in faster responses to an I/O bound system.
- Decompression processing can be distributed (i.e., embedded in workstations).
- Transmission of compressed data may result in reduced communications bandwidth requirements, and thus reduced communications costs.
- Backup/recovery time may be reduced.

However, these benefits do not come without potential drawbacks which include the following:

- Data processing overhead will be increased for data compression/decompression algorithms.
- Data Base Management System (DBMS) design may be made more complex to account for interrelationship between index/file design, search processing, and data compression algorithms.
- Some data compression schemes may destroy properties of the data which may be required by a DBMS.
- Sensitivity to bit error rates may be increased.

These advantages and disadvantages from data compression must be evaluated within the context of the desired application. Consequently, the use of data compression to the desired application data must be weighed with a performance measurment for the desired data quality. This performance measurement is the so-called compression ratio (CR). A high CR usually results in a low data quality due to the high root mean square error (RMSE) associated with high CR. For instance, a user, who desires to have his application data with high accuracy, may decline the use of any data compression on his data acquisition in fear that the compressed data may not be recovered in its original (exact) form for his special studies. In this case, the user's data (non-imagery), which is expected to be relatively small in quantity, will be processed, stored, and transmitted in an uncompressed form. For user(s) whose spectral/spatial data is acquired through high resolution remote sensor systems, the volume of data is expected to be very large. In this case the quality of reconstructed imagery with a very large compression ratio may be found adequate for visual display in a digital browse facility available to the remote user(s) at a minimal charge.

Some compressed mission data are more sensitive to channel noise than others because an error in the compressed data during transmission through a noise channel will usually introduce considerable amount of distortion. Error correction coding, therefore, is often adopted when data compression techniques are used to assure noiseless data transmission.

Data Compression options are grouped into four general categories as follows:

- o Textual Data Compression
- o General Purpose Data Compression
- o Spectral/Spatial Data Compression
- o Data compression coupled with channel coding

1.4.1.1.1 Textual_Data_Compression

1.4.1.1.1.1 Description. Data compression techniques in this category are generally applicable to a wide range of text-oriented algorithms. The options include, but are not necessarily limited to, the following algorithmic techniques:

a. Repeated Character Compression
b. Fixed Length Encoding
c. Variable Length Encoding
d. Phase-oriented Compression

1.4.1.1.1.2 Option_Characterization. The textual data compression schemes listed above are described as follows.

a. Repeated_Character_Compression

This technique was the first to be used in commercial database management systems as well as operating systems. The intent is to either eliminate unnecessary characters (i.e., trailing blanks/zeros, etc.) or to replace strings of repeated characters with counts or other information requiring less storage space. Systems using this technique include IBM's HASP and WYLBUR. Repeated character compression has the following characteristics:

- o Low computational overhead
- o Effective for embedded blanks or other repetitive characters.
- o Most effective with formatted text (e.g., printouts, reports, computer programs, etc.).

b. Fixed_length_encoding

This technique is based on the fact that, while data is encoded using, say, an 8-bit character set, most of the bit combinations appear very seldom in the data. In some applications, all necessary characters can be comfortably encoded into smaller field code. This provides an immediate, data-independent reduction in required storage space. Baudot and 6-bit ASCII codes are examples of this technique. The characteristics of fixed-length encoding include the following:

- Not effective if a complete character set is required.
- Low computational overhead for actual compression/decompression.
- Depending on the byte-oriented nature of the host machine, algorithms involving shorter characters can be slow and complex to program.

c. Variable_length_Encoding

This technique is based on the observation that some characters occur more frequently than others. The algorithm builds a table of variable-length bit encodings for the characters, the most frequent being represented by a small number of bits, and the less common ones by relatively long bit strings. The σ-code algorithm by Hart[1] is one of the variable length encoding techniques developed for data compression. In some applications, compression of the order of 50% have been reported. This approach can be charactrized as follows:

- Optimal encoding techniques
- High computational overhead and relatively complex programming.
- Complex boundary conditions for byte-oriented transfer to external devices.
- Can be extended to character pairs.
- Compression efficiently depends on knowledge of character frequency statistics.

d. Phrase-oriented_compression

This technique takes advantage of detailed knowledge of the phrase occurrence rates in the database. This method depends heavily on the precise content of a specific database.

1.4.1.1.2 General_Purpose_Data_Compression

1.4.1.1.2.1 Description. Data compression algorithms in this category are, neither theory-oriented, nor specifically designed for a particular type of mission data, but generally applicable to reversible data reduction for general purpose. The options include, but are not necessarily limited to, the following:

a. Data Compression by Prediction Method
b. Data Compression by Interpolation Method
c. Transform Coding

1.4.1.1.2.2 Option_Characterization. The general purpose data compression algorithms listed above are described as follows.

a. Data_Compression_by_Prediction_Method

This technique developed for data source redundancy reduction is based on a test by comparing the predicted sample point, X', with the actual data point, X, to see whether the magnitude of the difference between two points is within an apriori tolerance band, B [2]. The predictor (the predicted data point for the present sample) is calculated with a difference polynomial by using the past samples; or simply, the predictor predicts the present sample by using the past samples. In case the magnitude of the difference between X and X' is less than or equal to B, the point will not be transmitted. The process is repeated until the absolute difference is over the threshold value B, the actual sample point is transmitted appended with a code to indicate the number of sample points which were not transmitted. Of course, the first actual sample point is always transmitted and used as the starting point (reference point) for the calculation of the first predictor. During decompression, the data points that were not transmitted will be filled out with the calculated predictors by using the same difference polynomial for data compression.

The predictor can be calculated with an Nth order difference polynomial, for N = 0, 1, 2, ... It is apparent that the higher is the N value, the more complex the hardware/software design is involved,

and consequently, the less efficient the prediction data compression will become. Therefore, only four relatively simple prediction algorithms for data compression are described as follows:

(1) Zero Order - The predictor is always set equal to the actually transmitted sample point or the previous successfully predicted one.

(2) Zero Order with Offset - This technique differs from the zero order in that the predictor will remain the same as described above as long as no sample point is transmitted. Once an actual point is transmitted the predictor will be calculated with an added value which is simply the magnitude of the offset.

(3) First Order Predictor - This is similar to the zero order algorithm discussed above except that a first order difference polynomial is used to compute the predictor.

(4) First Order with Slope Correction - This algorithm is defined mathematically with a slope correction term added to the first order predictor, where the slope correction is a function of increment in actual sample points X and the number of data points skipped prior to a data transmission.

These prediction algorithms, in general, are designed for calculating a predictor with Nth difference polynomial, when $N \geq 2$, tend to increase complexity for hardware/software implementation.

The operational characteristics of the prediction methods for data compression are given [2] in Table 1.4.1.1-1 below:

Table 1.4.1.1-1
Option Characterization of Prediction Methods

Prediction Algorithms	Best Applied To Image Data Type	Efficiency	Hardware Complexity	Software Complexity
Zero Order	Nearly non-constant, slow varying	Very Good	Low	Low
Zero Order with offset	Constant, slow varying	Good	Low	Low
First Order	Medium Varying	Good	Low	Low
First Order with Slope Correction	Moderately Active	Good	Low	Medium

b. Data_Compression_by_Interpolation_Method

The interpolation data compression technique is similar to the predictor algorithm using an Nth order difference polynomial, where N = 0, 1, 2, ... The interpolator differs from the predictor in that all sample points between the last transmitted point and the present actual point affect the interpolation [3]. According to the software evaluation results as shown in [2], [3] and [4], the performance improvement of the interpolator from a first order difference polynomial to a second or third order does not justify the added hardware/software complexity, therefore, only the zero order and first order interpolator algorithms are described as follows:

(1) Zero Order Interpolator - The functional operation of the zero order interpolator algorithm as illustrated in Figure 1.4.1.1-1, is similar to the zero order predictor. The main difference pertains to the sample selected to represent the redundant set. The transmitted sample point for the zero order interpolator is the interpolated sample point and determined at the end of the redundant set.

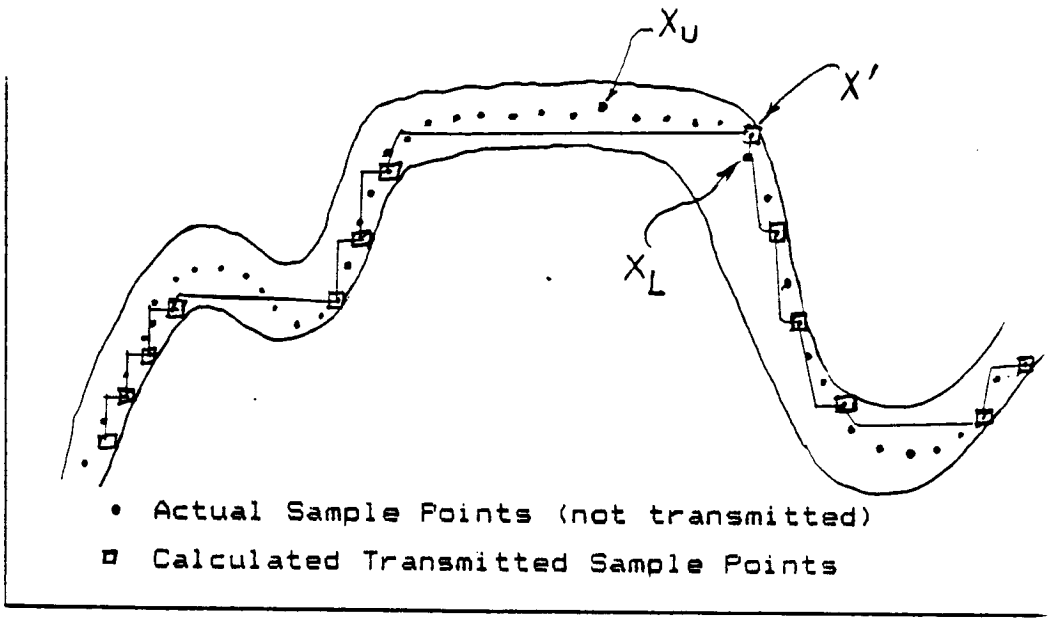


Figure 1.4.1.1-1 Zero Order Interpolator

As shown in Figure 1.4.1.1-1, for example, the transmitted sample point X is computed as the average between the most positive sample X_U and the most negative sample X_L in the set. All actual samples which were not transmitted prior to X' are within an a priori tolerance from X'.

(2) First Order Interpolator - The functional operation of the first order interpolator algorithm can be described as drawing a straight line by using the first order difference polynomial between the present sample and the last transmitted sample point such that all intermediate data points (not transmitted) are within the preset tolerance of the interpolated point at the end of the straight line. In this algorithm, the very first sample point is transmitted. This algorithm demonstrates that the starting point of a new line is common to the end point of the previous straight line, and thus the continuous presentation of the data is provided.

The interpolator algorithms described above for data compression have the following characteristics:

- In general, the interpolation technique for redundant reduction is more efficient than the predictor, when applied to the type of data varying continuously in a random manner or perturbed by high-frequency noise.

- The zero order interpolator is simple in terms of hardware/software implementation and very efficient when applied to nearly constant and slow varying data.

- The first order interpolator can be applied efficiently to any non-burst data, but may increase the complexity in hardware design.

c. Transform Coding

The transform coding technique developed for channel bandwidth compression is performed in a sequence of transformations using two operators as described in [2], [5], and [6]. The mathematical operator transforms the input image data into another domain in which a closely correlated input data is transformed into a form of independent coefficients. The second operator quantizes and codes each of the coefficients. The two-dimensional transform then transmits the code over a channel rather than the image itself. An inverse transform at the receiver reconstructs the imagery data. Figure 1.4.1.1-2 is given below to illustrate a generalized transform coding scheme.

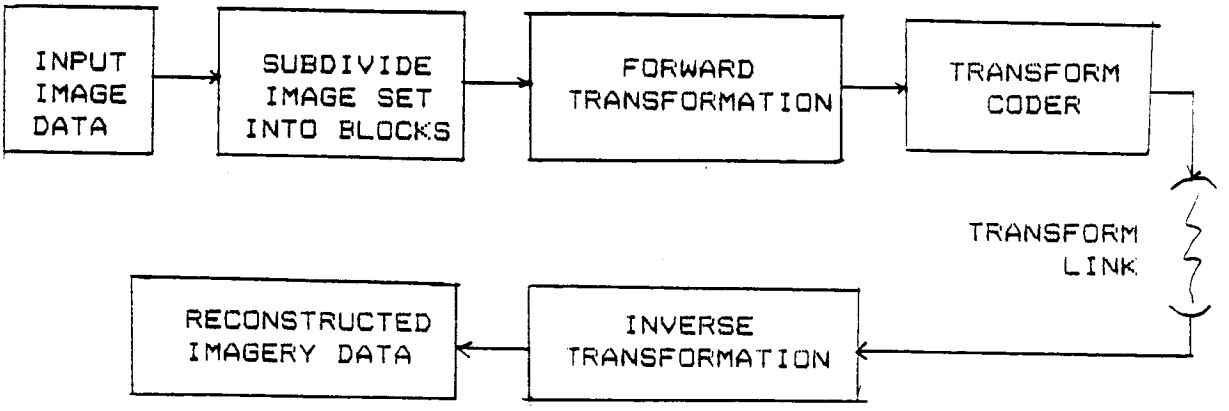


Figure 1.4.1.1-2 Transform Coding Functional Flow

During transform coding processing, the imagery data set is divided into data blocks for subsequent processing. The design logic is that in case any error occurs during transform processing, it will be averaged out in a single block so that the error propagation is reduced. The forward transformation provides the axis change and outputs the transformed coefficients. The transform coder provides the data compression by selecting the various coefficients according to their significance. Those coefficients that do not meet the preset threshold required will not be transmitted.

The transform coding technique has another property which compacts the input image energy into a few coefficients. This enables the deletion of the least significant coefficients without increasing error in the reconstructed imagery data. Therefore, adaptive thresholds should be used for coefficient selection, i.e., in an imagery data block with active data, such as an edge of an object, more information data should be selected by presetting a relatively low threshold. As noted, the inverse is calculated identically, except the normalizing factor, as the forward transform. Therefore, the inverse transformation uses the same information as the forward transformation to reconstruct the image.

Four commonly used transform coding techniques are described briefly in the following:

(1) Karhunen-Loeve Transform - This algorithm is considered optimal [5] in that it generates uncorrelated coefficients, compacts most of the energy in a few coefficients and thus results in minimum mean square quantization error. However, the mathematical operations are tedious due to the need for a precise estimation of the covariance matrix for the random field and determination of eigen functions of the matrix. Therefore, this technique is usually not recommended for real-time data compression.

(2) Fast Fourier Transform - The advantage of the fast fourier transform coding is that it produces a decomposition of input images into sinusoidal waveforms [5]. The transformed image will be quantized, coded, and transmitted over the communication channels. Then at the receiver, the inverse Fourier transform is taken to reconstruct the visual image.

(3) Hadamard Transform - This transform coding is based on the Hadamard matrix which is a square array of plus and minus ones and whose rows and columns vectors are mutually orthogonal [5]. That implies that the transpose and the inverse of the matrix are identical. This algorithm simplifies the implementation since it does not require any multiplication.

(4) Discrete-Cosine Transform - A special transform coding technique was developed and evaluated as shown in detail in [6]. This algorithm uses Hamming coding with the two-dimensional discrete cosine transform, the so-called 2D-DCT, at a transmitted data rate of 1 bit/pixel over a binary symmetric channel. The design bit error rate (BER) of interest is defined at 10^{-2}. The research results showed that the allocation of 33 out of 256 (16 by 16) bits per block using the Hamming code to protect (select) the most important 2D-DCT coefficients can substantially improve the quality of the reconstructed image at a BER of 10^{-2}. The most important bits to select are determined by calculating the mean squared reconstruction error (associated with an A-Factor table), contributed by each bit in a 256-bit block, where each A of A_1 through A_8 in A-Factor table is defined as the normalized average reconstruction error power caused by a single binary bit error in bits 1 through 8, respectively. The bits are thus ranked according to their calculated error values from the largest to the smallest. Then, the bits corresponding to the largest errors are deemed to be most important. As for the number of bits to be selected for transmission, it is calculated based on a well defined probability bit error equation [6].

The transform coding techniques used for data compression have the following characteristics:

- o The transform coding, in general, involves tremendous amounts of computations and complex implementation in hardware design. It seems not suitable for multispectral imaging data compression unless some special purpose chips currently being developed, such as GaAs, can then be available for the SSIS real-time hardware/software implementation.

- o It may be applicable for channel error recovery for transform image coding as discussed in [7].

1.4.1.1.3 Spectral/Spatial Data Compression

1.4.1.1.3.1 Description. Interest in data compression on space mission data is growing, especially in high-data-rate systems such as the Multispectral Linear Array (MLA). This MLA concept arises from the user needs which drive the design of the next earth resources satellites away from the current Landsat Multispectral Scanner (MSS) and Thematic Mapper (TM) configurations. Adequate data compression techniques are required to insure that the instrument generated high data rates can be compatible with the Tracking and Data Relay Satellite System (TDRSS) and with ground data processing.

For some users of the high-data-rate systems, the operational purposes of a compression technique are two-fold. The primary goal is image understanding and information preserving rather than characterization of absolute scene radiance. Secondarily, the reconstruction image process should be relatively simple even though the data compression might be computationally tedious. The options in this spectral/spatial data compression category incude, but are not necessarily limited to, the following algorithmic techniques:

a. Cluster Coding
b. Differential Pulse Code Modulation
c. Entropy Measurements and Maximum Compression Ratio

1.4.1.1.3.2 Option Characterization

a. Cluster Coding

The Cluster Coding Algorithm (CCA) was developed by Hilbert [8] [9] and Ramapriyan [10] for clustering and source coding to compress multispectral image. All clustering techniques depend on a distance measure between measurement vectors and a distance measure between clusters. The distance measures between vectors, usually referred to as the mean features, approximate the vectors and thus give the spectral definition of a multispectral image. The distance measures between clusters, usually referred to as the cluster map features, give the spatial definition. A simple flow of the Clustering Coding Algorithm implemented by Ramapriyan [10] is given in Figure 1.4.1.1-3.

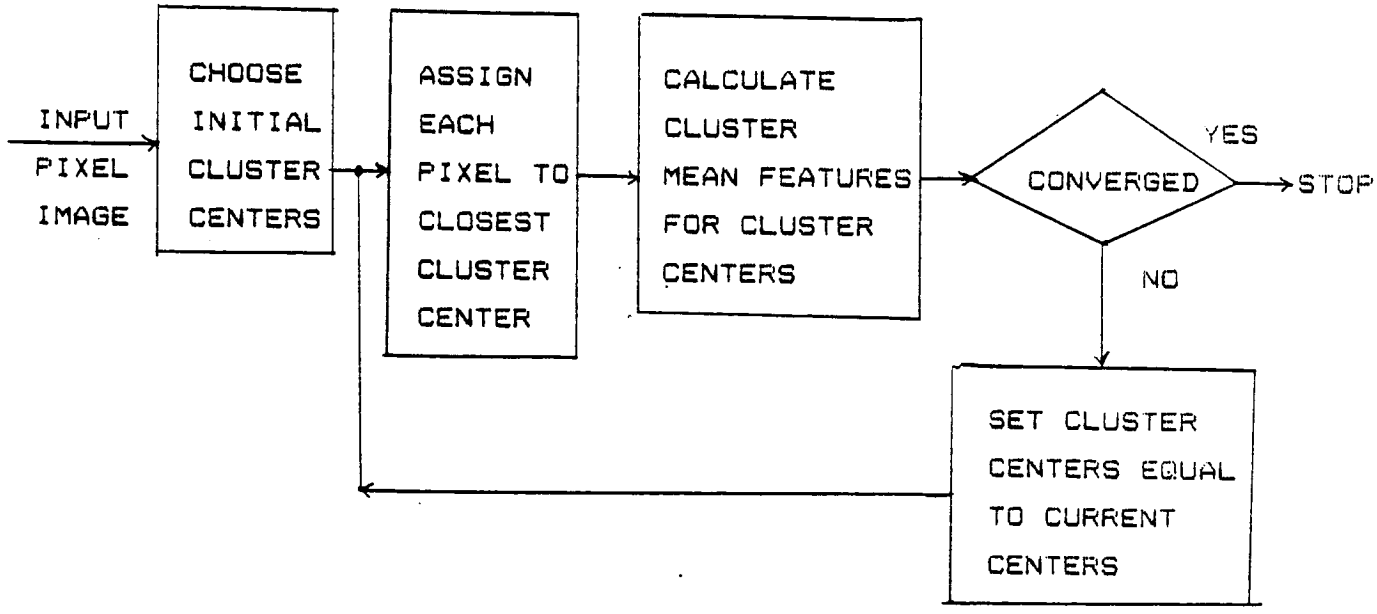


Figure 1.4.1.1-3 CCA Compression Flow

The CCA used for spectral/spatial data compression, as shown in Figure 1.4.1.1-3, has the following characteristics:

- Clustering is a means for automatically grouping multidimensional high-data-rate remotely sensed data.

- To being with a CCA, a number of initial cluster centers are determined by a set of a priori feature values of means and variances for the multispectral data vectors to be clustered.

- The input image is divided into non-overlapping cluster blocks, and is processed (compressed) block by block by the clustering algorithm.

- The nearest cluster center to a pixel is determined by calculating the Euclidean distance between the pixel and each cluster center.

- Each cluster mean is computed after each pixel is assigned to the cluster with the nearest cluster center. In case no pixel is assigned to a cluster center, the cluster mean remains unchanged.

- The cluster mean feature values and the cluster map feature values are output respectively to the cluster mean feature file and cluster map feature file for use in future image reconstruction.

- The convergence test can be accomplished in one of the two schemes: The simplest way is a pre-determined integer to indicate the number of iterations desired. The other case is that in each iteration a fraction parameter (in percent) of the pixels that changed the cluster assignment is calculated and then checked against an a priori threshold. If the calculated percentage is smaller than the threshold value, the clustering process is assumed to have converged.

- The spectral and spatial compression ratios are calculated respectively. The spectral compression ratio, corresponding to the cluster mean features file, is a function of f, m, d and n, where f is the number of bits per feature value per band, m is the number of clusters per cluster block, d is the number of bits per original pixel value per band, and n is the

number of pixels per cluster block. The spatial compression ratio, corresponding to the cluster map features file, is defined as the number of bits required to represent that data in the cluster map file divided by the number of bits required to represent the original data.

- The total compression ratio is the sum of the spectral and the spatial compression ratios.

- The compression factor, as it is oftenly used as an alternative to measure the compression performance, is defined as the inverse of the total data compression ratio.

- The image reconstruction, or image decompression, is simply done as follows. For each cluster block, each pixel value is set (without calculation) equal to the mean value of the cluster (i.e., the cluster map feature) which the pixel is assigned to according to the cluster map file. The mean value of each cluster for the current cluster block is read from the cluster feature file.

- The compression process on the multispectral image involves very tedious calculations, therefore, a data processing system with very high throughput is required.

b. Differential Pulse Code Modulation

The Differential Pulse Code Modulation (DPCM) scheme was used by Hawkes [11] to compress the space data from a Multispectral Linear Array (MLA) imaging system by using the Gallium Arsenide integrated circuit technology in a feasibility study. During the DPCM processing a prediction value X' is calculated from preceding transmitted image samples to predict the present input sample X. The difference between X and X' is coded and transmitted to the decoder, and the image is then reconstructed in the decoder by adding the coded difference to the prediction value X'. Three different DPCM data compression schemes applied specifically to the multispectral image [11] are briefly described in this section. They are:

- o DPCM with Huffman Type Entropy Coder
- o Block DPCM with Limited Overflows
- o DPCM with Non-uniform Max-quantizer

(1) DPCM_with_Huffman_Type_Entropy_Coder. A typical Huffman type DPCM data compression scheme is depicted in Figure 1.4.1.1-4. The multispectral image is fed into the Huffman type data compressor. The predictor is designed to reduce the dynamic range of the image data before it is presented to the entropy coder. The entropy coder, which applies a Huffman type coding algorithm to assign variable length prefix codes on a one-to-one basis for the differences given to it by the predictor, is briefly described as follows.

As shown in Figure 1.4.1.1-4, the predictor X' can be:

a) Set equal to the adjacent (previous) $X_{i-1,j}$,

b) Calculated with two previous samples as the difference of $(2X_{i-1,j} - X_{i-2,j})$ by using linear extrapolation, or

c) Computed as a two-dimensional adjacent sample mean as $(X_{i-1,j} + X_{i,j-1})$ over 2. Then the difference presented to the entropy coder for Huffman type coding will simply be $(X_{i,j} - X')$.

The design logic of the transmit buffers in the scheme is to smooth out the variations in bit rate caused by the variable length of code words.

(2) Block_DPCM_with_Limited_Overflows. The DPCM algorithm takes a fixed number of image pixels (8 bits/pixel) from the scan line and packs them into a data block which contains:

a) 1 (one) pixel reference value with 8 bits.

b) N pixel differences with 3 or 4 bits each.

c) P number of overflow with 8 bits per overflow.

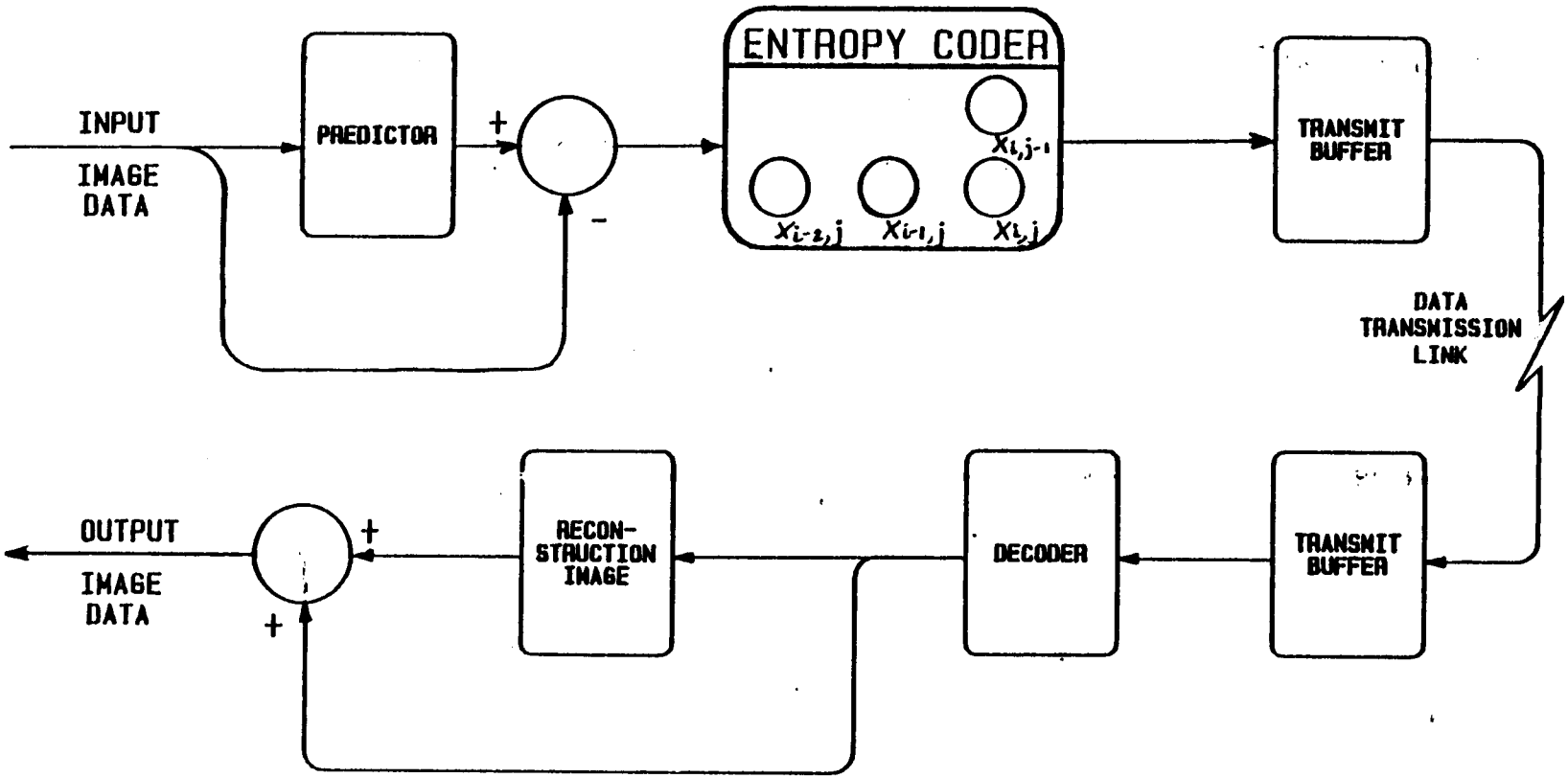


Figure 1.4.1.1 - 4 Typical Huffman Data Compression Scheme

The scheme is depicted in Figure 1.4.1.1-5.

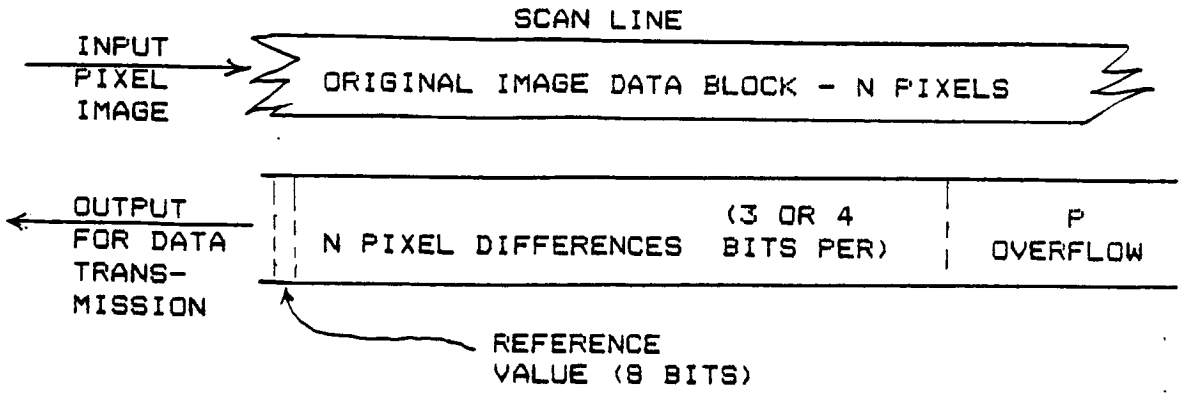


Figure 1.4.1.1-5 Block DPCM with Limited Over-Flow Scheme

The pixel differences are calculated with the simple adjacent prediction arithmetic as described above in paragraph (1)a). The difference values are normally in the range of $\pm 2^B$, where B is 8 representing 8-bit pixel value. Data compression is achieved by limiting the pixel differences to $\pm (2^{L-1}-1)$, where L is 3 or 4. In some cases, however, the pixel difference values computed this way may well exceed the above defined limit. When this occurs, the pixel difference, usually represented with a 3-bit (or 4-bit) value, is replaced with a code instead, to indicate an overflow situation, and the overflow pixel difference value in 8 bits is placed in the first overflow slot. Subsequent overflows are placed in sequence in the remaining overflow slots. During decompression, the reconstruction of the original data image from the compressed data block is straight forward.

(3) DPCM_with_Non-uniform_Max-quantizer. This algorithm uses a prediction/differencing scheme on the image pixels from a scan line, and then the differences are fed into a non-uniform quantizer as shown in Figure 1.4.1.1-6, where X is the original input pixel, X' is the reconstructed reference value, D is the difference of X' from X, and R is the coded reconstruction level. The non-uniform quantizer has only limited number of decision and reconstruction levels which are characterized by a 3 or 4 bit code. In this scheme, there is no exact representation of the differences.

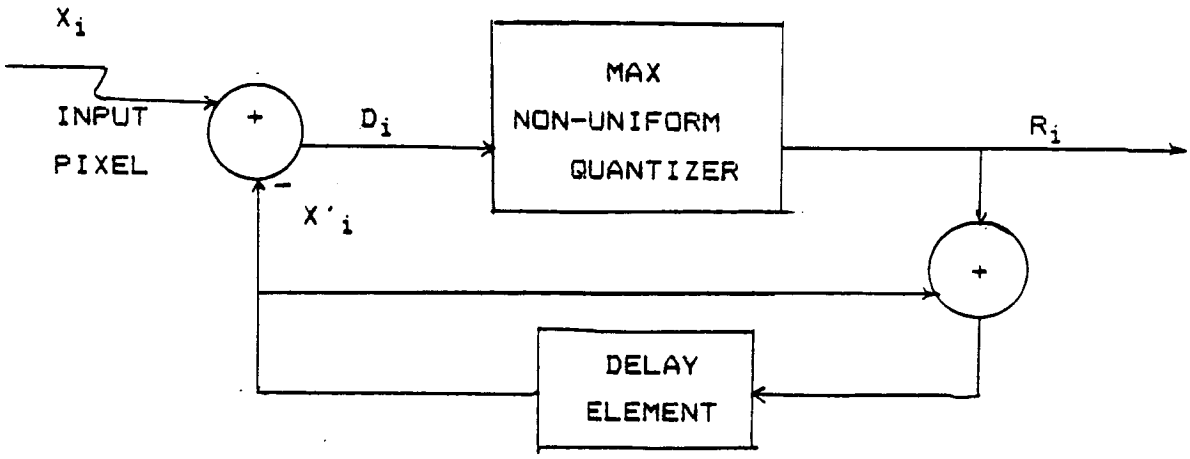


Figure 1.4.1.1-6 DPCM with Max-Quantizer

The predicted value used to compute the difference, is not the value of the previous pixel as specified in the simple adjacent prediction algorithm, but is the sum over the previous reconstruction differences. The placement of the decision and reconstruction levels in quantization theory is usually solved based on some optimization criterion. The Max-quantizer was designed with a criterion of minimizing the mean squared error between input and output by an assumption of a particular probability density function for data entering the quantizer [11]. The Max-quantizer has, as its input/output, continuous signals. The results are generally given in the form of a table of decision and reconstruction levels normalized with respect to the standard deviation of the probability density function of the input data. It normally derives the standard deviation of the input and scales the table as desired.

The three DPCM data compression techniques have the performance characteristics as tabulated below [11]:

Table 1.4.1.1 - 2

Option Characterization of Three DPCM Schemes

Scheme	Advantage	Disadvantage	Compression Ratio
DPCM with Huffman Entropy Coder	• Could produce high fidelity data with error correction code	• Transmission error can cause loss of code sync	2.0 - 2.3
Block DPCM with Limited Overflow	• Fixed block structure • Simple to implement	• Potential buffer overflow • Large memory required on-board	1.6 -
DPCM with Non-uniform Max-Quantizer	• Simple to implement • Degrade gracefully as image gets busier • Fixed block structure	• Produce distortion	2.0 - 2.6

c. Entropy Measurements and Maximum Compression Ratio. Miller developed an algorithm related to data compression for the NASA End-to-End Data Systems Program with the MLA spatial resolution requirements as a baseline [12]. It is not a data compression technique but a scheme which provides an upper bound to the amount of data compression that can be achieved to preserve the scene spatial resolution with minimum (or without) distortion during image reconstruction. The Miller option has the following characteristics [12]:

- A zero-order entropy, H(X) defined as the quantized pixel size, is derived as a measure of the average source data rate N (with N = 8, i.e., 8 bits/pixel).

- To include the mutual data information between adjacent pixels, Y and X, where Y refers to a pixel output with given knowledge of the preceding pixel X, a first-order entropy, H(Y/X), can be derived accordingly. As noted, H(Y/X) is always smaller or equal to H(X) due to pixel to pixel correlation.

- The maximum data compression ratio, C_{max}, is defined as a function of N over H, where N is number of bits (per pixel, of original image), and H is the zero-order entropy or the first-order entropy, in bits.

- In order to reconstruct the image from the receiver, such overheads in bits have to be added to the transmitted data, as synchronization (S), channel error control (E), and reference information (R). Then a data compression ratio, C, with overhead parameters is defined as (N+S)/(A+S+E+R), where A is the compressed average bit rate. It should be observed that C is always less than C_{max}.

- Based on Miller's study [12], the average compression ratio with no distortion during image reconstruction is in the range of 2.5 to 3.0 (without overhead). However, the compression ratio in an actual system would be lower, due to the effect of the overhead parameters discussed above.

- As noted in Sobieski's technical briefing on "Techniques for Reducing Processing Requirement," a data compression factor of 0.5 was shown as an indicator of compression performance for reducing data storage in space [13]. The Sobieski compression factor as a function of data entropy, was taken as an inverse of the compression ratio from Miller's study [12].

1.4.1.1.4 Data Compression Coupled with Channel Coding

1.4.1.1.4.1 Description. Data compression algorithms have been developed and implemented for remotely sensed imagery and/or GSE data applications at Jet Propulsion Laboratory (JPL) for efficient space data transmission. As noted, compressed data during end-to-end downlink transmission are, in general, more sensitive to the channel noise than the data uncompressed, because an error in the compressed data generally introduces a considerable amount of distortion by going through a noisy channel. For this simple argument, some data compression techniques have been developed by making direct use of the error-free concatenated Reed-Solomon/Viterbi channel coding for compressed data transmission as shown in Figure 1.4.1.1-7. Prior to introducing data compression techniques developed in this category, a very brief discussion of the channel coding is found necessary.

The concatenated channel coding, as shown in Figure 1.4.1.1-7 between the data compression and data reconstruction, consists of the Reed-Solomon (RS) codes as the outer code and the Viterbi convolutional codes as the inner code, designed for data transmission [14]. As described in [15], the RS code is commonly referred to by two code parameters, J and E, and denoted as a $(2^J-1, 2^J-1-2E)$ RS code, where J is usually set to 8 to indicate the number of bits per RS symbol, and E is usually set to 16 to indicate the RS symbol error correction capability with an RS codeword. In this coding system, the incoming data bits are grouped into J-bit symbols and encoded by an RS encoder. The RS encoder receives consecutively (2^J-1-2E) symbols as the information symbols and generates 2E check symbols appended to information symbols to form an RS codeword containing (2^J-1) symbols. The RS codewords thus formulated are then fed into a

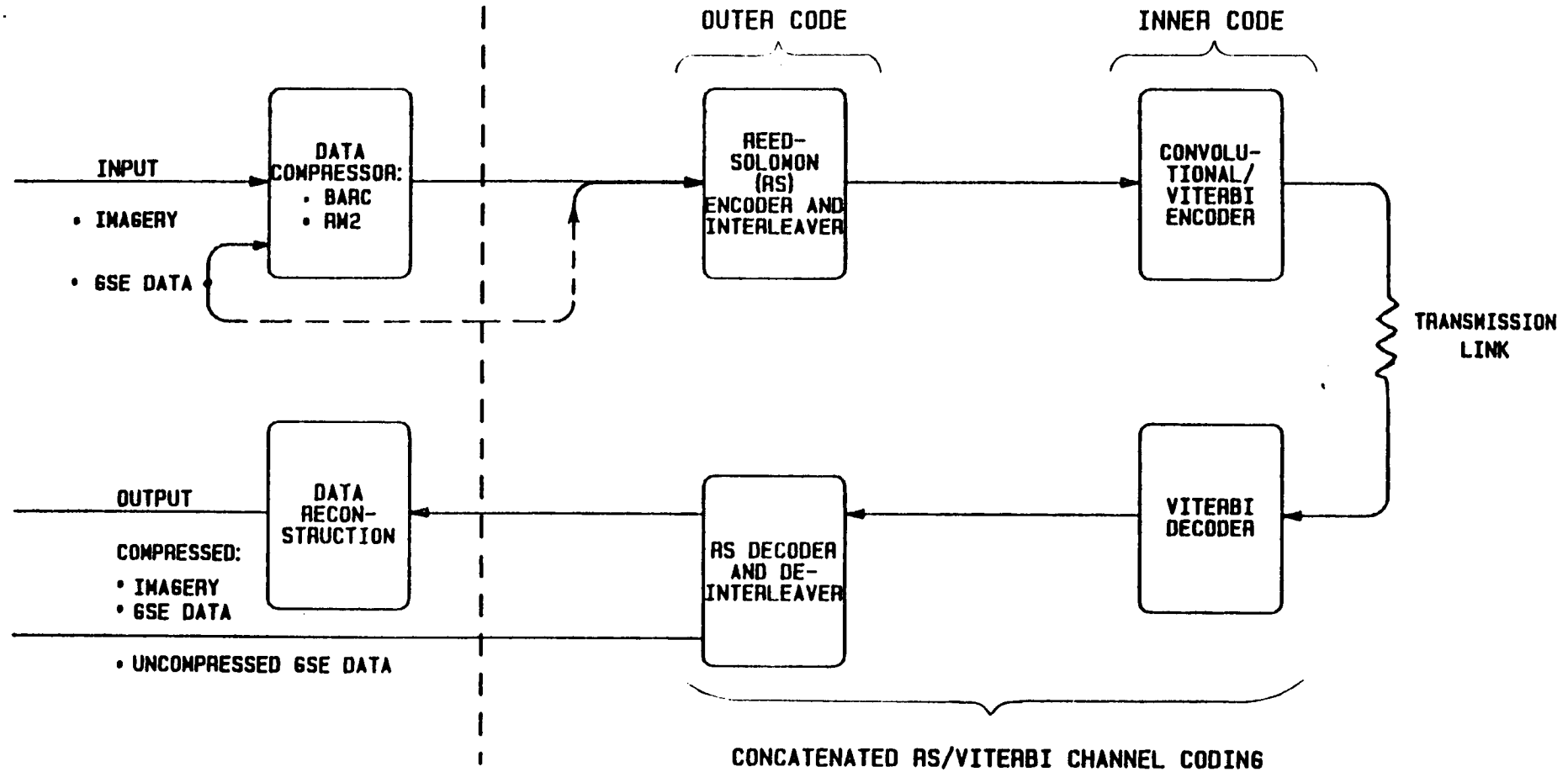


Figure 1.4.1.1 - 7 Compressed Data Transmission Through Concatenated RS/Viterbi Channel Coding

convolutional encoder and transmitted through a communication link to the receiver. The received data is Viterbi-decoded and then fed to an RS decoder for decoding.

As shown from the test results [15] [16], a concatenated coding system with an ideal interleaving depth provides a virtually error-free communication channel. As a matter of fact, to insure a BER of 10^{-5} or less as generally required for error-sensitive GSE space mission data transmission, is practically achievable. Since a virtually error-free channel is feasible, any sophisticated adaptive source coding techniques can then be applied for imaging and GSE data compression without concerning the error sensitivity/distortion problems associated with compressed data.

The data compression algorithms developed in conjunction with the concatenated RS/Viterbi channel coding, include, but are not necessarily limited to the following:

- o Block Adaptive Rate Controlled Image Data Compression
- o RM2 Image Data Compression

1.4.1.1.4.2 Option Characterization. The data compression algorithms given above are described as follows:

a. Block Adaptive Rate Controlled Image Data Compression. The Block Adaptive Rate Controlled (BARC) image data compression was developed by Rice and Lee and implemented at JPL for remotely sensed space data transmission through the concatenated channel coding [17]. The functional operations illustrated in Figure 1.4.1.1-8 are fundamental to the BARC algorithm. The basic design logic of BARC is to partition a line (one-dimensional) of input data sequence of image with N bits into smaller data blocks. For each block, an activity estimator will be calculated simply by taking the quantized sample (pixel) value of the entropy. The activity measures are used for those partitioned blocks to determine which blocks should receive reductions in linear quantization. The number of reductions and their location is determined with some simple arithmetic algorithms [17] such that,

(1) when all the blocks are efficiently coded the number of bits used equals the number allowed for the input data sequence, and

(2) reductions in quantizations are first applied to blocks with higher activity measures (larger sample-to-sample variations).

As shown in Figure 1.4.1.1-8, the block quantizer is simply a linear quantization operation. This is accomplished by a shift and roundoff operation to the calculated X' based on input sample (pixel) X [17]. The BARC noiseless coder consists of two operations: the preprocessing operator and the code operator. The preprocessor basically performs appropriate decorrelation and relabeling operations while the code operator performs the assignment of variable length codewords to the preprocessed data [17] [18]. These two operations are reversible in that inverse operations applied to the output data transmitted through the concatenated channel coding will reconstruct exactly the original input data.

b. RM2 Image Data Compression

The RM2 data compression technique was developed by Rice for remote sensing image data reduction [18]. RM2, an acronym without definition in any of Rice's publications, is defined literally in this paper with his consent as the Rice Machine 2 (in the true sense of software). The RM2 was developed prior to the BARC compressor, mainly for imaging data reduction, and that is why the two algorithms have all (almost) the same functional and performance characteristics. The distinct difference between these two compressors is that for the block quantization function as shown in Figure 1.4.1.1-8, BARC uses a one-dimensional algorithm for deriving the quantized X' by a shift and roundoff operation over the original sample X, while the RM2 algorithm applies to a two-dimensional sample structure [18]. It is similar to the "two-dimensional adjacent samples" predictor for the Huffman entropy coder as shown in Figure 1.4.1.1-4.

The option characterization of these two algorithms are comparatively described in the following:

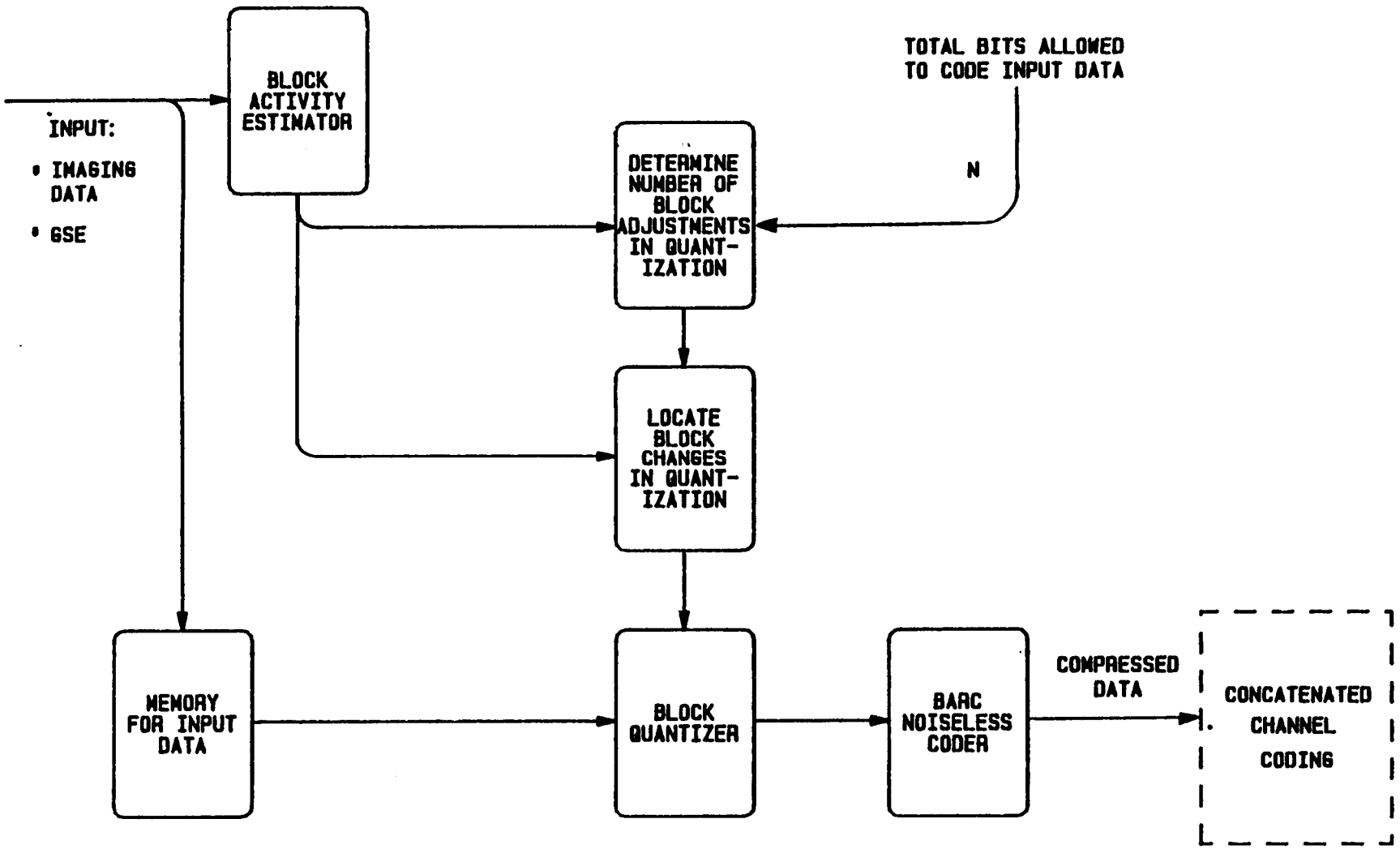


Figure 1.4.1.1 - 8 BARC Block Diagram

- Functionally, both algorithms allow arbitrary selectable compression rates, but the RM2 two-dimensional structure for block quantization provides a broader range of options. That is, at high rates of 3 bits per sample and above, the rate/quality performance of both algorithms is equivalent, whereas at lower rates RM2 provides a decided advantage.

- Both algorithms can be operated with the noiseless coders with code rates close to the data differential entropy for all entropies above the neighborhood of 0.7 bits per sample [17].

- BARC basically provides the top end of the RM2 rate/quality performance range while applying only one-dimensional processing. The one-dimensional processing also means that BARC is applicable to, besides imaging data, the GSE type of correlated data for which there are stringent fidelity requirements.

- Both algorithms use the concatenated RS/Viterbi channel coding for virtually error-free data transmission [19].

1.4.1.1.5 Data Compression Projected Capabilities

For achieving efficient space mission data transmission and conserving communications channel bandwidth, data compression techniques have been developed. As a result of limited time and effort for literature search, discussed above are the following 16 data compression algorithms arbitrarily grouped into 4 categories as listed below:

Category 1: Textual Data Compression (4 algorithms)

- Repeated Character Compression
- Fixed Length Encoding
- Variable Length Enclding
- Phase-oriented Compression

Category 2: General Purpose Data Compression (6)

- o Data Compression by Prediction Method
- o Data Compression by Interpolation Method
- o Transform Coding:
  - Karhunen-Loeve Transform
  - Fast Fourier Transform
  - Hadamard Transform
  - Discrete-cosine Transform

Category 3: Spectral/Spatial Data Compression (4)

- o Cluster Coding
- o Differential Pulse Code Modulation:
  - DPCM with Huffman Type Entropy Coder
  - Block DPCM with Limited Overflows
  - DPCM with Non-Uniform Max-Quantizer
- o Entropy Measurements and Maximum Compression Ratio (not data compression algorithm but upper bound measurement for evaluating spatial data compression performance).

Category 4: Data Compression Coupled with Channel Coding (2)

- o Block Adaptive Rate Controlled Image Data Compression
- o RM2 Image Data Compression

The data compression algorithms listed above have been developed by scholars in the academic fields or by experts/researchers in aerospace industries and particularly in some space centers. It is conceivable that the algorithms on the list, even though not exhaustive, are definitely representative. As a result of this study, the projected capabilities of data compression techniques which can be applied to the space image and/or GSE data, are discussed as follows.

a. Data Unique/Instrument Unique/User Unique

Space data compression is data unique, instrument unique or user unique. Different users, on ground or in space, may request mission data using different instrument(s) in space at different data rates for different purposes. Therefore, data generated during a specified mission flight will be vastly different from each other in terms of

data volumes (large, medium or small) or in terms of data types (spatial data or science engineering data). Consequently, data compression technique(s) required for data reduction will be different. In other words, a unique data compression algorithm should be applied to a data type uniquely generated for a user with unique mission requests using specific instruments. Furthermore, some performance parameters included and used in a specific data compressor should be specified differently in the data base to meet different (or the same) user requirements. For instance, the RM2 imaging compression algorithm provides the rate/quality performance [19] as shown in Figure 1.4.1.1-10. It indicates that at an average rate of 2 bits per pixel (picture element) the Rmse (Root Mean Square Error) is approximately 0.4, but an average rate of 0.5 bits/pixel will yield an Rmse approximately 3.6. This implies that, assuming a user had planned a mission to generate large volumes of multispectral data by using a high-rate sensor onboard, he might decide to use the RM2 compressor for data reduction with either one of the two alternatives: taking a compression ratio of 4:1 (2 bits per pixel) for a better Rmse, or specifying a compression ratio of 16:1 with a higher Rmse, depending on the quality of the reconstructed data he desired for some special purposes.

b. Exact Data Transmission with Compression Option

A user may have planned a mission and requests his mission data be generated and transmitted without compression for special research that requires data integrity. Of course, this type of mission data is expected to be well planned and the size of data generated is not in large quantity (relatively speaking). However, for such user's in some special mission(s), the unnecessary characters, such as trailing blanks/zeros, may appear consecutively in the generated data sequence. To this case, a compressor in the Space Station data system, such as the Repeated Character Compression, may well be applied automatically even without the user's permission, for efficient data transmission.

c. High Computer Throughput Capability Requirement

The hardware/software complexity associated with most of the data compression algorithms design has always posed a severe problem for the

current computers to resolve. However, some new computer developments, such as the VHSIC program sponsored by DoD, are striving to show high performance capabilities in improving throughput and radiation tolerance. Lately, the Gallium Arsenide (GaAs) development for data processing has shown significant potential for future space onboard/ground applications with its high electron mobility and inherent radiation tolerance. These new computer developments should enhance the projected capability of the data compression techniques implemented for space imaging and science engineering data reduction.

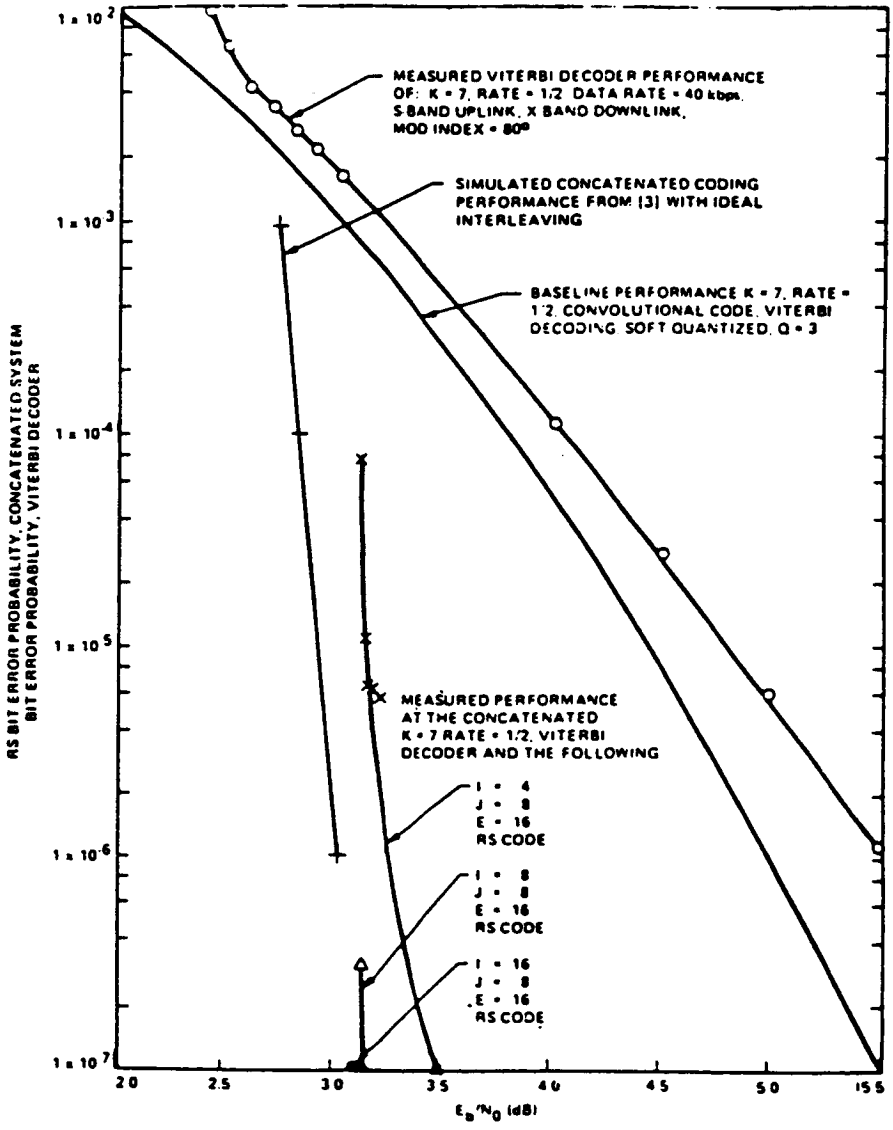
d. Concatenated Channel Coding

The development of sophisticated adaptive source coding (data compression) algorithms together with inherent error sensitivity problems fostered the need for efficient space data communication at very low bit error probabilities. This led to the development and implementation of such channel coding system as the one discussed above in paragraph 1.4.1.1.4.1. The performance of the concatenated channel coding scheme was evaluated experimentally under a strong uplink and downlink condition. The experimental results showed that the concatenated coding scheme provides a coding gain of 2.5 dB or more at very low BER ($\leq 10^{16}$) as compared with the Viterbi-decoded convolutional-only system as illustrated in Figure 1.4.1.1-9 [15]. It is felt strongly that during the SSDS software design the concatenated channel coding scheme should be considered for implementation, especially when BARC and RM2 data compression algorithms are considered for space data reduction.

e. Promising Data Compression Algorithms

As a study result of the data compression algorithms discussed above, the following action items related to the data compression projected capabilities are suggested:

(1) Optional Data Compression. It seems logical that the Repeated Character Compression scheme should be implemented as an option for the SSDS management to compress the unnecessary character strings in a mission data sequence for efficient space data communication.



Performance of the RS/Viterbi concatenated coding system (bit error probability versus E_b/N_0).

Figure 1.4.1.1-9

(2) Feasible Data Compression Techniques. Assuming that the new computer development programs for future space data processing applications provide significant potential and that the virtually error-free channel coding is readily applicable, the Differential Pulse Code Modulation techniques as referenced in Table 1.4.1.1-2, and the Cluster Coding Algorithm developed at GSFC for spectral/spatial data compression [11], are worthwhile for further exploration. Especially, based on results as shown in Figure 1.4.1.1-10, the RM2 and BARC image compression algorithms developed and implemented at JPL for deep space data reduction are recommended for consideration.

Based upon the results of this literature survey, the performance of the 16 data compression algorithms given above are summarized, with respect to their potential applications, efficiency or compression ratio, and implementation complexity, in Table 1.4.1.1-3 to conclude this study.

Of course, for efficient data communication, some special efforts sponsored by NASA on developing new data compression algorithms and/or improving current existing data compression algorithms should continue until real-time data system implementation.

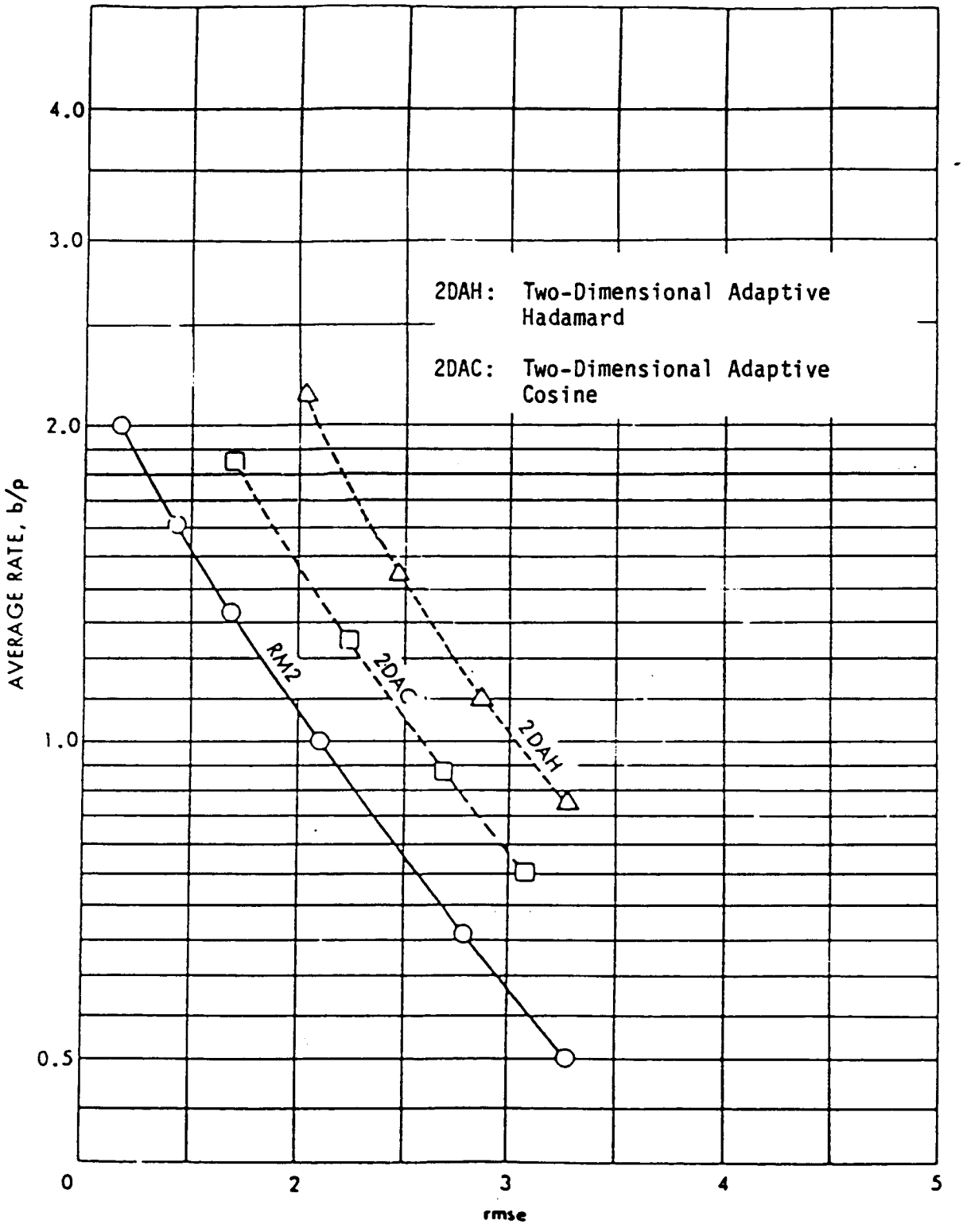


Figure 1.4.1.1-10. Rate Versus Rmse.

Table 1.4.1.1-3

Data Compression Algorithms

Performance Summary

DATA COMPRESSION ALGORITHM	POTENTIAL APPLICATION	EFFICIENCY OR COMPRESSION RATIO	H/W AND S/W IMPLEMENTATION COMPLEXITY
o Repeated Character Compression	Text	Good	Low
o Fixed Length Encoding	Text	Good	H/W Low, S/W Medium
o Variable Length Encoding	Text	Good	S/W High H/W Low
o Phase-Oriented Compression	Text	Good	S/W High
o Data Compression by Prediction Method	Low to Moderate Data Rate	Good	Low to Medium
o Data Compression by Interpolation Method	Low to Moderate Data Rate	Very Good	Low
o Karhunen-Loeve Transform	Low, Medium or Burst (any type)	Very Good	High
o Fast Fourier Transform	Any Type	Good	Medium
o Hadamard Transform	Any Type	Almost Good	Medium

Table 1.4.1.1-3

DATA COMPRESSION ALGORITHMS

PERFORMANCE SUMMARY (CONTINUED)

DATA COMPRESSION ALGORITHM	POTENTIAL APPLICATION	EFFICIENCY OR COMPRESSION RATIO	H/W AND S/W IMPLEMENTATION COMPLEXITY
o Discrete-Cosine Transform	Any Type	Very Good	H/W High S/W Medium
o Cluster Coding	Landsat	2.77	S/W High H/W Medium
o DPCM with Huffman Type Entropy Coder	Multispectral Linear Array (MLA) Future Landsat	2.0 - 2.3	H.W High (buffer & memory)
o Block DPCM with Limited Overflows	Future Landsat	1.6	S/W High
o DPCM with Non-Uniform Max-Quantizer	Future Landsat	2.0-2.67	Medium
o Block Adaptive Rate Controlled Image Data Compression	Spatial Imagery & GSE Data	2.0+	S/W High H/W Medium
o RM2 Image Image Data Compression	Spatial Imagery & GSE Data	2.0 - 6.0	S/W High H/W Medium

1.4.1.1.6 References

[1] M. M. Hart, "δ-Code, A Variable Length Code for Data Sources," NASA, Langley Research Center, Hampton, VA, December 1984 (unpublished).

[2] M. M. Hart, "A Preliminary Study on a Switching Algorithm for Data Compression," NASA Langley Research Center, Hampton, VA, December 1984 (unpublished).

[3] C. M. Kortman, "Redundancy Reduction - A Practical Method of Data Compression," Proceedings of the IEEE, Vol. 55, No. 3, March 1967.

[4] C. A. Andrews, J. M. Davies, and G. R. Schwarz, "Adaptive Data Compression," Proceedings of the IEEE, Vol. 55, No. 3, March 1967.

[5] G. A. Nimmo, "The Hadamard Transform and Its Use for Bandwidth Compression," MDAC, March 14, 1977.

[6] D. R. Comstock and J. D. Gibson, "Hamming Coding of DCT-Compressed Images Over Noisy Channels," IEEE Transactions on Communications, Vol. COM-21, No. 7, July 1984.

[7] O. R. Mitchell and A. J. Tabatabai, "Channel Error Recovery for Transforms Image Coding," IEEE Transactions on Communications, Vol. COM-29, December 1981.

[8] E. E. Hilbert, "Joint Pattern Recognition/Data Compression Concept for ERTS Multispectral Imaging," SPIE Seminar Proceedings, Efficient Transmission of Pictorial Information, Vol. 66, August 1975.

[9] E. E. Hilbert, "Cluster Compression Algorithms: A Joint Clustering/Data Compression Concept," JPL Publication, 77-43, 1977, Jet Propulsion Laboratory (JPL), Pasadena, CA.

[10] K. H. Ramapriyan, J. C. Tilton and E. J. Seiler, "Impact of Data Compression on Spectral/Spatial Classification of Remote Sensed Data," NASA Goddard Space Flight Center (GSFC), Greenbelt, MD, December 1984 (unpublished).

[11] C. D. Hawkes and D. Firstenberg, "Gallium Arsenide Integrated Circuit Technology Feasibility Study," Rockwell International Contract No. NAS5-26732, Volume I of III, For NASA Goddard Space Flight Center, Greenbelt, MD, September 1983.

[12] W. H. Miller, T. J. Lynch, and C. R. Gilgore, "Entropy Measurements and Maximum Compression Ratio with No Distortion," Document No. X-728-82-13, NASA Goddard Space Flight Center, Greenbelt, MD, May 1982.

[13] S. Sobieski, "Analysis of Processing Requirements for Space Station Science Data," a briefing given at Johnson Space Center, 23 October 1984, (Sobieski works for GSFC, Flight Mission Support Office-Code 501).

[14] "Telemetry Channel Coding," Recommendation for Space Data System Standards, Blue Book, Issue-1, May 1984, published by CCSDS (Consultative Committee for Space Data Systems), Secretariat, Communications and Data Systems Division, Code-TS, NASA, Washington, D.C.

[15] J. J. Lee and K. Y. Liu, "Recent Results on the Use of Concatenated Reed-Solomon/Viterbi Channel Coding and Data Compression for Space Communications," IEEE Transactions on Communications, Vol. COM-32, No. 5, May 1984.

[16] R. F. Rice, "Channel Coding and Data Compression System Considerations for Efficient Communication of Planetary Imaging Data," JPL Technical Memorandum 33-695, NASA, JPL, Pasadena, CA, 1 September 1974.

[17] R. F. Rice, J. J. Lee, et al., "Block Adaptive Rate Controlled Image Data Compression," Proceedings of 1979 National Telecommunications Conference, Washington, D.C., November 1979.

[18] R. F. Rice, "Practical Universal Noiseless Coding," SPIE Symposium Proceedings, Vol. 207, San Diego, CA, August 1979.

[19] R. F. Rice, "End-To-End Imaging Information Rate Advantages of Various Alternative Communication Systems," JPL Publication 82-61, NASA, JPL, Pasadena, CA, September 1, 1982.

1.4.2 On-board Space Station High Order Language

1.4.2.1 On-board Source Language

1.4.2.1.1 Description

The Phase B RFP for the Space Station Software Development Environment states that "The reduction of life-cycle costs, maximum commonality of hardware, software, and systems among elements of the SSP are principal objectives of the program". It further states "For software, commonality of programming languages, support software, operating systems, and user interface languages are major goals". The on-board source languages, which are used for application and system software both on the On-board Space Station, platforms, and in the development and simulation environments on the ground are the subject of this section. Specifically excluded are design languages, user control and interface languages, and simulation languages.

We believe a single general purpose programming language is available that could truly meet the requirements of commonality, provide the capabilities needed, (both general purpose and real-time) and provide the necessary media for minimizing life cycle costs. We should judge such a language on richness and functional capabilities, ease of learning, maturity/availability, ease of use, readability, modularity, concurrency, exception handling, and applicability to the space station.

Eight candidate languages are considered; these are Ada, Pascal, Modula-2, HAL/S, JOVIAL, C, PL/1, and FORTRAN. Other languages were not considered; generally, because they lacked modern features, have not been accepted in the community, were not standardized, and/or did not provide the functions required by the On-board Space Station.

In addition, we need to look at what language support tools are provided, how well the language supports modern software concepts and methodologies and determine its stability and potential for the future.

1.4.2.1.1.1 On-board Source Language

The On-board Space Station applications are varied. The language must support both system and application type programs. The language must be suitable for embedded computer applications, provide real time services to an embedded network operating system, be capable of generating the tools required for simulations and other processes associated with the space station and its ground based development environment. The language must be able to support interactive processing, be able to interface with a data base management system, and be able to support the communication services required by the space station in communicating with its satellites, the Shuttle and the ground support systems.

1.4.2.1.1.2 Characteristics of a Modern Programming Language

In order to address the life-cycle and productivity costs of programming for the Space Station, new techniques and methods must be applied in the way programs are generated and reused. A modern programming language can aid in making this possible. The characteristics that are essential and would be provided in part by most modern programming language are as follows:

- Be amenable and supportive of top-down structured programming techniques and other modern design and implementation methodologies
- Provide modularity
- Have strong typing
- Provide isolation of the user from private data and code (information hiding)
- Have provisions for data abstraction

By use of these concepts and techniques it is possible to develop programs that are useable, reliable, easily maintained and understood, secure, and reusable. More detail information about their characteristics and application follows:

- Structured programming – Top-down structured programming provides for the development of a program in a modular hierarchical form. The modules may be programs, procedures, tasks, and subroutines or some equivalent organizations depending on the language.

The selected language must not only have these capabilities, but also have mechanisms to insure the consistency of the relations between these organizations. In addition, a mechanism should be in place that would allow or provide stubs for lower level references, so that the rest of the design can be accomplished, coded, compiled and tested.

A structured language must have language constructs that are well defined and which provide a concise representation of a logical sequence within a module (e.g., constructs, such as when, while, if then else, loop). These constructs foster the use of non-goto sequences, but more importantly, they enhance the quality of the design by making the design simpler, clearer, and more readable. As a consequence the design is easier to generate, implement, maintain, and review.

It should be noted that in the discussion of structured programming that the top-down methodology is not the only viable methodology. Often in designing a program, basic building blocks are identified, such as subroutines, which may have general applicability. These may be designed and implemented first, resulting in conformance to this lower level design by higher levels of a program. This bottom-up methodology is aided by whatever modularization capabilities a language possesses. Thus, the best methodology will be a blend of the top-down and bottom-up approaches together with other proven software methodologies.

- Modularity - Modularity is the process of breaking up a program into manageable parts that are logically consistent. Modularity allows many developers to work concurrently on a project. But, more importantly, it allows a program to be reduced to manageable parts that can be visualized and understood. For example, it has been a standard for many years in IBM/FSD [36] that modules should not have more than 50 statements. Larger modules are difficult to comprehend and therefore difficult to develop, read, and maintain. The language should foster and be amenable to the construction of manageable modular units.

- Strong Typing - The Rationale for the Design of the Ada* Programming Language [1] states that "a type characterizes the set of values that objects of the type may assume, and the set of operations that may be performed on them". The Rationale further states that typing serves the purpose of collecting in one place the common properties of objects and giving them a name. It also serves to separate the underlining and internal implementation dependent properties and to distinguish in a program the distinct properties of the objects. A strong typed language does not allow values of a variable of one type to be assigned to variables of another type. Nor does it allow mixing of variables of different types in the same expression unless explicitly provided for. Strong typing in a programming language guarantees these properties and ensures the reliability and the consistency of the productions.

- Information Hiding - Information hiding is a technique in which a user is isolated from data and code which a user should not modify, which the user can use without being dependent on its definitions or operation other than for interface purposes, and which can be modified only by the originator, so long as it remains functionally equivalent and the interfaces remain the same.

- Data Abstraction - Grady Booch in his book "Software Engineering in Ada" [3] quotes Ross, Goodenough, and Irvine in their article on "Software Engineering" on abstraction as follows; "The essence of abstraction is to extract essential properties while omitting inessential details". Grady Booch in the glossary of his book defines abstraction as "Our view of an entity in the problem space; in fact, everything that we know is an abstraction. All abstractions are part of a ladder of abstraction in which given levels are implemented at a lower level." William F. Appelbe in his paper entitled

  * Ada is a trademark of the U.S. Government Ada Joint Project Office.

"Abstract Data Types in Ada" [5] says "Abstract data types were developed as a tool for designing and specifying modular, reliable software. An abstract data type defines a class of objects, together with the operations which may be applied to objects of that class." He then cites as common examples queue, stack, buffer, and file. The ability to limit the set of operations to that set defined for the abstract data type is of utmost importance especially in system programming.

1.4.2.1.1.3 Other Language Considerations

In addition to the above, consideration must be given to other factors which would reduce development costs and provide reliable software for the Space Station. First, is the development of reusable components. To make code more viable and reusable for the On-board Space Station, a single general purpose programming language should be used. This language should have properties such as modularity, as previously mentioned, have macro or generic capabilities to allow for the broader application of the sequences and generation of reliable code, should have precise interface definitions and utilize information hiding. Another factor is the availability of useable code. With a single language that is mature and is not changing, therefore truly portable, it becomes possible to use code from one project to another.

Also, vendors will concentrate on producing code sequences in the single language source format. If the single language of choice for the Space Station is a also the choice for other embedded systems, the number of offerings of useable source modules can become almost unlimited.

Additional factors that must be considered in a high order language for the Space Station are exception handling, concurrency, the ability to interface with other languages, and I/O and communication capabilities. The selected language must allow for the precise handling of anomalies when they are encountered during the execution of code. Even though the Space Station will not have the critical ascent and entry problems of the Space Shuttle, critical events and/or processes do occur, such as maintaining the proper operation of the life support systems, maintaining the attitude of the craft, controlling the operation of satellites, supporting payload operations. For these, the language must be capable of providing corrective actions, e.g., driving external alarms or controls. The foregoing was not meant to imply that control of these processes is under the exclusive control of software, but to suggest that if hardware is not used for these purposes, software control is required.

The language must be able to accommodate concurrent processing. This is particularly important on the Space Station itself, where multiple processors will be used in a distributed network system. In this situation multiple concurrent executions are required to provide, for example, redundancy in case of component failure and to ensure certain real-time operations.

The language of choice must be capable of interfacing with other languages. This is especially important in the ground-based Space Station preparation areas where hundreds of thousands of lines of useable and proven code already exist. In this case, it would be desirable to write new source code in the new language and interface to the old code for various services and actions. This is not a major factor in the Space Station On-board system, as most code must be rewritten to accommodate changed requirements and a new environment.

The new language must be capable of providing all types of I/O and communication services. Both application and system type programs must be serviced. This means a generalized I/O capability must be provided; both interactive and general.

1.4.2.1.2 On-Board Source Language Option Characterization

Ada list of general purpose programming language options for the On-board Space Station are as follows:

- Ada
- Pascal
- Modula-2
- HAL/S
- JOVIAL 73
- C
- PL/1
- FORTRAN

1.4.2.1.3.1 Ada

Ada is a modern programming language [1,2,3,14,30,...] that was designed for large real-time embedded systems, but which has general purpose programming capabilities.

It has strong modularity, typing, and information hiding capabilities and lends itself well to modern programming methodology, such as structured programming and data abstraction.

It has facilities for exception handling, for concurrency, and for interfacing with other languages. Although it does not have direct I/O constructs, these functions are provided adequately thorough packages. It supports reusability through generics and the application of modules. It also has capabilities for addressing specific storage cells and for "dropping" into assembly language.

Ada is a new language and as of yet has not been proven on a large scale real-time embedded system. It is complex and will require considerable amount of training to use it properly. It is an ANSI standard language. Its compilers are required to be validated. Also, it is the required language for all new DOD embedded systems.

1.4.2.1.2.2 Pascal [14,26,30]

Pascal is a language of the 70's, which has become exceedingly popular in the university and in some industrial communities. It is the basis for a number of the newer modern languages. New versions have been formulated from it, such as, Path Pascal and Concurrent Pascal. It provides strong typing, checking of interfaces to procedure and function modules, constraining of range values, and has a set of well-thought-out control statements, that enhance structured programming. Not provided are separate compilation, real-time tasking constructs, low-level I/O, means for connecting software modules to hardware interrupts, information hiding, and constructs for detecting or handling run-time errors. Some of the deficiencies of Pascal have been overcome in the Path Pascal and Concurrent Pascal versions, however, because of a lack of a separate compilation capability in these versions they will not be further considered.

The language is an ANSI standard language. However, because of extensions for system constructs in the useable versions (i.e., in the extended versions), the language cannot be considered truly standard or stable.

1.4.2.1.2.3 Modula-2

Modula-2 [26,30], an enhancement of Pascal, provides modular capabilities. It is strongly typed, provides compiler allocation of data storage, allows specifying an absolute address for a data element or routine, provides range specification, provides task management, and allows separate compilation of modules. No information hiding is provided.

It is a strong language that overcomes most of the Pascal deficiencies and provides most of the capabilities required by the Space Station. However, it has one serious fault [30] in its inability to interface with modules other than Modula-2 and assembly language modules. The language is not currently an ANSI standard and no validation procedures have been established for its compilers.

1.4.2.1.2.4 HAL/S

HAL/S is a language of the very early 1970's which contains many of the important structured programming features of today. It was and is being used with considerable success on one of the largest embedded programming systems; namely, the Space Shuttle Systems. Although not strongly typed, the language overcomes some of the typing problems by annotating the various references in the compiler listing. HAL/S provides dynamic error detection and exception handling. It has numerous modular constructs, provides for checking module interfaces at compile-time, and allows for separate compilation of program, function, procedure, and data modules. It provides real-time tasking constructs with explicit control of initiation, termination, and cyclic task operation.

It has limited I/O capabilities, provides no dynamic storage management, has no absolute addressing mechanism, and contains no "drop in" assembly language capabilities.

The language is controlled by NASA and it appears unlikely the language will be changed in the near future. Limited compiler implementations exist for the language and none have been formally validated.

1.4.2.1.2.5 JOVIAL 73

JOVIAL 73 [14] is an upgrade of the original JOVIAL designed in the early 1960's. It has been successfully used throughout the years; mainly for Air Force projects. It is a weakly typed language. It provides programs, function, procedure, and data modules, but no task modules. These modules may

be separately compiled. Interface checking is performed. No information hiding and real data abstraction support is provided. The language provides no real-time tasking constructs, no I/O capability, and no interrupt handling. Extensions are being considered.

The language is controlled by the Air Force and all implementations must be validated by the Air Force. The language will continue to be used for current projects. It will be replaced by Ada for new projects as soon as a satisfactory implementation of Ada becomes available.

1.4.2.1.2.6 C [33,14,30]

C is a general-purpose language developed in the early 1970's. It is considered by its authors as a "low level" language. It deals "with the same sort of objects that most computers do, namely characters, numbers, and addresses". It has been primarily used in systems programming (writing compilers and operating systems), i.e., where it is necessary to specify particular registers and addresses.

No aggregate operations are defined. The language does not define any storage allocation facility, nor does it provide input-output, tasking, or exception handling facilities:

The language is classified by the author [33] as "typeless"; with the only data type being the machine word, "C provides the fundamental flow-control constructions required for well-structured programs: statement grouping; decision making (if); looping (while, for and do); and selecting one of a set of possible cases (switch):" C uses pointers and has the ability to do address arithmetic. Functions may be separately compiled. No run-time reusage checking is provided by C.

Modularity as provided through function and data modules, however, no interfacing checking is performed between external modules. Data modules may be separately compiled.

There is no official standard for the C language.

1.4.2.1.2.7 PL/1 [30]

PL/1 was designed in 1965 by a committee of six individuals; three from industry and three from IBM. It was based upon FORTRAN, ALGOL, and Commercial Translater. It was intended to serve both scientific and commercial applications. It is used to provide support tools for the On-board Shuttle project; namely of the system programming variety.

The language provides more facilities than any of the other candidate languages. It is complex; and probably for this reason has not been universally accepted. It is weakly typed. It is highly structured and provides modules which can be separately compiled. However, no interface checking is performed. No information hiding is provided. It provides tasking and exception handling. No range checking is provided.

PL/1 is a standard language; but, its compilers are not formally validated.

1.4.2.1.2.8 FORTRAN 77 [14,30]

FORTRAN was developed by IBM in 1954 to address the scientific computing problem. It is the second most widely used language in the world; COBOL being the most widely used. It has undergone many evolutions; the latest one resulting in a version called FORTRAN 77.

An IF, THEN, ELSE structure has been added to the language to make it more structured. In addition, an ability to handle character strings and a capability to more easily open and close files has been added [30].

FORTRAN 77 still embodies all of the old language features. They do not all have to be used, but can be confusing to a person learning the language. Also, FORTRAN lacks portability because of the nonstandard extensions in the various implementations. FORTRAN 77 is weakly typed, provides no constructs for detecting run-time errors and has no information hiding capabilities. In fact, the shared use of COMMON has the opposite effect. The language does provide modular capabilities; but, provides no checking of the interfaces between modules.

FORTRAN 77 provides no real-time tasking constructs, but these can be realized with the use of the extension ISA 61.1. Also, it provides no low level I/O handling function or absolute addressing capabilities.

FORTRAN's main advantages are its simplicity, acceptability, and the existence of a large library of useful routines.

FORTRAN 77 is an ANSI standard, as were its previous versions. However, no strict control is applied to insure consistency among the implementations, as is being performed for Ada and JOVIAL 73.

1.4.2.1.3 Projected Capabilities

At this time the most suitable general purpose programming language for the On-board Space Station applications appears to be Ada. It fulfills all of the requisites needed for developing application and system type programs for the On-board Space Station and does it well. Its features, which are well formulated, are those of a modern programming language. The language is a mature language that has been reviewed by thousands of language experts here and abroad and is now an ANSI standard language. No changes will be allowed in it until some time in 1988, if then. The implementations are guaranteed to conform to the language specification by the independent validation and repeated validation processes instituted by the DOD. As such, users of Ada can look forward to having a stable and functionally capable language.

Of more importance, even if all of the languages were of equal quality, is how well the language will be accepted, and how well the language accommodates and fosters modern technology concepts and methodologies. These have importance in the availability of a wider range of products that would be useable on a project and the enhancements in software engineering that would be fostered by a large usage base. We see Ada as being the basis for most of the new technological and methodology advancements. The reasons for this are the facilities and functions preceded by the Ada language and the 43 million dollars being spent by DOD in current Ada based initiatives such an, STARS and SEI. We see Ada being required on all new DOD embedded computing programs starting after 1 July 1984. We note that there are currently 37 DOD programs using Ada, representing some 307 million dollars.

Additionally, there are 120 new DOD programs in the works that will use Ada, representing some 663 million dollars. By fiscal year 1990 it is estimated that there will be 1.30 billion dollars worth of new projects that will require Ada. (These estimates of DOD programs were supplied by Major Al Kopp at the AdaJug – SigAda Conference of 28 November 1984.) We see Ada being promoted for use in commercial type applications in the DOD. (Directive 5000.31 is being reopened to consider the inclusion of non-mission critical applications). In addition, Ada is being used to rewrite one of the very largest of the DOD programs (WWMCCS, having approximately, 21 million lines of COBOL code). As a result of this DOD impetus, it is speculated that in the not too distant future, Ada will be one of the major programming languages for all types of applications. Ada will probably never be as widely used as COBOL (over 60% of the world's programs are written in COBOL). But, if DOD's influence can make COBOL. a mediocre language, such a success, one wonders what it will do for Ada, an eminently superior language.

However, the DOD interest in Ada is not the only interest; multiple commercial establishments have expressed interest in the language and a considerable number of software houses have become involved in producing Ada compilers, software tools, and various forms of Ada packages. Fourteen Ada compilers were validated by the end of 1984; only one of which was directly supported by DOD. There were 24 other identified compiler implementations in progress as of September 1984 [4]. Many more products are being designed by these vendors, not only for the possible financial rewards, but for the opportunity to be in the forefront of modern technology.

1.4.2.1.4 References

1. "Rationale for the Design of the Ada Programming Language" J D Ichbiah, et al, ACM Sigplan Notices, Vol 14, Nbr 6. June 1979

2. "Reference Manual for the Ada Programming Language, ANSI/MIL-STD-1851-1983", United States Department of Defense, 17 February 1983

3. "Software Engineering with Ada", Grady Booch, 1983

4. "Validated Ada Compilers", ACM Ada Letters, Vol IV Issue 3 November, December 1984

5. "Abstract Data Types in Ada", William F Appelbe, J. Pascal Ada, v 3 n 1, Jan-Feb 1984 p 26-29

6. "Ada Interface", David M. Bulman, J. Pascal Ada, v 2 n 2, Mar-Apr 1983, p 22-24

7. "Ada Interface", David M. Bulman, J. Pascal Ada, v 2 n 6, Nov-Dec 1983, p 18-19

8. "Ada and Its Lessons for HAL/S", Bruce Knobe, Intermeterics Inc., Memo No. 08-79, 10 Oct 1979

9. "Ada and NIL: A Comparison of two Models of Structuring Software Systems", Robert E. Strom and Shula Yemini, IBM Research, Peter Wegner, Brown University, Proc. of the 18th Hawaii International Conf. on System Sciences, 1985

10. "Ada Decision Matrix", D. B. Baker, Aerospace Corp, Aerospace Report No. TOR-0084(4453-06)-1, 23 March 1984

11. "Ada Goes to Work", Defense Electronics, v 14 n 7, Jul 82

12. "Ada - Not Just Another Programming Language", R. M. Blasewitz, RCA, RCA Eng, v 29 n 1 Jan-Feb 1984, p 23-31

13. "Ada, A Standard Programming Language for Defense Systems, William E. Carlson, DOD, Signal p 25-27 38, Mar 1980

14. "AIPS Language Trade Study", Alton A. Knosp, Jr., CSDL, Report to JSC/NASA, Number CSDL-C-5964, March 1984

15. "A Comparative Evaluation of Ada and Euclid:, D. F. Athersych, et al, INFOR, v 21 n 3, Aug 1983, p 157-176

16. "Concurrent Programming in the Ada Language: The Polling Bias, N. H. Gehani and T. A. Cargill, Bell Laboratories, Software-Practice and Experience, V 14 N 5, May 1984, p 413-427

17. "Design of Ada Systems Yielding Reusable Components: An Approach Using Structured Algebraic Specification", S. D. Litvintchouk and A. S. Matsumoto, IEEE Transactions on Software Engineering, V SE-10 N 5, Sep 1984, p 544-551

18. "DOD's Common Programming Language Effort", D. A. Fisher, DOD Report, 1980

19. "HAL/S Versus Ada - Tradeoff Study for the Space Station Program", K. Koehler, et al, Intermetrics Report IR-TX-049 to JSC/NASA 1 Apr 1983

20. "The Implementation and Use of Ada on Distributed Systems with High Reliability Requirements:, J. C. Knight, S. T. Gregory, and J, I. A. Urquhart of the U. of Virginia, Report No. UVA/528213/AMCS84/IC4 submitted to LRC/NASA, February 1984

21. "Flight Languages - Ada vs. HAL/S", Bruce Knobe, Intermetrics, Inc., no date

22. "Introducing Ada", W. E. Carlson, L. E. Druffel, D. A. Fisher, W. A. Whitaker, Proceeding of the 1980 ACM Annual Conference, p 263-269, Oct 27-29, 1980

23. "Is Ada the Answer?", D. M. Bulman, Pragmatics, Inc., The Yourdon Report, V6-6 N7-1, (1981, 1982)

24. "Modular Software Construction and Object-Oriented Design Using Ada", R. R. Sincovec, R. S. Wiener, Univ of Colorado, J. Pascal Ada Modula 2, V3 N2, Mar-Apr 1984, p 29-34 48

25. "An Operating System for Future Aerospace Vehicle Computer Systems", E. C. Foudriat, et al, LRC/NASA, NASA Technical Memorandum 85784, p 8-10 30-31

26. "Pascal, Ada, and MODULA-2, David Coar, Byte, August 1984 p 215-219 222-232

27. "Program Overview - Ada", Peter Fonash, AJPO, SIGNAL, July 1983, p 27-31

28. "Safety Analysis of Ada Programs Using Fault Trees", N. G. Leveson and J. L. Stolzy of the Univ of California, Irvine, IEEE Transactions on Reliability, V R-32 N5, Dec 1983. p 479-483

29. "Seeding the Ada Software Components Industry", Ken Bowles of Telesoft, Proceedings of the Annual Conference on Ada Technology held at Hampton, Va. 27-28 Mar 84, p 125-128

30. "Selection of a General Purpose Language and a Real-Time Language Suitable for Shipboard Data System III", S. R. Barnum of the National Ocean Service, Report No. PB84-180892, Jan 1984

31. "Software Development Methodologies and Ada", AJPO, Three papers:

- o "Ada Methodologies: Concepts and Requirements", A. Wasserman of UCSF and P. Freeman of UC Irvine, Nov 1982
- o "Ada Methodology Questionnaire Summary", M. Porcella and P. Freeman of U C Irvine, and A. Wasserman of UCSF, Nov 1982 "Comparing Software"
- o Comparing Software Design Methods for Ada: A Study Plan" P. Freeman and A. Wasserman, Nov 1982

32. "Solve Process-Control Problems with Ada's Special Capabilities", G. Booch of the USAF Academy, EDN, June 23, 1982, p 143-152

33. "The C Programming Language", B. W. Kernighan and D. M. Ritchie, Prentice Hall, 1978

34. "Transitions to Ada: an Incremental Approach", D. H. J. Brown of Logica Limited UK, The Computer Journal, V 27 N 1, Feb 1984, p 37-41

35. "What is Ada", R. F. Brender and I. R. Nassi of DEC, IEEE, 1981

36. "FSD Software Standards, Manual 33-09", IBM/FSD (IBM Internal Use Only)

1.4.2.2 User Oriented Control Language

1.4.2.2.1 Description

This paper presents the user's interface to the Space Stations onboard DMS. A user is defined as either: 1) an operator interfacing with the core (housekeeping) Space Station DMS elements or 2) an operator managing and controlling a payload. It is a general consensus that the user's interface to the Space Station DMS should be in the form of a precisely defined, user friendly, English like language. The Space Station Phase B RFP describes the UIL: "The DMS shall support a user-friendly language for the man/machine interface. The language shall be capable of interfacing between man and machine for communications, display generation, monitoring, checkout and control during all phases of development and operations." See reference [4]. In the same document, the SDE definition references the User Interface Language (UIL): "a standard user-friendly language for interfacing users with Space Station ground and flight computer systems."

The scope of the language should extend through all aspects of user involvement with the Space Station program. From factory or laboratory level testing, through integration level testing, to on-orbit testing, integration and interfacing, the general user should be supported by a single language environment. This single user oriented language will ease the operator's transitions through the various steps in the development path from concept to on-orbit operation.

A NASA wide committee (ad hoc committee for Space Station User Interface language) has researched requirements for a UIL for Space Station and has made recommendations for defining requirements for a new language for the Space Station user interface. The resulting UIL environment will minimize total life cycle costs for development of test and integration procedures for both Space Station users and core systems developers. The UIL environment would be more than just operator commands to the on-orbit DMS. The language needs to have the following characteristics:

- English like: easy to learn, use and read.
- Useful for crew, scientists, and engineers.
- Provides real time interactive use as well as preplanned program development, test and execution like a general purpose programming language.
- Support on-orbit and ground integration, test and operations:
  - o Manufacturing development test
  - o Pre-launch integration
  - o Pre-launch checkout
  - o Post-launch checkout
  - o Ground monitoring and control
  - o On-orbit integration and testing
  - o Operation functions
  - o On-orbit maintenance and repair testing

Experience has shown that there is a great deal of functional overlap between real time operator interaction with a H/W and S/W system such as the Space Station DMS may require, and integration and testing functions which take place during the development of such systems. This is the basic justification for a UIL with such a broad scope. A UIL of this scope will necessitate a complex off line development environment, presumably in the Space Station SSE, and on-line environments (or target environments) ranging from small single processor checkout system in the factory or lab to the full up on board core and customer distributed systems.

Technology transparency is another key feature of the UIL. Both the off-line and on-line UIL environments must be as independent as possible of the processing hardware that they execute in and the hardware that they are controlling or testing. In an on-line environment, transportability to different processors may be a requirement since it is unlikely that all checkout facilities and the onboard DMS will use the same type processors.

The following is a summary of other requirements for a UIL. These have been analyzed in great detail in other high order language studies (see references). These requirements will be referred to in the next section which will characterize various existing test and integration type languages.

- Command and monitor functions
- External interface methodology
- Control of the system under test
- Accurate timing functions
- Ability to respond to external interrupts
- Graphics, output and input functions, interactive displays
- General "programming language" type functions:
    - o arithmetic, logical and relational operations
    - o data manipulation (shift, rotate)
    - o transcendentals (SINE, COSINE)
- Procedural control - begin, end, perform, terminate, rendezvous
- Conditional execution - if-then-else, case
- Etc.

The UIL type languages that are discussed are:

- Atlas
- GOAL
- SCOL
- STOL
- Ada

1.4.2.2.2 Options Characterization

Many languages have been analyzed by NASA and contractor studies for applicability to the user interface and integration and test type functions listed above. For various reasons all existing languages have proven unsatisfactory and a new language called SSOL (Space Stations Operation Language) is being defined. See references [4][5]. Attributes of many languages are being incorporated into SSOL to draw from past experience. The following summarizes the problems with existing languages.

- ATLAS - ATLAS has several positive factors. It is a very mature language and has maintained an "English language" type syntax. Its lack of an external interface methodology however, causes it to be heavily "procedure/test" interdependent. That is, changes to external hardware configurations (H/W addresses or attributes) require program changes.

- GOAL – GOAL is a readable, English-like language with many other attributes of the UIL. GOAL is designed for integration, test, and control in a distributed environment. It has an external interface methodology in which the GOAL application programs are totally isolated from H/W configuration changes. GOAL however, has become very oriented to the Shuttle Launch Processing System and contains syntax, real time constructs and other characteristics which would prohibit it from being used as a Space Station UIL.

- SCOL – SCOL is an effort by the IEEE ATLAS committee to standardize a language for test and operations. It is in the design phase and still to early to accurately analyze.

- STOL – STOL has the right orientation for a UIL. It can be procedural or interactive and is easily written and learned. It is hardware independent. It is an interpretive language which eliminates the need for any version of the procedures other than the source language. The limitation of STOL is its scope. It was designed for a small, centralized, serial processing system.

- ADA – It is felt that Ada is not oriented to the problem area to be addressed by the UIL. It is oriented towards experienced programmers for systems programming. Some qualities of the Ada Programming Support Environment (APSE) are intended to be UIL characteristics: a comprehensive set of development tools, standardization of the language, hardware independence and reliability.

What is being recommended as a result of these studies is that a new language be defined for the Space Station UIL. It should be based on a GOAL type syntax and incorporate positive qualities of all languages studied. It should be executable in an interactive mode or procedural (compile and execute) type mode. It should have an external interface methodology which isolates the procedures from the hardware specifications.

1.4.2.2.3 Projected Capabilities

A Space Station UIL does not exist and it appears that one will be designed. This design process will likely culminate in a set of requirements to be implemented in the SSE. The first implementations will be required to coincide with initial Space Station hardware and software testing. The language environment will be expected to support for the life of the Space Station.

1.4.2.2.4 References

[1] NASA Trade Study: High Order Languages, Space Station Operations Working Groups, 7/20/83

[2] Space Station High Order Language Study, IBM Corp., Cape Canaveral, FL, January 1984.

[3] Report of the ADHOC Committee for Space Station User Interface Language, July 9, 1984.

[4] Space Station Definition and Preliminary Design - Request for Proposal, 9/15/84

1.4.3 DELETED

1.4.4 Advanced Tools

1.4.4.1 Automated Code Generation

1.4.4.1.1 Description.

Automated Code Generation or automatic programming (AP) is the automation of some part of the programming process. To an assembly language programmer, a Fortran compiler is an automated code generator. The forces which led to the development of high level languages we have today are now leading us to the next level in automatic programming.

These new systems are based on artificial intelligence research. They not only generate code but perform many other functions to aid the programmer. The options which will be addressed here are:

- The Programmers Apprentice
- PSI
- SAFE

1.4.4.1.2 Automated Code Generation Options Characterization

PROGRAMMERS APPRENTICE

The Programmers Apprentice is an interactive tool for helping programmers program. The intent is that the programmer will do the difficult parts of design and implementation, while the apprentice acts as a helper and critic, keeping track of details and assisting the programmer in the documentation, verification, debugging and modification of his program. To help, the Apprentice must be able to understand what is going on. This has been accomplished by the design of a representation called a plan, for programs and for knowledge about programming that serves as the basis for the understanding. Developing plans and reasoning about them are the central activity of the Programmers Apprentice. Below are some basic areas in which the Apprentice can assist a programmer: References [1], [2]

1. Documentation. One of the primary services the Apprentice provides is automatic, permanent, and in-depth documentation of the program. It remembers not only explicit commentary supplied by the programmer with the code, but also a substantial body of derived information describing the logical structure underlying the program, such as the dependency relationships between parts of the program.

2. Verification. The development of a program is accompanied by the construction of a sequence of plans at various levels of abstraction. At each step, the Apprentice attempts to verify that the current plan is both consistent and sufficient to accomplish the desired goal. As more information is specified, the Apprentice's reasoning about these plans approaches a complete verification of the program.

3. Debugging. Any discrepancy between the Apprentice's understanding of the programmer's intent and the actual operation of the program is reported to the programmer as a potential bug.

4. Managing modification. Perhaps the most useful aspect of the Apprentice is that it can help a programmer modify his program without introducing new bugs. Based on its knowledge of the logical relationships between parts of a program; the Apprentice is able to determine what parts of a program can be affected by a proposed change and how they can be affected. It can use this information to warn the programmer of impending difficulties.

PSI

The goal of PSI was the integration of the more specialized methods of automatic programming into a total system. This system incorporates knowledge engineering, model acquisition, program synthesis, efficiency analysis, and specification by examples, trace or interactive natural language dialog.

The PSI system deals with programs in the general class of symbolic computation, including list processing, searching and sorting, data storage and retrieval, and concept formation programs. It is a knowledge-based system organized as a set of closely interacting "experts." PSI is comprised of the following "experts":

The PARSER/INTERPRETER expert handles the acquisition phase. It parses sentences and interprets these parses into less linguistic and more program oriented terms. This expert handles a very large English grammar and has knowledge of data structures (sets, records, etc.) control structures (loops, conditional, etc.) and more complicated algorithm ideas.

The DIALOGUE MODERATOR expert models the user, the dialogue, and the state of the system and selects appropriate questions and statements to present to the user. It determines whether the user or the system has the initiative and on what level and what subject, and attempts to keep PSI and the user in agreement on the current topic. The DIALOGUE MODERATOR expert decides which of the many questions being asked by the other experts should be passed on to the user.

The EXPLAINER expert phrases questions in terms that the user finds meaningful, in terms related to the problem domain and the previous sentences in the dialogue.

The EXAMPLE/TRACE expert allows specification by traces and examples, because these are useful for inferring data structures and simple spatial transformation. This expert handles simple loop and data structure inference.

The TASK DOMAIN expert uses knowledge of the application area to help the PARSER/INTERPRETER and EXAMPLE/TRACE experts fill in missing information in the program.

The PROGRAM-MODEL BUILDER expert applies knowledge of what constitutes a correct program to the conversion of the program into a model which will be used to actually create the code by the CODE expert. It also analyzes the model for consistency.

The CODING and EFFICIENCY experts are responsible for the synthesis phase. The CODING expert's knowledge base contains rules that transform parts of a program description to forms closer to the target language. It is the goal of the EFFICIENCY expert to guide the choice of the different rules, so that an efficient target-language implementation eventually results. References [1], [3]

SAFE

The SAFE system accepts a program specification consisting of preparsed English, with limited syntax and vocabulary, including terms from the problem domain. These may be ambiguous, and may fail to provide all the information required in a formal specification. SAFE resolves these ambiguities using a large number of built in constraints, any specified constraints from the problem domain, and interaction with the user. SAFE then creates a high level complete program specification.

The SAFE system views the task of automatic programming as the production of a program from a description of the desired behavior of that system. There are four major differences between a conventionally specified program and a program described in terms of its desired behavior. References [1], [4]

1. Informality: The behavioral description is informal. It has ambiguities and partial constructs.

2. Vocabulary: The primitive terms in the behavioral description are those of the problem domain. General purpose programming languages, on the other hand, provide a primitive vocabulary that is independent of particular problem areas.

3. Executability: It is possible, and sometimes desirable, to describe behavior in terms of relationships between the desired and achieved states of a process, rather than by rules that specify how to obtain a desired state.

4. Efficiency: Conventionally specified programs contain many details of operation beyond the desired input/output behavior. Among these are data representation, internal communications protocols, etc.

1.4.4.1.3 Projected Capabilities

These tools are still in the academic world. Much refinement and experimentation are required before they will be adopted by industry. By 1987, no major changes are anticipated. By 1995–2000, they may be making an impact. For the Programmer's Apprentice, simple program synthesis and efficiency issue are to be addressed in the future as well as strengthening existing capabilities.

For the PSI system, a new language "V" has been developed and is being used to describe an environment called CHI which is to provide not only a knowledge-based synthesis system, but also a supportive, high level programming environment.

For the SAFE system, a reformulation of the SAFE system is underway to correct certain limitations. Also, the system is being scaled up to handle both larger specifications and to handle formalization of incremental informal specifications.

1.4.4.1.4 References

[1] Avron Barr and Edward Feigenbaum, The Handbook of Artificial Intelligence, Heuristech Press, Stanford, CA., 1982

[2] Rich, C., and Shrobe, H.E., "Initial Report on a LISP Programmer's Apprentice," IEEE Transactions on Software Engineering, SE-4(6):456-467

[3] Green, C., 1979, "Results in Knowledge Based Program Synthesis," IJCAI 6, 342-344

[4] Balzer, R. M., Goldman, N., and Wile, D. 1977, "Informality in Program Specification" 1977 IJCAI 5, 389-397 4

1.4.4.2 Automated Code Evaluation/Verification

1.4.4.2.1 Description

Code evaluation and verification can be divided into 3 main levels: unit testing, integration testing, and system testing. Each level has in general the following phases: planning, test case setup, test execution, test analysis and test result reporting. Also each level has a set of tools to aid the process. These are tools such as logic flow graph generators, data flow graph generators, complexity measuring tools, stub/driver generator, test data generator, source level debugger test design language, performance monitor tools, data logging and reduction tools, and symbolic execution tools. Reference [1]

Many of the above tools are being automated in advanced programming environments. One significant tool is the symbolic debugger. This tool symbolically executes the program under test. Here the tool simulates the program execution with symbolic values placed in the program's variables. Two such tools described here are:

- EFFIGY
- SELECT

1.4.4.2.2 Options Characterization

EFFIGY

EFFIGY is an interactive symbolic execution system for testing and debugging programs written in a simple PL/I style programming language. The language is restricted to integer valued variables and vectors (one dimensional arrays). It has many interactive debugging features including execution trace, break-points, and state saving and restoring. Reference [2]

SELECT is an experimental system for assisting in the formal systematic debugging of programs. It is intended to be a compromise between an automated program proving system and the current ad hoc debugging practice. SELECT systematically handles the paths of programs written in a LISP subset that includes arrays. For each execution path SELECT returns simplified conditions on input variables that cause the path to be executed, and simplified symbolic values for program variables at the path output. The users can insert constraint conditions, at any point in the program including the output, in the form of symbolically executable assertions. Reference [3]

1.4.4.2.3 Projected Capabilities

These and other automated test tools will become more common and effective in the near future. As Ada matures, automated test tools environments will become very robust. Transportability among Ada environments will greatly aid the development of tools.

The EFFIGY system is currently experimenting with "test path-managers" which would embody some heuristics for automating this process, exhaustively exploring all the "interesting" paths. The EFFIGY system is also working on practical methods for dealing with more advanced programming language features.

1.4.4.2.4 References

[1] David Hamilton, IBM FSD Houston, "SDE TEST and Analysis Function", January 1985

[2] James C. King, "A New Approach to Program Testing," IBM Thomas J. Watson Research Center

[3] Robert S. Boyer, Bernard Elspas, Karl N. Levitt, "SELECT—A Formal System for Testing and Debugging Programs by Symbolic Execution", Computer Science Group, Stanford Research Institute, Menlo Park, CA 94025

1.4.4.3 Expert System Builders

1.4.4.3.1 Description

Expert system builders are the first substantive artificial intelligence (AI) products to reach the marketplace. There are about a dozen products which allow non-AI programmers to build expert systems. Normally included in these packages are an inference engine and tools for building a knowledge base.

Building a knowledge base implies specifying a sequence of IF-THEN rules, giving examples of decisions or providing lists of items and their characteristics. The two main types of knowledge specification techniques are rule-based and frame-based. Rule-based reasoning represents knowledge in the form of IF-THEN rules while frame-based representation classifies objects and their attributes in a semantic network.

The following expert system builders will be discussed here as examples of the products available:

- KEE
- ART
- PRISM

1.4.4.3.2 Options Characterization

- KEE

  KEE (Knowledge Engineering Environment) from Intellicorp is a general purpose builder which uses both frame-based and rule-based reasoning to build its knowledge base. KEE uses object oriented programming. An object is an entity representing a collection of information. Objects are organized into classes and each object is associated with characteristics called attributes. In KEE objects called "units" have attributes called "slots". Object-oriented programming allows frame based representation. Many people, however, find it harder to work with frames than rules. Rules are simple and direct, and they best represent the procedural knowledge of a domain.

KEE runs on XEROX series 1100 machines, the Symbolics 3600, LISP Machines Inc's own LISP units, and the Texas Instruments' Explorer. The price is $60,000 for the development kit of which half goes for training and support. Reference [1]

- ART

ART (Automated Reasoning Tool) from Inference Corp is the most sophisticated and expensive tool available. ART combines both rule-based and frame-based reasoning. ART has a built-in mechanism to process and represent a large number of possible alternatives simultaneously. ART uses a blackboard mechanism to process "view points". These are views that rules have of the knowledge. Viewpoints allow ART to chart alternative courses of action called "hypothetical worlds." This means ART can consider "what-if" rules as well as if-then rules.

ART is available in the Symbolics 3600, LMI Lisp Machines, and VAX/VMS Lisp. Price is $100,000. Reference [1]

- PRISM

PRISM (PRototype Inference SysteM) is an IBM general purpose rule-based expert system builder. It has two operating modes. Client Mode (for users) and Builder Mode (for system development). Rules are written in a very natural language. The system allows builders and users to deal with uncertainty and to ask for how, why and what type explanations.

PRISM is designed for the IBM VM/370 architecture. No price is available as the program is not currently a formal product. Reference [2]

1.4.4.3.3 Projected Capabilities.

"Industrial strength" expert system building tools began to appear on the market in 1984. As a result, the production of large, complex expert systems is becoming economically viable for a growing number of industrial applications. Further refinement and extension of these tools in the next year or two will probably lead to the burgeoning of expert system applications across the industrial spectrum. Two- and three-fold improvements in capability can probably be expected for expert system builders over the next few years, opening up the production of expert systems to the vast numbers of companies with limited programming resources and capabilities.

1.4.4.3.4 References

[1] Richard Geering, "Do-it-yourself Development Tools Speed AI Applications," Computer Design, December 1984, 29-39

[2] Larry Pennington, IBM FSD Houston, "PRISM building tool description", February 1985.

1.5 DELETED

1.6 ARTIFICIAL INTELLIGENCE

This report describes within the context of the SSDS the implementation technology and the applications options of the computer science of artificial intelligence. SSDS applications are specified throughout section 1.6.2, and a high-level summary is provided in section 1.6.3.

Artificial Intelligence (AI) is a branch of computer science that seeks to understand and to model intelligent behavior with the aid of computers. Intelligent behavior involves thinking about objects in the environment, how objects relate to each other, and the properties and uses of such objects. AI encompasses several fields including image and speech recognition, natural language software, expert systems and problem solving. This report presents options for all the AI fields, but the majority of the options describe applications in the latter two fields, expert systems and problem solving.

Robotics technology, being composed of several disciplines many of which are outside the scope of the SSDS, is not discussed within this report; however, the results of other on-going studies, such as the Advanced Technology Advisory Committee (ATAC) Reports, will be assessed as to their impact on the SSDS.

1.6.1 Implementation Technology

This section describes the current and projected technologies for the development of AI systems. Options are grouped in the following categories:

- Hardware
- Kernel Languages
- Support Environments

1.6.1.1 Hardware

1.6.1.1.1 Description

This category includes processors for the development and execution of AI systems. The options include:

- LISP Machines
- Fifth Generation Architectures
- General Purpose Machines
- Space-Qualified Processors

1.6.1.1.2 Option Characterization

1.6.1.1.2.1 LISP Machines

LISP machines are those which are microcoded in dialects of the LISP language. These machines are primarily single-user workstations, though capabilities for file sharing networking have emerged. They have architectural features for the manipulation of symbolic data, such as data tagging; large virtual memory; and LISP function calls. Their speed for the execution of LISP software can be up to 20 times the speed of general purpose machines. In general these machines offer an ideal environment in which to develop artificial intelligence applications. It must be pointed out, however, that the eventual target processor may be a conventional processor. It should also be noted that all of the LISP machines developed to date are of von Neumann architecture.

Three major companies have emerged as producers of LISP machines. They are Symbolics Inc., Xerox Corp., and LISP Machine Inc. (LMI). A fourth company, Texas Instruments (TI), is expected to begin production on a LISP machine in April 1985. Both Symbolics and LMI are small companies which evolved from efforts at MIT. Xerox's entry into the field was the result of development of wordprocessing machines. TI, the most recent company to show interest in LISP

machines, had previously acquired a percentage of LMI and built upon the LMI technology. The similarities of these machines are more striking than their differences. Each offers high-resolution, bit-mapped displays, with windows, and advanced editing and debugging capabilities. Table 1.6-1 summarizes the characteristics of these machines.

TABLE 1.6-1
LISP MACHINE CHARACTERISTICS

Nomenclature:	1108-105
Manufacturer:	XEROX
System Architecture:	Specialized processor and microcode to execute LISP. Optional floating-point processor.
Main Memory:	1.5 Mbytes expandable to 3.5 Mbytes.
Virtual Memory:	8 Mbytes.
Local Storage:	42 Mbytes rigid disk, 1.2 Mbytes Floppy disk. Optional 80 and 315 Mbytes rigid disk.
Software:	InterLISP-D with Smalltalk.
Communications:	10 MHz Ethernet. Optional RS-232C serial port. Optional parallel I/O port.
Display:	17" CRT, 1024 X 808 pixels
Cost:	$30,000 (approx.)

Nomenclature:	1108-115
Manufacturer:	XEROX
System Architecture:	Specialized processor and microcode to execute LISP. Optional floating-point processor.
Main Memory:	2.0 Mbytes expandable to 8 Mbytes.
Virtual Memory:	8 Mbytes.
Local Storage:	42 Mbytes rigid disk, 1.2 Mbytes Floppy disk. Optional 80 and 315 Mbytes rigid disk.
Software:	InterLISP-D with Smalltalk.
Communications:	10 MHz Ethernet. Optional RS-232C serial port. Optional parallel I/O port.
Display:	17" CRT, 1024 X 808 pixels.
Cost:	$40,000 (approx.)

TABLE 1.6-1 (CONT'D)
LISP MACHINE CHARACTERISTICS

Nomenclature:	1132
Manufacturer:	XEROX
System Architecture:	Specialized ECL processor and microcode to execute LISP.
Main Memory:	2.0 Mbytes expandable in increments of 2 Mbytes to 8 Mbytes.
Virtual Memory:	8 Mbytes.
Local Storage:	80 Mbytes rigid disk. Optional 315 Mbytes rigid disk.
Software:	InterLISP-D with Smalltalk.
Communications:	10 MHz Ethernet. Optional RS-232C serial port. Optional parallel I/O port.
Display:	17" CRT, 1024 X 808 pixels. Optional color display.
Cost:	$130,000 (approx.)

Nomenclature:	S3640
Manufacturer:	SYMBOLICS
System Architecture:	Specialized processor and microcode to execute LISP. Based on MIT CADR machine. Special 36-bit bus. Optional floating-point hardware.
Main Memory:	2.0 Mbytes expandable to 8 Mbytes.
Virtual Memory:	15 to 60 Mbytes.
Local Storage:	140 Mbytes rigid disk. Streamer tape cassette TC4S 1/4".
Software:	ZetaLISP, ZMACS editor, flavors, networking, and electronic mail.
Communications:	10 MHz Ethernet. Optional RS-232C serial port.
Display:	17" CRT, 1100 X 800 pixels. Optional color display.
Cost:	$60,000 (approx.)

TABLE 1.6-1 (CONT'D)
LISP MACHINE CHARACTERISTICS

Nomenclature:	S3670
Manufacturer:	SYMBOLICS
System Architecture:	Specialized processor and microcode to execute LISP. Based on MIT CADR machine. Special 36-bit bus. Optional floating-point hardware.
Main Memory:	2.0 Mbytes expandable to 30 Mbytes.
Virtual Memory:	15 to 60 Mbytes.
Local Storage:	167.5, 300, or 474 Mbytes rigid disk. Optional 474 Mytes rigid disks add-on. Streamer tape cassette TC4S 1/4" or TD80 1/2".
Software:	ZetaLISP, ZMACS editor, flavors, networking, and electronic mail.
Communications:	10 MHz Ethernet. Optional RS-232C serial port.
Display:	17" CRT, 1100 X 800 pixels. Optional color display.
Cost:	$90,000 (approx.)

Nomenclature:	LAMBDA
Manufacturer:	LISP MACHINES INCORPORATED (LMI)
System Architecture:	Specialized processor and microcode to execute LISP. Based on MIT CADR machine. Special 32-bit bus. Optional UNIX 68010 Co-processor. 37.5 Mbyte Multibus, and Nu bus.
Main Memory:	4.0 Mbytes.
Virtual Memory:	67 Mbytes.
Local Storage:	169 or 470 Mbytes rigid disk. Additional drives available. Optional 1/2" or 1/4" Streamer tape and reel to reel.
Software:	ZetaLISP, ZMACS editor, flavors, networking, and electronic mail.
Communications:	10 MHz Ethernet. Optional RS-232C serial port. Multi-bus cards.
Display:	17" CRT, 1024 X 800 pixels. Optional color display.
Cost:	$90,000 (approx.)

TABLE 1.6-1 (CONT'D)
LISP MACHINE CHARACTERISTICS

Nomenclature:	EXPLORER
Manufacturer:	TEXAS INSTRUMENTS
System Architecture:	Specialized processor and microcode to execute LISP. Based on MIT CADR machine. Special 32-bit local bus, and Nu bus.
Main Memory:	2.0 Mbytes expandable to 16 Mbytes.
Virtual Memory:	128 Mbytes.
Local Storage:	112 Mbytes rigid disk. Additional drives available. Optional 1/4" Streamer tape.
Software:	Common LISP, ZMACS editor, flavors, networking, and electronic mail.
Communications:	10 MHz Ethernet. RS-232C serial port. Parallel printer port.
Display:	17" CRT, 1024 X 808 pixels. Optional color display.
Cost:	$60,000 (approx.)

1.6.1.1.2.2 Fifth Generation Architectures

Progress in AI research and subsequent applications has been proportional to the increase in computing power and speed. Faster machines and cheaper memory have heralded advancements in AI. The next, or fifth, generation architectures feature massively parallel arrangements of VLSI circuits to vastly increase speed and memory power. Such architectures would provide AI systems with capabilities for concurrent pattern matching and evaluation of rule sets. Major projects for the development of the fifth generation computer include goals for the advancement of AI.

a. Japanese Fifth Generation Computer Systems

The Japanese Institute for New Generation Computer Technology (ICOT) was formed in April 1982 and united researchers from eight participating firms to work on a project called the Fifth Generation Computer Systems. The Ministry of International Trade and Industry (MITI) has funded the project at $500 million over ten years. Matching industrial funds are expected to bring total funding to $850 million.

The Japanese technology is to be geared toward the processing of symbolic data with the production of hardware and software for knowledge information processing system (KIPS). The hardware is to be microcoded in an extension of the AI language PROLOG. Applications are to be in the fields of expert systems, natural language systems, and robotics. Goals have been set for innovations in three main parts of expert systems: very large knowledge bases, problem solving and inference, and man–machine interfaces.

The prototype knowledge base subsystem is to handle thousands of rules and thousands of objects, a capacity comparable to that of current large expert systems. The goal is to develop the capacity for knowledge bases to handle tens of thousands of rules and one hundred million objects.

The prototype PROLOG workstation is to have a capability of performing one million logical inferences per second (LIPS). The goal for the inference supercomputer is to process one hundred million to one billion LIPS.

The goals for increasing the capacity of man-machine interfaces are equally ambitious and include the development of:

- a speech understanding system with a vocabulary of 50,000 words from a few hundred speakers with 95% accuracy that is capable of controlling a speech-activated typewriter;

- a question/answering system with a 5000+ vocabulary and 10,000+ inference rules;

- an image understanding system with a capacity of reading 100,000+ images;

- a machine translation system between English and Japanese with a vocabulary of 100,000 words and a 90% accuracy.

b. DARPA

In 1983, the Pentagon's Defense Advanced Research Projects Agency (DARPA) announced the "Strategic Computing" plan with a projected funding of $600 million by 1988. The results are to be a variety of new techniques for advancing supercomputing and artificial intelligence technologies for defense applications.

The plan calls for the development of special architectures to exploit concurrent processing of expert systems and for faster, denser VLSI microelectronics. Initial software funding will be applied to the research and development of generic capabilities in the areas of speech understanding, natural language processing, image processing, and rapid information search and retrieval from very large databases. Subsequent expert systems will be developed for applications that include:

- autonomous vehicles (military satellites, unmanned aircraft, submersibles, and land vehicles)

- pilot's expert associate, a "mechanized co-pilot"

- large scale battle management

- war gaming

c. Microelectronics and Computer Technology Corp.

The Microelectronics and Computer Technology Corp. (MCC), was founded by William C. Norris, head of Control Data Corporation. This research consortium of 19 U.S. high-technology companies began operations in Austin, Texas in 1983. The MCC's budget for 1984 was $30 million. Its budget will be $50 million for 1985 and approximately $65 million per year for 1986 and beyond. It is headed by retired Adm. Bobby Ray Inman and will employ about 350 researchers.

The research is divided into four programs:

- IC packaging for highly complex circuits, a six year program;

- software technology, a seven year program;

- VLSI/computer-aided design, an eight year program;

- advanced computer architectures, a ten year program.

The final program, advanced computer architectures, is the most ambitious. It consists of projects in AI knowledge based systems, data base system management, parallel processing, and human factors technology.

d. University Research and Development

Much of the credit for the current state of the art in artificial intelligence must be given to University researchers. The primary centers of research include: Massachusetts Institute of Technology (MIT), Carnegie-Mellon University (CMU), and Stanford University. These Universities, and several others to a lesser degree, have established strong programs for performing research. The MIT lab, headed by Patrick H. Winston, has been responsible for

the evolution of many of the current commercial LISP processors and for much of the supporting software. CMU and Stanford have led the field in the development of expert systems and related topics. The OPS-5 inference engine was developed under the direction of Charles Forgy at CMU. The Heuristic Programming Project, headed by Edward Feigenbaum at Stanford, represents several outstanding projects by the most respected researchers in the field.

e. Governmental Agencies

Several agencies within the U.S. have been involved with AI research for the last decade. These include: Argonne National Laboratories, Jet Propulsion Laboratories, Ames Research Center, Naval Research Laboratory, and Rome Air Development Center.

The work centered at Argonne Labs is concerned primarily with theorem proving and inference engines. Larry Wos has been leading an effort for the past several years there and is recognized as an outstanding researcher in this field.

The effort at JPL, headed by Leonard Friedman, has its origins in unmanned spacecraft. JPL has been responsible for the development of robotic systems and diagnostic expert systems used on deep space probes.

f. Private Industry

The most recognized companies for research and development in the private sector include: Rand Corporation, Xerox, Teknowledge Inc., Symbolics, and TI.

Rand has produced several expert systems and is probably best known for its production system, ROSIE. Xerox Palo Alto Research Center is recognized as one of the foremost research centers in AI. This center is the origin of Smalltalk, LOOPS, and LISP processors. Teknowledge is a newly organized AI consultant company that has gained much respect in the last two years. Symbolics is a spin-off company of research performed at MIT and has developed the most widely used commercial LISP processor. TI, the most recent entry into the AI venture, is developing LISP processors on a chip.

1.6.1.1.2.3 General Purpose Machines

Probably the best known of the general purpose machines used for development of artificial intelligence applications are Digital Equipment Corporation's (DEC) PDP 10 and PDP 20 series computers. To some extent the DEC VAX 11/780 computers have been used for this purpose but generally the multi-user environment is not suitable for the development of large scale efforts. The requirement of large memories and storage for AI applications is a discriminator against using general purpose computers. Even so, many of the major manufacturers of general purpose computers offer LISP as a high level language. LISP is even available on some mini- and micro-computers but using one to develop a serious AI application would be very challenging.

1.6.1.1.2.4 Space-Qualified Processors

Research is currently being undertaken by NASA's Ames Research Center, under the direction of Henry Lum, to develop a flight-qualified LISP processor. This is presently a joint venture between Ames and Symbolics. They are beginning with a S3640 processor, but Dr. Lum believes the end result will be a very different, much smaller machine. Major issues will be shock determination and real-time reaction.

Another alternative for space-qualified processors is to use general purpose processors that have already met the specifications for being space-qualified or will be qualified in the proper time frame. These general purpose computers would be targeted for the implementation rather than the development of the AI application.

1.6.1.1.3 Projected Capabilities

DARPA has been instrumental in the continuing development of AI technology both in the area of software and hardware. In August 1984, the U. S. Navy Electronics Systems Command awarded Texas Instruments a $6-million, 27 month contract, to develop a compact LISP machine, based on high-performance semiconductor technology. The work is being performed for DARPA as a key element in its Strategic Computing Program for embedding advanced symbolic

computing capabilities in military systems. The processor will be capable of executing a superset of Common LISP with major language extensions that support object-oriented programming and message passing. Under the contract, TI will develop a custom LISP processor chip in sub 2-micron CMOS technology using VLSI semiconductor design. The computer will incorporate high-speed static RAM (1.25-micron) and the VLSI chip will operate at speeds up to 40 MHz. The new chip is designed to provide 2 to 10 times the processing power of today's symbolic processors. Production is expected to begin in 1987.

The market for LISP machines is expected to grow dramatically in this decade. Sales have increased tenfold since 1981 to around 2000 machines or $100 million in 1984. By 1990, sales in the range of $1 billion to $2.5 billion are predicted.

The development supported by DARPA and other governmental agencies, development by the MCC, development by the Japanese, development by Universities, and development in the private sector are expected to provide necessary hardware to support the needs of the SSDS in both ground-based and onboard systems that may require symbolic processors.

1.6.1.1.4 References

Alexander, Tom, "The Next Revolution in Computer Programming," Fortune, October 29, 1984, p. 82.

DARPA Strategic Computing Plan for Revolutionary Advances in Machine Intelligence Technology, November 7, 1983.

Fahlman, Scott, "Computing Facilities for AI: A Survey of Present and Near-Future Options," AI Magazine, Winter 1980-1981, pp. 16-23.

Feigenbaum, Edward A. and Pamela McCorduck, The Fifth Generation: Artificial Intelligence and Japan's Computer Challenge to the World, New York, New American Library, 1984.

Inman, Adm. B. R., USN (ret), Chairman, President and CEO, Microelectronics and Computer Technology Corporation, (Address), Sixth Annual Conference on Computer Developments, University of Houston-Clear Lake, Texas, November 8, 1984.

Lum, Henry, NASA Ames Research Center, (Telecon), November 1, 1984.

Matthews, Lawrence E., Compact LISP Machine, (Briefing), Texas Instruments, Inc., Dallas, Texas, November 16, 1984.

Stotesbery, William D., Director, Government and Public Affaris, Microelectronics and Computer Technology Corporation, Austin, Texas, (Telecon), November 26, 1984.

TI Receives $6-Million Navy Contract for Compact LISP Machine, (News Release C-564), Texas Instruments, Inc., Dallas, Texas, August 6, 1984.

1.6.1.2 Kernel Languages

1.6.1.2.1 Description

This category includes the computer languages available for AI applications. The options are:

- LISP
- PROLOG
- Other

1.6.1.2.2 Option Characterization

1.6.1.2.2.1 LISP

Even though many dialects of LISP such as, MACLISP, FRANZ LISP, ZetaLISP, InterLISP, and most recently Common LISP, have evolved, LISP still remains the choice of most AI researchers and knowledge engineers.

LISP is a computer programming language that originated as a tool to facilitate AI research. LISP is designed to facilitate the representation of arbitrary objects and relationships among them. It also facilitates the modeling of procedural knowledge.

1.6.1.2.2.2 PROLOG

PROLOG is a high level language that was developed in France and is a popular language in Europe. A version of PROLOG has been chosen as the language for the Japanese Fifth Generation Computer Systems Project. In many respects PROLOG is quite different from LISP and compares more favorably with inference engines such as OPS-5. PROLOG uses pattern matching and backward inferencing in order to achieve desired goals. The syntax is terse and mathematical in nature. It is a highly extensible language. Few applications have emerged in the United States, and PROLOG has not yet achieved great popularity among AI researchers although it is now available on several main-frame, mini- and micro- computers.

1.6.1.2.2.3 Other

Several languages other than PROLOG and LISP have evolved over the last decade. These include such languages as SAIL, PLANNER/CONNIVER, and POPLER/POP2; but for the most part these have not been widely used. Some languages such as SUBTLE and FRL have been developed but are actually embedded in LISP.

Some have expressed interest in using Ada* as a language for the development of AI applications, but this concept has not been well received by researchers or knowledge engineers. A study released by SRI (May 1980) suggests that Ada is probably not suitable as an AI developmental language. This does not preclude the use of LISP environments for proof-of-concept prototyping of applications and the use of Ada for their subsequent implementation.

* Ada is a registered trademark of the U.S. Department of Defense Ada Joint Programming Office.

1.6.1.2.3 Projected Capabilities

The evolution of LISP should continue and some uniformity should emerge through the use of Common LISP. The use of object-oriented language should continue to flourish, as well as, the development of special supporting editing and graphics tools.

There still exist three camps of software development which show no promise of merging. The first group, the east coast group, evolved from MIT and encompasses the SYMBOLICS, LMI, and TI processors. This group endorses Common LISP and flavors. The second group, the west coast group, has origins at Stanford, XEROX and Rand Corporation, and has embraced InterLISP and Smalltalk. The third camp is centered in Europe and Japan and has selected PROLOG as their language of choice.

1.6.1.2.4 References

Dietz, David C., "Hybrid Programming Language Eases Applications of Artificial Intelligence," Defense Electronics, October, 1983, pp. 169-177.

Martin, William A. and Peter Szolovits, "Semantic Networks in LISP: Fundamental Concepts and a Specific Implementation," MIT Computer Science Laboratory, July, 1980.

Schwartz, Richard L. and Peter M. Melliar-Smith, The Suitability of Ada for Artificial Intelligence Applications, SRI International, May, 1980.

1.6.1.3 Support Environments

1.6.1.3.1 Description

This category provides a sampling of the support tools available for the development of AI systems. The options are:

- LISP Machine Support Environments
- Inference Engines

1.6.1.3.2 Option Characterization

1.6.1.3.2.1 LISP Machine Support Environments

The most evident feature of all of the LISP processors is the robustness of the software tools in the environment. This environment includes windows, mouse-sensitivity, message-passing, high-resolution graphics (including color) tools, editors, and debuggers. These tools provide the ideal environment for rapid prototyping of systems and interactive software development.

a. Windowing

One of the more unique and convenient features common to each LISP processor is its ability to have multiple windows on the same screen. This allows the user to monitor multiple processes or to view more than one file at the same time. The format of these windows is variable, and they may be configured either before or after creation.

b. Menu Selection

Another feature of the LISP processor is its menu selection ability. This feature utilizes the windowing feature of the LISP processor to create temporary windows containing items which may be selected using either the mouse or keyboard entry. This gives the ability to create smooth, convenient user interfaces to the system.

c. Flavors and Smalltalk

Flavors within the ZetaLISP environment and Smalltalk in the InterLISP environment are facilities which support object-oriented programming. Flavors and Smalltalk are abstract types. The objects are instances that are manipulated by sending messages, which are requests for specific operations. These systems provide a unique and powerful mechanism for declaring relationships.

Using flavors or Smalltalk, programs of great complexity can be built that still maintain the advantages of modularity and maintainability.

d. Text Editors

Most of the LISP processors offer a robust text editor. It is a real-time display editor. The text being edited is always visible, and commands are executed immediately. The editor allows users to switch between several files being edited. Special features for editing programs and for communicating with the LISP environment are provided.

The editors exploit the mouse and the graphics capabilities of the console display. The mouse can be used to issue certain commands and to point at a particular character or to graphically mark a region.

e. Processes

The LISP processor supports multi-task processing and has systems software designed for scheduling these processes. The task scheduler provides a number of services, including:

- Real-time processes, wired in main memory
- Fast response for interactive activities
- Background activities
- Priority setting under user control

A process can wait for any arbitrary condition to occur. To wait for a condition, a process passes the scheduler a waiting function. The scheduler periodically calls this function, and as soon as the function returns a true value, the process is allowed to proceed. From this, programmers can construct more complex multiprocessing control structures. Multiple tasks can be both run and displayed concurrently.

f. Graphics

The LISP processors have excellent graphics capabilities, with a screen resolution of nearly 1000 x 1000 pixels. This is augmented with a large variety of graphics primitives useful for constructing custom graphics. There is also a font editor for producing fonts (collections of graphic symbols) of any resolution and size. This feature aids in producing useful user interfaces with software packages. These graphics can be treated as arrays and manipulated as such, which allows interactive rotations and translations to be easily produced. There is also the capability to handle color graphics.

g. Debugging

As an aid for program development, LISP processors offer excellent debuggers. The debugger can be used in either a line or full screen mode. In the line mode, errors are detected and displayed, and options are presented for modifying data or code and allowing the program to continue rather than aborting. In the full screen mode, the debugger allows the developer to view not only the section in which the error appeared, but also the LISP primitive instructions and a listing of the recently executed commands. Using the mouse, values of any recently used variables or function definitions may be viewed or modified.

h. Networking

An extensive networking system exists for the LISP processor. This system enables CHAOSNET, ARPANET and ETHERNET networks to be linked into the machine. The communications software is integrated into the file system and other parts of the system such that files on any other system may be treated as if they resided on the host system. Some of the LISP processors are virtual file machines.

1.6.1.3.2.2 Inference Engines

The inference engine is a major part of an expert system and is the software mechanism by which the rules and data are utilized to reach a conclusion. The inference engine, which is often written in LISP, looks for "matches" or "hits" of the situation of a rule to be satisfied by the data from the data base. If the situation is satisfied (or true), then the inference engine causes the action to be performed. The primary interest in evaluating an inference engine is the efficiency of its algorithm in detecting the matches of the hypothesis.

The inference engine also determines the order in which rules "fire", i.e., the strategy for selecting these rules. It is frequently the case that several rules may be satisfied at the same time, and the order in which the rules "fire" influences the conclusion reached. Rules must be written with the strategy of the inference engine in mind. Furthermore, rules for one inference engine may not be suitable for another inference engine due to differences in strategy.

The rules of most inference engines are not in an "English-like" form but rather in a pseudo-English structure. Hence, there must be a translation from the logical form in English to the syntax of the inference engine.

The designer of the expert system has the option of creating his own inference engine or using one of the many inference engines that have been developed by both the academic and industrial community.

Some of the commonly employed inference engines are EMYCIN, ROSIE, OPS-5, YAPS, and AGE. Most of these have been evolved over a period of years by AI researchers. A few of these have been modified and offered to the public. Many can be obtained from the originators for a nominal processing fee.

a. EMYCIN. The EMYCIN inference engine is the result of many researchers working on it for a period of several years. The product that has evolved is a mixture of different ideas and "fixes". This product is also not well documented. Some of these difficulties are being resolved by Teknowledge, Inc., which has developed a commercial expert system kit called S.1.

b. ROSIE. The inference engine ROSIE, developed by Rand Corp., is one of the better documented and user friendly products. This product was developed in an InterLISP environment; thus, it must be adapted to the ZetaLISP environment of the Symbolics, LMI, and TI processors. Rand is currently working on a version suitable for the ZetaLISP environment.

c. OPS-5. OPS-5 is the culmination of more than ten years of research on inference engines at Carnegie-Mellon University. Like EMYCIN, it represents the effort of several researchers, and it also has many "fixes" to improve its performance. Likewise, the documentation is somewhat lacking. However, OPS-5 does have a "track record" of successes in R1 and other expert systems. Futhermore, it is available for all the major LISP processors, is relatively easy to use, and has an efficient search algorithm (Rete). Several vendors such as XEROX, DEC, Verac, and Smart Systems sell commercial versions of OPS-5 on a variety of processors. One of these versions, OPS-83, is an extension of OPS-5 that is said to overcome some of the difficulties of OPS-5.

d. YAPS. Yet Another Production System (YAPS) was developed at the University of Maryland. YAPS uses the same search algorithm and pattern-matching scheme as OPS-5, but improvements have been made on some of the inefficiency of the OPS-5 structure. Futhermore, YAPS is written in flavors and represents much less code than OPS-5.

e. AGE. AGE (Attempt to GEneralize), developed at Stanford by H.P. Nii and N. Aiello, is a tool for helping knowledge engineers design, build, and test different frameworks for expert systems. AGE permits the user to develop an expert system by using components (collection of AI support mechanisms) and frameworks (predefined configuration of components). The production rule component is composed of a rule-interpreter and a collection of rule strategies. AGE is less widely used than other expert system builders, probably because of its lack of useful I/O, data base construction, and explanation facilities.

1.6.1.3.3 Projected Capabilities

Several production system "kits" have appeared on the market in recent months to join those that have been developed in the academic community.

Intellicorp, of Menlo Park, California, has developed a production system kit known as the Knowledge Engineering Environment (KEE). KEE, patterned somewhat after LOOPS (developed by XEROX), is a set of software tools designed to assist system developers in building their own knowledge-based systems. KEE uses the concepts of object-oriented programming, frame-based knowledge representation, taxonomic inheritance, rule-based reasoning, data-driven reasoning, and LISP functional programming.

Another production system tool, developed by Inference Corporation of Los Angeles, is the Automated Reasoning Tool (ART). ART is similar in some respect to KEE but has its origins more closely aligned to OPS-5. Both of these systems provide the capability to quickly prototype applications and aid the knowledge engineer in developing expert systems.

Other lesser known products include: DUCK (Smart Systems), S.1 and T.1 (Teknowledge), Expert-Ease (Jeffry Perrone & Assoc.), CHI (Kestrel Institute), and TIMM (General Research Corporation).

This trend of developing software tool kits in order to make the application of AI more readily useable, is expected to continue. Unfortunately these systems still require some expertise in building expert systems and are not suitable for the novice. Futhermore, many have not yet been proven to be useful for building expert systems.

In the longer term, the MCC and Japanese Fifth Generation Computer Systems projects may produce products facilitating the building of expert systems. These products may include natural language systems, possibly including voice recognition, for the automatic generation of rule sets.

1.6.1.3.4 References

Alexander, Tom, "Computers on the Road to Self-Improvement," Fortune, June, 1982, pp. 148-160.

"Artificial Intelligence Research in the Heuristic Programming Project," Stanford University, June, 1983.

Buchanan, Bruce G. and Richard O. Duda, "Principles of Rule-Based Expert Systems," HPP-82-14, Stanford University, August, 1982.

Cashman, Mike, "The Debut of Second Generation Artificial Intelligence," Digital Design, December, 1983, pp. 82-84.

Clancey, William J., "Methodology for Building an Intelligent Tutoring System," HPP, Stanford University.

Forgy, Charles L., OPS5 Users Manual, Carnegie-Mellon University, Pittsburgh, Pennsylvania, 1981.

_____ "Rete: A Fast Algorithm for the Many Pattern/Many Object Pattern Match Problem, "Artificial Intelligence, 19 (1982), pp. 17-37.

Goldberg, Adele, "Introducing the Smalltalk-80 System," Byte, August, 1981, pp. 14-26.

Ham, Michael, "Playing by the Rules," PC World, January, 1984, pp. 34-41.

McDermott, John, "R1's Formative Years," AI Magazine, vol. 2, no.2.

Minsky, Marvin, "A Framework for Representing Knowledge," AIM 306, MIT AI Laboratory, June, 1974.

Rich, Elaine, "The Gradual Expansion of Artificial Intelligence," IEEE Computer, May, 1984, pp. 5-12.

Robson, David, "Object-Oriented Software System," Byte, August, 1981, pp. 74-147.

Scott, A. Carlisle, Randall Davis, William Clancey, and Edward H. Shortliffe, "Explanation Capabilities of Production-Based Consultation Systems," HPP-Memo 77-1, STAN-77-593, 1977.

van Melle, William, "A Domain-Independent Production-Rule System for Consultation Programs," HPP-79-7, Stanford University, 1979.

van Melle, W., A. C. Scott, J. S. Bennett, and M. Peairs, "The Emycin Manual," HPP-81-16, STAN-CS-81-885, October, 1981.

Weinreb, Daniel and David Moon, LISP Machine Manual, MIT AI Laboratory, July, 1981.

Winston, Patrick H., "Learning and Reasoning by Analogy: The Details," AIM 520, MIT AI Laboratory, May, 1980.

Xerox Learning Research Group, "The Smalltalk-80 System," Byte, August, 1981, pp. 36-48.

1.6.2 Applications

This section provides a survey of existing AI applications and a projection of growth. The applications are grouped into the following categories:

- Expert Systems and Problem Solving
- Image and Speech Recognition
- Natural Language Software

1.6.2.1 Expert Systems and Problem Solving

1.6.2.1.1 Description

A production system,or rule-based system, is a computer program. These programs are frequently written in LISP but are not limited to the LISP language. The characteristic that most typifies the production system is that the solution is based more on a heuristic approach rather than a deterministic approach.

A production system that captures the expertise of a human expert is called an expert system. The production system evolves into the expert system as it is

"trained" through codifying of the knowledge and cognitive processes of the expert(s) in a particular field. The code is often represented in the form of rules. These rules, which are often based on empirical data and heuristics, may be difficult to obtain. Frequently, the expert is unable to ascertain the methods that enable him to make decisions. The extraction of that information rests with the expert system designer, who is called a "knowledge engineer".

Typically, the knowledge engineer selects a data base structure, a rule base structure, and an inference engine that are suitable for the application. He then builds a prototype system with the rules extracted from the expert(s) for the application. The prototype system is applied to the application, and the expert critiques the results in an iterative fashion with the knowledge engineer modifying or adding to the rule set as applicable. This process continues with more complicated situations or pathological conditions with additional rules being added to the rule set until the expert is satisfied with the results.

Not all problems lend themselves to the expert system approach, but those that do frequently exhibit some or all of the following properties:

- Resists attempts to solve by conventional software.
- Uses heuristic or "rule of thumb" solutions.
- Complex, unwieldy logic.
- Unmanageable task.
- Unstable, constantly changing, evolutionary problem.
- Experts usually make decisions resulting in solutions.

Several expert systems have evolved in recent years particularly in the areas of Computer Systems, Education, Engineering, Fault Diagnosis,Geology, and Medicine.

The earliest efforts with expert systems began in 1965 at Stanford University under the direction of J. Lederberg, A. Feigenbaum, and B. Buchanan. The first system, called DENDRAL, was designed to imitate the organic chemist in finding the structure of organic molecules given the results of a mass spectograph. This program, which required 30-45 manyears to develop, is still in use today.

Another successful expert system is R1, developed by J. McDermott between 1978-81 for Digital Equipment Corporation. This system was designed to configure the VAX computer systems. R1 has subsequently evolved into XCON and is used on a routine basis by DEC.

The expert system GUIDON, developed by W. Clancy, teaches students by eliciting and correcting answers to a series of questions.

The best known of the diagnostic systems (non-medical) is DART, a joint effort of IBM and Stanford. This diagnostic-assistance tool is used in field engineering to aid in the diagnosis of computer hardware failures.

Two programs have evolved in the field of geology that deserve mention. The first is PROSPECTOR, developed by P. Hart and R. Duda, an expert system geological consultant that evaluates sites for potential mineral deposits. The second is DIPMETER, developed at Schlumbeger, a system for analyzing oil-well logs.

Several systems have been developed for medical purposes, mostly diagnostic in nature. Most prominent are MYCIN, for diagnosing bacterial infection, and PUFF for identifying lung disorders.

Areas of potential application for the SSDS include:

- Subsystem Control and Monitoring
- System Configuration
- Computer Programming and Computer Assisted Instruction

- Biomedical
- Fault Detection/Diagnosis/Correction
- Planning, Scheduling, and Logistics
- Modeling
- Distributed Data Base Management

1.6.2.1.2 Option Characterization

1.6.2.1.2.1 Subsystem Monitoring and Control

Prototypes have already sprung up at NASA-JSC and elsewhere demonstrating the feasibility of using expert systems for monitoring and control. The NAVEX (navigation expert system) developed by engineers at NASA-JSC, accepts simulated navigation telemetry data and monitors the health of onboard shuttle equipment such as the Inertial Measurement Units (IMU). This function is normally performed by NASA navigation experts during a mission where decisions are made that critically affect the mission. Although there are no plans to replace the human in this situation, the feasibility of such a replacement has been demonstrated.

All types of data may be monitored, both ground and onboard. This includes the state and status of all subsystems. Expert systems may project parameter trends; recognize patterns; detect, predict and explain anomolous conditions; recommend courses of action; and implement courses of action. The capabilities of the subsystem monitoring and control expert systems may be limited at IOC by the speed of their response times. They may only be recommended for functions of criticality 3 (as defined in the SSDS Task 1 Functional Data Sheets) or higher, i.e. for those functions with recovery times of 10 or more minutes. They may also be used to supplement other automated or human monitoring functions. Some of the SSDS functions to be studied for their application are:

2.5.3 Support OTV Operations

2.5.4 Support OMV Operations

4.1 Operate Avionics Systems

4.2 Operate Non-Avionics Core Systems

4.3.4 EVA Support

4.5.1 Core Systems Status Monitoring

4.5.2 Customer Systems Status Monitoring

5.1.2 Flight Resource Management (Facility Status)

5.2.2 SSCC Resource Management (Facility Status)

5.2.4 Global Facilities Management

5.3.2 Satellite Center Resource Management (Facility Status)

5.4.2 DHC Resource Management (Facility Status)

5.5.2 Development Support Resource Management (Facility Status)

1.6.2.1.2.2 System Configuration

The feasibility of expert systems for system configuration is demonstrated by the success that DEC has had with the system XCON. This system, which has in excess of 4,000 rules, successfully configures various computer systems manufactured by DEC, even when incorrect or incomplete data is submitted by buyers.

System configuration expert systems would be valuable in managing the complexity of the SSDS components. Specific functions for further study are:

1.3.3 Data Distribution Routing

2.5.5 Customer Payload Checkout/Service

2.6 SS Payload Equipment Checkout and Servicing

4.x.x.x.x Device Management

5.2.4 Global Facilities Management

5.1.2.6 Reconfigure/Disconnect Payloads and Core Systems

5.x.2.4 Configure Data Processing Equipment

6.x.1 Configure System 'x' Simulation

1.6.2.1.2.3 Computer Programming and Computer Assisted Instruction

Research is being done in this area by the University of Texas on a programmer's apprentice system which aids the programmer in developing and debugging his programs.

Schlumberger has developed a system known as PHI-O which permits an expert to develop programs for oil-well logging analysis simply by expressing quantitative relationships.

Other areas in which research has resulted in useful products include automatic code generation for data base query systems. Several commercial products are available which include this capability. See section 1.6.2.3.2.

Applications within the SSDS for computer programming systems fall within the software development functions and for computer assisted instruction within the training functions. Specific functions are:

6.8 Develop Training Exercise Configuration
6.9 Conduct Training Exercise
6.10 Develop Software

1.6.2.1.2.4 Biomedical

One of the most successful areas for expert systems has been in the biomedical sciences. This may be attributed to the wealth of heuristics used in this area and the willingness of experts to participate in the technology transfer. Systems such as INTERNIST, CADUCEUS, MYCIN, ONCOCIN, PUFF, RX, and VM have demonstrated feasibility in this area.

Biomedical expert systems may fulfill some of the health maintenance functions within the SSDS such as:

4.3.1.2 Medical Diagnostics Support

4.3.1.3 Treatment Support

1.6.2.1.2.5 Fault Detection/Diagnosis/Correction

FAITH is a system developed by JPL that provides powerful representational and diagnostic capability, and has been applied to the Voyager spacecraft Mission Telemetry Monitoring and Diagnosis process. Component behavior in FAITH is simulated by rules that are typed as Events and Inferences permitting it to imitate certain aspects of human diagnostic performance.

This type of diagnostic system is able to represent different levels of details of system components, to troubleshoot, and to infer the component failure even to the most primitive component. It is within the current capabilities of diagnostic systems to monitor, detect, and in some cases correct failures of equipment.

Diagnostic expert systems may be employed for the detection and diagnosing of faults within mary SSDS systems; however, they may not be suitable for correcting failures of critical systems where very rapid response times are required, i.e. for those systems requiring redundant or hot backups. Functions to be examined are:

1.3.3 Data Distribution Routing and Transmission

2.5.3.2 OTV Checkout and Diagnostics

2.5.4.2 OMV Checkout and Diagnostics

2.5.5 Customer Payload Checkout/Service

2.6 SS Payload Equipment Checkout and Servicing

4.5.4 System Diagnostic Support

4.x.x.x Device Management

5.x.x.x Facilities' Device Management

1.6.2.1.2.6 Planning, Scheduling, and Logistics

The areas of planning and scheduling lend themselves to development by expert systems. Rand has developed at least two scheduling systems. NASA JPL has developed a ground-based scheduling system, DEVISOR, used for scheduling onboard activities of unmanned spacecraft. M. Fox has developed a job-shop scheduling system based upon constraint-directed reasoning. Ford Aerospace and Communications Corporation has developed the Resource Planning and Management System (RPMS), a general purpose resource scheduling system.

It should be noted, however, that state-of-the-art planning systems are only capable of resolving scheduling constraints with respect to the optimization of a very limited number of resources. Thus, current systems are more suited for the scheduling of activities than for the optimization of resources.

Since conventional approaches to planning and scheduling problems do not often provide satisfactory solutions, the merits of expert planning and scheduling systems will be studied closely. The following functions will be addressed:

3.1 Develop Typical Day Schedules

3.2 Develop Short Term Schedules

4.3.1.5 Exercise Planner

5.x.2 Facilities' Resource Management

5.2.4 Global Facilities Management

7.1.1 Develop Transportation Plan

7.1.3 Develop Maintenance Schedules

7.1.4 Develop Training Schedules

1.6.2.1.2.7 Modeling

A program called Natural Language for Queuing Simulation (NLPQ) was written at the Naval Postgraduate School in the early seventies. This program accepted an English description of events and their interrelationships and produced GPSS (a conventional simulation language program) code. This code could then be read by the GPSS program, and simulations could be run.

Model building has been a significant part on many expert systems such as DENDRAL, which models organic molecules; PHI-0, which models oil-well drilling; and DEVISOR, which models scheduled events. These represent only a few of the evolved expert systems in which modeling is an integral part of the system.

There is much promise for modeling and simulation using expert systems, particularly rule-based environments where constraints can be established. Modeling is also an inherent feature of planning/scheduling systems. Other SSDS functions for modeling are:

1.3.3 Data Distribution Routing and Transmission

2.5.3 Support OTV Operations

2.5.4 Support OMV Operations

4.x.x.x Device Management

6.10 Develop Software — Modeling

7.4 Control Inventories

1.6.2.1.2.8 Distributed Data Base Management

The main function of Distributed Data Base Management (DDBM) is to provide the mechanism for storing and retrieving information. Information in this context is more than mere data; it includes knowledge necessary for expert systems to infer conclusions. Although the function of storing and retrieving is a typical function of conventional data management systems, this system, unlike a conventional one, is charged with "making sense" of requests from a user and selecting the "best-fit" for the user request. Furthermore, the DDBM must be able to search out, request, and retrieve information even though it exists in other networked data base systems. The DDBM must be cognizant of the content of external systems and verify retrieved information.

The concept of "making sense" of a user requests assumes a knowledge of English syntactic constructions, abbreviations, pronoun references, ellipses (i.e. omissions of one or more words that can be inferred through context), and minor errors (e.g. spelling or grammar).

The "best-fit" information means that the DDBM can infer from the request the nature of the data that the user needs even though the user may have been imprecise or incorrect in his request. It also presumes the user can tolerate a certain measure of incorrect responses.

The DDBM must have knowledge of the universe in which it exists in order to extract and deliver the information that is requested, regardless of where the information is located (perhaps even several locations), or to digest and store the information it is given.

No examples of an operational expert system DDBM can be cited.

Potential SSDS functions for which an expert system DDBM can be considered are:

5.x.1 Data Base Management

5.2.4 Global Facilities Management (Data Base)

1.6.2.1.3 Projected Capabilities

The appearance of such "Expert Systems" companies as Applied Expert Systems (Cambridge, Ma.), Cognitive Systems (New Haven, Ct.), Computer*Thought (Plano, Tx.), Inference Corporation (Los Angeles, Ca.), IntelliCorp (Palo Alto, Ca.), Smart Systems (Alexandria, Va.), Syntelligence (Menlo Park, Ca.), and Teknowledge (Palo Alto, Ca.) is evidence of the success that Expert Systems have experienced in the last few years.

Many companies are beginning to establish AI laboratories with the intent of developing expert systems.

DARPA, the National Security Agency, NASA, and the armed services are all engaged in promoting the development of expert systems for a myriad of applications. Research on approaches that would speed the execution of expert systems, namely parallel processing and the development of a real-time inference engine, could help to broaden the range of SSDS applications. Presently, there are no large scale, real-time expert systems. Rome Air Development Center released an RFP in early 1984 for research intended to result in an inference engine capable of handling 10,000 rules and performing 4000 inferences per second.

It seems likely that expert systems could play a significant role in the automating of SSDS functions that do not critically require large, real-time systems.

1.6.2.1.4 References

Brachman, Ronald J. and Hector J. Levesque, "Competence in Knowledge Representation," Proceedings of the National Conference on AI, August, 1982.

Clancey, William J., "Theory and Practice of Expert Systems," Stanford University, July, 1983.

Davis, Randall and Jonathan King, "An Overview of Production Systems," HPP-75-7, AIM-271, Stanford AI Laboratory, October, 1975.

Drogin, Edwin M., "AI Issues for Real-Time Systems," Defense Electronics, August, 1983, pp. 71-79.

Fain, J., F. Hayes-Roth, H. Sowizral, and D. Waterman, Programming in ROSIE: An Introduction by Means of Examples, N-1646-ARPA, Rand Note, February, 1982.

Fox, Mark S., Brad Allen, and Gary Strohm, "Job-Shop Scheduling: An Investigation in Constraint-Directed Reasoning," Proceedings of the National Conference on AI, August, 1982.

Gevarter, William B., "Expert Systems: Limited but Powerful," IEEE Spectrum, August, 1983.

_____ "An Overview of Expert Systems," NBSIR 82-2505, May, 1982.

Genesereth, Michael R., Milton Grinberg, and Jay Lark, "SUBTLE Manual," HPP-81-11, Rev. 3, Stanford University, January, 1982.

Hayes-Roth, Frederick, "Knowledge-Based Expert Systems," IEEE Computer, October, 1984, pp. 263-273.

Hayes-Roth, Frederick, D. A. Waterman, and D. B. Lenat, Building Expert Systems, Reading, Massachusetts, Addison-Wesley Publishing Co., 1983.

McDermott, John, "R1: A Rule-Based Configurer of Computer Systems," Artificial Intelligence, 19 (1982), pp. 39-88.

Nau, Dana S., "Expert Systems," IEEE Computer, February, 1983.

Sleeman, Derek, "Theory and Practice of Expert Systems," Stanford University, July, 1983.

Stefik, Mark, "An Examination of a Frame-Structured Representation System," Stanford University.

Stefik, Mark, Jan Aikins, Robert Balzar, John Benoit, Lawrence Birnbaum, Frederick Hayes-Roth, and Earl Sacerdoti, "The Organization of Expert Systems, a Tutorial," Artificial Intelligence, 18 (1982), pp. 135-173.

Stambler, Irwin, "Move to Satellite Autonomy Spurs 'Expert' System Research," Research & Development, February, 1984, pp. 62-63.

Vere, Steven, Planning in Time: Windows and Durations for Activities and Goals, JPL Publication, November, 1981.

Vesonder, Gregg T., Salvatore J. Stolofo, John E. Zielinski, Fredrick D. Miller, and David H. Copp, "Ace: An Expert System for Telephone Cable Maintenance."

1.6.2.2 Image and Speech Recognition

1.6.2.2.1 Description

Image recognition is probably the most difficult area of AI and represents less dramatic advances. Systems tend to be crude and limited in their capability to detect and identify objects.

Vision is often divided into three categories: 1) low-level vision, or early processing, which includes such items as intensity and orientation of edge elements; 2) intermediate- processing, or segmentation, which includes features such as lines, regions, shape, and surface; 3) high-level processing, which deals with objects that rely on domain-specific knowledge to construct scene descriptions.

Speech recognition may be considered to be signal processing. More progress has been accomplished in this area as compared to vision.

1.6.2.2.2 Option Characterization

1.6.2.2.2.1 Image Recognition

Most of the applied successes have been associated with robotic vision. At the Ford Motor Robotic Center in Dearborn, Mi., vision has been used to identify the holes in engine blocks in order for an industrial robot to place it on a pallet. However, they have had little success with using vision to identify streaks or runs in paint.

A fully automatic system for transistor wire bonding, developed by Hitachi, was one of the first production robotic-vision systems to use image processing functions extensively. This system, which assembles 2,000 chips per hour, uses vision to locate integrated circuits.

CONSIGHT-I, developed at General Motors, is a vision-based system that picks up parts that have been randomly placed on a moving conveyor belt.

SRI International has developed a leading machine-vision system called the SRI Vision Module. The system is a package of useful programs with all necessary hardware for visual sensing and inspection tasks.

1.6.2.2.2.2 Speech Recognition

Research is being performed by many groups. In particular, the Air Force has been sponsoring efforts whereby pilots may converse with their aircraft thus freeing their hands for other duties. It has been noted, however, that the human voice tends to change pitch in stressful conditions therefore making successful pattern recognition algorithms somewhat more difficult to achieve.

A voice recognition control system with a vocabulary of 100 discrete words is being tested at the NASA JSC Space Station Command Center Mockup.

1.6.2.2.3 Projected Capabilities

When DARPA announced its "Strategic Computing" plan in 1983, it estimated that it would require another 10 years of concentrated effort before vision would reach the state where an unmanned vehicle could traverse unknown terrain successfully.

It is unlikely that image recognition systems could be a viable option for SSDS applications that would require three-dimensional vision, e.g. rendezvous or collision avoidance.

Two-dimensional vision shows more promise and may be a viable option for astrophysics applications. Some research in this area is being conducted at NASA's Ames Research Center. An SSDS function for two-dimensional vision is:

6.10 Develop Software — the digitization of visual scenes (from photographs, drawings, etc.) for Speech recognition for disconnected voice, i.e. word recognition, shows more promise and may be used in a fashion similar to that of the pilots. In the long term, industry, the MCC, and the Japanese Fifth Generation projects' research may produce products with greatly increased vocabularies; however, speech recognition for connected voice cannot now be predicted as a viable option for the SSDS. SSDS functions for disconnected voice recognition are:

4.x.x.x Core Systems' Command Interface Processing

5.x.x.x Facilities' Command Interface Processing

1.6.2.2.4 References

Ericsson, K. Anders, and Herbert A. Simon, "Verbal Reports as Data," Psychological Review, vol. 87, no. 3, May, 1980, pp. 215-251.

Johnson, Ron, "Automatic Target Recognition Fuses Sensors and Artificial Intelligence," Defense Electronics, April, 1984, pp. 106-115.

"Space Station Command Center Mockup: Description," Avionics Integration Branch, Simulation and Avionics Integration Division, NASA JSC, July, 1984.

1.6.2.3 Natural Language Software

1.6.2.3.1 Description

The processing of natural language by machines requires a possession of contextual knowledge for the message and the process for drawing inferences from both the message and the contextual knowledge.

Natural language understanding is concerned with the constituents of the language. These include: morphemes (meaningful substrings within words), inflections (prefixes and suffixes), lexical items (words), determiners (articles and demonstratives), quantifiers (adjectives and adverbs), syntactic entities (noun phrase, verb phrase, adverb, etc), semantic roles, clauses, negation markers, and sentential components.

The areas where most research has been concentrated on natural language processing include: data base retrieval (DB query), data base management (DB interfaces), text comprehension, text generation, question answering, interactive dialogues, and machine translation.

Natural language processing for data base access must be able to handle grammatically incorrect input, clarify interactions, instruct neophytes, address experts at their level, and incorporate domain-specific knowledge of the data base.

The general architecture of a natural language data base query system includes: 1) English input query, 2) natural language analyzer, 3) internal representation mechanism, 4) code generator (automatic programming), and 5) executable retrieval routine.

1.6.2.3.2 Option Characterization

Several natural language (NL) programs have emerged in the past few years. These include: INTELLECT (Artificial Intelligence Corp., Waltham, Ma.), a NL data base retrieval interface written in PL-1; STRAIGHT TALK (Symantec, Sunnyvale, Ca.), a portable NL data base interface written in PASCAL; PEARL (Cognitive Systems, Inc., New Haven, Ct.), a customized NL interface system written in LISP; NLMENU (Texas Instrument Inc., Dallas, Tx.), a NL interface to relational data bases; WEIDNER (Weidner Communications Corp., Provo, Ut.), a semi-automatic natural language translation; LOGOS (Logos Computer Systems Inc., Waltham, Ma.), an interactive natural language translation.

1.6.2.3.3 Projected Capabilities

Funding for natural language processing research has come basically from the Office of Naval Research (ONR), National Science Foundation (NSF), and Defense Advanced Research Projects Agency (DARPA). This research is being undertaken at such universities as Yale, University of Massachusetts, University of California, Carnegie-Mellon, University of Illinois, Brown, Stanford, MIT, and University of Texas.

Several members of the industrial community are also investigating natural language processing. Some of these are: Bolt Beranek & Newman, TRW, IBM, Burroughs, Sperry Univac, Systems Development Corp., Hewlett Packard, Martin Marietta, Texas Instruments, Xerox, Bell Labs, Institute for Scientific Information, General Motors, and Honeywell.

It appears that the trend for developing natural language processing systems will continue, and more sophisticated systems should be forthcoming in the next few years. Natural language processing is a desirable option for the SSDS in that it would provide an interface that could be "friendly" to a large group of users from varying technical backgrounds. Thus, it merits additional study. However, it must also be noted that no natural language interface has as yet been developed to such complex and distributed data bases as those of the SSDS promise to be. SSDS functions to be evaluated include:

4.x.x.x Core Systems' Command Interface Processing

5.x.x System 'x' Data Base Management

5.3.3.1 User Process Control (Satellite Centers)

5.x.x.x Facilities' Command Interface Processing

6.9.5 Conduct Training Exercise

7.2 Customer Usage of System (Accounting)

Natural language processing should also be an important feature of the SSDS expert systems, particularly those used for planning and scheduling.

1.6.2.3.4 References

Kaplan, S. Jerrold, "Natural Language in the DP World," Datamation, August, 1982, pp. 115-118.

Rauch-Hindin, Wendy, "Natural Language," Systems Software, January, 1984, pp. 187-200.

1.6.3 Summary

AI, particularly the field of knowledge-based or expert systems, addresses the fundamental problem of the transfer and application of knowledge and

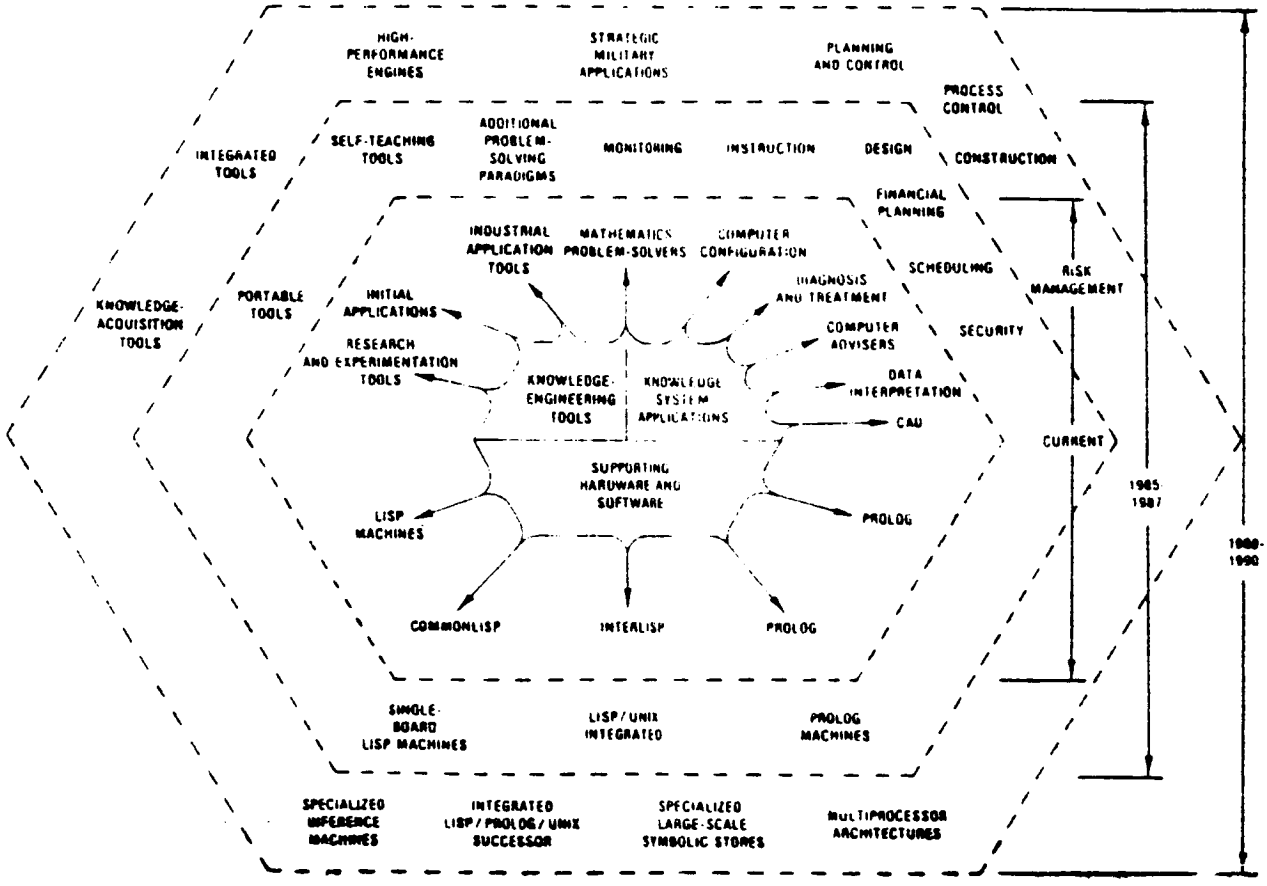
expertise. It seeks computerized solutions to the problems largely created by computers: how to capture, analyze, and distribute vast amounts of information. The human reaction to this knowledge explosion has been the trend towards specialization. Each person's expertise must now be funneled into an ever-narrowing domain. Thus, another problem is created: the reliance upon experts, an unpredictable resource, for the performance of required functions.

Whereas other areas of computer science are concerned with the generating, straightforward processing, gathering, and transmitting of data, interpreting the significance of the data ("figuring out what it all means") falls within the realm of AI.

Technological progress may, therefore, be paced by its ability to solve the problems AI addresses. The recognition of this fact is what has provided the impetus for the tremendous amount of ongoing and projected research in AI.

The commercialization of this research will be rapid and dramatic. Figure 1.6-1 illustrates the current and predicted commercialization of knowledge system technology. Table 1.6-2 illustrates the past and predicted growth in five AI markets.

FIGURE 1.6-1
COMMERCIALIZATION OF KNOWLEDGE SYSTEM TECHNOLOGY



Source: Hayes-Roth, Frederick, "Knowledge-Based Expert Systems," IEEE Computer, October 1984, p. 270.

TABLE 1.6-2
ARTIFICIAL INTELLIGENCE MARKET GROWTH
($ Millions)

MARKET AREA	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990
Expert Systems	4	8	16	32	55	95	160	270	460	780
Natural Language	5	8	18	32	55	100	175	300	525	920
Computer-Aided Instruction	3	5	8	12	20	30	50	80	125	200
Image Recognition	7	15	30	55	85	130	202	320	490	760
Voice Recognition	4	6	10	17	25	40	60	90	130	200
TOTALS	23	42	82	148	240	395	647	1060	1730	2860

Source: DM Data Update, vol. 1, no. 1, June 1984.

Yet, it must also be recognized that the AI technologies are immature. Significant numbers of products have emerged only within the last 5 years. One can predict that AI technologies will undergo tremendous growth, but the paths they will take are unpredictable. Rapid obsolescence and the abandonment of approaches will be characteristic of the technologies for the next decade.

AI's immaturity presents several issues to be addressed in greater detail in Task 3's AI Automation Trade Study. Some of these issues are:

- Scarcity of engineers trained in AI applications, e.g. knowledge engineers
- Limited breadth of knowledge
- Slowness of response time due to the lack of a real-time inference engine, multiprocessor architectures, or parallel processing
- Availability of space-qualified processors and their integration into the DMS
- Lack of systems engineering tools to support the design, development, verification, and maintenanceof software
- Difficulty in providing management insight into the development process, i.e. assessing the status
- Lack of modularity and techniques to distribute the software effort over a large engineering team
- Speculative nature of AI products and services.

The impact of each of these issues may vary according to the nature of the particular SSDS function and the time period being considered. References were made throughout this report on specific SSDS functions where AI technologies might be applied. Table 1.6-3 provides an overview of those

references. Whether and when an AI approach is preferable to a conventional approach for the performance of particular functions, considering the issues and their impact upon risk and cost criteria, is the subject of the AI Automation (Expert Systems) Trade Study.

TABLE 1.6-3
APPLICABILITY MATRIX: OPTIONS VS. SSDS FUNCTIONS

		SSDS Functions (7)						
1.6.2 Applications		1.0	2.0	3.0	4.0	5.0	6.0	7.0
1.6.2.1	Expert Systems and Prob. Solving						(1)	
1.6.2.1.2.1	Subsystem Monitor & Control	NO	YES	NO	YES	YES	NO	NO
1.6.2.1.2.2	System Configuration	YES	YES	NO	YES	YES	YES	NO
1.6.2.1.2.3	Programming and CAI	NO	NO	NO	NO	NO	YES	NO
1.6.2.1.2.4	Biomedical	NO	NO	NO	YES	NO	NO	NO
1.6.2.1.2.5	Fault Diagnosis	YES	YES	NO	YES	YES	NO	NO
1.6.2.1.2.6	Planning, Scheduling	NO	NO	YES	YES	YES	NO	YES
1.6.2.1.2.7	Modeling	YES	YES	NO(2)	YES	NO(2)	YES	YES
1.6.2.1.2.8	Distributed Data Base Mgmt.	NO	NO	NO	NO	YES	NO	NO
1.6.2.2	Image and Speech Recognition	NO	NO	NO	YES(3)	YES(3)	YES(4)	NO
1.6.2.3	Natural Language	NO	NO	NO(5)	YES	YES	YES	YES

Notes:

1 All applications listed under 4.0, Operate Core Systems, would also be required under 6.0, Simulation of the Core Systems.

2 However, modeling is an inherent feature of the planning and scheduling expert systems.

3 Disconnected voice recognition only.

4 Scene digitization.

5 However, natural language interfaces are an inherent feature of the planning and scheduling expert systems.

7 SSDS function numbers represent the following major functional categories:

1.0 Manage Customer/Operator Delivered Data
2.0 Manage Customer/Operator Supplied Data
3.0 Schedule and Execute Operations
4.0 Operate Core Systems
5.0 Manage SSDS Facilities
6.0 Develop, Simulate, Integrate, and Train
7.0 Support Space Station Program

1.7 COMMUNICATIONS

1.7.1 HARD-WIRED COMMUNICATIONS

1.7.1.1 Network Media for Space Station Program

1.7.1.1.1 Description

The transmission media of a computer network is the physical signal carrying element connecting the nodes of the network. The media may consist of: (1) coaxial cable (coax), (2) twisted shielded pair (TSP), (3) optical fiber, or (4) electromagnetic or optical transmission through free space.

Different transmission media differ in transmission capacity bandwidth, reliability, ease of connectivity, immunity to noise, cost, applicable modulation schemes, attenuation, sensitivity to radiation, and acceptable temperature range.

It is not necessary for a computer network to contain only one type of media. Hybrid interconnections may be required in certain situations that require the use of optimal properties of given media. For example, a network extended over a flammable region may use mostly TSP because of cost, except at the flammable region, where optical fiber would be used. Optical fiber carries no electricity, so no sparks could cause an explosion.
In general, the discussion that follows applies to the following elements of the Space Station Program (SSP):

- The Space Station
- Co-orbiting Platforms (COP)
- Polar Orbiting Platforms (POP)
- Orbital Maneuvering Vehicle (OMV)
- Orbital Transfer Vehicle (OTV)

1.7.1.1.2 OPTION CHARACTERIZATION

1.7.1.1.2.1 Areas of Comparison

The following areas of comparison include general characteristics for media selection and some that have particular application to the space station and other space based networks. No attempt was made to place these in order of importance.

a) Bandwidth. The frequency domain width of a signal is known as its bandwidth, and different media can only carry signals of certain maximum bandwidths. It is proportional to the information carrying capacity of a channel or medium. When a signal is to be propagated over a relatively long distance, the bandwidth–distance product is important also. As a signal travels, dispersion and other physical phenomena can cause errors in detection at the receiver because successive pulses start merging together. A typical bandwidth–distance product for a communications system might be 10 MHz.km, which means that a 10 MHz signal can be carried for one km. or 1 MHz for 10 km, etc., as long as the product of bandwidth (in MHz), and distance (in km) is less than 10. In addition, the receiver and transmitter rise times can be a limiting factor in the overall system, especially in local area networks where distances are small and the bandwidth–distance product of the media may not be the limiting factor.

b) Cost. The relative cost of one media versus another can be a factor in media selection, specially when long distances are involved. The transmitters and receivers can also vary in cost, depending on the medium with which they are designed to work.

c) Reliability. As in cost, for very localized networks the end to end reliability is not so much a function of the medium, as it is of the transmitters and receivers.

d) Noise immunity and bit error rate (BER). Noise, or electro-magnetic interference can have a devastating effect on a transmission system if the system medium is susceptible to picking up that interference. If the system is digital, the effect of noise is to increase the number of bit errors for each bit transmitted (10^{-6}, for example is a typical BER). Figure 1 shows a typical plot of BER versus Signal to Noise Ratio (SNR). If the modulation is analog, the SNR decreases and intelligibility of the received signal may suffer.

e) Electromagnetic transmission. When a signal is carried through a medium, it is possible that an antenna effect will exist, and an electromagnetic signal proportional to the signal carried will be transmitted. This situation is the reverse of what happened in d) above, where the medium acts as a receiver. Media transmission of electromagnetic radiation is a problem for two reasons. First, it poses a potential security problem if the data transmitted is classified, and second, it can cause interference with adjacent communication lines.

f) Attenuation. As a signal propagates it loses some of its energy for various reasons. Attenuation is a measure of how fast this energy is lost as a function of distance travelled (units are dB/km). If attenuation is very high, then repeaters are needed at closer distances, with higher cost and lower reliability.

g) Modulation schemes. The way in which a signal is mixed with others to facilitate propagation through a medium is known as modulation. In AM radio, for example, an audio signal is used to amplitude modulate a radio frequency carrier, so that the audio signal can travel much further than it could otherwise, and without disturbing anyone. AM is a type of broadband transmission. FM, PM, SSB-AM, FSK, PSK are other broadband methods. In baseband, the information carrying signal is not modulated, but is sent as is down the medium. The best scheme to use will depend on whether the data is analog or digital, the BER of the medium, the degree to which data must be multiplexed, etc. The BER vs SNR curve shown in Figure 1

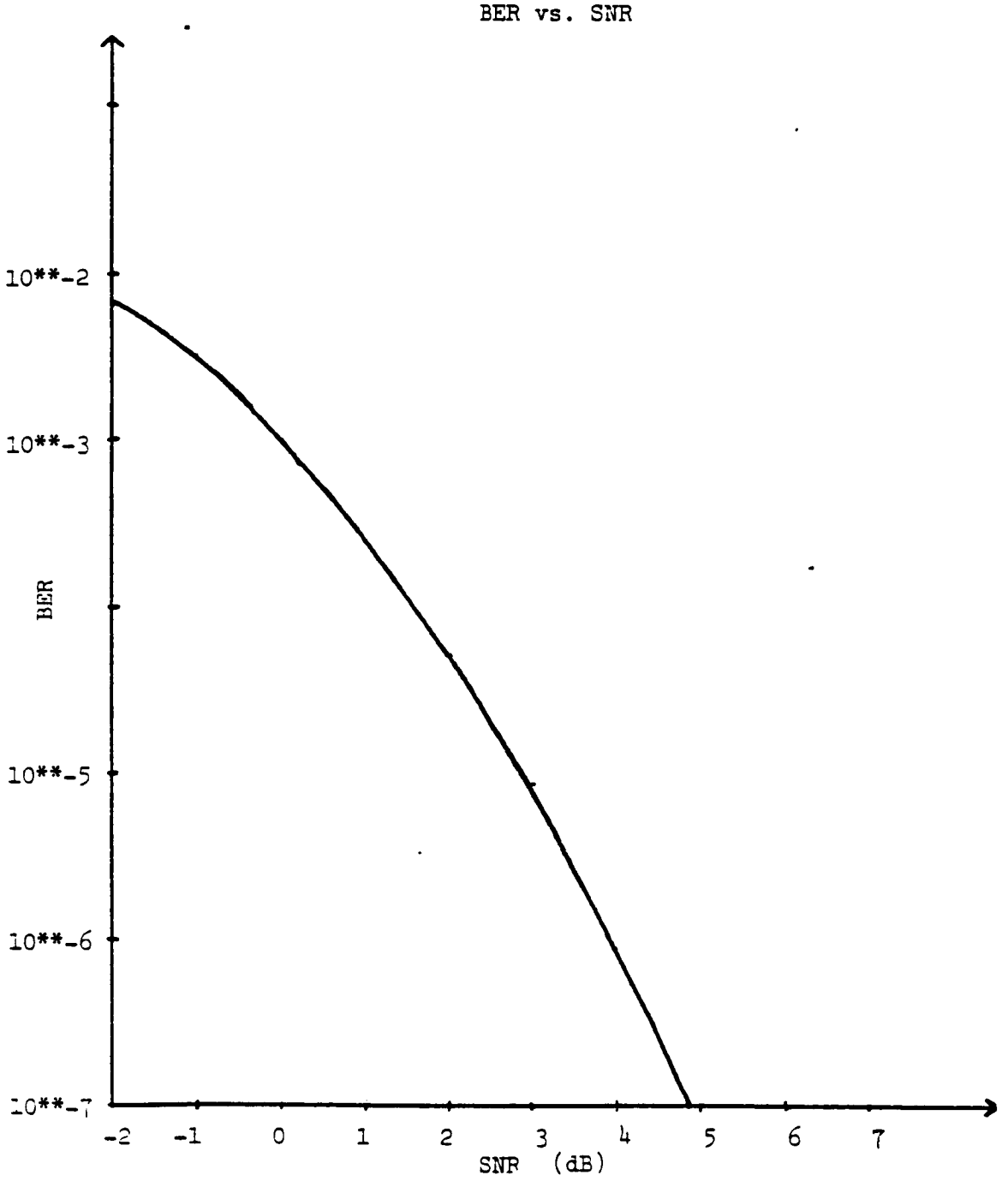


Figure 1

will shift considerably depending on the modulation scheme. More complex modulations will usually yield a lower BER for a given SNR. This allows a lower power level at the transmitter, and can save weight, space and power.

h) Connectivity – directivity – topology implications. Some transmission media are capable of point to point and broadcast connectivity. Also some can transmit more easily in one direction, while others are naturally bidirectional. Connectivity and directivity have direct implications on the topology that a medium will allow. For example, if a medium is not well suited for broadcast, a bus topology may be a poor choice, because all nodes in a bus need to receive the data at about the same time, but a token ring may be appropriate because only the "next" node needs to receive data.

i) Space environment implications. The space environment of low earth orbit may damage some media unless certain precautions are taken. The cumulative effect of cosmic rays, and the very large temperature ranges are good examples. The zero–g and vacuum conditions of space could also be a problem.

j) Transmitter and receiver electronics. Different media require different transmitters and receivers. This physical link that interfaces with the media has implications in cost, weight, reliability, complexity, maintainability, temperature sensitivity, and power and space requirements.

1.7.1.1.2.2.1 Twisted Shielded Pair (TSP)

TSP is a form of transmission line in which two wires are arranged in a spiral pattern so that electrical properties are constant throughout the length of the line, and to reduce noise. They are available with different numbers of twists per foot and various types of shields.

a) Bandwidth. 64 kbits/sec is a typical data rate, but a few megabits/sec can be achieved if distances to be travelled are very short. The present Space Shuttle bus network consists of TSP and runs at 1 Mb/sec over a distance of 300 feet.

b) Cost. This is one of the cheapest media per linear foot, and transmitters/receivers are also inexpensive. It is an old technology, however, so the price to performance ratio is as high now as it is likely to ever be. Newer media are gaining on TSP, especially when cost of transmission capacity is considered instead of cost per linear foot.

c) Reliability. Highly reliable because of its simplicity.

d) Noise immunity and BER. Not very good, with a typical BER of 10^{-5}.

e) Electromagnetic transmission. When the separation between the conductors is in the same range as operating wavelength EM radiation can take place, so TSP is best suited for transmission of relatively low frequencies (3-4 MHz or less).

f) Attenuation. This is dependent on the frequency of transmission. The higher the frequency the higher the attenuation because of two reasons. First, the higher the frequency, the more loss due to radiative effects, and second, higher frequencies tend to travel on the outside of a cable (skin effect) so that the impedance is higher at higher frequencies and more energy is lost to heating.

g) Modulation schemes. Analog or digital data can be transmitted with a variety of signaling approaches. Baseband is normally used because high frequencies are attenuated and broadband usually includes significant high frequency components.

h) Connectivity - directivity - topology implications. Capable of both point to point and multipoint connectivity, but much better suited for point to point applications such as in a Private Branch Exchange (PBX). TSP is bidirectional, but because it is better for point to point, the selected topology should take this into consideration.

i) Space environment implications. The internally controlled space environment in the shuttle has caused no problems for TSP. Direct space exposure has not caused problems in previous space missions.

1.7.1.1.2.2.2 Coaxial Cable (Coax)

Coaxial cable is a type of transmission line very similar in concept to TSP, but with modified construction that gives Coax different operating characteristics. Coax has an inner wire conductor (usually copper), with an outer conductor that surrounds the inner one and is usually grounded. Air, or some other dielectric material separates the two conductors. An insulator surrounds the entire cable.

Two major types of coax are available; 50 ohm for baseband transmission, and 75 ohm for broadband.

a) Bandwidth. Baseband coax can carry 10 - 20 Mbits/sec, half-duplex broadband coax can carry as much as 150 Mbits/sec full-duplex.

b) Cost. Coax is slightly more expensive than TSP, and taps and connectors for it are also more expensive, but the higher bandwidth and other properties of coax can make it very cost effective compared to TSP for some applications.

c) Reliability. Very reliable, especially for baseband where no transponders or active modulators are needed. Broadband is also reliable, and redundant active elements can increase the reliability to that of baseband.

d) Noise immunity and BER. Coax is more immune to noise than TSP, especially at higher frequencies, and the BER is usually less than 10^{-5}.

e) Electromagnetic transmission. As in TSP, coax can act as a transmitter antenna for electromagnetic waves, particularly at high frequencies, so can pose security problems also.

f) Attenuation. Varies with frequency. At 10 MHz it is about 10–30 dB/km, and at 100 MHz it is about 30–100 dB/km. For spacecraft applications, distances are not likely to be more than 200 m, and will usually be much less than that.

g) Modulation schemes. In baseband there is no modulation, but the data is usually Manchester encoded so that the clock can be easily recovered. In broadband, frequency and phase modulation are used.

h) Connectivity – directivity – topology implications. Point to point is easily implemented, but coax is primarily used for multipoint topologies such as bus and tree. Baseband coax can typically have 100 or so drops, and broadband can support 1000 or more drops. Because of the high attenuation of coax, however, repeaters or amplifiers must be placed every one–half kilometer approximately.

i) Space environment implications. Coaxial cable has been used extensively in space without any problems.

1.7.1.1.2.2.3 Optical Fiber

Communications with optical fiber occurs by sending a beam of optical or infrared radiation through the fiber. An optical transmitter converts an electrical signal into a modulated beam which is then optically coupled to the fiber. A receiver at the other end performs the inverse operation where the electrical signal is recovered from the modulated beam. The fiber consists of a center core of glass with an index of refraction slightly higher than that of the surrounding material, known as the cladding. The ratio of the indices of refraction of the two materials is such that a beam travelling in the core undergoes total internal reflection when it contacts the core/cladding boundary.

There are three different ways in which light propagates down a fiber, depending on the diameter of the core and how fast the index of refraction changes at the core/cladding interface. When the core is of a very small

diameter (5–10 microns) and the index of refraction changes abruptly at the interface, the result is single–mode step index fiber, which transmits a single mode of linearly polarized electromagnetic radiation. When the diameter of the core is fairly large (50–400 microns) and the index of refraction also changes abruptly, the fiber becomes multi–mode step–index. In this type of fiber many modes of light propagate at the same time. The third type of fiber is the multi–mode graded index fiber, in which the index of refraction changes slowly from the inside of the core to the outside of the cladding. Light is propagated because of the bending of the light that takes place as the index of refraction changes, not because of internal reflection.

Because optical fibers are so thin, most cables include several fibers inside them, and strength members to keep the structure from falling apart under axial and tangential forces.

a) Bandwidth. Practical systems available off–the–shelf provide data rates up to about 50 Mbps, but under laboratory conditions data transfer up to a few Gigabits per second have been demonstrated. For rates of less than 100 Mbps, highly reliable and inexpensive LED's can be used, but for higher data rates laser diodes are required. Laser diodes are not very reliable, are expensive and very temperature sensitive.

b) Cost. The cost per foot of fiber is quickly approaching that of coax and TSP, but the optoelectronic transmitters and receivers are still expensive (see section j). Connecting fiber is also more difficult and expensive than TSP and coax because optical alignment is required, so unexpected modifications in the topology can be costly.

c) Reliability. Systems using LED's are very reliable, but those with laser diodes are fairly unreliable because of present differences in MTBF's. The fiber itself is very strong and does not significantly degrade the reliability of the overall system much unless humidity is allowed to affect it, in which case microcracks propagate and the fiber can split.

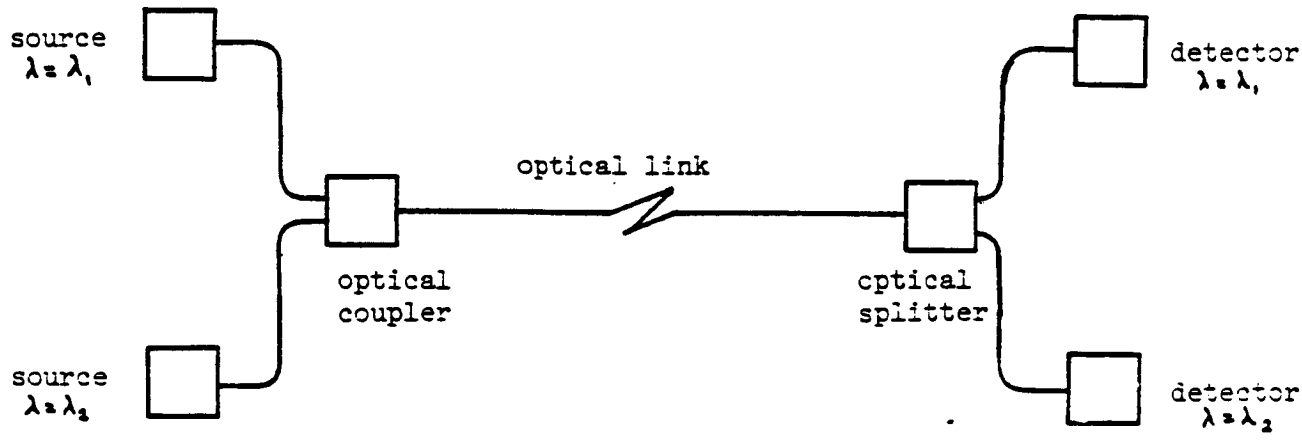
d) Noise immunity and BER. The negligible noise susceptibility of fiber is one of its biggest advantages over other media. Electromagnetic interference does not interact with the fiber because the optical energy has a wavelength very different than radio frequencies, and the opaque cover of fiber does not allow interference from optical sources. Fiber also has an extremely low BER, in the order of 10^{-9} to 10^{-12}.

e) Electromagnetic transmission. EM transmission is negligible, and fiber is very secure as a result, because there are no spurious transmissions that could be picked up. The only way to tap into a fiber is by physically getting a "piece" of the beam transmitted, and such attempts are very difficult and can usually be detected.

f) Attenuation. It can be as low as .2 dB/km for single-mode fiber, but typically it is about 2 - 5 dB/km.

g) Modulation schemes. Optical fiber systems normally operate on baseband where the light is quickly turned on and off along with the digital signal to be transmitted. In certain cases it can be advantageous to send two or more beams of different wavelength on the same fiber at the same time, i.e. "color modulation". (Figure 2). LED's that operate at different wavelengths can couple their output onto the same fiber, and light detectors of the incoming wavelengths are placed in the receiver.

h) Connectivity - directivity - topology implications. Mostly limited to point to point, but multidrop is possible at higher expense by using optical couplers and splitters. Passive multidrop systems are presently limited to about 16 - 32 nodes because of the losses at the taps. Propagation through the fiber is intrinsically unidirectional, so a bus topology would require two fibers to meet the bidirectionality requirements. Fiber is ideal for a token ring type topology where requirements are for unidirectional data transmission, and the node bypass technology is already available.


source
λ = λ1
source
λ = λ2
optical
coupler
optical link
cptical
splitter
detector
λ = λ1
detector
λ = λ2

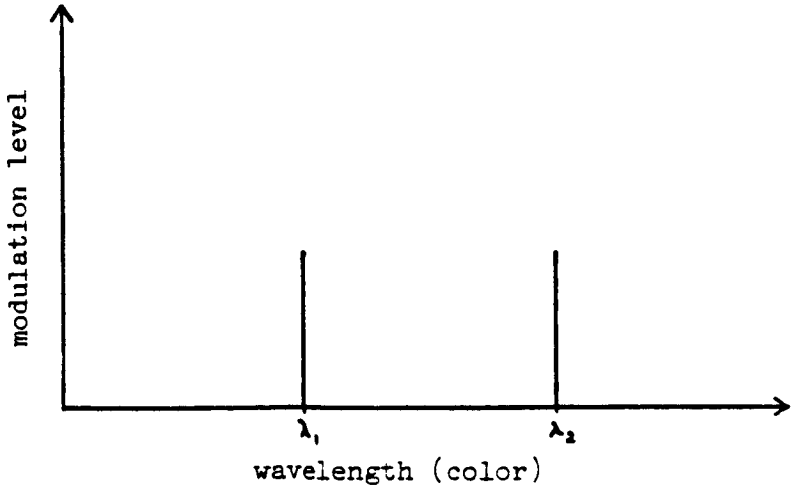

modulation level
λ1
λ2
wavelength (color)

Figure 2

Passive and active star networks have been built with 16-64 nodes. Passive ones are very reliable but are limited to about 32 nodes and receiver sensitivity and transmitted power limit how much the power can be divided.

i) Space environment implications. TBD

1.7.1.1.2.2.4 Radio and Light Through Free Space

When physical connection using one of the media previously discussed is difficult or even impossible, information can still be carried through free space with radio or light. Radio frequency modems, for example, can be used for data transmission between computers that are not physically connected. Point to point infrared optical systems of very high bandwidths have been used for computer to computer communications in line of sight systems. Atmospheric disturbances and dispersion are the limiting factors in these systems, but in the vacuum of space, and over the short distances in a space vehicle, these factors become relatively insignificant. Microwave directional transmission is another form of transmission that could be applicable.

a) Bandwidth. For radio, it depends on the portion of the spectrum that can be dedicated. If a relatively low power transmitter is used in space, the interference with earthbound systems can be made insignificant. Most systems available now offer packetized digital radio for communications with mobile systems, such as military vehicles. For infrared transmission, data rates around 100 kbps are common over a range of a few kilometers. Reliable communications at 1.5 Mbps are possible over 1 km paths. The inverse relation between data rate and distance is very apparent here. Microwaves can also carry high data rates in point to point links.

b) Cost. This is very difficult to assess because it depends very much on the application. There is no physical media to buy or to install, but the cost of transmitters and receivers can be substantial. For mobile systems, radio may be the only alternative, and for a system that needs to be reconfigured often, movable infrared sources and detectors may be a good choice.

c) Reliability. Depends on the electronics of the transmitter and receiver, but can be very high if redundancy is used.

d) Noise immunity and BER. Dependent on the distance over which transmission takes place, and atmospheric conditions. Typically the BER is around 10^{-6}. Could be susceptible to jamming.

e) Electromagnetic transmission. Radio is nothing but EM waves, so security problems are substantial unless the data is encrypted. For line of sight optical communications, enough of the modulated beam can be tapped, so security can also be a problem. Microwave and radio could potentially interfere with the data transmission through TDRS, etc., so careful spectral analysis is required.

f) Attenuation. Variable depending on the frequency or wavelength of transmission, and atmospheric conditions. Signal fading can also occur, mostly because of varying atmospheric conditions.

g) Modulation schemes. For radio, any of the normal modulation schemes can be used, but spread spectrum techniques offer the best performance while requiring more sophisticated transmitters and receivers. For infrared, transmission is usually baseband, with several varieties of pulse modulation that optimize immunity to noise and atmospheric scintillation.

h) Connectivity - directivity - topology implications. Radio is inherently a broadcast type medium and is ideal for multidrop multiple access type systems, but can also be used for point to point communications. Infrared is normally used for point to point, but broadcast applications within a room have also been developed.

i) Space environment implications. As long as the electronics in the transmitter and receiver are well protected, there should be no problems with radio or infrared transmission. The infrared noise from the sun could be a problem when the spacecraft is being directly illuminated. This needs to be investigated further.

1.7.1.1.2.3 Hybrid Media Applications for Space Station

An optimal networking solution for the space station may require more than one type of media. Communications within the habitation modules could be performed with optical fiber or coax, but to reach the opposite end of the space station, where the antennas are probably going to be located, may require traversing about 100 meters or so of free space, where the temperature range varies from -TBD^{o}c to +TBD^{o}c very quickly, according to the 90 minute orbital cycle. If a cable or fiber is used that cannot withstand these temperature extremes, the communication link would fail. An infrared or radio link may be a better alternative for this environment.

Power cables need to go to the antennas also, but the self-heating of a power cable may be enough to keep low temperatures above a certain minimum, so that the data could be carried by modulation over the d.c. power component. High temperatures could be a problem, however, when the station is on the "sun" side of the earth.

Clearly the final design will require very thorough thermal analysis, and thermal study of the selected media. Bending of the station structure will also have to be considered because of the potential stress it will place on connecting cables. Also if an infrared line of sight link is established, enough dispersion of the beam must be allowed so that bending will not disrupt reception. Redundant beams separated by a few meters may be required so that both paths will not become obstructed.

1.7.1.1.3 Projected Capabilities

1.7.1.1.3.1 Twisted Shielded Pair (TSP)

The current TSP technology is very mature and is not likely to change significantly in the 1987 or 1995-2000 time frame. TSP's limitations are physical rather than technological. For relatively low rate (under 1 Mbps) data communication, this is an inexpensive and proven technology.

1.7.1.1.3.2 Coaxial Cable

The current technology is mature and will only see minor improvement by 1987 or 1995-2000. Better dielectric materials will lead to some improvements in the performance of coax, but as in TSP, the limitations are inherently physical. Coax would find applications in medium rate baseband communications, broadband, and VHF/UHF television transmission.

1.7.1.1.3.3 Optical Fiber

Research in optical fiber is very significant, and breakthroughs are reported constantly. For long distance communications purposes, most of the research is directed towards lowering the attenuation of fiber so that long distance links with fewer repeaters can be built. Increasing the bandwidth of the transmitters and receivers is another present research goal. The improvements that this research will bring about by 1987 will include lower attenuation and higher bandwidth by perhaps a factor of 2 or 3 from present levels. The status by 1995-2000 is far harder to predict, but it can be assumed that optical fiber will be used for many more applications than today and will have gained widespread acceptance.

For the space avionics requirements, better connectors, splices, by-passes, multiplexers and demultiplexers will be necessary, however, if optical fiber is to be used in reconfigurable space vehicles. At present, optical fiber connectivity is one of the major problems limiting its use. Some topologies are difficult to configure with fiber, and until better connectors are available, this connectivity problem will continue to pose practical problems. The passive star, for example, is limited to about 32 nodes, and the bus is also limited in number of nodes because taps incur additive losses. Several companies have developed practical connectors, multiplexers, demultiplexers, by-pass switches, and fail-safe connectors. Substantially improved devices should be available by 1987, and this connectivity problem will probably be solved by 1995 or so.

1.7.1.1.3.4 Radio and Light Through Free Space

The radio technology is well understood, but radio frequency modems are still being improved upon. Infrared line of sight transmission will also see improvements in the transmitters and receivers in the next few years.

1.7.1.1.4 References

Keiser, Gerd. "Optical Fiber Communications." McGraw-Hill, 1983

Schwartz, Mischa. "Information Transmission, Modulation and Noise." McGraw-Hill, 1980

Stallings, William. "Local Networks - An Introduction." MacMillan Publishing, 1984

Finley, Marion R. Jr. "Optical Fiber in Local Networks." IEEE Communications Magazine, Vol. 22 #8, August 1984, pp 22-35.

"Space Station and Preliminary Design." NASA JSC RFP 9-BF-10-4-01P, September 15, 1984

"Space Station Reference Configuration Description." JSC-19989, August 1984

W. Vlasak, G. Pfister. "A Fiberoptic Local-Area-Network Solution for Tactical Command and Control Systems." SPIE Vol. 434, pp 24-40

H. D. Hendricks, N. D. Murray. "Wavelength Division Multiplexing for Future Space Station Data Systems." SPIE Vol. 434, pp 41-49

1.7.1.2 Network Interface Unit

1.7.1.2.1 Description

The Network Interface Unit (NIU) is a device that acts as a communications controller to provide data transmission to one or more attached devices (subscribers). The NIU transforms subscriber data rate and protocol to that of local network transmission medium and vice versa. Data on the medium are available to all devices.

The NIU can function as a gateway (providing interconnection of multiple networks that use different protocols) or as a bridge (providing interconnection of multiple networks that use the same protocols). The uses of an NIU in a communications network are shown in Figure 1. In general terms, the NIU performs the following functions.

- For data from the attached devices to the network.
    - Accepts data from attached devices/networks.
    - Buffers data until medium access is achieved.
    - Transmits data in addressed packets.
- For data from the network to the attached devices.
    - Scans each packet on medium for own address (and the address of any device on the other network in the case of bridges and gateways).
    - Reads packet into buffer.
    - Transmits data to attached devices/networks at the proper data rate.

In general, the discussion that follows applies to all orbital elements of the Space Station Program (SSP):

- The Space Station
- Co-orbiting Platform (COP)
- Polar Orbiting Platform (POP)

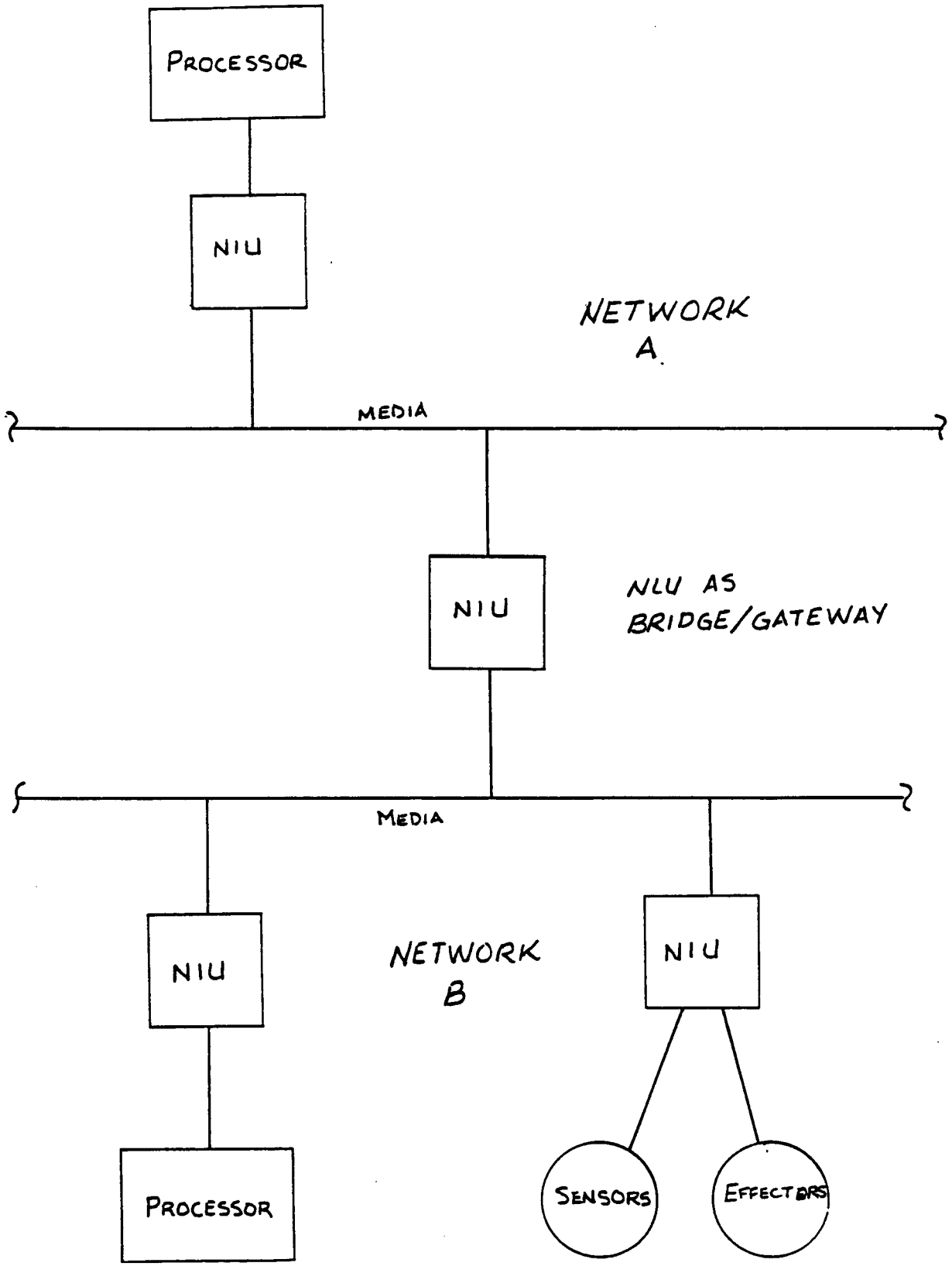


FIGURE 1. USES OF NIU

1.7.1.2.2 Option Characterization

First, a brief discussion of background material on modern layered structures for communications system is presented. Then, the following network interface devices are characterized.

- Advanced Information Processing System (AIPS)
- SubACS (Submarine Advanced Combat System)
- Destek
- Concord Data Systems
- Interlan
- Sytec
- Ungermann-Bass
- Contel Information Systems
- Complexx Systems
- Sperry

The NIU devices are characterized in matrix form to allow for easy comparison between manufacturers. The options considered are by no means inclusive, but are representative of NIUs in general. Layering The International Standards Organization/Open Systems Interconnect (ISO/OSI) model for communication systems is pertinent to the study of NIUs. The Open Systems Interconnect Model consists of seven distinct layers each performing a set of unique functions as shown in Figure 2. (ref. 9)

A layered architecture provides flexibility in revising the communications system. As long as the way information is passed between the layers is not affected, only the appropriate layer needs to be altered to implement a change. This provides the ability to continuously incorporate new technology into the existing system.

FIGURE 2

ISO/OSI MODEL

7	APPLICATIONS LAYER	o	Serves the end user application process
6	PRESENTATION LAYER	o	Performs data transformations
		o	Data translation
		o	Formatting
5	SESSION LAYER	o	Establishes connection, or session, between two presentation layers
		o	Manages the dialog
		o	Provides circuit fault recovery
4	TRANSPORT LAYER	o	Segmentation of message
		o	Flow control
		o	Error detection/control
		o	Multiplexing
3	NETWORK LAYER	o	Packetization of messages
		o	Routing
		o	Congestion control
2	DATA LINK LAYER	o	Framing
		o	Processes acknowledgement frames
		o	Error handling
		o	Media Access
1	PHYSICAL LAYER	o	The mechanical, electrical, and procedural interfacing to the media

The Physical and Data Link Layers (ISO/OSI) are implemented primarily in hardware, whereas, the upper layers are software intensive. The layers can also be grouped according to their functions. The four lower layers provide the connectivity between devices. The three upper layers allow for cooperation between devices and are, therefore, application dependent. (Ref. 1) Consequently, the division of layers between the NIU and host will be an important factor in determining the modularity/commonality of the NIU and the functions it performs. The alternatives for allocation are shown in the following tables.

NIU LAYER ALTERNATIVES

NIU 1

7	Application	
6	Presentation	
5	Session	Implemented in Host
4	Transport	
3	Network	
2	Media Access	
1	Physical	Implemented in NIU

- Software intensive layers (3-7) in host utilize host memory and CPU time
- Requires additional hardware incorporated in host to implement layer 2
- NIU unable to function as a bridge
- Unable to function as a gateway
- Requires intelligent host
- Host must be aware of the details of network topology and protocol
- Highest performance NIU (response time)
- Minimum size, weight, complexity ...
- Example. Fiber optic transmitter/receiver

NIU LAYER ALTERNATIVES (CONT'D)

NIU 2

7	Application	
6	Presentation	
5	Session	Implemented in host
4	Transport	
3	Network	
2	Media Access	Implemented in NIU
1	Physical	

- Software intensive layers reside in host
- Requires host memory and CPU time
- Host must be aware of the details of network topology and protocol
- Unable to function as bridge
  - Remote device unable to exercise flow control over the source device
  - Doesn't support multiplexing
- Unable to function as a gateway
- High performance NIU
- Requires intelligent host
- Host must be aware of the details of network topology and protocol
- Example.. AIPS

NIU LAYER ALTERNATIVES (CONT'D)

NIU 3

7	Application	
6	Presentation	Implemented in host
5	Session	
4	Transport	
3	Network	
2	Data link	Implemented in NIU
1	Physical	

- Upper layers implemented in host are "end to end" layers, unaffected by the details below.
- Host must be aware of the details of the network topology and protocol
- Functional as a bridge
- Unable to function as a gateway
- Supports simple digital I/O as well as intelligent hosts.
- Example. Station Mate (see Table 1)

NIU LAYER ALTERNATIVES (CONT'D)

NIU 4

7	Application	
6	Presentation	Implemented in host
5	Session	
4	Transport	
3	Network	Implemented in NIU
2	Data Link	
1	Physical	

- Layers 5–7 are application dependent. Implementation in the host allows for standardization of NIU software
- Requires less host memory and CPU time than NIU's 1,2,3
- Host is not aware of network topology and protocol
- Functional as a gateway
- Functional as a bridge
- Example. BIU/Control Information Systems (see Table 1)

NIU LAYER ALTERNATIVES (CONT'D)

NIU 5

7	Application	Implemented in host
6	Presentation	
5	Session	
4	Transport	
3	Network	Implemented in NIU
2	Data Link	
1	Physical	

- Many options exist at the session layer
- Requires minimum CPU time and host memory
- Functional as a bridge
- Functional as a gateway
- Example. SubACS
  TIM 220 (see Table 1)

At the session and presentation layers, many options exist for services. The functions performed by these layers are directly used and driven according to the application requirements. (Ref. 1) The presence of these layers in the NIU decreases its modularity. Therefore, the session layer is the highest layer considered in the NIU.

This paper has focused on the options for the allocation of functions between the network interface unit and the host using the ISO/OSI layered model as a reference. Many options exist within each layer for the implementation of these functions. However, the options for the implementation of the functions cannot be considered layer by layer but must be evaluated as a whole in a local area network because it is the net effect of these options which determines the LAN characteristics such as performance, cost, growth potential, etc....

The options for implementing the layers in the NIU are discussed in the LAN paper (2.5.3) and the distributed operating systems paper (2.1.3).

The Advanced Information Processing System (AIPS) designed by the Charles Stark Draper Laboratory (CSDL) is a fault tolerant processor complex which communicates using an Input/Output Network (1/O), an Intercomputer (IC) Network and a mass memory bus. Devices are connected to the networks via network interfaces. The IO and IC interfaces are interconnected by switching devices (nodes) as depicted in the proof of concept configuration shown in Figure 3. The nodes and interfaces are described below.

Each node in the proof-of-concept configuration has five input/output ports. Three independent nodes provide redundancy. The node performs the following functions:

- Receives data
- Checks for protocol conformity and transmission errors
- Regenerates signal
- Transmits data
- Enables/disables port transmitters as commanded
- Circuit switching for fault recovery
- Responds to error and status requests

AIPS. INTERCOMPUTER NETWORK INTERFACE

The IC network is a cross-connected set of nodes which uses circuit switching for recovery from node-to-node link faults. Attached processors transmit on only one of the triply redundant IC buses, yet listen to all three. The IC network interface performs the following functions.

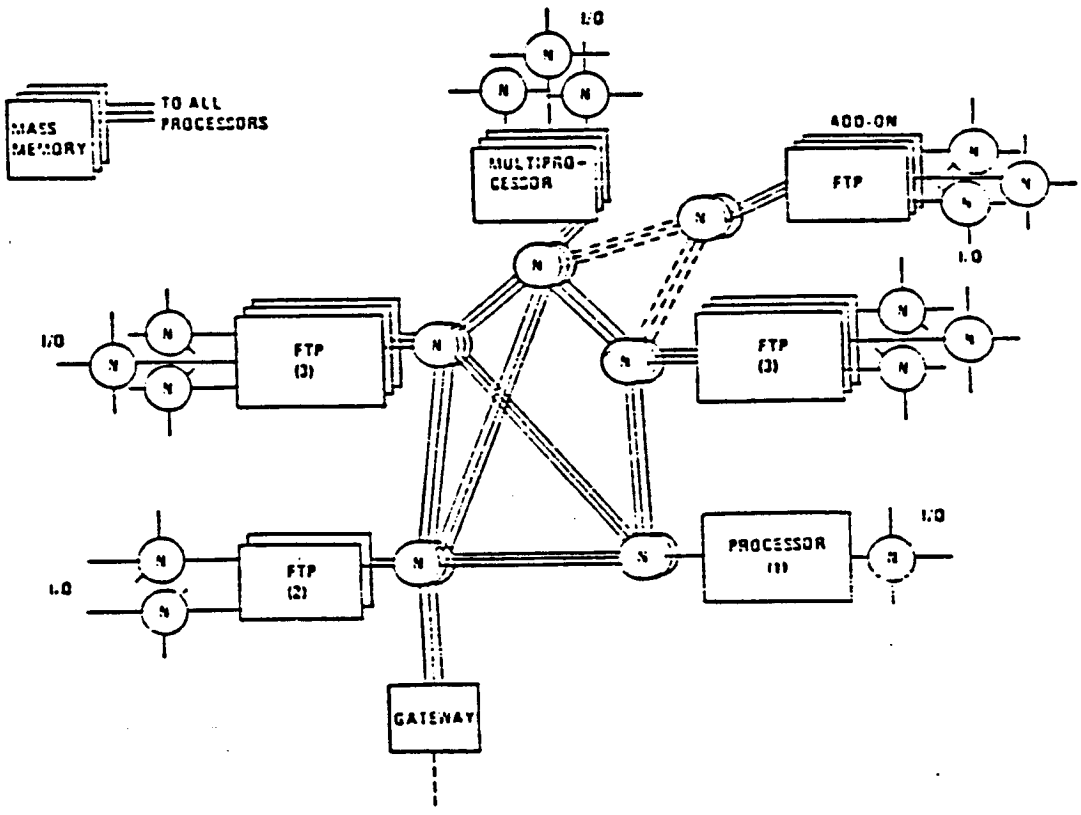


FIGURE 3 AIPS PROOF-OF-CONCEPT CONFIGURATION

- Receives data
- Checks for protocol conformity and transmission errors
- Performs a bit by bit comparison of the three data signals from the triply redundant network
- Converts Serial/Parallel Data
- Decodes addresses
- Transmits data and enforces a transmission length limitation
- Enables/disables functioning of the interface
- Contends for the network using the Laning Poll technique

AIPS. INPUT/OUTPUT NETWORK INTERFACE

The I/O network is a cross-connected set of nodes which uses circuit switching for recovery from node-to-node link faults. It is a simplex network in which only one I/O processor is enabled to receive or transmit during an I/O exchange. The I/O interface performs the following functions.

- Receives data
- Checks for protocol conformity and transmission errors
- Converts Serial/Parallel
- Transmits data and enforces a transmission length limitation
- Enables/disables functioning of the interface
- Contends for the network using the Laning Poll technique

The AIPS also includes a triplex multiplex bus which provides communication between the mass memory and the general purpose computers (GPC). The interface to this bus, the mass memory bus interface, performs essentially the same functions as the IC network interface except address decoding, which is not necessary.

In order to perform functions, the interfaces and nodes should contain the physical, data link, and network layers of the ISO/OSI model.

SubACS BIU CHARACTERIZATION

The SubACS bus interface unit (BIU) and network operating system (NOS) can be briefly characterized as a modular, intelligent unit for message distribution in a local area network. The BIU is the hardware component in which the NOS software executes. The BIU/NOS include functions through layer 5 of the ISO/OSI reference model.

The following discussion is for the BIU and NOS as they exist in late 1984. The network and its capabilities have planned upgrades that will affect some of the details, but not the overall concept of operation.

The primary purpose of the BIU is to interface any of several processors or devices to the distributed system data bus (DSDB) so that those components can communicate in performing their functions. The BIU has a modular design both at the interface to the transmission medium and at the interface to a processor or device. A core set of modules and functions is used for all BIUs. The BIU can be personalized to connect to any of several Navy standard processor/device interfaces by the inclusion of the appropriate standard card and NOS software. A different medium or data transfer rate can be used by including the appropriate interface card, such as one to talk over a fiber optics link or another to talk over a wire link. SubACS does not include gateways, because the network was designed to have compatible protocols throughout the system and therefore needs no conversion functions supplied by a gateway.

A bridge is a special case of a BIU which has been personalized with two media cards and the related NOS software in order to interface the transmission media of two networks. The bridge is used to selectively receive messages on one port for retransmission on the other port. SubACS includes both wire/fiber and fiber/fiber bridges between local area networks.

The NOS which executes in the BIU performs network failure management functions, in addition to normal message transmission and reception. At initiation of a connection between two ports, the NOS locates a path to establish as the virtual circuit, based on parameters of the new messages, and the failure status and loading of the parts of the network. At a failure, the NOS/BIU isolates the problem, reestablishes the virtual circuit, and continues operation automatically. Programs are moved to alternate machines at failure of a processor, if a suitable replacement is available. Failures are reported to the operator.

The BIU acts as a store and forward unit, first selectively receiving a message into a buffer in the BIU from the medium or attached device, then forwarding the message when the channel is available to its final destination. When functioning as a bridge, the NOS has the knowledge of which messages are to be ignored, and which are to be forwarded through to the other port after reception. The information about which processes and devices are active at each port is maintained dynamically as processes are activated or deactivated and as hardware is turned on or off or fails.

The BIU/NOS maintains a common time within the network by periodic equalization of local times to common reference. This time is used for various logs, allowing identification of the order of events across the network for problem analysis and evaluation of such performance parameters as time delays of messages.

FODS BIU

The Fiber Optic Demonstration System (FODS) is a high speed Fiber Optic Data Bus which is being developed by Sperry under the direction of NASA Goddard Space Flight Center. The network consists of fiber optic links interconnected by a passive star coupler. Communication devices are interfaced to the media by the BIU's.

FODS uses a Carrier Sense Multiple Access with Collision Detection and Time Slots (CSMA/CD/TS described in 2.5.3) media access method. "The BIUs can operate in either of two modes: Random Access or Controlled Access. BIUs switch to the controlled access mode when a collision occurs on the bus. When all BIUs have had one opportunity to transmit in the controlled access mode, the BIUs return to the random access mode." (Ref. 12)

The BIU consists of a network interface and a front-end-processor. Messages are transmitted and received by the network interface. The network interface also performs the following functions.

- o Packetization of messages
- o Media access
- o Error detection
- o Acknowledgements

The front-end-processor performs protocol adaptations for data transfer and it can provide routing decisions. Thus, the FODS BIU implements layers 1 and 2 of the ISO/OSI model with the possibility for future expansion to include Layer 3.

Characterization of other NIUs

The following pages list a number of NIU alternatives from commercial manufacturers. An explanation of the entries used in the comparison matrices is given below.

ISO/OSI layers. In some centrally-controlled networks, the NIU supports only the physical connection. In most networks with distributed control, the NIU supports the Physical and Data link layers. Some very intelligent NIUs control the Network, Transport, and even Session and Application layers for their attached devices.

Communications protocol. A number of protocols are available for local area networking from both vendors and standards groups. The most popular are Xerox Network System and X.25. Some vendors offer Proprietary protocols at the Transport layer.

Access method: Committee 802 of the IEEE is attempting to standardize protocols for local area networking. Current protocol standards include 802.3 (a CSMA/CD standard resembling Ethernet), 802.4 (a standard for token-passing bus networks). and 802.5 (a standard for token-passing ring networks).

Topology: This refers to the physical network layout and node connectivity. Possible network topologies are star, ring, bus, tree, loop, and grid.

Level of redundancy: The additional number of extra equipment to provide tolerance of faults.

Data transmission medium: This entry lists the transmission medium used for the network's principal data channel.

Data transmission technique. Possible network data transmission techniques are baseband and broadband.

Data transmission rate: This entry lists maximum raw aggregate throughput that the network can support in bits per second (bps). Depending on the network, not all of this capacity may be available for end user communications.

Video/voice distribution.. A number of networks can support voice or video applications in addition to data communications. Voice applications include one- and two-way analog or digitized voice. Video applications, usually available only on broadband networks, include one- and two-way full motion, slow-scan and freeze-frame video.

Backend interfaces. This entry lists the specific end-user interfaces the NIU can support (e.g., RS-232-C, CCITT v.35, etc.).

Units installed. Most vendors regard installed-base information as proprietary. This entry lists the total number of network stations or nodes the vendor has installed.

Table 1 provides the characterization of twelve (12) commercial NIU's. The entires were derived from information received from each vendor. Reference 7 provides a brief description of a large number of commercial NIU's.

AIPS/SUBACS/SPERRY COMPARISON

Table 2 provides a summary comparison for the AIPS, SuBACS and Sperry NIU's. The comparison matrix approach for the commercial NIU's was applied.

1.7.1.2.3 Projected Capabilities

Standards for the ISO/OSI layers are currently being developed. For example, the IEEE 802 standards specify the physical and data link layers for various topologies. (Ref. 2) As standards evolve for the higher layers, a truly "open" system can be achieved. However, no existing communication system implements all seven ISO/OSI layers. (Ref. 3)

1.7.1.2.4 References

1. Francois, P. and A. Potocki. "Some Methods for Providing OSI Transport in SNA", IBM Journal of Research and Development, Vol. 27, No. 5, Sept. 1983. pp. 452 - 463.

2. Graube, Maris and Michael C. Mulder. "Local Area Networks," IEEE Computer Oct. 1984

NIU/ Manufacturer	IOS/OSI Layers	Comm. Protocol	Access Method	Network Topology	Level of Redundancy	Data Trans. Media	Data Trans. Tech.	Data Trans. Rate	Video/ Voice Interface	Backend Interfaces	Physical Specifications W" H" D" Weight (lbs)	Power Requirements	Environmental Specifications	Units Installed
NTS 10/ InterLan	1-7	XNS	CSMA/CD	Bus	0	Coax (Ethernet)	Base-band	10 Mbps	None	-RS-232 (up to 8)	13.25 2.5 11.5	110/220 VAC 60 Hz 55 W max	Operating temp.: -0-40 deg C Rel. humidity: -90%	>200
PCU/ Sytek	1-6	HDLC X.25	CSMA/CD	Tree	0	CATV	Broad-band	2 Mbps	Can coexist	-RS-232 (up to 8)		115 VAC • 60 Hz 220 VAC • 60 Hz	Operating Temp.: -0-40 deg C Rel. humidity: -95%	
BIU/ Contel Information Systems	1-4	X.25	CSMA/CD	Bus	0	CATV Fiber Optic	Broad-band	10 Mbps	Can coexist	-RS-232 (up to 32)				

Table 1: Commercial NIU's

Table 1 (continued)

NIU/ Manufacturer	IOS/OSI Layers	Comm. Protocol	Access Method	Network Topology	Level of Redundancy	Data Trans. Media	Data Trans. Tech.	Data Trans. Rate	Video/ Voice Interface	Backend Interfaces	Physical Specifications W" H" D" Weight (lbs)	Power Requirements	Environmental Specifications	Units Installed
StationMate/ Complexx Systems	1-3	X.25	CSMA/CD	Bus	0	2-pair shielded wire	Base-band	1 Mbps	None	-RS-232 (up to 3)				
NIU-2/ Ungermann-Bass	1-7	Async Bisync HDLC SDLC DDCMP X.25 SNA	CSMA/CD	Bus/ Tree	0	Coax CATV Fiber Optic	Base-band Broad-band	10 Mbps 5 Mbps	Can coexist	-RS-232 -RS-449 /422 -V.35 -IEEE-488 -DR11-W -DR11-B -Parallel 8,16,32 24 users per NIU	16.7 8.4 25.9 40	115 VAC • 3 A max 230 VAC • 1.5 A max 100 VAC • 3 A max 250 W max	Operating temp.: -10-40 deg C Rel. humidity: -5-80%	> 2900 base-band > 100 broad-band (all models)
NIU-150/ Ungermann-Bass	1-7	Async Bisync HDLC SDLC DDCMP X.25 SNA	CSMA/CD	Bus/ Tree	0	Coax CATV Fiber Optic	Base-band Broad-band	10 Mbps 5 Mbps	Can coexist	-RS-232 -RS-449 /422 -V.35 -IEEE-488 -DR11-W -DR11-B -Parallel 8,16,32 6 users	17 5.2 14 26	115 VAC • 3 A max 230 VAC • 1.5 A max 100 VAC • 3 A max 100 W max	Operating temp.: -20-65 deg C Rel. humidity: -5-80%	See NIU-2

NIU/ Manufacturer	IOS/OSI Layers	Comm. Protocol	Access Method	Network Topology	Level of Redundancy	Data Trans. Media	Data Trans. Tech.	Data Trans. Rate	Video/ Voice Interface	Backend interfaces	Physical Specifications W" H" D" Weight (lbs)	Power Requirements	Environmental Specifications	Units installed
NIU-130/ Ungermann-Bass	1-7	Async Bisync HDLC SDLC DDCMP X.25 SNA	CSMA/CD	Bus Tree	0	Coax CATV Fiber Optic	Base-band Broad-band	10 Mbps 5 Mbps	Can coexist	-RS-232 (up to 2)	9.5 3.3 12.5 6.5	115 VAC • .5 A max or 230 VAC • .25 A max 100 VAC or • .5 A max (seperate trans-former) 56 W max	Operating temp.: -0-40 deg C Rel. humidity: -5-80%	See NIU-2
Personal NIU/ Ungermann-Bass	1-7	XNS	CSMA/CD	Bus	0	Coax CATV Fiber Optic	Base-band Broad-band	10 Mbps 5 Mbps	Can coexist	Single-board interface for PC's	4.2 13.3	5 V • 2.7 A 12 V • .5 A	Operating temp.: -0-55 deg C Rel. humidity: -5-80%	See NIU-2
TIM-220/ Concord Data Systems	1-5	ECMA	Token-passing	Tree	0	CATV	Broad-band	5 Mbps	Can coexist	-RS-232 -RS-449 /422 (up to 12)	15 5.5 16.25 15	115/220 VAC 70 W max	Operating temp.: -0-50 deg C Rel. humidity: -0-90%	1983 New product

Table 1 (continued)

Table 1 (continued)

NIU/ Manufacturer	IOS/OSI Layers	Comm. Protocol	Access Method	Network Topology	Level of Redundancy	Data Trans. Media	Data Trans. Tech.	Data Trans. Rate	Video/ Voice Interface	Backend Interfaces	Physical Specifications W" H" D" Weight (lbs)	Power Requirements	Environmental Specifications	Units Installed
NIS/ Destek	1-2	HDLC SDLC	CSMA/CD	Bus	0	Coax Fiber Optic	Base-band Broad-band	2 Mbps	Can coexist	-RS-232 -RS-422 -Modem -IEEE -488 -Parallel (Centronics)	11 3.25 5.55 2.25	115 VAC • .25 A max	Operating temp.: -0-55 deg C Rel. humidity: -90%	
Bridge/ Ungermann-Bass		HDLC X.25	CSMA/CD	Bus Tree	0	Coax CATV Fiber Optic	Base-band Broad-band	504 Kbps	Can coexist	-RS-232 -RS-449 /422 -V.35 (Connects 2 LAN's)	17 5.2 14 21	Same as NIU-150	Operating temp.: -0-40 deg C Rel. humidity: -5-80%	See NIU-2
Gateway/ Ungermann-Bass		X.25	CSMA/CD	Bus Tree	0	Coax CATV Fiber Optic	Base-band Broad-band	64 Kbps	Can coexist	-RS-232 -RS-449 /422 -V.35 (Connects LAN or X.25 host to PDN)	16.7 8.4 25.9 40	Same as NIU-2	Operating temp.: -10-40 deg C Rel. humidity: -5-80%	See NIU-2

Table 2: Non-commercial NIU's

NIU/ MANUFACTURER	IOS/OSI LAYERS	ACCESS METHOD	NETWORK TOPOLOGY	LEVEL OF REDUNDANCY	DATA TRANS.	DATA TRANS.	DATA TRANS.	VIDEO/ VOICE INTERFACE	BACKEND INTER-FACES	POWER REQUIREMENTS	ENVIRONMENTAL SPECIFICATIONS
SubACS/ IBM	1-5	Priority arbitration	Multiple buses (passive star)	1-2 (NIU is simplex path is redundant)	Fiber Optic wire	Baseband	64 Mbps	None	Navy devices, processors	Approx. 300W	Operating temp.: MIL-STD Rel. humidity: MIL-STD
AIPS/ CSD Laboratory	1-3	Laning Poll	Mesh	1-3 (NIU is simplex network is redundant)		Baseband	3 Mbps (later to 100)	Planned			Operating temp.: MIL-STD Rel. humidity:
FODS Sperry	1-2 increasing	CSMA/ CD/TS	Bus (passive star)	1-2 (NIU is simplex network is redundant)	Optical Fiber	Baseband	100 Mbps (later to 300)	Possibly	RS232 & a DMA high speed interface	35W (later decreased by 1/3)	Operating temp.: Rel. humidity

3. "AIPS Technology Survey Report," Charles Stark Draper Laboratory, Inc., Cambridge, Mass. NASA - JSC NAS9-16023.

4. "AIPS System Specification," Charles Stark Draper Laboratory, Inc., Cambridge, Mass. NASA - JSC NAS9-16023.

5. Tanenbaum, Andrew S. Computer Networks. Prentice-Hall, Inc., Englewood Cliffs, N.J., 1981.

6. Stallings, William. Local Networks. Macmillan Publishing Co., N.Y., N.Y., 1984

7. Data-Pro Research Corp., Delran, N.Y., 1983

8. Submarine Advanced Combat System Navy Program

9. ISO Reference Model of Open-Systems Interconnection ISO/TC97/SC16, DP 7498; available from the American National Standards Institute, 1430 Broadway, New York, NY 10018

10. "FODS Industry Briefing", Sperry Flight Systems.

11. Rende, John. Goddard Space Flight Center. Greenbelt, MD.

12. Bhatia, Veena. "FODS Simulation. Requirement Specification," May 15, 1984

1.7.2 DELETED