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Acquisition Times of Carrier Tracking Sampled Data Phase-Locked Loops

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Phase acquisition times of type II and III loops typical of the Advanced Receiver are studied by computer simulations when the loops are disturbed by gaussian noise. Reliable estimates are obtained by running 5000 trials for each combination of loop signal-to-noise ratio (SNR) and frequency offset. The probabilities of acquisition are shown versus time from start of acquisition for various loop SNRs and frequency offsets. For frequency offsets smaller than one-fourth of the loop bandwidth and for loop SNRs of 10 dB and higher, the loops acquire with probability 0.99 within $2.5/B_L$ for type II loops and within $7/B_L$ for type III loops.

I. Introduction

During the acquisition mode, the nature of the phase-locked loop is highly nonlinear. This is further complicated by the presence of noise, thus precluding a detailed analysis of the behavior of the loop during this mode of operation.

Very little analytical work has been published in the open literature on the subject of acquisition. Viterbi (Ref. 1) and Lindsey (Ref. 2), among others, developed approximate expressions for the time necessary to acquire in a noiseless environment. Their expressions are useful when the frequency offset is large compared to the bandwidth of the loop. Hurd and Anderson (Ref 3) and Holmes (Ref. 4) present results of acquisition experiments in a noisy environment for a digital transition tracking loop (DTTL) symbol synchronizer and continuous time carrier tracking loops, respectively. Although all previous sources serve as a general guidance, more specific results are needed for the proposed carrier tracking loops of the DSN Advanced Receiver (Ref. 5).

In this article, we show results based on Monte Carlo simulations of phase acquisition for types II and III sampled data loops typical of the Advanced Receiver, where the type of loop indicates the number of perfect integrators present, including that contributed by the NCO. Plots of probability of acquisition versus normalized time are presented with initial frquency detuning (frequency offset) as a parameter, for different loop signal-to-noise ratios.

II. Description of the Sampled Data Loop Model

A block diagram of the nonlinear baseband model employed in the simulation is shown in Fig. 1. The symbols contained in the diagram are defined as follows:

A = rms value of carrier signal (V)

$\theta_n = \phi_0 + \Omega_0 t_n$

= input phase at time t_n (rad)

ϕ_0 = initial phase offset (rad)

Ω_0 = initial frequency detuning (rad/s)

ϕ_n = phase estimation error at time t_n (rad)

AK = loop gain

W_n = zero mean white gaussian noise sample with variance $N_0/2T$

T = update time (s)

$$F(z) = G_1 + \frac{G_2}{1-z^{-1}} + \frac{G_3}{(1-z^{-1})^2}$$

= loop filer (1)

$$N(z) = T(z+1)/2z^2(z-1)$$

= NCO transfer function including the transport lag of the loop (2)

The loop modeled in Fig. 1 is the proposed implementation for the carrier tracking loop of the Advanced Receiver (Ref. 5). Operationally, the behavior of the loop is characterized by

$$\phi_n = \theta_n - \hat{\theta}_n \tag{3}$$

$$\phi_n = \theta_n - AKF(z)\{\sin(\phi_n) + W_n/A\}N(z) \tag{4}$$

The PLLs considered are sampled data analogies of continuous time loops. For the type II and III loops with update time T, sampled data PLLs analogous to continuous loops of one-sided bandwidth b/T Hz have parameters (see Appendix for details):

$$AKTG_1 = rd \tag{5a}$$

$$AKTG_2 = rd^2 \tag{5b}$$

$$AKTG_3 = krd^3 \tag{5c}$$

$$d = \frac{4b}{r}\left(\frac{r-k}{r-k+1}\right) \tag{6}$$

where r is the damping parameter, and k is a type III loop gain component ($k=0$ for type II loop). The actual loop noise bandwidths, B_L, of the sampled data loops are given by:

$$B_L = \frac{1}{2T}\frac{1}{H^2(1)}\frac{1}{2\pi j}\oint_{|z|=1} H(z)H(z^{-1})\frac{dz}{z} \tag{7}$$

where $H(z)$ is the closed loop transfer function. These bandwidths are approximately b/T for $b \ll 1$, and are somewhat wider for larger b. The analogy is used so that the typical continuous loop parameters (Ref. 6 and TR 900-450[1]) can be specified as inputs to perform the simulations (note that B_L and b here correspond to $B_L{}^*$ and $B_L T$ of Ref. 5).

III. Description of Simulation

Introducing the state variables u_n, v_n, defined as the outputs of the first and second integrators in the loop filter $F(z)$, it can be shown (see Appendix) that the difference equations describing the behavior of the PLL are given by:

$$u_n = u_{n-1} + rd^2 d_n \tag{8}$$

$$v_n = v_{n-1} + kdu_n \tag{9}$$

$$y'_n = rdd_n + u_n + v_n \tag{10}$$

$$d_n = \sin(\phi_n) + W_n/A \tag{11}$$

$$\hat{\theta}_{n+1} = \hat{\theta}_n + (y'_{n-1} + y'_{n-2})/2 \tag{12}$$

The simulations were conducted by solving Eq. (4) with help from Eqs. (8)–(12) with zero initial conditions for the state variables.

In order to obtain accurate estimates, 5000 independent runs, produced by 5000 nonoverlapping sequences of pseudo-random noise, were employed to generate a single probability of acquisition curve for a given frequency offset and loop signal-to-noise ratio SNR $= A^2/N_0 B_L$. The phase offset for each run was randomly selected between $(-\pi, \pi)$.

To assure phase locking, each simulation was run for a maximum of $50/B_L$. The loop was declared to be in lock when the magnitude of the phase error dropped below 90 deg for at least $10/B_L$. This threshold is arbitrarily chosen so that PLLs operating with small loop SNRs (large variance of the tracking phase error) may be studied.

The simulations were performed on a VAX 11/750 computer. To generate the noise samples, a gaussian noise generator was synthesized using the direct method (Ref. 7) based on

[1] Tausworthe, R. C., and Crow, R B, *Practical Design of Third Order Phase-Locked Loops*, Technical Report 900-450, Jet Propulsion Laboratory, Pasadena, Calif, Apr 27, 1971.

the uniform random number generator provided by the VAX 11/750. The simulations were run for $B_L T = 0.02$, which is representative of the numbers presently imposed by both hardware speed (which influences T) and bandwidth requirements to track input dynamics.

IV. Summary of Results

Figures 2–5 present the distribution functions resulting from simulations of phase acquisitions. The ordinates of these figures are the probability of phase acquisitions occurring within time t. Time t, as indicated on the abscissa, is normalized by the bandwidth of the loop. For example, consider a type II loop with bandwidth B_L = 50 Hz, a loop SNR of 10 dB, and a frequency offset of 25 Hz, or $B_L/2$. From Fig. 3(b), phase acquisition with probability of 0.95 is achieved at $B_L t = 3$ or $t = 3/B_L = 0.06$ s. The figures show that for the normal range of loop SNRs, greater than 10 dB, and for frequency offset values smaller than one-half the loop bandwidth, the loops attain phase lock with high probability (0.99) within $5/B_L$ or $15/B_L$, for type II and type III loops, respectively. Acquisition times are approximately reduced by one-half if the offset is reduced to $B_L/4$.

Larger frequency offsets may require an excessive time to lock. Aiding of acquisition by sweeping the local oscillator or by estimating the frequency offset by a fast Fourier transform (FFT) is indicated when the frequency offset is large. Since type II loops lock faster than type III loops, it is often useful to acquire with a type II loop and then change to a type III. This can be done without loss of phase lock.

Our results are in close agreement with the earlier results for symbol synchronizers and for continuous time PLLs. This is not surprising for the continuous time PLL since for small values of $B_L T$ the sampled data loop behaves very similarly.

If we use equations (3.21) and (10–18) of Refs. 1 and 2, respectively, we can get an upper bound for the necessary time to phase lock a noiseless type II continuous time PLL. These equations show that when the frequency offset equals the loop bandwidth, and $r = 2$, the loop locks in $7.9/B_L$. The simulations indicate $9.2/B_L$ with probability 0.99 when the loop SNR = 16 dB.

Although the DTTL symbol synchronizer does not possess a sinusoidal characteristic for its phase detector, in Ref. 3 it was found that for low symbol SNR, acquisition is obtained in about $7/B_L$ for an optimized midphase integration window of one-quarter of the symbol time and a frequency offset of $B_L/2$. Large symbol SNRs require roughly $0.6/B_L$ for the same frequency offset. Interpolation of the data of Ref. 4 indicates that a continuous loop locks in $3.8/B_L$ when SNR = 10 dB and the frequency detuning is $B_L/2$. The close agreement in acquisition times adds confidence in the results.

References

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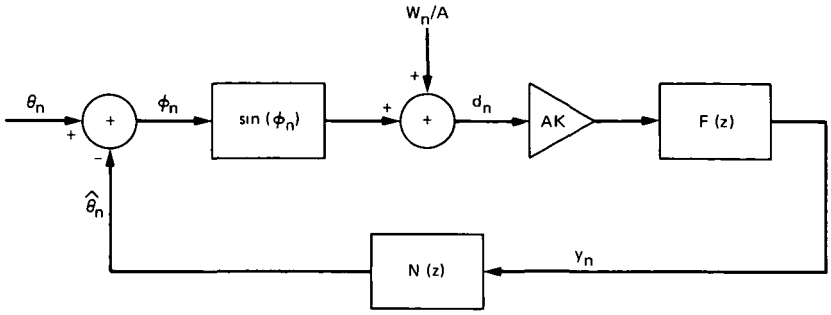

Fig. 1. Nonlinear baseband sampled data loop model

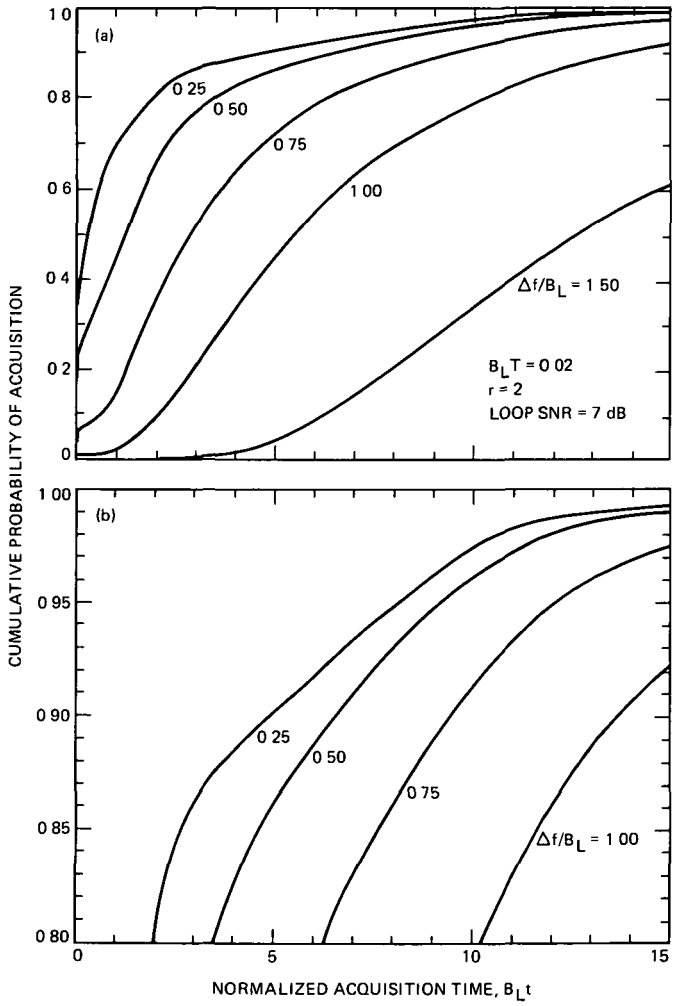

Fig. 2. Cumulative probability of phase acquisition as a function of normalized time for type II sampled data loop at 7-dB loop SNR: (a) Probability range 0 to 1, (b) Expansion of high probability region

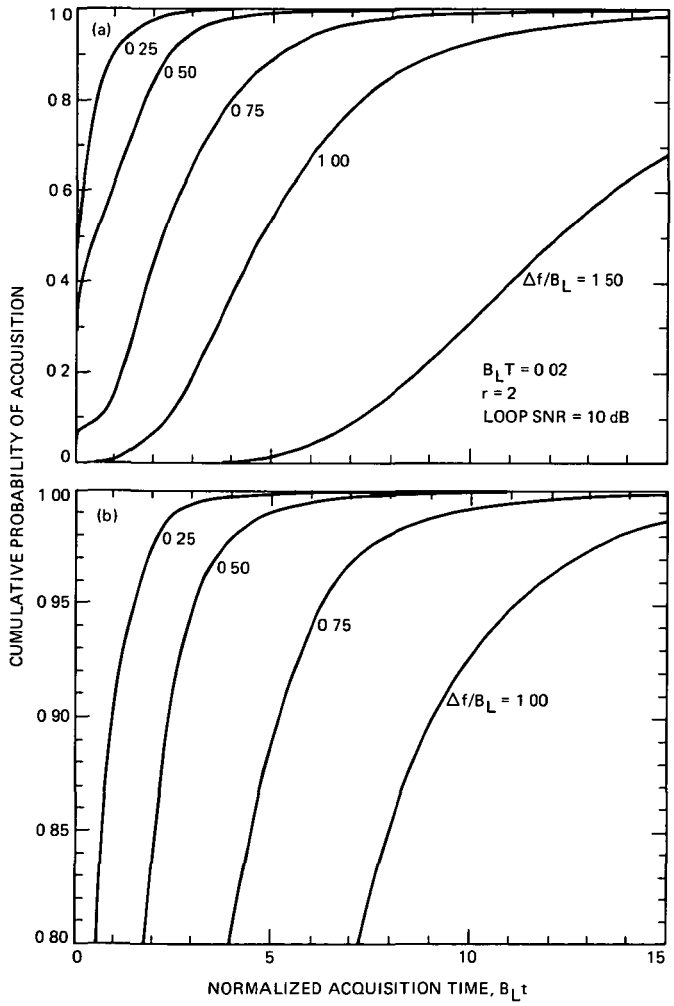

Fig. 3. Cumulative probability of phase acquisition as a function of normalized time for type II sampled data loop at 10-dB loop SNR: (a) Probability range 0 to 1, (b) Expansion of high probability region

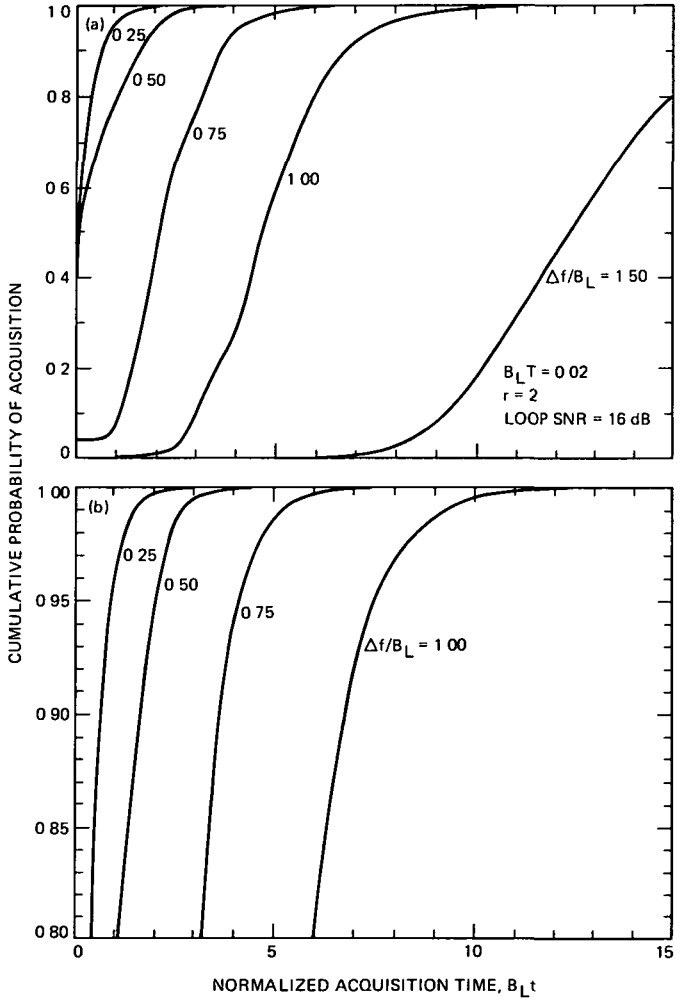

Fig. 4. Cumulative probability of phase acquisition as a function of normalized time for type II sampled data loop at 16-dB loop SNR: (a) Probability range 0 to 1, (b) Expansion of high probability region

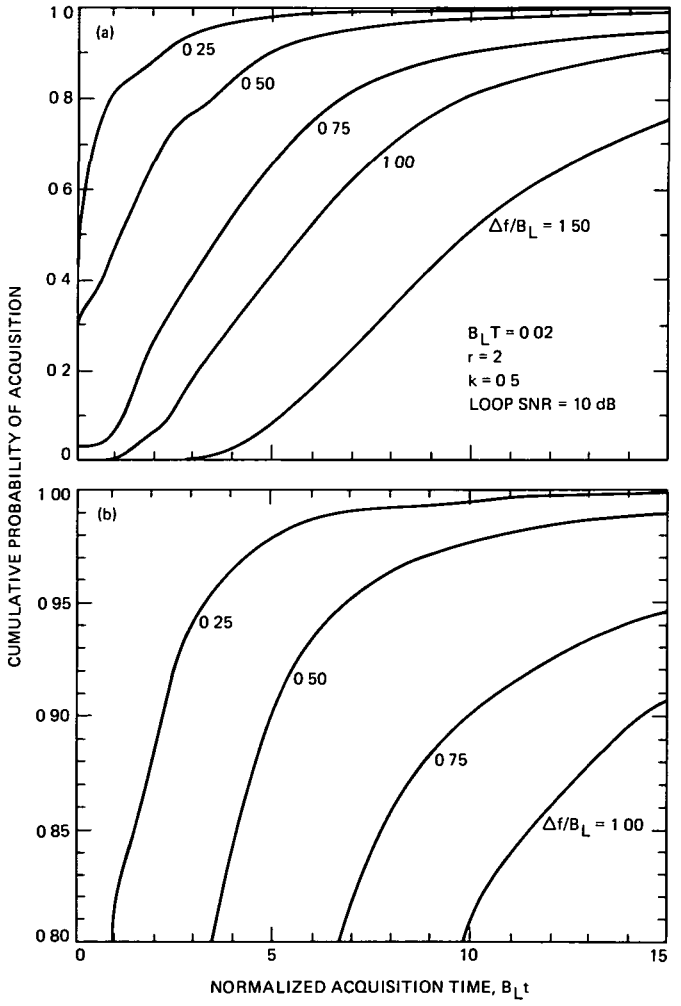

Fig. 5. Cumulative probability of phase acquisition as a function of normalized time for type III sampled data loop at 10-dB loop SNR: (a) Probability range 0 to 1, (b) Expansion of high probability region

Appendix

Setup of Equations for Simulation

From Ref. 4 and TR 900–450, a type II loop filter of a continuous time PLL can be expressed as

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s} + \frac{1}{\tau_1 \tau_3 s^2} \tag{A-1}$$

which is related to the commonly used parameters

$$r = AK\tau_2^2/\tau_1 \tag{A-2}$$

$$k = \tau_2/\tau_3 \tag{A-3}$$

$$\frac{b}{T} = \frac{r}{4\tau_2}\left(\frac{r-k+1}{r-k}\right) \text{ one-sided loop bandwidth} \tag{A-4}$$

Define

$$G_1 = \tau_2/\tau_1 \tag{A-5}$$

$$G_2 = T/\tau_1 \tag{A-6}$$

$$G_3 = T^2/\tau_1\tau_3 \tag{A-7}$$

Substitution of Eqs. (A-2)–(A-7) into the transfer function of the sampled data loop filter $F(z)$ produces Eq. (5). Notice that the term AKT was absorbed by the filter coefficients. With this in mind, define

$$\frac{Y'(z)}{D(z)} = AKTF(z) = rd + \frac{rd^2}{1 - z^{-1}} + \frac{krd^3}{(1 - z^{-1})^2} \tag{A-8}$$

where $Y'(z) = TY(z)$ (see Fig. 1), from which Eqs. (8)–(12) follow easily. These, in conjunction with Eq. (4), are the required equations for simulation.