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(NHB-5300.4(3K)) DESIGN REQUIREMENTS FOR RIGID PRINTED WIRING BOARDS AND ASSEMBLIES (National Aeronautics and Space Administration) 98 p HC A05/MF A01; also available SOD HC $5 as 0 CSCL 09A G3/33

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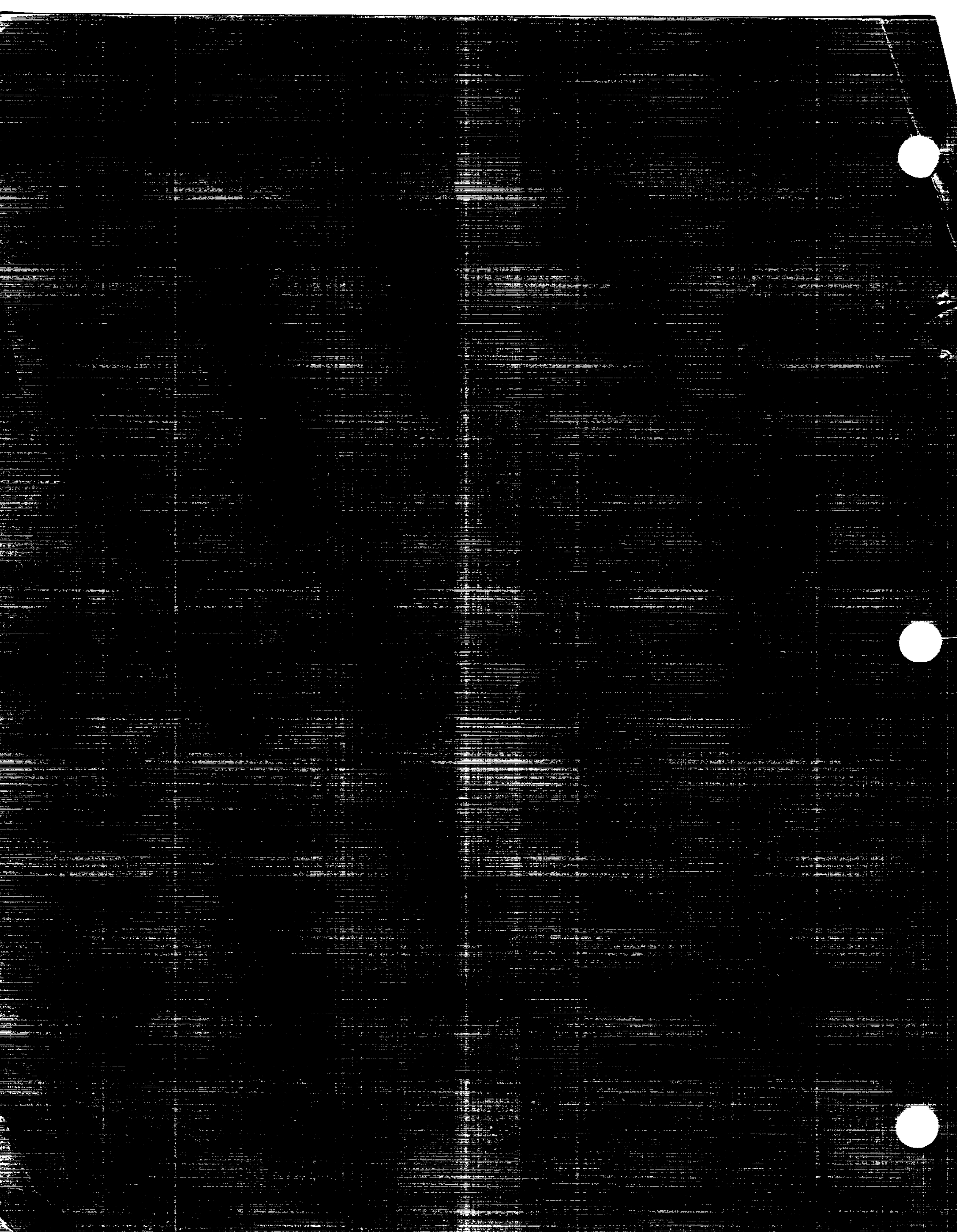

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PREFACE

Effective Date: January 7, 1986

Expiration Date: January 7, 1989

In order to maintain the high standards of the NASA printed wiring programs, this publication:

Prescribes NASA's requirements for assuring reliable rigid printed wiring board design.

Describes and incorporates basic considerations necessary to assure reliable rigid printed wiring board design.

NASA installations shall:

Invoke the provisions of this publication in procurements involving rigid printed wiring boards for aircraft, spacecraft, launch vehicles, mission essential support equipment, and elements thereof as appropriate to design or project requirements.

Amend, when timely and within cost constraints, existing contracts to invoke the requirements of this publication.

Utilize the provisions of this publication for in-house printed wiring design.

Assure that NASA contractors invoke the provisions of this publication in their subcontracts and purchase orders.

Furnish copies of this publication, in the quantities required, to NASA contractors, subcontractors, and subtier suppliers.

Questions concerning application of this publication to specific procurements shall be referred to the procuring NASA installation or its designated representative.

This publication shall not be rewritten or reissued in any other form.

Copies of this publication are available from the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

Milton A. Silveira
Chief Engineer

DISTRIBUTION:

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ORGANIZATION OF THE R&QA MANUAL

OVERALL COVERAGE

The Reliability and Quality Assurance Manual - referred to as the "R&QA Manual" - is the overall generic title which identifies all NASA R&QA management publications published under the basic R&QA subject classification code. The publications are grouped by major subject breakdown and further divided into specific categories identified as Parts. These Parts (not a complete R&QA Manual) are published as individual R&QA publications.

The following list shows the grouping and R&QA publications:

Title

Volume 1 - General Provisions

Title	Number
Reliability Program Provisions for Aeronautical and Space System Contractors	NHB 5300.4(1A) DECEMBER 1985
Quality Program Provisions for Aeronautical and Space System Contractors	NHB 5300.4(1B) DECEMBER 1985
Inspection System Provisions for Aeronautical and Space System Materials, Parts, Components and Services	NHB 5300.4(1C) DECEMBER 1985
Safety, Reliability, Maintainability and Quality Provisions for the Space Shuttle Program	NHB 5300.4(1D-2) DECEMBER 1985

Volume 2 - Government Agency Provisions

Title	Number
Quality Assurance Provisions for Government Agencies	NHB 5300.4(2B) DECEMBER 1985

Volume 3 - Standards

Title	Number
Requirements for Soldered Electrical Connections	NHB 5300.4(3A-1) DECEMBER 1985

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Qualified Products Lists Requirements for Microcircuits	NHB 5300.4(3F) DECEMBER 1985
Requirements for Interconnecting Cables, Harnesses, and Wiring	NHB 5300.4(3G) DECEMBER 1985
Requirements for Crimping and Wire Wrap	NHB 5300.4(3H) DECEMBER 1985
Requirements for Printed Wiring Boards	NHB 5300.4(3I) DECEMBER 1985
Requirements for Conformal Coating and Staking of Printed Wiring Boards and Electronic Assemblies	NHB 5300.4(3J) DECEMBER 1985
Design Requirements for Rigid Printed Wiring Boards and Assemblies	NHB 5300.4(3K) JANUARY 1986

DOCUMENT REFERENCING

Each R&QA Manual Part is assigned its own identification number within the basic classification code. The numeric-alpha suffix within a parenthesis identifies the grouping of the publication, that is, the volume and part, such as NHB 5300.4(3A): This number indicates that this is the first "Standards" (Volume 3) publication to be issued.

When a part is revised, the suffix identification will be changed to indicate the revision number, such as NHB 5300.4(3A-1).

In referencing or requesting any R&QA publication, the complete specific NHB number must be used.

PARAGRAPH REFERENCING

1. **Within the R&QA Manual.** The following shows the paragraph numbering system applicable to all R&QA publications.

3 A 3 01 1a(1)(a)

Volume 3
Part
Chapter 3
Paragraph 301
Subparagraphs

This system provides for referencing any R&QA publication requirement (paragraph) in any other R&QA publication without the need for identifying the NHB number, title, the volume number, or part. However, when referencing a complete Part within another R&QA publication, the specific NHB number must be used.

2. **In Other NASA Documents.** When it is necessary to reference an R&QA publication requirement (paragraph) in any other NASA document, the specific NHB number and paragraph number must be used together as follows: ''NHB 5300.4(3A-1), paragraph 3A301-1a(1)(a),'' or ''paragraph 3A301-2b of NHB 5300.4(3A-1).''

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CHAPTER 1: BASIC PRINCIPLES

3K100 APPLICABILITY AND SCOPE

1. **Applicability.** This publication is applicable to NASA programs involving the design of electronic components incorporating rigid single-sided, double-sided, and/or multilayer copper clad printed wiring boards and assemblies, and where invoked contractually in procurements. The assemblies designed in conformance with this standard are intended for use in aircraft, spacecraft, launch vehicles, and mission-essential support equipment.

2. **Scope.** This publication sets forth requirements for the design of rigid printed wiring boards and assemblies.

3. **Special Requirements.** Special requirements may exist which are not covered by or are not in conformance with the requirements of this publication. *Design documentation shall contain the detail for such requirements, and they shall take precedence over conflicting portions of this publication when they have been approved in writing by the procuring NASA installation.*

   When the design deviates from this standard, a design verification test program, approved by the procuring NASA installation, shall be conducted to provide objective evidence and data to substantiate that reliability will not be compromised. These tests may include, but not be limited to, thermal cycling, moisture conditioning, and mechanical stress, as appropriate,to mission requirements.

3K101 CLASSIFICATION

Printed wiring boards shall be of the types specified as follows:

a. Type 1 - single-sided board.

b. Type 2 - double-sided board.

c. Type 3 - multilayer board.

3K102 PRINCIPLES OF RELIABLE DESIGN FOR PRINTED WIRING BOARDS AND ASSEMBLIES

1. **Factors Controlling Reliability.** Reliable printed wiring boards result from proper design and control of processes, tools, materials, work environment, and workmanship.

2. **Design Considerations.** The basic design considerations to assure reliable printed wiring boards and assemblies are as follows:

   a. Proper selection of materials to meet anticipated electrical and mechanical requirements and environmental conditions.

   b. Proper selection of part mounting requirements and solder joint design.

   c. Selection of printed wiring board conductor line widths, spacings, and other critical dimensional characteristics to provide adequate electrical performance and compensation for manufacturing tolerances.

   d. Proper sizing of holes to fit part lead sizes and/or feedthrough requirements.

   e. Proper sizing of termination areas (lands) and provisions for adequate annular rings.

   f. Optimum utilization of available space.

   g. Accurate artwork and complete detail drawings.

NOTE
Additional information and supplementary data are contained in Appendix B and should be considered in finalizing the design of reliable printed wiring board assemblies.

3K103 GENERAL

When related requirements or changes in requirements are specified, NASA quality assurance personnel will assure that the Government agency delegated at the supplier's site has received full instructions so that the work will be accomplished to the actual contract requirements.

3K104 RELATED DOCUMENTS

1. **Applicable Specifications.** Copies of the following specifications, when required in connection with a specific procurement, may be obtained from the procuring NASA installation or as directed by the contracting officer:

   Federal Specifications:

      QQ-N-290, "Nickel Plating (Electrodeposited)."

      QQ-S-571, "Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy."

Military Specifications:

MIL-P-13949, "Plastic Sheet, Laminated, Copper-Clad (For Printed Wiring)."

MIL-C-14550, "Copper Plating (Electrodeposited)."

MIL-I-43553, "Ink Marking, Epoxy Base."

MIL-G-45204, "Gold Plating, Electrodeposited."

MIL-P-81728, "Plating, Tin-Lead, Electrodeposited."

2. **Other Publications**

ANSI/IPC-SM-840 1/, "Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Circuit Boards."

NHB 5300.4 (3I), "Requirements for Printed Wiring Boards."

NHB 5300.4 (3J), "Requirements for Conformal Coating and Staking of Printed Wiring Boards and Electronic Assemblies."

1/ Application for copies should be addressed to IPC, 3451 Church St., Evanston, Il 60203.

3K105 DEVIATION AND WAIVER REQUESTS

1. **Approval of Changes.** This publication requires that:

   a. Written approval shall be obtained from the cognizant NASA Contracting Officer or designated NASA Representative for technical changes, deviations, or waivers initiated by the supplier.

   b. All deviation and waiver requests shall be supported by objective evidence and data substantiating that performance, reliability, and/or quality will not be compromised.

2. **Responsibility**. The prime contractor is responsible for assuring that any departures from this publication are evaluated, coordinated with, and submitted to the procuring NASA installation for approval prior to use or implementation.

3K106 DEFINITIONS

For the purposes of this publication, the definitions in Appendix A shall apply.

CHAPTER 2: DOCUMENTATION REQUIREMENTS

3K200 GENERAL

The information that is provided to the printed wiring board design organization as input normally consists of a schematic diagram and/or a logic diagram, a parts list, and the end product requirements. The minimum documentation output required from the design organization to produce a printed wiring assembly shall be a master drawing, a set of artwork, an assembly drawing, and a parts list.

3K201 MASTER DRAWING

The master drawing shall contain all the information necessary to produce the printed wiring board. It shall establish the type, size, and shape of the printed wiring board, the size and location of all holes therein, location of traceability markings, quality conformance test circuitry, material requirements and minimum dielectric separation between layers (when applicable). All appropriate detail board requirements shall be defined on the master drawing. Specific requirements to be identified on the master drawing are:

1. **Outline Dimensions.** The printed-wiring board outline shall be dimensioned and toleranced on the master drawing. Outline tolerances should be no tighter than ± .010 inch (.25 mm). For multilayers, the thickness tolerance should be ± 10 percent or ± .007 inch (.18 mm), whichever is larger. If tighter tolerances are required, lower producibility and increased costs can be expected.

2. **Special Features.** Location, dimensions, and tolerances for all special features shall be specified. Tolerances should be realistic, and no smaller than design requirements necessitate.

3. **General Notes.** The drawing notes shall include, but not be limited to the following information, as appropriate:

   a. Fabricate to the requirements of NHB 5300.4(3I) or other approved specification.

   b. Material callout. For Type 3 boards, the prepreg generally should be the same type as the laminate material (see 3K402).

   c. Etchback requirements for Type 3 boards (when required). A .0005 inch (.013 mm) etchback is preferred; limits are .0002 inch (.005 mm) minimum to .003 inch (.076 mm) maximum.

d. Dielectric separation (after curing) between layers shall be specified when electrically critical. The minimum separation shall be .0035 inch (.089 mm) after cure for voltages under 100 volts and .005 inch (.13 mm) for 100 volts or greater. When prepreg provides the separation, two or more sheets must be used.

e. Any special materials to be specified for board construction, insulation, plating, etc., with their controlling specifications.

f. Apply solder mask to the requirements of NHB 5300.4(3I) or other approved specification. Specify type of solder mask.

3K202 ARTWORK

The artwork shall be an accurate depiction of all details necessary to produce the printed wiring board. It shall establish size, shape, and location of all holes, lands, and conductors; board identification; reduction dimensions; and tooling hole targets. Nonsymmetrical registration marks and test circuitry shall be depicted as appropriate. When required, separate artwork shall be provided for solder mask application and for silk screening part designations and location information.

1. **Location Dimensioning.** All holes, test points, lands, and overall completed board dimensions shall be dimensioned by use of a modular grid system, except where necessary to mate parts not on grid (such as some connectors and some transistors). The basic modular units of length shall be .100, .050, .025 inch, or other multiples of .005 inch in that order of preference and shall be applied in the X and Y axes of the Cartesian coordinates. Critical pattern features which may affect circuit performance shall also be dimensioned.

2. **External Artwork Features**

   a. To assure reduction to proper master pattern size, a horizontal or vertical dimension and tolerance (preferably the longest) is placed between target marks outside the circuitry with the words "reduce to" establishing the final dimension to which the artwork is to be reduced. If artwork is generated on a 1:1 scale by an automatic method, the words "reduce to" are not used.

   b. When appropriate, nonsymmetrical registration marks shall be located on each layer to aid in registering the artwork.

   c. Tooling hole locations on each layer shall be designated by tooling hole targets.

d. Identification markings consisting of the part number and layer number (if appropriate) shall be shown on each layer. Artwork conductor layers shall be numbered consecutively starting with the part side as layer 1.

e. Quality conformance test circuitry artwork shall have identification markings corresponding to the associated printed wiring boards.

3. **Artwork Construction.** The accuracy of feature location on the finished printed wiring board is controlled by the accuracy of the original artwork, hence great care is required in artwork development to meet these accuracy requirements. Following are the four principal methods for creating artwork:

   a. Hand layout - tape. The artwork is created by laying pressure sensitive pads and tape in accordance with the printed wiring layout on a Mylar® base at an expanded scale, usually 4:1. The scale used will be determined by the accuracy required on the end product.

      Photographic reduction of the tape master to the final 1:1 artwork size should be done as quickly as possible to minimize registration errors because of tape slippage.

   b. Hand layout - Rubylith.® This material consists of two plies of Mylar®, one clear and the other red or ruby. Circuit lands and conductors are formed by cutting through the ruby layer with special tools and stripping away the excess material. The same essential steps are followed as in the case of tape layouts, except that immediate photographic reproduction of the 4:1 masters is not as critical, since the material is much more stable dimensionally than the taped up masters.

   c. Computer aided design (CAD) system or digitizing and photoplotting. Digitizing equipment is used to generate coordinate locations for all features, such as holes, lands, and conductors in a form suitable to drive a photoplotter for direct creation of the 1:1 artwork.

   d. Computer generated layout and artwork. Artwork is designed and layout made from computer program.

3K203 ASSEMBLY DRAWING

All assembly requirements, allowances, and necessary manufacturing data shall be documented and defined on the printed wiring assembly drawing or subassembly drawing which shall include as a minimum, the following information:

1. Part installation requirements and applicable specifications.
2. Any special requirements for control of cleanliness, static discharge protection, torque values, etc.
3. Type of conformal coating and masking, thickness requirements, and applicable specifications and procedures.
4. Location and identification of all parts.
5. Part orientation and polarity.
6. Structural details when required for support and rigidity, including the use of transistor mounting pads, clamps, supports, and heat sinks.
7. Lead termination configuration requirements, e.g., clinched, lapped, and stud.
8. Staking materials, location, and applicable specifications and procedures.
9. Sleeving materials, location, and applicable specifications.
10. Assembly envelope dimensions, including maximum part height, if critical.
11. Marking requirements, location, type and color of marking materials, and applicable specifications and procedures.
12. Wiring interconnection requirements to other assemblies. Connector keying requirements where applicable.
13. Any special process and technique requirements other than those previously listed.
14. Soldering requirements and applicable specification, e.g., NHB 5300.4 (3A-1).
15. Terminal installation requirements, including type, location, orientation, method of attachment, and applicable specifications and procedures.

3K204 PARTS LIST

The parts list shall include all parts (electronic, connectors, etc.) and all other items required to complete the printed wiring assembly and shall include reference designators for proper identification. It shall identify part numbers, values, tolerances, wattage/voltage ratings, the required reliability levels, and specifications or source control drawing numbers. Parts that require special handling because of electrostatic sensitivity shall be identified on the parts list.

CHAPTER 3: GENERAL DESIGN REQUIREMENTS

3K300 GENERAL

The total design package shall take into consideration not only the printed wiring board itself, but the entire printed wiring assembly. In addition to the basic elements of design outlined in this handbook, it shall include, where possible, consideration of such factors as cleanliness, inspectability, maintainability, and serviceability.

Materials used in low-pressure or vacuum compartments shall have low emittance of condensibles and noxious or toxic gases. Materials used shall be approved by the procuring NASA installation.

3K301 PRINTED WIRING LAYOUT

The printed wiring layout is a drawing which serves as a design aid and should contain all the information needed for part placement and interconnection routing. Typically, it is a hand layout on a gridded background. Part outlines are placed into position to scale using specification dimensions, and interconnections are added from the schematic.

3K302 DESIGN LAYOUT GRID SYSTEM

The locations of pattern features are normally based on a modular grid system whose units of length are .100, .050 and .025 inch or other multiples of .005 inch in that order of preference. For automatic plotting systems, a tape or disc is created with all features located by grid intersection for subsequent direct photoplotting of the 1:1 artwork. The location of features is established with respect to the X and Y axes of the Cartesian coordinate system. Unless otherwise specified, the layout should be dimensioned so that the resulting hole pattern on the printed wiring board has all centers located within a .010 inch (.25 mm) diameter of true position indicated by the grid location or dimensioned location.

The board layout should be positioned from the X and Y coordinate scales at the lower left hand corner of the grid so that all dimensional values are positive.

3K303 PRINTED WIRING BOARD CONFIGURATION

For ease of board fabrication, processing, and handling, boards should be rectangular in shape. Curved outside edges should be avoided and inside corners should have a minimum radius of .062 inch (1.57 mm). Whenever possible, board shape and size should be standardized for compatibility with techniques such as multiple pattern processing, and numerically controlled drilling and routing. Table 3-1 shows the maximum unsupported board width suggested to prevent warpage when using wave soldering, based on board thickness. A limitation on the use of wave soldering may occur if board design requirements dictate width and thickness relationships beyond those shown in the table.

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TABLE 3-1
MAXIMUM RECOMMENDED UNSUPPORTED
BOARD WIDTH FOR WAVE SOLDERING

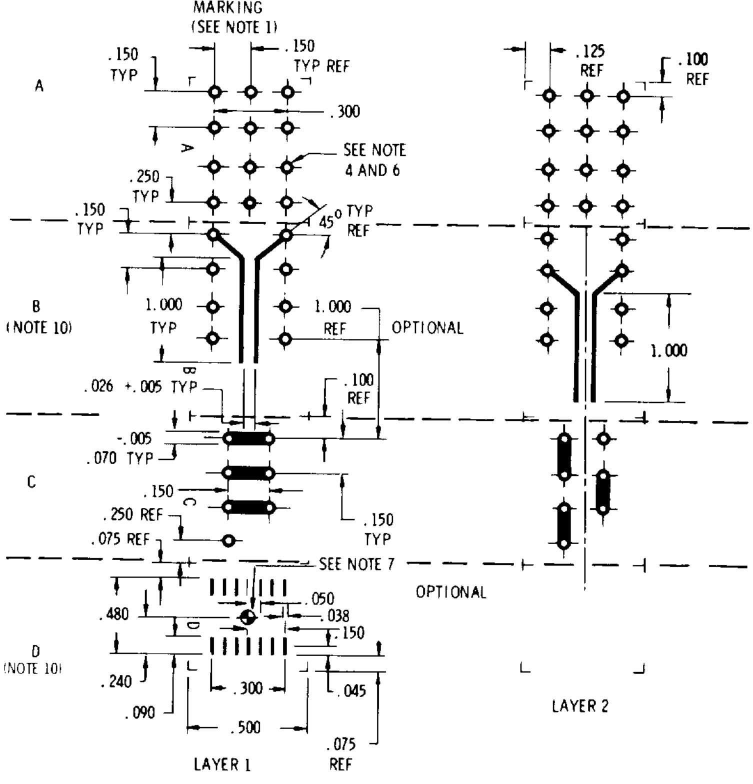
Thickness Inch (mm)	Maximum Unsupported Width Inches (mm)
.031 (.79)	4.0 (101.6)
.047 (1.19)	7.0 (177.8)
.062 (1.57)	10.0 (254.0)
.093 (2.36)	11.0 (279.4)

3K304 QUALITY CONFORMANCE TEST CIRCUITRY

1. To assist in the determination of the quality and reliability of boards, test patterns are placed on each fabricated working panel. The pattern shown in Figure 3-1 is for Type 1 and Type 2 boards, and its use is optional, but the pattern in Figure 3-2 is for Type 3 boards, and, as a minimum, test circuits A or F, B, and C shall be used. (NOTE: C is required only if solder mask is used.) The use of test circuits D, E, and G is optional; however, they are useful for special or referee testing. The lengths of test circuits D, E, and G are dependent upon the number of layers in the panel. For test circuits D and G, a pair of holes and a conductor between must be provided for each layer. Electrical connection is in series, stepwise, through each conductor layer of the board. For test circuit E, a pair of holes and conductors must be provided for the first layer and each internal layer.

2. Holes in land areas must be the diameter of the smallest plated-through hole in the associated board. For coupon F, the minimum land area dimension and shape must be that used on the associated board. The hole must be the largest used in this minimum size land area. If a Type 3 board contains internal copper planes, the test coupon shall contain internal copper planes on the appropriate layers of all segments except D, E, and G.

3. The test circuitry shall be placed on the artwork within .5 inch (12.7 mm) of the edge of the board.



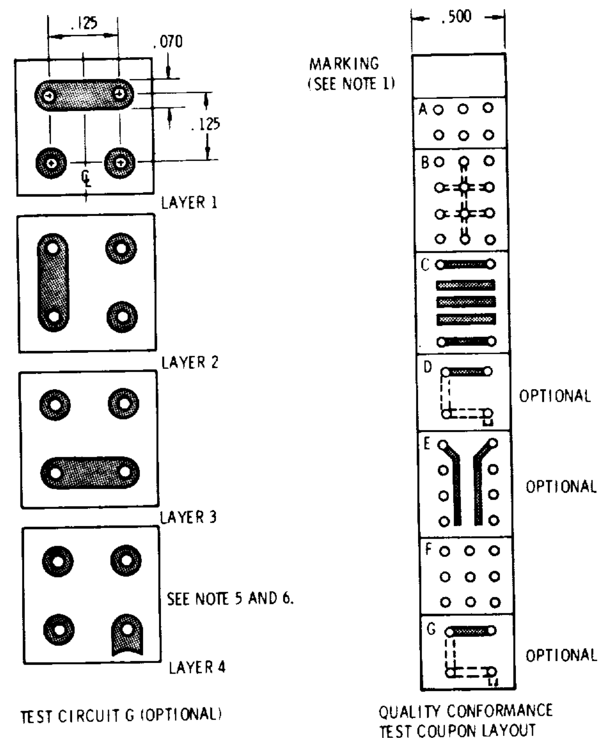
NOTES:

1. TEST COUPONS ARE TO BE IDENTIFIED WITH THE FOLLOWING DATA:
   A. FEDERAL SUPPLY CODE FOR MANUFACTURERS (FSCM)
   B. PART NUMBER AND REVISION LETTER
   C. BOARD TRACEABILITY OR LOT NUMBER

   CHARACTERS MUST BE LEGIBLE: STYLE, HEIGHT AND WIDTH ARE OPTIONAL
2. TEST COUPONS SHALL BE AN INTEGRAL PART OF ALL MASTER DRAWINGS AND FABRICATION ARTWORK.
3. THE ETCHED LETTERS ON THE COUPONS ARE FOR IDENTIFICATION PURPOSES ONLY.
4. ALL LANDS SHALL BE .070 INCH ± .005 DIAMETER. HOLES SHALL BE THE DIAMETER OF THE SMALLEST HOLE IN THE ASSOCIATED BOARD.
5. ALL CONDUCTORS SHALL BE .020 INCH ± .003 WIDE, UNLESS OTHERWISE SPECIFIED.
6. ALL HOLE TOLERANCES SHALL MEET THE REQUIREMENTS OF THE END PRODUCT BOARD.
7. THE NOTED TARGET ⊕ REPRESENTS THE THEORETICAL CENTERLINES OF THE COUPON.

   ALL TOLERANCES SHALL BE ± .001 ON THE FABRICATION ARTWORK.
8. DIMENSIONS ARE IN INCHES.
9. FOR CONVERSION TO CENTIMETER EQUIVALENTS, MULTIPLY BY 2.54.
10. COUPONS "B" AND "D" ARE NOT REQUIRED FOR QUALITY CONFORMANCE INSPECTION BUT MAY BE USED FOR ADDITIONAL TESTING IF REQUIRED.

FIGURE 3-1
QUALITY CONFORMANCE TEST COUPON FOR TYPE 1 AND TYPE 2 PRINTED WIRING BOARDS



TEST CIRCUIT G (OPTIONAL)

QUALITY CONFORMANCE TEST COUPON LAYOUT

NOTES:

1. TEST COUPONS ARE TO BE IDENTIFIED WITH THE FOLLOWING DATA:
   A. FEDERAL SUPPLY CODE FOR MANUFACTURERS (FSCM).
   B. PART NUMBER AND REVISION LETTER.
   C. BOARD TRACEABILITY OR LOT NUMBER.
2. ALL LINES SHALL BE .020 ± .003 WIDE, UNLESS OTHERWISE SPECIFIED.
3. UNLESS OTHERWISE SPECIFIED, THE TOLERANCES SHALL MEET THE REQUIREMENTS OF THIS SPECIFICATION.
4. THE MINIMUM LAND DIMENSION SHALL BE .070 ± .005 AND MAY REPRESENT THE PAD SHAPE USED ON THE ASSOCIATED BOARD. HOLES IN TERMINAL AREAS SHALL BE THE DIAMETER OF THE SMALLEST HOLE IN THE ASSOCIATED BOARD (SEE NOTE 7).
5. ALL FIRST LAYERS AND INTERNAL LAYERS SHALL BE AS SPECIFIED ON THE MASTER DRAWING. COPPER PLANE AREAS MAY BE USED ON ALL COUPONS ON APPROPRIATE PLANE LAYERS, EXCEPT FOR THE D, E, AND G SEGMENTS.
6. THE LENGTHS OF TEST CIRCUITS D, E, AND G, ARE DEPENDENT ON THE NUMBER OF LAYERS IN THE PANEL. FOR TEST CIRCUITS D AND G, A PAIR OF HOLES AND A CONDUCTOR BETWEEN SAME SHALL BE PROVIDED FOR EACH LAYER. ELECTRICAL CONNECTION SHALL BE IN SERIES, STEPWISE, THROUGH EACH CONDUCTOR LAYER OF THE BOARD. FOR TEST CIRCUIT E, A PAIR OF HOLES AND CONDUCTORS MUST BE PROVIDED FOR THE FIRST LAYER AND EACH INTERNAL LAYER.
7. FOR COUPON F, THE MINIMUM LAND DIMENSION AND SHAPE SHALL BE THAT USED ON THE ASSOCIATED BOARD. THE HOLE SHALL BE THE MAXIMUM USED IN THE SMALLEST LAND USED FOR LEAD INSERTION.
8. THE QUALITY CONFORMANCE TEST CIRCUITRY MAY BE SEGMENTED, HOWEVER TEST CIRCUITRY A, B, AND F MUST BE JOINED TOGETHER. TEST CIRCUITRY C, D, G, AND E MAY BE ARRANGED TO OPTIMIZE BOARD LAYOUT. ALL TEST COUPONS ILLUSTRATED MUST APPEAR ON EACH PANEL. THE NUMBER OF LAYERS MUST BE IDENTICAL TO THE NUMBER OF LAYERS IN THE BOARDS DERIVED FROM THE PANELS.
9. ETCHED LETTERS ON COUPONS ARE FOR IDENTIFICATION PURPOSES ONLY.
10. NUMBER OF LAYERS SHOWN IN THESE TEST COUPONS ARE FOR ILLUSTRATION PURPOSES ONLY. CONDUCTOR LAYER NUMBER 1 SHALL BE THE LAYER ON THE COMPONENT SIDE, AND ALL OTHER CONDUCTOR LAYERS SHALL BE COUNTED CONSECUTIVELY DOWNWARD THROUGH THE LAMINATED BOARD TO THE BOTTOM CONDUCTOR LAYER WHICH IS THE SOLDER SIDE.
11. DIMENSIONS ARE IN INCHES.
12. FOR CONVERSION TO CENTIMETER EQUIVALENTS, MULTIPLY BY 2.54
13. COUPONS "D", "E", AND "G" ARE NOT REQUIRED FOR QUALITY CONFORMANCE INSPECTION, BUT MAY BE USED FOR ADDITIONAL TESTING IF REQUIRED.

FIGURE 3-2
QUALITY CONFORMANCE TEST COUPON TYPE 3

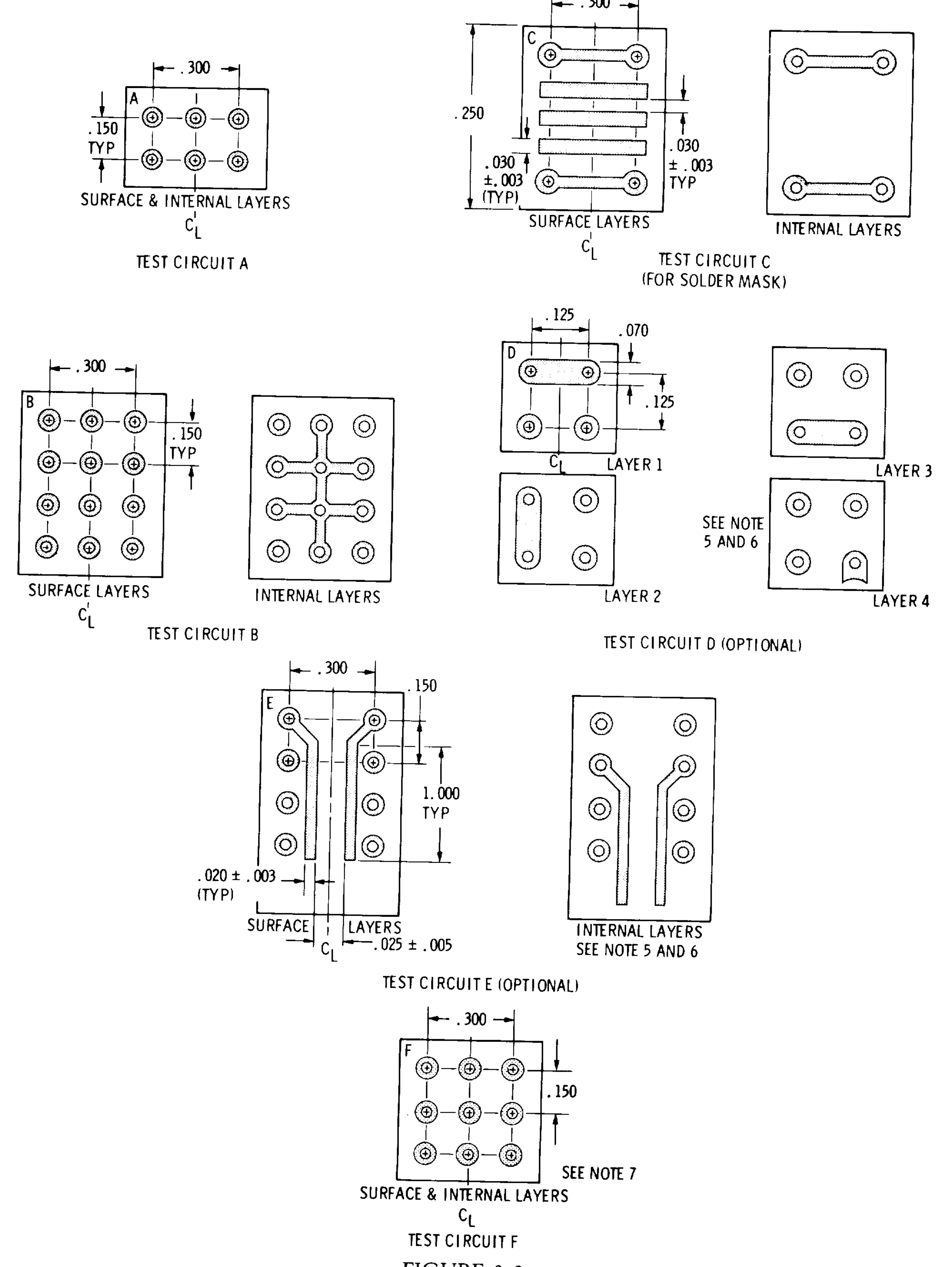


FIGURE 3-2
QUALITY CONFORMANCE TEST COUPON TYPE 3 (CONTINUED)

3K305 APPLICATION OF SOLDER MASK

1. When solder mask is to be applied to the printed wiring board, the conductor areas under the solder mask shall be bare copper or oxide treated copper. All exposed conductor areas (lands, plated-through holes, etc.) shall be coated with solder or fused tin-lead.

2. The size of the openings in the solder mask is determined by the solder mask artwork. The location tolerances of the openings are as follows:

   a. For part mounting lands, the openings in the solder mask shall be located so that the entire land area is free from solder mask and a minimum of the adjacent circuitry is exposed.

   b. For all other openings in the solder mask, the location shall be within .020 inch (.50 mm) of that depicted on the artwork.

3. Marking inks typically used on printed wiring boards can be used on solder mask. However, compatibility of the ink with the solder mask shall be verified prior to its use.

   The use of solder mask on printed wiring boards does not eliminate the need for conformal coating on printed wiring assemblies.

3K306 APPLICATION OF STAKING MATERIALS

1. Staking materials shall be applied to printed wiring assemblies when required to protect and support components which may be damaged by shock, vibration, or handling. Staking is mandatory on axial lead solid slug tantalum capacitors.

2. Staking material shall be noncorrosive, electrically insulative material that is strong enough to provide adequate mechanical support while imposing minimal thermomechanical stress on parts or solder joints. The material shall not be applied to the adjustable portion of adjustable parts or to electrical or mechanical mating surfaces. Wherever practical, the designer should specify the use of a staking material with a contrasting color to that of the conformal coating and/or solder mask material. This will provide visual assurance that the staking materials have been applied and applied only in those areas desired. Staking material shall also be compatible with and must adhere to the board or substrate and part staked and to the conformal coating to be applied after staking.

3K307 APPLICATION OF CONFORMAL COATING

1. All printed wiring assemblies shall be conformally coated unless compelling design reasons dictate otherwise and concurrence has been given in writing by the NASA procuring installation.

2. The coating shall not be applied to the adjustable portion of adjustable parts or to electrical and mechanical mating surfaces.

3. Printed wiring assemblies shall be constructed and adequately masked or otherwise protected in such a manner that application of conformal coating does not degrade the thermal or electrical performance of the assembly.

CHAPTER 4: MATERIAL REQUIREMENTS

3K400 BOARD MATERIAL

1. Boards designed to this standard will require either epoxy-glass (type GE, GF, or GH) or polyimide-glass (type GI) material. The use of Teflon® -glass (types GP, GR, GT, or GX) is generally limited to stripline or microstrip boards. Table 4-1 includes a list of applicable specifications for the materials and their prepregs.

   Because of material cost, polyimide-glass boards are more expensive to manufacture than epoxy-glass; however, they provide an advantage in improved resistance at elevated temperatures to land lifting, measling, delamination, plated-through hole cracking, and laminate voids in multilayer boards. Because of the brittle nature of the material, they are more susceptible to edge chipping and cracking.

TABLE 4-1
APPLICABLE MATERIAL SPECIFICATIONS FOR PWB FABRICATION

Material	Military/Federal Specification	Type
Copper-clad dielectric:		
Polyimide fiberglass	MIL-13949/10	GI
Epoxy fiberglass	MIL-P-13949/3	GE
Epoxy fiberglass (flame-retardant)	MIL-P-13949/4	GF
Epoxy fiberglass (heat-resistant)	MIL-P-13949/5	GH
Teflon® glass	MIL-P-13949/6-9	GP, GR, GT, GX
Prepreg:		
Polyimide	MIL-P-13949/13	GI
Epoxy	MIL-P-13949/11	GE
Epoxy (flame-retardant)	MIL-P-13949/12	GF
Electrodeposited metal:		
Copper	MIL-C-14550	
Tin-lead	MIL-P-81728	
Nickel	QQ-N-290	
Gold	MIL-G-45204	
Solder coating	QQ-S-571	
Permanent solder mask	IPC-SM-840	Class 3
Marking ink	MIL-I-43553	

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2. In their final printed wiring board form, all materials except type GE are considered flame resistant and self-extinguishing.

3K401 MATERIAL CALLOUTS — CLAD LAMINATES

Clad laminate material shall be specified in accordance with the requirements of MIL-P-13949.

3K402 MATERIAL CALLOUTS — PREPREG

Inner layer bonding material or prepreg shall be specified in accordance with the requirements of MIL-P-13949 and generally should be the same type (GE, GF, GI, etc.) as the base laminate. GI prepreg shall not be used with GF or GE laminate. A typical callout should be as follows:

Type PC GF XXXX XX XXX XX

The elements of this callout have the following meanings:

PC - Designates prepreg material

GF - Signifies flame retardant, glass epoxy.

"X's" indicate callouts for glass style, resin flow, gel time, and resin content, which are material manufacturer's variables, normally selected by the board fabricator in a combination which will optimize the manufacturing process.

3K403 MULTILAYER BOARD THICKNESS

When specifying thickness requirements, the preferred method is to specify overall thickness including plating. Do not specify inner laminate core thickness or spacing between layers created by prepreg (except to establish a minimum), unless required for critical electrical reasons. In this case, some relaxation of overall thickness tolerances may be required.

3K404 PLATING

Printed wiring boards designed to this specification and fabricated to the requirements of NHB 5300.4(3I) require all external conductive patterns (plated-through holes, lands, conductors, etc.) to be solder coated or tin-lead plated and fused unless a permanent solder mask coating is used (see 3K406) or other plating is required because of the circuit design requirements (e.g., edge card connector pads). Plating shall be in accordance with the following:

1. **Electroless copper plating.** An electroless copper deposition system shall be used as a preliminary process for providing the conductive layer over nonconductive material for subsequent electrodeposition of plated-through holes. The thickness of this electroless copper layer shall be sufficient for subsequent electrodeposition.

2. **Electrolytic copper plating.** All electrolytic copper shall be in accordance with MIL-C-14550 and shall have a minimum purity of 99.5 percent. The minimum thickness shall be .001 inch (.025 mm) at the thinnest point. The type of copper may be specified by the NASA procuring installation.

3. **Tin-lead plating.** Tin-lead plating shall be in accordance with MIL-P-81728. Fusing shall be performed on all tin-lead plated surfaces. The fused tin-lead shall be .0003-inch (.008 mm) thick minimum when measured at the crest of the conductor. A minimum plating of .0001 inch (.002 mm) in the hole is required.

4. **Gold plate:** All electrolytically deposited gold plating shall be in accordance with MIL-G-45204. The minimum thickness shall be .000050 inch (.0013 mm). The use of gold plate requires underplating of electrolytically deposited nickel conforming to QQ-N-290, Class 2, with a minimum thickness of .000200 inch (.005 mm) between gold and copper. The type and class of all plating shall be specified on the master drawing.

3K405 SOLDER COATING

Solder coating shall be in accordance with composition SN60 or SN63 of QQ-S-571. The solder coating shall be .0003-inch (.008-mm) thick minimum when measured on the surface at the crest of the conductor. A coating of .0001 inch (.002 mm) minimum in the hole is required.

3K406 SOLDER MASK

Solder mask is a polymer coating which can be selectively applied to all types of printed wiring boards for the primary purpose of masking the board to limit the areas on which solder may be applied. Secondary uses may include any or all of the following:

- Physical protection.
- A moisture inhibitor.
- Improvement of insulation resistance.
- An insulator.
- A thermal barrier during wave soldering.

When properly cured, the material becomes a permanent part of the printed wiring board and must meet the requirements of IPC-SM-840, Class 3. Materials which qualify to this specification are classified as follows:

- Type A - Liquid film - Typically a screenable epoxy mask.
- Type B - Dry film - A photosensitive dry film polymeric mask.

3K407 STAKING

Staking materials shall be specified on the assembly drawing in accordance with requirements of NHB 5300.4 (3J).

3K408 CONFORMAL COATING

1. Conformal coating materials shall be specified on the assembly drawing in accordance with the requirements of NHB 5300.4 (3J).

2. The thickness of the conformal coating shall be specified on the assembly drawing as follows for the type identified, when measured on a flat, unencumbered surface:

   a. Types urethane (UR), epoxy (ER), and acrylic (AR):
   .001 to .004 inch (.025 to .10 mm).

   b. Type silicone (SR): .002 to .008 inch (.05 to .20 mm).

   c. Type Parylene® (XY): .0005 to .002 inch (.013 to .05 mm).

CHAPTER 5: PART MOUNTING REQUIREMENTS

3K500 STRESS RELIEF

1. Stress relief is the best design approach to prevent solder joint cracking or part damage in printed wiring board assemblies. Stress relief shall be provided between the part and the part termination. Stress relief is the freedom of the part lead to move between constraints to prevent detrimental forces from building up in the printed wiring board assembly during thermal and mechanical excursions. Examples of constraint points and stress relief in parts mounting are illustrated in Figure 5-1.

2. Whenever the part mounting configuration does not allow for stress relief, the solder connections shall be reinforced by a plated-through hole and additional external solder. Plated-through holes will provide joint reinforcement by increasing the solder shear area in the termination; however, this increase is insignificant in boards .032 inch (.81 mm) thick or less. Typical mounting configurations are shown in Figure 5-2.

3K501 PART PLACEMENT

Unless otherwise required by design, parts should be mutually parallel or perpendicular to each other and in contact with the mounting surface. The body of the part should be approximately centered between its terminations.

3K502 MINIMUM HOLE SPACING FOR AXIAL LEADED PARTS

The minimum hole spacing for axial leaded parts is given by the following formula (see Figure 5-3);

$$E_{min} = L + 5d + (.060 \text{ inch } (1.52 \text{ mm}) \text{ or } 4d, \text{ whichever is smaller})$$

where:

E min = minimum hole spacing.

L = maximum body length including body extensions such as lead fillets from body (both sides), cathode extension, or the weld bead (both sides).

d = nominal lead diameter.

150-369 O - 86 - 2 QL.3

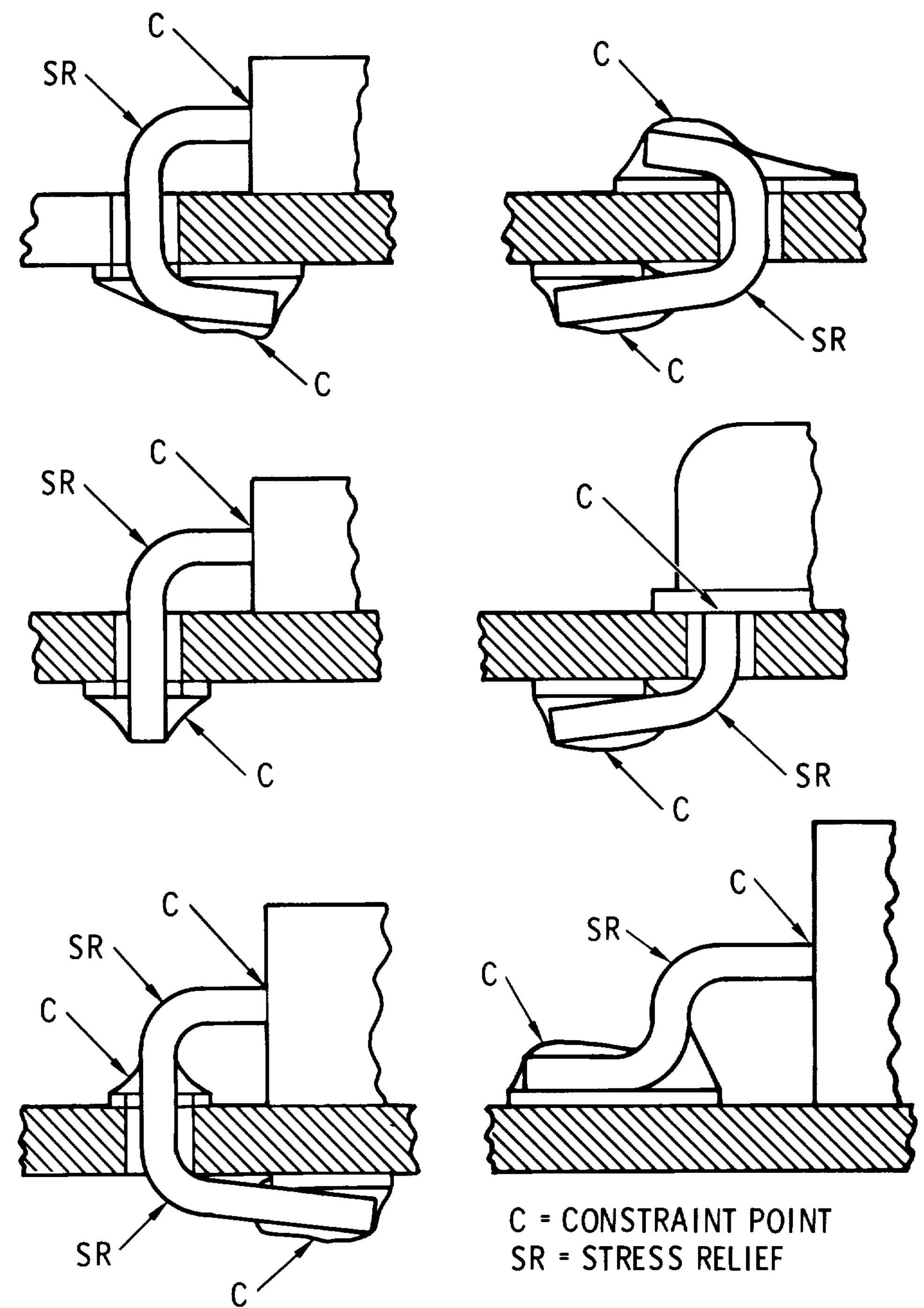


FIGURE 5-1
STRESS RELIEF AND CONSTRAINTS

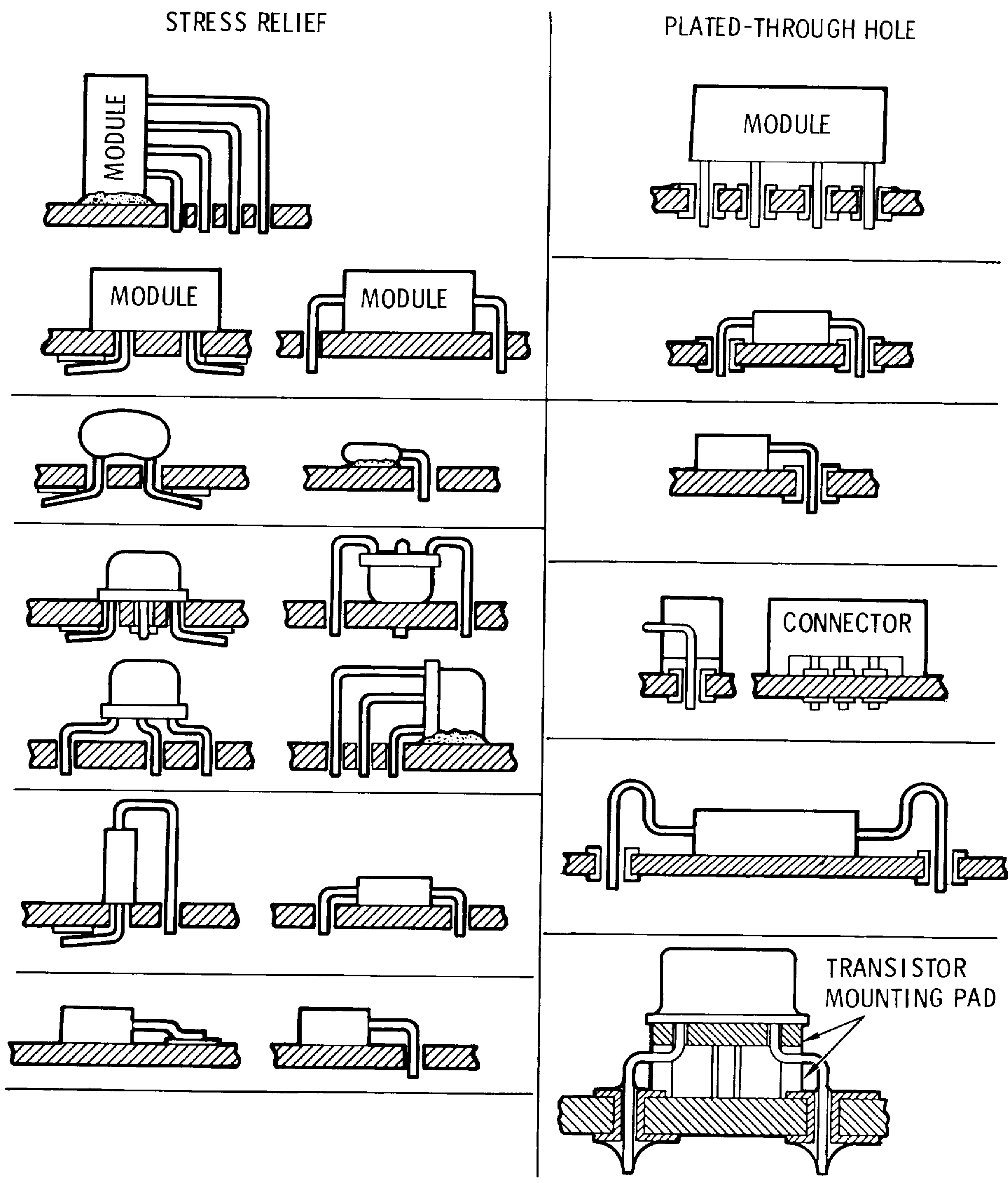


FIGURE 5-2
MOUNTING CONFIGURATIONS

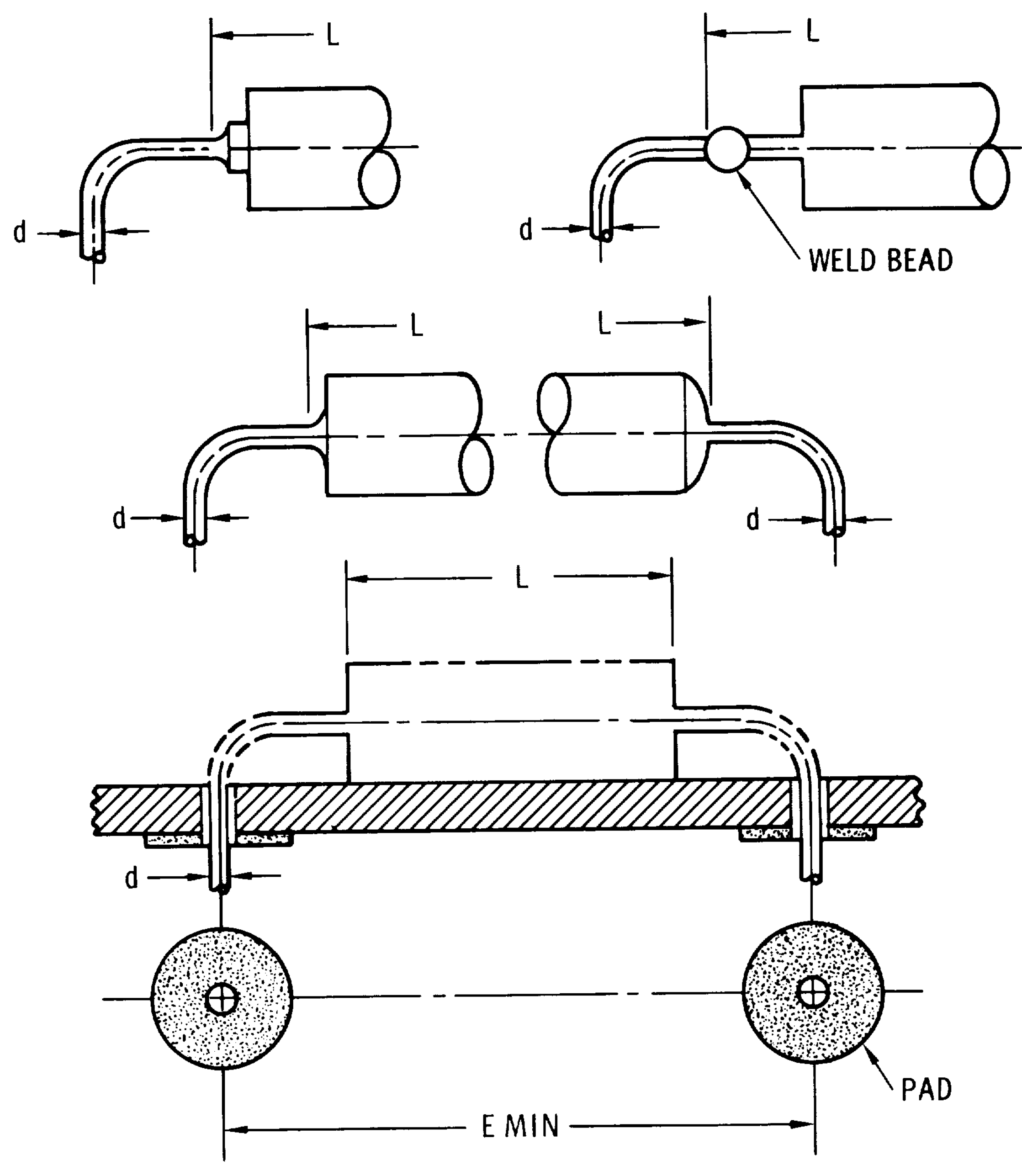


FIGURE 5-3
MINIMUM HOLE SPACING FOR AXIAL LEADED PARTS

3K503 LAYOUT FOR SURFACE MOUNTED PARTS

1. **Land Spacing for Parts with Round Leads.** The land spacings shall be established using Figure 5-4A. See Figure 5-7B for determining land size.

2. **Land Spacing for Parts with Ribbon Leads.** The minimum land spacings shall be established using Figure 5-4B. See Figure 5-8B for determining land size.

In general, land spacing should be kept as near the minimum as other design considerations permit, since excessive lead length can aggravate stress on the solder joints caused by vibration.

3K504 VERTICALLY MOUNTED AXIAL LEADED PARTS

When absolutely necessary, axial leaded parts may be mounted perpendicularly to the board (vertical, hairpin mounting) (see Figure 5-5). To relieve stress on the solder joints, the end of the part body must be mounted with at least .020 inch (.51 mm) clearance above the board surface unless stress relief is provided by off-pad lap-joint mounting methods. The end of the part is defined to include any extension such as coating meniscus, solder seal, or solder or weld bead.

3K505 PART LOCATION REQUIREMENTS

The following requirements apply:

1. A separate hole shall be provided for each part lead and wire terminated in a land.

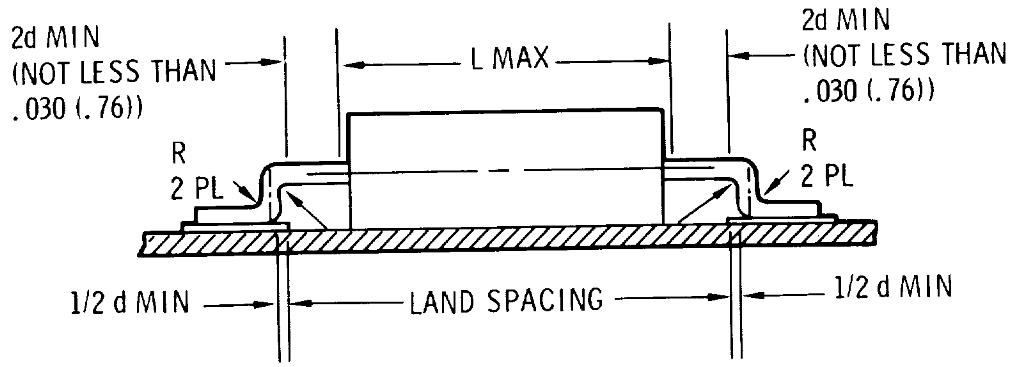
2. The location of all parts shall permit access to the termination of all other parts, part leads, and wires.

3. Parts shall be located so that any part can be removed from the board without removing any other part, except for stacked parts.

4. A part shall not extend beyond the perimeter of the board.

5. Parts shall be located such that adequate cleaning and removal of residual soldering fluxes can be accomplished and verified.

6. Parts shall be located such that adequate visual inspection of the finished solder joints can be accomplished.



L MAX = MAXIMUM BODY LENGTH (INCLUDING EXTENSIONS SUCH AS LEAD FILLETS (BOTH SIDES), CATHODE EXTENSIONS, OR WELD BEADS (BOTH ENDS)

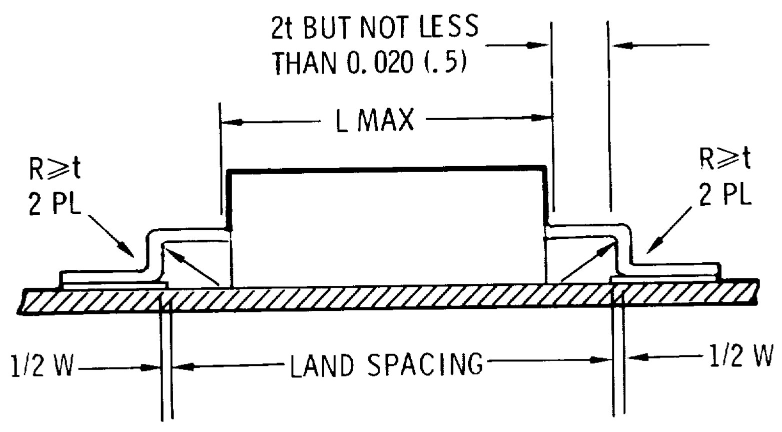
d = NOMINAL LEAD DIAMETER

R = d FOR LEADS UP TO 0.027 (.68) DIAMETER

= 1.5d FOR LEADS FROM 0.028 TO 0.047 (.71 TO 1.19) DIAMETER

= 2d FOR LEADS OF 0.048 (1.19) DIAMETER AND LARGER

A. ROUND LEADS



L MAX = MAXIMUM BODY LENGTH OR WIDTH INCLUDING EXTENSIONS SUCH AS LEAD FILLETS (BOTH SIDES) AND GLASS SEALS

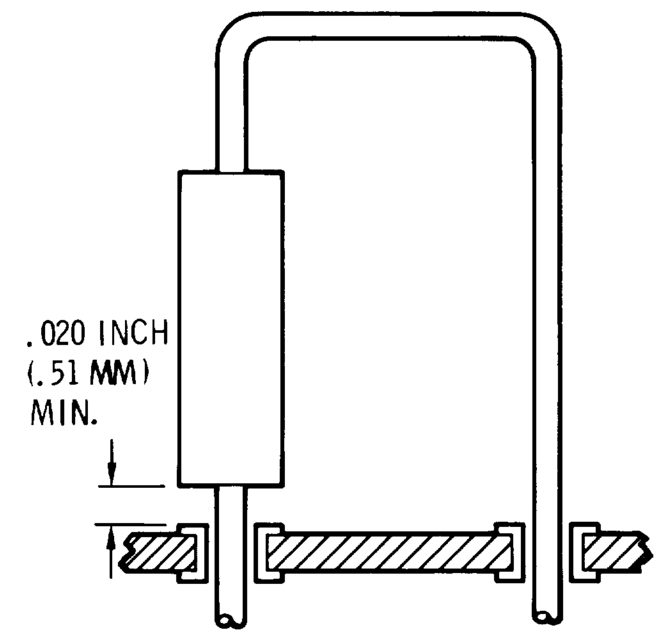
W = NOMINAL LEAD WIDTH

t = NOMINAL LEAD THICKNESS

B. RIBBON LEADS

DIMENSIONS IN INCHES (MILLIMETERS)

FIGURE 5-4
LAND SPACING FOR SURFACE MOUNTED PARTS



A. PLATED-THROUGH HOLE

B. NONPLATED-THROUGH HOLE

FIGURE 5-5
VERTICAL PART MOUNTING

3K506 PART MOUNTING REQUIREMENTS

The following requirements must be observed:

1. Metal cased parts mounted over printed conductors (including ground planes, voltage planes, and heat sinks), or which are in close proximity to other conductive materials, shall be separated by insulation of suitable thickness. Insulation shall be such that part identification markings remain visible and legible.

2. High heat dissipating parts shall be thermally shunted as required.

3. When the weight of the part exceeds .5 ounce (14 grams), additional support shall be provided. Staking or mechanical means such as clamps, brackets, or flanges may be used. The method used shall not produce stresses which could cause functional degradation or damage to the part or assembly.

4. Unless stress relief is provided by off-pad lap-joint mounting methods, nonaxial leaded parts shall be mounted so that the surface from which the leads project (end of the part) will be a minimum of .020 inch (.51 mm) above the printed wiring board surface. Consideration shall be given to providing adequate support to prevent part, lead, or solder joint damage.

5. Multiple-leaded parts (parts with three or more leads), except those mounted to thermal planes or heat sinks, shall be mounted in such a manner that parts are spaced above the board to facilitate cleaning, provide electrical isolation, and prevent moisture traps. A clearance of .020 inch (.51 mm) minimum applies unless otherwise specified by design. Special spacers such as transistor mounting pads and other mounting supports that will provide stress relief areas for leads and adequate provisions to facilitate cleaning, electrical isolation, and inspectability are desirable and sometimes indicated. Design requirements for staking these special spacers (devices) to component bodies and to printed wiring boards should be considered and may be required for vibration protection.

6. Dual in-line packages (DIPs) with through-hole mounting shall not be staked prior to soldering.

7. Axial leaded solid slug tantalum capacitors shall be staked or otherwise rigidly mounted to the board. When staking capacitors with a case size larger than "C," they shall be staked all around (length and ends).

8. Glass bodied parts shall be sleeved or coated with a buffer material when Type ER (epoxy resin) conformal coatings or staking materials are to be used. When sleeving is required, choose a thin, pliant material such as polyethylene terephthalate or polyvinylidene fluoride that is nonreactive with the conformal coating and staking materials and with all parts of the printed wiring assembly. When a buffer material is

needed, it shall be fungus- and flame-resistant, have a low outgassing after cure, and be clear or transparent so that the markings on the parts are visible.

> **NOTE**
>
> Board designers are cautioned that sleevings and buffer materials will increase part overall size: this should be considered when assigning space and location for mounting.

9. The use of part plug-in sockets for flight equipment is not recommended. If compelling design reasons require the use of sockets, the socket leads should be of the stress-relieved variety if used in nonplated-through holes. If sockets are used, the parts shall be held in sockets by some method other than part lead friction.

10. For TO-3 and TO-66 power transistors, the collector is tied internally to the case; sometimes this creates difficulty in making a reliable connection from an etched line or terminal on a board to the transistor case. Since solder tangs or eyelets are not provided on these configurations, the collector electrical connection must be made by mechanical pressure contact. The design of such a connection shall include the following considerations:

    a. The connection must remain free of contamination such as grease, oxidation, and dirt.

    b. The connection must be as direct as possible for low resistance applications and must be a reliable connection in all environments.

    c. Some form of pressure device is required to permit contact retention as the device case and the attaching hardware undergo different expansion/contraction rates over the specified temperature range.

    d. Contact pressure resulting from attaching hardware must be distributed, especially when soft materials such as printed wiring laminates or insulators of polyimide are used.

3K507 INTERFACIAL CONNECTIONS

1. **Plated-Through Holes.** The standard method for providing electrical interconnection from one side of a double-sided printed wiring board to the other side is a plated-through hole. Multilayer boards are always made with plated-through holes. Interfacial connections on double-sided boards that utilize plated-through holes require additional support. This shall be done with a wire soldered into the plated-through hole (see Figures 5-6B, F or J). For multilayer boards, holes may be kept bare or filled.

2. **Nonplated-Through Holes.** Interfacial connections in nonplated-through holes shall be made with a conductor soldered on both sides of the board. The solder joint on at least one side shall be a lapped termination as shown in Figure 5-8. Acceptable configurations are shown in Figures 5-6D, E, or G. Terminals, rivets, and eyelets shall not be used as interfacial connections.

3. **External Interconnection Methods.** Two-part connectors (plug and receptacle) are preferred for all external connections for plug-in assemblies.

   For non-plug-in assemblies, external electrical connections should be wired directly to the board or to terminals or attached with flex cables with suitable mechanical support and stress relief.

4. When plated-through holes in multilayer printed wiring boards are used for interfacial connections only, a note should be placed on the assembly drawings identifying and permitting these holes to be closed after fusing and/or wave soldering.

3K508 TERMINATIONS

All terminating surfaces shall be solder tinned prior to soldering. Solder joints shall be visible for inspection after soldering. Part leads shall be terminated to the printed wiring board by lapped, clinched, or stud terminations. Acceptable terminations are shown in Figure 5-6.

1. **Lapped Terminations.** Round lead lapped terminations shall be as shown in Figure 5-7. Ribbon lead lapped terminations shall be as shown in Figure 5-8.

2. **Clinched Terminations.** Clinched terminations shall be as shown in Figure 5-9. The lead shall be bent in the direction of the land. It shall be bent to make contact with the printed wiring board and be allowed to spring back.

3. **Stud Terminations.** Stud terminations with nonplated-through holes shall be as shown in Figure 5-10A. Stud terminations with plated-through holes shall be as shown in Figure 5-10B.

4. **Terminal Mounting.** When parts are mounted between bifurcated terminals without lead wrap, it is not mandatory that the part leads have stress relief bends. When parts are mounted between other terminal types, it is mandatory to put a stress relief bend in at least one lead.

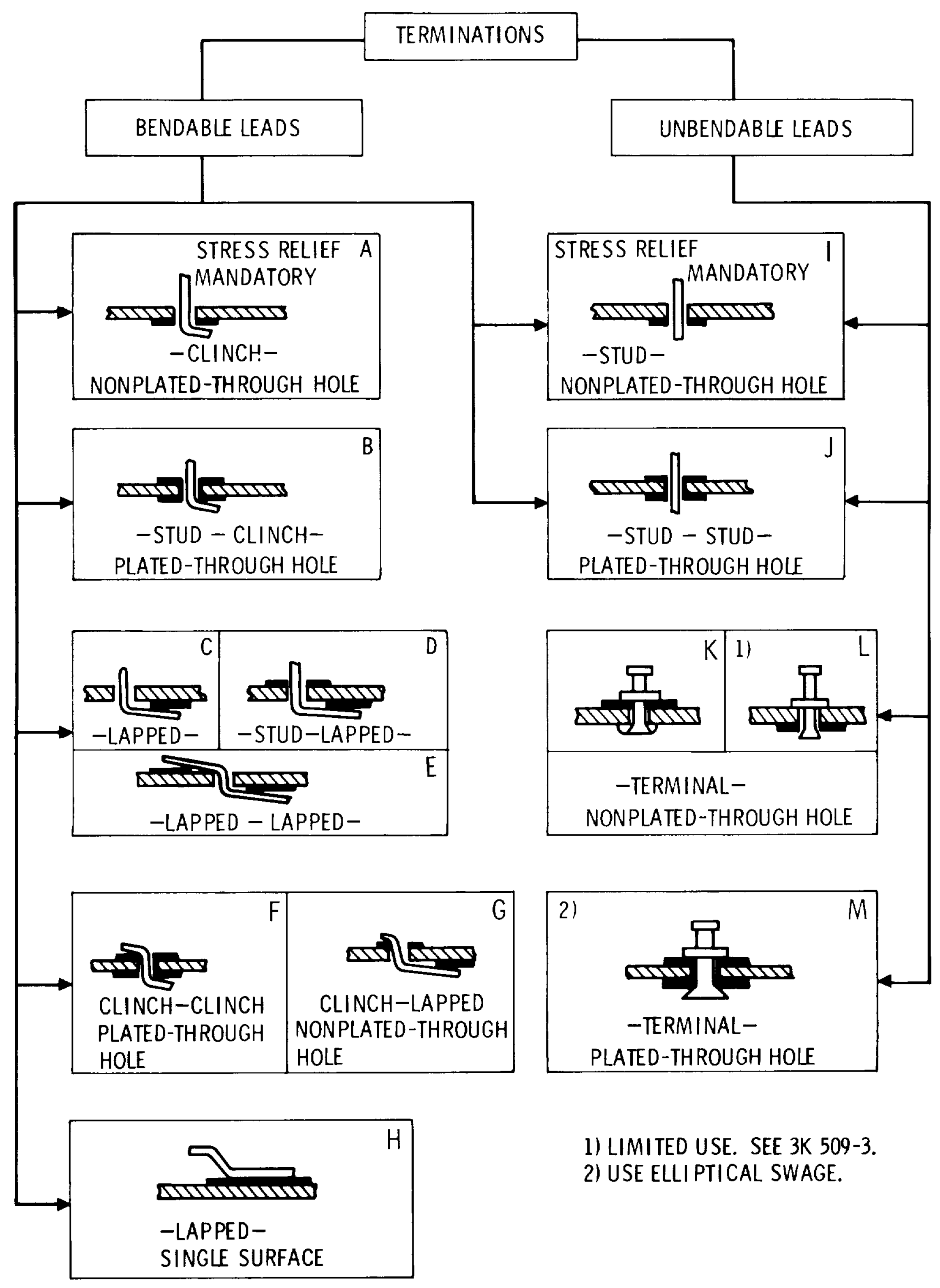
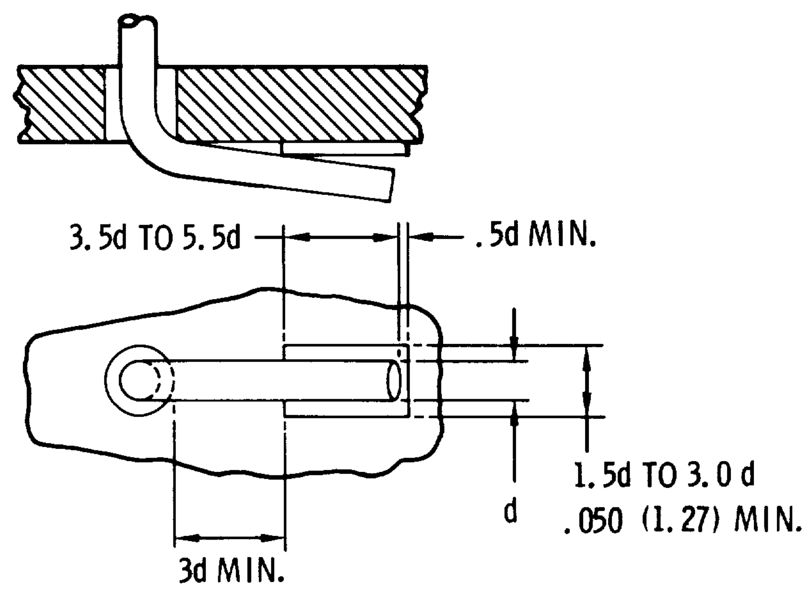
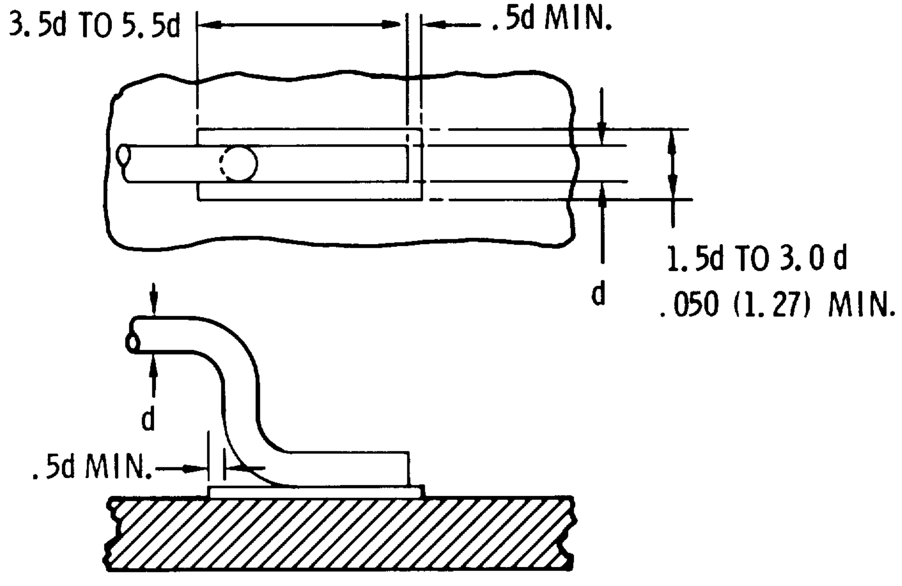


FIGURE 5-6
ACCEPTABLE TERMINATIONS FOR TYPE 1 AND TYPE 2 BOARDS



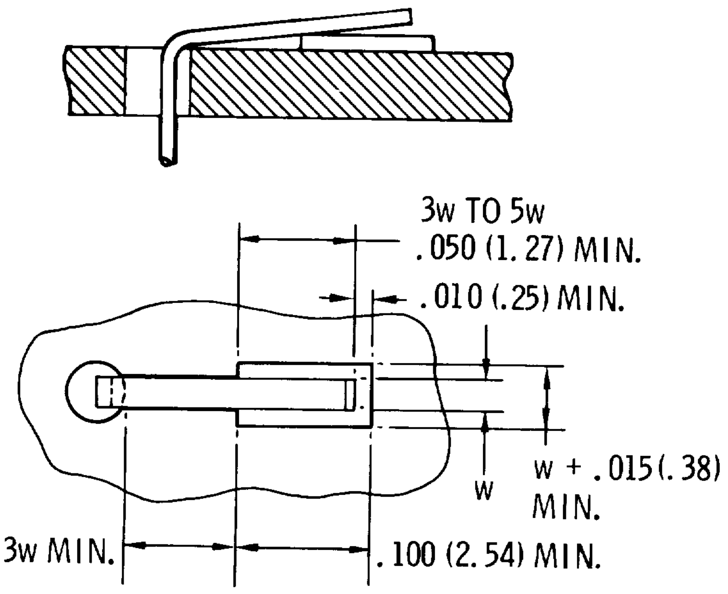
A. THROUGH-HOLE LAPPED TERMINATION



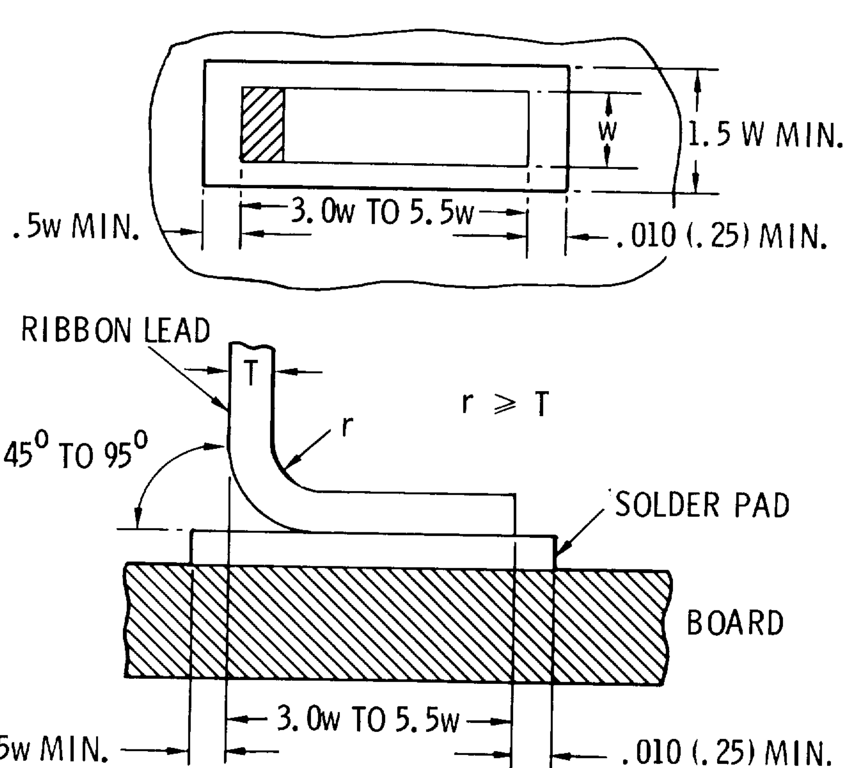
B. SINGLE SURFACE LAPPED TERMINATION

DIMENSIONS IN INCHES (MILLIMETERS)

FIGURE 5-7
ROUND LEAD LAPPED TERMINATIONS



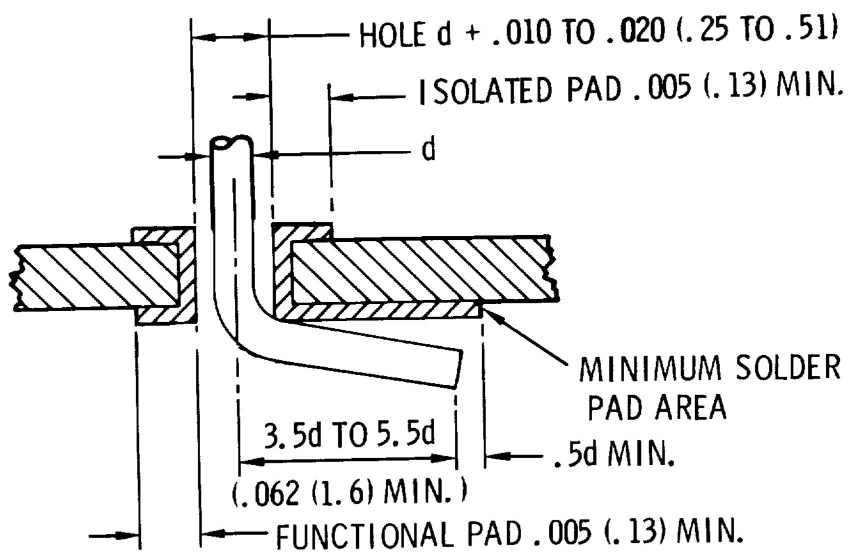
A. THROUGH-HOLE LAPPED TERMINATION



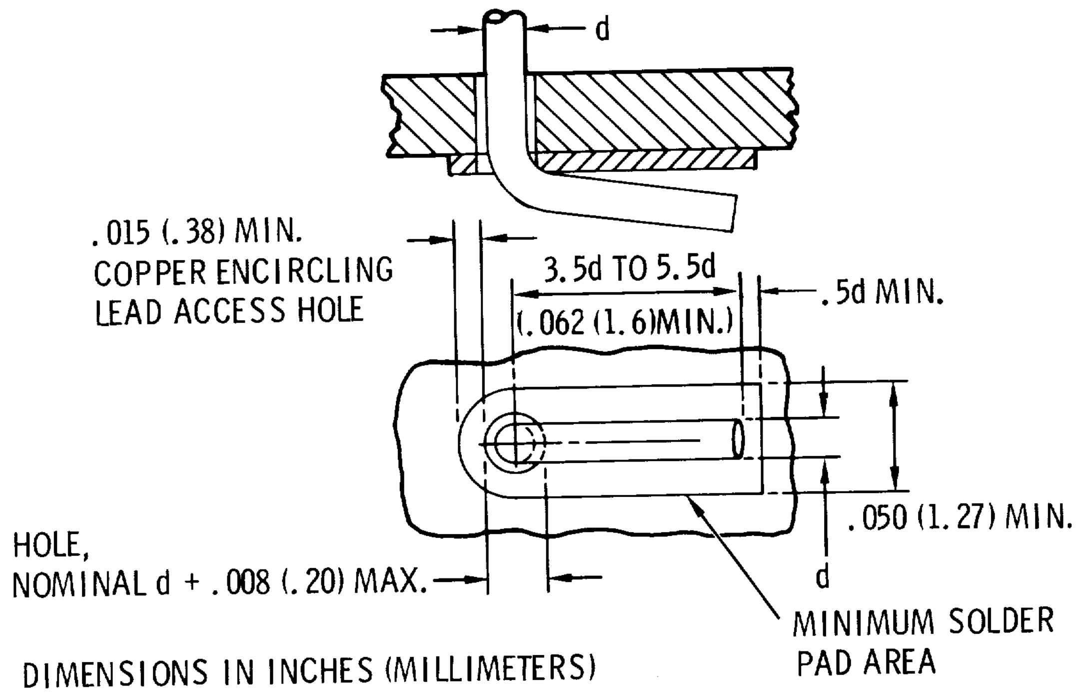
B. SINGLE SURFACE LAPPED TERMINATION

DIMENSIONS IN INCHES (MILLIMETERS)

FIGURE 5-8
RIBBON LEAD LAPPED TERMINATIONS

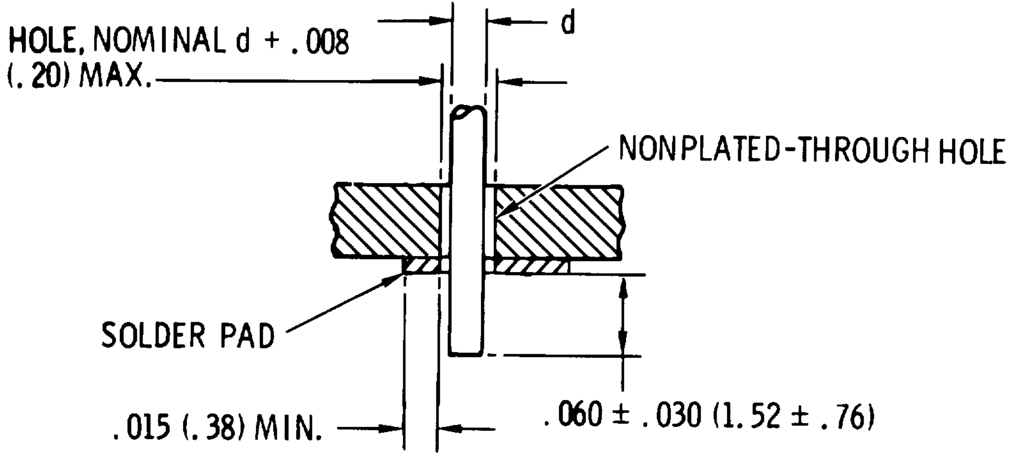


A. ROUND LEAD PLATED THROUGH-HOLE TERMINATION

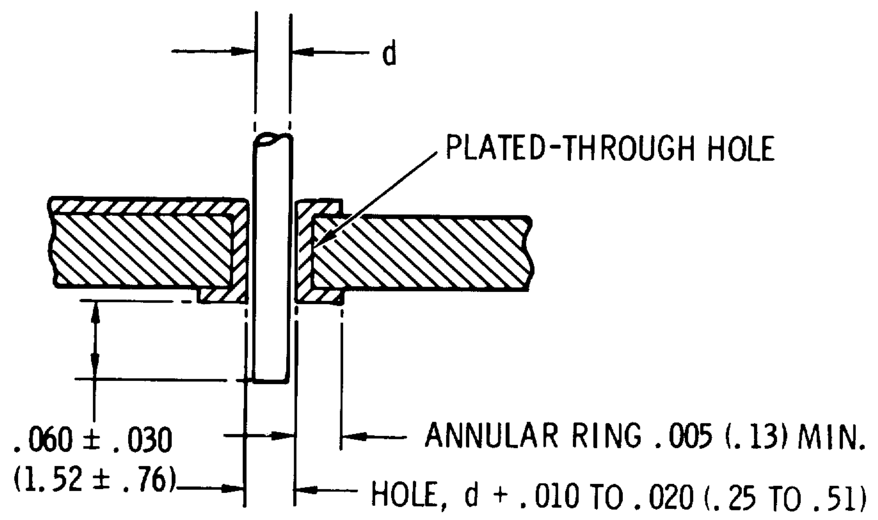


B. ROUND LEAD NONPLATED-THROUGH HOLE TERMINATION

FIGURE 5-9
THROUGH-HOLE CLINCHED TERMINATIONS



A. NONPLATED-THROUGH HOLE



B. PLATED-THROUGH HOLE

DIMENSIONS IN INCHES (MILLIMETERS)

FIGURE 5-10
STUD TERMINATIONS

3K509 TERMINALS

If terminals are required, they must be tin-lead plated and fused or solder coated in accordance with 3K404 and must have a minimum .0001 inch (.0025 mm) copper underplate in accordance with MIL-C-14550. The following general requirements apply:

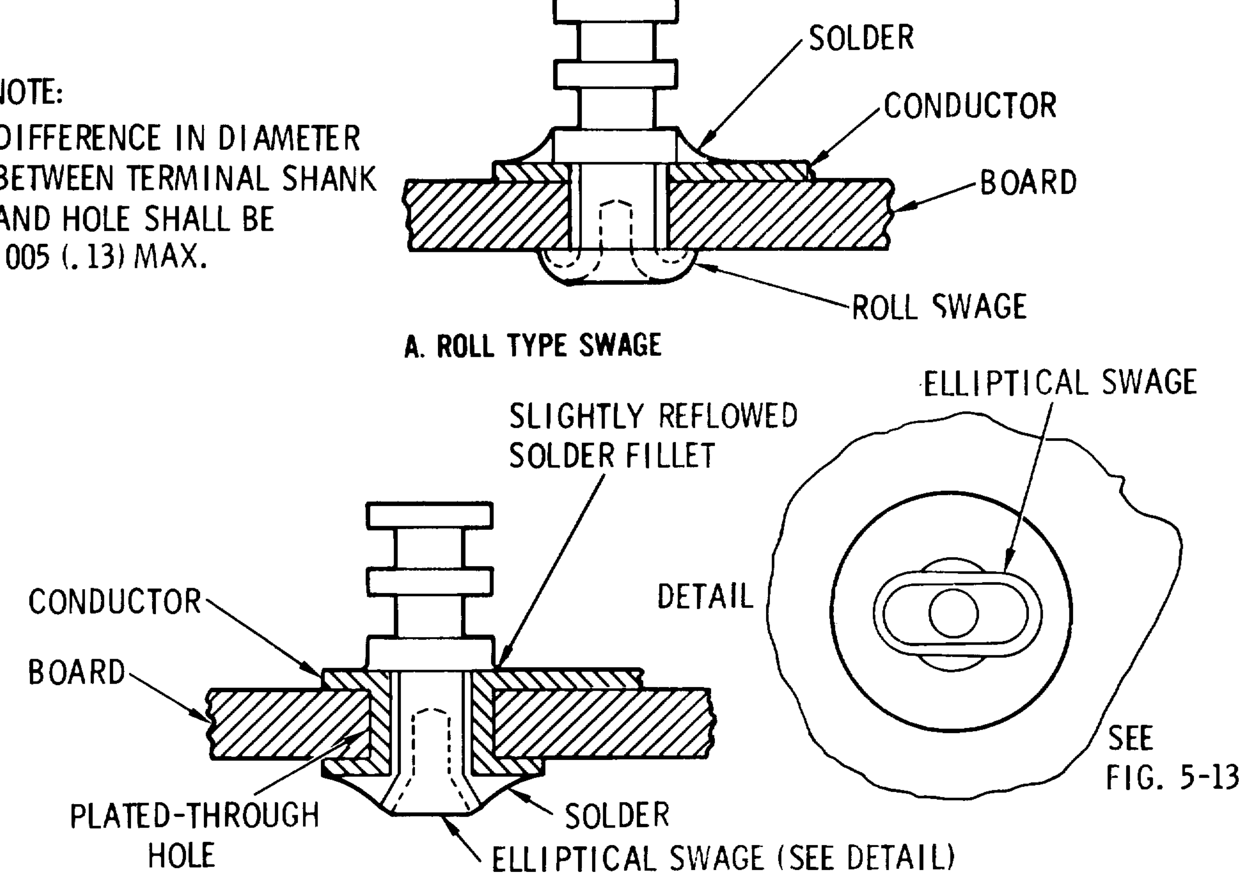
1. Use of terminals should be restricted generally to situations where parts are expected to be removed and replaced five times or more, or where there are other compelling design requirements.

2. Swage type terminals designed to have the terminal shoulder soldered to printed wiring shall be secured to the printed wiring board base material by a roll swage (see Figure 5-11A).

3. Board designs calling for soldering of the swaged end of the terminal to printed wiring shall not be used unless the solder joint on the funnel side is inspectable after subsequent soldering operations (see Figure 5-11C).

4. Terminals shall not be used as interfacial connections in printed wiring boards with nonplated-through holes.

5. Swage type terminals that are mounted in a plated-through hole shall be secured to the printed wiring board by an elliptical funnel swage to permit complete filling of the plated-through hole with solder (see Figure 5-11B and Figure 5-12).



A. ROLL TYPE SWAGE

NOTE: DIFFERENCE IN DIAMETER BETWEEN TERMINAL SHANK AND HOLE SHALL BE .010 TO .020 (.25 TO .51)

B. ELLIPTICAL TYPE SWAGE

C. V-FUNNEL TYPE SWAGE (SEE 3K509-3 FOR USAGE LIMITATION)

DIMENSIONS IN INCHES (MILLIMETERS)

FIGURE 5-11
TYPES OF TERMINAL SWAGING

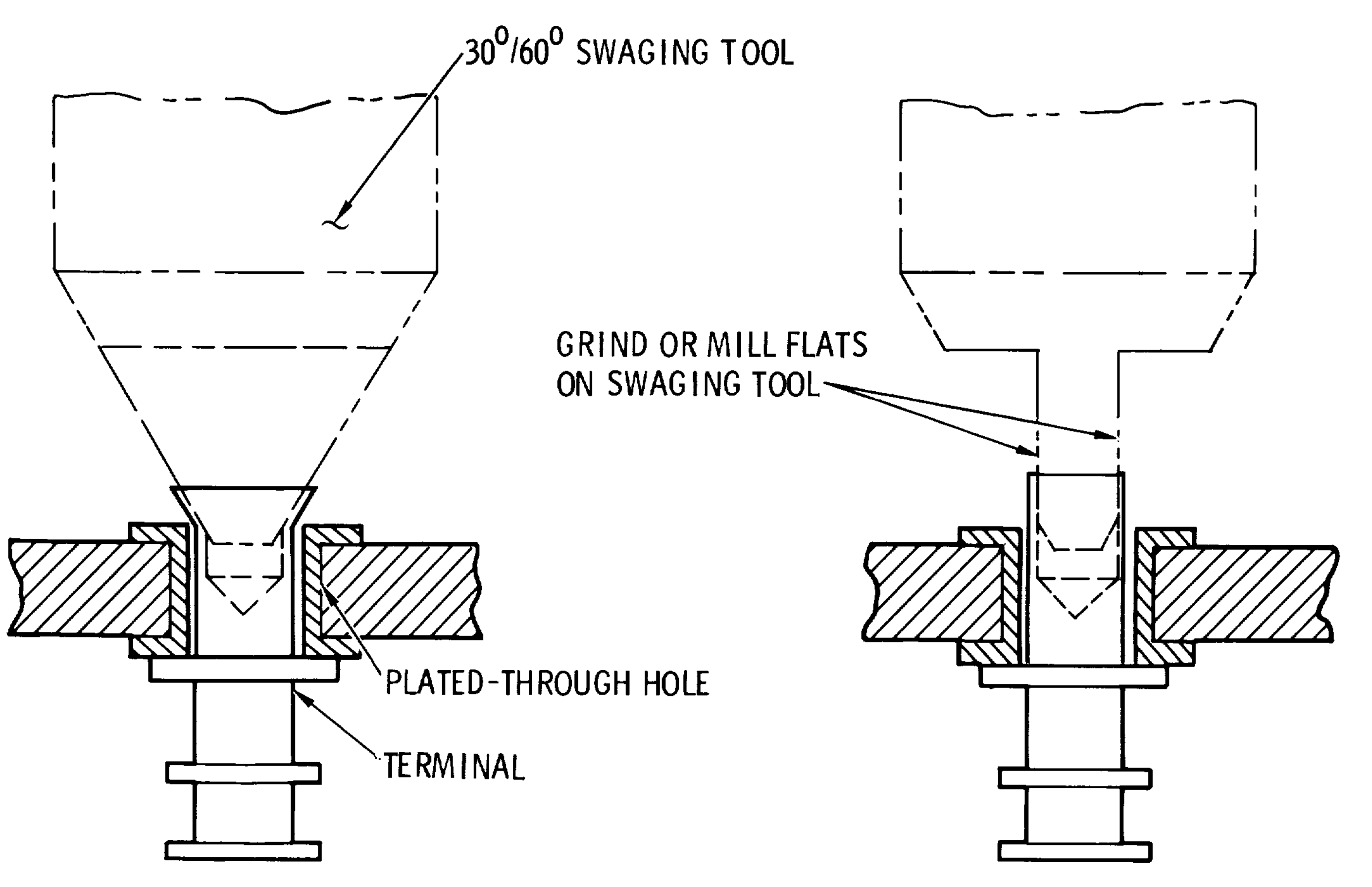


FIGURE 5-12
ELLIPTICAL FUNNEL SWAGE

CHAPTER 6: CONDUCTOR REQUIREMENTS

3K600 CONDUCTOR FOIL THICKNESS

1. **External.** The minimum foil thickness for external conductors shall be .0007 inch (.018 mm) or 1/2 ounce per square foot. When plated-through holes are used, the final thickness for external layers is .002 to 0.003 inches (.05 to 0.076 mm). This thickness is obtained by plating approximately .0015 inches (0.4 mm) of copper over the original base foil. This thickness is necessary to assure the minimum .001 inch (.0025 mm) of copper in the plated-through hole, as required by NHB 5300.4(3I).

2. **Internal.** The minimum foil thickness for internal layers of multilayer boards shall be .0014 inch (.036 mm) or 1 ounce per square foot. Internal layers should not receive additional plating.

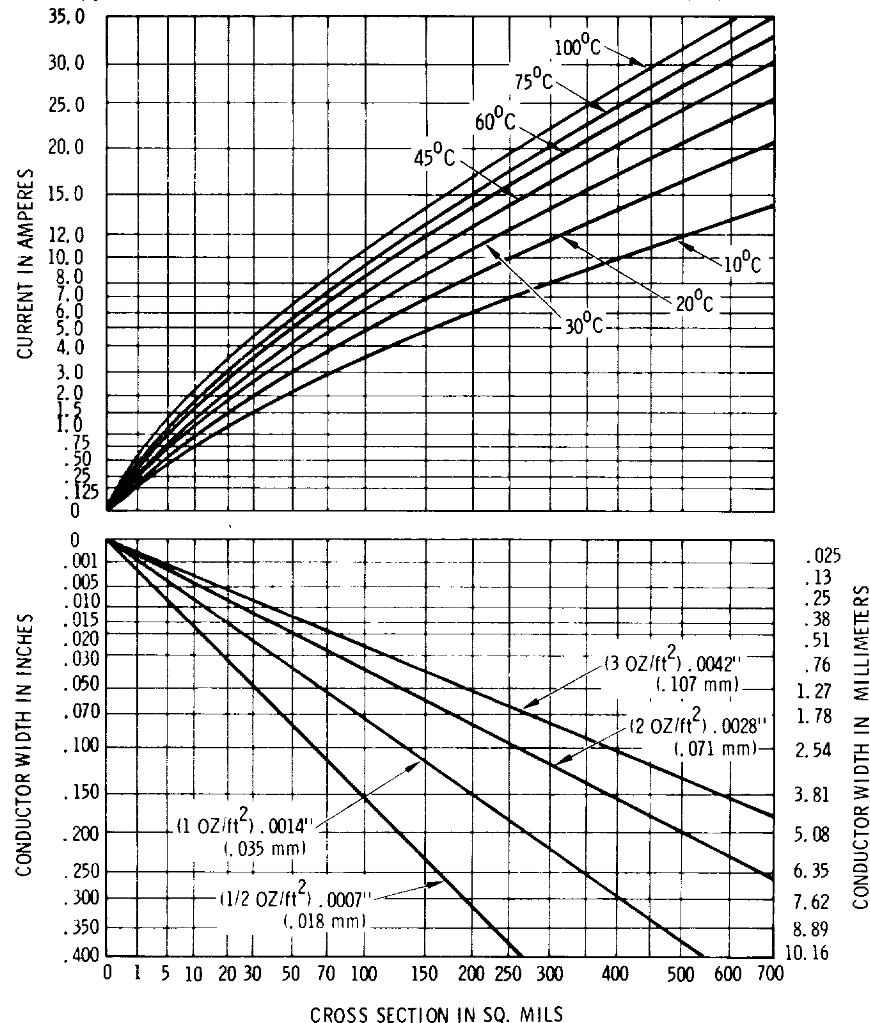
3K601 CONDUCTOR WIDTH

The minimum width and thickness of conductors on the finished printed wiring board are determined on the basis of the current carrying capacity required and the allowable temperature rise of the conductor. Figure 6-1 establishes minimum conductor widths for various copper thicknesses and temperature increases for Type 1, Type 2, and external layers of Type 3, and Figure 6-2 for internal layers of Type 3. Maximum conductor width consistent with minimum spacing requirements should be maintained for ease of manufacture and durability in use. The minimum conductor width shown on the master drawing should not be less than .008 inch (.20 mm). Unless otherwise required by special design, use 20 °C as a maximum allowable temperature rise. The designer should note that the design width of inner layer conductors on the artwork may be reduced on the finished printed wiring board due to processing by as much as twice the thickness of the copper being etched. On external layers this reduction may be less because of plating outgrowth.

3K602 CONDUCTOR SPACING

The minimum spacing as a function of voltage for conductors on the same side or layer of the printed wiring board is shown in Table 6-1.

Larger spacings should be used, whenever possible, and the designer should note that the spacing limitations in Table 6-1 apply on a given layer not only to space between conductors, but also between conductor patterns, and between conductive materials such as conductive markings and mounting hardware. Conductor spacings on finished printed wiring boards may be increased because of the possible reduction of conductor widths noted in 3K601.



NOTES:

1. THE DESIGN CHART HAS BEEN PREPARED AS AN AID IN ESTIMATING TEMPERATURE RISES (ABOVE AMBIENT) VS CURRENT FOR VARIOUS CROSS-SECTIONAL AREAS OF ETCHED COPPER CONDUCTORS. IT IS ASSUMED THAT FOR NORMAL DESIGN CONDITIONS PREVAIL WHERE THE CONDUCTOR SURFACE AREA IS RELATIVELY SMALL COMPARED TO THE ADJACENT FREE PANEL AREA. THE CURVES AS PRESENTED INCLUDE A NOMINAL 10 PERCENT DERATING (ON A CURRENT BASIS) TO ALLOW FOR NORMAL VARIATIONS IN ETCHING TECHNIQUES, COPPER THICKNESS, CONDUCTOR WIDTH ESTIMATES, AND CROSS-SECTIONAL AREA.
2. ADDITIONAL DERATING OF 15 PERCENT (CURRENT-WISE) IS SUGGESTED UNDER THE FOLLOWING CONDITIONS:
   (a) FOR PANEL THICKNESS OF 1/32 INCH OR LESS.
   (b) FOR CONDUCTOR THICKNESS OF 0.0042 INCH (3 OZ/FT²) OR THICKER.
3. FOR GENERAL USE THE PERMISSIBLE TEMPERATURE RISE IS DEFINED AS THE DIFFERENCE BETWEEN THE MAXIMUM SAFE OPERATING TEMPERATURE OF THE LAMINATE AND THE MAXIMUM AMBIENT TEMPERATURE IN THE LOCATION WHERE THE PANEL WILL BE USED.
4. FOR SINGLE CONDUCTOR APPLICATIONS THE CHART MAY BE USED DIRECTLY FOR DETERMINING CONDUCTOR WIDTHS, CONDUCTOR THICKNESS, CROSS-SECTIONAL AREAS, AND CURRENT CARRYING CAPACITY FOR VARIOUS TEMPERATURE RISES.
5. FOR GROUPS OF SIMILAR PARALLEL CONDUCTORS, IF CLOSELY SPACED, THE TEMPERATURE RISE MAY BE FOUND BY USING AN EQUIVALENT CROSS-SECTION AND AN EQUIVALENT CURRENT. THE EQUIVALENT CROSS-SECTION IS EQUAL TO THE SUM OF THE CROSS-SECTIONS OF THE PARALLEL CONDUCTORS, AND THE EQUIVALENT CURRENT IS THE SUM OF THE CURRENTS IN THE CONDUCTORS.
6. THE EFFECT OF HEATING DUE TO ATTACHMENT OF POWER DISSIPATING PARTS IS NOT INCLUDED.
7. THE CONDUCTOR THICKNESSES IN THE DESIGN CHART DO NOT INCLUDE CONDUCTOR OVERPLATING WITH METALS OTHER THAN COPPER.

FIGURE 6-1
CONDUCTOR THICKNESS AND WIDTH FOR TYPE 1, TYPE 2, AND EXTERNAL LAYERS OF TYPE 3 PRINTED WIRING BOARDS

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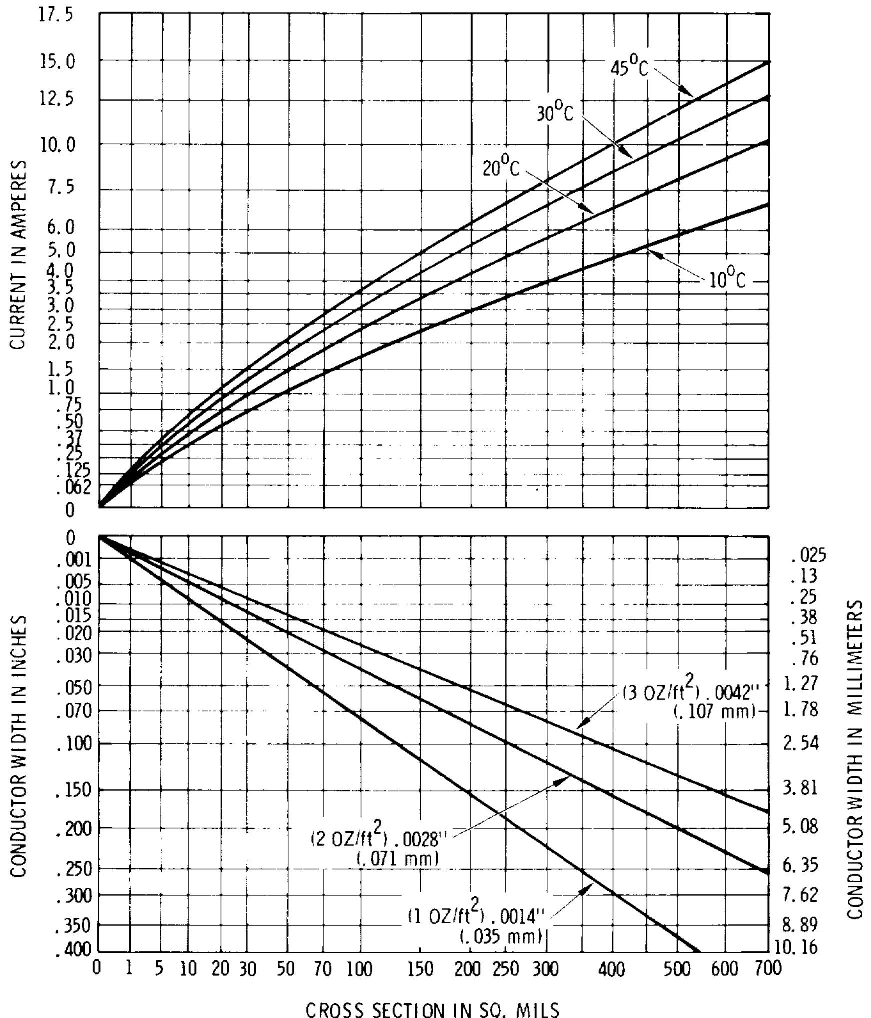

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6. THE EFFECT OF HEATING DUE TO ATTACHMENT OF POWER DISSIPATING PARTS IS NOT INCLUDED.
7. THE CONDUCTOR THICKNESSES IN THE DESIGN CHART DO NOT INCLUDE CONDUCTOR OVERPLATING WITH METALS OTHER THAN COPPER.
8. THE CURRENT MAY BE UP-RATED 100 PERCENT FOR EXTERNAL CIRCUITRY.

FIGURE 6-2
CONDUCTOR THICKNESS AND WIDTH FOR INTERNAL LAYERS OF TYPE 3 BOARDS

TABLE 6-1
CONDUCTOR SPACING FOR COATED BOARDS

Voltage Between Conductors DC or AC Peak	Minimum Spacing (Inch)	(mm)
0 to 15	0.005	(0.13)
16 to 30	0.010	(0.25)
31 to 50	0.015	(0.38)
51 to 100	0.020	(0.51)
101 to 300	0.030	(0.76)
301 to 500	0.060	(1.52)
Greater than 500	0.00012 1/	(0.003)1/

1/ Inch (mm) per volt.

3K603 MOUNTING CLEARANCES AND SPACING

1. **Mounting Hardware Clearance.** Conductive patterns other than those designed for grounding must clear all mounting features (holes, connector brackets, hardware, etc.) by a minimum of .025 inch (.635 mm) or .015 inch (.38 mm) plus the appropriate value from Table 6-1, whichever is greater, based on the worst case position of the mounting feature. This worst case position must take tolerances into account to allow for such contingencies as board shifting caused by oversized mounting holes, bracket dimensions, machining of the housing, drilling of the printed circuit board, and oversized washers. Nonplated-through holes should have a clearance around ground planes or circuitry of .040 inch (1.02 mm) minimum.

2. **Board Edge Spacing.** Spacing from the circuitry to the edge of the board is determined by design requirements such as board mounting methods, board thickness and size, proximity of adjacent circuit board assemblies and other unit parts, and special requirements and shall not be less than the spacing specified in Table 6-1. When the printed wiring board assembly is to be encapsulated as a module and if the encapsulant is at least .050 inch (1.27 mm) thick, the spacing to the edge of the board may be .003 inch (.08 mm) minimum.

3K604 LARGE CONDUCTOR AREAS

Circuitry areas greater than .50 inch (12.7 mm) diameter (generally copper used for shielding, heat sinks, ground or voltage planes) should be relieved by a series of slots, squares, or other shapes designed to furnish an electrically continuous pattern. This technique reduces the possibility of circuitry blistering and board warpage during mass soldering operations. The slots or circles should be kept clear of drilled holes.

When a large conductive area that extends beyond a 1-inch diameter circle is used on an internal layer, the layer should be placed as near the center of the board as possible. If more than one internal layer has a large conductive area, the layers should be located symmetrically within the board, e.g., layers 3 and 8 of a 10-layer board.

3K605 GUIDE CLIP SLIDE AREA

If the design calls for metal guide clips to mount the printed wiring assembly, a pattern may be etched along each side of the board in the area where the board slides into the clips to provide for heat sinking, abrasion resistance, or both. The circuit design engineer specifies whether or not this pattern is to be connected to the board ground plane to provide a chassis ground. The pattern should be plated with .0005 inch (.013 mm) nickel in accordance with QQ-N-290, Class 2. A gold overplate may also be specified.

CHAPTER 7: LAND AND HOLE REQUIREMENTS

3K700 HOLE SIZE AND LOCATION

1. **Hole to Hole Spacing.** Adjacent holes must be spaced so that the lands surrounding the holes meet the dimensional requirements of this Chapter and the spacing requirements of 3K602.

2. **Hole to Board-Edge Spacing.** Part holes must be spaced a sufficient distance from the board edge to allow lands surrounding the holes to meet the requirements of 3K602 and 3K603.

3. **Hole Sizes.** Hole diameters should be compatible with standard drill sizes, and the maximum and minimum diameters should be specified for each hole. Diameters must be compatible with hole-to-lead size ratios specified in 3K709.

3K701 ANNULAR RING

1. **External Layers.** The minimum annular ring on external layers is defined as the minimum amount of copper (at the narrowest point) between the edge of the land and the inside edge of the hole, after it has been plated for plated-through holes, or as drilled for nonplated-through holes. The minimum annular ring for nonplated-through holes is .015 inch (.38 mm). For two-sided plated-through holes and outside layers of multilayer boards, it is .005 inch (.13 mm). For terminal installations,see 3K705.

2. **Internal Layers.** The minimum annular ring for internal lands is defined as the minimum amount of copper (at the narrowest point) between the edge of the land and the edge of the drilled hole. The minimum annular ring for internal lands on multilayer boards is .002 inch (.05 mm).

3K702 MINIMUM LAND DIAMETER

To provide for the minimum annular ring requirement indicated in 3K701 and to compensate for an accumulation of tolerances during manufacture, minimum land diameter for printed wiring board holes should be as follows:

1. Nonplated-through hole: Maximum drilled diameter plus .050 inch (1.27 mm).

2. Plated-through hole: Maximum finished diameter plus .030 inch (.76 mm).

3. Terminal installation: See 3K705.

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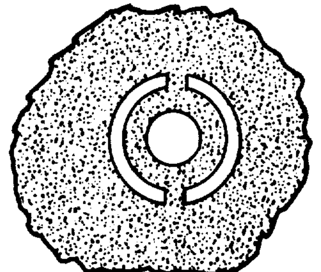
3K703 NONFUNCTIONAL LANDS (MULTILAYER BOARDS)

Nonfunctional lands shall be included on all internal layers of multilayer boards, except that they need not be used on ground planes, voltage planes, heat sinking planes, and in areas where required electrical clearances do not permit.

3K704 LANDS IN LARGE CONDUCTOR AREAS

Lands in ground or voltage planes shall be relieved locally in the area of the plated-through hole by the use of heat restrictors in order to restrict heat flow during soldering operations (see Figure 7-1).



LAND AREA AFTER
DRILLING

FIGURE 7-1
GROUND AND VOLTAGE PLANE LAND AREA (TYPICAL)
WITH HEAT RESTRICTORS

3K705 LANDS FOR TERMINAL INSTALLATION

The minimum land diameter for the installation of terminals shall be .020 inch (.50 mm) greater than the maximum diameter of the flange of the terminal for plated-through holes and .015 inch (.38 mm) for nonplated-through holes.

3K706 LANDS FOR SURFACE MOUNTED PARTS

1. **Lands for Ribbon Lead Attachment.** Required after-etching sizes of lands for ribbon leaded parts are as follows:

    a. A rectangle with the narrowest dimension equal to or exceeding 1.5 times the nominal width (W) of the lead and the wider dimension equal to 3.5 to 6.0 W plus .010 inch min (see Figure 5-8B.)

    b. Minimum spacing (see Table 6-1).

2. **Lands for Parts with Round Axial Leads.** Lands for surface terminated parts with round axial leads should be rectangular with the width 1.5 to 3.0 times that of the lead diameter (D), .050 inch (1.27 mm) minimum and the length 4.0 to 6.0 D (see Figure 5-7B).

3K707 SOLDER FILLETS

The contour of the etched pattern influences the shape of the solder fillet. Circular shapes for attachment lands are preferred because they furnish more uniform heating resulting in more uniform fillets (see Figure 7-2).

3K708 PLATED-THROUGH HOLE DIMENSIONS AND TOLERANCES

The hole size specified on the master drawing is the dimension after plating and fusing. The total tolerance should be at least .006 inch (.15 mm), preferably .007 inch (.18 mm); a typical callout would read .039 to 0.46 inch (.99 to 1.17 mm). Do not specify drill size or preplate hole diameter.

3K709 HOLE TO PART LEAD CLEARANCE

Plated-through hole diameters should be established to fit the nominal diameters of the part leads that will go through them. They should be sufficiently large to permit uniform flow of solder between the lead and the hole wall, but not so large that capillary force would be insufficient for good solder flow. To provide these conditions, holes should be no less than .010 inch (.25 mm) and no more than .020 inch (.51 mm) larger than the nominal wire diameter or diagonal dimension of rectangular leads. For nonplated-through holes, the maximum difference shall be .008 inch (.20 mm) for nominal wire diameter.

PREFERRED

(A)

UNIFORM PATTERN AROUND HOLE

(B)

(C)

(D)

NONPREFERRED

(E)

SOLDER FILLET WILL BE NONSYMMETRICAL

(F)

OUTSIDE SOLDER FILLETS
WILL BE NONSYMMETRICAL

(G)

CENTER SOLDER
FILLET WILL
BE GOOD

OUTSIDE SOLDER
FILLETS WILL
BE POOR

(H)

SOLDER WILL FLOW
TOWARD LARGE HOLE

FIGURE 7-2
EXAMPLES OF PREFERRED AND NONPREFERRED TERMINAL AREAS

3K710 HOLE TO TERMINAL CLEARANCE

For plated-through holes, the hole diameter shall be no less than .010 inch (.25 mm) and no more than .020 inch (.51 mm) larger than the nominal terminal shank diameter. For nonplated-through holes, the maximum difference shall be .005 inch (.13 mm) for nominal terminal diameter.

3K711 MOUNTING HOLES

Because screw torquing should not be done directly against laminate, circuit board mounting holes are often reinforced by a surrounding land of copper, except where there is the possibility of electrical shorting. This is especially important with type GI material due to its tendency to chip during drilling. Mounting holes shall be dimensionally located for inspection purposes. Any hole through which electrical hardware is to be swaged or bolted may have a land to support the hardware and protect the board from damage. For fabricating economy, mounting holes are normally round rather than rectangular or specially shaped. Circuit board mounting holes normally are not plated-through or counterbored.

3K712 TOOLING OR INDEX HOLES

1. The preferred tooling hole diameter is .125 + .002 − .001 inch (3.18 + .05 − .025 mm). Tooling holes should be located on a standard grid, and only one hole size and location should be used for a series of boards on a program. The primary tooling hole, or program zero, is the reference point for the two primary datums.

2. Tooling or index holes must be dimensioned on the master drawing. They are normally located inside the board outline and the center lines of the holes are used to dimension the board outline. Generally, only two tooling holes are used. If the printed wiring board outline and its two tooling holes are symmetrical, a third tooling hole is added to preclude errors. Occasionally, because of space limitation, separate tooling holes cannot be drilled within the board outline. In such cases, it is acceptable practice to designate mounting, hardware, or other holes as tooling holes, provided that the holes are not countersunk, and meet the dimensional tolerances required for tooling holes (−.001, +.002 inch). Tooling holes should never be plated-through.

3K713 HOLES FOR WIRE WRAP POSTS

1. Almost all wire wrap posts used in direct printed circuit applications are .025 x .025 inch (.635 mm) square with a nominal base dimension of .025 x .042 inch (.635 x 1.07 mm). These posts are installed by force fit in plated-through holes whose dimensions must be critically maintained so that the fit will provide adequate resistance to wrapping torque without damaging hole interface connections.

2. To hold these tolerances, the preplate drill size shall be specified as .0453 + .001 − .000 inch (1.15 + .025 − .000 mm). After-plate dimensions shall be .040 ± .003 inch (1.02 ± .076 mm). When wrap posts are soldered in place, the nominal finished plated-through hole diameter shall be no less than .005 inch (.127 mm) and no more than .010 inch (.254 mm) larger than the nominal diagonal of the post.

APPENDIX A
DEFINITIONS

The following definitions apply to terms used in printed wiring board fabrication:

Adhesion. The attractive force that exists between a coating material and its substrate that can be measured as a force required to separate the coating material and its substrate.

Annular Ring. An annular ring is the portion of conductive material completely surrounding a hole.

B-Stage. B-stage is an intermediate state of cure of a thermosetting resin.

Blister. A blister is a localized swelling and separation between any of the layers of a laminated base material or between base material and conductive foil.

Bonding Layer. A bonding layer is an adhesive layer used in bonding together other discrete layers of a multilayer printed board during lamination.

Bow (Base Material). Bow is the deviation from flatness of a board characterized by a roughly cylindrical or spherical curvature such that, if the board is rectangular, its corners or edges are in the same plane as the major surfaces of the board (see Figure A-1).

FIGURE A-1
BOW (BASE MATERIAL)

Clad or Cladding. Clad or cladding is a relatively thin layer or sheet of metal foil which is bonded to the base material.

Component. A part or combination of parts mounted together to perform a design function(s). A "black box" (e.g., transmitter, receiver, transponder,and star tracker).

Conformal Coating. An insulating protective coating which conforms to the configuration of the object coated, applied to the completed board assembly.

Delamination. Delamination is a separation between plies within the base laminate, between any of the layers of the base laminate and B-stage material, or between the laminate and the metal cladding.

Dewetting. Dewetting is a condition which results when the molten solder has coated the surface and then receded, leaving irregularly shaped mounds of solder separated by areas covered with a thin solder film; the base metal is not exposed (see Figure A-2).

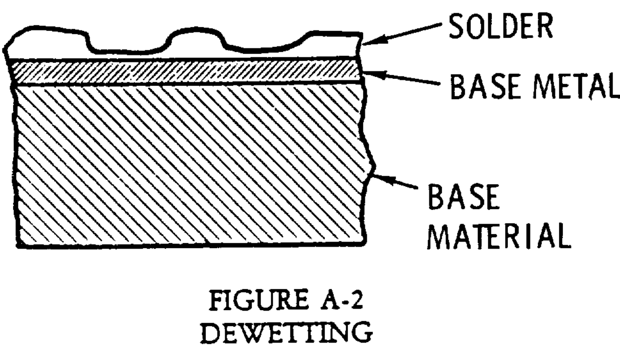


FIGURE A-2
DEWETTING

Dielectric Withstanding Voltage Tests. Tests made to determine the ability of insulating materials and spacings to withstand specified overvoltage for a specific time without flashover or puncture.

Etchback. Etchback is the process of removing glass fibers and resin between the conductor layers in order to facilitate a mechanical and electrical bond on the protruding portion of the conductor materials in the plated-through holes.

Flux. Flux is a chemically active compound that facilitates the wetting of metals with solder.

Insulation Resistance. Insulation resistance is the electrical resistance of the insulating material between any pair of contacts, conductors, or grounding devices in various combinations.

Interfacial Connection. An electrical connection between conductive patterns on opposite sides of an insulating base, e.g., plated-through hole or clinched jumper wire.

Laminate. Laminate is the product made by bonding together two or more layers of material using an adhesive with heat and pressure.

Land. A portion of a conductive pattern usually, but not exclusively, used for the connection, or attachment, or both of parts.

Mask. A mask is a coating material/resist used to cover or protect selected areas of a pattern from the action of an etchant, solder, plating, or coating.

Mass Soldering. A process wherein all or almost all solder connections on a printed wiring assembly are made simultaneously by continuous automatic or semiautomatic machinery (e.g., wave soldering).

Minimum Annular Ring. The minimum width of metal, at the narrowest point, between the edge of the hole and the outer edge of the land. This measurement is made to the drilled hole in internal layers of multilayer printed boards and to the edge of the plating on outside layers of multilayer boards and double-sided boards.

Moisture Resistance. Moisture resistance is the ability of a material to resist absorbing ambient moisture.

Nonfunctional Land. A land on internal or external layers, not connected to the conductive pattern on its layer.

Optical Punch. A hole punching machine which utilizes an optical system to accurately locate the punching tool relative to a target on the material to be punched.

Outgrowth. The increase in conductor width at one side of a conductor, caused by plating build-up, over that delineated on the production master (see Figures A-3 and A-4).

Overhang. The sum of outgrowth and undercut (see Figure A-4). If undercut does not occur, the overhang is the outgrowth only.

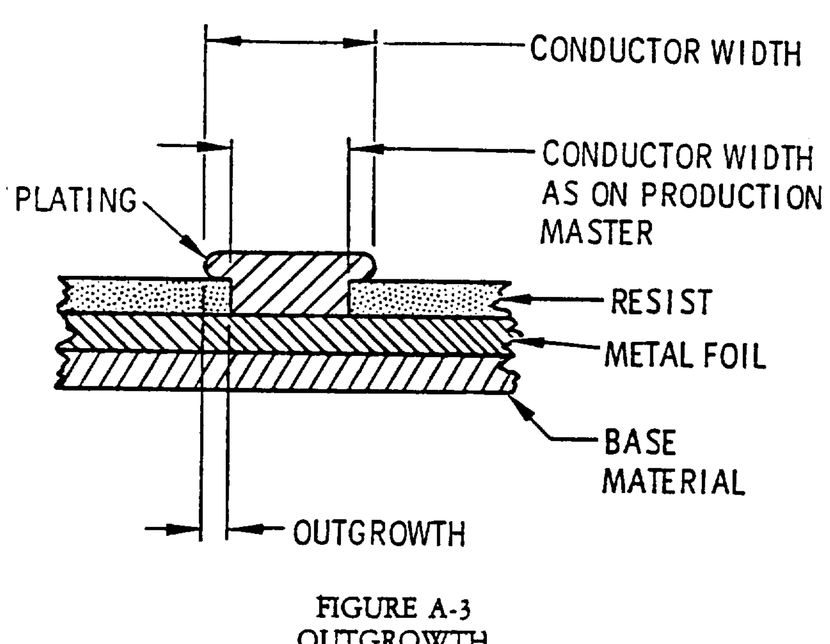


FIGURE A-3
OUTGROWTH

150-369 O - 86 - 3 QL. 3

Part. One piece or two or more pieces joined together which are not normally subjected to disassembly without destruction of design use. Synonymous with detail part or component part (e.g., resistor, capacitor, relay, and integrated circuit).

PWB. Printed wiring board.

Plasma. An etchback or chemical hole cleaning process wherein drilled panels are exposed to a dry, ionized, chemically active gas in a partial vacuum to remove resin from the hole walls.

Plated-Through Hole. A plated-through hole is an interfacial connection formed by the deposition of conductive material on the sides of a hole through the base material.

Plating Void. Plating void is the area where metal plating is missing.

Prepreg. Sheet material (e.g., glass fabric) impregnated with a resin cured to an intermediate stage (B-stage resin).

Repair. Operations performed on a nonconforming article to place it in usable condition. Repair is distinguished from rework in that alternate processes rather than reprocessing are employed.

Rework. The reprocessing of articles or material that will make it conform to drawings, specifications, or contract.

Solderability. Solderability is the property of a metal to be wet by solder.

Test Coupon (Quality Conformance Test Coupon). A portion of a printed board or panel containing printed coupons, used to determine the acceptability of such a board(s).

Thermal-Shock Test. A test used to determine the ability of a printed wiring board to withstand repeated temperature cycling without losing electrical continuity and current-carrying capacity and without degradation of the materials.

Thermal-Stress Test. A test used to determine the ability of a printed wiring board to withstand the soldering operation without fracturing the plated-through holes or other conductors and without degradation of the materials. It consists of floating the specimens on molten solder followed by microsectioning the plated-through holes and visually examining the board and the microsectioned holes.

Undercut. The distance on one edge of a conductor measured parallel to the board surface from the outer edge of the conductor, excluding overplating and coatings, to the maximum point of indentation on the same edge (see Figure A-4).

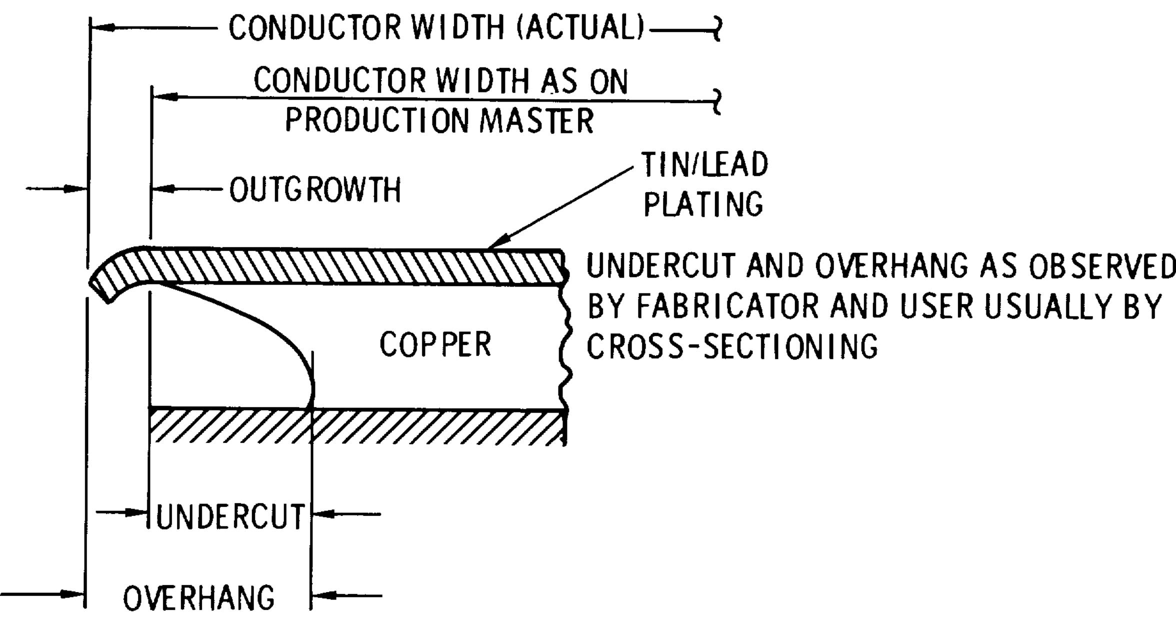


FIGURE A-4
OVERHANG AND UNDERCUT

Warp (Fabric). The warp consists of the threads of the reinforcing glass fabric that run in machine or rolled direction of the basic roll of glass fabric when woven or processed. The resulting laminated base material is usually stronger in the warp direction than in the fill direction.

Wave Soldering. A process wherein printed boards are brought in contact with the surface of continuously flowing and circulating solder.

APPENDIX B
SUPPLEMENTARY DESIGN INFORMATION
(FOR INFORMATION ONLY)

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A. PRINTED WIRING BOARD TYPES, MATERIALS, AND MANUFACTURING PROCESSES

Board Types

There are three basic types of rigid printed wiring boards: single-sided boards, double-sided boards, and multilayer boards. The fabrication of all three types is covered by NHB 5300.4(3I).

1. **Single-Sided Boards.** Single-sided boards have a conductive pattern on only one side of a dielectric substrate. The conductive pattern is usually solder coated or plated with a tin-lead alloy and fused to enhance solderability during the assembly operation.

2. **Double-Sided Boards.** Double-sided boards consist of a dielectric substrate with printed wiring conductor patterns on both sides. The two patterns are normally interconnected by holes that are plated-through with copper. As in single-sided boards, the conductive patterns and plated-through holes are usually solder coated or plated with a tin-lead alloy and fused.

3. **Multilayer Boards.** Multilayer boards have three or more layers of conductor patterns that are insulated from each other, laminated together and interconnected by plated-through holes. The requirement that these holes be accurately positioned through the lands on many internal layers has dictated extremely accurate and sophisticated registration tooling. The almost universal use of precision plotters for multilayer artwork generation and numerically controlled drills for multilayer board drilling is an outgrowth of these requirements. As with the other types, the outer layer conductor patterns and plated-through holes are solder coated or plated with a tin-lead alloy and fused to provide a readily solderable surface.

Board Materials

Conventional printed wiring boards consist of etched and plated conductors on a plastic dielectric base. The materials involved, therefore, are the plastic insulators or dielectrics, the metal foils that clad these dielectrics, and the metals that have been plated and etched to form corrosion resistant and solderable circuitry.

1. **Dielectrics.** The substrate materials used in printed wiring board fabrication are all made in essentially the same manner. The basic building block is created by impregnating woven glass cloth with resin in liquid form and then partially curing the resin by controlled heat exposure to a tack-free condition (B-stage). The material is then cut into sheets of "prepreg," normally 38 inches wide and from 44 to 74 inches long. The cloth is available in nominal thicknesses from .001 inch to .007 inch, and the two primary resin systems are epoxy and polyimide.

   The required thickness is achieved by simultaneously laminating a preselected number of prepreg sheets together with metal foil (usually copper) on one or both sides under sufficient heat and pressure to complete the cure of the resin. Variations in thickness are achieved by using different quantities and thicknesses of prepreg sheets. After lamination, the sheets are trimmed to standard sizes, typically 36 by 42 inches, 36 by 48 inches, or 36 by 72 inches. Other sizes may be available depending on the press capabilities of the laminator. The B-stage plies of resin and glass cloth (prepreg) are also used as the bonding material between layers in the production of multilayer printed wiring boards.

2. **Metal Foils.** The principal metal foil used is electrodeposited copper in thicknesses ranging from 1/8 ounce to 15 ounces per square foot. Based on a nominal thickness of .0014 inch for 1-ounce material, typical thicknesses run from approximately .0002 inch to .021 inch. The electrodeposited foil is produced by direct electrodeposition on a highly polished stainless steel drum rotating through a copper plating solution. The drum is kept in a cathodic state and the thickness of the deposited copper is controlled by varying current density in the plating bath and the rate of rotation of the drum. As the foil forms, the side adjacent to the drum (drum side) develops a smooth, polished surface, while the outer side has a dull, matte finish. This matte surface is subsequently treated chemically to enhance its bondability. For some multilayer applications, the drum side is also treated to produce a "double treat" foil. By proper selection of code identifiers in MIL-P-13949, the copper foil on each side of a laminate may be individually specified to any desired condition and thickness.

   Polyimide and epoxy are the two most commonly used resin systems. If the epoxy is required to be self-extinguishing, up to 20 percent brominated epoxy resin may be added to meet Underwriter's Laboratory standards. Boards used for very high frequency circuits may be made from Teflon-glass materials because of their low (2.2 - 2.5) and closely controllable dielectric constants.

   Polyimide-glass is more resistant to thermal damage at soldering temperatures than is epoxy and, therefore, is favored when rework is probable. In addition, since it has a lower Z-axis coefficient of thermal expansion, a lower stress is imparted to the plated-through hole copper during thermal excursions. Table B-1 shows typical property value comparisons between polyimide-glass and epoxy-glass.

150-369 O - 86 - 4 QL. 3

TABLE B-1
TYPICAL MATERIAL PROPERTY COMPARISON — POLYIMIDE-GLASS VERSUS EPOXY-GLASS 1/

Parameters	Test Temperatures			Percent Change From Original Ambient Value	
	50 °C	100 °C	250 °C	Humidity Conditioning 2/	Temperature Conditioning 3/
Dielectric constant at 1 MHz	4.65 (4.8)	4.60 (5.1)	4.80 (—)	+9.1 (+1.7)	−2.2 (+1.0)
Dissipation Factor at 1 MHz	0.005 (0.019)	0.006 (0.010)	0.010 (—)	+70.1 (+11.5)	−31.2 (+6.0)
Z-axis thermal expansion coeff (in/in/ °C × 10^{-5}) 4/, 5/	4.6 (6.5)	4.4 (5.0)	4.0 (20.0) 6/		
Flexural strength retention (percent)	99	97	72		

1/ Values for epoxy-glass are in parentheses.
2/ 65 hrs at 25 °C (77 °F) and 90 percent relative humidity.
3/ After baking 70 hours at 125 °C (257 °F).
4/ Glass transition temperature (T_g) is 115 °C (239 °F) for epoxy-glass and 270 °C (518 °F) for polyimide-glass.
5/ X-Y axis values are controlled primarily by the glass cloth.
6/ Approximate value.

Board Manufacturing Processes

Almost all plated-through hole printed wiring boards are made with essentially the same sequence of mechanical and chemical processing steps. Some are omitted for single-sided or double-sided nonplated-through hole boards, and additional ones are required for multilayer. The following sequential steps define a typical process. Tooling requirements are described where appropriate.

1. **Drilling**. All holes which are to be plated-through are drilled as a first operation, either by numerically controlled (N/C) equipment or with specialized non-N/C machines developed specifically for the industry. For N/C drilling, hole location is established on the tape, and most machines are equipped with automatic drill changers holding from five to seven different sizes which are selected by the machine by tooling order on the tape. On non-N/C equipment, all holes of a given size are consecutively sequenced. Plated-through holes are drilled .003 - .006 inch oversize to accommodate subsequent copper and tin-lead plating. Nonplated-through holes are either located by undersized holes drilled in this step for subsequent enlargement or are put in by a second drill after plating.

Tooling Requirements. For small quantities of parts, drilling may be done visually with no tooling, locating to a circuit pattern preprinted on the panel. When N/C drilling equipment is used, a drill tape or drill list containing directions for the location of all holes, the drilling sequence, and tool change orders for different drill sizes is required. Specialized, non-N/C equipment usually requires a hard template with each hole location established by a cone shaped depression that is picked up by a stylus on the machine.

2. **Electroless Copper.** To permit the electrodeposition of copper through the holes, the polymer surface of the hole wall must be made electrically conductive. This is done by exposing the panels to a series of solutions which successively activate the surface, first by reducing and depositing an almost monomolecular film of palladium, and then by the autocatalytic deposition of 5-30 microinches of electroless copper through the holes and on the panel surface. Once continuity has been established, a copper film of .0001 - .0002 inch, called a copper strike, is electrodeposited to protect the film during the next processing steps. In some operations, the electroless deposition of copper is allowed to continue until a thickness of .0001 - .0002 inches is reached, eliminating the need for the electrodeposited strike.

3. **Photoimaging.** To maintain close control of conductor width and spacing, the electrodeposited copper and the subsequent tin-lead plating should be deposited only on the circuits themselves. To accomplish this, a photoimaging process is used. Almost all photoimaging today is done with dry-film photopolymers, laminated to the copper surface of the board. A negative plating resist pattern is established by exposing the ultraviolet (UV) sensitive film through a positive film master of the circuitry. The photo resist, by the action of the UV light, is hardened only in the clear areas of the film, which are the noncircuit areas of the positive. Development in an organic or aqueous solvent removes the unhardened material, exposing bare copper in the circuit areas.

Liquid photoresist is still used by some manufacturers. It may be applied by spray coating, dipping, or roller application. It reacts in the same manner as the dry-film material, but, since it is quite thin, the plating has a tendency to grow out over it, widening the conductors.

Where circuit densities are low and board volume is high, resists may be applied by silk screen techniques, although this approach is used mainly in commercial, single-sided applications.

Tooling Requirements. A positive 1:1 film master of the printed wiring patterns for both sides. These are normally reproduced on stable .007 inch Mylar® film with either a silver halide or diazo emulsion.

4. **Copper Electroplate.** To provide the full .001 to .0015 inch of copper normally required on the hole wall, electrodeposition is used; the copper is deposited through the hole and on the exposed conductors and lands on the surfaces. The use of plating resist to limit the deposit of copper and solder only to the circuit area is called "pattern plating." In some applications, the full thickness of copper is plated over the entire panel and the resist is applied to limit the solder plate. This technique, called "panel plating," is generally less desirable, since it requires that the etching operation remove this additional plated copper as well as the original .0007 to .0014-inch base copper. In pattern plating, only the base copper and the strike are required to be etched. Many types of copper plating systems exist, but the two most commonly used are an alkaline system using copper pyrophosphate and an acidic copper sulfate. The acid copper deposit has a more needle-like grain and generally a higher ductility at room temperature than the pyro deposit; however, it is more susceptible to embrittlement from organic contamination. Both systems use organic brighteners to promote throwing-power or covering ability, grain refinement, and deposit brightness. Pyro plating baths are often operated without brighteners to improve the plating ductility. However, this requires more stringent control of the plating baths.

5. **Tin-Lead Electroplate.** After either pattern or panel copper plating, a layer of tin-lead is electrodeposited selectively on the circuitry, land areas, and in the holes. Tin and lead are codeposited from an alloy plating bath typically in a ratio of 55 to 75 percent tin, and the balance is lead. This provides a highly solderable surface for subsequent assembly and corrosion protection for the copper and serves as an etch resist during later removal of unwanted copper.

6. **Etching.** After the conductive paths and lands have been defined and covered by the copper/solder plate, the superfluous copper must be removed. It is first exposed by removing the covering layer of photoresist material with an organic solvent. In order to preserve the solder coated areas, the etching of the copper must be done in a solution which will attack copper but not solder. The most commonly used etchants are proprietary ammoniacal solutions, chromic acid, and ammonium persulfate. Because of waste disposal problems, use of the latter two is diminishing rapidly, and almost all etching of solder coated circuitry is done with ammoniacal solutions, operating in a closed loop to a constant copper content for consistency of etch.

7. **Fusing.** Solder-plated boards are fused to convert the tin-lead to a true alloy and to provide verification of preplate cleaning, improved solderability, and extended shelf life. Fusing is done typically by immersion in hot oil at about 425° to 450°F or in a specially designed infrared oven.

8. **Contouring.** The outside configuration of the board is normally cut by pin routing. This may be done manually, using as a guide a routing block accurately cut to the outside configuration of the board, or by tape control of an N/C router. Special inside cutouts, if required, may also be done at this time.

Tooling Requirements. A hard template of the outside (and inside, if necessary) configuration or a tape if N/C routing equipment is used.

9. **Solder Masking.** A polymeric coating is applied directly over the printed wiring board, leaving only the land areas exposed. The material is either a silk-screened epoxy or a proprietary photopolymer film that can be developed to expose only the land areas. In the most commonly used approach, the solder plating is stripped in the areas where the resist is to be applied (typically all circuitry except land areas used for soldering) to expose bare copper. To enhance the bond of the resist to the copper, an oxide layer is frequently formed on the copper surface by chemical treatment.

Manufacturing Processes Unique to Multilayer Board Fabrication

1. **Inner Layer Print and Etch.** Prior to lamination, circuitry on inner layers is formed by a print and etch operation. These layers or details normally consist of thin (.004 to .025 inch) laminate, clad on one or both sides with copper. In the inner layer photoimaging operation, a dry film photoresist is applied to the copper surface by lamination. It is exposed to the UV light source through a negative circuit image film which exposes and permits the hardening of the resist only in the conductor and land areas. When the unexposed resist is removed by the developer, only circuitry is covered. The unwanted copper is removed by etching. The same etchants used with solder resist may be used and frequently are, but, in addition, etchants such as cupric chloride are popular.

   Tooling Requirements. A negative 1:1 film master of the printed wiring pattern for each internal layer, and a punching fixture or optical punch to accurately locate the tooling holes in the individual layer material and in the film negative of the individual layer circuit pattern.

2. **Inner Layer Oxidizing.** Prior to lamination, it is desirable to treat the surfaces of the inner layer circuitry to enhance their bondability during lamination. This is done by immersing the layers in a hot, strongly oxidizing solution which forms a thin black or brown copper oxide film on the copper conductors. This treatment more than doubles the strength of the subsequent inner laminate bond.

3. **Laminating.** The lamination step creates the multilayer board by bonding together the individual circuit details consisting of thin laminates with etched circuitry on one or both sides. The bonding material or prepreg is thin glass cloth preimpregnated with the appropriate epoxy or polyimide resin system, and partially cured, or B-staged, to a tack-free condition.

Lamination generally takes place in a hydraulic press with platens heated by electricity, steam, or hot oil. The laminate book, consisting of alternate etched details and plies of prepreg, is placed between steel or aluminum plates, protected by a dry-film mold release, and held in the press from 1 to 4 hours under a pressure of 200 to 300 psi and at temperatures varying from 350 °F for epoxy up to 425 °F for polyimide. This cycle completes the cure of the resin and establishes the structural integrity of the multilayer board.

It is critical that close layer-to-layer registration between circuits be maintained to assure that drilled holes fall within the proper circuit land on each layer through the board. This is accomplished by a specific pattern of tooling holes keyed to each individual layer of artwork film and each detail layer. These are matched to tooling pins in the lamination plates and finally to the N/C drill tape itself.

Tooling Requirements. Flat ground steel or aluminum laminating plates with accurately located tooling holes to control registration of the hole and circuit patterns from layer to layer.

4. **Etchback or Cleaning.** After the multilayer laminate has been drilled, the last unique operation is a cleaning or etchback step to remove any resin that has been smeared during the drilling operation and assure good electrical contact between the internal copper lands exposed by drilling and the subsequently plated-through copper barrel. On epoxy boards, sulfuric or chromic acid is used to remove resin, followed by hydrofluoric acid to clean out exposed glass fibers. Because polyimide resin is inert to most chemicals, etchback is accomplished either by mechanical abrasion or by plasma attack. Plasma may also be used on epoxy boards.

5. **Processing After Etchback.** Following the etchback step, all subsequent processing of multilayer boards is the same as that used for two-sided boards.

6. **Electrical Testing.** Shorts or open circuits in two-sided boards are generally apparent to visual examination, but this is not the case with mutlilayer boards. The possibility of finding board failures only after component assembly and test makes it almost mandatory that they be checked electrically prior to use. Microprocessor driven automatic test equipment can ''ring out'' a highly complex board in seconds and give reasonable assurance that the board is electrically sound. Interface to the board is made through a pattern of spring loaded contacts, and testing can be done at voltages up to 1000 volts. Most of the testers are self-programming from a known good board.

   Tooling Requirements. An electrical test fixture for continuity and short testing.

7. **Microsectioning.** Metallurgical techniques are used to examine cross-sections of plated-through holes at magnifications of 50X to 200X to verify such things as drilling and plating quality, the integrity of internal connections to the plated-through hole barrel, and the ability of the internal structure to withstand thermal stress testing.

B. GENERAL DOCUMENTATION INFORMATION

1. Sequence of Drawing Development

Figure B-1 illustrates the normal sequence of drawing development, and the usual area of responsibility for each stage. The minimum requirements that the designer must receive from the circuit design area are a schematic diagram which defines basic circuit functions, voltages, frequencies, currents and other special details, a parts list detailing parts, and a list of end product requirements establishing the physical parameters of the board. From this, the designer can produce a printed wiring layout which leads into the artwork or artwork master, the master drawing, and the assembly drawing and from these manufacturing can derive the production master or multiple image production master and thence the finished board and assembly.

2. Order of Preparation

The normal chronological sequence for preparation of the drawings and forms associated with a printed wiring assembly is as follows:

a. Schematic diagram.

b. Parts list.

c. Printed wiring layout.

d. Artwork master (including marking master and solder mask artwork).

   If manual preparation of the artwork is necessary, the sequence is as follows:

   (1) Land master.

   (2) Photographic (contact print) Mylar® copies of artwork (printed wiring and marking).

   (3) Printed wiring artwork.

   (4) Marking artwork.

   (5) Photographic Mylar® copies of artwork (printed wiring and marking).

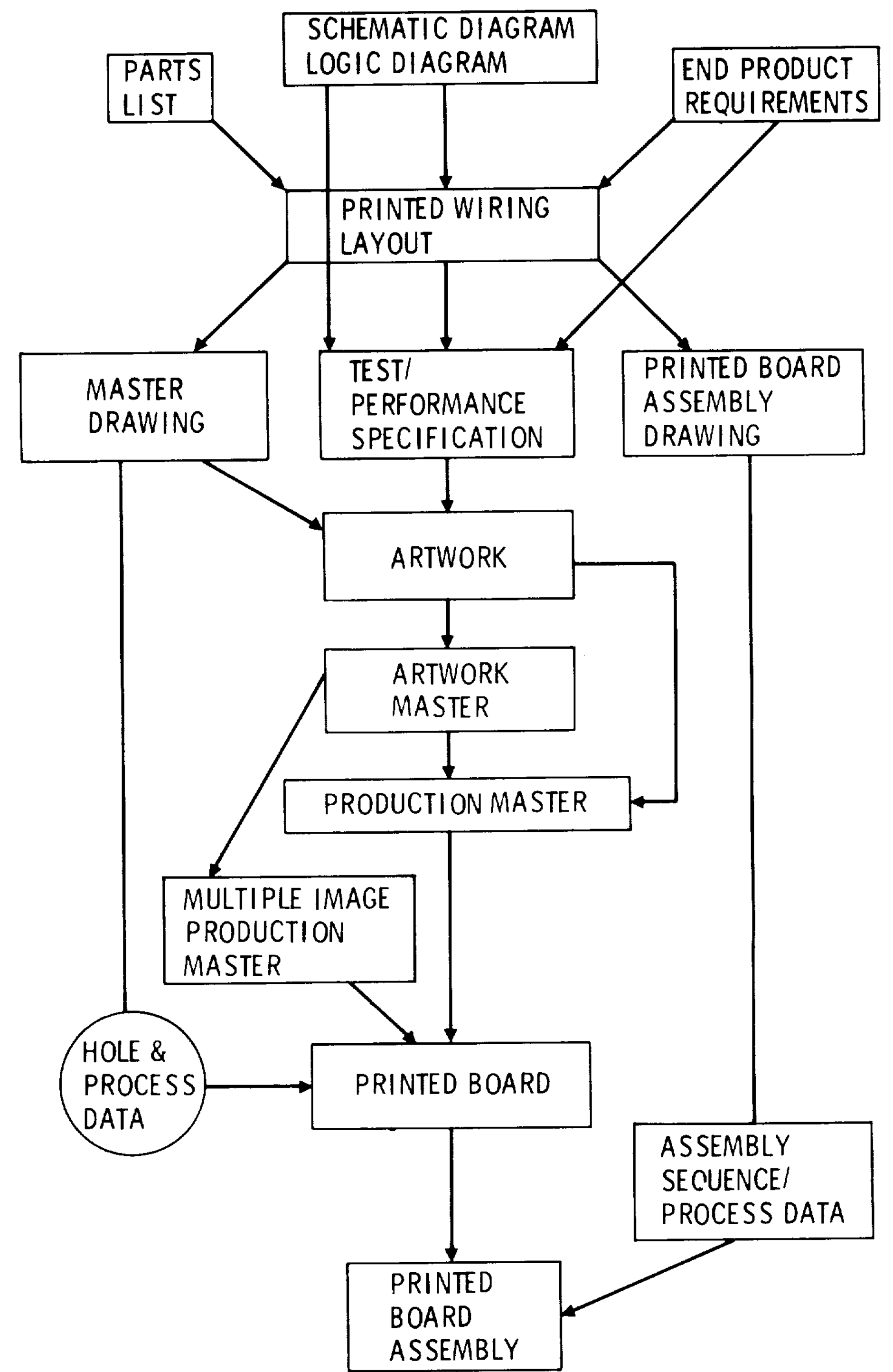

FIGURE B-1
SIMPLIFIED FLOW CHART OF PRINTED BOARD DESIGN/FABRICATION SEQUENCE

e. Master drawing.

f. Detail fabricated part drawing (brackets, clips, etc.).

g. Assembly drawing.

3. **Schematic Diagram**

A clear, readable schematic diagram should be provided containing the following information as a minimum:

a. The circuit elements (integrated circuits, transistors, diodes, resistors, etc.) and their interconnections.

b. Nomenclature for all input and output signals to and from the assembly and preestablished input/output assignments when necessary.

c. All signals to be monitored with test points.

d. Returns and grounds (when more than one) to be indicated with separate distinct interconnections and/or symbols.

e. Maximum voltage level for each signal that exceeds ± 15 volts.

f. Maximum continuous current and/or time current profile for each signal that exceeds 1.5 amps.

g. Maximum continuous power dissipation and/or time dissipation profile for each circuit element that exceeds 0.5 watt.

h. Any signal that is particularly sensitive to noise pickup, and any signal likely to create problems for other signal lines due to rapid switching, or any other signal line that has critical impedance requirements.

4. **Master Drawing**

a. **Single Sheet Master Drawing.** Wherever practicable, all information should be placed on one sheet; however, if the number of holes or the complexity of the pattern would cause a drawing to become too complicated or difficult to interpret, a multisheet master drawing should be prepared.

b. **Multisheet Master Drawing.** The first sheet(s) of a multisheet master drawing shall establish the size and shape of the printed-wiring board, the diameter, tolerance, and location of all holes, and shall contain all notes. Any and all pattern features not controlled by the hole sizes and locations shall be adequately dimensioned, either specifically or by notes. Subsequent sheets shall establish the shape and arrangements of the conductor and nonconductor patterns on each layer of the printed wiring board.

5. Material Callouts

a. Copper-clad laminate materials for all types of printed wiring boards are specified in accordance with MIL-P-13949. A typical callout for a double-sided epoxy-glass board would be as follows:

Type GFN-0590-C1/C1-B-2B

The elements of this callout have the following meanings:

GFN — Signifies flame retardant glass-epoxy with no coloring material. Polyimide-glass would be denoted by type GIN.

0590 — This number is the thickness of the core only (less copper) in ten thousandths of an inch (nominal overall thickness is .062 inch).

C1/C1 — Denotes 1-ounce copper on both sides. The "C" also indicates that the copper is electrodeposited drum (shiny) side out. Other classifications of copper may only be used for specific engineering requirements.

B — Grade of pits and dents.

2 — Tolerance grade, in this case, ± .005 inch.

B — Grade of bow and twist.

b. Standard board thicknesses should be used when possible, e.g., .031, .047, .062, and .093 inch with the selection based on such considerations as strength, mechanical support, and minimum plated-through hole sizes.

c. For multilayer boards, select type GE, GF, or GI single- or double-clad laminate material conforming to MIL-P-13949, using the same callout as above, except that base material thickness of individual layers is not normally specified, unless there is a specific electrical requirement. Minimum thickness of laminate material is .002 inch although minimum dielectric spacing between layers is .0035 inch. Copper is specified for each side, either as "C" for drum-side-out or "D" for double-treat. Grades of pits and dents and classes for thickness tolerance are specified as applicable, but bow and twist are not because of the lack of rigidity in the thin laminates.

6. Datums

There shall be two mutually perpendicular datums for each board (see Figure B-2). Datums are base lines for determining the pattern location, and are established by at least two holes, points, or symbols. The datums shall be located on grid and should be within the outline of the printed wiring board.

7. Design Layout Grid System

All holes, lands, contacts, targets, and other features on the layout, such as board outline and conductors, must be located at intersections of the modular grid system or dimensioned. Dimensions are specific in accordance with the true position technique, using the X and Y axes as datum lines. Features not otherwise dimensioned are centered at the nearest grid intersection.

a. **Multilead parts.** Multilead parts requiring holes that cannot all be located at grid intersections must be mounted with one of the following hole patterns:

- The hole for at least one part lead is located at a grid intersection, and the other holes in the pattern are dimensioned from that location.

- The center of the pattern is located at a grid intersection, and all holes of the pattern are dimensioned from that grid location.

b. **Land location.** All lands, except when part of a multilead component pattern, are located at grid intersections. For digital numerical control processing only, temporary reference axes must also be established outside the board, with origin near the lower left corner (see Figure B-2). When numerical control information for drilling is captured during the digitizing process, the point of origin called program zero is identified by a separate pattern located at the X-Y datum reference point as shown in Figure B-2. This grid reference point must appear on all pertinent drawings and must be dimensioned from the permanent X-Y datum axis when used.

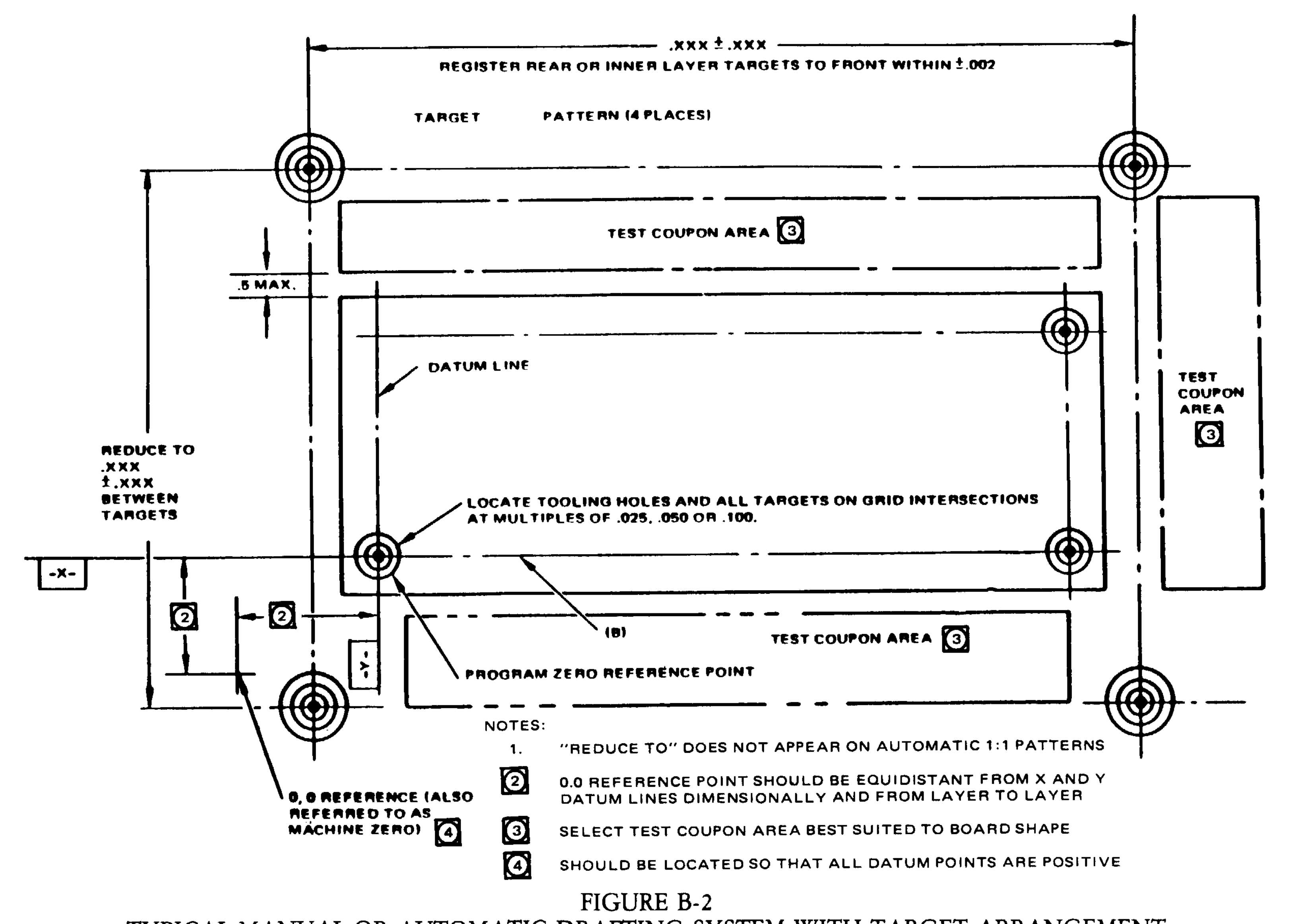

FIGURE B-2
TYPICAL MANUAL OR AUTOMATIC DRAFTING SYSTEM WITH TARGET ARRANGEMENT
(DISTANCE BETWEEN TARGETS SHOULD ALWAYS BE GREATER THAN
MAXIMUM CIRCUIT PATTERN)

8. Computer-Aided Design

a. In-house computer-aided design centers for semiautomatic routing are located in some facilities. This "autorouting" is done by computer after a data capture step initiated by the printed wiring board designer. Many of these autorouting systems are not truly interactive and require design inputs. A schematic, parts list, layout and board outline with design rules would represent a typical input. A form of digitizing is used to enter part locations and board size, while a computer program operates on interconnect nodes entered by keyboard to route the required traces on each layer. The computer generated data file is used again to drive photoplotting equipment to get the artwork master film for each layer.

b. Truly interactive design systems exist which allow an operator to design all aspects of the printed wiring board from a graphics work station. The parts placement, by selection from a library, can be done on screen, in real time, and the editing is equally simple, without laborious hand rearrangement. Also, the autorouting process can be reviewed and guided in real time so that special features can be under operator control as needed. As before, the computer generated data file can be used to drive photoplotters.

C. MISCELLANEOUS DESIGN CONSIDERATIONS

1. **Thickness Control for Multilayer Boards.** The finished overall thickness of a multilayer board can be estimated using the chart shown in Figure B-3. This illustrates the construction of a typical six layer board using 3-6 mil thick cores clad with 1-ounce copper layers, 2-ounce ground and voltage planes, and three plies of prepreg between internal details. In addition to the external circuitry, it has two internal signal layers, one ground and one voltage plane.

Step 1 - Sketch core materials (a six-layer board has three cores).

Step 2 - Sketch metal layers, and enter layer description: lands, voltage plane, signal, ground plane. (Signal layers do not contribute to overall thickness because they become embedded in the prepreg.)

Step 3 - Sketch required prepreg layers. Allow one sheet of prepreg minimum for each ounce of facing copper. The absolute minimum between layers is two sheets with a thickness of approximately 2.2 mils per sheet. Three sheets minimum is preferred.

Step 4 - Enter required thickness for each layer in appropriate column.

Step 5 - Calculate total board thickness and a tolerance of ±.007 or ±10 percent, whichever is larger. (When tighter tolerances are required for edge board connectors or card guide rails, these should be specified in critical areas only.)

Layer		Description	Copper (Mils)	Core (Mils)	Prepreg (Mils)
1	Core	Lands	4 (incl. plating)	6	
2		GND	2.8		
	Prepreg				6.6 (3 plies)
3	Core	SIG	0	6	
4		SIG	0		
	Prepreg				6.6 (3 plies)
5	Core	VOLT.	2.8	6	
6		Lands	4		
	Total Thickness =		13.6 +	18 +	13.2 = 44.8 mils

FIGURE B-3
MULTILAYER THICKNESS CALCULATION

2. Stiffeners

One or more stiffeners may be required to prevent distortion or flexing of the board during vibration or for other mechanical reasons. The required stiffeners should be specified by the product design engineer. If conductive patterns must be routed under stiffeners, one of the following conditions must be met:

a. The stiffener must be an electrically insulating material; or

b. An insulating material must be used between the stiffener and the surface of the board; or

c. The stiffener must be relieved in the area of the conductive pattern.

The preferred method is a nonconductive stiffener, installed on the top side to avoid interference with wave soldering.

> **NOTE**
>
> Under no circumstance should there be a solder joint located under a stiffener.

3. Thermal Dissipation Considerations

a. **Part Body Temperature.** In selecting parts, make sure that the extreme part body temperatures that will be developed in service as a combination of part body temperature and ambient temperature are within the rated body temperature extremes for that part.

b. **Heat Sinking with Printed Wiring Patterns.** When local control of part or printed wiring board temperatures is required, the printed wiring pattern on layer 1 should function as the heat sink whenever possible. Wide conductor paths may be routed under axial lead parts, dual-in-line-parts, and flatpacks to conduct heat away from the part cases. Plated-through holes under the parts may also be provided to act as thermal ''vias'' to conduct heat to the backside of the board. To make this type of heat sinking effective, the part must be mounted with no airspace between it and the conductor path. Good thermal contact between the part and the conductor may be enhanced by specifying on the assembly drawing the requirement for a thermally conductive filleting material.

c. **Heat Sinking with Secondary Heat Sinks.** If additional cooling is required to maintain temperatures within the limits of reliable operation, heat sink plates may be added to the printed wiring board to conduct heat away from the parts. These plates, usually copper or aluminum, are normally mounted between the parts and the board and are installed either by bonding or riveting. For more detailed information, see Section G.

4. Test Points

Test points are special points of access to an electrical circuit used for testing purposes. Although many types of test points are available, the most commonly used are either turret terminals installed in plated-through holes or etched pads in the circuitry. Test points should be installed as close as possible to the point to be tested and must be located either at the end of a conductor or offset from the conductor as shown in Figure B-4.

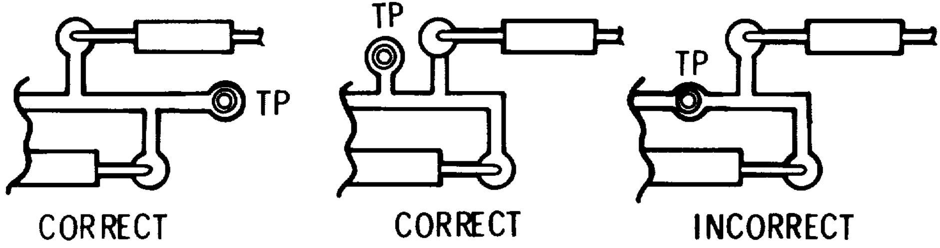

FIGURE B-4
TEST POINT (TP) LOCATIONS

D. CONDUCTORS

1. General Design Considerations

The design of conductor pattern layouts must include the consideration of such basic characteristics as the current carrying capacity of the conductors, resistance of the copper, dielectric strength, insulation resistance, capacitance, inductance, and crosstalk. Special properties such as signal propagation attenuation, characteristic impedance, EMI susceptibility and radiation also may need to be evaluated.

a. **Design Sequence.** The designer should review the schematic to determine basic circuit applications, voltage, frequencies, currents, and other special details. He/she may then group the electrical functions into the following four basic categories and consider their interactions:

(1) Signal circuits: Transmit intelligence in the form of signals. These circuits control the accuracy and legibility of the information transmitted and, therefore, are of prime importance. There may be crosstalk from one signal to another, and they are susceptible to EMI from control and power circuits.

(2) Sensing circuits: May be used for measuring temperature, pressure, or motion and are usually of low energy magnitude. They will not radiate sufficiently to cause problems in any of the other circuits and probably will not interfere with each other. Their susceptibility to EMI from the control and power circuits should be considered.

(3) Control circuits: Are used for relays, potentiometers, or gyros and are usually less sensitive to crosstalk and EMI than signal or sensing circuits and can act as a buffer between radiating power circuits and signals. Relay surges and switching arcs can be detrimental to the sensing and signal circuits.

(4) Power circuits:Transmit power from permanent power sources to motors, heaters, blowers, pumps, lamps, filaments, and various actuating devices. They are usually the greatest source of EMI and require the largest conductors.

b. **Location and Routing.** Based on this analysis, the designer should locate conductors to minimize crosstalk and EMI. No specific rules can be established regarding location and routing, but it is good design practice to locate signal and power circuits as far apart as possible, with sensing circuits or control circuits in between. On multilayer boards, ground planes may be used as shields for AC or pulsed power circuits as well as critical signal circuits.

2. **Maximum Current and Temperature Rise.** The maximum current allowable in an etched conductor should be such that the operating temperature is not raised to a point at which (1) the conductor bond fails, (2) the protective coating fails, (3) the insulation of any wire degrades in the vicinity of the board, or (4) conductive heat degrades the performance of components on the board.

In determining the temperature rise of conductors, the following factors should be considered:

- Cross-Section Area — Temperature rise of conductors is inversely proportional to cross-section area, decreasing as the area increases.

- Ratio of Conductor Width to Thickness — As illustrated in Figure B-5, Conductor B will exhibit less temperature rise than Conductor A because of the reduced concentration of mass. Heat dissipates more rapidly into the laminate in the Conductor B design.

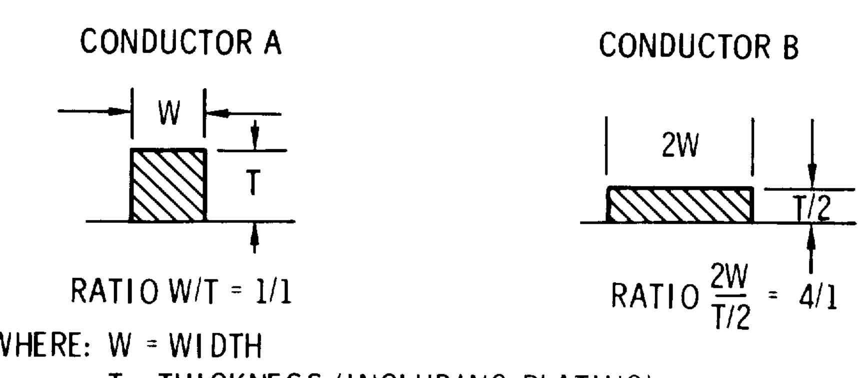

FIGURE B-5
RATIO OF CONDUCTOR WIDTH TO THICKNESS

3. **Conductor Spacing.** While the minimum spacing between conductors is primarily a function of voltage, additional spacing factors involved in printed wiring board design, which are a function of the specific application, are insulation resistance, capacitance between conductors, conductor resistance, and inductance. A conformal coating is assumed to reduce effects of humidity and contamination. If AC voltages are present, then dielectric constants and dissipation factors may be important.

4. **Parallel Conductors.** Closely spaced parallel conductors should be avoided to reduce etching and solder bridging problems. Conductors should be positioned to take full advantage of available space, thus improving board quality and producibility.

> **NOTE**
>
> Long runs of parallel conductors should be avoided whenever possible because in some circuit designs they act as high-frequency transformers that couple noise into other circuits.

E. LANDS AND HOLES

1. Land and Hole Shapes and Locations

a. Land areas are provided at each point where a part lead or other electrical connection is made to the printed wiring board. Usually each hole through which a component lead is inserted and soldered is centered in a round land. For an interfacial connection, i.e., a plated-through hole used for electrical communication from one side of the board to the other, a land surrounds the hole on each side of the board.

b. For surface mounted parts, the land is a rectangle which usually includes a plated-through hole that electrically connects the land to the circuit. This hole must not be located under the part lead. The land may also be connected to a plated-through hole by a conductor line. With the increased use and greater flexibility of photoplotting equipment for artwork construction, square or hexagonal lands are used in place of round ones when it will help a specific design. Occasionally, other land shapes are required by such design considerations as component mounting brackets.

2. **Lands and Holes for Terminal Installation.** When terminals are installed in plated-through holes, they shall be secured by an elliptical swage. If the plated-through hole has an internal connection, the terminal may be installed in an adjacent hole (plated-through or nonplated through) and connected externally to the original plated-through hole, either with a surface conductor or a wire (see Figure B-6).

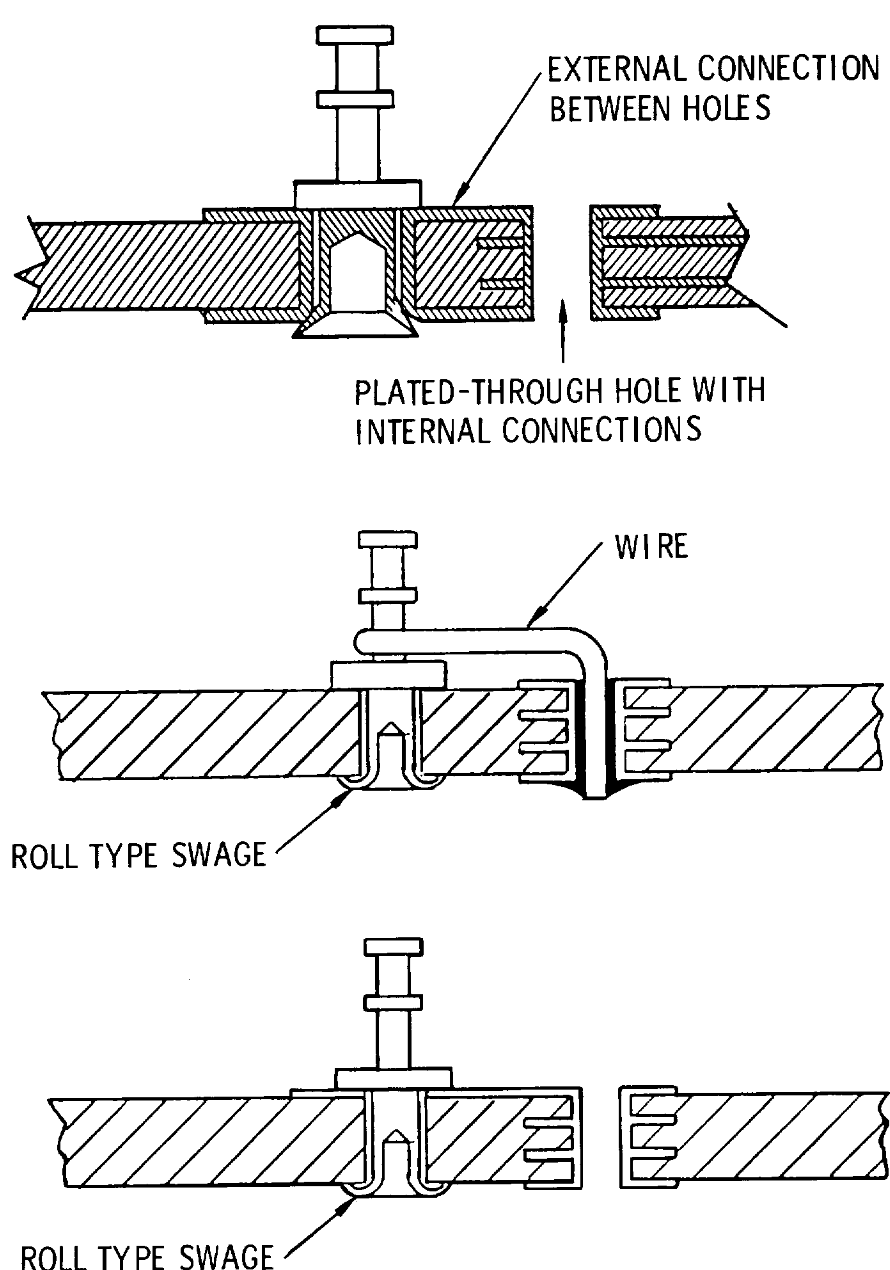

FIGURE B-6
EXTERNAL CONNECTION FOR STANDOFF TERMINAL

F. HIGH VOLTAGE CONSIDERATIONS

1. Operating Voltage Levels

For purposes of this handbook, three voltage ranges have been categorized to help make designs less corona susceptible. These are 0 to 50 volts, 50 to 250 volts, and 250 to 1000 volts. Peak voltages in excess of 1000 volts are not recommended for printed circuit boards.

a. **Zero to 50 volts.** Corona due to gaseous ionization is not likely in air or nitrogen atmospheres between commonly used metallic surfaces in this voltage range. If the following design practices are followed, tracking and metal migration should not occur:

- Select materials and dimensions that can withstand the worst-case voltage gradients around the energized conductors.
- Avoid short air gaps between thinly-insulated or bare conductors.
- Select insulating materials with maximum resistivity and dielectric strength.
- Base all calculations on the instantaneous peak ''abnormal overvoltage'' of the system.
- Select materials with suitable outgassing characteristics.

b. **50 to 250 Volts.** In this range, besides the above stated practices, the following will minimize the probability that corona will occur:

- In AC circuits, avoid an increase in voltage stress between insulators due to use of insulators with large difference in dielectric constant.
- Encapsulate with void-free potting materials well bonded to all surfaces.
- Avoid sharp projections.
- When hermetic sealing is required, pressurize with a suitable dry gas with a high dielectric strength in a thoroughly dry enclosure.
- Dampen inductive switching surges.
- Design for abnormal fault and transient voltages.
- Provide moisture inhibitors on insulating surfaces.

- Arrange conductors so that high and low voltage groups are separated from each other.

- Provide rounded corners on electrical conductors and ground planes next to energized circuits.

- For this voltage range only, use at least .010 inch insulation between rounded electrodes and .050 inch between flat surfaces.

c. **250 to 1000 Volts.** In addition to all of the above, the following apply:

- Design circuit layout to assure that peak voltage differences do not exceed 1000 volts. This sometimes occurs when positive and negative voltage divider strings are immediately adjacent.

- In AC circuits, check adjacent conductors for instantaneous voltage differences between them.

- Provide suitable shielding grids and/or traps to prevent the entry of ionized particles or electrons into the circuitry from the surrounding environment.

- A recommended spacing of conductors on the same side of the printed wiring board is given by the formula d = .12 V in inches where V is kilovolts (.00012 in/volt).

d. The following typical problems can occur in these last two voltage ranges if the above precautions are not observed:

- Corona may be enhanced by gases such as helium, argon, neon, or hydrogen, if they should be mixed with the pressurizing gas in pressurized containers during such operations as leak detection.

- Creepage and tracking can cause increased temperature in localized areas and eventually lead to surface flashover.

- Voltage transients may cause surface flashover to occur. Between 6 and 10 flashovers will form tracking and eventually voltage breakdown.

2. **High Voltage Conformal Coating**

Most printed circuit boards require some insulation, regardless of voltage; this is particularly true for space flight hardware. The circuit board assemblies should be conformally coated with at least three separate layers of a low viscosity insulation. Application may be either by dipping or spraying, with each layer applied at right angles to the preceding layer. The three layers are recommended to eliminate the pin holes (continuous leakage path) and uncoated areas that may occur in single or double coating processes.

All boards, conductors, wiring, and components must be cleaned properly before the unit is conformally coated.

3. **High Voltage Terminations**

Solder terminations on the printed wiring board must be smooth and even with no projections from the component lead or solder spikes.

Standoff terminal and feed-through connections must be solder-balled (see Figure B-7). The radius of the solder ball facing a ground plane should be at least 1/6 of the value of the spacing between the solder ball and ground plane or adjacent high voltage circuit. This low ratio decreases the voltage gradient at the surface of the solder ball and decreases the probability of corona. When large spacings are involved, the solder ball should be at least .125 inch in diameter. Clinch type solder joints offer some advantages over stud type solder joints.

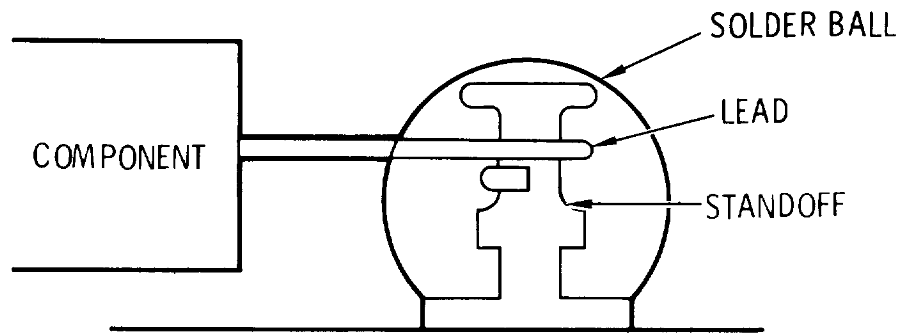

FIGURE B-7a
ACCEPTABLE STANDOFF CONNECTION

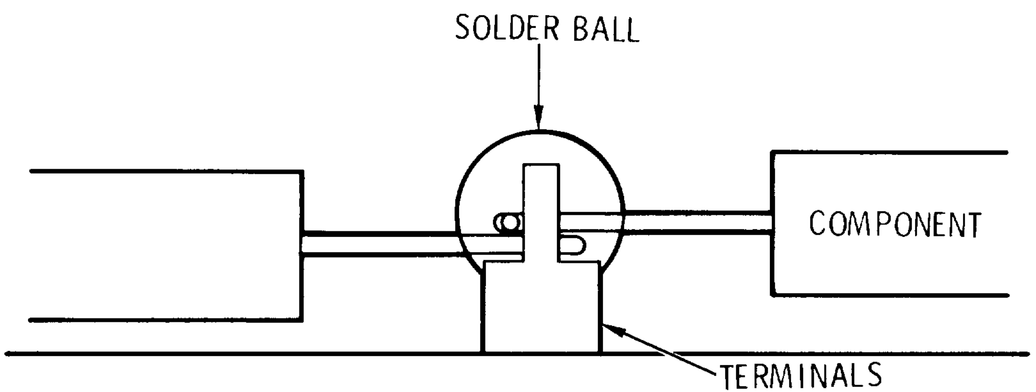

FIGURE B-7b
ACCEPTABLE COMPONENT INTERCONNECTION

G. HEAT SINKS

1. Heat Sink Fabrication

a. **General.** Some electronic parts mounted on printed wiring boards (PWB) require additional cooling to maintain temperatures that will guarantee reliable operation within their rated body temperature extremes. In such cases, heat sinking plates are added to the boards to conduct heat away from the parts. These plates, usually copper or aluminum, may be mounted between the parts and board or may be internal to the board itself.

Heat is transferred to the metal plates and conducted to the edges where, through metal card guides or by direct attachment, it is transferred to the chassis, plenum chamber, or housing. The configuration and material of a heat sink are determined by the amount of heat to be dissipated, the method of attachment to the housing, the need for mechanical rigidity to support the PWB and components, and the cost.

b. **Types**

(1) Surface mounted. Surface mounted heat sinks are made from copper or aluminum sheet. Copper heat sinks are generally nickel plated to a thickness of .0002 to .0008 inch in accordance with QQ-N-290, Class 2. Copper sheet material is available with glass-epoxy or glass-epoxy prepreg laminated to one side for subsequent bonding to the printed wiring board. Aluminum heat sinks are hard-anodized to a thickness of .002 ± .0005 inch in accordance with MIL-A-8625 Type III. A series of holes, slots, or cutouts to clear the lands of the printed wiring board are machined or chem-milled in the heat sink and attachment to the board is made by bonding or riveting.

(2) Metal Core

(a) Metal core heat sinks are used where a high degree of heat transfer is required. Clearance holes for plated-through holes are machined or etched in an aluminum or copper plate and filled with insulating material. The plates are then bonded between copper-clad laminate layers, and a plated-through hole board is produced by conventional processing Access to the metal core is usually through cutouts milled in the PWB layers after lamination. Thickness of the plate should be kept to a minimum, since thermal expansion of the plate places severe stress on the barrels of the plated-through holes.

(b) A special type of metal core heat sinking is the two-sided finned module. Two metal plates with a finned core brazed between them and a printed wiring board bonded on each side provide a controlled temperature platform for the components. Air flow at a controlled rate and temperature assures a constant temperature of the plates. This type of heat sink provides the most efficient method of heat transfer of any of the systems discussed, but it is limited to certain applications because it requires a source of cooled, forced air. Cost of the module is high, and parts must be surface mounted. This method is desirable for airborne equipment where extreme temperature variations are encountered and high density packaging is required.

Materials. Typical heat sink materials are as follows:

- Copper sheet, usually 0.015 inch thick, conforming to QQ-C-576, cold-rolled light or half hard.
- 6061 aluminum alloy sheet, usually 0.015 to 0.030 inch thick, conforming to QQ-A-250/11.
- Metal-clad, laminated plastic sheet GFN-XXXX-C10/0-A-1-A (conforming to MIL-P-13949/4) or GIN-XXXX-C10/0-A-1-A (conforming to MIL-P-13949/10).
- Copper-clad, thermosetting, epoxy-preimpregnated glass fabric.
- No-flow acrylic or epoxy preimpregnated glass cloth.

d. **Assembly.** Heat sinks are normally bonded to the printed wiring board with a no-flow epoxy-glass or acrylic-glass prepreg, or liquid adhesive which provides both the bonding adhesive and the electrical insulation. In the case of copper-clad prepreg, both the copper and the prepreg are normally machined to the heat sink configuration simultaneously. With bare copper or aluminum, this is done separately. Copper clad laminate with no-flow prepreg may be used when more dielectric spacing is required. In the case of aluminum heat sinks, hard anodizing, although providing electrical insulation, may not be sufficient to assure complete electrical isolation when heat sinks are bonded over conductors.

Two-sided finned cooling modules are custom brazed or bonded assemblies. Construction methods and materials are generally unique to each design.

2. Design Guidelines

a. **Thermal Analysis.** Heat sinks are usually designed as an integral part of the PWB. After the circuit engineer has calculated the power dissipation of each part in the circuit and the designer has established a preliminary layout of the parts, a thermal analyst is consulted. If the heat sink plate has been preselected, thermal analysis will determine if the plate material and thickness are adequate to cool the parts. However, preselecting a heat sink sometimes leads to overdesign. A more efficient method of analysis, if available, is to use a computer program to generate a thermal map of the part layout. When this is optimized to spread the heat uniformly over the entire heat sink, packaging engineers can establish the final arrangement of parts and determine the type of material and thickness of the heat sink.

b. **General Design Rules**

- Minimum clearance around lands should be selected based on operating voltages, or 0.020 inch, whichever is greater.
- Do not design in "T" configuration. Unsupported legs may curl up during bonding.
- Eliminate sharp corners by forming a minimum radius of 0.05 inch.
- Provide a continuous frame at the periphery of the heat sink; this maintains the mechanical rigidity of the heat sink and minimizes warpage.
- Shape cutouts and slots to allow space for markings.
- Chem-milled heat sinks should not exceed 0.050 inch in thickness.
- For chem-milled heat sinks, allow 1 mil/mil thickness for undercut when calculating hole, slot, and cutout size tolerances.
- Remove the least amount of material possible when designing holes, slots, and cutouts.
- Minimum material thickness between holes, slots, and cutouts should be .100 inch (2.54 mm).
- Markings should be 0.020 inch minimum from the edge of holes, slots, and cutouts.

- Include four tooling or rivet holes for alignment of heat sink with PWB.

- Center all holes, slots, and cutouts on 0.100 grid intersections (4X scale) for digitizing.

General Design Factors

- Minimize the number of interfaces between the parts and the chassis. A well planned heat sink system provides for efficient heat transfer, thereby reducing the size, weight, and cost of the heat sink.

- Select materials and finishes carefully to minimize differences in temperature coefficients at the interfaces.

- Determine the cost of different methods of manufacture; in some cases, chemical milling is one third as expensive as machining. Also, machine drawings must be completely dimensioned, resulting in a very complex drawing that requires expensive quality control (QC) procedures.

- The preferred method for preparing master patterns for chemically milled or etched heat sinks is to lay out on a gridded Mylar® sheet at 4X, digitize, and plot.

- Partial heat sinks may be sufficient if the heat is concentrated in one area of the board.

H. PRINTED WIRING BOARD MARKINGS

1. General

a. Printed wiring board markings are placed on boards for a number of reasons. The principal ones are as follows:

(1) To identify the board by part number and, when required, provide a serial number for traceability.

(2) To provide part location, orientation, and identification information.

(3) To identify the board manufacturer.

(4) To identify the next assembly number.

(5) To identify layers on a multilayer board.

b. There are a number of methods for applying markings. Silk screening is the preferred method, particularly on multilayer boards with no circuitry on the outer layers. Printing and etching of marks delineated in the artwork is the most commonly used alternative. Rubber stamping or etching with an electrical pencil (on a copper pad provided for this purpose) is permitted; however, this is less commonly used except for serial numbers or, in the case of rubber stamping, for the rework of illegible or wrong markings.

2. Design Considerations

In the design and location of markings for PWB's,the following must be considered:

a. Etching may reduce the width of fine lines. To assure a properly bonded letter or number on the etched board, the character height should be at least 0.06 inch with a line width of at least .008 inch after etch. If this minimum size cannot be maintained, an alternate method such as silk screening should be used.

b. Etched numbers or letters may cause shorts or reduce the spacing between conductors beyond the acceptable minimum. Designers must allow for this when calculating conductor spacing.

c. For silk screening or rubber stamping, an electrically nonconductive epoxy ink of contrasting color, conforming to MIL-I-43553, must be used. Wherever possible, markings should not be located on conductors or bridge between conductor and base laminate. In no event should markings be located on lands which must subsequently be soldered.

CAUTION!

Ink should not be used on hardware with outgassing requirements unless markings are covered with an approved material with respect to outgassing.

3. **Part Identification**

Part identification typically establishes the identification, location and, when appropriate, directional mounting requirements of each part. It is primarily done to provide an assembly aid for manual part placement and may also act as an inspection guide. Serialization is added when required. Lands for serial numbers should be in the same location for all boards of the same size and program. Part reference designators are shown where space permits. Polarization or directional mounting requirements must be shown by marking or etching, or be clearly depicted on the assembly drawing if part assembly identification is not used.

4. **Printed Wiring Board Identification**

The part number marking for the printed wiring board should be placed within the finished board outline; preferably, it should not be evident when the part assembly part number is viewed.

5. **Board Traceability Markings**

NHB 5300.4(3I) specifies that each board and each set of quality conformance test coupons must be marked with the manufacturing date and Federal Supply Code for Manufacturers (FSCM) code number. For traceability, the quality control test coupons must be identified with the corresponding production boards. The marking must be produced by one of the methods identified in H-1. Provisions for these markings must be made when the board is designed. Preferably, the markings should be associated with the board part number.

I. SPECIAL DESIGN CONSIDERATIONS

1. **Fine-Line Printed Wiring Boards**

   a. **General.** Fine-line PWB's are used in some specialized applications. In general, they are defined as boards with line width and spacing requirements which are close to or less than the allowable minimums. Some common applications are:

      - Conversion of a multilayer PWB to a two-sided PWB for decreased cost.

      - High-density interconnect systems for large scale integrated devices (LSI) using leadless chip carriers with terminal spacings on 0.040- or 0.050-inch centers.

- Reduced line widths and spacings present increasing manufacturing difficulties as they decrease from 0.010 inch to 0.004 inch. The quantity production of fine-line boards became practical only after laminates with copper cladding thinner than 1 oz/ft^2 became available, and improvements in resolution capability of photoresists and exposure devices were realized.

b. **Minimum Width and Thickness.** The width and thickness of fine-line conductors is determined on the basis of required current-carrying capacity. For manufacturing purposes, it is more desirable to place fine-line conductors on internal layers. Here conductor thickness is established by the thickness of the cladding, and etching can be controlled closely by the use of thin (0.0007 inch), high resolution photoresists. When it is necessary to place fine-line conductors on outer layers, the final thickness is the sum of the thickness of the copper cladding (which should be as thin as possible for etching control) and of the plated copper. The thickness of the plated copper is normally limited to approximately 0.002 inch, the maximum thickness of photoresist which can be used for 0.004-inch line resolution. A practical minimum width, from a manufacturing standpoint, is 0.004 inch (.10 mm).

c. **Minimum Spacing.** Published values in MIL-STD-275 and Table 6-1 of this standard are conservative, but no definitive data is available to indicate the extent to which they can be extended. Where design requirements indicate that higher voltages will be imposed, specific testing may be required to evaluate the minimum spacing allowable.

d. **Materials.** Thin copper foil of 1/8-, 1/4-, 3/8-, 1/2-, and 3/4–ounce/ft^2 (normal thickness of 0.00020, 0.00036, 0.00052, 0.0007 and 0.0010 inch) may be used for fine-line boards. The thinner the copper foil used, the more closely the conductor width will correspond to the artwork. Use of the thinner copper may require that the minimum surface copper-plating thickness be specified on the master drawing. For example, if 1/4-ounce foil is required on the master drawing, and a minimum conductor thickness of 0.0018 inch is required for current carrying capacity, a note should be added to the master drawing requiring a minimum copper-plating thickness on the conductor of 0.0015 inch. The copper plating thickness in the plated-through holes would remain as specified in NHB 5300.4(3I) because the conductive area of the plated-through-hole wall is several times greater than the conductors.

e. **Design and Drafting Requirements.** The general design information, basic design considerations, conductor requirements (except thickness, width, and spacing), and information on terminal areas and holes, component mounting and layout, heat sinks, and markings of the previous chapters are applicable.

2. Leadless Chip Carriers

The leadless chip carrier (LCC), sometimes also referred to as the hermetic chip carrier (HCC), is a rectangular device containing the electronic portion of a hermetic dual-inline package (DIP) with leads and excess package material discarded. It has contacts on all four sides, suitable for direct attachment by reflow soldering. Attachment may also be made with sockets, or by add-on leads, attached during the soldering process. When compared to conventional DIP's, LCC's seem to offer significant reductions in package volume and weight and an improvement in high-frequency and high-speed switching performance.

At the present time, a primary difficulty in attaching LCC's to conventional printed wiring board substrates is the thermal expansion mismatch between ceramic LCC's and the substrate, which will result in fractured solder joints if the assembly is subjected to thermal shock, thermal cycling, or high operating temperatures. This factor, coupled with the rapidly changing availability status of functional parts as the changeovers are made from leaded to leadless parts, makes it difficult to present useful design information that will still be current in the reasonably near future. The most current design information available is contained in the IPC publication, IPC-CM-78, "Guidelines for Surface Mounting and Interconnecting Chip Carriers," and monthly technical publications devoted to the design of printed wiring assemblies.

END

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