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ORGANIZATION OF THE CHANNEL-SWITCHING PROCESS IN PARALLEL COMPUTER SYSTEMS BASED ON A MATRIX OPTICAL SWITCH

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ORGANIZATION OF THE CHANNEL-SWITCHING PROCESS IN PARALLEL COMPUTER SYSTEMS BASED ON A MATRIX OPTICAL SWITCH

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Given the development of high-speed computer systems, /16* switching communications channels is now an urgent problem. The following factors are the cause: the increasing speed of computers, which imposes additional requirements on switching devices within individual computers; extensive use of multiprocessor computers, which makes it necessary to consider relationships among processors and between processors and peripherals; the appearance of computer systems constituting a single computer net, which creates additional complicated switching problems; undercapacity of modern electronic switches for I/O operations, data exchange, and data movement in a system in view of the sequential nature of these operations; active development of optoelectronic computers, which can process information in pages; and rapid development of fiber-optic communications systems. These factors have made it necessary to develop matrix optical switches (MOS), which show great promise for use in computers and communications.

Parallel computer systems, including multiprocessor computers distinguished by high flexibility, speed, reliability, and longevity, are now of particular interest [1]. The typical form of communication between processor modules (PMs) and on-line memory modules (OMMs) in homogeneous and heterogeneous multiprocessor systems is cross communication, accomplished by a centralized matrix switch which is also used to connect peripherals. Cross communication circuitry is universal in the structure of communications within multiprocessor systems. Switching is usually

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accomplished at each point on the matrix circuit, which thereby ensures physical connection of any memory module to any processor. Despite the fact that several information transfer methods can be set up simultaneously in a matrix, there is still a constant need to resolve conflicts which arise when connections are made in systems. Finally, existing internal communication switches have one other important weak point: if the number of PMs and OMMs matches the number of switch outlets (maximum makeup), it is virtually impossible to add more of these modules to the system without structural changes.

Figure 1 illustrates the structure of a system with cross communication. Each matrix point represents a gate circuit. Therefore, the set of time delays for crossover gate components is to a great extent limited by gate module switching speed [2].
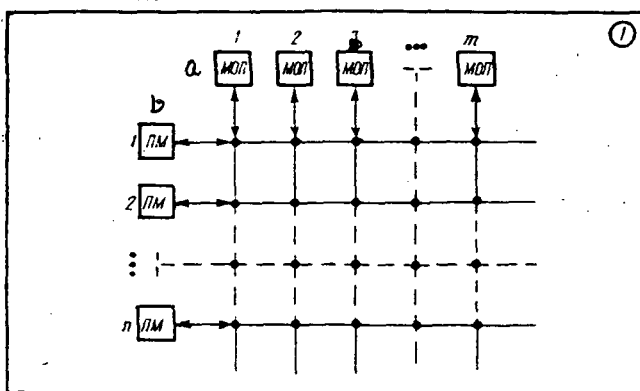

Fig. 1. Diagram of intrasystem crossover communications.
Key: a - OMM; b - PM.

References [1,3] classify gate circuits by analyzing equipment-level inter-processor information exchange communications, which facilitate connection of each processor to any other processor in gate circuits and nets. The star-shaped structure corresponds to indirect transfer along different routes if control is centralized. During transfer, messages pass through a central switch (S). This structure is usually implemented with a matrix switch.

A multiprocessor system with common memory is the most
frequent type of communication in gate circuits; in it, more
than two processors are connected to common memory. Note that
the structure is highly modular, so that the cost per module
may be good if not all processors are equipped with their own
trunk for exchange with memory, and communication is
accomplished through a switching device directly connected to
memory [3].

The structures selected are primarily modular. Systems
with these structures offer greater opportunities for
increasing capacity, since almost unlimited expansion is
possible. However, system capabilities are now limited because
of the complexities of switching processor modules. Therefore,
it is quite important to solve the problem of developing a high-
capacity switching system.

Structures for communication between the central portion of
gate circuits and I/O channels can be classified as follows
[1]: channel-central processor; channel-mainframe memory;
channel-system controller. The last structure provides for a
central switching point: all data transfers to and from
peripherals, central processor, and mainframe memory are
accomplished under the control of the system controller. This
controller is the logical connecting link between the mainframe /17
memory and the central processor and regulates information flow
in the system. The major advantage of the channel-system
controller structure is logical coordination of all system
actions.

Networks of tracks which join the central portion of a gate
circuit to peripherals are of one basic type [1]; they have I/O
controllers (IOCs) as their main functional unit. These
controllers can be combined with a central processor, employed
as stand-alones, and combined with peripherals. There are
three main types of channel connection and selection to

accomplish I/O. The first is based on permanent individual
connection of each device to another device; the second, on
connection of a limited group of channels to accomplish
specific input or output; the third, on a universal method of
connecting channel equipment ("floating" channel or matrix).
Universal channel connection ensures full use of all gate
circuit channels, but this requires a well-organized switching
system.

A great deal of attention is now being given to gate
circuits with combined and variable structure. The advantage
of these systems is that they can ensure a gain in speed
possible only with specialized computers and, at the same time,
because their configurations can undergo dynamic change, they
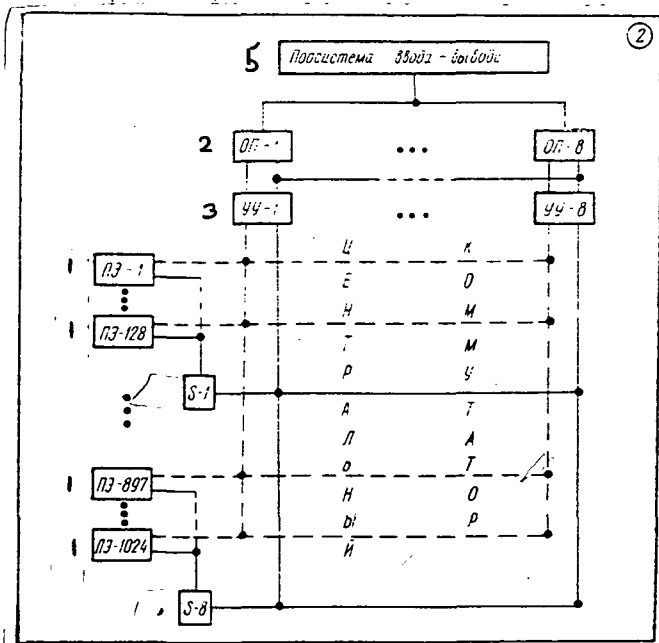have a margin of adaptability unattainable by specialized
machines.

Fig. 2. Block diagram
of a MAP system.
Key: 1 - Processor
component; 2 - System
on-line memory module; 3
- Control; 4 - Processor
component sector switch;
5 - I/O subsystem.

A large MAP system combining the properties of ensembles and matrix and associative systems is of particular interest as one example of a machine with combined structure [1]. In a system organized in this way (fig. 2), processor components are distributable resources which, in combination with several controls, permit simultaneous transfer of commands and data from any controller to any set of processor components and transfer of data from any processor component to any other processor component connected past a certain controller. There are a total of 8 x 1,024 command bus switchings.

Reference [4] proposes a system with dynamic architecture in which units (components) and internal communications between them are reconfigured. Depending on the type of problem to be solved, the set of processor components can be broken down into separate dynamic groups, in each of which a different number of processor components can be formed and the required configuration of connections between them established. Variable-structure computers are organized on a principle by which a machine's structure should match the natural structure of the algorithm being executed, in contrast to ordinary computers with a storable program, where the form of the algorithm realized as a program matches the computer's rigid structure.

Reference [5] proposes a structure for a variable-configuration switching computer. Reconfiguration is done by establishing direct connections between outlets of some operating devices and inlets of others in accordance with the structure of the entire algorithm or part of it (with the structure of the information flow model). The switch in this case is the central portion of the computer (fig. 3).
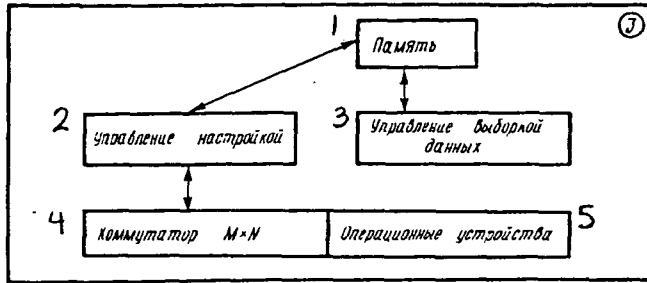
Fig. 3. Block diagram /18 of a switching computer. Key: 1 - Memory; 2 - Setting control; 3 - Data selection control; 4 - MxN switch; 5 - Operating devices.

Because of the rapid development of large integrated circuit technology, there is a marked tendency to structure gate circuits on the basis of microprocessors. The result is inexpensive computing capabilities and, if there is a large number of identical processors, high reliability. These systems are highly modular, which facilitates their expansion by modules, simplifies maintenance, and increases production. Reference [1] discusses a matrix system with reconfiguration and variable structure. Microprocessors are connected to the net's vertex; modules and I/O devices, to its roots (base nodes). Each bus may contain, for example, 8 data lines, 16 addressing lines, 4 control lines, and 3 monitoring-diagnostic lines. Data and addressing lines are used to form communications between processors and memory modules. Processors are interconnected by net vertices. These processors are microprocessors which can be expanded in byte increments. Exchange with memory and I/O devices is accomplished in bytes. System memory in the form of modules has page logic, control of which is allocated in terms of individual pages. This facilitates changing the system's structure and configuration.

Thus, in systems with a large number of processors which can be restructured, structure efficiency and economy greatly depend on the characteristics of the switch; this switch governs the possibility of effective interaction between processors and ensures restructuring of the system depending on

a change in its load.

Classification and Analysis of Electronic and Optoelectronic Switching Devices. Depending on design, switches are classified as machine and circuit, contact and solid state. Machine devices take the form of a structurally unified assembly; circuit devices consist of standard assemblies.

Multichannel control system circuits and combined computers most often use circuit switches (electronic switches with semiconductor components). As a rule they are made up of diode and triode keys. However, the resistance of a closed key is much lower than that of open relay contacts. Therefore, there are problems when a switch is constructed for a large number of switchable channels: as the number of channels increases, the input resistance of the switch diminishes and the lower minimum signal level rises because residual currents at the open switch channel resistor are added together. The channels' reciprocal effect may be diminished by separating the key circuits' control circuits. However, the complexity of the switch and the number of cells at each switchable channel increase. Control circuits of these switches are usually made up of pulse transformers, tunnel diodes, etc. Switches can be constructed from diode matrices.

The following factors are taken into account when electronic switches are being constructed: residual voltage (5 mV), contact resistance (500 Ohm), insulation resistance to the casing (1 milliohm), residual filament current (20 microamperes), time to switch one channel (300 microseconds).

Switches can be structured using crossbar switches (CBS) [7], which are electromechanical switching devices. Their operating principle is based on cross connection of vertical

and horizontal buses. A crossbar switch is controlled by selecting and locking electromagnets acting on specific armatures mechanically connected to a bar which controls corresponding contact groups. Electromagnets which select and lock by means of bars form a coordinate system, and the contacts of the switching portion of the CBS constitute a contact bank. Contact status is maintained during relay magnetization. Note that the operating reliability of the CBS is commensurate with that of the electromagnetic relays and that detecting malfunctions in CBS and restoring them to operation if they fail are extremely complicated.

Integrated optoelectronic switches (OES) have now become common [8]. Galvanic discharge is an important OES feature, since it permits creation of a switching field of spatially separated circuits and signal sources. New optoelectronic instruments (optrons) make it possible to solve this problem (discharge) microelectronically. However, OES have considerable deficiencies: limited response speed and current gain (the ratio of maximum switchable current to control current) in the light-emitter/light-receiver pair; residual voltage on an open key; leakage current from a closed key; significant spread of optoelectronic key parameters from model to model and high temperature dependence of parameters; and /19 compatibility of all optoelectronic keys with integrated logic circuit series in speed and in response time. These disadvantages necessitate use of additional electronic stages in switches.

In terms of production process, the OES is a hybrid integrated circuit, although in terms of function some of them are classified as universal semiconductor devices (photothyristor, phototransistor, and photodiode optrons). Use of hybrid process is necessary because of the use of various semiconductor materials for the light-emitter, because of

nonplanar optron structure, and because of the optical isolation between channels in multichannel integrated switches. Isolation is achieved by spatial separation of channels, i.e. use of a separate substrate for each.

To these difficulties is added the complexity of isolating elements in the circuit. Preventing electrical communication between channels in multichannel switches requires a near-zero current gain between injecting and isolating (p-n)-junctions, which is not a simple design task.

It has now been proven that all existing components for switches need improved speed, output, and integration characteristics [9]. A primary factor in the evolution of computer networks is introduction of optical cables which make it possible to transfer large files of information at high speeds.

Optical communications will be used in computers of the future [10]. Replacement of traditional computer interfaces with optical cable systems is a result of the following factors: low information transfer bandwidth and transmission length; complex computer design and maintenance; high size and weight; low reliability and noise immunity; and high cost. Unfortunately, however, use of optical cables solves only transmission problems; switching problems remain. Optical switches of the future may be the central node of communication channels between computers.

Principles of Constructing a Matrix Optical Switch and Its Structure. Rapid switching, when the time taken to establish a connection should be equal to or a little less than the time taken by machine operation, is of great importance in microprocessor systems. Many switches used in this field of communications are unacceptable for these speeds, since

equipment becomes considerably more complex or because it is theoretically impossible to construct a control algorithm which performs a job in a given time [11]. The data processing system's macrostructure must be restructured (especially in complicated systems), and this requires simultaneous switching of a large number of communication channels.

It has been proposed that switching circuits be classified in terms of control characters [11] to determine a switch's structure. If any switching circuit outlet is accessible to any inlet, it is called fully accessible; if not, non-fully accessible. Accessibility may vary when connections are set up in switching circuits. If certain ones become inaccessible due to connections already installed, the switching circuit is called a switching circuit with interlocks. If this situation is impossible, the switching circuit is noninterlocking.

Switching circuits in which the inlet is joined to the outlet by one switching point are called single-stage. Circuits in which switching is accomplished over several serially connected points are called multistage.

Depending on whether or not the switching circuit is made together with a control device, these circuits are classified as centralized or decentralized. We can differentiate switching circuits in which control is allocated to a set of elementary switches if the circuit itself is centralized.

Switching circuits in which one inlet can be connected with several outlets are called non-single.

According to this classification, the switching circuit for the proposed device is fully accessible, noninterlocking, multistage, centralized, and non-single. Development of the optical switching method and the switching device was based on

these requirements.

Let us consider the general block diagram of an MOS (fig. 4) consisting of a control module, which coordinates the work of register Rl for incoming addressing communication channels A and register R2 for outgoing addressing channels B, switching channel register R3, the module which calculates initial switching module operating fields, and outgoing channel register P4. Here S_{in} and S_{out} are, respectively, incoming and outgoing information (switchable) channels; T - external control channel.
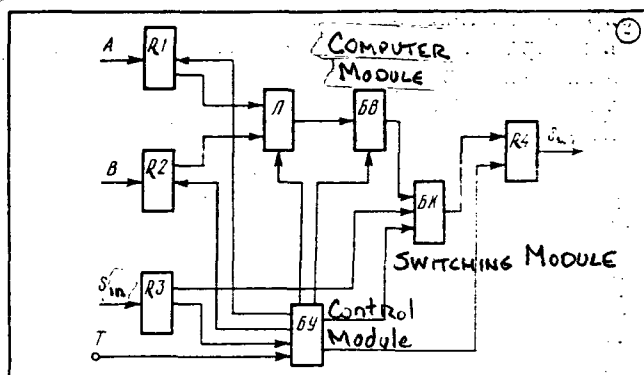
Fig. 4 MOS block diagram.

The switching module is a set of page-switching modules (PSWMs) and page-selection modules (PSEMs). In the first switching module, initial computing module operating fields are used to switch module R3's information channels on the basis of optical control signals from the control module, and the result of this switching operation is sent to module R4. However, when switching is performed, channels may cross. Therefore, the following method has been proposed to eliminate crossovers in this device. If crossovers occur, one of the pair of crossed channels is addressed to the second switching module,

where switching of the remaining channels is repeated. If crossovers again develop, they are eliminated in similar fashion, i.e. half of the crossed channels are transferred to the next switching module. There are no crossovers in the k-th switching module, and the result of switching is sent from this module, as from previous ones, to register R4, where the results of switching all k switching modules are combined.

The required number of consecutively connected PSWM and PSEM modules in each switching module is determined by the dimensions of the initial image matrix, whereby the first switching module will contain the largest number of PSWMs and PSEMs. In subsequent switching modules, the number of PSWMs and PSEMs drops respectively, since the number of crossed switchable image channels drops during the shift from the first to the next modules.

Input signals for the PSWM are matrices (bit planes converted according to a specific law) of switchable communication channel input and output addresses (images). Thus, a system of page switching modules governs (forms) working operating fields which control switching. Each communication channel shifts at their commands. The main output signal of each PSWM is a working operating field.

The input signal of the first PSEM is an incoming switchable signal matrix. Inlets of subsequent PSEMs are operating fields formed in the PSWM and information (switchable) fields. Resulting communication channel bit planes are output from PSEM outputs.

Signals are switched and moved vertically and horizontally to a matrix field of certain dimensions in steps whose size diminishes by binary law. In other words, given a 32x32 matrix, for example, the first step is 16 units up/down,

left/right; then 8, 4, 2, and 1 unit. Alternation of
horizontal and vertical steps decreases the probability that
channels will cross during switching.

We must mention a property of an MOS which sets it above
existing devices. PSWM and PSEM modules arranged vertically
make it possible to perform the required operations in
parallel. Therefore, if initial matrices are large, the total
number of steps is comparatively small.

The essence of operations used in switching modules is as
follows. One PSWM module in the first switching module
performs switching, inhibition, and conjunction. The resulting
working operating fields z_1^p, z_2^p, ... are used in this
same module when information channels are switched.

Information channels are switched one array at a time using
working operators calculated for each array. One PSEM module
in the first switching module performs position-by-position
operations of pair exclusion, inhibition, and conjuntion.

Information "Switching." This operation is performed in
two versions in the device. The first is accomplished only in
the first PSWM and PSEM modules as follows. When the second
working operator z_2^p arrives at the PSWM, the second
initial operator Z_{20} is switched by the first working
operator z_1^p:

$$Z_2^p = Z_{20} \; \overline{|K|} Z_1^p,$$

where $\boxed{K}$ is the symbol for "switching." For the subject
matrices, this operation means that the right half of Z_{20}
becomes the left and vice versa. When the initial information
image Z_{el} is switched by the first working operator in the
PSEM, the lower half shifts upward; the upper, downward. Thus,

switching is accomplished if $z_{el}=z_1^p$. Otherwise it must
be performed for the second modification together with
remaining switchings, which is always accomplished for any
working operating field. Units in this field are the control
signal for the field to be switched by the working operator.
If a unit in a working operator matrix has coordinate ij and
lies in the left (right) part of the matrix, so that switching
must be accomplished along the horizontal, and the point with
these same coordinates has a unit in the matrix to be switched,
then this unit should be moved the required number of units to
the right (left) part of the matrix. Switching along the
vertical proceeds in similar fashion. Units for which there are <u>/21</u>
no controlling signals in the working operator change their
positions.

"Pair Exclusion Operation." This operation eliminates
information channel crossovers, which occur when the next
switching operation is performed, by shifting the crossed
channels to the next switching module. Two matrices are
crossed to do this. Results of this crossover determine the
channels to be switched and points to which the channels must
be moved. If these addresses are occupied by channels which
are not to be switched in this cycle, they are formed into a
matrix which is sent to the next module for switching. The
term "pair exclusion" defines the essence of the process of
eliminating channels using pairs of controlling working
operating signals. Combination, inhibition, and conjunction
operations used in the device are performed in accordance with
the definitions of these operations.

Thus, as the MOS operating cycle ends, i.e. after all
switching channels in the device have been formed, any
switchable image must be transferred until new addressing
images A_1 and B_1 arrive, after which new switching channels
are formed in the device.

Optical Communication Channel Switching Method. Let us give a brief mathematical proof of the optical switching method used in the proposed device. Since the switch employs the page method of information processing, i.e. binary arrays represented as a matrix of a certain dimension undergo certain operations, these operations are completed on each matrix cell. This statement can be written as follows:

$$A_{IJ}\sigma B_{IJ} = \begin{vmatrix} a_{11}\sigma b_{11}, & a_{12}\sigma b_{12}, & \dots, a_{1M}\sigma b_{1M} \\ a_{21}\sigma b_{21}, & a_{22}\sigma b_{22}, & \dots, a_{2M}\sigma b_{2M} \\ \cdot & \cdot & \cdot \cdot \cdot \cdot \cdot \cdot \cdot \cdot \\ a_{N1}\sigma b_{N1}, & a_{N2}\sigma b_{N2}, & \dots, a_{NM}\sigma b_{NM} \end{vmatrix},$$

where $\sigma \in \Gamma$; $\Gamma = \{\neg, V, \wedge, \equiv, \subset, \dots, \uparrow\}$ is the set of operations; σ, the logic operator of set Γ. Switching operations may be directly interpreted as shift operations; the matrix shift operation, as $\overrightarrow{A_{\alpha\beta}} = \overleftrightarrow{A_{IJ}}(K, L)$,
where the symbol $\leftrightarrows$ denotes the shift operation; K, L, steps in the displacement per line and column respectively; $\alpha = I+K$, $\beta = J+L$, $I=1,2,\dots,N$; $J=1,2,\dots,M$; $K=\pm 2^k$; $L=\pm 2^l$; $k=n-1$; $l=m-j$; $n=\log_2 N$, $m=\log_2 M$; $i=0,1,2,\dots,n$; $j=0,1,2,\dots,m$. The following conditions must be met: $1 \leqslant \alpha \leqslant N$, $1 \leqslant \beta \leqslant M$. Then each cell in the new matrix will be defined as follows:

1) If

$$a_{\alpha\beta} = \begin{cases} a_{IJ} \text{ at } N \geqslant \alpha \geqslant 1 + 2^k, & M \geqslant \beta \geqslant 1 + 2^l, \\ - \text{ is not determined if } \alpha > N, \ \beta > M; \end{cases}$$

$$a_{\alpha\beta} = \begin{cases} a_{IJ} \text{ at } N \geqslant \alpha \geqslant 1 + 2^k, & M \geqslant \beta \geqslant 1 + 2^l, \\ 0 \text{ is not determined if } \alpha < 1 + 2^k, \ \beta < 1 + 2^l; \end{cases}$$

2) 2) If $K = -2^k$, $L = -2^l$

$$a_{\alpha\beta} = \begin{cases} a_{IJ} \text{ at } 1 \leqslant \alpha \leqslant N - 2^k, & 1 \leqslant \beta < M - 2^l, \\ \text{ is not determined if } \alpha < 1, \ \beta < 1; \end{cases}$$

$$a_{\alpha\beta} = \begin{cases} a_{IJ} \text{ at } 1 \leqslant \alpha \leqslant N - 2^k, & 1 \leqslant \beta \leqslant M - 2^l; \\ 0 \text{ is not determined if } \alpha > N - 2^k, \ \beta > M - 2^l. \end{cases}$$

Then the parallel switching process may be expressed according to matrix operations:

$$(A_{IJ})_{\gamma+1} = (A_{\alpha\beta} \wedge Z_{\alpha\beta})_\gamma \vee (A_{IJ} \wedge Z_{IJ})_\gamma \vee \qquad (1)$$
$$\vee (A_{\alpha\beta} \wedge Z_{\alpha\beta})'_\gamma,$$

where $\gamma = 0, 1, 2, \ldots, n+m$; $(Z_{\alpha\beta})_\gamma$, $(Z_{IJ})_\gamma$, $(Z_{\alpha\beta})_\gamma$, are operator matrices; $(A_{\alpha\beta})'$, $(Z_{\alpha\beta})'$ are matrices $(A_{\alpha\beta})$, $(Z_{\alpha\beta})$ if $K = -2^k$, $L = -2^l$. Here the result of switching is matrix $(A_{IJ})_{n+m}$. If the resulting matrix in (1) is obtained, controlling operator method is used, since the channel switching rule obviously may vary for different matrix values.

Initial operator fields Z^0 can be determined by the logical sum

$$Z_\gamma^0 = D_\gamma \oplus E_\gamma, \qquad (2)$$

where D_1, D_2, ..., D , ..., D_{n+m} are input and E_1, E_2, ..., E , ..., E_{n+m} are output addresses of communication channels, represented as binary matrices. However, initial operator fields calculated according to (2) do not take into account switching channels in subsequent positions ($\gamma = 2, 3, \ldots, n+m$). Therefore, they must be transformed as follows:

$$Z_1^{11} = Z_1^0 \wedge Z_1^0,$$
$$Z_2^{11} = Z_1^0 \wedge Z_2^0,$$
$$\cdots \cdots \cdots \qquad (3)$$
$$Z_\gamma^{11} = Z_1^0 \wedge Z_\gamma^0.$$

To determine working operating fields, one must conduct switching operations on operators calculated according to (3). Then

$$Z_1^{p1} = Z_1^{11},$$
$$Z_2^{p1} = [(Z_{\alpha\beta}^{11})_2 \wedge (Z_{\alpha\beta}^{p1})_1] \vee [(Z_{IJ}^{11})_2 \wedge (Z_{IJ}^{p1})] \vee$$

$$\bigvee \left[(Z_{\alpha\beta}^{11})_2' \wedge (Z_{\alpha\beta}^{p1})_1'\right] = Z_2^{11} \boxed{K} Z_1^{p1},$$

$$Z_3^{p1} = \left[(Z_{\alpha\beta}^{k11}) \wedge (Z_{\alpha\beta}^{p1})_2\right] \vee \left[(Z_{IJ}^{k11}) \wedge (Z_{IJ}^{p1})_2\right] \vee$$

$$\bigvee_1 \left[(Z_{\alpha\beta}^{k11})' \wedge (Z_{\alpha\beta}^{p1})_2'\right] = Z_3^{k11} \boxed{K} Z_2^{p1} =$$

$$= (Z_3^{11} \boxed{K} Z_1^{p1}) \boxed{K} Z_2^{p1},$$

where

$$Z_3^{k11} = (Z_{\alpha\beta}^{11})_3 = \left[(Z_{\alpha\beta}^{11}) \wedge (Z_{\alpha\beta}^{p1})_1\right] \vee \left[(Z_{IJ}^{11})_3 \wedge (Z_{IJ}^{p1})_1\right] \vee$$

$$\bigvee \left[(Z_{\alpha\beta}^{11})_3' \wedge (Z_{\alpha\beta}^{p1})_1'\right] = Z_3^{11} \boxed{K} Z_1^{p1},$$

so that

$$Z_\gamma^{p1} = (((Z_\gamma^{11} \boxed{K} Z_1^{p1}) \boxed{K} Z_2^{p1}) \boxed{K} \ldots) \boxed{K} Z_{\gamma-1}^{p1}.$$

$$(4)$$

Operators for all channels which do not undergo switching at the first position (inverse channels) are calculated in similar fashion:

$$Z_2^{10} = \bar{Z}_1^0 \wedge Z_2^0,$$

$$Z_3^{10} = \bar{Z}_1^0 \wedge Z_3^0,$$

$$\cdots \cdots \cdots$$

$$Z_\gamma^{10} = \bar{Z}_1^0 \wedge Z_\gamma^0.$$

In this case working operator fields are determined as

$$Z_2^{p0} = Z_2^{10},$$

$$Z_3^{p0} = \left[(Z_{\alpha\beta}^{10})_3 \wedge (Z_{\alpha\beta}^{p0})_2\right] \vee \left[(Z_{IJ}^{10})_3 \wedge (Z_{IJ}^{p0})_2\right] \vee$$

$$\vee \left[(Z_{\alpha\beta}^{10})_3' \wedge (Z_{\alpha\beta}^{p0})_2'\right] = Z_3^{10} \boxed{K} Z_2^{p0},$$

$$\cdots \cdots \cdots \cdots \cdots \cdots$$

$$Z_\gamma^{p0} = ((Z_\gamma^{10} \boxed{K} Z_2^{p0}) \boxed{K} \ldots) \boxed{K} Z_{\gamma-1}^{p0}.$$

To avoid loss of information during possible crossovers when operators are calculated and channels switched, crossed signals are stored and then switched according to these rules. Then the equation for crossed signals takes the form

$$(A_{IJ}^0)_{\gamma 1} = \left[(A_{\alpha\beta})_\gamma \wedge (A_{IJ})_\gamma \wedge (\bar{Z}_{\alpha\beta})_\gamma\right] \vee$$

$$\vee \left[(A_{\alpha\beta})_\gamma' \wedge (A_{IJ})_\gamma' \wedge (\bar{Z}_{\alpha\beta})_\gamma'\right].$$

These signals are the basis for determining crossed operators

$$(Z^\delta_{IJ})_{\gamma 1} = (A^\delta_{IJ})_2 \wedge (Z^{k1}_\gamma),$$
$$(Z^\delta_{IJ})_{\gamma 2} = (A^\delta_{IJ})_3 \wedge (Z^{k2}_\gamma),$$

$$\cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot \quad \cdot$$

$$(Z^\delta_{IJ})_{\gamma, \gamma-2} = (A^\delta_{IJ})_{\gamma-1} \wedge (Z^{k,\gamma-2}_\gamma).$$

Thus, at the next step, crossed channels $(A^\delta_{IJ})_\gamma$ are switched by operators $(Z^\delta_{IJ})_{\gamma, \gamma-2}$. The process continues until crossovers are eliminated.

Characteristics of Matrix Optical Switches and the Potential for Their Use. Parallel switching process (1) may be carried out in the optical circuit depicted in fig. 5. MOS modules which execute combination, inhibition, conjunction, and pair exclusion operations should also be based on optical controllable transparencies.
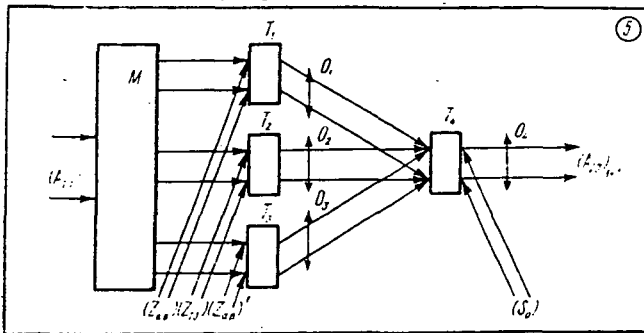

Fig. 5. Optical switching circuit: M - multiplexor: T_1, T_2, T_3, T_4 - optically controllable transparencies; O_1, O_2, O_3, O_4 - objectives (lenses); S_0, uniform light flow.

The primary functional element of this device is an optically controllable transparency (OCT). With this switch, MOS time characteristics and, ultimately, total time to form all switching channels in the device will depend on the total number of OCTs.

Let us determine MOS operating time

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$$T_{MOS}=t_{it}^A+t_{it}^B+t_{it}^{Sout}+t_r+T_c+t_{rem}^{Sout},$$

where t_{it}^A, t_{it}^B, and t_{it}^{Sout} are time to input into the matrix input A, output B, and information (switchable) communication channels S_{in}; t_r, time required to calculate initial operating fields z_i^0; T_c, time required to establish connections; t_{rem}^{Sout}, time to output the output information communication channel matrix S_{out}.

Operations to input addressing and information channel matrices may be performed simultaneously, while MOS operating time may hypothetically be broken down into four basic periods.

In turn, time to establish connections can be considered as a set of three periods: $T_c+T_w+T_s+T_{sw}$, where T_w is the time to calculate working operating fields; T_s, selection (crossover elimination) time; T_{sw}, switching time.

The switching process is completed in one cycle if a control signal from the switching module appears. The length of an elementary period is determined by the time taken to "write-erase" in the OCT, which is 20-50 microsec [12]. Thus, total switching time is low, which completely satisfies response time requirements for optical gate circuits [13]. However, time to set up connections in a switch and the amount of equipment (number of OCTs) are two related figures (this stems directly from the MOS' parallel structure). The relationship between the required number of OCTs and information channel matrix size were evaluated. The results of these calculations served as the basis for plotting a graph of the number of required OCTs, N, as a function of matrix size m (fig. 6). Times to write and read from the OCTs match in all parallel switching modules, and time is determined by only one three-period connection setup cycle T_c.
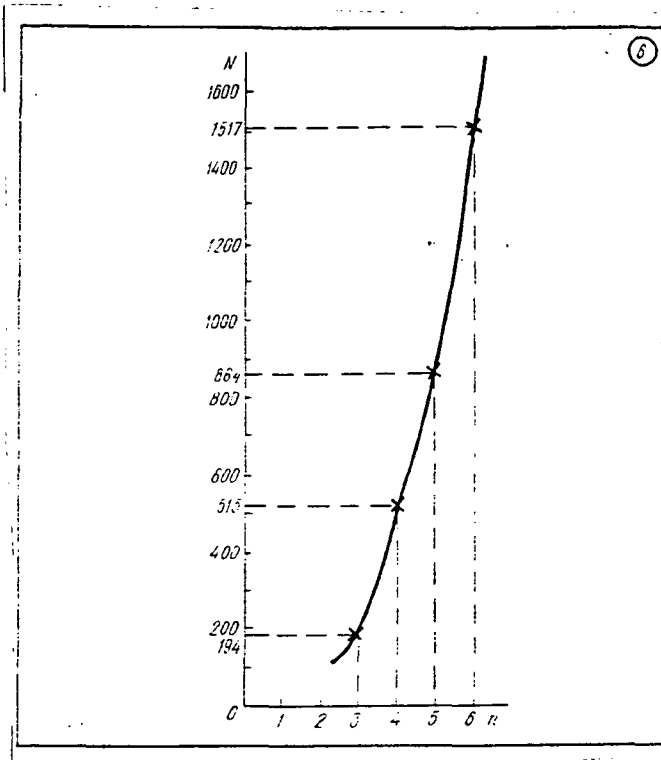
Fig. 6.   N=f(n),
n=log$_2$m.

Given minimum equipment expenditures and lack of strict limitations on time, one might set up other MOS operating modes by simplifying the structure of the entire device without changing the structure of an individual switching module. The channel switching process in this case can be set up in several cycles in the same switching module. Then switching a 64x64-cell binary matrix would require 45 OCTs; a 128x128-bit matrix, 100 OCTs. In terms of time spent, a 128x128-cell matrix can be switched in nine T_c cycles. The number of periods in each cycle will vary. As the number of cycles increases, the number of periods in each cycle decreases. The total number of periods for switching a 128x128-cell matrix is 41.

Organizing the Structure of a Parallel Computer System with a Matrix Optical Switch. Let us consider gate circuit structures created by optical channel switching based on a parallel-operation MOS suitable for traditional electronic gate circuits.

The solution to the problem of switching channels using MOS may be used also to consider the concept of a planar computer [14]. The structure of this system is formed by input and output planes between which lies an array of processor elements. There is a natural "flow" of information through the system. Optical page switching eliminates lost time when this system processes information.

A parallel-operation matrix optical switch is an integral part of optoelectronic computing complexes which are now common. Reference [15] reviews general questions of the structural organization of these complexes. In these complexes, information is processed on a qualitatively higher level: the discrete method of processing digital patterns is used. In particular, extensive capabilities of the controlling operator method, which underlies MOS functioning, are indicated.

Reference [16] proposes principles for constructing an optical processor with variable logic structure; reference [17] discusses ways to realize an optical processor and a possible structure for the device. The proposed optical processor alternative is intended to process information with two-dimensional arrays and is an information-processing method in which pages of information 10^3-10^4 bits in size are parallel-processed, so that the variable operators act on input data arrays. Obviously, the structure of this processor and that of the MOS are quite close, and this device therefore offers the greatest promise for joint use.

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16. Abstract

After a classification and analysis of electronic and optoelectronic switching devices, the paper describes the design principles and structure of a matrix optical switch. The switching and pair-exlcusion operations in this type of switch are examined, and a method for the optical switching of communication channels is elaborated. Finally, attention is given to the structural organization of a parallel computer system with a matrix optical switch.

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