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MODIFIED TIMING MODULE FOR LORAN-C RECEIVER*

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I. ABSTRACT

Hardware documentation is provided for the modified Loran-C timing module, which uses interrupt-driven software control in determining loop sample times. Computer loading is reduced by eliminating polled operation of the timing loop.

II. SUMMARY

The original design for the Ohio University Loran-C receiver featured a software/hardware locked-loop signal processor, based upon the Mostek 50395 timing integrated circuit (IC) [1,2]. This IC provides a six-digit binary-coded decimal (BCD) counter and a BCD register compared to generate an output pulse when the register and counter contents are equal. Operated at 1 MHz, this timing circuit permits microcomputer-selected sample times to be precisely set within a one-second counter interval, with a resolution of one microsecond.

In order to accomplish the data load for the IC register, the computer must detect that the IC digit scan oscillator has selected the appropriate 4-bit BCD digit, and then strobe the new digit data into the register. The IC design requires a scan oscillator frequency of no higher than 20 kHz, which places a lower limit on the time required to load all six digits. In practice, the complete register load requires approximately 500 microseconds (μs).

The original receiver design makes all six IC digit strobe signals available to the microcomputer, which then strobes the new digit data into the register after detecting the presence of the appropriate strobe signal. This operation must take place in order to preset the next loop sample time, triggered by the EQUAL pulse from the Mostek IC. Therefore, the register load must be performed between each Loran-C pulse. The technique of polling the digit strobe lines to detect the next digit to be loaded requires full attention from the microcomputer, delaying background processing.

The modified circuit described in this technical memorandum combines all six-digit strobes into one master strobe signal, which appears as an interrupt to the microcomputer. Therefore, once a digit is loaded into the IC register, the computer is free to process background code while awaiting the next digit strobe interrupt. See figure 1 for a block diagram.

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This modification is required, to permit the single processor (a MOS Technology 6502) to perform all required computations for the entire Loran-C process. Expansion of the receiver from a three-station tracker to full five-station operation would cause over 20 percent of processor power to be lost to the strobe polling operation, causing a reduction in navigation data output rates, and a reduction in the number of pilot-oriented features which could be added using the single processor.

Full hardware documentation is provided in this document for the circuit card implementing the Loran-C timing loop, and the receiver event-mark and re-track functions. This documentation is to be combined with overall receiver drawings to form the as-built record for this device. Computer software to support this module is integrated with the remainder of the receiver software, in the LORPROM program.

III. CIRCUIT DESCRIPTION

Figure 2 shows the complete logic diagram for the Loran-C timing module. To the far left are signal descriptors for the system computer, an MAI SuperJolt based upon the MOS Technology 6502 with 6520 peripheral interface adapter (PIA). All connections, except for CLOCK and IRQ, are made through the 6520 PIA. Figure 3 gives a summary of PIA pin assignments, useful in software design and coding. The Mostek 50395 chip description is given as figure 4, and pinouts are shown in figure 5.

Referring to figure 2, note that seven lines provide data and control signals to the Mostek IC (U3). All these signals are output by the computer as TTL-compatible signals, and must be changed to the 12-volt MOS specification required by U3. This conversion is performed in open-collector drivers U1 and U2, pulled up to 12v through 680-ohm resistors. These lines carry the four data bits for register digits Ra, Rb, Rc and Rd. The LR (Load Register) strobe and $\overline{SET}$ (Set digit counter to most-significant digit) signals.

The timing chip U3 is wired for free-running counter, counting up, and is driven by the CLOCK, which is a buffered version of the main microcomputer clock (a temperature-compensated crystal oscillator). The scan oscillator which generates the digit strobes to indicate the load window for each register digit is set to 20 kHz using the capacitor at pin 21. Digit strobes, one for each register BCD digit, are output by U3 at pins 24 through 29 and are immediately NORed by U6. Note that this 8-input NOR is a CMOS chip running at 12v to eliminate the need for the six voltage dividers used in the previous design to return the MOS levels from U3 to TTL levels. The combined digit strobe is then returned to TTL levels, inverted by U7 and applied as a clock to the U8 D flip-flop latch.

The Q output of the U8 latch is high after receipt of a digit strobe, which causes the output of the U7 interrupt combiner gate to go low, causing an interrupt (IRQ) condition at edge connector pin 19. Once the computer program has serviced this interrupt, the digit strobe interrupt latch U8 is cleared by a low signal at $\overline{CLRD}$, or pin 12. The computer software simply counts interrupts from the digit strobe latch, recognizing that the digit strobes appear in fixed order from digit one through six.

Appropriate signals are then placed on the Ra - Rd lines and the U3 control lines to achieve the full register load.

Once the register is fully loaded, the digit strobe interrupts are disabled by placing a low level on $\overline{CLRD}$, forcing the U8 latch into reset condition. The U5 Loran-C interrupt and data latches are then enabled by bringing $\overline{CLRP}$ high. When the free running counter in U3 reaches the register value just loaded, U3 issues an EQUAL pulse for one clock period (one μs) which clocks the U5 latches. The output of the IRQ combiner gate in U7 goes low since the Q output of the U5 interrupt latch always goes high upon clocking. An interrupt is signaled at $\overline{IRQ}$ to the computer. LDAT, latched by the U5 Loran-C latch, assumes the instantaneous value of the Loran-C digital waveform received at $\overline{LRIN}$ from the receiver front-end module. Note that $\overline{LRIN}$ is processed by U4 to set a pulse width of approximately 70 μs. before it is sampled. This pulse width is necessary to provide a guard time after the leading pulse edge to permit successful pulse tracking, and to minimize initial search time. Since the various front-end processors designed to date have presented various pulse widths, this U4 mono-stable multivibrator has been provided to equalize the waveform before sampling.

The remainder of the circuit, U12, deals with receiver features included for evaluation. The event latch is driven by a front-panel push-button to place on the receiver output tape a unique mark so output data may be correlated with flight events. The retrack latch, also operated by pushbutton, signals the computer that the operator wishes to restart the Loran-C search process. To minimize contact bounce, these latches are configured to operate on the pushbutton release cycle.

Once the computer program has serviced the Loran-C sample interrupt thus generated, the U5 latches are disabled by a low at $\overline{CLRP}$ and the digit strobe interrupt is enabled by a high on $\overline{CLRD}$. Another register load sequence begins.

In this manner, successive samples may be taken of the Loran-C input waveform at times which are precisely controlled by the microcomputer. The programmer may now select algorithms for detecting received Loran-C chains and stations by varying the sample time and observing the result at LDAT.

The module pictorial appears in figure 6, giving placement of ICs and other major components.

IV. REFERENCES

[1] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," paper (No. 81-2329), presented at the AIAA/IEE Fourth Digital Avionics Systems Conference, November 1981.

[2] Lilley, R. W. and D. L. McCall, "A Loran-C Prototype Navigation Receiver for General Aviation," (NASA) Technical Memorandum 80, Avionics Engineering Center, Department of Electrical and Computer Engineering, Ohio University, August 1981.
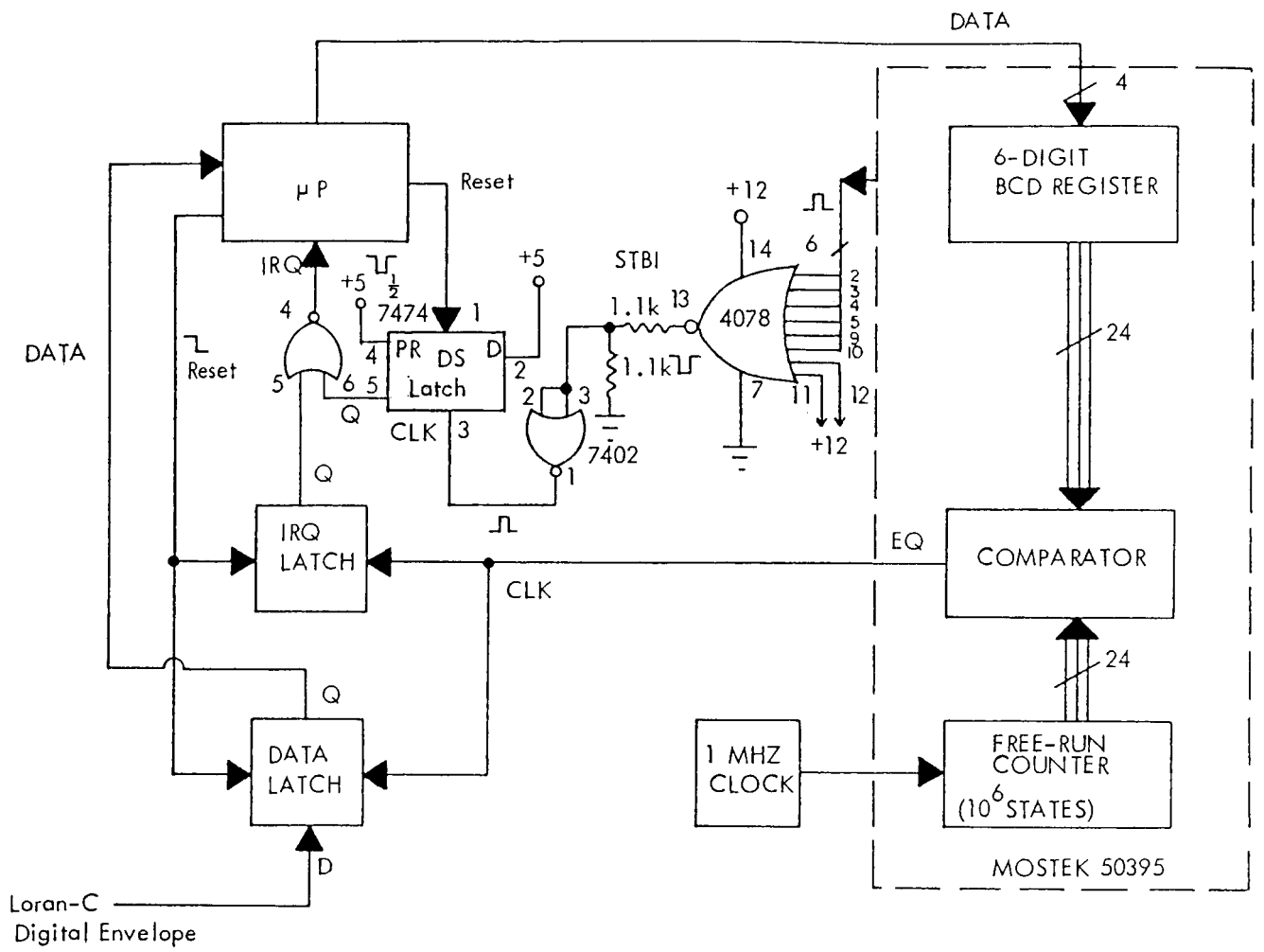
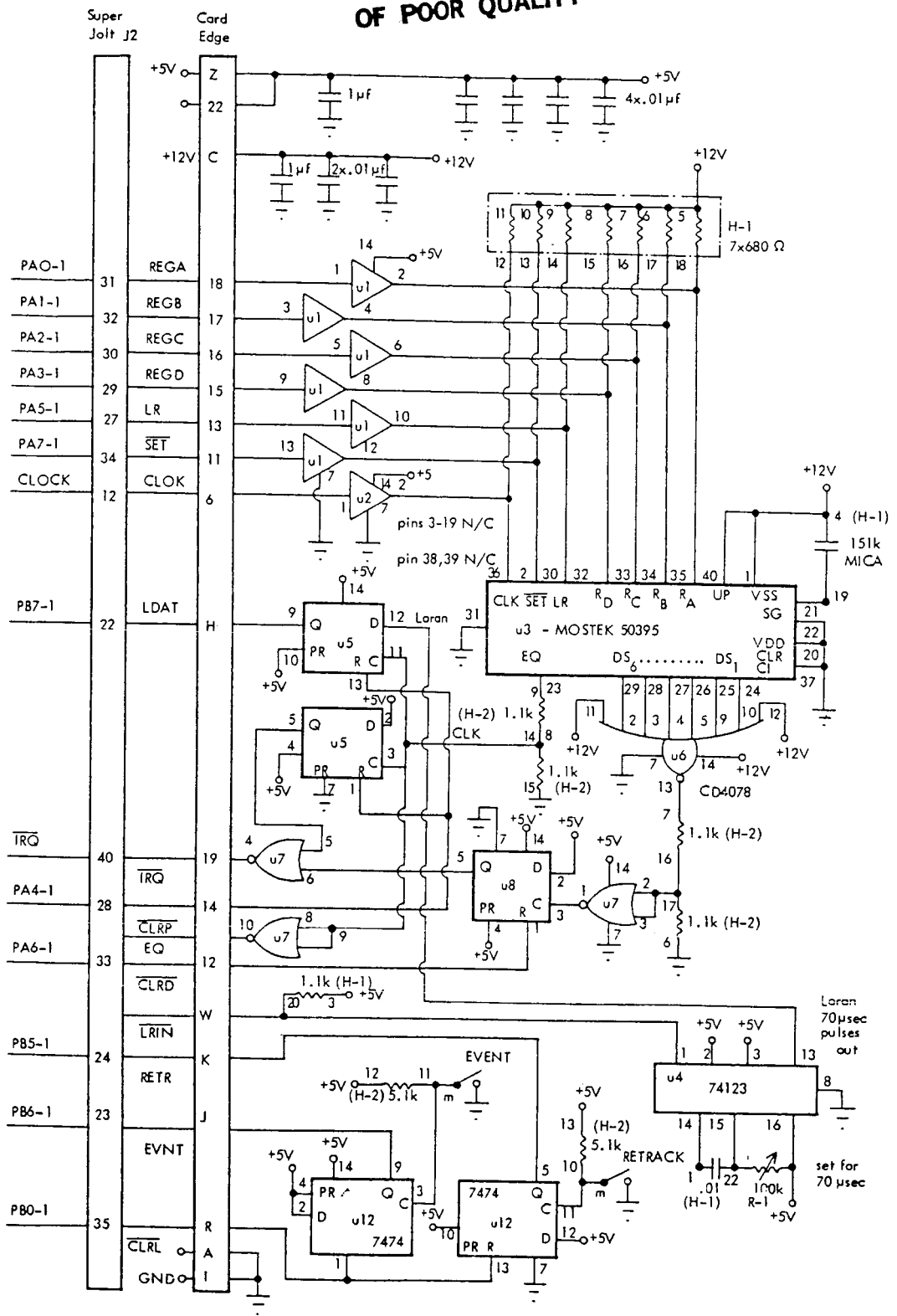Figure 1. Block diagram, Loran-C timing module.

Figure 2. Loran-C timing board for updated RF board only.

o = output
i = input
x = not used

[Loop Data] LDAT

[Event] EVNT
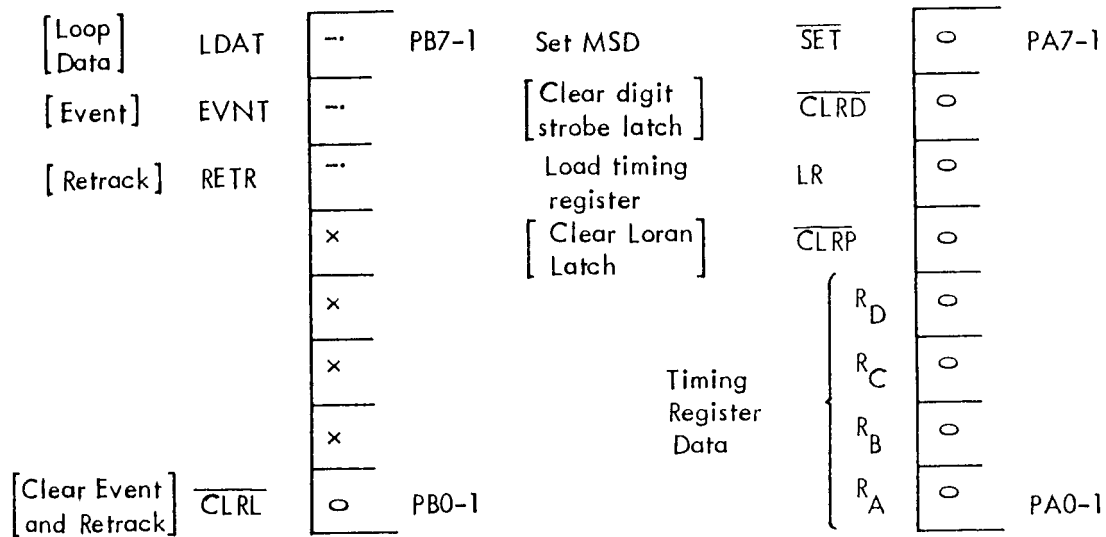
[Retrack] RETR

[Clear Event and Retrack] $\overline{CLRL}$

--·	PB7-1
--·	
--·	
×	
×	
×	
×	
o	PB0-1

Set MSD $\overline{SET}$

[Clear digit strobe latch] $\overline{CLRD}$

Load timing register LR

[Clear Loran Latch] $\overline{CLRP}$

Timing Register Data $\left\{ \begin{array}{l} R_D \\ R_C \\ R_B \\ R_A \end{array} \right.$

o	PA7-1
o	
o	
o	
o	
o	
o	
o	PA0-1

Figure 3. SuperJolt to timing board summary of PIA assignments.

FUNCTIONAL DIAGRAM
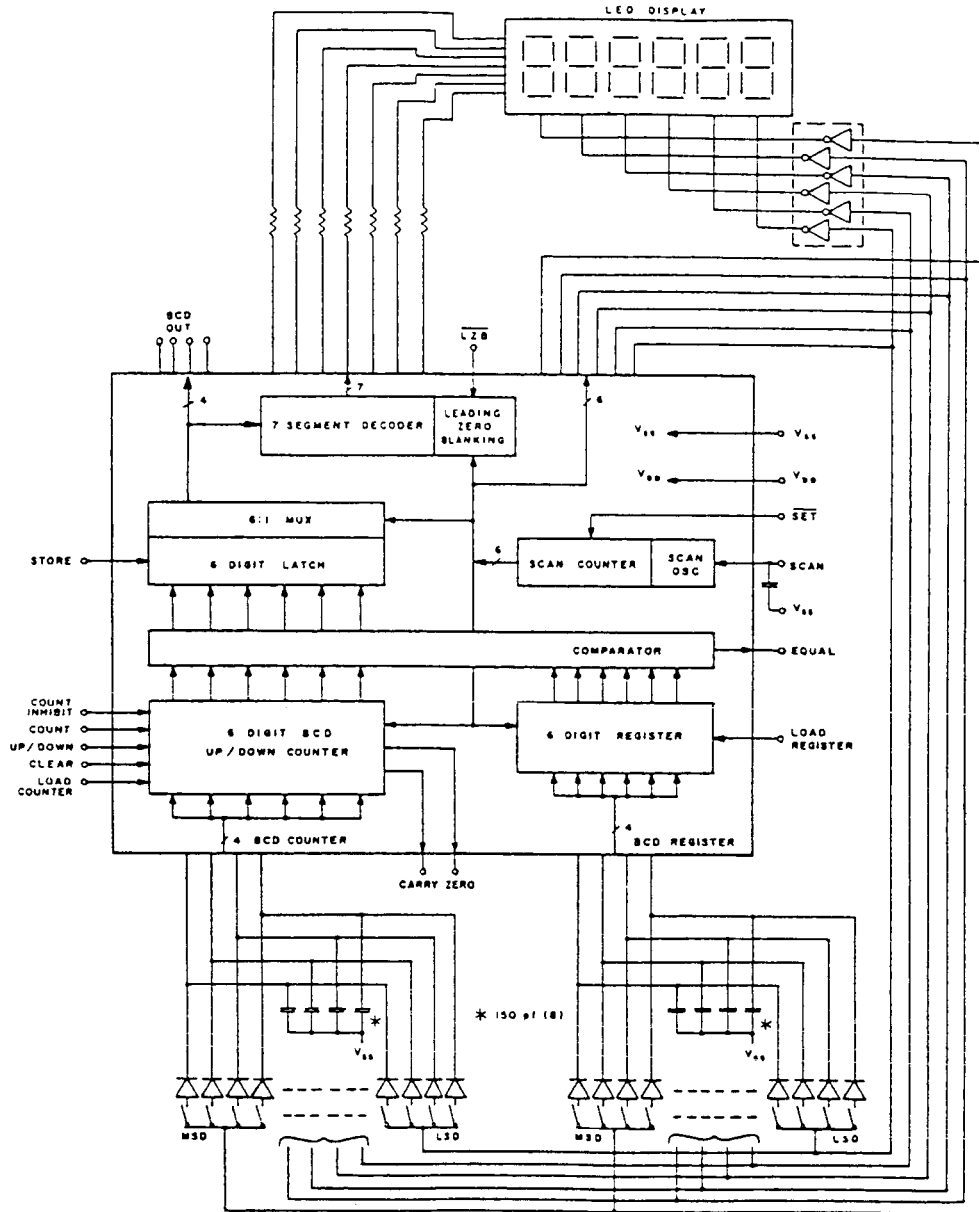
Figure 4.   MOSTEK 50395 integrated circuit.
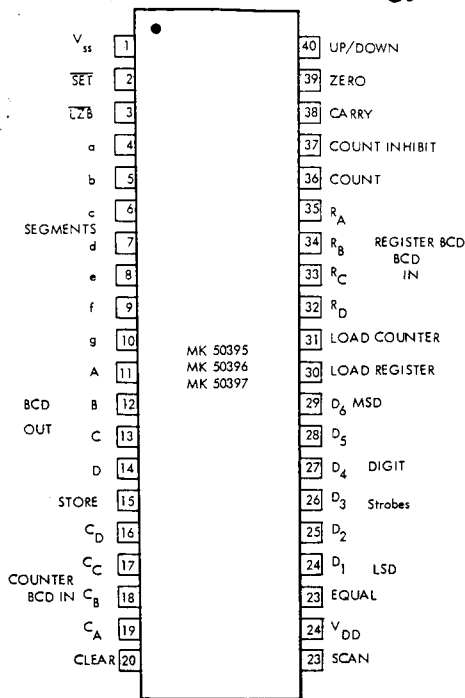
Figure 5.   MOSTEK 50395 pinouts.
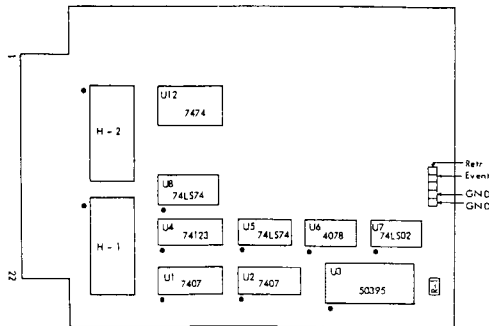
Pin	Signal	Description
R	CLRL	Low clears retrack & event latches.
J	EVNT	High indicates user event mark, cleared by CLRL.
K	RETR	High indicates user retrack, cleared by CLRL.
W	LRIN	Input Loran-C pulses from front-end. TTL, open-collector, pulled up to 5V on this board
18 17 16 15	REGA REGB REGC REGD	4-bit BCD digit load for U3 register.
13	LR	Load 50395 (U3) Register strobe.
11	SET	Set U3 to MSD for data load.
6	CLOK	1 MHz clock, from microcomputer.
12	CLRD	Low clears digit strobe IRQ latch.
14	CLRP	Low clears Loran data latch.
H	LDAT	Loran data - loop sample output.
19	IRQC	Combined IRQ from loop and digit strobes.
V	EQ	Equal pulse, for monitoring.

Figure 6.   Pictorial and signal glossary.