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A Computer Controlled Signal Preprocessor for Laser Fringe Anemometer Applications

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SUMMARY

Commercially available laser fringe anemometer (LFA) signal processors are designed and built under the assumption that adjustments to optimize the signal must be made by the operator outside the control of the computer used for reducing the acquired data. Because of this limitation, on-line modification of the data acquisition parameters can be difficult and time consuming. A computer controlled interface, called a preprocessor has been designed and built at NASA Lewis Research Center to alleviate this problem.

The raw signal from the photo-multiplier tube is input to this preprocessor which splits the dc component (pedestal) from the signal; and under computer control, filters the remaining ac signal to reduce noise, then amplifies the signal to an acceptable level. In addition, certain "housekeeping" procedures are performed also under computer control, such as handshaking to the processor, monitoring the photomultiplier dc current output, controlling the photomultiplier supply voltage, and controlling the seed generator.

INTRODUCTION

The laser fringe anemometer (LFA) technique has become the most widely used method for nonintrusive measurement of fluid flow (ref. 1). A block diagram of a typical LFA system is shown in figure 1. The laser generates a coherent light beam. The transmitting optics split this beam into two, focus the beams and cause them to intersect at the probe volume. The interference of the two focused, intersecting beams creates fringes within the probe volume. In many applications, a seed generator is used to produce particles which are meant to follow the flow and pass through the probe volume. A seed particle flowing through the fringes scatters the incoming light generating an optical signal whose frequency is proportional to the velocity of the particle. The scattered light is focused by the receiving optics onto a photo-multiplier tube (PMT) which converts the light signal into an electrical signal.

Normally the electrical signal is then fed into a signal processor which amplifies and filters the signal before converting it into a form which can be processed by the computer. Of the many different types of signal processors used in laser fringe anemometry, one of the most prominent is the counter-processor. The remainder of this paper assumes the use of such a signal processor. A good introduction to laser anemometry, including a brief discussion of the operation of the counter processor is provided by Ronald Adrian (ref. 2).

Data sent to the computer is usually the time-of-flight of a particle through a fixed number of fringes in the probe volume, and the particle

interarrival time, that is, the elapsed time between the current particle and the previous valid particle. In the LFA systems at Lewis Research Center, this data is fed directly from the signal processor to the memory of the computer via a technique called Direct Memory Access or DMA.

Commercially available counter-processors (ref. 3) require that the operator make adjustments to the controls depending on the operating conditions of the flow field under investigation. Previously, this was not believed to be a problem. However, there is increasing evidence that such settings as the gain of the system and the choice of filters influence the data quality to such an extent that incorrect settings can invalidate a data set.

Hosel and Rodi (ref. 4), in their work, describe the effect of signal to noise ratio (SNR) on data quality. The value of SNR is a function of the gain of the system (including signal gain, and the voltage supplied to the PMT), as well as the noise (both shot noise, and electronic noise). Previous work (ref. 5) has also described the effect of filter choice on data quality. Poorly chosen filters can be worse than not filtering at all. Both references describe the dependence of data quality on these phenomena as a function of the parameters of the input signal. Systems which would take advantage of these theories must take control of these parameters.

Even when optimization is not used, the data is usually reduced by a digital computer. In this case, the researcher finds it necessary to record the system gain and filter settings along with the data for off-line data reduction. Rather than entering the settings through the keyboard, it is much more effective to allow the computer to set and store these parameters directly. This relieves the researcher from setting the options, and then recording them.

A computer controlled preprocessor has been developed which performs these functions, thereby making possible the optimization of signals from an LFA system. This component is shown in dotted lines in figure 1. Since the counter-processor is widely available, a preprocessor was designed to be used in conjunction with the counter-processor to perform those functions previously controlled with manual settings. The preprocessor allows direct computer control of the high pass and low pass filter settings, the system gain, the PMT voltage, the seed generator, and the DMA control signals. These functions are all under direct control of the same digital computer which is acquiring the data from the counter. In addition, the preprocessor allows both the computer (through an analog input channel), and the researcher (with a variety of meters and alarms) to monitor the dc portion of the input signal from the PMT. This design enables the system to set up conditions for which the highest signal quality can be obtained quickly and consistently.

DESIGN

A number of criteria were involved in the design of the preprocessor. First, the control functions were to be interfaced to the computer used for data acquisition. The interface chosen for this device is a parallel interface which provides and accepts TTL logic levels. This design choice provides both speed and ease of use.

Second, it was desired that the components be of an "off-the-shelf" variety to minimize both development and repair time. Obviously, ready-made components are not necessarily available to perform the necessary functions, so this requirement was relaxed where necessary to include components at the chip level. Because of the interface choice, the logic design was constrained to TTL compatible components. Since there is a wide range of TTL compatible products, this simplified the logic design.

Third, it was essential that, for all functions, both manual and computer control be provided. The checkout of the system was greatly simplified by the use of manual switching. Also, during the setup process, it is sometimes desirable to switch the settings manually for data verification purposes. It was assumed that for data acquisition purposes, the computer would control the preprocessor. This decision simplified the design, because the communications interface need only function in one direction.

Fourth, the user required that the filters, and other signal path components, be easily swappable with other types. This means that the connections to these signal path components be of a "quick-disconnect" type and that these components be self-contained, as far as possible. At design time we were undecided as to which type of filter would be the best suited for conditioning the Doppler signal. Thus it was also advantageous for the filters to be swapable so as to take advantage of new information about filter performance.

Finally, as with all research equipment, the design was to allow for future upgrades and expansion. In many cases, the experiment requires other operations to be controlled through the computer in the same manner as the counter processor. Since this functionality could be added to the preprocessor with little effort, it was decided to do so.

The requirements for the control and interface software were less stringent, at least in the primary phase. The existing data acquisition and reduction software was written in FORTRAN IV (ref. 6), with some high speed data handling routines written in MACRO Assembly (ref. 7). Because of this, the new software to handle the preprocessor had to be written in these, or a compatible language. Due to the expected high data rates available with the existing system, the computer preprocessor interface requires fast implementation of commands for on-line modification of the control functions. In addition, the human computer interface was to be "user-friendly." This necessitated a high level language interface. The best solution was to write an Assembly language driver routine for the hardware interface, combining it with a FORTRAN IV program to control the user interface.

It was also decided that optimization schemes would be implemented in software, rather than hardware, to allow for modification as new techniques are learned. Although some loss of implementation speed results from this decision, the overall gain in speed, compared to manual optimization, is well worth the effort.

IMPLEMENTATION

A block diagram of the signal flow path is shown in figure 2. Each function performed by the preprocessor can be controlled via the computer, or

directly from the front panel. The signal from the PMT is split into its nominal ac and dc components by means of a capacitor. The dc component, known as the pedestal, is fed to an integrator with a preprocessor controlled time constant. The resulting integrated dc signal is then input to an ammeter, with associated hardware alarm, and to an analog input line tied to the computer. The meter allows the user to monitor the average output current of the PMT, while the input to the computer allows the software to record this signal. The ac signal path is more complicated. The signal is fed to the first of two banks of filters. Under preprocessor control the signal can be fed to any one of up to eight high pass filters to remove the remains of the pedestal from the information at the Doppler frequency. After passing through the high pass filter, the signal is amplified using a 20 dB fixed gain amplifier. Following this amplification the signal is fed to the second bank of eight filters, this time low pass filters to remove high frequency noise. As before, the selection of the filter is controlled by the preprocessor. The resultant signal is amplified again, using a 30 dB fixed gain amplifier, for a total gain of 50 dB. For most flow conditions, this gain is enough to saturate the counter electronics, causing a systematic measurement error. For this reason a 0 to 127 dB programmable attenuator is used to reduce the signal strength. (This setup is similar to that found in the input conditioner of counter-processors.) The amount of attenuation is controlled via the preprocessor. This filtered, amplified signal is then fed into the counter-processor.

The functions of the counter that are pre-empted by the preprocessor are turned off. The filters in the counter are set to "off", and the internal gain of the processor is set to 1. At these settings, the gain and filter settings are entirely in the control of the preprocessor.

The simplest way to describe the implementation of the control functions of the preprocessor is to work in reverse order from the design; that is to proceed from the software to the hardware. Eight functions are presently controlled using the preprocessor. These are the ammeter integrator time constant, the high pass filter, the low pass filter, the programmable attenuator, the seed generator, the DMA control switches, the inter-arrival time counter, and the PMT supply voltage. In addition, four spare latches are provided for future expansion.

A logic diagram of the eight control functions is shown in figure 3. The address decoder determines which of the eight latches is to be enabled by the incoming data. The manual enable is only energized when the computer/manual selection switch is in the "manual" position. This is shown symbollically by the "AND" gate. The data can come from either the computer (while the preprocessor is in computer mode), or from physical switches on the preprocessor (while the preprocessor is in manual mode). After the data is latched to the correct controlled function, the data is displayed using LED's on the preprocessor face, and sent in parallel to the circuitry which controls the requested function. Figure 4 shows a photograph of the front face of the prototype preprocessor. Above the LED which verifies the control function choice is a switch corresponding to the particular bit in the control function which can be set in the manual mode. A detailed drawing of the logic board layout, with a parts list, and a sketch of the preprocessor front panel, is given in appendix A.

The ammeter integrator time constant is determined by the value of a capacitor switched into the feedback loop of an op-amp (see analog board layout in appendix A). The values of capacitance were chosen to provide time constants of 0, 0.01, 0.1, 1.0, and 10.0 sec, respectively. The 0 sec time constant is provided by means of a disable switch on the op-amp to allow the display of the instantaneous value of phomultiplier current. The "address" of this control function is "0", and the data sent is the choice of time constant, using the following code: "0" - 0.01; "1" - 0.1; "2" - 1.0; "3" - 10.0; and "8" - 0 sec.

The second of the control functions to be implemented is the choice of high pass filter. The high pass filter bank is a set of eight high pass filters connected through two single pole/eight throw coax switches which route the signal to and from the requested filter. The "address" of this function is "1", and the data sent is the choice of filter numbered from "0" to "7." Since the connections to the switches in the analog path are BNC type, the filters can be swapped for other types, depending on the test specifications. Because the type and cutoff frequency of the filters is immaterial to the operation of the preprocessor, no filters will be specified in this paper. A discussion of the steps required in the choice of filters is presented in reference 5.

The third control function, naturally enough, is the low pass filter selection. The internal workings of this control hardware set are identical to those of the high pass filter circuit. The "address" of this function is "2."

The fourth, and last function in the analog signal path is the attenuation. The programmable attenuator provides up to 127 dB of attenuation in 1 dB steps. The signal has already been amplified by 50 dB. Thus the programmable attenuator allows the user, under preprocessor control, to select the overall system gain under a total range of -67 to +50 dB. The "address" of this function is "3" and the data sent is a number from "0" to "127" representing the amount of attenuation.

The next control function is a simple on-off switch to control the seed generator. The experiment for which this preprocessor was designed uses a fluidized bed seed generator (ref. 8) to provide particles with which to measure the flow. The "address" of this function is "4", with the data sent being a "0" for seed generator and air flow off and a "1" for seed generator and air flow on.

The next two control functions deal with the data sent across the DMA interface from the signal processor to the computer. The first, the DMA data control switches, determine the makeup of the data sent. In the processor used at NASA Lewis, a switch package on a printed circuit board in the DMA interface module allows the user to select up to three data words to be sent to the computer for each valid data point. In addition, handshaking protocols are determined by other switches on this package. All of these functions are replaced by drivers in the preprocessor which are wired directly into the PC board, replacing the switch package. The "address" of this function is "5," with the data sent being a number representing those functions which are enabled. Each function is one bit in the number set, in the following order:

Function	Bit Number	
Processor settings ("A" word)	0	0 = Off, 1 = on
Data interarrival time	1	0 = Off, 1 = on
Not used	2	Set to 1
SENDER BUSY (control signal)	3	0 = High true, 1 = low true
RECEIVER READY (control signal)	4	0 = High true, 1 = low true

A more complete explanation can be found in the manual (ref. 3). The result of this setup is that the data sent to the preprocessor is a number from "0" to "31" representing the required switch setup.

The second function which modifies the counter-processor is the determination of the exponent used in the counter which processes the data interarrival time. This data interarrival time is also called the time between data points, or TBD. The "address" of this function is "6", and the data sent is the value of the exponent of 2 used in setting the counter frequency. For example, a command sending a "0" to this address sets the interarrival time counter to count in increments of 2^0 microseconds (μs). A "3" sent to this address requires the counter to count in increments of 2^3 μs (increments of 8 μs).

The final control function implemented is the PMT supply voltage. The voltage supplied determines the sensitivity of the PMT to incoming light and, as such, is an indirect control of the signal-to-noise ratio of the system. The "address" of this function is "7," and the data sent is a fraction of the maximum allowable voltage. The number is eight bits wide, giving the user 256 increments to choose for a voltage. "0" corresponds to 0 V, while "256" corresponds to the maximum allowable voltage. In the software which provides the user computer interface, this number can be manipulated so that the user enters the voltage required, and the computer calculates the number between 0 and 256 which matches this requirement most closely.

Because the software algorithms for optimization are not mature, the only software which can be described deals with the hardware interface from the computer to the preprocessor. As has been mentioned previously, this routine is designed to be called from a FORTRAN program but, due to speed requirements, is written in Assembly Language. The subroutine, called PREPRC, sends a 16 bit binary number to the digital interface in the following form:

High order byte	Low order byte
preprocessor function address	preprocessor function command

The call from FORTRAN is made using the command line:

```
CALL PREPRC (NADRES,NDATA)
```

where

NADRES - Address (0 to 7) of function to be controlled
NDATA - The coded command to be processed

The listing for this simple routine is found in appendix B.

CONCLUSIONS

The preprocessor functions as expected for both the improvement of data acquisition speed, and the increase of data accuracy. Using computer control of the various functions available with the preprocessor, the researcher is able to monitor the effect of the filters and gain on signal quality, and to quickly change the settings of these functions without the worry of manually recording these settings. As a hardware tool in the laser anemometry field, the signal preprocessor should prove very useful.

With the availability of the preprocessor, certain steps can be taken to further improve data quality, in a quantitative manner. One could develop algorithms for the optimization of the laser signal as a function of the filter settings for on-line use as well as algorithms to determine the effect of laser power, PMT voltage, and gain setting on the resultant laser signal. The inclusion of control of laser power will require the addition of circuitry similar to that which controls the PMT voltage.

The signal preprocessor is a device which can expand to account for future improvement in LFA signal quality and is easy enough and fast enough to use in present day experiments to improve the data record by recording such settings as filter choices and gain.

APPENDIX A - CIRCUIT LAYOUTS AND PARTS LIST

The preprocessor layout is broken down into three sections; the logic board, the analog board, and power and auxiliary control. The logic board is shown in figure A.1, with IC's and components marked consistent with the parts list given in table I. The pin configurations for the connectors C, D, E, F, G, H, I, and L are given in table V. The switches S1, S2, S19, and S27 through S31 are the connections through connector A to the front panel; while the LED's L1 through L45 are the connections through connector B to the front panel. The switches labelled with T are connections through connector A to the thumbwheel switches on the front panel. All thumbwheel connections have 3 digits associated with the switch. The first is the switch number, the second is the number of the thumbwheel in the switch (some thumbwheel switches have two thumbwheels), and the third number is the pin number to which the line is tied. For example T612 signifies that the line is tied to pin 2 of thumbwheel number 1 in switch 6. The pin configurations for connectors A and B are given in table IV, and more thoroughly described below. The power connections marked on this drawing and on figure A.2 come from the power leads shown in figure A.3. The components layed out in figure A.1 completely describe the logic control of the preprocessor.

Figure A.2 depicts the analog circuit layout of the preprocessor. As with the previous figure, the switches S20, S21, and S40 are the connections through connector A to the front panel. The BNC connections shown on this drawing are on the front, or back panel, as marked.

Figure A.3 shows four separate drawings. The first, the back panel layout, is self explanatory. Below the back panel is the layout for the cable which is placed inside the DMA data interface on the counter-processor. By the use of this cable, control of the DMA data switches, and the $\Delta\tau$ switch (for interarrival time) is given to the computer. The circuit board components replaced by the cable are called out for the model 1998A. To the right of the back panel is the seed generator control relay assembly. This assembly is housed in a separate chassis located near the experiment and connected to the back panel via an RG59 cable with BNC connections. Finally, in the lower right hand corner of figure A.3, the power supply circuit is shown, including the circuit to generate the 20 VDC output necessary to power the amplifiers in figure A.2. The component parts list for the power supply circuit is given in table III.

Figure A.4 shows the layout of the front panel asembly. All switches shown in this figure are tied to connector pin A45 for the "on" position, and tied to connector pin A41 for the "off" position. The common position for each switch is tied through the connector to the location given in table IV. The exceptions to this convention are: 1) Switch S3 "on" is tied to A41, and "off" is tied to A45; 2) S20, S21, S22, and S40 which are tied according to the instructions given in table IV(a). The thumbwheel switches each have a pin labelled "X" which is tied to A45 (+5VDC), and a pin labelled "Y" which is tied to A41 (GND); providing positive TTL logic to the digital board. The positive terminals of LED's L1 through L4, and L28 through L45 are tied to connector pin A45. The positive terminals of LED's L5 through L27 are tied to connector pin A46. The negative terminals of all LED's are tied through connector B to the locations given in table IV(b).

The switches are set so that, when in local mode (the local enable switch, S2 is depressed) the settings determined by the switch positions for all eight functions are sent to the latches, and displayed via the LED's. For the time constant and the high and low pass filters, the thumbwheels act as binary counters. For example to choose high pass filter three in the local mode, T3 is set to read the digit "3." The thumbwheels for the attenuation, $\Delta\tau$, and photo tube voltage operate in the same manner, but the LED's indicate whether or not the given binary digit is in the "on" position. The value of each of these three banks is determined as the sum of all the "on" LED's. The LED's for all functions signify an "on" state when lit. For the seed generator, the DMA control switches, the attribute is enabled individually by placing the related switch in the "on" position. Switches S21 and S40 control the ammeter. This meter can show either the supplied voltage to the PMT ("VOLTAGE" position on switch S40), or the current from the PMT ("CURRENT" position). When switch S40 is in the "CURRENT" position, switch S21 determines whether the operator is viewing the Alarm level (the "ALARM" position), or the actual dc current level from the PMT (the "METER" position). Resistor R29 is the point at which the alarm current level is set. While the meter can display three different readings, the bargraph display continually shows the PMT output dc current as a percentage of the alarm current level. When the current output by the PMT exceeds the alarm level, the bar graph flashes, and the "SONALERT" alarm sounds (if switch S20 is "on").

Switch S1 enables the rest of the switches if in the "local" position, and disables all data switches and thumbwheels if in the computer mode. The LED's, however display the current setting of all control functions regardless of the position of switch S1. The final switch S22, is the ac power switch, and obviously, nothing happens if the power is off.

Connectors A and B are mounted on the rear face of the front panel, along with those components separated from the rest in figure A.2.

APPENDIX B - INTERFACE SOFTWARE DESCRIPTION

As was stated previously, this software was written for use on a Digital Equipment Corporation PDP series computer. The interface card used is the DR11-K digital input/output card. The interface software consists of an Assembly Language routine which packs the "address" of the control function, and the "data" into a single 16-bit word, complements this word, and places the complemented word in the DR11-K's output register. The word is complemented because logical "1"'s are interpreted by the DR11-K as 0 V, while logical "0"'s are interpreted at +5 V. The complementing of the data word reduces confusion to the operator. The subroutine which performs these functions is shown below:

```
                .TITLE PREPRC
                .PSECT USER$I,RW,I,LCL,REL,CON
; FORTRAN CALL: CALL PREPRC(ADDRESS,DATA)
;               ADDRESS - CONTROL FUNCTION
;               DATA    - CODED COMMAND
                .GLOBL PREPRC
                STA = 16770 ; DR-11 STATUS REGISTER
                OUTPUT=STA+4          ; DR-11 OUTPUT REGISTER
PREPRC:         CLR     @#STA         ; CLEAR STATUS REGISTER
                MOV     @2(R5),R1     ; MOVE ADDRESS TO R1
                ASH     @10,R1        ; SHIFT ADDRESS TO HIGH BYTE
                ADD     @4(R5),R1     ; MOVE DATA TO LOWER BYTE OF R1
                COM     R1            ; TAKE ONES COMPLEMENT OF R1
                MOV     R1,@#OUTPUT   ; MOVE R1 to DR-11 OUTPUT REGISTER
                RTS     PC            ; RETURN TO CALLING ROUTINE
                .END
```

Except for the DMA switches (address #5), the data sent to the DR11-K is the number representing the command sent, in accordance with table VI. The DMA switches conform to the discussion in Section III. Table VI should be used as a template to design the routine which calls PREPRC to perform the manipulations necessary for the control of the preprocessor.

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TABLE I. - PREPROCESSOR LOGIC BOARD PARTS LIST

(a) Integrated circuits

Number	IC Type	IC Function
U1,U2,U23,U24	DM71LS97N	Octal buffer
U3	DM74154N	4 to 16 Decoder
U4-U6	DM74157N	Quad 2 to 1 select
U7-U15,U42,U43	DM74LS298N	Quad latch w/select
U16-U18	DM7445N	Decoder/driver
U19,U20,U22,U46	ULN2003	Darlington driver
U21	LF11508	See table II
U25	DM7404N	Hex inverter
U45	DAC-02	Digital to analog Cnv
U47	LM3900	Quad Op-amp

(b) Resistors, LED's

Number	Type
R1-R23	8.5 kΩ, 1/4 W
R117-R123	200 Ω, 1/4 W
R34	1 kΩ, 1/4 W
R35	5 kΩ Potentiometer
R38	63 kΩ, 1/4 W
R39	100 kΩ Potentiometer
L1-L45	Dialco PN 559-0102-001 LED

(c) Connector destinations

Connector	Destination drawing
C,D,E,F,G,L H,I	A.2 Analog board A.3 Back panel connections

TABLE II. - PREPROCESSOR ANALOG BOARD PARTS LIST

(a) Integrated circuits

Number	IC Type	IC Function
U21	LF11508	SP8T Analog switch
U26	LM3900	Op-amp
U27	LM311N	Comparator
U28	NSM39147	Bar-graph display driver
U29	SCG616NP	Sonalert alarm
U30	152-0256	μ-Ammeter
U31,U32,U33,U34	7108-DRS	SP8T Switch
U35	GAM-20-150	20 dB Amplifier
U36	GAM-30-150	30 dB Amplifier
U37	PA-54	127 dB Attenuator
U38	ZSC-2-1W	Coupler
U44	PMT-20A/N	Photo-multiplier supply
HF1-HF8		High pass filters
LF1-LF8		Low pass filters

(b) Resistors, capacitors

Number	Type
R25	25 kΩ, 1/4 W
R26	100 kΩ Potentiometer
R27	100 kΩ, 1/4 W
R28	5 kΩ Potentiometer
R29	100 kΩ Potentiometer
R30	1.2 kΩ, 1/4 W
R31	470 Ω, 1/4 W
R32	1 kΩ, 1/4 W
C1,C2	0.1 μF
C3	1.0 μF
C4,C7	10.0 μF
C5,C6	100 μF

(c) Connector destinations

Connector	Destination drawing
C,D,E,F,G,L	A.1 Logic board

TABLE III. - PREPROCESSOR "OTHER" PARTS LIST

(a) Integrated circuits

Number	IC Type	Type
U49	LM117N	Voltage regulator
U50		50 V @ 100 mA Supply
U51,U52,U53		±15 V @ 350 mA Supply

(b) Resistors, capacitors

Number	Type
R40	15 kΩ, 1/4 W
R41	1 kΩ, 1/4 W
C8	0.1 μF
C9	1.0 μF

(c) Connector destinations

Connector	Destination drawing
H,I	A.1 Logic board

TABLE IV. - PREPROCESSOR FRONT PANEL CONNECTOR LIST

(a) Connector A

Pin number	Device	Board position
1	S1	pin 10 (U7-U15,U42,U43)
2	S2	pins 3,6,10,13 (U4,U6,U6)
3	T114	U7-6
4	T112	U7-1
5	T111	U7-2
6	T214	U8-5
7	T212	U8-1
8	T211	U8-2
9	T314	U9-5
10	T312	U9-1
11	T311	U9-2
12	T414	U11-5
13	T412	U11-1
14	T411	U11-2
15	T428	U10-6
16	T424	U10-5
17	T422	U10-1
18	T421	U10-2
19	S19	U12-2
20	S20C	U27-7 [S20 on R29 (-), S20 off NC]
21	S21 On	U26-8,U26-10 [S21C thru 25 kΩ to U30 (+)
22	S40 Off U28-6	U26-4,U26-13 [S40C to S21 off]
23	S40 On	U47-10
24	T518	U15-6
25	T514	U15-5
26	T512	U15-1
27	T511	U15-2
28	S27	U14-2
29	S28	U14-1
30	S29	U14-5
31	S30	U14-6
32	S31	U13-2
33	T618	U43-6
34	T614	U43-5
35	T612	U43-1
36	T611	U43-2
37	T628	U42-6
38	T624	U42-5
39	T622	U42-1
40	T621	U42-2
41	U30 (-) U28-9, Pin Y of all thumbwheels	GND
42	U29 (+)	R28 (-)
43	U28-7 R29 (-)	U27-2,U26-9

TABLE IV(a). - Continued.

Pin number	Device		Board position
44	U28-4	+15 VDC	
45	U28-1, Pin X of all thumbwheels	+5 VDC	
46	R29 (+)	+30 VDC	

(b) Connector B

Pin number	Device	Board position
1	L1	U16-1
2	L2	U16-2
3	L3	U16-3
4	L4	U16-4
5	L5	R1(+)
6	L6	R2(+)
7	L7	R3(+)
8	L8	R4(+)
9	L9	R5(+)
10	L10	R6(+)
11	L11	R7(+)
12	L12	R8(+)
13	L13	R9(+)
14	L14	R10(+)
15	L15	R11(+)
16	L16	R12(+)
17	L17	R13(+)
18	L18	R14(+)
19	L19	R15(+)
20	L20	R16(+)
21	L21	R23(+)
22	L22	R22(+)
23	L23	R21(+)
24	L24	R20(+)
25	L25	R19(+)
26	L26	R18(+)
27	L27	R17(+)
28	L28	U20-14
29	L29	U22-13
30	L30	U22-14
31	L31	U22-15
32	L32	U22-16
33	L33	U22-12
34	L34	U22-11
35	L35	U22-10
36	L36	U20-16
37	L37	U20-15

TABLE IV(b). - Concluded.

Pin number	Device	Board position
38	L38	U46-10
39	L39	U46-11
40	L40	U46-12
41	L41	U46-13
42	L42	U46-14
43	L43	U46-15
44	L44	U46-16
45	L45	U20-13

TABLE V. - PREPROCESSOR AUXILIARY CONNECTORS LIST

(a) Connectors C and D

Pin number	Device	"C" Destination	"D" Destination
1	U17-1	U31-1	U32-1
2	U17-2	U31-2	U32-2
3	U17-3	U31-3	U32-3
4	U17-4	U31-4	U32-4
5	U17-5	U31-5	U32-5
6	U17-6	U31-6	U32-6
7	U17-7	U31-7	U32-7
8	U17-9	U31-8	U32-8

(b) Connectors E and F

Pin number	Device	"E" Destination	"F" Destination
1	U18-1	U33-1	U34-1
2	U18-2	U33-2	U34-2
3	U18-3	U33-3	U34-3
4	U18-4	U33-4	U34-4
5	U18-5	U33-5	U34-5
6	U18-6	U33-6	U34-6
7	U18-7	U33-7	U34-7
8	U18-9	U33-8	U34-8

(c) Connector G

Pin number	Device	Destination
1	R117(+)	U37-1
2	R118(+)	U37-2
3	R119(+)	U37-4
4	R120(+)	U37-8
5	R121(+)	U37-16
6	R122(+)	U37-32
7	R123(+)	U37-64

TABLE V. - Concluded

(d) Connector H

Pin number	Device	DR11-K desg[a]	Pin number	Device	DR11-K desg[a]
1	U2-2	Out 0	9	U1-2	Out 8
2	U2-4	Out 1	10	U1-4	Out 9
3	U2-6	Out 2	11	U1-6	Out 10
4	U2-8	Out 3	12	U1-8	Out 11
5	U2-12	Out 4	13	U1-12	Out 12
6	U2-14	Out 5	14	U1-14	Out 13
7	U2-16	Out 6	15	U1-16	Out 14
8	U2-18	Out 7	16	U1-18	Out 15
17	GND	GND	18	GND	GND

[a]Not shown in drawings.

(e) Connector I

Pin Number	Device	Destination
1	U24-3	TSI DMA 1
2	U24-5	TSI DMA 2
3	U24-7	TSI DMA 3
4	U24-9	TSI DMA 5
5	U24-11	TSI DMA 6
6	GND	TSI $\Delta\tau$ (brn)
7	U25-8	TSI $\Delta\tau$ (red)
8	U25-6	TSI $\Delta\tau$ (org)
9	U25-4	TSI $\Delta\tau$ (yel)
10	U25-2	TSI $\Delta\tau$ (grn)

(f) Connector L

Pin Number	Device	Destination
1	U47-13	U44-11
2	U45-14	U44-8
3	U20-14	BNC seed generator
4	+5 V	Isolated low BNC seed generator
5	+30 V	Power supplies
6	GND	Power supplies

TABLE VI. - PREPROCESSOR FUNCTION CODES

Function	Address	Number of bits	Data
μ-Ammeter time constant	XXX0000	4	0000 - 0.01 sec 0001 - 0.1 sec 0010 - 1.0 sec 0011 - 10.0 sec 1XXX - Disable
High pass filter select	XXX0001	4	0000 - Filter 0 0111 - Filter 7
Low pass filter select	XXX0010	4	0000 - Filter 0 0111 - Filter 7
Attenuation control	XXX0011	8	X0000000 - 0 dB X1111111 - 127 dB
Seed generator and air flow control	XXX0100	4	XXX0 - Off XXX1 - On
DMA Data control	XXX0101	8	The binary sum of the following: +1 - Enables "A" word +2 - Enables "TBD" word +4 - Not used +8 - sel GND true busy +16 - sel GND true beady
$\Delta\tau$ (delta tau) switch control	XXX0110	4	0000 - 2^0 Clock rate (μs) 1111 - 2^{15} Clock rate (μs)
Photo-multiplier tube	XXX0111	8	00000000 - 0% max V 11111111 - 100% max V
EXTRA latches	XXX1001 XXX1010	4 or 8	

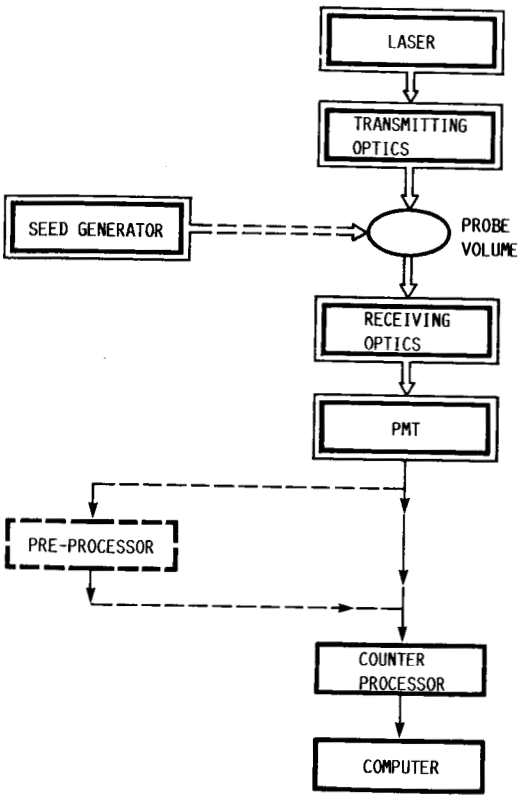

FIGURE 1. - TYPICAL LASER FRINGE ANEMOMETER SYSTEM.

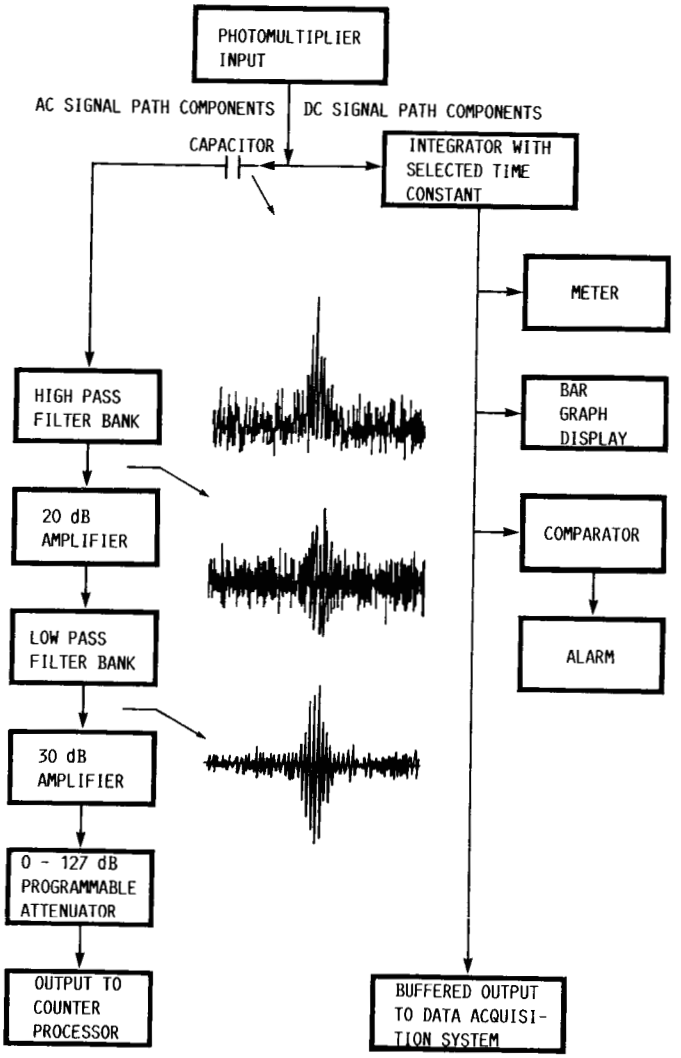

FIGURE 2. - LASER FRINGE ANEMOMETER PRE-PROCESSOR SIGNAL FLOW DIAGRAM SHOWING THE DOPPLER SIGNAL IN THE TIME DOMAIN AT THREE POINTS IN THE SIGNAL FLOW.

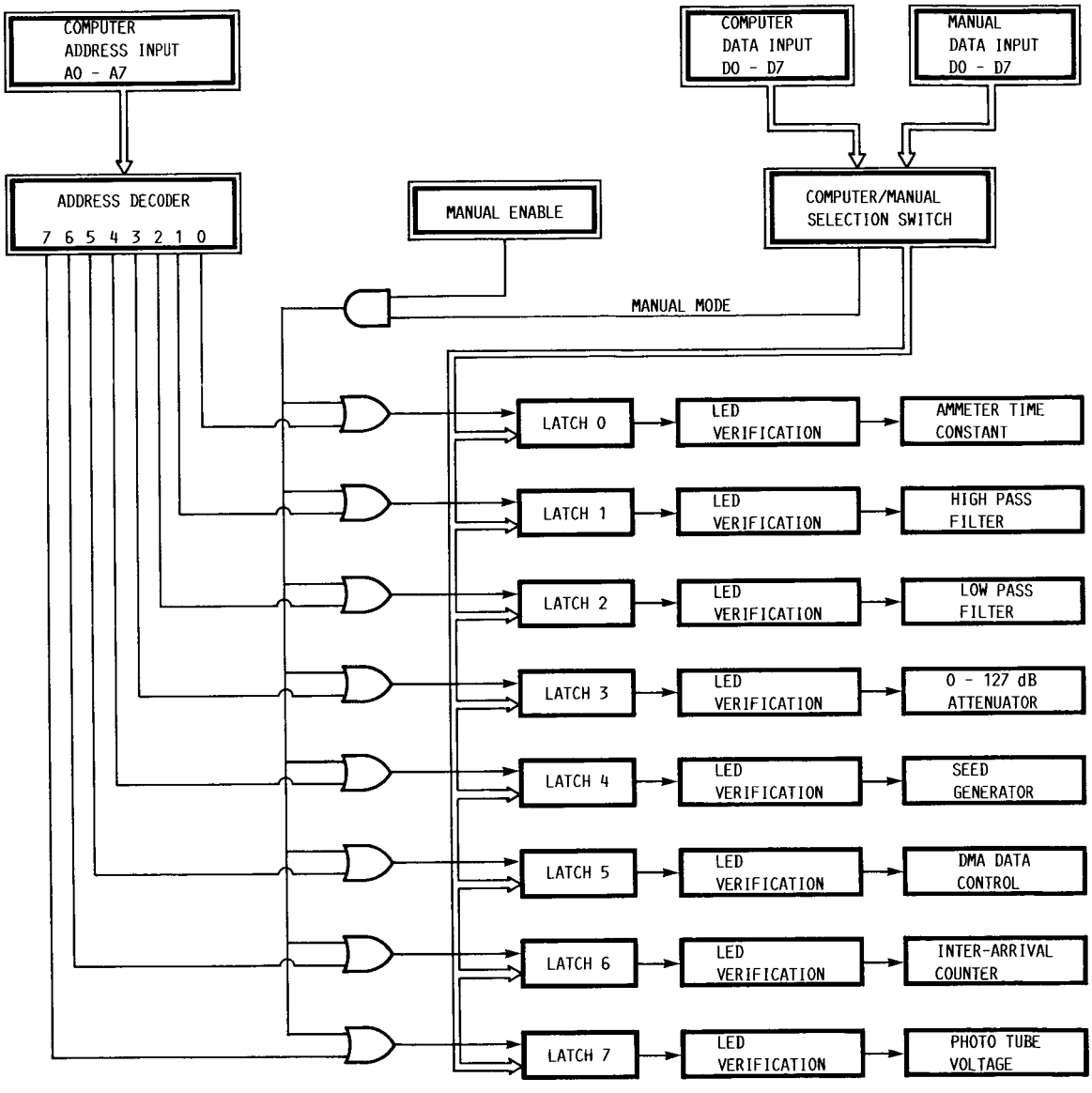

FIGURE 3. - LASER FRINGE ANEMOMETER PRE-PROCESSOR LOGIC DIAGRAM.

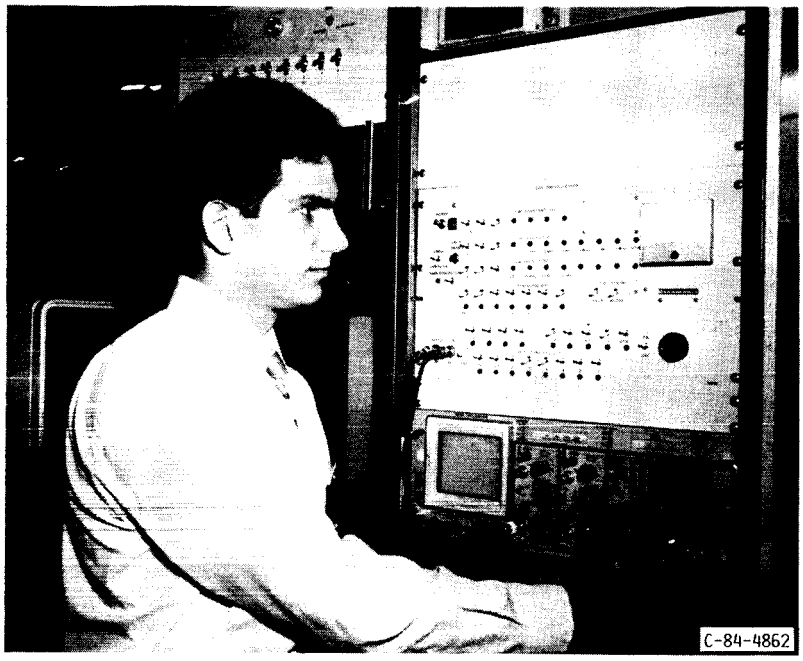

FIGURE 4. - LASER FRINGE ANEMOMETER PRE-PROCESSOR FRONT PANEL.

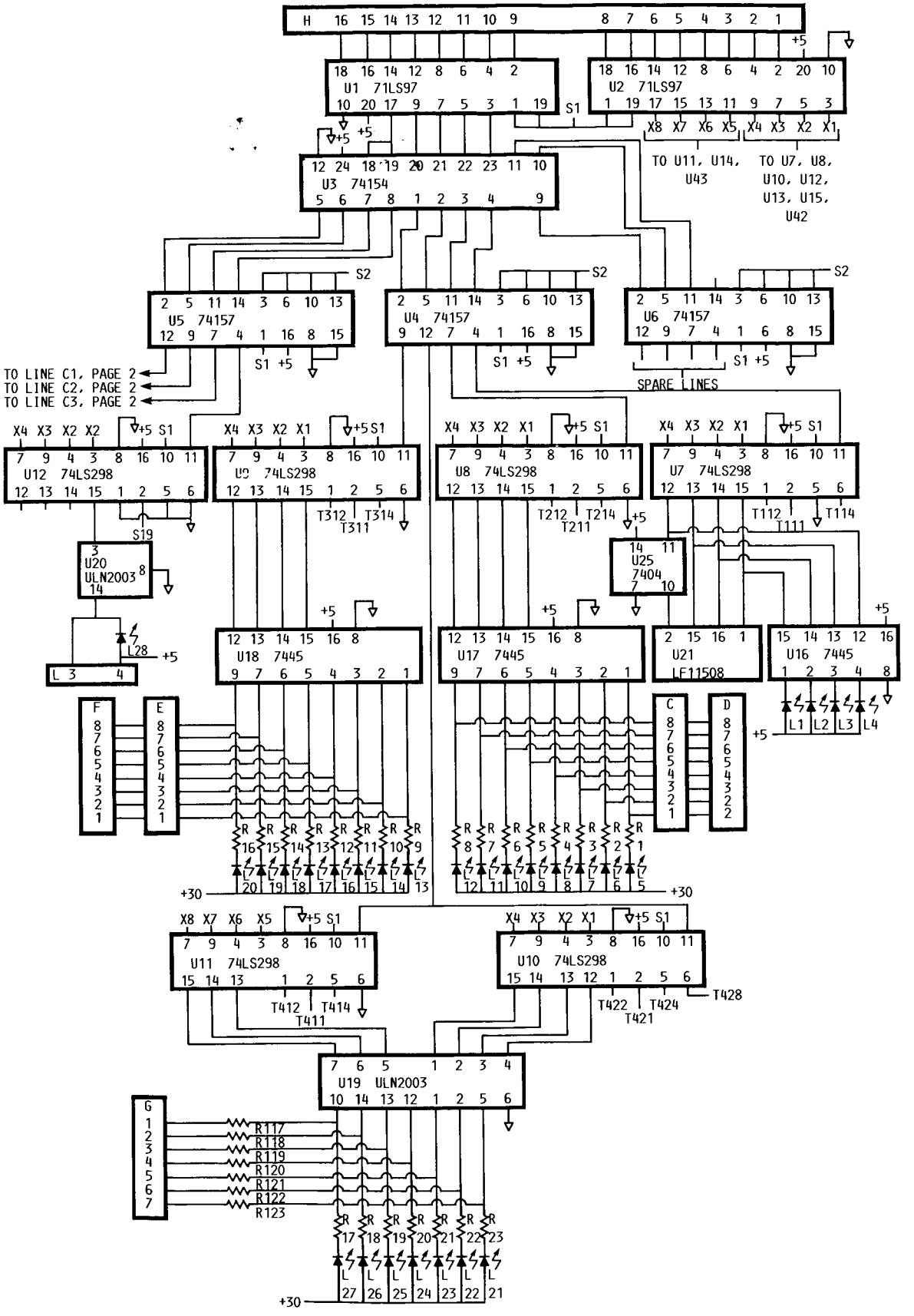

FIGURE A.1. - LFA PRE-PROCESSOR LOGIC BOARD.

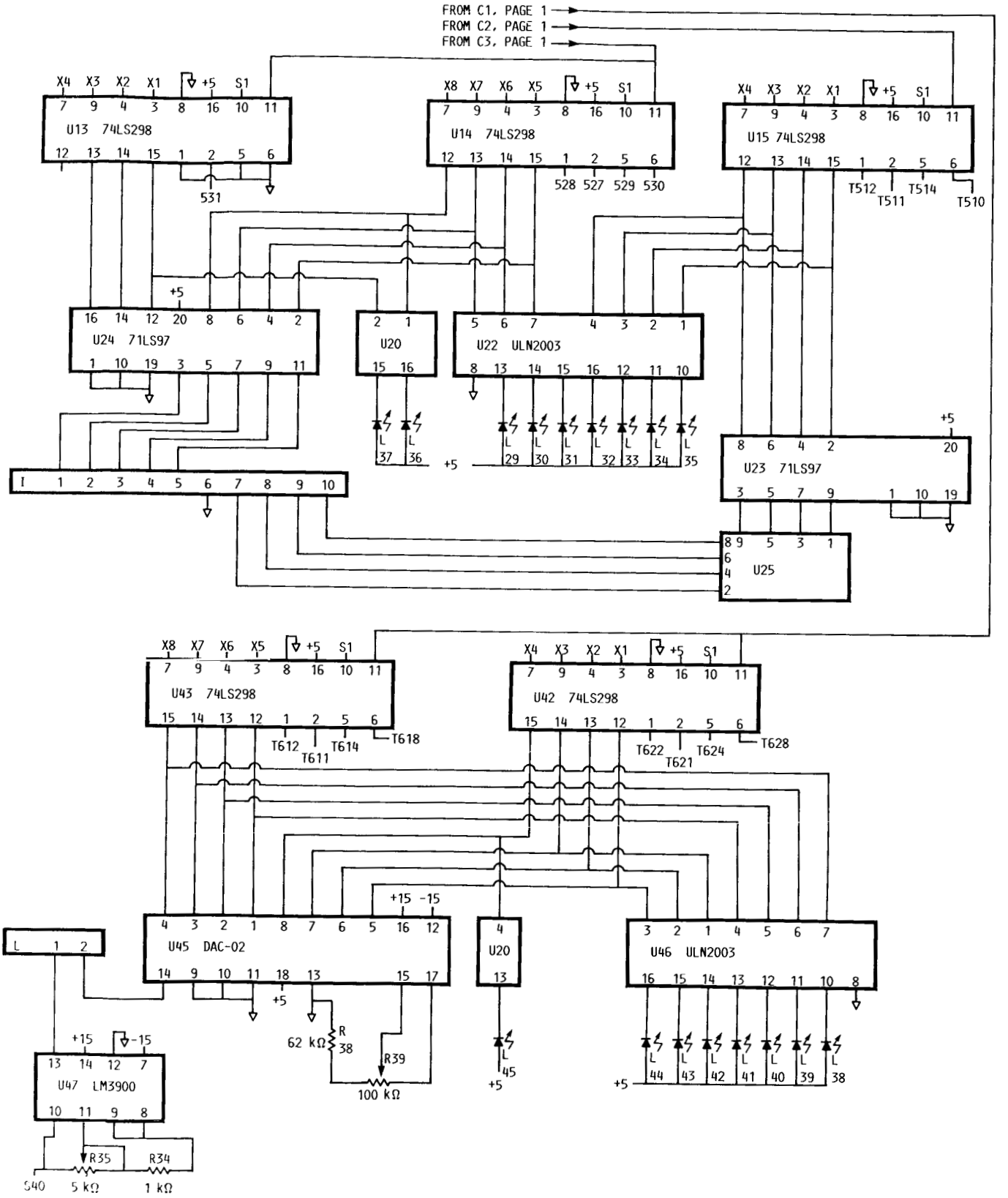

FIGURE A.1. - CONCLUDED.

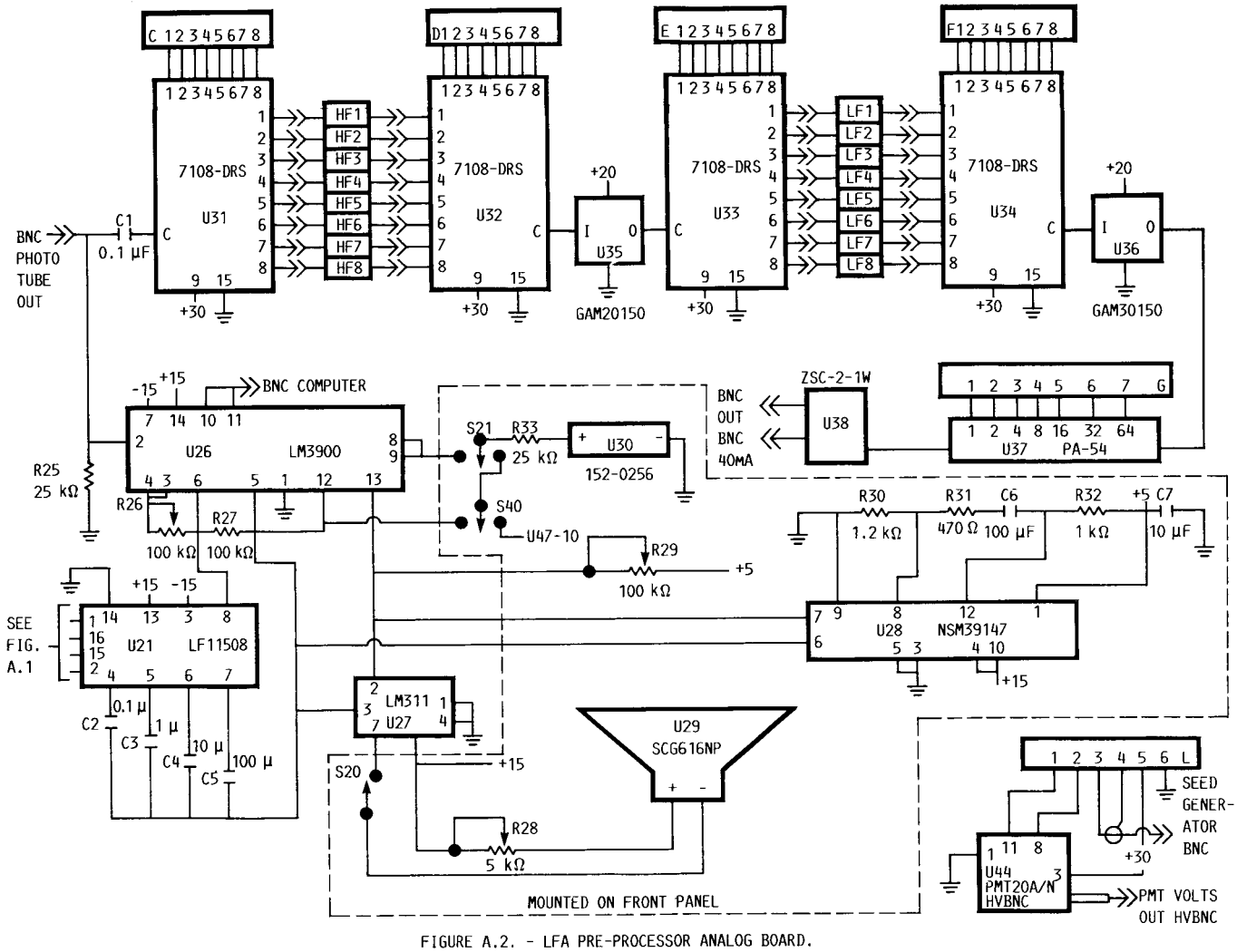

FIGURE A.2. - LFA PRE-PROCESSOR ANALOG BOARD.

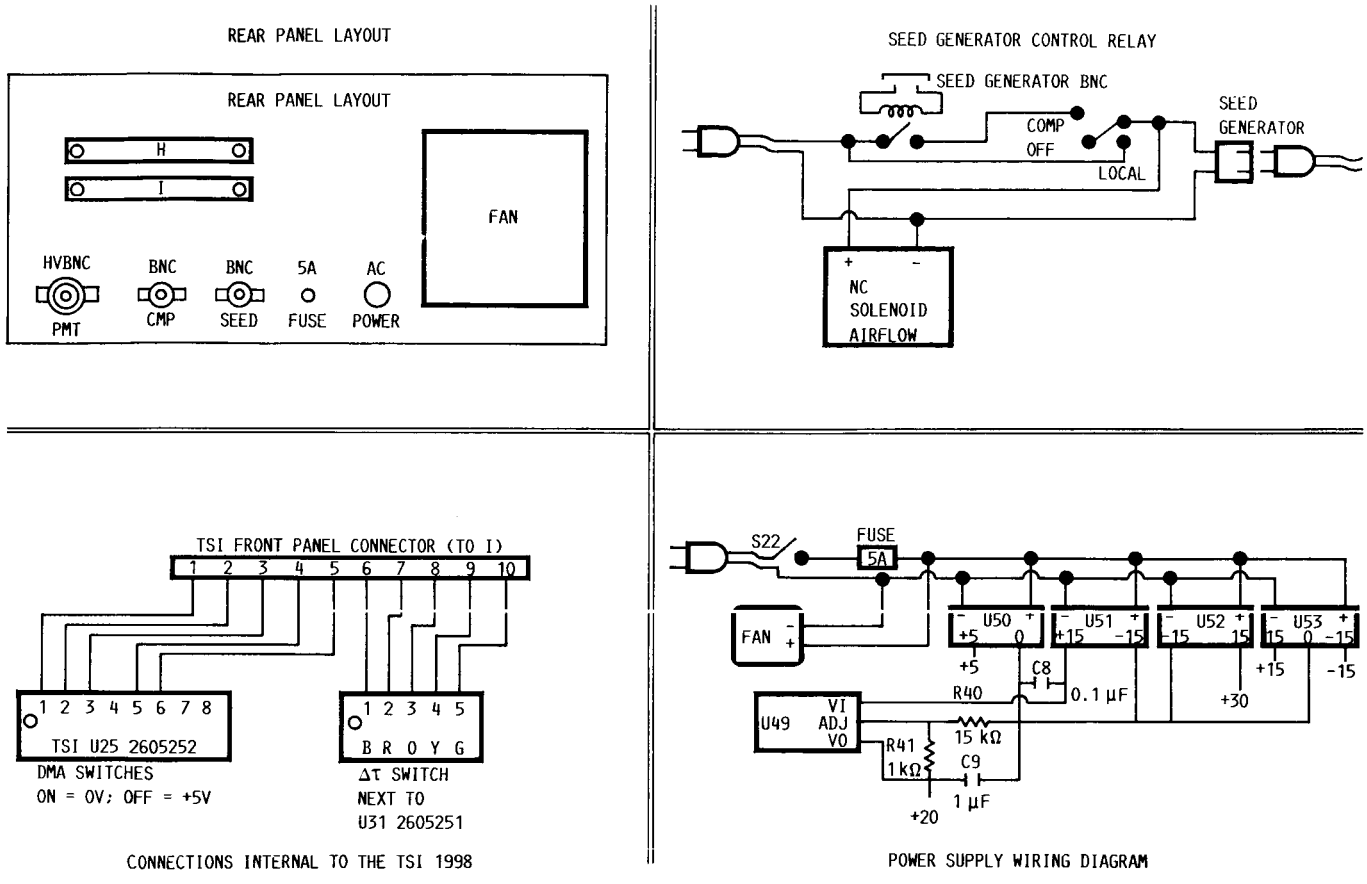

FIGURE A.3. - LFA PRE-PROCESSOR POWER SUPPLY, REAR PANEL, AND EXTERIOR CONNECTIONS.

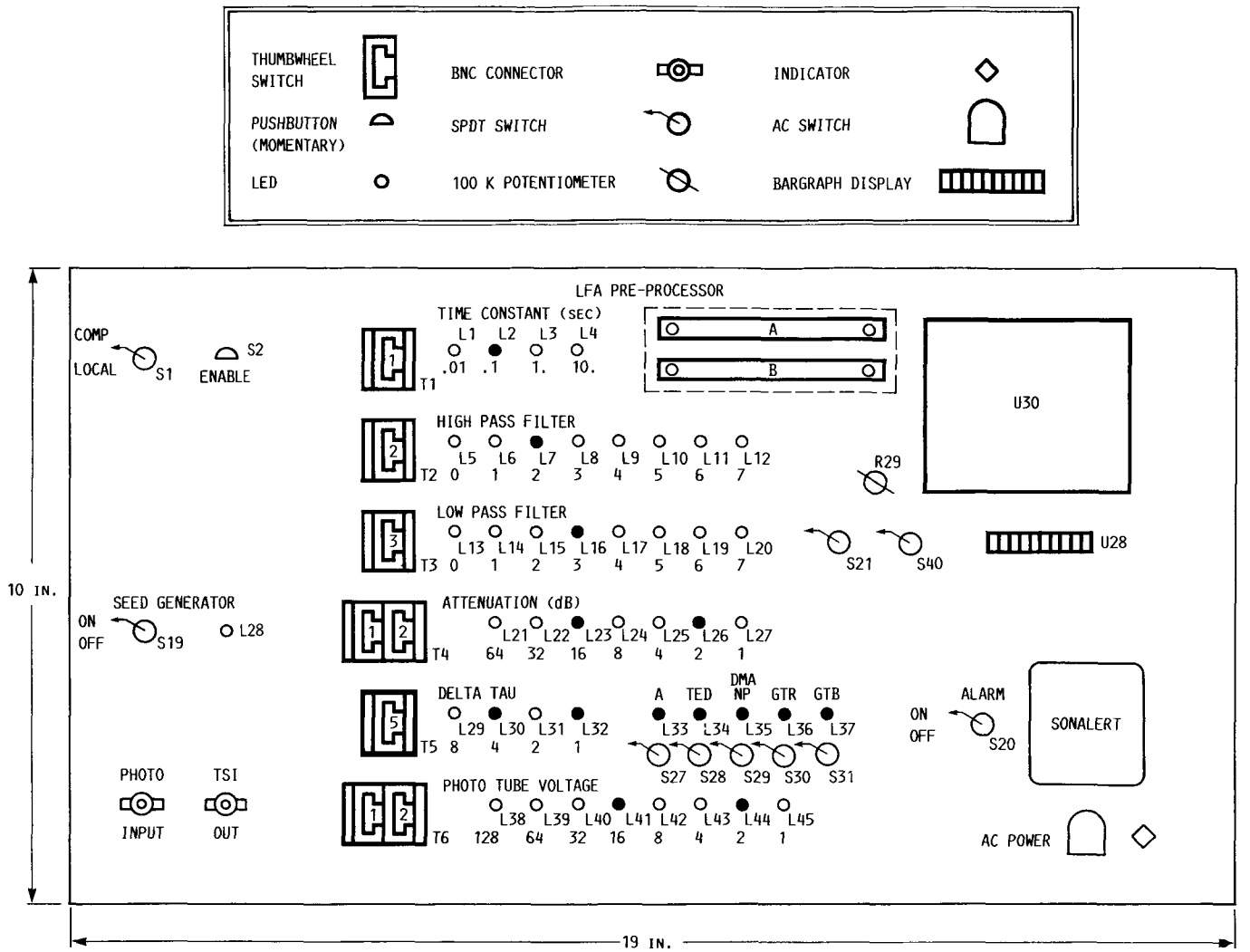

FIGURE A.4. - LFA PRE-PROCESSOR FRONT PANEL.

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15. Supplementary Notes

16. Abstract

The operation of most commercially available laser fringe anemometer (LFA) counter-processors assumes that adjustments are made to the signal processing independent of the computer used for reducing the data acquired. Not only does the researcher desire a record of these parameters attached to the data acquired, but changes in flow conditions generally require that these settings be changed to improve data quality. Because of this limitation, on-line modification of the data acquisition parameters can be difficult and time consuming. A computer-controlled signal preprocessor has been developed which makes possible this optimization of the photomultiplier signal as a normal part of the data acquisition process. It allows computer control of the filter selection, signal gain, and photo-multiplier voltage. The raw signal from the photomultiplier tube is input to the preprocessor which, under the control of a digital computer, filters the signal and amplifies it to an acceptable level. The counter-processor used at Lewis Research Center generates the particle interarrival times, as well as the time-of-flight of the particle through the probe volume. The signal preprocessor allows computer control of the acquisition of these data. Through the preprocessor, the computer also can control the hand shaking signals for the interface between itself and the counter-processor. Finally, the signal preprocessor splits the pedestal from the signal before filtering, and monitors the photo-multiplier dc current, sends a signal proportional to this current to the computer through an analog to digital converter, and provides an alarm if the current exceeds a predefined maximum. Complete drawings and explanations are provided in the text as well as a sample interface program for use with the data acquisition software.

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