WAFER LEVEL RELIABILITY TESTING: AN IDEA WHOSE TIME HAS COME

N87-27209

O. D. Trapp
Technology Associates
Portola Valley, CA

Abstract. Wafer level reliability testing has been nurtured in the DARPA supported workshops, held each autumn since 1982, at the Stanford Sierra Lodge on Fallen Leaf Lake, Lake Tahoe, CA. The seeds planted in 1982 have produced an active crop of VLSI manufacturers applying wafer level reliability test methods. Computer-Aided Reliability (CAR) is a new seed being nurtured. Users are now being awakened by the huge economic value of the wafer reliability testing technology.

Planting Seeds

In the late 1970's, NSA attempted to install wafer level reliability testing. The IC manufacturers would not accept this concept. The idea of stressing test structures to obtain their lognormal failure distribution was repugnant to say the least. Most suppliers advised that they would not supply wafers if those kinds of tests were to be done!

In the early 1980's, Paul Losleben moved from NSA to DARPA and again asked this author to establish wafer level reliability testing for specific application for the MOSIS program. The microelectronics industry has a long history of resisting ideas forced upon them. Therefore, this author believed our industry should be nurtured in the value of performing wafer level reliability testing.

The technical leaders of the IC industry were invited to send their key manufacturing people to talk and think about these ideas in a workshop, open by invitation only. Only U.S. companies were permitted to attend. Stanford University and University of California (Berkeley) co-sponsored the workshops. These universities also contributed graduate students to work (for travel expenses) and participate in open, free discussion with our industry technical leaders.

Initial Results

The first workshop concluded that although this was an interesting idea, it would not work; it was just plain impractical; who would think of doing a probe test on the wafer for 100's of hours, etc. But there was a glimmer of hope; there was a strong agreement that the workshop should be held again.

The seeds did fall into fertile minds and ideas slowly became plans of actions. Why? The time was right for this idea. With the increased drive for higher performance VLSI devices, we were awakened to new reliability limitations. We were demanding performance approaching the "Reliability Materials Limit" illustrated in Fig. 1. In the 1960's and 1970's there was a wide "Margin of Reliability Assurance." Our designs and processing could be sloppy but the devices still yielded and were reliable. But in the 1980's and beyond, the "Device Rules and Device Performance" will be pushing up against these materials limits.

Our attention was focused of scaling algorithms essential for our moves from MSI to VLSI. The new failure mechanisms restricted and required modifications to these algorithms. Murray Woods of Intel frequently jolted our minds about the problems of 1 μm device reliability.

At the end of the second workshop, the question was not that wafer level testing could not be done, but where was it economic to do such tests? The seeds had germinated and the concept was healthy and growing.

New products use advanced design rules and new technologies. This is the ideal place to evaluate wafer level reliability testing. The results were staggering (Fig. 2). By applying reliability testing on the wafer, not on packaged devices, it is possible to rapidly solve reliability problems that are found to exist with the design rules and the processes. A normal qualification, as specified in MIL M 38510 or MIL STD 883, requires approximately 12 weeks to complete after the devices have been produced and assembled. By this technique, in the 1970's the average process/product development cycle time was 40 months. Today that has been shortened to an average of 30 months, for far more complex devices and processes.

By the end of the fourth workshop in 1985, it is clear that these ideas not only apply to process/product development, but are critically and economically important in high volume manufacturing.

There are still issues to be resolved. Can these wafer level reliability tests be correlated to traditional packaged reliability tests? Do both of these tests correlate to field reliability in VLSI devices? These questions must be addressed for each failure mechanism. The data reported at the 1985 workshop show that wafer level reliability tests do correlate to both packaged accelerated stress tests and to limited field data.

With or Without Wafer Level Reliability Testing

This comparison is complex (Fig. 3). There are many issues to consider. Each manufacturer and each user must understand the benefits and obligations of wafer level reliability testing. Figure 3 addresses the benefits. What are the obligations? Any new approach requires changes, new learning, acceptance of new values, job restructuring, etc.

If either device users or IC manufacturers value inexpensive, controlled manufacturing, then they will want to have wafer level reliability testing on their products (Fig. 4). For the U.S., this is KEY to our Strategic World Leadership. Today much is written about the fact that very few memory devices are made in the U.S.A. Should there be a national emergency that would separate us from our major sources of memory devices, we would be at a great disadvantage. By a broad implementation of wafer level reliability testing we can regain the necessary strategic role as VLSI leaders.

CAR

At the 1984 workshop we coined a new acronym, CAR. This stands for Computer-Aided Reliability. All industries have seen the benefits of CAD and CAM. Today designers can rapidly create very interesting, useful devices with the CAD tools. But in the area of reliability, few of the reliability engineers fully understand each of the failure mechanisms and their implications to the wide variety of VLSI designs. How

then can we educate the multitude of designers so that they will not create monstrous reliability problems in future devices?

The only possible way to avoid future device chaos is to provide a CAR tool which can be integrated with CAD. This is not easy. Most of our failure mechanism mathematical models are crude at best. Most are tested by holding all variables constant except one. Unfortunately, devices have many parameters varying at the same time. CAR will cost money. But the value received will be even greater than the value of CAD. Will the U.S. accept the challenge or will it have to learn from other nations? Some activity is beginning, using internal funds, because our VLSI manufacturers know that the return justifies the investment. The workshop will continue to nurture this idea.

1986 Workshop

What is holding back the U.S. aerospace electronics industry? That is clearly a question for many to ponder. We encouraged aerospace users and manufacturers to participate actively in the 1986 Wafer Reliability Assessment Workshop. In the past only a few have attended. Does a meeting have to be visibly sponsored by a contracting agency to attract attention? Clearly that is important, but advances can also occur outside of funded meetings and funded activities!

The Wafer Reliability Workshops break the form of the traditional meetings. Clearly they have helped nurture a clear advance in reliability control and process control technology of doing accelerated life testing on the wafer. They are on the leading edge of the concept of CAR.

Margin of Reliability Assurance

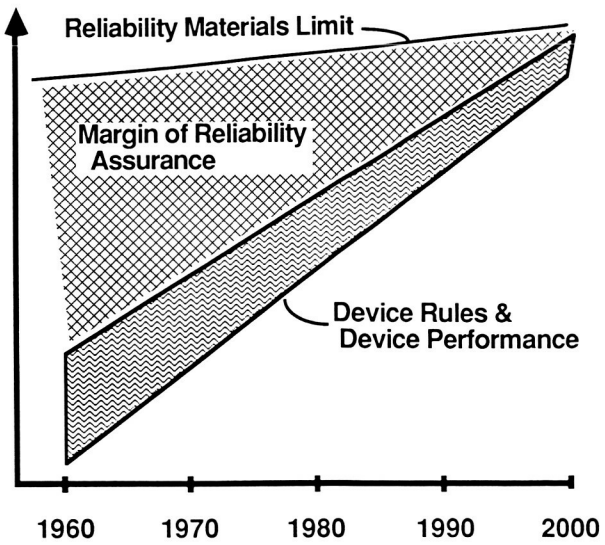

Figure 1

Process/Product Development Cycle Time

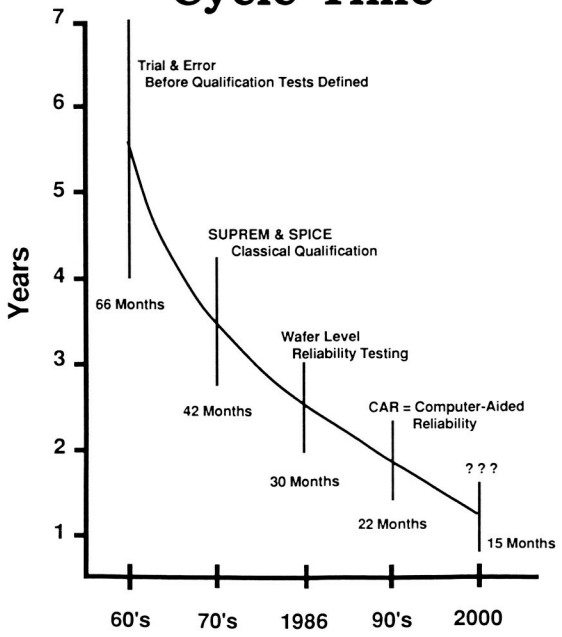

Figure 2

Wafer Level Reliability Testing

Without	With
❖ Qual Test - 12 Weeks 200 Devices	❖ Qual Test - *On the wafer* - hours/days
❖ Very Slow Corrective Action - Years	❖ Fast Turn-Around Corrective Action - Weeks
❖ Not Competitive Slow Development	❖ 30 months for 80386, etc.
❖ Delays & Cost Overruns	❖ Key to "Just in Time" Manufacturing
❖ Adverse Reliability Surprises	❖ Controlled Device Manufacturing - No Surprises
❖ Cost - Expensive	❖ Cost - Inexpensive
❖ Yields - Variable or Zero	❖ Yields - High
❖ Who Does It? MIL STD Users	❖ Who Does It? Commerical VLSI Makers & Computer Industry

Figure 3

What is holding back the U.S. Aerospace Electronics Industry?

Figure 4