NASA CR-180829
September 1987

SPACE STATION POWER SEMICONDUCTOR PACKAGE DEVELOPMENT

Power Technology Components
Microsemi Corporation
23201 South Normandie Avenue
Torrance, California 90501

Prepared for:

National Aeronautics & Space Administration
NASA-Lewis Research Center
Contract NAS3-24662

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16. Abstract

Under this program a package for high power switching semiconductors for the Space Station was designed and fabricated. The package includes a high voltage (600 Volts) high current (50 Ampere) NPN Fast Switching Power Transistor and a high voltage (1200 Volts), high current (50 Ampere) Fast Recovery Diode.

The package features an isolated collector for the transistors and an isolated anode for the diode. Beryllia is used as the isolation material resulting in a thermal resistance for both devices of .2 degrees per watt.

Additional features include a hermetical seal for long life--greater than 10 years in a space environment. Also, the package design resulted in a low electrical energy loss with the reduction of eddy currents, stray inductances, circuit inductance and capacitance.

The required package design and device parameters have been achieved. Test results for the transistor and diode utilizing the Space Station package is given.

17. Key Words (Suggested by Author(s))
beryllia - circuit inductance - eddy currents - fast recovery - fast switching - isolated anode - isolated collector - stray inductances - thermal resistance

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1.0 SUMMARY

The requirement of this contract, advanced development of the packaging for high power switching semiconductor devices, (transistors, diodes, MOSFET devices, GTO thyristors, etc.) is an integral part of the overall program at NASA Lewis Research Center to build high power distribution systems for the initial Space Station and future space craft.

As specified in the statement of work, the emphasis of the task to be performed is on the design, fabrication and testing of suitable packages to house power semiconductor devices, while conforming to the constraints of the Space Station, defined in terms of the package thermal, electrical and mechanical parameters. The package concept has to be adaptable to various types of devices as well as be scalable to higher and lower power levels.

A transistor and diode with specified electrical ratings and characteristics are used as a vehicle to establish and test the package design. The chip procurement for these devices was an option, but considering the experience in high current and high voltage device design and manufacturing at Power Technology Components (P.T.C.) and the advantage of improved compatibility, complete device design has been performed for both transistor and diode. The major physical dimensions of the two chips, the external package outline and most of the internal assembly components are identical and conform to the same or similar chip fabrication and assembly techniques.

The main common features of both devices are:

1. High temperature glass passivated junctions.

2. Chip surfaces coated with high voltage junction coating.
3. All of the interior surfaces of the assembly cavity are vacuum process coated with Parylene.
4. All electrical, thermal and mechanical interfaces are metallurgically bonded.
5. Thermal conduction accomplished across a single surface.
6. Hermetically sealed in nitrogen.
7. Electrically isolated package.
8. Thermal resistance junction to case 0.2°C/W, typical.
9. Power dissipation greater than 250W at 75°C.

Major electrical ratings and typical characteristic requirements:

Transistor

Collector Base voltage	600	volts
Collector Emitter voltage (sustaining)	500	volts
Gain Rated Coll. current	50	ampere
Continuous Coll. current	100	ampere
Switch time (off) (at rated current)	3,0μs	

Diode

DC Blocking voltage	1000	volts
Average forward current	50	ampere
Peak surge current	600	ampere
Reverse Recovery (at rated current)	0.5μs	

All of the major package design features and test parameters as well as the device characteristics have been met or exceeded. The exceptions are elevated temperature (100°C) diode leakage currents and reverse recovery time.

2.0 INTRODUCTION

Nasa Lewis Research Center has in the past been instrumental in the development of power semiconductor components for space power distribution. These components include bipolar power transistors and fast switching power diodes. These devices are now commercially available. The Lewis program with Westinghouse developed the D60T/D62T capable of 50 amperes and 500 volts with switching frequencies of 20 to 50 KHZ.

P.T.C., under contract to Lewis, previously developed two high voltage, high current fast recovery diodes. These diodes are now commercially available as P.T.C.'s PTC923 (50A) and PTC953 (130A) diodes. The previous device development program at Lewis, however, concentrated on chip development and did not address the problem of packaging high current, high voltage semiconductor devices. The devices developed were encapsulated in existing power semiconductor packages. These packages were designed for terrestrial applications, where weight, size and isolation were not problems.

The benefits of high voltages and high frequencies can reduce conductor and magnetic material weight. The power semiconductor devices themselves would need a new type of package to make them comply to the weight reduction program for space flight.

The current development program is a program to develop a package to house both a high current, high voltage transistor and a high voltage, high current, fast recovery diode in an isolated housing.

The transistor specifications call for a 50 ampere gain of

12 at 2.5 volts, and a sustaining voltage of 500 volts. The diode specification calls for a 50 ampere forward voltage of 1.5 volts and a reverse voltage of 1000 volts with a reverse recovery time of 500 nanoseconds at 50 amperes.

The 50 ampere and 500 volt requirement defined the design limitations of the package. The resultant package outline is larger than required for a 50 ampere diode, since it was determined that the chip design in the package could accommodate a 1000 volt, 125 ampere fast recovery diode. This report will describe a 50 ampere diode as required by the contract.

3.0 CHIP DESIGN

3.1 General

The major chip design features for both the transistor and diode are based on previous designs utilized at P.T.C.. Two power diodes rated at 1200 volts, 50 and 150 amperes were developed for NASA under contracts NAS3-22539 and NAS3-23280. Large area (up to .550 inch square) darlington transistors with ratings up to 1000 volts and 100 amperes were developed and fabricated for motor control applications.

To avoid the detailed matching of chip characteristics for paralleled chip assemblies, in all of these devices, a single chip has been used successfully. The same approach was chosen for this project. To take full advantage of the package dimensions, as well as provide for the maximum thermal and power characteristic evaluation, the largest area transistor and diode chips that could be accommodated in the package, have been designed. Hexagonal shape chips help to maximize the use of circular package design and allow the use of conventional processing by circular saw cutting wafers into chips.

The large chip size imposes stringent requirements on the uniformity of the silicon starting material. To obtain homogenous distribution of doping impurities, high minority carrier lifetime and low oxygen and carbon content, neutron transmutation doped, float zone processed silicon is used.

3.2 Transistor

The transistor chip is an NPN triple diffused, glass passivated mesa, with solderable metallization on the collector side. The base and emitter metallization is aluminum which

enables wire attachment by ultrasonic wire bonding. Heavily doped N^+ region in the collector gives the chip its mechanical strength to endure the handling during the manufacturing processes. This layer has no bearing on the operation of the transistor and constitutes a negligible series resistance. The lightly doped collector layer (N^-) determines the voltage capabilities of the transistor; its thickness increasing as the breakdown voltage rating (V_{CBO}) of the transistor increases.

The dimensions and impurity concentration of the P-layer base affect the switching time, emitter base voltage and gain related characteristics.

The emitter N^+ layer and its surface area and geometry configuration determines the gain and current carrying capability of the transistor. (Figure 1)

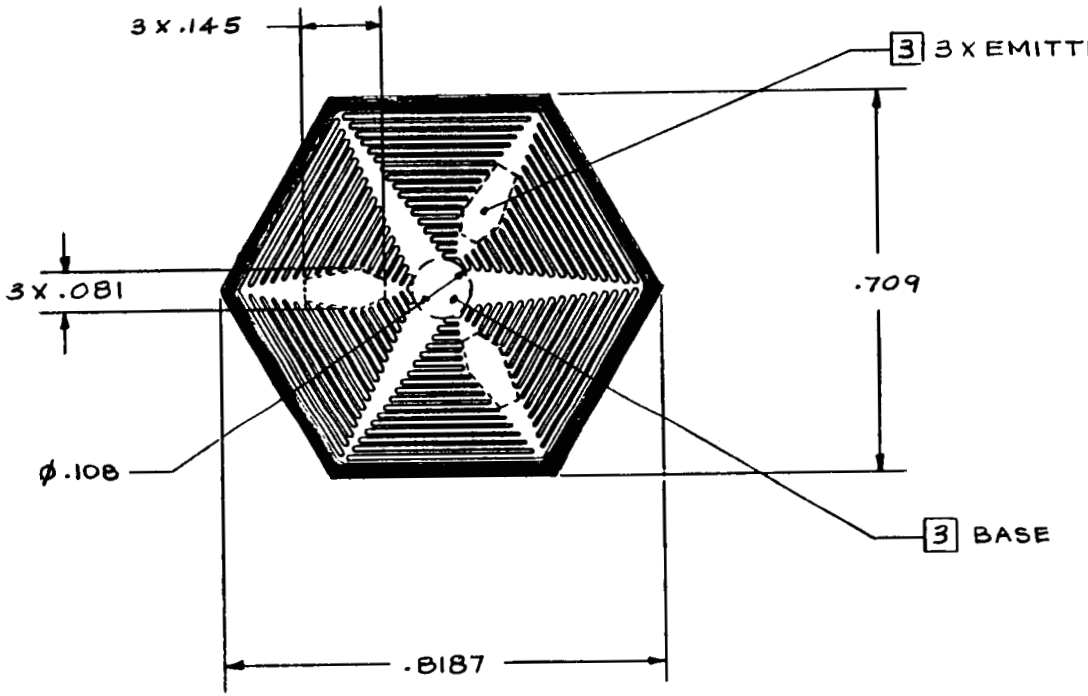
3.2.1. Static Characteristics

In any transistor design the basic and initial considerations are those of maximum voltage and current handling capabilities. These are the static or dc characteristics of the device.

3.2.1.1 Voltage

The requirement is for the minimum base-collector breakdown voltage (V_{CBO}) to be 600 volts. The collector-emitter sustaining voltage ($V_{CEO}(sus)$) is specified at 500 volts.

V_{CBO}. Based on previous experience and confirmed by calculations, 60 ohm cm resistivity starting material was specified. In the triple diffused transistor structure it forms the undiffused collector region and during the reverse bias conditions, will support the specified voltage.



2 PHOTOMASK SET	
DWG. NO.	DESCRIPTION
41-0003-820	MASTER
41-0003-821	EMITTER
41-0003-822	MOAT
41-0003-823	OXIDE REMOVAL
41-0003-824	METAL REMOVAL

Figure 1

4. PART DESCRIPTION: TRIPLE DIFFUSED MESA BIPOLAR TRANSISTOR.

[3] METALLIZATION: EMITTER AND BASE—ALUMINUM. AREAS BOUNDED BY DASHED LINES INDICATE PROPOSED ALUMINUM WIRE BONDING AREAS. COLLECTOR (ENTIRE BACK SURFACE)—NICKEL FOR SOFT SOLDER SURFACE MOUNTING.

[2] PHOTOMASK SET IS SHOWN IN CHART.

1. ALL DIMENSIONS ARE IN INCHES.

NOTES: UNLESS OTHERWISE SPECIFIED.

CAT 1 RELEASE

REFERENCES	SCALE: NONE	TRANSISTOR (.709 HEX)	WAS
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	4 PLACE DECIMAL (.XXXX) ± .005	CHKD. DATE 24 JUL 86	DWG. SIZE B 60-0013
	ANGLES ±.05°	APPD. DATE 7 AUG '86	

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When a reverse bias potential is applied between the collector and base or emitter terminals, the undiffused, n-type intrinsic resistivity layer and the diffused, p-type base layer are depleted of free charge carriers until the electric field generated by the negative donor ions in the collector and the positive acceptor ions in the base cancels the applied field. The depletion region spreads from the p-n junction as the applied potential is increased until either the intrinsic layer or the base layer is entirely depleted. For a graded base layer, assuming that the voltage blocking capability is limited only by the depletion width and not by junction passivation or ionization effects, the thickness of the depletion region, d, at a given applied voltage, Vbd, is given by the following formula:

$$d=(2KEoVbd/qNd)^{1/2} \qquad [1]$$

where Eo = permittivity of free space = 55.4 $\frac{\text{electron charges}}{\text{volt micrometer}}$

q = electron charge

K = dielectric constant of silicon = 12

Nd = donor concentration in 60 ohm cm n-type silicon

= 9 x 10exp13 atoms/cm3 = 90 atoms/cubic micrometer

For Vbd = 600 volts, the calculation indicates a depletion layer thickness of 95 micrometers. Therefore, the transistors undiffused, intrinsic collector layer must be at least this thick.

V_{CEO}(sus.). The minimum reverse bias collector to emitter avalanche voltage that occurs when the base terminal is floating or open, termed the sustaining voltage, V_{CEO}(sus), is less than the voltage allowed by collector base depletion that was used in

the calculation above. This is due to low level current gain of the carriers provided by the forward biased base emitter junction causing premature breakdown. An approximation of the sustaining voltage is given by the following relation:

$$V_{CEO(sus)} = V_{CBO}/(B)^{1/n} \qquad [1]$$

where V_{CBO} = the base collector breakdown voltage
= 600 volts

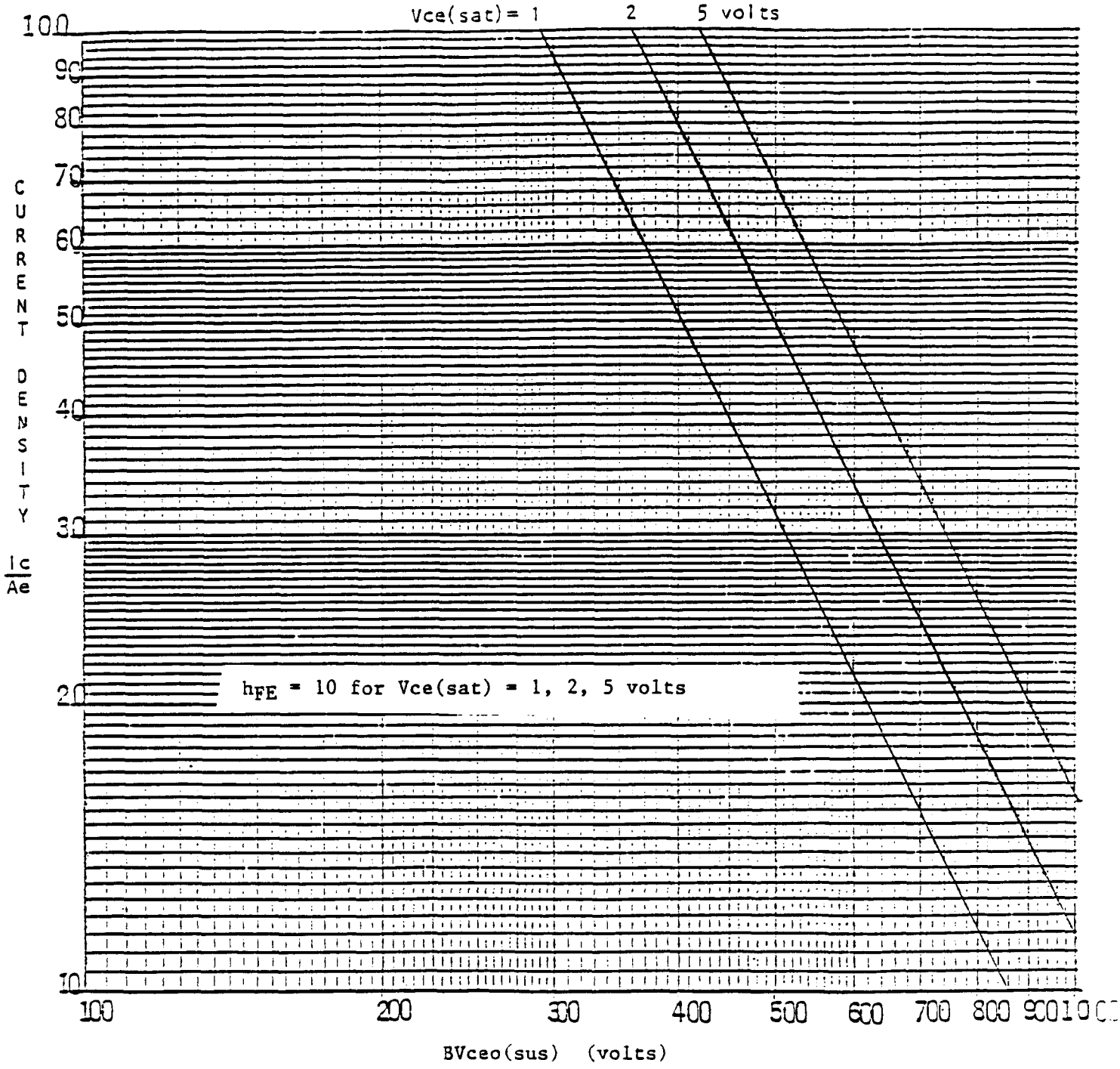
B = the low level current gain
= 2

n = a parameter of the avalanche multiplication factor M
= 4 for npn silicon transistors

The relation indicates that a sustaining voltage of 505 volts may be anticipated for a transistor with a base collector breakdown voltage of 600 volts. [1]

3.2.1.2 Current

As suggested above, a tradeoff does exist between maximum controllable current density and collector-emitter sustaining voltage. These considerations are based on the work done by P. L. Hower under NASA contract NAS3-18916. The current density is calculated by dividing the maximum gain rated current by the active emitter area. The specified on-state collector-emitter saturation voltage is 1 volt at 50 amperes and the gain of 8. For chip design shown on Figure 1, the current density J = 32.5 amperes/cm^2. [2] Reference to graph in Figure 2 of maximum controllable current density vs. collector emitter saturation voltage, indicates that greater than 500 volt capability can be expected at the given conditions and the required gain of 12 at



Maximum Controllable Current Density versus
Collector Emitter Sustaining Voltage [2]

Figure 2

50 amperes and 2.5 volts of $V_{CE}(sat)$. This is also confirmed by the results of two diffusion lot evaluations shown in Figure 3,a.

3.2.2 Dynamic Characteristics

In energy conversion applications the transistor is used in the switching mode. During the last few years, following the progress made in power transistor voltage and current handling capabilities, the attention has been directed to switching characteristics between "on" and "off" states and the associated power losses. Power switching transistor must handle large voltages during the off condition and large currents during the on conditions. The switching from one state to the other should happen as rapidly as possible; therefore, the transistor must respond to a driving signal, virtually instantaneously.

In designing transistors for maximum switching speed, the primary task is to evaluate and balance the trade-off effect on other device characteristic requirements. The major parameters affected are collector-base breakdown voltage, grounded-emitter saturation voltage, base resistance, emitter-base breakdown voltage, punch-through voltage and collector capacitance.

3.2.2.1 Physical Properties

For the triple diffused power transistor structure, the physical characteristics that had to be optimized are the emitter area, the P-type base layer and the N^- collector region.

To make the emitter area as small as possible for lower junction capacitance and still maintain the current carrying capability, three individual emitter cells connected in parallel have been utilized.

TRANSISTOR WAFER FAB. LOT EVALUATION

LOT #	INPUT MATERIAL N-	INPUT MATERIAL N+	DIFFUSION Xjb	DIFFUSION Xje	DIFFUSION Wb	DIFFUSION Ps base		Vcbo 300uA V	Vceo (SUS) Im=.2A Ic=.8A 2 MhY	lebo 1mA V	IC @ 4A/2.5V A	Vce (S) 50A/6.25A V	Vbe (S) 50A/6.25A V	Ts @ 50A IB1=2A IB2=4A uS	Tf @ 300V IB1=2A IB2=4A uS
	Ohm cm μ	μ	μ	μ	μ	Ohms/sq	Spec.	>600	>500	N/A	>50	<1.0	<1.3	<2.5	<.5
8051	60 94	145	28	16	12	54		716	606	14.0	54	0.38	1.60	0.8	0.50
8052	60 99	145	30	18	12	45		833	531	13.0	56	0.37	1.60	1.0	0.70

Figure 3a

DIODE WAFER FAB. LOT EVALUATION

LOT NO.	INPUT MATERIAL N-	INPUT MATERIAL P+	DIFFUSION N+		ELECTRICAL Average VR @ 100uA	Average VF @ 50A	Average Trr @ 50A
	Ohm cm μ	μ	μ	Spec =	>1000V	<1.5v	<500nS
016	35 117	147	17		1100	1.30	440
019	35 117	135	18		1200	1.42	384

Figure 3b

The impurity concentration and the metallurgical base width are directly related to the gain of the transistor, however, the speed at which the collector current rises during the turn-on phase, is inversely proportional to the gain. A compromise has been achieved by empirical adjustments of the base parameters during diffusion processing.

The turn-off switching of the collector current is physically related to the transistor region that has to support the voltage, the N^- collector region. The higher the transistor voltage rating, the longer it takes to turn it off.

Some of the physical parameter effects and electrical characteristic trade-offs can be seen in Figure 3, a.

3.2.2.2 Switching Times

The switching period between the two stable states consists of two transitional states: turn-on (t_{on}) to conduction and turn-off (t_{off}) to return the transistor to its cut-off state.

Turn-on of a transistor from its cut-off state is characterized in the delay time (t_d) to build up the collector current to 10% of its maximum value and the collector current rise time (t_r), measured from 10% to 90% of the maximum value.

At cut-off the collector base and base-emitter junctions are reverse biased. The transition from one state to the other requires a certain quantity of charge. As the base drive is initiated, the charges are supplied by the base current and the emitter-base capacitance is charged. The time to attain the charge is a delay in rise time.

The rise time of the collector current characterizes the speed of the transition to the conduction state. It is directly

related to the effective (not metallurgical) base width thickness. The rise time of the collector current is important in applications concerned with turn-on power losses.

Turn-off switching also is divided in two phases, although the distinction is purely electrical and does not correspond to any physical reference. In order to return the transistor to its cut-off state, all of the accumulated charges must be eliminated. By changing the polarity of the base drive, the base-emitter junction is reverse polarized. However, the fall of the collector current cannot occur until a sufficiently large portion of the stored charges in the collector have been removed.

The time interval from the base current reversal to the time the collector voltage has increased to 10% of its maximum value is defined as storage time (t_s), Figure 32. The storage time is related to the minority carrier lifetime in the base and collector regions. It is also largely dependent on the base drive circuits and certain circuit design techniques are used to limit this time considerably.

As the operating point of the collector current moves from the quasi-saturation to the linear portion of the load line it traverses through the active region into the off state. This turn-off portion is defined as collector current fall time (t_f). The fall time is of particular importance in applications with inductive loads because the majority of power losses occur during the end of storage time and especially during the fall time; therefore, it must be as short as possible. The fall time physically is related to the collector thickness and its

resistivity. The higher the collector region resistivity, the longer the fall time.

3.3 Diode

The diode design calculations and analysis were performed and proven under NASA contract NAS3-23280 and reported in final report No. CR168196. Although a new chip has been designed, increasing the area to fit the maximum space allocated in the package, the design approach remains the same. (Figure 4)

3.3.1 Physical Properties

The chip is fabricated from 35 ohm cm, float zone, neutron doped n-type silicon. The p-n junction terminates on the positive bevel of the moat and is high temperature glass passivated. The positive bevel mesa contouring allows the use of relatively low resistivity material. This improves the trade-off between blocking voltage, switch time and the forward voltage drop. A flash of evaporated gold (200-300 angstroms), deposited on the anode surface, in addition to the tri-metal (Al-Ti-Ni), improves the solderability, thereby reducing the contact resistance. The following parameters have been established and used to fabricate the device:

Starting material resistivity = 35 ohm cm

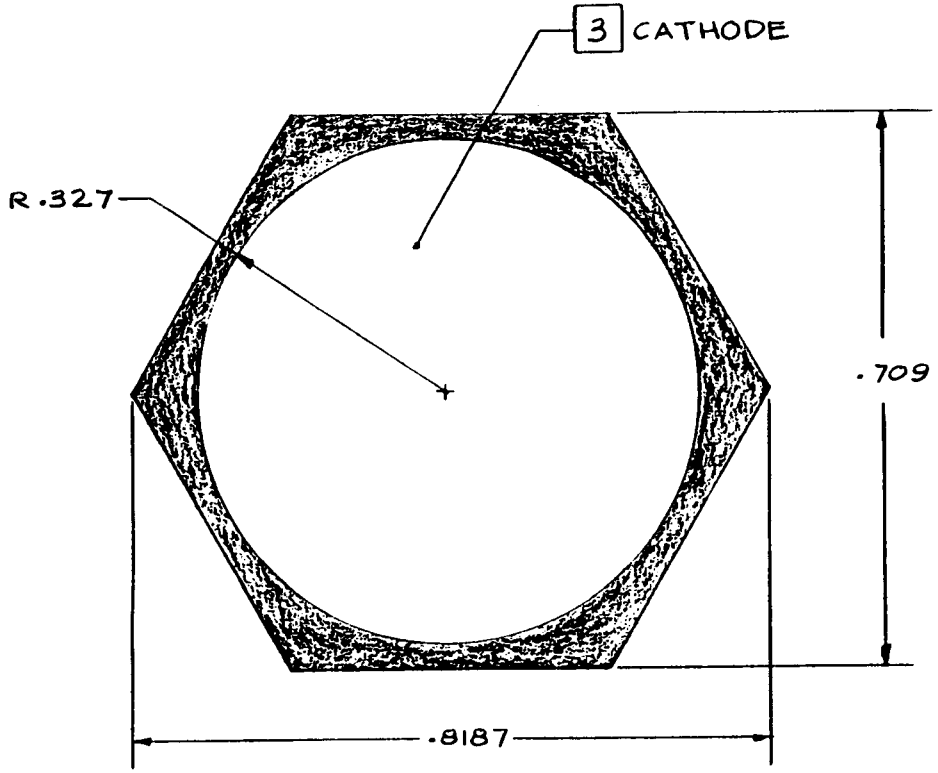
Background impurity conc. = 1.5×10^{14} atoms/cm^3

Anode surface impurity conc. = 2.5×10^{19} atoms/cm^3

p^+ anode junction depth = 140 microns

Depletion layer width @ 1250 V, is 92 microns

Grade constant of the p^+ layer = 1.29×10^{17} atoms/cm^3 [1]



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2 PHOTOMASK SET	
DWG. NO.	DESCRIPTION
40-0006-820	MASTER
40-0006-822	MOAT
40-0006-823	OXIDE REMOVAL
40-0006-824	METAL REMOVAL
40-0006-829	ALIGNMENT

Figure 4

CAT I RELEASE

4. PART DESCRIPTION: HIGH POWER DIODE, POSITIVE BEVEL MESA.
3 ENTIRE BACK SURFACE (ANODE) AND CIRCULAR FRONT (CATHODE) SURFACES ARE SOLDERABLE CONTACT AREAS.
2 PHOTOMASK SET IS SHOWN IN CHART.
1. ALL DIMENSIONS ARE IN INCHES.
NOTES: UNLESS OTHERWISE SPECIFIED.

NASA NAS 3-24662		REFERENCES	SCALE: NONE
USED ON	NEXT ASSY	REVISION N/C	RELEASE
		REFER BOOK	

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(DIMENSIONS IN INCHES) TOLERANCES UNLESS OTHERWISE SPECIFIED
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4 PLACE DECIMAL (.XXXX) ± .005
ANGLES ± .05°

DIODE (.709 HEX)

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APPD.	DATE 7 AUG. '86	60-0014

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MILWAUKEE, WISCONSIN

FORM NO. 821

3.3.2 Electrical Characteristics

The blocking voltage (V_R) that can be theoretically achieved with this structure is approximately 1680 volts. The highest voltage obtained with this device to date is approximately 1400 volts with a typical average value of 1100 volts.

The reverse leakage current (I_R) is higher than specified, especially at elevated temperature. This is due to the larger chip area and gold diffusion. A typical leakage current value at rated voltage (1000v) at room temperature is approximately 100 micro amperes.

The forward voltage (V_F) is considerably better than specified due to large area higher current capability.

The reverse recovery (t_{rr}) time is the time lapse required for the diode to regain its reverse bias capabilities from a forward conduction condition, after it is abruptly reverse biased. The specification for the recovery time is at elevated temperature only (100°C) and on the average runs 150 to 250 nanoseconds higher than specified. At room temperature the readings are at or below the elevated temperature requirement of 500 nanoseconds at 50 amperes. Gold diffusion is used to reduce the minority carrier lifetime and increase the recovery speed.

Additional process and structure adjustments are required to further reduce the reverse recovery time, especially at the higher current specifications with increasing junction capacitance as the device area is increased.

In addition to the specified current rating requirements, the diode evaluation tests were increased to 125 amperes, as shown in Figure 36.

3.4 Evaluation

Every wafer fabrication lot prior to its release for assembly was evaluated by random chip selection, experimental assembly and electrical testing of the major characteristics V_R, V_F, t_{rr} for the diode and V_{CBO}, $I_C(sat.)$, $V_{CEO}(sus)$, $V_{CE}(sat.)$, $V_{BE}(sat.)$ and switching times for the transistor.

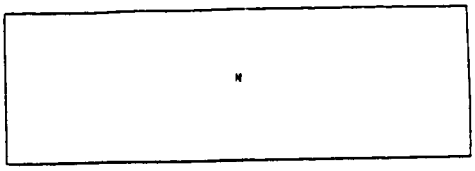
The sample chips were not assembled in the newly designed package but in a special assembly arrangement to eliminate any potential variables introduced by the new design. A sample of the wafer fabrication lot evaluations is shown in Figure 3, b.

Additional information of the diffused junction parameters is included to show the correlation of the calculated target values, actual measured values and the resulting "on the target" electrical characteristics. (Figure 3, a & b)

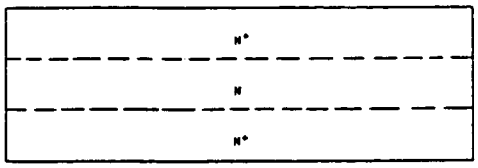
4.0 WAFER PROCESSING

Wafer fabrication processes are mostly conventional silicon processing procedures with minor modifications. These have been described previously in detail. Process flow diagrams, Figure 5, for the transistor and Figure 6 for the diode, outline the major fabrication steps with the appropriate cross sections of the devices.

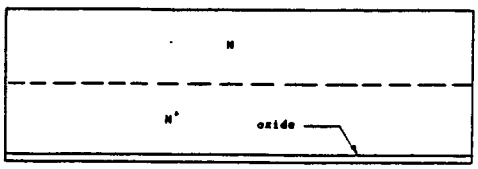
Neutron doped n-type silicon wafer



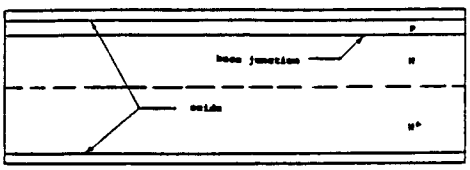
Phosphorus deposition and drive-in diffusion to form collector n+ layer



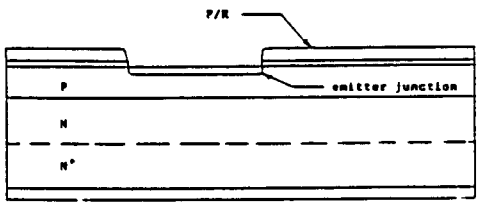
Single sided lap and polish. Oxidation and oxide removal from base side.



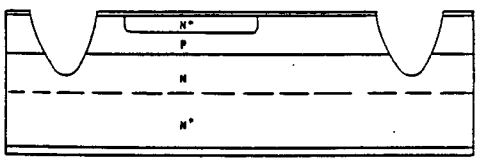
Boron deposition and drive-in diffusion to form p base layer



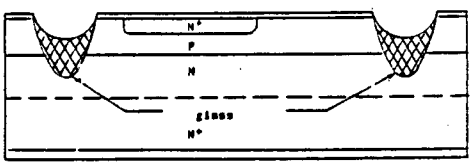
Photoresist mask, oxide etch, phosphorus deposition and drive-in to form n+ emitter pattern



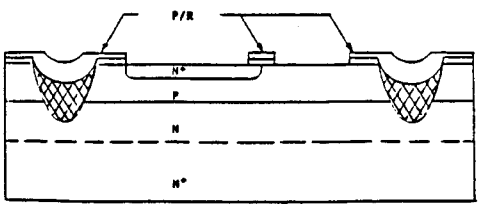
Photoresist mask, oxide etch and silicon etch to form collector-base junction termination



Hard glass passivation of pn junction in moat



Contact photoresist mask and oxide etch to define base and emitter regions



Collector 3-layer and base/emitter aluminum metallization

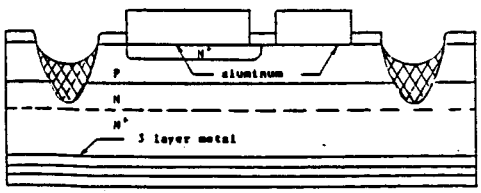
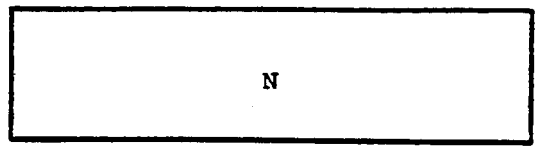
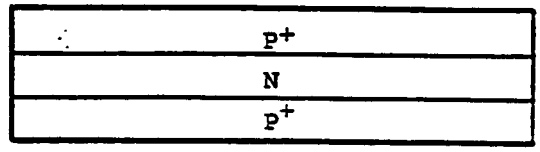


Figure 5, Triple-diffused Transistor Process Sequence Outline

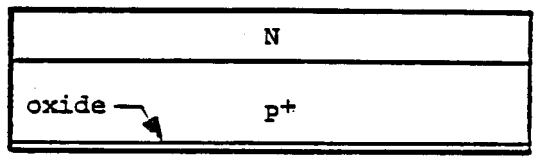
Starting material wafer, neutron doped N-type silicon



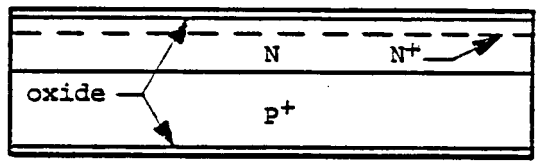
Boron deposition and drive in diffusion to form anode P^+ layer



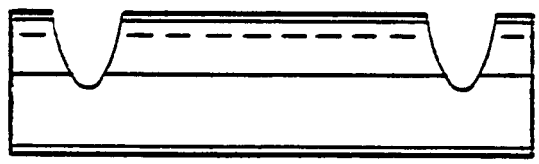
Single side lap & polish oxidation and oxide removal from cathode side



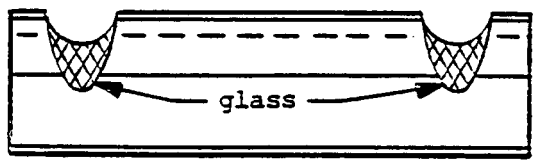
Phorphorus deposition and drive-in diffusion to form N^+ cathode layer



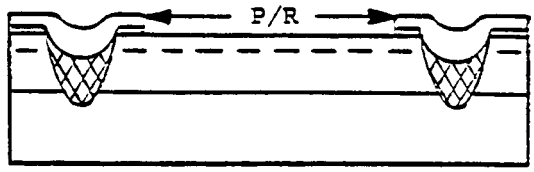
Photoresist mask, oxide and moat etch to form positive angle bevel



Hard glass passivation of the P/N junction in the moat



Contact photoresist and oxide etch to define anode and cathode areas



Anode and cathode three layer metallization

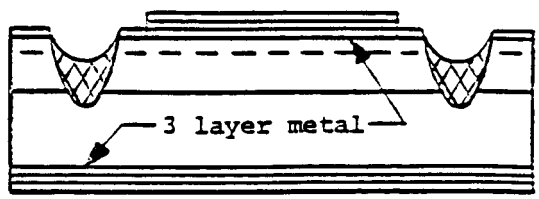


Figure 6, Diode Process sequence outline

5.0 PACKAGE DESIGN CONSIDERATIONS

5.1 Diode and Transistor Package Features

Space station semiconductor package design reflects some of the latest technology in high power semiconductor device material and processes. The package is designed to hermetically enclose the device and provide: 1) protection from space environment, ground handling and shuttle launch conditions, long term orbit Power Management and Distribution (PMAD) operation, 2) reliable electrical, thermal and mechanical interfaces and, 3) light weight and low volume construction. (Figures 7 and 8)

As many common piece parts as possible are shared by both transistor and diode, with the assembly methods nearly identical.

The package materials were selected to be compatible to Space Station environment as well as comply with the mechanical, electrical and thermal requirements of the semiconductor devices.

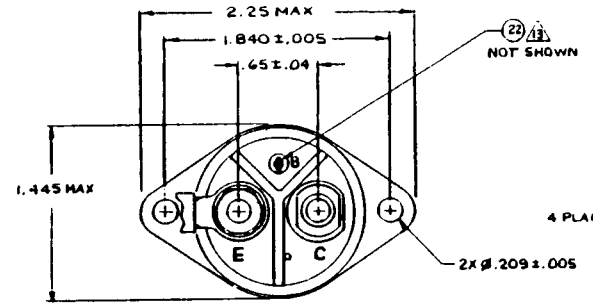
5.1.1 Electrical

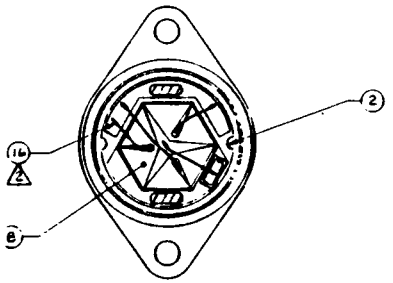
All electrically active components are isolated from the main body of the package. The insulation is designed to comply with the requirement to withstand a 2500 volt potential difference between the bottom plate and the collector of the transistor and the anode of the diode.

The material selection and the package structure features are designed to minimize electrical energy losses due to eddy currents, stray inductances and capacitances.

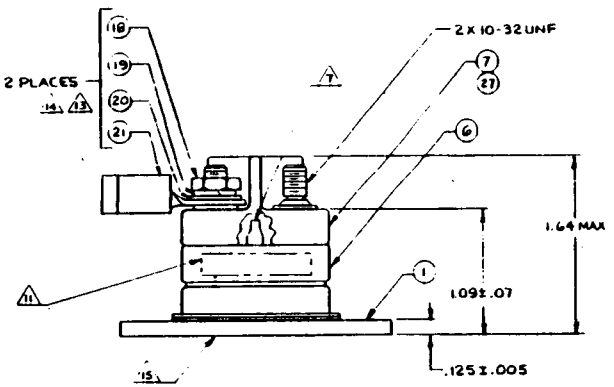
The following package features are designed to minimize energy losses:

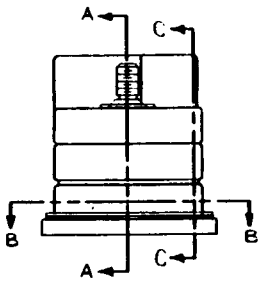
1. The package is single-ended with all electrical terminals on a single plane. This prevents coupling into the

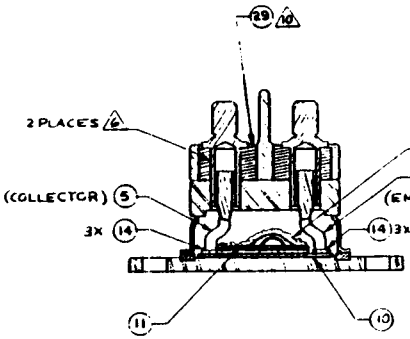




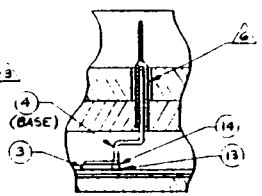
SECTION B-B







SECTION A-A



SECTION C-C

16. FINISHED ASSEMBLY SHALL BE HERMETICALLY SEALED AND MUST NOT LEAK MORE THAN 1×10^{-7} STD CC/SEC OF HELIUM ON A MASS SPECTROMETER AT ONE ATMOSPHERE PRESSURE DIFFERENTIAL.

15. BEFORE FINAL PLATING (NOTE 8) FLATTEN AND POLISH BOTTOM SURFACE

14. WHEN READY FOR USE, ASSEMBLE ITEMS 18 THRU 21 AS SHOWN AND TIGHTEN ITEM 18(NUT) TO 12 ±.5 INCH POUNDS.

13. ITEMS 18 THRU 22 (HARDWARE) ARE TO BE SUPPLIED WITH PART.

12. TEST PER REQUIREMENTS OF NASA CONTRACT NAS3-24662.

11. MARK PART NUMBER AND P.T.C. LOGO WHERE SHOWN WITH PERMANENT BLACK INK.

10. FILL CAVITIES IN ITEM 7 (PLASTIC CAP) WITH ITEM 29 (ENCAPSULATING COMPOUND) LEVEL OR SLIGHTLY BELOW TOP SURFACE OF ITEM 7.

9. ATTACH ITEM 7 (PLASTIC CAP) TO ITEM 6 (CAP) USING ITEM 27 (ADHESIVE)

8. AFTER PART IS SEALED AND BEFORE INSTALLATION OF ITEM 7 (PLASTIC CAP) PLATE ALL EXPOSED METAL SURFACES WITH ELECTROLYTIC COPPER PER MIL-C-14550B, 100 TO 200 MIN. THICK, FOLLOWED BY ELECTROLESS HIGH PHOSPHORUS NICKEL, 150 TO 200 MIN. THICK, 10% TO 12% PHOSPHORUS, FIDELITY BATH NUMBER 4875.

7. AFTER ASSEMBLING, BEFORE INSTALLATION OF ITEM 7 (PLASTIC CAP), AND BEFORE FINAL SEALING, COAT ENTIRE INSIDE SURFACE WITH ITEM 25 (PARYLENE). THEN BACK FILL WITH NITROGEN AT ATMOSPHERIC PRESSURE AND HERMETICALLY SEAL BY CRIMPING AND RESISTANCE WELDING FILLER TUBE AS SHOWN. SEAL LEAKAGE IS PER NOTE 5

6. CRIMP AND RESISTANCE WELD TERMINALS OF ITEM 6 (CAP) TO ITEMS 4 (BASE PIN) AND 5 ((CABLE) APPROXIMATELY WHERE SHOWN.

5. RESISTANCE WELD ITEM 6 ((CAP) TO ITEM 1 (BOTTOM PLATE). SEAL SHALL BE HERMETIC AND NOT LEAK MORE THAN 1×10^{-8} STD CC/SEC OF HELIUM ON A MASS SPECTROMETER AT ONE ATMOSPHERE PRESSURE DIFFERENTIAL

4. WELD RING OF ITEM 1 (BOTTOM PLATE) MUST BE FREE OF ANY ITEM 29 (ENCAPSULATING COMPOUND).

3. APPLY ITEM 29 (ENCAPSULATING COMPOUND) ALL AROUND ITEM 8 (TRANSISTOR) AND ITEM 16 (ALUMINUM WIRE).

2. ULTRASONIC WELD BOTH ENDS OF ITEM 16 (ALUMINUM WIRE) AS SHOWN.

1. ASSEMBLE BY TUNNEL FURNACE SOLDERING COMPONENT PARTS, ITEMS 1, 2, 3, 4, 5, 8, 10, 11, 13, 14 USING ASSEMBLY FIXTURES ITEMS 31 THRU 36.

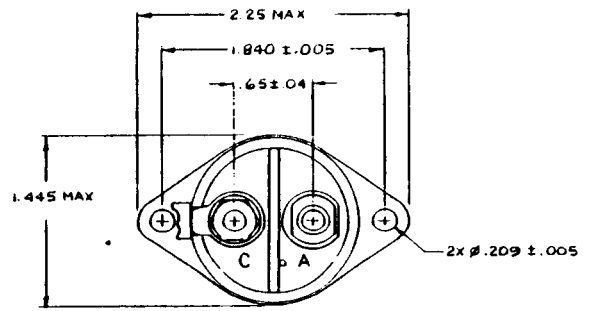
NOTES: UNLESS OTHERWISE SPECIFIED

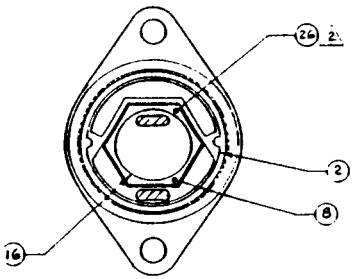
Figure 7

SEE SEPARATE PARTS LIST PL50-0267
(SHEET 2 AND 3)

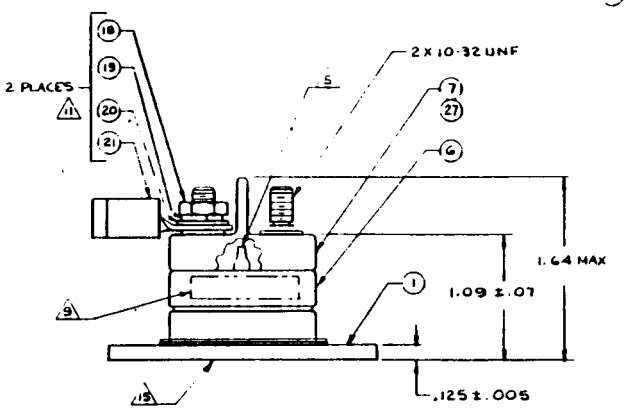
CATAGORY 1 RELEASE

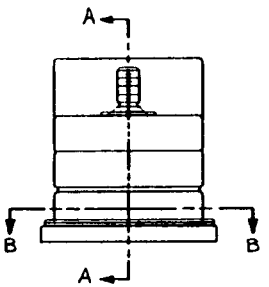
REFERENCES	SCALE: 2/1	SPACE STATION TRANSISTOR ASSEMBLY		WAS
REVISION N/C	RELEASE	NASA NAS3-24662		ALLEN-BRADLEY
		USED ON	NEXT ASSY	
		DR	DATE 26 JUN 87	SHEET 1 OF 3
		CHKD	DATE 29 JUN 87	SIZE B 50-0267
		APPD	DATE 26 JUN 87	

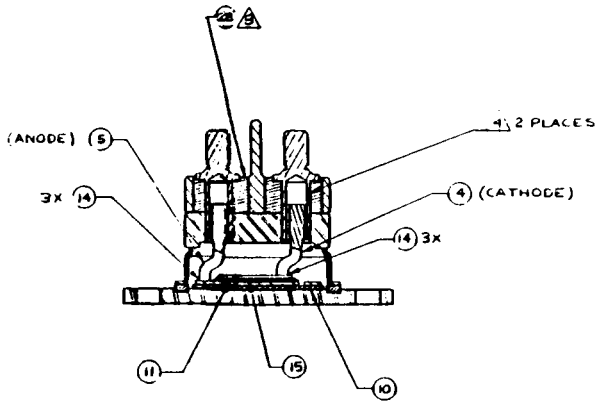




SECTION B-B







SECTION A-A

16. FINISHED ASSEMBLY SHALL BE HERMETICALLY SEALED AND MUST NOT LEAK MORE THAN 1×10^{-7} STD CC/SEC OF HELIUM ON A MASS SPECTROMETER AT ONE ATMOSPHERE PRESSURE DIFFERENTIAL.

△12 BEFORE FINAL PLATING (NOTE 6) FLATTEN AND POLISH BOTTOM SURFACE

△11 ITEMS 18 THRU 21 (HARDWARE) ARE TO BE SUPPLIED WITH PART. WHEN READY FOR USE ASSEMBLE AS SHOWN AND TIGHTEN ITEM 18 (NUT) TO 12±.5 INCH-POUNDS.

10 TEST PER REQUIREMENTS OF NASA CONTRACT NAS3-24662.

△9 MARK PART NUMBER AND R.T.C. LOGO WHERE SHOWN WITH PERMANENT BLACK INK.

△8 FILL CAVITIES IN ITEM 7 (PLASTIC CAP) WITH ITEM 28 (ENCAPSULATING COMPOUND) LEVEL WITH OR SLIGHTLY BELOW TOP SURFACE OF ITEM 7.

7 ATTACH ITEM 7 (PLASTIC CAP) TO ITEM 6 (CAP) USING ITEM 27 (ADHESIVE).

6 AFTER PART IS SEALED AND BEFORE INSTALLATION OF ITEM 7 (PLASTIC CAP) PLATE ALL EXPOSED METAL SURFACES WITH ELECTROLYTIC COPPER PER MIL-C-14550B, 100 TO 200 μIN. THICK, FOLLOWED BY ELECTROLESS HIGH PHOSPHORUS NICKEL, 150 TO 200 μIN. THICK, 10% TO 12% PHOSPHORUS FIDELITY BATH NO. 4875.

△5 AFTER ASSEMBLING, BEFORE INSTALLATION OF ITEM 7 (PLASTIC CAP) AND BEFORE FINAL SEALING, COAT ENTIRE INSIDE SURFACE WITH ITEM 25 (PARYLENE). THEN BACK FILL WITH NITROGEN AT ATMOSPHERIC PRESSURE AND HERMETICALLY SEAL BY CRIMPING AND RESISTANCE WELDING FILLER TUBE AS SHOWN. SEAL LEAKAGE IS PER NOTE 3.

△4 CRIMP AND RESISTANCE WELD TERMINALS OF ITEM 6 (CAP) TO ITEMS 4 AND 5 (CABLES) APPROXIMATELY WHERE SHOWN.

3 RESISTANCE WELD ITEM 6 (CAP) TO ITEM 1 (BOTTOM PLATE). SEAL SHALL BE HERMETIC AND NOT LEAK MORE THAN 1×10^{-8} STD CC/SEC OF HELIUM ON A MASS SPECTROMETER AT ONE ATMOSPHERE PRESSURE DIFFERENTIAL.

△2 APPLY ITEM 26 (JUNCTION COATING) ALL AROUND TO EXPOSED PORTIONS OF ITEM 8 (DIODE).

1 ASSEMBLE BY TUNNEL FURNACE SOLDERING COMPONENT PARTS ITEMS 1, 2, 4, 5, 8, 10, 11, 14, 15, 16 USING ASSEMBLY FIXTURES ITEMS 31 THRU 36.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 8

SEE SEPARATE PARTS LIST PL50-0268
(SHEET 2 AND 3)
CATAGORY 1 RELEASE

REFERENCES	SCALE 2/1	SPACE STATION DIODE	WAS
NEXT ASSY	REVISION RELEASE	ASSEMBLY	ALLEN-BRADLEY MILWAUKEE WISCONSIN
		NASA NAS3-24662	
		USED ON	NEXT ASSY
		DR	DATE 25 JUN 87
		CHKD	DATE 29 JUN 87
		APPD	DATE 26 JUN 87
		SIZE D	50-0268
			SHEET 1 OF 3

inherent shorted turns. The conventional double-ended package for power semiconductors has a "shorted turn" problem that must be considered when analyzing their energy loss profiles. This problem presents itself, by looking at the transformer action of the various package components. The secondaries or "shorted turns" that cause losses are conductive rings used to manufacture the package, such as glass-to-metal or metal seals or weld rings. This problem is diagrammed in Figure 9.

There are two ways to eliminate coupling into the shorted turn. One obvious way is to eliminate the rings or open them so they cannot conduct. This method is not practical. The second way is to terminate the package on one plane. This method prevents coupling even when the rings are present, see Figure 10.

2. All electrical contacts between internal conductors and the external terminals are crimped and resistance welded.

3. Stranded internal power conductors (cables) aid high frequency electrical conduction by skin effect.

4. Large, pure copper (oxygen free high conductivity) power conductors minimize electrical resistance.

5. All conductors are minimum length and maximum diameter to minimize circuit inductance.

6. Insulators have high dielectric strength and low dissipation factor.

5.1.2 Electrical/Mechanical

At the top of the diode package are two high power, threaded copper, stud terminals for anode and cathode connection. At the base of each stud terminal is a jam taper cone, which provides an interference fit with the ring tongue terminal inside diameter,

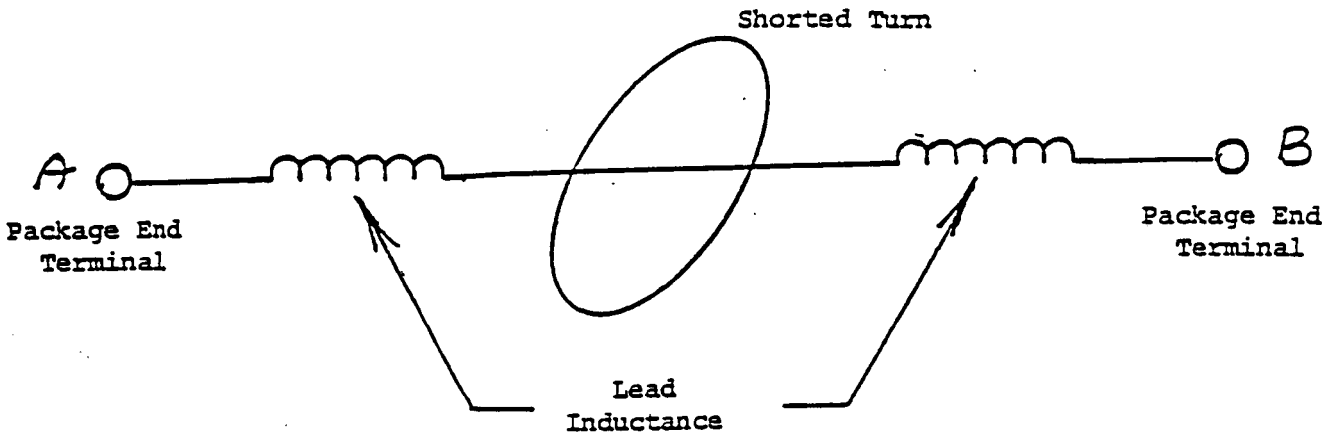


Figure 9

Simplified schematic diagram of a double-ended package with a short-ended turn as indicated.

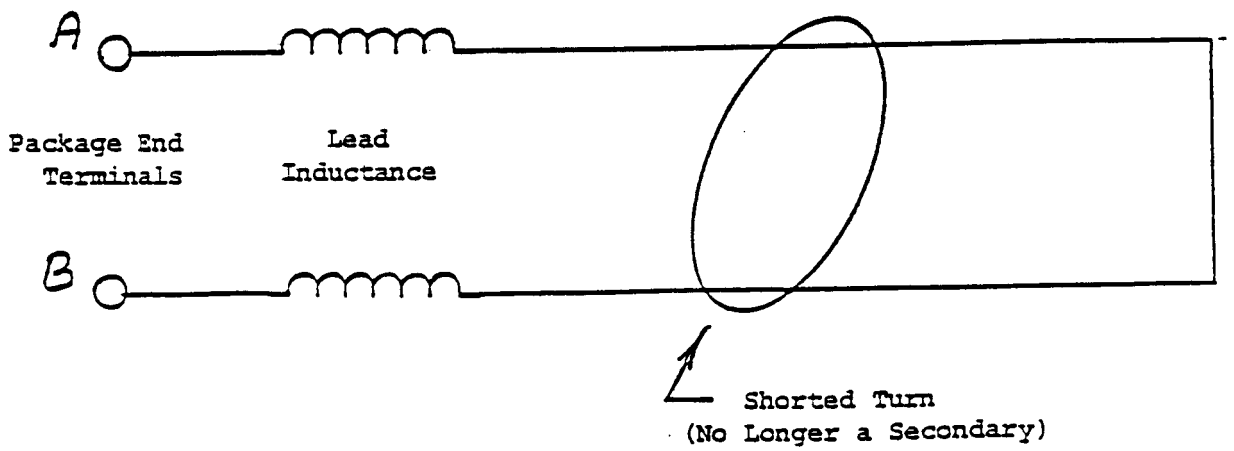


Figure 10

Schematic of single-ended package

thereby, reducing electrical contact resistance. It also prevents the ring tongue terminal from rotating.

The ring tongue terminal and American Standard No. 10 stainless steel hardware is supplied. To provide a secure and reliable electrical/mechanical connection without damage to the soft copper stud, the following procedure is recommended:

1. Loosely assemble ring tongue terminal, lock washer, flat washer and nut as shown in drawing 50-0268.

2. Center inside diameter of ring tongue terminal on jam taper cone and hold in place by hand.

3. Center flat washer to ring tongue terminal outside diameter and hand tighten nut.

4. Torque nut to 12 inch-pounds $\pm$ 0.5 inch-pounds.

The plain nut, NAS 671C10 is a small pattern type. It allows enough clearance from the electrical barrier on the plastic cap to insert a socket or nut driver. The nut can be easily tightened to the torque specified with an 11/32 socket and a torque wrench reading in inch-pounds.

The transistor package has two stud terminals identical to the diode package. They are the emitter and collector connections. Information and description of hardware pertaining to the diode package also applies. In addition there is a smaller flattened and pierced terminal. It is the base connection and mates with the insulated terminal provided.

Terminals on the transistor package are spaced in accordance with NEMA, General Standards For Industrial Controls and Systems, No. ICS 1-1983, Table 1-111-2, which calls for 900 volts peak working voltage. The package also exceeds the requirements of

Underwriters Laboratories UL1557, Standards for Safety, Electrically Isolated Semiconductor Devices for 600 volts RMS at the terminals. Creepage from the base terminal to either collector or emitter terminal is .575 inches. Creepage from any terminal to any conductive point on the package is .625 inches minimum. All paths through air are .438 inches minimum. The transistor package exceeds the 600 volt Underwriters Laboratories specification.

Terminals on the diode package are spaced in accordance with the same NEMA specification. The package is suitable for 1400 volts peak working voltage applied to the terminals. Creepage from terminal to terminal and from any terminal to any conductive point on the package is .625 inches minimum. All paths through air are .438 inches minimum. The package exceeds the requirements of the UL1557 specification.

5.1.3 Thermal

The prime consideration of the package design is the transfer of heat generated by the silicon chip of the device. A number of individual components and their metallurgical interfaces determine the thermal resistance of the device depending on the following parameters:

1. Material thermal resistance.
2. Material temperature.
3. Thickness of material parallel to the direction of thermal flow.
4. Area of material normal to the direction of thermal flow.

5. Amount of voids in interconnecting layers (solder).

6. Quality of interconnecting layers (solder).

7. Thermal flow (spreading) normal to the direction of major thermal flow.

In addition, the thermal performance of a package mounted to an external heat sink will depend on an intimate contact between the heat sink and the heat dissipating surface of the package.

Heat is conducted from the package across a single surface, the external surface of the bottom plate. It is surfaced and polished to remove any variation in flatness.

Internally, thermal resistance is reduced by using a beryllium oxide insulating substrate. Beryllia was chosen for mechanical strength, dielectric strength and its exceptionally low thermal resistance.

To reduce further thermal resistance and meet the $R\Theta_{JC}$ requirements of .2°C/W, the silicon device area is maximized, while the package size is minimized.

Thermal conductivity (K) is not a constant and does vary with temperature. To simplify calculations it is assumed to be constant. An average value is used for a temperature range from -65°C to 150°C. Plating, coatings and metallizations have been omitted from the calculations. Their thickness dimension is small, .0005 inches maximum and is included in the overall dimension of the component part to which they are applied. The magnitude of their thermal resistance is small enough to be disregarded.

Based on experience, it is assumed that all solder and braze joints contain 20% voids in the form of relatively small bubbles

evenly distributed throughout the joint. All heat is assumed to originate at the device junction located at the top of the device and is evenly distributed over the device area.

Junction temperature is determined by the total power dissipation in the device P_T, the ambient or case temperature T_C, and the thermal resistance $R\theta_{JC}$ from junction to case.

$$T_J = T_C + R\theta_{JC} P_T$$

The basic equation for the conduction of thermal energy is:

$$Q = \frac{KA}{L} \Delta T = \frac{KA}{L}(T_1 - T_2) \qquad [6]$$

where Q = heat flow/unit of time

K = thermal conductivity constant, W/cm, °C

A = area of thermal path, cm^2

L = length of thermal path, cm

T_1 = temperature of heat source, °C

T_2 = temperature of heat sink, °C

rewritten $$Q = \frac{T_1 - T_2}{L/KA} = \frac{T_1 - T_2}{R\theta_{JC}}$$

and $$R\theta_{JC} = \frac{L}{KA}$$

It is assumed that geometries are circular and spreading occurs at a 45° angle. The equation then becomes:

$$R\theta_{JCcircle} = \frac{L}{K\pi(r^2 + rL)} \qquad [6]$$

where r = radius of the circle

Thermal resistance calculated values for each assembly component of the package are shown in the following table. All components are assumed to be circular and are listed in the sequence of the thermal conductive path.

Package Assembly Component	Thermal Resistance RΘ in °C/W
Silicon Device	0.0119
Solder Interface	0.0066
Molybdenum Plate	0.0064
Silver-Copper Braze Interface	0.0005
Copper Conductor Plate	0.0067
Silver-Copper Braze Interface	0.0004
BeO Ceramic	0.0081
Solder Interface	0.0045
Copper Bottom Plate	0.0164

The resulting theoretical junction to case thermal resistance is approximately .062°C/W.

5.1.4 Mechanical

The final package design is shown in the assembly drawings, Figures 7 and 8.

In the following outline, each component part and the associated direct materials are identified by part number. A brief description of the structure and materials is included. (Figures 11 and 12)

Ceramic Plate Subassembly 50-0266-1

Four component parts are brazed together using a 72% silver, 28% copper alloy commonly referred to as BT material, melting at 780°C.

The four component parts are:

1. **Ceramic plate, 50-0251-1**--a flat, circular ceramic substrate made of 99.5% beryllium oxide, metallized with a pattern on both sides with a co-fired molybdenum-manganese alloy followed by nickel plating.

2. **Conductor plate, 50-0252-1**--a flat, crescent shaped OFHC copper, stamped, electrical conductor, nickel plated.

ITEM	QUAN.	PART NUMBER	DESCRIPTION	VALUE / TYPE NO.	VENDOR PART NO.	VENDOR NAME
1	1	50-0220	BOTTOM PLATE			
2	1	50-0266-1	CERAMIC PLATE SUBASSEMBLY			
3	1	50-0244	BASE INSULATOR			
4	1	50-0245	BASE PIN			
5	2	50-0256-1	CABLE			
6	1	50-0225-1	CAP			
7	1	50-0243-1	PLASTIC CAP			
8	1	60-0013	TRANSISTOR			
9						
10	1	50-0259-4	SOLDER PREFORM, ROUND			
11	1	50-0258-1	SOLDER PREFORM, HEXAGON			
12						
13	1	50-0257-1	SOLDER PREFORM, RECTANGLE			
14	7	50-0257-2	SOLDER PREFORM, RECTANGLE			
15						
16	A/R	50-0269-7	ALUMINUM WIRE			
17						
18	2		NUT, PLAIN, SMALL PATTERN, S/S	10-32UNF	NAS671C10	
19	2		WASHER, LOCK, SPLIT, S/S	#10	MS35338-138	
20	2		WASHER, FLAT, S/S	#10	MS15795-808	
21	2		TERMINAL, RING TONGUE		35273	AMP
22	1		TERMINAL, INSULATED	110 FASTON	2-520084-2	AMP
23						
24						

DRAWN BY	DATE	ENGINEER	DATE	CHIEF ENG.	DATE	NEXT ASSEMBLY	TITLE
[signature]	29 JUN 87			[signature]		—	SPACE STATION TRANSISTOR ASSEMBLY

A·B	SHEET 2 OF 3	QUALITY CATAGORY 1 RELEASE	USED ON NASA NAS3-24662	DWG. NO PL50-0267	REV N/C

Figure 11

ITEM	QUAN.	PART NUMBER	DESCRIPTION	VALUE / TYPE NO.	VENDOR PART NO.	VENDOR NAME
25	A/R		COATING, DIELECTRIC, POLYMER	.0015/.0010 THK	PARYLENE N	UNION CARBIDE
26						
27	A/R		ADHESIVE, STRUCTURAL	SPEED BONDER	325	LOCTITE CORP.
28						
29	A/R		ENCAPSULATING COMPOUND, SILICONE RUBBER	THERMASIL	TYPE I	TRANSENE CO.
30						
31	REF	50-0261-1	LOCATOR PLATE			
32	REF	50-0260	WEIGHT PLATE			
33	REF	50-0264	WEIGHT			
34	REF	50-0263-2	WEIGHT			
35	REF	50-0265	FURNACE BOAT			
36	REF		SPRING PIN, S/S	Ø3/32 x .50		
37						

DRAWN BY	DATE	ENGINEER	DATE	CHIEF ENG.	DATE	NEXT ASSEMBLY	TITLE
[illegible]	29JUN87			[illegible]	26 Aug 87	—	SPACE STATION TRANSISTOR ASSEMBLY

A-B	SHEET 3 OF 3	QUALITY CATAGORY 1 RELEASE	USED ON NASA NAS3-24662	DWG. NO PL50-0267 / REV N/C

Figure 11 (Continued)

ITEM	QUAN.	PART NUMBER	DESCRIPTION	VALUE / TYPE NO.	VENDOR PART NO.	VENDOR NAME
1	1	50-0220	BOTTOM PLATE			
2	1	50-0266-1	CERAMIC PLATE SUBASSEMBLY			
3						
4	1	50-0256-2	CABLE			
5	1	50-0256-1	CABLE			
6	1	50-0225-2	CAP			
7	1	50-0243-2	PLASTIC CAP			
8	1	60-0014	DIODE			
9						
10	1	50-0259-4	SOLDER PREFORM, ROUND			
11	1	50-0258-1	SOLDER PREFORM, HEXAGON			
12						
13						
14	6	50-0257-2	SOLDER PREFORM, RECTANGLE			
15	1	50-0259-1	SOLDER PREFORM, ROUND			
16	1	50-0254	MOLY, ROUND			
17						
18	2		NUT, PLAIN, SMALL PATTERN, S/S	10-32UNF	NAS671C10	
19	2		WASHER, LOCK, SPLIT, S/S	#10	MS35338-138	
20	2		WASHER, FLAT, S/S	#10	MS15795-808	
21	2		TERMINAL, RING TONGUE		35273	AMP
22						
23						
24						

DRAWN BY	DATE	ENGINEER	DATE	CHIEF ENG.	DATE	NEXT ASSEMBLY	TITLE
[illegible]	29JUN87			[illegible]	26AUG'87	—	SPACE STATION DIODE ASSEMBLY

A-B	SHEET 2 OF 3	QUALITY CATAGORY 1 RELEASE	USED ON NASA-NAS3-24662
		DWG. NO PL50-0268	REV N/C

Figure 12

ITEM	QUAN.	PART NUMBER	DESCRIPTION	VALUE / TYPE NO.	VENDOR PART NO.	VENDOR NAME
25	A/R		COATING, DIELECTRIC, POLYMER	.0015/.0010 THK	PARYLENE N	UNION CARBIDE
26	A/R		COATING, DIELECTRIC (JUNCTION COATING)		V-176	VISILOX SYSTS.
27	A/R		ADHESIVE, STRUCTURAL	SPEED BONDER	325	LOCTITE CORP.
28	A/R		ENCAPSULATING COMPOUND, SILICON RUBBER	THERMASIL	TYPE I	TRANSENE CO.
29						
30						
31	REF	50-0261-1	LOCATOR PLATE			
32	REF	50-0260	WEIGHT PLATE			
33	REF	50-0264	WEIGHT			
34	REF	50-0262	SPACER			
35	REF	50-0265	FURNACE BOAT			
36	REF		SPRING PIN, S/S	Ø 3/32 X .50		
37						

DRAWN BY	DATE	ENGINEER	DATE	CHIEF ENG.	DATE	NEXT ASSEMBLY	TITLE
[illegible]	29JUN87			[illegible]	26AUG87	—	SPACE STATION DIODE ASSEMBLY

A·B	SHEET 3 OF 3	QUALITY CATAGORY 1 RELEASE	USED ON NASA NAS3-24662

DWG. NO	REV
PL50-0268	N/C

Figure 12 (Continued)

3. **Conductor plate, 50-0252-2**--a flat semi-hexagonal shaped OFHC copper, stamped electrical and thermal conductor, nickel plated.

4. **Moly, hexagon 50,0253-1**--a flat .010 inch thick, hexagonal stamping, made of molybdenum with a layer of nickel cladding on both sides.

Bottom Plate 50-0220

An assembly of two component parts brazed together using a 72% silver, 28% copper alloy (BT). The two component parts are:

1. **Weld Ring**--an alloy C1010 steel ring, nickel plated.

2. **Plate**--a .125 thick flat semi-oval shaped stamping. It has a groove cut in it that fits the ring. It is made of OFHC copper. The finished assembly is nickel plated.

CAP 50-0225-1 and 50-225-2

An assembly of five component parts brazed together using a 72% silver, 28% copper alloy (BT). One component is used twice. The five different component parts are:

1. **Flange**--a deep drawn, .015 inch thick, cylindrical shape, made of alloy C1010 steel and nickel plated.

2. **Ceramic Insulator, glazed**--a solid cylindrical shaped insulator made of 92% minimum aluminum oxide, with four holes and coated with a thin layer of glass. It is 1.215 inches in diameter.

3. **Tube**--a short section of .125 inch diameter tubing made of OFHC copper.

4. **Base Terminal**--a short section of tubing, .110 inch diameter flattened and pierced at one end to form a male terminal that mates with a standard 110 female terminal. It is made of

OFHC copper.

5. **Emitter and Collector Stud Terminal**--threaded, semi-cylindrical shaped, electrical conductors made of OFHC copper. The tread size is American Standard 10-32 UNF.

The 50-0225-1 assembly contains all component parts and is used for the transistor package. The 50-0225-2 assembly does not contain the 110 base terminal and is used for the diode package.

Transistor 60-0013, and Diode 60-0014 Chip

Both devices are .010 inch thick, hexagonal silicon chips. The dimension across the flats is .709 inch. Back side metallization of both chips and front side of the diode is solderable nickel. For the transistor, the front side metallization is aluminum, for ultrasonic bonding of aluminum wires.

Plastic Cap 50-0243-1 and 50-0243-2

This is an injection molded solid, semi-cylindrical shaped insulator, 1.215 inches in diameter, with four holes. It has several ridges on the top surface that are electrical insulating barriers between the power terminals. The cap is made of a liquid crystal polymer, Vectra A130, from Celanese Engineering Resins, Inc. The material is stable up to 200°C. It is reinforced with 30% glass fiber, has a heat deflection temperature of 229°C at 264 PSI and has an Underwriters Laboratories flammability rating of UL-94 V-0. The dielectric strength is 1100 volts/mil. A very low shrink rate of .001 inch/inch allows molding of solid cross sections without warpage. This eliminates the need for making the part hollow thereby

eliminating air pockets. It has terminal identification of raised letters molded into the top surface. The 50-0243-1 part is used for the transistor package. The 50-0243-2 part has one less hole and a different ridge configuration. It is used for the diode package.

Cable 50-0256-1 and 50-0256-2

Three component parts are joined together by crimping and swaging. The three component parts are:

1. **Wire**--AWG 10 gage, stranded, OFHC copper wire.
2. **Terminal**--a short length of OFHC copper tubing.
3. **Ferrule**--a short length of a different size OFHC copper tubing.

The ferrule is crimped to the wire by squeezing both together, maintaining a cylindrical shape, until both are a solid mass. The terminal is crimped to the wire by a similar method. It is then swaged into a flat "S" bend shape.

A quantity of two of the 50-0256-1 cables are used in the transistor package. One each of the 50-0256-1 and 50-0256-2 are used in the diode package.

Aluminum Wire 50-0269-7

Twenty five mil diameter wire made of 99.99% pure aluminum is used only in the transistor package.

Moly, Round 50-0254

Circular stamping, .020 inch thick, .625 inches in diameter, made of molybdenum with a layer of nickel cladding on both sides. It is used only in the diode package.

Solder Preform, Round 50-0259-4

Circular stamping, .002 inches thick, 1.150 inches in diameter. made of 95.5% lead, 2.5% silver and 2.0% tin alloy.

Solder Preform, Hexagon 50-0258-1

Hexagonal stamping, .002 inch thick, of same alloy as above.

Solder Preform, Rectangle 50-0257-1

Rectangular stamping, .002 inch thick, .100 inches x.250 inches alloy same as above, used only in the transistor package.

Solder Preform, Rectangle 50-0257-2

Rectangular stamping, .005 inch thick, .100 inches x.250 inches and made of soft solder alloy as above.

Solder Preform, Round 50-0259-1

Circular stamping, .002 inch thick, .625 inches in diameter, made of same soft solder alloy as above. The preform is used only in the diode package.

Base Insulator 50-0244

Rectangular ceramic insulator, .030 inch thick, .250 inches x.110 inches and made of 96% aluminum oxide, metallized on both sides with a secondary firing of a molybdenum-manganese alloy followed by nickel plating. It is used only in the transistor package to provide isolation and bonding pad for the base terminal.

Base Pin 50-0245

Four-slide formed pin with three 90° bends, made of OFHC copper wire, .032 inches in diameter. It is used only in the transistor package.

Coating, Dielectric, Polymer

A dielectric coating applied by vacuum deposition, .001 inches to .0015 inches thick. The material is Parylene N, a polymer, made by Union Carbide Corporation. It will withstand 220°C in the absence of oxygen. The dielectric strength is 5000 volts/mil of thickness.

Encapsulating Compound

A silicon rubber called Thermasil, type I, made by Transene Company. It is a fire-resistant, noncombustible, thermally conductive, dielectric, encapsulating compound. It will withstand temperatures up to 250°C. The dielectric strength is 490 volts/mil. It is used only on the transistor package.

Adhesive, Structural

Speedbonder 325, made by Loctite Corporation, is a strong activator cured adhesive that is solvent resistant. The dielectric strength is 752 volts/mil of thickness. It can withstand temperatures up to 209°C.

Coating, Dielectric, Junction

A dielectric coating, v-176 made by Visilox Systems, Inc., is a one part siloxane polymer dispersion, developed for application on semiconductor devices. It will withstand temperatures up to 200°C. The dielectric strength is 2700 volts/mil of thickness. The dissipation factor is .003 at 1000Hz. It is used only on the diode package.

Hardware

Standard size 10, 300 series stainless steel hardware, two each: plain nut, flat washer and split lock washer. It is corrosion resistant and there is no plating to chip or flake off.

Terminal, Ring Tongue

A standard ring tongue terminal made by AMP Incorporated, part number 35273. It is a copper, crimp type with vinyl insulation and tin plating. It accepts wire sizes of AWG 12 or 10 stranded and will withstand temperatures up to 105°C.

Terminal, Insulated

A standard receptacle made by AMP, Incorporated, part number 2-520084-2. It is a tin plated, copper alloy, crimp type, .110 size, fully insulated FASTON terminal, part no. 2-520084-2. It accepts wire sizes of AWG 22 to 18, stranded and its nylon insulation will withstand temperatures up to 105°C. It is used only on the transistor package.

5.1.5 Environmental

All external metal portions of the package are nickel plated with Fidelity 4875. This is a high-phosphorus, electroless nickel plating, 150 to 200 microinches thick.

External metal portions are the copper electrical terminals, steel cap flange and copper bottom plate. This is necessary to prevent oxidation or corrosion of these areas. Oxidation of the terminals would increase electrical contact resistance. Corrosion on the surface of the bottom plate would reduce thermal conductivity.

High phosphorus electroless nickel plating provides all of the qualities necessary for protection from a Space Station environment, during ground handling, through launch and during long term orbit operation. It insures reliable electrical and thermal interfaces. The external surface of the ceramic

insulator is glazed. This is a glass coating used to protect the aluminum oxide ceramic from contamination such as metal smears and oils. Any contamination on the surface of the glaze is easily removed by normal cleaning methods and its smooth nonporous surface resists metal smears.

5.1.6 Reliability

Thermal fatigue occurs during the normal course of the operation of the device as it is cycled over a wide range of temperatures. It is generated by the mechanical stresses caused by the differences in thermal expansion of the components used in the device assembly. This can be a result of a temperature differential between the adjacent component parts or the difference in their coefficient of thermal expansion or both. Fatigue is normally experienced as cracks or separations within the component parts or the interfaces joining them. Often it appears in the silicon device and joints.

The large ceramic substrate is solder mounted to the bottom plate for a different reason. A large mismatch in the coefficient of thermal expansion, a significant temperature differential and large size cause a large difference in thermal expansion. Cracking the relatively tough component parts is not the main concern. Solder is used to absorb stresses thereby preventing severe warping of both bottom plate and ceramic substrate.

A molybdenum plate is used between the silicon device and copper conductor plate carrying the device current. Molybdenum has a coefficient of thermal expansion close to silicon, reducing

stress to a minimum.

The temperature differential between bottom plate and ceramic substrate is reduced by using beryllium oxide rather than the more commonly used aluminum oxide. Thermal conductivity of BeO (2.20 W/CM°C) is closer to copper (3.91 W/CM°C) so there is a reduction in thermal stress.

Large flexible, stranded and braided, copper cables connect the external terminals with the internal conductor plates. In the case of the diode package, one cable is attached to a molybdenum disc, soldered directly to the diode. The cables absorb minor assembly misalignments and package thermal expansion and prevent transmission of stress to devices and solder joints. A bend in the internal base pin achieves the same objective.

Aluminum wires connecting transistor emitter and base contacts to the internal package conductors are looped for flexibility, providing the means to absorb package thermal expansion and relieving stress on the ultrasonic bonds at each end of the wires.

Internal conductors are crimped and welded to external terminals. Resistance welding is a significant improvement over crimping only. Reliability and consistency of the contact is improved while lowering electrical resistance and the heat generated thereby.

Package conductors are as large as possible considering all aspects of the package requirements. They are made of the highest electrically conductive material consistent with overall goals. Reliability degrading heat generated due to electrical

resistance is minimized.

Ceramic plate subassembly component parts are joined by brazing with a silver-copper alloy. The strength of the components are able to withstand thermal induced stresses. Reliability is enhanced by the strength of the brazing alloy and its superior thermal conductivity.

Solder joints will eventually fail from thermal fatigue, probably before any of the component parts. Solder joints are a critical element in package reliability. Several measures were taken in the design and assembly of the package to insure highly reliable solder joints.

High purity solder alloy preforms (99.99% pure) are used exclusively for all solder joints. Extreme care is taken during assembly to prevent contamination from entering the solder joints. No flux is used. Impurities and contamination in the solder would result in dislocation pileup, thereby accelerating failure.

Appropriate precautions are taken to prevent oxidation of the solder preforms. Packages remain sealed until ready for use and parts are stored in a dry nitrogen desiccator. Oxidation contributes toward solder joint voids which create hot spots and act as crack nucleation sites thereby accelerating thermal shock failure.

Through the use of solder preforms the volume of solder is controlled. Voids are reduced and unwanted over flow is minimized.

A lead-silver-tin solder alloy is used (304°C liquidus) to insure melting temperatures well above 200°C. This is a

relatively strong solder having a mechanical strength which lies between that of the hard and soft solders, thereby avoiding damage to component parts (especially the silicon device) while resisting thermal fatigue between silicon and substrate.

5.2 Alternative Design Approaches

This contract presented the opportunity to investigate several new materials and processes for power semiconductor device fabrication. Listed in this section are several approaches investigated prior to the selection of the final design for the Space Station power semiconductor packaging.

Bottom Plate

There are three basic bottom plate approaches. The first is a hermetically brazed assembly consisting of a flat ceramic disc surrounded by a flat nickel-iron frame. Mounting holes pass through extensions on the frame. Internal component parts can be stacked on the ceramic disc. There is a weld projection on the frame for cap attachment. The ceramic disc can be either metallized with fired molybdenum-manganese alloy or layered with copper foil by the directly bonded copper (DBC) method.

Second is a hermetically brazed assembly consisting of a flat ceramic substrate and a flat nickel-iron frame both having identical external shapes. Mounting holes pass through both parts. There is a weld projection on the frame for cap attachment. In the center of the frame is a large circular cutout so internal component parts can be stacked on the ceramic substrate, which can be either metallized with fired molybdenum-manganese or layered with copper foil by the DBC method.

In both designs the intent is to eliminate the thick copper heat sink normally present in order to reduce thermal resistance. The ceramic would directly contact an external heat sink for heat transfer. If the DBC substrate is used, a molybdenum under the silicon device may not be needed, thereby further reducing thermal resistance. Neither design was used because of concerns for reliability and hermeticity. Hermetic sealing appeared difficult and there existed the probability of a cracked ceramic from use or rough handling.

The third approach consists of a flat pure copper stamped plate with a steel weld projection hermetically brazed. There are mounting holes at each end and internal components are stacked on the plate.

Internal Connectors

Three forms have been considered for the conductors connecting external terminals to internal components. An early design consisted of a copper cable split into a "y" shape with terminals swaged on each end. The design allowed too much flexibility for fixturing and was too complicated to make.

Next was a flat copper stamping, bent at 90°, with a cylindrical copper shaft attached by swaging. After soldering in place and wire bonding an additional 90° bend was applied bringing the shaft into position to mate with the cap. The bend was necessary since the shaft in its final position obstructed wire bonding operations. Because it was too rigid and the bend difficult to make accurately this design was dropped in favor of the third, a simplified copper cable used in the final design.

Internal/External Terminal Contacts

Two methods considered but not used are soldering and crimping. Soldering would consist of remelting a solder deposit within the joint between internal cable and external terminal, a preform could be placed inside the terminal prior to assembly or the cable end solder plated. Soldering was rejected in favor of welding. Difficulties anticipated were as follows: Heating and melting the solder might disturb previous solder joints, maintaining a forming gas atmosphere at the joint, inspecting the joint and avoiding contamination to internal parts. Crimping involves squeezing the external terminal inward to contact the internal cable forming a mechanical/electrical contact. Voids in the contact area have been observed with crimp contacts, resulting in high contact resistance.

Internal Contacts

Initial designs called for an assembly stack brazed with 780°C silver-copper and consisting of a copper bottom plate, ceramic substrate, copper conductor plates and molybdenum plate. After encountering severe warpage the same assembly was made using a 640°C silver-copper-phosphorus alloy with similar warpage. Next an all soft solder assembly was considered, but not tried. It was felt that as many component parts as possible should be brazed together. A brazed subassembly was used.

Ceramic Plate

In the final design it is possible to substitute two variations that were considered. These were aluminum nitride as a substitute for alumina and direct bonded copper.

Aluminum nitride is in the development process. It appears to be a good compromise between the high cost of beryllia and the poor thermal conductivity of alumina. Thermal conductivity of aluminum nitride is as high as 2.00 watts per centimeter per °C and the coefficient of thermal expansion is 4.6×10^{-6} meter per meter per °C, with a dielectric strength and resistivity similar to beryllia and alumina. [6] There are two significant differences. The thermal conductivity of beryllia drops rapidly between 100°C and 300°C. At about 100°C to 200°C the thermal conductivity of aluminum nitride equals that of beryllia. The low coefficient of thermal expansion will increase thermal expansion mismatch with other components in the package.

Ceramic with copper sheet directly bonded on both sides is available. Bonding a .032 inches thick copper layer on both sides is state of the art. Copper coefficient of thermal expansion is reduced by an intrinsic bond with the ceramic. A molybdenum plate would be needed under the silicon device. Thermal expansion mismatch from the molybdenum plate to the directly bonded copper would be reduced. Test data taken from P.T.C. high power modules constructed with both conventional metallized ceramic and direct bond copper ceramic, indicates a slightly lower $R\theta_{JC}$ with the conventional ceramic construction.

Cap

1. Zirconium copper CDA 150, chrome copper CDA182 and iron-nickel alloy 42 were considered for the external terminals.

2. Dielectric insulator:

   A. Aluminum oxide was to be used if plastic proved

unacceptable. Plastic has the preferred characteristics of lightweight and ease of manufacturing.

B. Valox 420-SE0, General Electric Co., is a thermoplastic polyester, 30% glass fiber filled. The heat deflection temperature @264 PSI is 204°C. It is affected by alkalies. Mold shrink rate is high and this material tends to warp.

C. Ryton R-7, Phillips 66 Co., is a polyphenylene sulfide, glass and mineral filled. The heat deflection temperature @264 PSI is 260°C. It is affected by ethers and amines and may outgas in a vacuum. It is difficult to mold and has moderate mold shrink rate.

D. Rynite FR-530, DuPont and Co., is a thermoplastic polyester, 30% glass fiber filled. The heat deflection temperature @264 PSI is 224°C. It is affected by alkalies and some polar solvents. Mold shrink rate is high.

E. Ultem 2300, General Electric Co., is a polyetherimide, 30% glass fiber filled. The heat deflection temperature @264 PSI is 210°C. It is affected by trichloroethane and phenol. Mold shrink rate is moderate.

Solder Preforms

Solder alloy selection is an important part of packaging design. Listed below are those alloys studied but not used in the final design:

50%	Pb,	50%	Sn	
50%	Pb,	50%	In	
95%	Pb,	5.0%	Sn	
92.5%	Pb,	5.0%	In,	2.5%Ag
92.5%	Pb,	5.0%	Sn,	2.5%Ag

A new process for manufacturing solder has been developed by

Allied Corporation with the trade name of Metglas. Although information was received too late for implementation, Metglas materials show promise. Metglas solder alloys are produced by Rapid Solidification (R/S). As a result, according to Allied, solder joints exhibit a fine grained homogenous microstructure. The uniform microstructure eliminates crack nucleation sites and defers crack propagation, thereby improving both the shear strength and resistance to thermal fatigue failure. Metglas solders achieve complete liquidity faster than conventional alloys. Since the foil is cast rather than rolled (conventional method), there are less surface oxides and other impurities are not rolled in, resulting in reduced joint voids and improved wetting. These high purity solders are available in most of the commonly used alloys. Of particular interest for this package is alloy MSFA-103, 92.5 Pb, 5.0% In, 2.5 Ag, Liquidus 310°C, solidus 300°C. A high lead content allows plastic deformation. The addition of silver improves thermal conductivity while indium improves wetting, contributes to plasticity and resistance to thermal fatigue. The Metglas solder will be used on all future programs at P.T.C., utilizing the Space Station semiconductor power package.

6.0 ASSEMBLY PROCESSING AND EVALUATIONS

6.1 Process

The assembly of the piece parts, as described, is a process that utilized the same processing steps for the diode and transistor.

6.1.1 Diode

Assembly process steps are outlined in the flow chart, Figure 13.

6.1.2. Transistor

Assembly for the transistor is outlined in the flow chart, Figure 14.

6.2 Equipment

6.2.1 Diode

Controlled atmosphere conveyer furnace
Watkins-Johnson Co.--Model number 8CS-96(S)

Inspection Microscope

Ultrasonic Vapor Degreaser
Delta Sonics--Model DS1012R

Automatic Dispensing System
EFD Corp.--Model No. 1000 DF/DG

Vacuum Bake Oven
Blue M Co.--Model POM-18VC-2

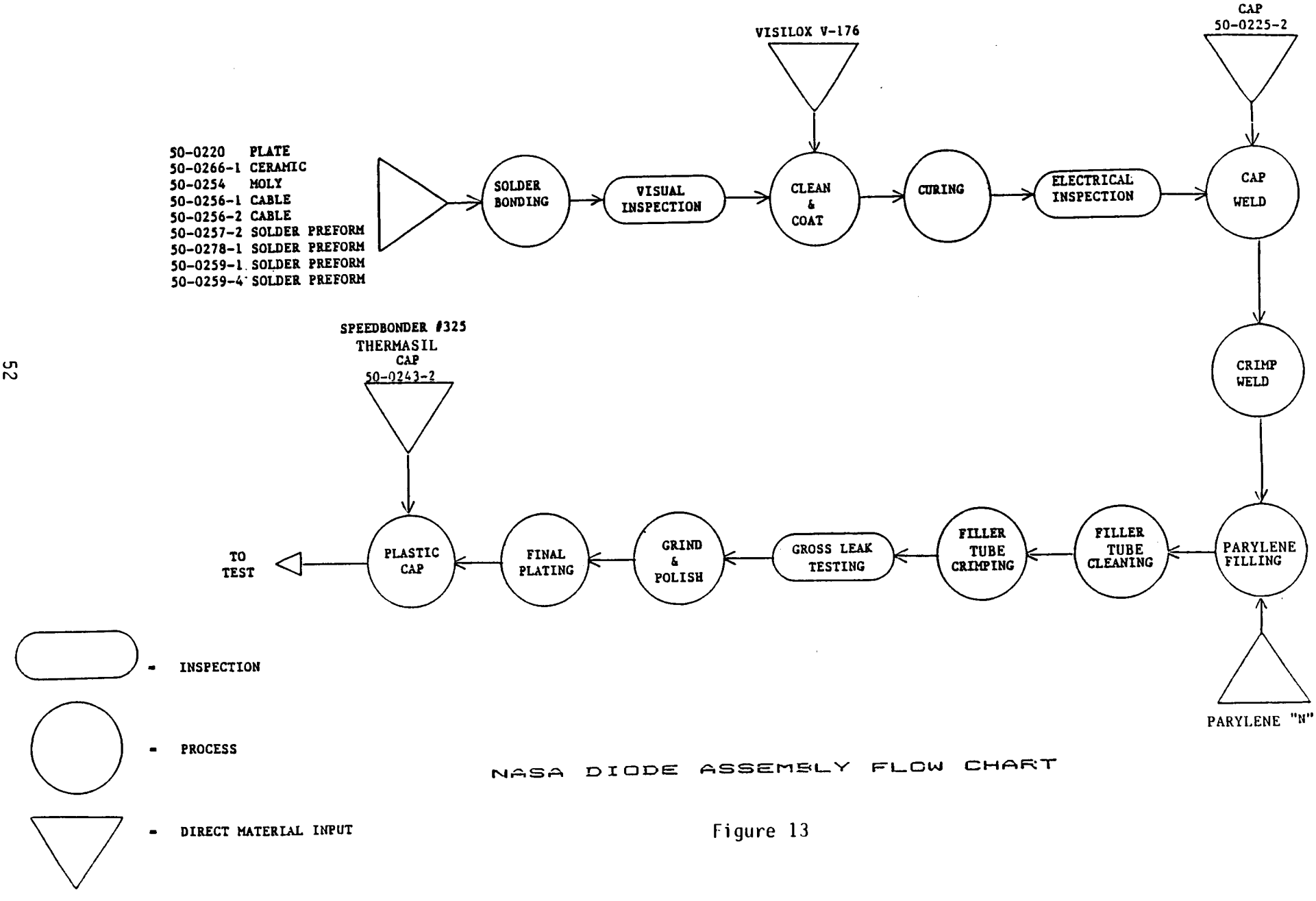
Semiconductor test system (in-process test)
Lorlin Impact II

Resistance Cap Welding System
Polaris Electronics Corp.--Model 5100 AC, 125KVA

Crimp Welding System
Unitek Co.--Phasemaster I, Model PMI

Bubble Testers
Trio-Tech--Model G-203

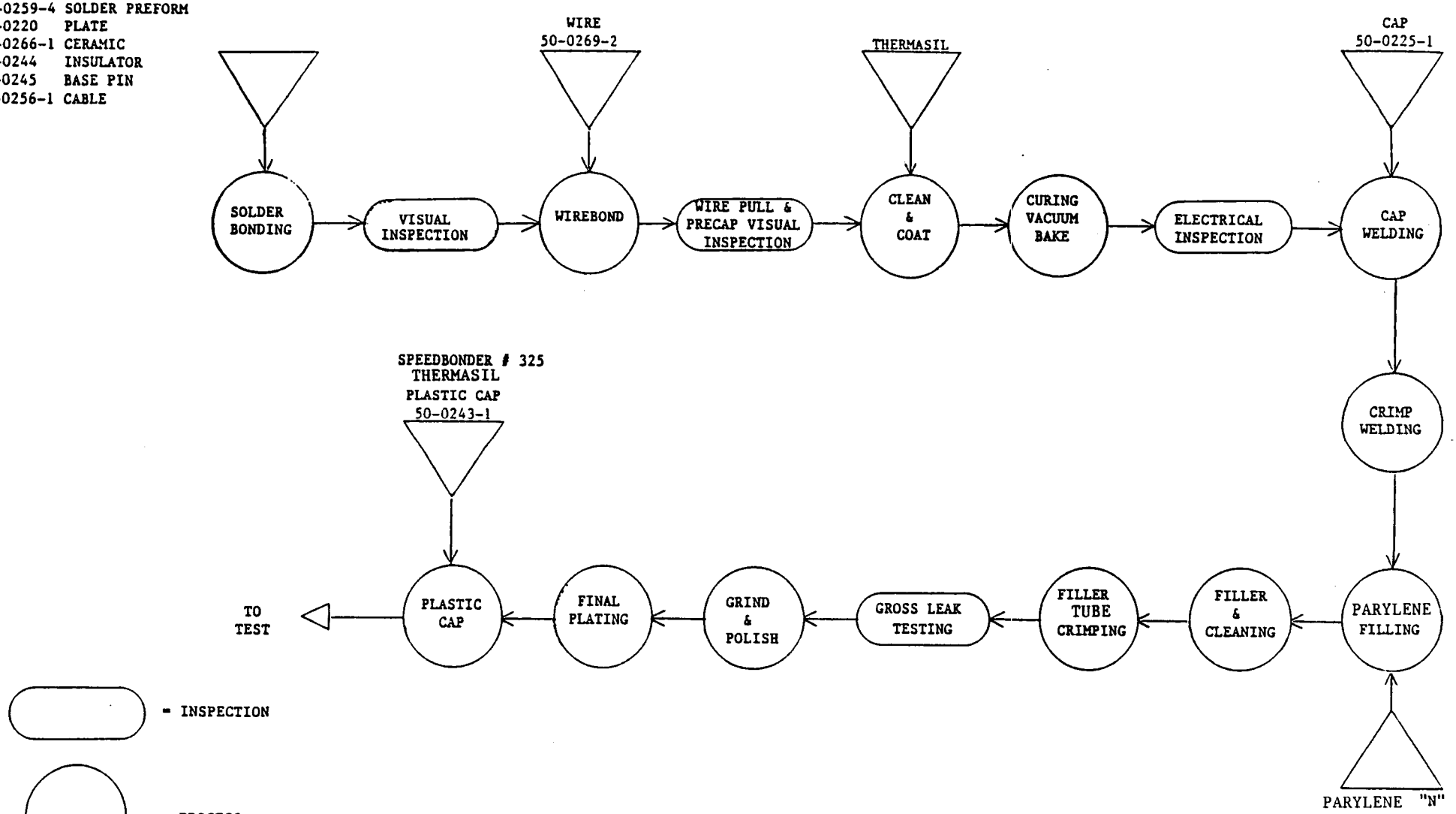
Rotary Disk Polisher



NASA DIODE ASSEMBLY FLOW CHART

Figure 13

50-0257-1 SOLDER PREFORM
50-0257-2 SOLDER PREFORM
50-0258-1 SOLDER PREFORM
50-0259-4 SOLDER PREFORM
50-0220 PLATE
50-0266-1 CERAMIC
50-0244 INSULATOR
50-0245 BASE PIN
50-0256-1 CABLE



NASA TRANSISTOR ASSEMBLY FLOW CHART

Figure 14

6.2.2 Transistor

Controlled atmosphere conveyer furnace
Watkins-Johnson Co.--Model number 8CS-96(S)

Inspection Microscope

Orthodyne Wirebonder
Model 20

Bond Pull Tester (0 to 2000 gms)
Hybrid Machine Products--Model M2305

Ultrasonic Vapor Degreaser
Delta Sonics--Model #DS1012R

Automatic Dispensing System
EFD Corp.--Model No. 1000 DF/DG

Vacuum Bake Oven
Blue M Co.--Model POM-18VC-2

Semiconductor test system (in process test)
Lorlin Impact II

Resistance Cap Welding System
Polaris Electronics Corp.--Model 5100 AC, 125KVA

Crimp Welding System
Unitek Co.--Phasemaster I, Model PMI

Bubble Testers
Trio-Tech--Model G-203

Rotary Disk Polisher

6.3 Tooling

6.3.1 Furnace Soldering Fixture

All soldering for both the diode and the transistor package is accomplished with the aid of a solder reflow fixture. One fixture design is used for both devices. It holds the component parts in place while the solder melts during a furnace pass and continues to hold the parts while the solder solidifies.

One fixture is used for each assembly. A single fixture consists of an assembly, one each of the following pieces:

Weight Plate	50-0260
Locator Plate	50-0261-1
Spacer	50-0262
Weight	50-0263-2
Weight	50-0264
Spring Pin	0 3/32x.50, S/S

Assembly begins with a furnace boat, 50-0265. This is a four position carrier tray used to hold the piece parts and fixture parts in a convenient position for easy assembly. It then serves to carry assemblies through the belt furnace, in a group of 4 assemblies, that is both compatible with the furnace capacity and efficient from a production standpoint.

The package piece parts and the fixture piece parts are assembled in a fixed order. All solder joints are individually weighted so that the weighting is both independent and appropriate to the size of the joint.

The fixture, furnace boat and package were designed for easy, efficient production. All soldering is accomplished with one pass through the belt furnace. Piece parts are properly located so they fit together with mating parts in later assembly operations, without additional bending or fitting. This system is easily expandable for larger assembly runs. All excess material has been removed, where practical, to minimize the mass of the fixture and furnace boat.

The component parts of the fixtures are made of AISI 410 stainless steel. The choice of material is as important to the functioning of the fixture as its design. Areas of the fixture come in contact with molten solder while in the furnace and must resist becoming soldered to the assembly. Type 410 stainless steel, containing about 12% chromium was chosen because it is

difficult to solder. It develops an oxide coat after heating and exposure to air, further reducing its solderability. Its life expectancy is long. The industry standard material for furnace fixtures has been graphite. Unlike graphite, stainless steel does not crack, chip, break or shed. It can be repaired or modified more easily than graphite because material can be added by welding. It is easy to clean and keep clean since it is nonporous and does not absorb oil from the hands or moisture from the air.

In an annealed condition, type 410 stainless steel is mechanically stable. There has been no warping, twisting or bending observed after repeated temperature cycling through the furnace at peak temperatures of 400°C. It has the lowest coefficient of expansion of all the other stainless steels considered.

The wire Electronic Discharge Machine (EDM) and ram EDM processes were used to make critical portions of the fixture. Remaining parts were made by conventional machining. The fixture was designed to take advantage of the computer controlled EDM process. Key features are:

1. **Repeatability.** Any number of identical pieces can be produced any time. Reorders are guaranteed to be identical.

2. **Stackability.** Work pieces can be stacked and wire cut at one time lowering costs.

3. **Machinability.** The process can cut difficult to machine materials or hardened tool steel easily and economically.

4. **Burrs.** The process makes a clean burr free cut.

5. **Accuracy.** Excellent precision is easily achieved.

6. **Intricate Shapes.** Fine, small, intricate shapes can be made that are not possible or practical with conventional machining.

7. **No Stress.** Stresses are not introduced into the work piece and as a result there is no bending or warpage.

8. **Cost.** With improvements in equipment and electronics, cutting speeds have increased thereby lowering piece part cost.

6.3.2 Cap Welding Electrode

Polaris Electronics Corporation working with P.T.C. designed and fabricated a set of tooling used to resistance weld the cap and bottom plate. The tooling consists of copper alloy, cylindrical upper and lower electrodes that were designed for a 125 KVA Polaris resistance welder. Both electrodes are easily removed for service. Plastic locator pins are incorporated into the lower electrode retaining ring, for automatic alignment of the cap and the bottom plate.

6.4 Assembly Problems and Solutions

6.4.1 Bottom Plate

The bottom plate consists of a copper plate with a weld ring brazed to it.

Some bottom plates were received with different types of weld rings and some of the weld ring cavities were not completely filled with solder braze, which produced voids under the weld ring resulting in leaks at capping.

The plates, as received from the vendor, were not flat. A dish shaped cavity was located in the center of the bottom plate.

This cavity severely affected the thermal resistance. It was required to surface all of the transistor and diode bottom plates prior to final plating.

Besides the voids in the weld ring, excessive braze material had overflowed from the ring cavity onto the top of the plate, creating a problem of nonuniform plating and mounting areas. Surface profile variations are shown in Figure 15.

The bottom plates were plated with high phosphorous, electroless nickel.

6.4.2 Ceramics

Both alumina and beryllia ceramics were used in this program. The alumina substrates were used to establish the process. Once processes were established, the beryllia (BeO) was used to assemble the engineering models.

The alumina ceramics were received with metal bridging along the edges. This necessitated sanding the sides of the ceramic to remove the metal bridges. This problem was created during the laser scribing operation done by the vendor. The BeO ceramics were not laser scribed and did not exhibit this problem.

Problems were encountered in trying to achieve a void free solder bond between the ceramic and the copper bottom plate. Gold plating of the ceramics resulted in poor solderability to the copper plate. The plating on the top did not present any problems in solder bonding the chip to the ceramic assembly. Some ceramics were sent to NASA Lewis for recleaning, using an atomic oxygen cleaning process. Also, an asher plasma cleaning process was used. There was no improvement using these cleaning

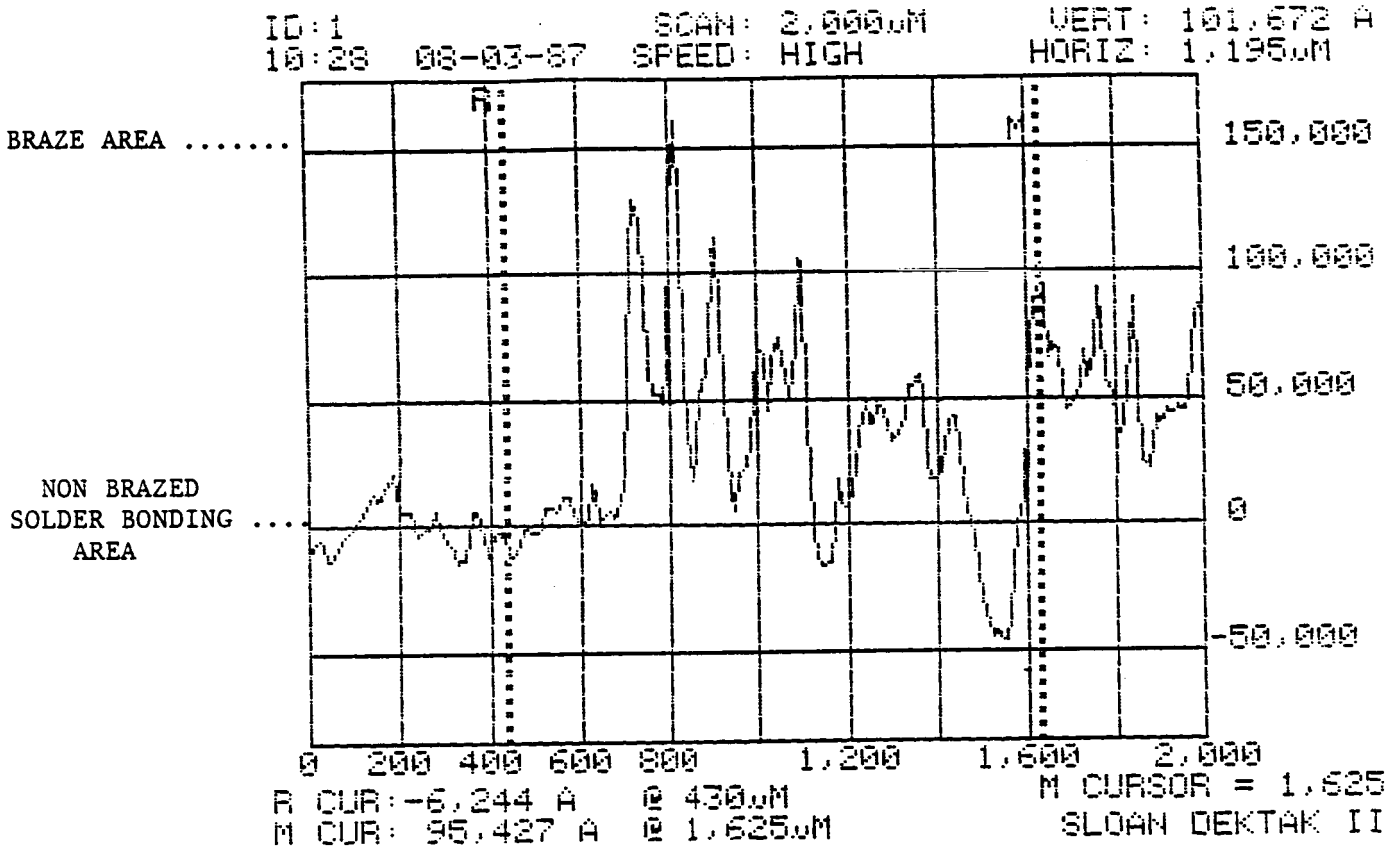


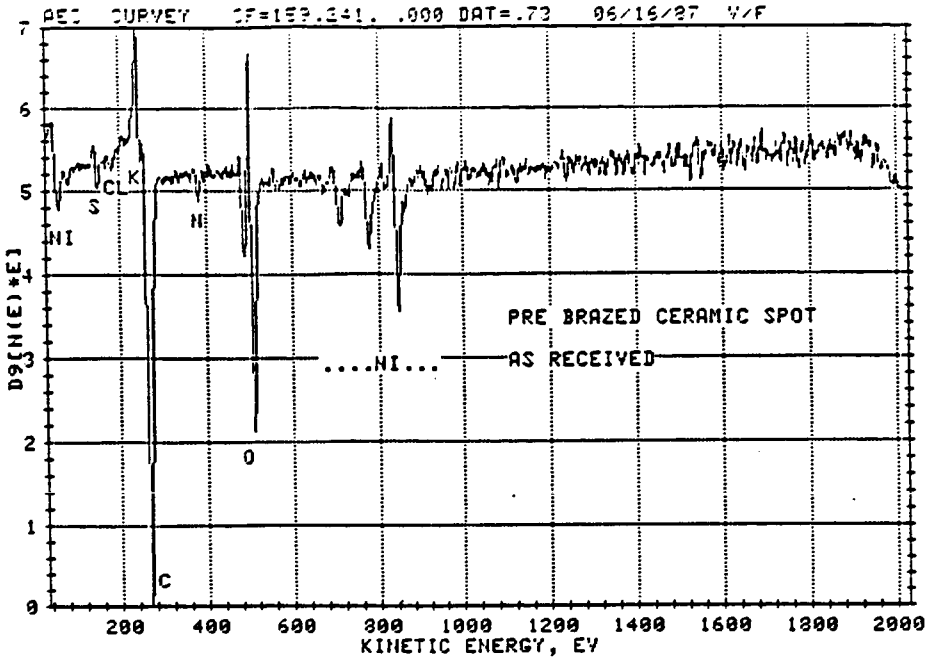
Figure 15, Bottom Plate Surface Profile

technologies. Because of the continuing problems with the back metallization on the ceramics, samples were sent for Scanning Auger Microanalysis (SAM). Several samples were analyzed and the results indicated traces of tungsten on the nickel surface to a depth greater than 100 A. The Auger analysis did not show any traces of tungsten prior to the brazing process. (Figure 16, a and b) To correct this problem it was necessary to remove or cover the tungsten. The final plating process for the ceramics was as follows: 150 microinch copper, 100 microinch nickel, 5 microinch gold strike (Au & Ni), 5 microinch pure gold.

Prior to assembly the gold plated ceramics were cleaned in a solution of 10% acetic acid and DI water. This process produced void free solder joints.

During the in-process test of thermal resistance ($R\theta_{JC}$) the initial transistors tested, read approximately 0.2°C/W up to 40 or 50 watts. Above 50 watts the $R\theta_{JC}$ would increase to levels as high as 1.5°C/W or higher. Some units would go into a forward bias secondary breakdown mode. When testing these same units on the Forward Bias Safe Operating Area Tester (FBSOA), they would pass at 10V/50A (500 watts). Some units passed at 10V/60A (600 watts). It was determined that voids between the ceramic interface and the copper metallization were causing the thermal resistance problem. The ceramics were then sent for radiographic inspection (x-ray), to check for voids between the ceramic-copper interface. Three groups were x-rayed.

Group #1	Al_2O_3	100 ea	=	100% failed with voids >25%
Group #2	BeO	100 ea	=	70% failed with voids >20%
Group #3	BeO	321 ea	=	51% failed with voids >20%



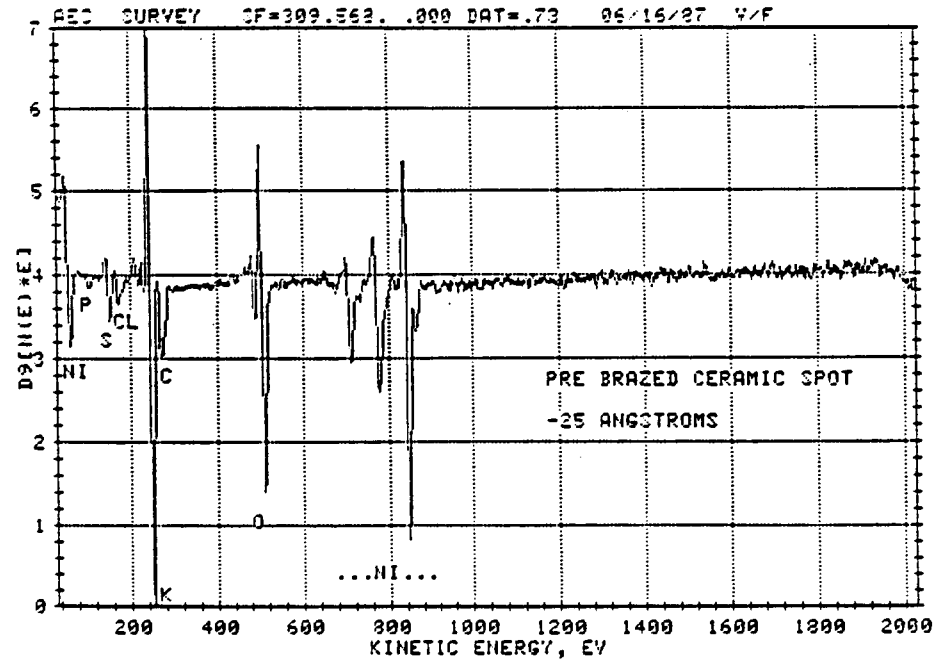
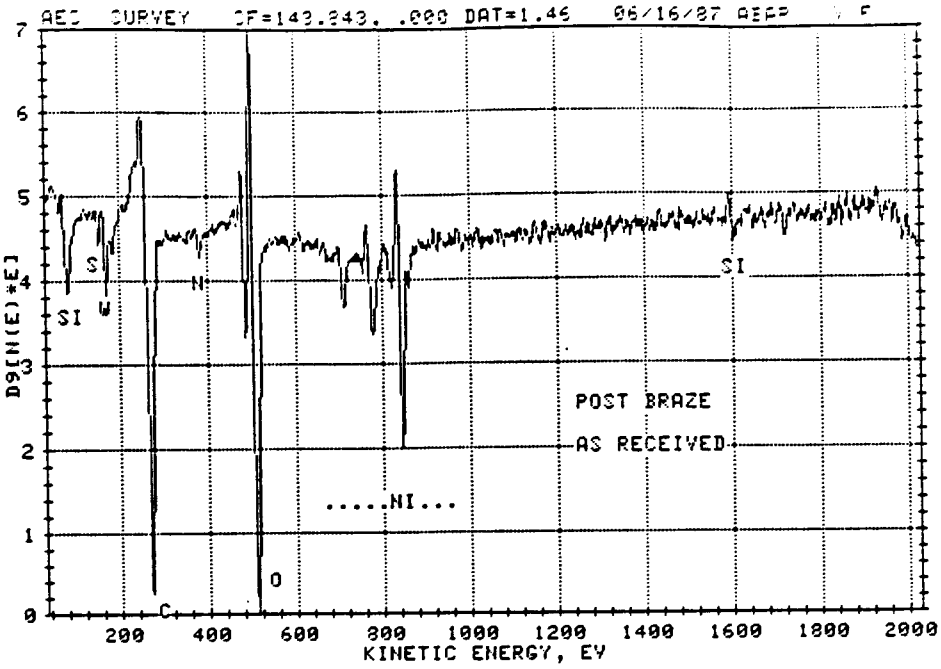


Figure 16a, Scanning Auger Microanalysis of Ceramic Metallization

Prior to Braze



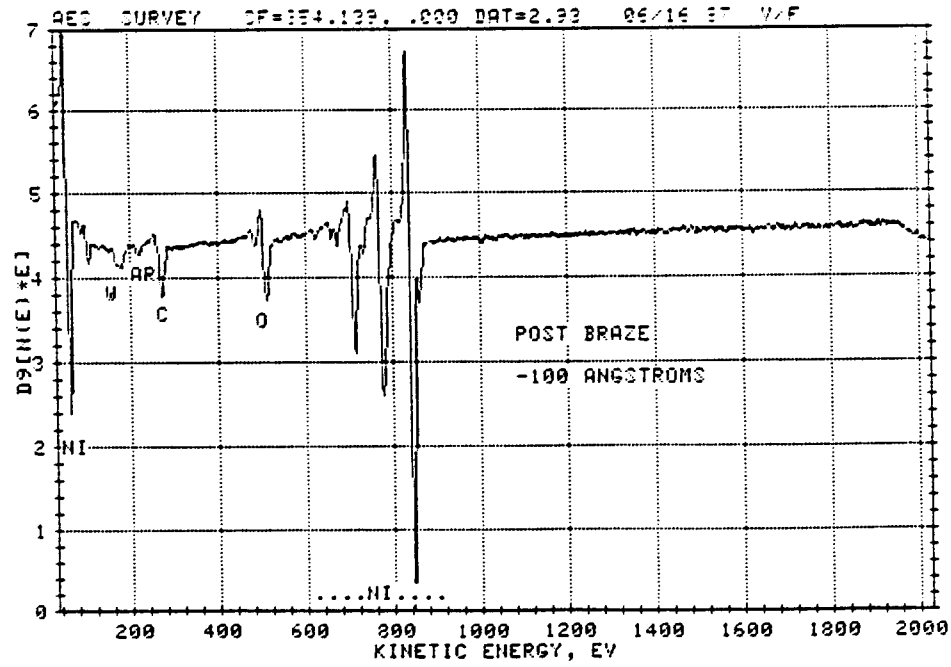


Figure 16b, Scanning Auger Microanalysis of Ceramic Metallization

Post Braze

The 164 BeO ceramics in group #3 that passed were used for the final assembly of both the transistor and the diode engineering models.

Figure 17 shows large circular voids were present under both the copper heat sinks and also under the hexagonal molybdenum pads on top of the copper. The vendor who brazed the copper to ceramic was contacted to determine the cause of the voids. Their response was that they had used round washer shaped braze preforms, where a disc shaped preform should have been used. These washer shaped preforms created the voids under both the molybdenum and the copper resulting in the marginal thermal resistance.

6.4.3 Cables

The first attempts of soldering the braided copper cables to their respective bonding pads did not work. The problem was the solder which should have remained at the bottom of the cable to provide the proper fillet, was wicked (sucked) into the center of the sleeve and climbed up the inside of the cables. Two corrective measures were taken simultaneously:

1. All the remaining cables were returned to the manufacturer for recrimping of the bottom sleeve.

2. All the recrimped cables were sent out for plating, first with nickel followed by a flash of gold. This corrected the wicking problem and produced fillets which are well feathered, continuous and smooth.

6.4.4 Wire Bonding

Electrical contacts to the active areas of the transistor consist of 25 mil aluminum wire ultrasonically bonded to the base

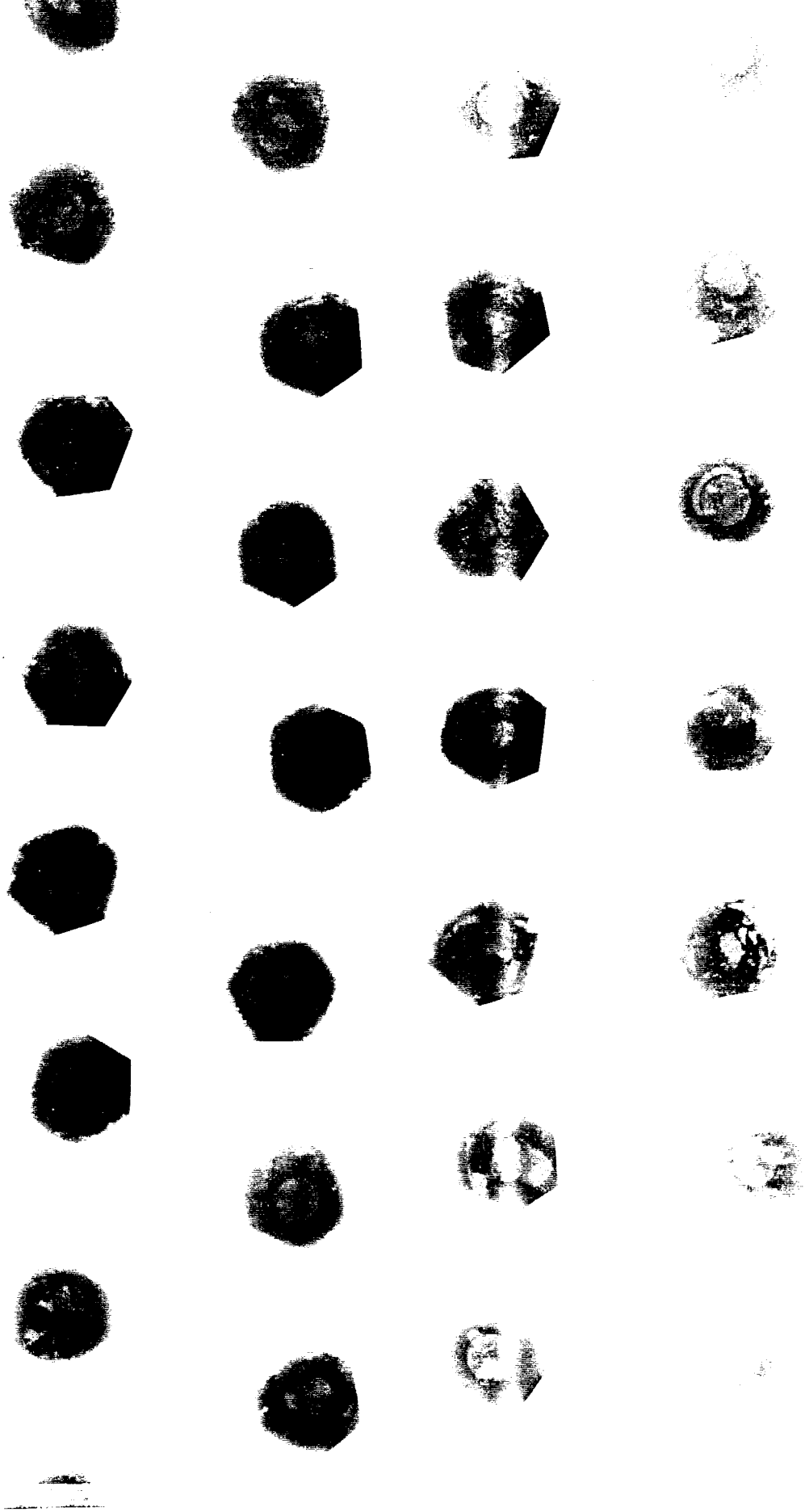


Figure 17, Ceramic-Copper Interface Inspection by X-Ray

and emitter bonding pads. Only minor problems were encountered with excessive solder reflow on the emitter bus.

6.4.5 Cap Welding

Some of the transistor caps had obstructions blocking the tubular portion of the base terminal. Because of this blockage, the cap would not seat properly without deforming the base pin. Correction for this problem was to use a go/no-go gage and test all of the tubes, discarding the blocked ones.

At capping, some of the caps had a misalignment of the ceramic and the steel welding flange which made them unusable, because they would not seat properly in the cap welder electrodes. All the caps were tested in a go/no-go fixture and separated prior to capping. After welding and tube sealing, the caps were tested for gross leakage.

6.4.6 Crimp Welding

A Unitek, Phasemaster I, Model PMI, was used to crimp weld the collector, emitter and base on the transistor and a cathode and anode on the diode. No major problems were experienced once the processing cycles were established.

6.4.7 Post Cap Interior Coating

The Parylene passivation was performed by Nova Tran Corp. When the units were received from Nova Tran the filler tube had a coating of Parylene on the inside. It was necessary to remove this coating prior to sealing the tube.

The initial attempts at crimp welding the tubes resulted in approximately 50% gross leak test failures. To improve the weld, the crimp area was moved up to .025" from the end of the tube. Crimping in this area would smash and melt all the copper at the

end of the tube, producing a tight seal.

6.4.8 Bottom Plate Surfacing

The weld ring brazing process leaves a concave area, located in the center of the bottom of the plate. To correct this, surfacing on a rotary grinder/polisher was performed.

6.4.9 Finish Plating

After surfacing, the units are final plated with 100 microinches copper per MIL-C-14550, class 0 and 150 microinches Electroless Nickel per MIL-C-26074B.

6.4.10 Plastic Cap

Filling the cavities which surround the copper terminals was more of a problem than anticipated. Only after several potting material evaluations, a satisfactory material and application technique was selected.

The cap is installed by first using a high temperature (-54°C to 177°C), high impact strength (2.1 J/cm^2) adhesive which gives maximum reliability under severe environmental conditions. The void is completely filled with the high temperature silicone rubber which was used to form the gasket. The silicone rubber used is solventless, forms a flexible heat-resistant seal which will withstand temperatures in excess of 275°C and electrical properties are not sacrificed at the high operating temperatures. Dielectric strength is 490 volts/mil. This potting compound will expand during the curing cycle but the excess can be trimmed.

7.0 ELECTRICAL TESTING

All electrical testing, from chip evaluation to final characteristic testing, is performed on equipment available in P.T.C.'s electrical test facility. The equipment calibration is maintained as defined in P.T.C. Q.A. Procedure, Document Number QRS-2003, Rev. A, that defines the control of all P.T.C.'s measurement and test equipment as required by MIL-STD-45662.

7.1 Chip Testing

Due to the large size of the chips and the necessity of staggering them on the wafer, it is not possible to automatically probe the wafers. Therefore, it is necessary for us to probe each chip by hand. To do this we had a dice probing fixture made by Martronic Engineering. Simi Valley, Calif. Each chip is placed into the dice cavity using a vacuum pickup tool, and the cover containing the spring loaded probing needles is lowered on to the top of the chip. The test fixture can be plugged into a Tektronix curve tracer or into an automatic tester. No guard band is added to the chip parameters because assembled chips improve in all of the characteristics.

7.1.1 Diodes

The diodes in chip form are tested for the following parameters prior to assembly:

1. I_R Reverse Leakage Current @ V_R=1000V <.200mA
2. V_F Forward Voltage @ I_F=50A <1.5V
3. t_{rr} Reverse Recovery Time @ I_F=50A <500nS
4. The average test values for the last eleven lots are:
   - A. V_R = 1068V
   - B. V_F = 1.48V
   - C. t_{rr} = 416nS

7.1.2 Transistor

The transistors in chip form are tested to the following parameters:

1. V_{CBO} Collector-Base Voltage @ I_C=.300mA >600V
2. V_{CEO}(sus) Collector-Emitter Sustaining Voltage
   @ I_C=200mA, I_B=0, .300ms pulse >500V
3. I_C(rated) Gain Rated Collector Current
   @ I_B=4.16A V_{CE}=2.5 >50A
4. The average test values for the last 13 lots are:

   V_{CBO} = 713V

   V_{CEO}(sus) = 492V

   I_C = 58A

7.2 Assembly In-Process Testing

After the assembled units are cleaned and coated with the respective passivation coatings, and prior to pre-cap visual inspection, they are electrically tested to eliminate the poor subperformance units. This test is performed on the Lorlin Impact II automatic tester, which has the capability of testing up to 100A and 2000V. At this stage of the assembly all tests were performed to specified parameters and at room temperature. All tests are datalogged for comparison with the finished tested units.

7.3 Final Characteristic Tests

7.3.1 Diode

1. DC Blocking Voltage (V_R)
   @0.050mA at 25°C
   and 5mA at 100°C
2. Peak nonrepetitive reverse voltage (V_{RSM}) is specified

at 100°C. Typical blocking voltage and peak reverse voltage values are plotted as a function of reverse current and temperature. (Figure 18 and Figure 23) The Tektronix Curve Tracer, Model 370 is used to plot a typical DC Blocking Voltage characteristic at 25°C as plotted on an Epson HI-80. (Figure 19)

3. Average Forward Current @100°C (I_F). The average current was measured on the Tektronix Curve Tracer, Model 576 and the data is presented in Figure 20, as a function of the forward voltage (V_F).

4. Nonrepetitive Peak Surge Current (I_{FSM}),@ 1/2 cycle, 60Hz, resistive load, 600A min. Measurements are made on the Martronic Surge Current Tester, Model 30. Figure 21 shows the typical wave forms of two devices under test. For surge current at specified conditions for the proposed 125A rated device, the surge current rating is increased to 2100A min.

5. Forward Voltage @ 50 ampere (V_F). The data was taken on a Tektronix Curve Tracer, Model 576 with a high current adapter Model 176. The data is shown in Figure 20 and Figure 23.

6. Reverse Recovery Time and Peak Reverse Recovery Current (t_{rr}) and (I_{RR}),@I_F=50A, dI/dt=25A/us T_J=100°C. Both tests were performed on a Martronic Reverse Recovery Time Tester using the JEDEC circuit. Figure 22 shows the t_{rr} wave forms at 25°C. Figure 23 lists the t_{rr} at 100°C for all engineering models delivered.

7. Interterminal Capacitance, anode to cathode

V_R=350V, f=0.1M Hz (Figure 34)

7.3.2 Transistor

1. Collector-Emitter Sustaining Voltage ($V_{CEO}(sus)$)
   @ I_C=200mA, I_B=0, 300 us pulse

Martronic Sustaining Voltage Tester Model, 11 was used to measure the sustaining voltage. (Figure 24 and Figure 25)

2. Collector-Base Voltage (V_{CBO}
   @ I_C=300mA

A Tektronix, Model 370 was used to test the collector-base voltage. (Figure 24 and Figure 26)

3. Gain-Collector Current Product ($h_{FE}I_C$)
   @ V_{CE}=2.5V

The tests were performed on the Mastech, Model 216 COM Automatic Tester. The data is presented in Figure 27 and 24.

4. Gain Rated Collector Current ($I_C(rated)$)
   @ h_{FE}=12, V_{CE}=2.5V

Mastech, Model 216 was used to measure gain rated collector current, $I_C(rated)$, Figure 24.

5. Continuous Collector Current ($I_C(cont.)$)

Test performed on Forward Bias Safe Operating Tester, Martronic, Model 29. Conditions were 10 volts V_{CE} and a base drive of 5.0 amperes.

6. Peak Collector Current, Pulsed ($I_C(peak)$)

The peak collector current was tested on the High Current Surge Tester, Martronic, Model #30. Parameters were 200 volts V_{CE}. with a base drive of 10 amperes.

7. DC Current Gain (h_{FE})
   @ I_C=50A, V_{CE}=2.5V (Pulsed with duty cycle <2%)

The DC current gain was measured on a Tektronix, Model 576 with high current adapter, Model 176, and the Mastech Automatic Tester. The data is present in a gain hold-up curve, Figure 27

and Figure 24.

8. Base Current, continuous (I_B)

Measured on the Tektronix 576 with a high current adapter, Model 176.

9. Collector-Emitter Saturation Voltage ($V_{CE}(sat)$)
@ I_C=50A, I_B=6.25A

The Mastech Automatic Tester was used. The data is presented in Figure 24 and Figure 28.

10. Base-Emitter Saturation Voltage ($V_{BE}(sat)$)
@ I_C=50A, I_B=6.25A

Measured in the same method as $V_{CE}(sat)$, the data is shown in Figure 24 and Figure 29.

11. Switch Time. ($t_{on}, t_d t_{stg}, t_f$)
V_{cc}=300 volts, I_C=50/A $I_{B1}=I_{B2}$=4.2A

The turn-on, rise, storage and fall times were measured on a Martronic Resistive Switch Time Tester. The storage and fall times are shown in Figures 24, 30, 31, 32, and 33.

12. Input Impedance: approximately 18000 ohms measured on Tektronix, Model 576.

13. Output Admittance: approximately 136 mhos measured on Tektronix, Model 576.

14. Interterminal Capacitance, Collector to Base

V_{CB}=350v, I_E=0, f=0.1 M Hz,

and C vs. V_R, Figure 35.

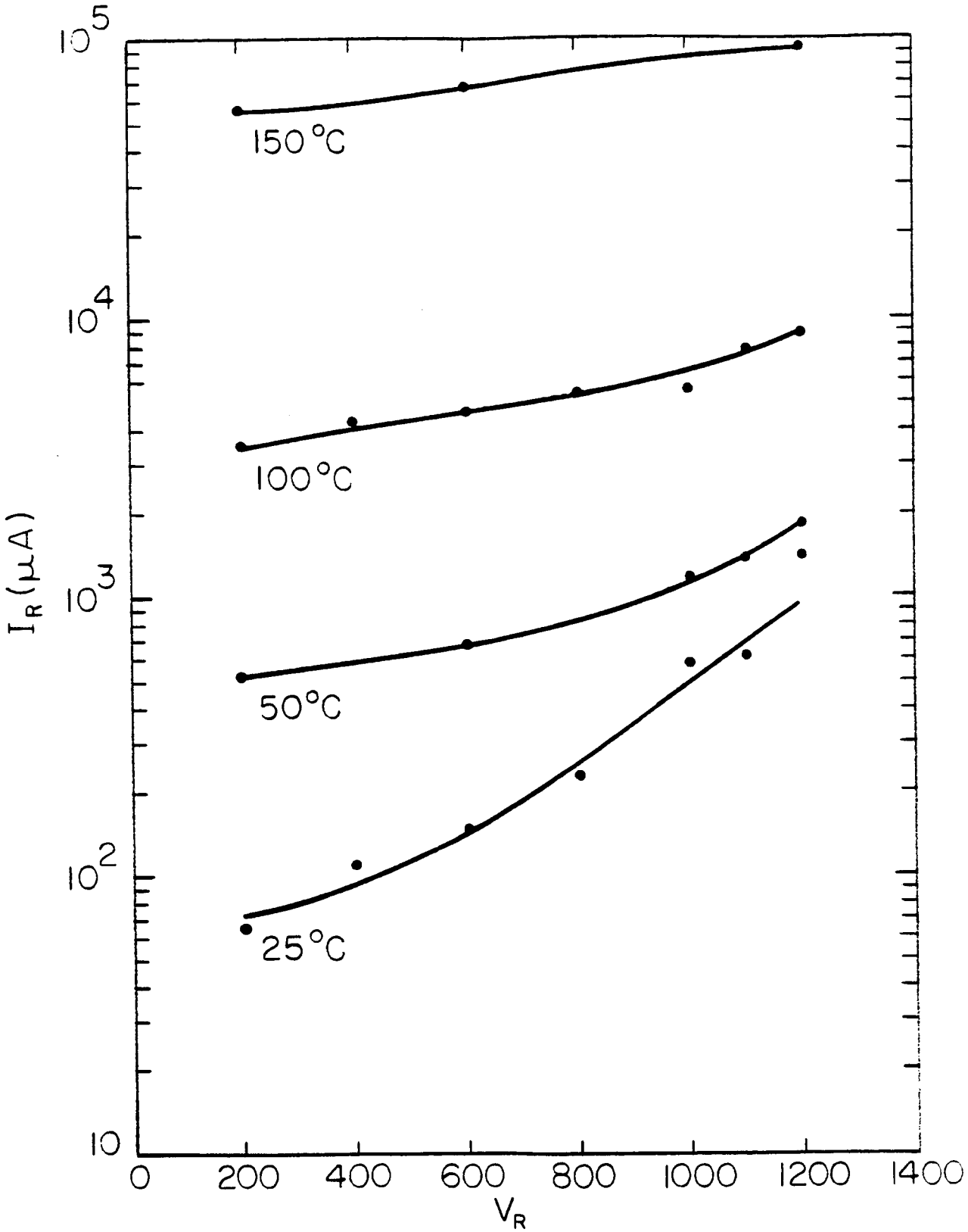


Figure 18, Diode Blocking Voltage (V_R) or Peak Inverse Voltage (PIV) vs. Reverse Leakage Current.

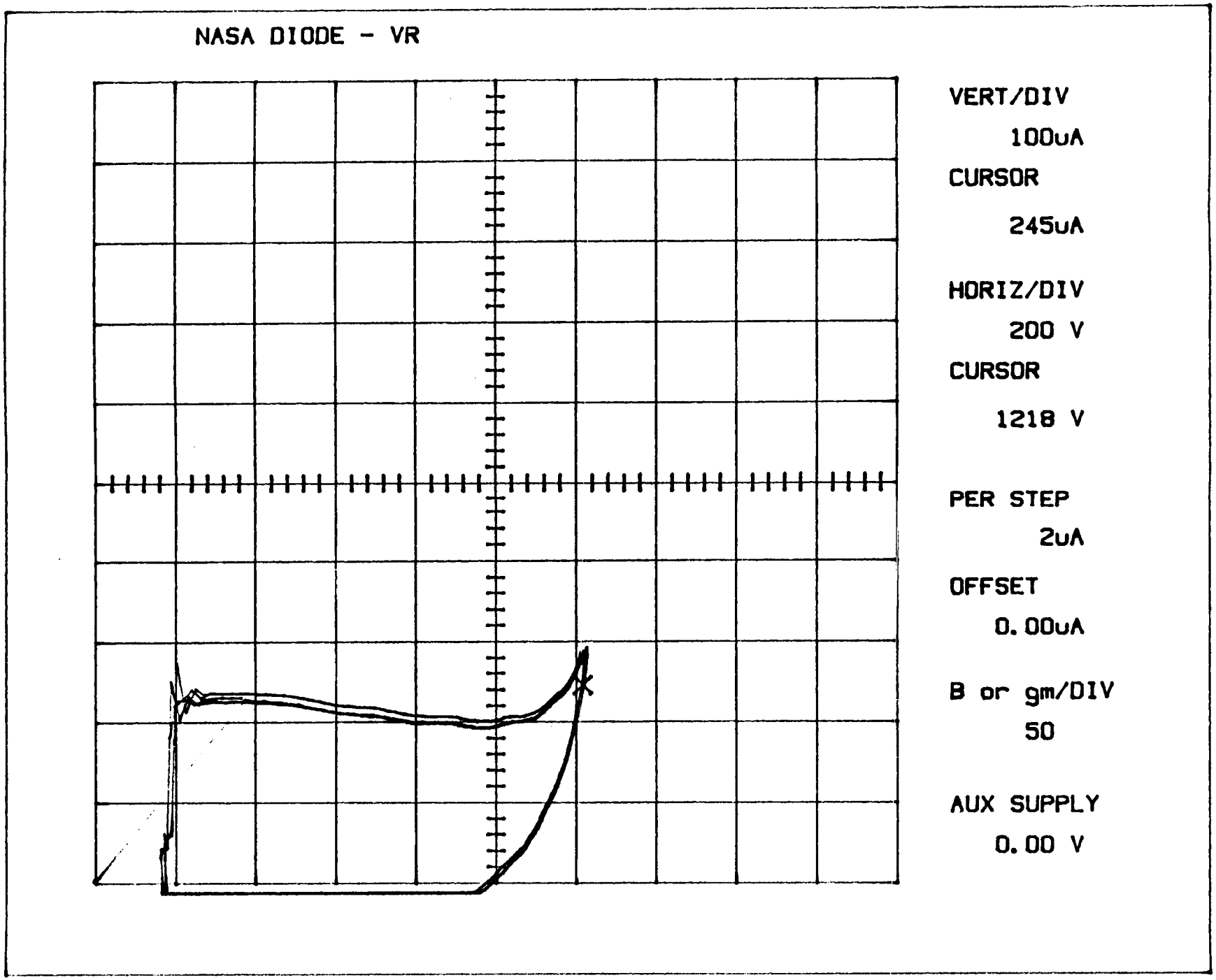

NASA DIODE - VR
VERT/DIV
100uA
CURSOR
245uA
HORIZ/DIV
200 V
CURSOR
1218 V
PER STEP
2uA
OFFSET
0.00uA
B or gm/DIV
50
AUX SUPPLY
0.00 V

Figure 19

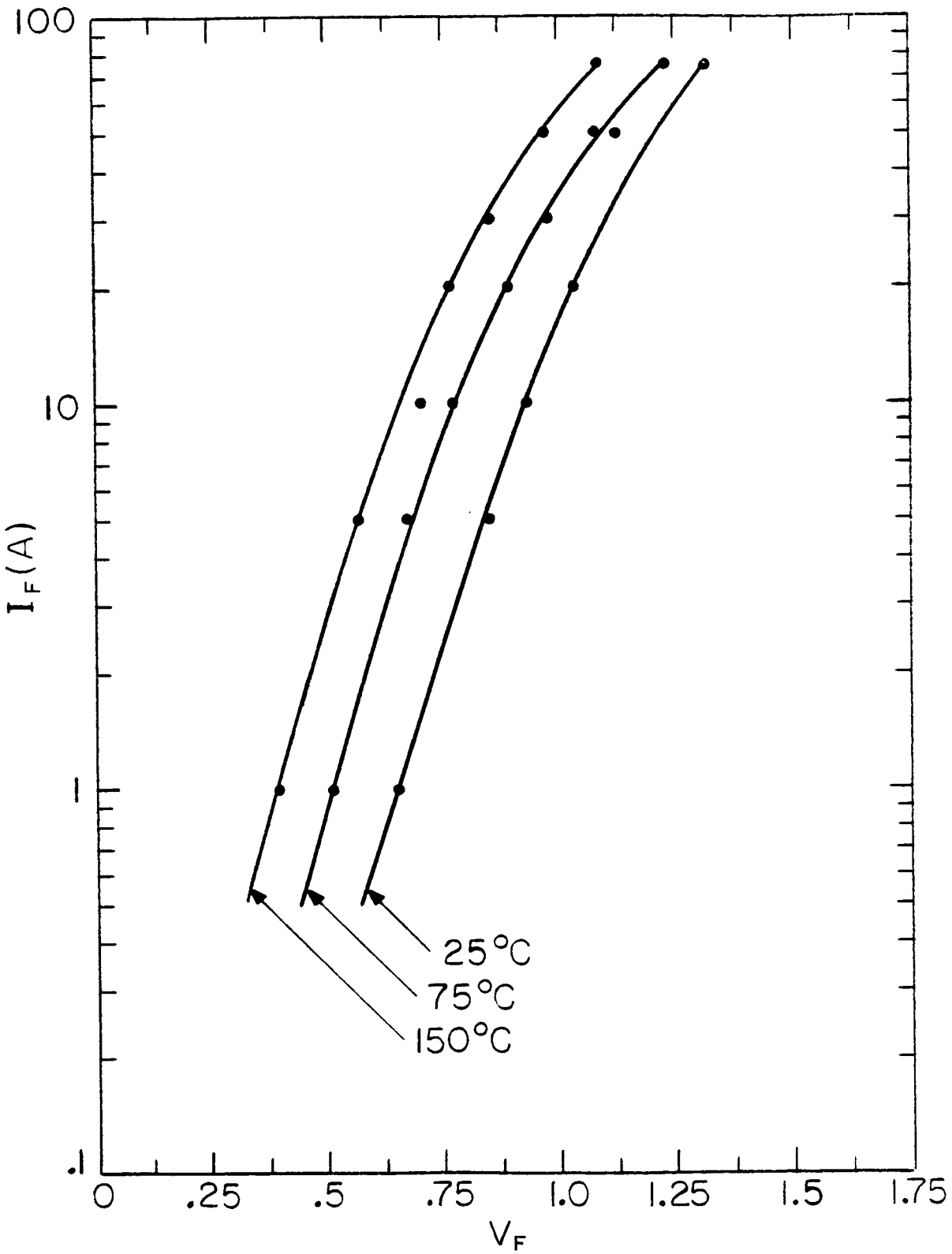
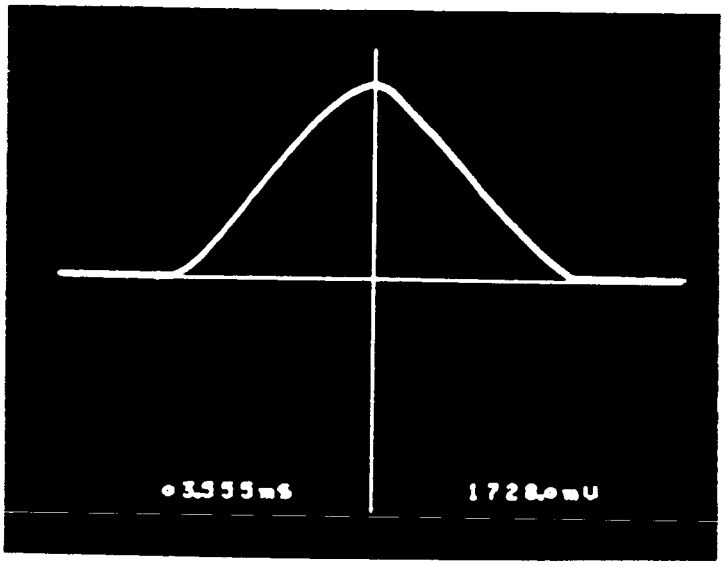
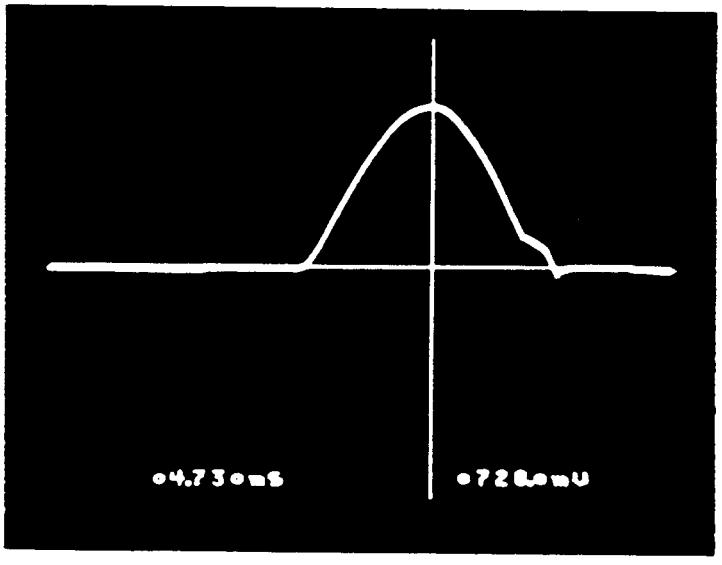


Figure 20, Diode Average Forward Voltage (V_F) vs. Forward Current (I_F).

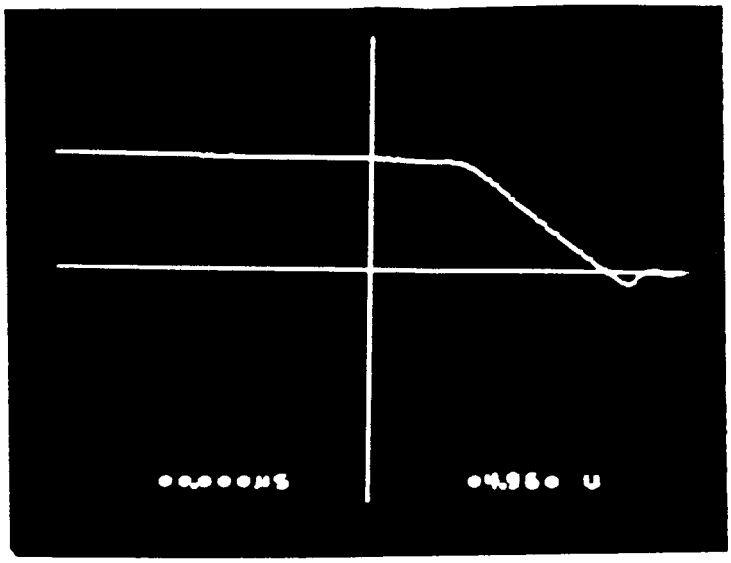


I_{FSM} = 1728A



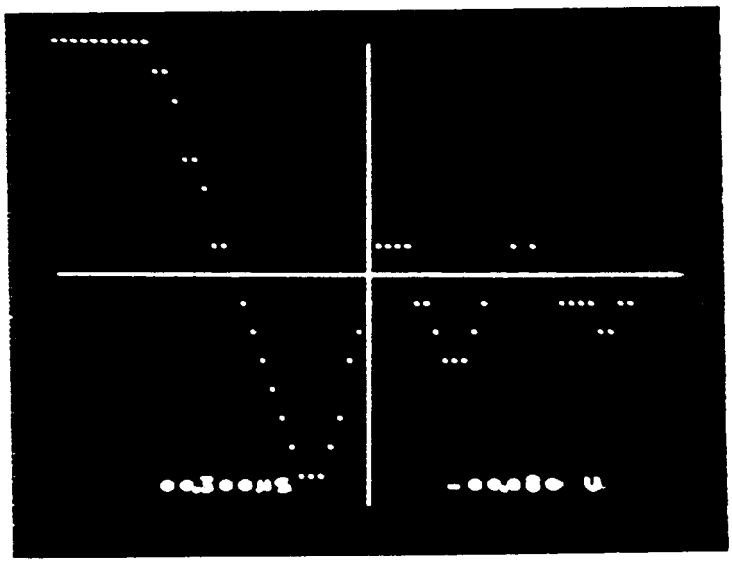
I_{FSM} = 728A

Figure 21, Nonrepetitive Peak Surge Current
Scale: 1000A per V



Scale: 1v = 10A

I_F = 49.6A



Expanded Scale:

t_{rr} = 300nS

Figure 22, Reverse Recovery Time

I_F = 50A, dI/dt = 25A/μs @ 25°C
(JEDEC Circuit)

DEVICE NUMBER	V_F @ 50A T_J = 25°C VOLTS	V_R @ 50μA T_J = 25°C VOLTS	V_R @ 5mA T_J = 100°C VOLTS	I_R @ 1000V T_J = 25°C μA	I_R @ 1000V T_J = 100°C mA	t_{rr} @ 50A di/dt = 25A/μS T_J = 25°C Nanoseconds	θ_{JS}; Tc = 50°C P_D = 62 WATTS t = 1 second °C/W	t_{rr} @ 50A di/dt = 25A/μS T_J = 100°C Nanosecond
1								
2	1.194	450V	200	85	9	.448	0.18	.662
3	1.245	40V	120	55	9.9	.475	0.16	.721
4	1.137	490V	150	80	9.6	.496	0.17	.779
5	1.190	450V	235	85	8.6	.503	0.17	.763
6	1.263	360V	85	80	11.5	.516	0.17	.706
7	1.182	440V	140	75	10	.456	0.15	.762
8	1.099	650V	200	85	9.6	.524	0.17	.783
10	1.279	390V	90	100	12	.464	0.18	.725
11	1.225	420V	200	100	8.5	.448	0.17	.674
12	1.156	550V	210	95	8	.476	0.19	.704
13	1.250	475V	190	140	9	.472	0.19	.729
14	1.284	420V	205	90	9.4	.476	0.17	.702
15	1.256	500V	175	92	10	.463	0.17	.718
16	1.128	640V	95	75	10.4	.535	0.17	.720
18	1.267	560V	130	90	9.8	.519	0.19	.808
19	1.444	230V	50	105	13.2	.428	0.18	.738
20	1.321	320V	70	100	12.5	.441	0.16	.680
21	1.282	325V	85	110	12	.454	0.19	.639
22	1.172	500V	125	95	10.5	.518	0.17	.673
23	1.201	390V	70	100	12	.490	0.18	.668
24	1.164	510V	150	75	10	.527	0.13	.718
25	1.156	260V	105	170	11	.512	0.15	.722
26	1.166	580V	40	80	12	.492	0.14	.716
28	1.347	53V	30	1mA	25	.434	0.18	.618

Figure 23, Final Test Data of Diode Engineering Models

DEVICE NUMBER	V_F @ 50A T_J = 25°C Volts	V_R @ 50 µA T_J = 25°C Volts	V_R @ 5mA T_J = 100°C Volts	I_R @ 1000V T_J = 25°C µA	I_R @ 1000V T_J = 100°C mA	t_{rr} @ 50A di/dt = 25A/µS T_J = 25°C Nanoseconds	θ_{JS}; Tc = 50°C P_D = 62 WATTS t_D = 1 second °C/W	t_{rr} @ 50A di/dt = 25A/µS T_J = 100°C Nanosecond
30	1.111	700	70	70	12.5	.542	0.14	.720
31	1.370	350	25	105	17	.439	0.20	.643
32	1.410	460	60	120	13	.523	0.14	.737
33	1.172	480	60	97	14.5	.467	0.16	.703
34	1.167	460	50	85	13	.509	0.15	.741
35	1.312	160	30	95	18	.507	0.19	.630
36	1.205	270	25	200	17	.461	0.18	.667
37	1.251	420	40	100	16	.461	0.16	.694
38	1.221	470	35	105	15.5	.481	0.17	.725
39	1.145	580	60	70	13	.530	0.14	.757
40	1.158	640	50	80	14.5	.482	0.14	.745
41	1.289	400	20	105	19	.466	0.21	.697
42	1.516	400	15	130	25	.444	0.14	.653
43	1.319	340	18	95	18	.434	0.18	.657
44	1.272	300	30	90	17.5	.455	0.29	.692
45	1.377	200	15	105	17	.427	0.16	.638
46	1.373	306	30	115	16	.432	0.19	.620
47	1.371	320	15	95	17	.431	0.20	.726
48	1.250	240	42	190	13.5	.518	0.12	.742
49	1.201	410	31	80	14.5	.503	0.19	.716
50	1.117	600	50	60	12	.550	0.16	.786
51	1.254	420	28	90	14	.489	0.18	.682
52	1.319	430	40	125	15	.443	0.21	.668
53	1.445	435	150	100	10	.447	0.20	.661

Figure 23, (cont.) Final Test Data of Diode Engineering Models

DEVICE NUMBER	V_{BE}(SAT.) I_c = 50A I_B = 6.25A Volts	V_{CE}(SAT.) I_c = 50A I_B = 6.25A Volts	h_{FE} I_c = 50A V_{CE} = 2.5	I_c (SAT.) h_{FE} = 12 V_{CE} = 2.5V AMPS	h_{FE} I_c V_{CE} = 2.5	V_{CEO} (SUS) I_c = 200mA 300μS Pulse Volts	V_{CBO} I_c = 100mA Volts	F.B.S.O.A. I_c = 60A V_{CE} = 10V 1 Cycle	θ_{JC} P_D = 300W I_M = 300mA t = 1 sec. °C/W	SWITCH TIME I_c = 50A; V_{cc} = 300V I_{B1} = I_{B^2} = 4.2A t_s μSec.	t_f μ Sec.
2	1.300	0.304	16.29	57.1	685.2	457	855	PASS	0.492	2.86	0.48
4	1.360	0.368	13.66	52.9	634.8	485	970	PASS	0.322	2.43	0.53
5	1.268	0.319	14.84	54.9	658.8	590	905	PASS	0.311	2.44	0.66
6	1.350	0.351	14.25	53.8	645.6	543	880	PASS	0.481	2.79	0.49
7	1.300	0.272	17.54	59.3	711.6	452	930	PASS	0.324	2.86	0.55
8	1.479	0.519	14.88	54.6	655.2	622	875	PASS	0.432	3.30	0.41
9	1.219	0.360	13.4	52.4	628.8	558	850	PASS	0.295	3.95	0.51
10	1.309	0.446	12.53	50.8	609.6	418	915	PASS	0.478	2.90	0.49
11	1.398	0.441	12.56	50.9	610.8	523	902	PASS	0.302	2.85	0.62
12	1.252	0.356	24.2	69.9	838.8	357	720	PASS	0.451	3.02	0.25
13	1.327	0.312	15.0	55.2	662.4	588	865	PASS	0.216	3.23	0.46
14	1.246	0.424	12.6	51.0	612	568	910	PASS	0.314	2.64	0.54
15	1.131	0.360	13.5	52.5	630	581	900	PASS	0.457	3.00	0.52
16	1.224	0.945	10.2	46.5	558	615	930	PASS	0.406	2.21	0.67
18	1.314	0.386	14.7	54.4	652.8	525	965	PASS	0.367	3.38	0.52
19	1.320	0.360	14.3	53.9	646.8	525	895	PASS	0.488	2.55	0.49
20	1.282	0.354	14.08	53.6	643.2	592	860	PASS	0.486	2.89	0.50
21	1.359	0.352	13.3	52.4	628.8	646	885	PASS	0.325	2.89	0.52
22	1.266	0.392	12.9	51.5	618	629	875	PASS	0.338	3.12	0.56
23	1.290	0.431	13.48	52.3	627.6	492	1050	PASS	0.298	3.54	0.77
24	1.343	0.335	14.58	54.3	651.6	520	950	PASS	0.486	3.14	0.51
25	1.223	0.297	17.01	57.6	691.2	478	925	PASS	0.592	3.73	0.66
26	1.344	0.366	13.7	52.9	634.8	519	905	PASS	0.483	2.83	0.54
27	1.234	0.346	13.44	52.6	631.2	639	890	PASS	0.286	2.99	0.46
28	1.260	0.349	14.2	53.7	644.4	499	900	PASS	0.294	3.01	0.56

Figure 24, Final Test Data of Transistor Engineering Models

DEVICE NUMBER	V_{BE}(SAT.) I_c = 50A I_B = 6.25A Volts	V_{CE}(SAT.) I_c = 50A I_B = 6.25A Volts	h_{FE} I_c = 50A V_{CE} = 2.5	I_c (SAT.) h_{FE} = 12 V_{CE} = 2.5V AMPS	h_{FE} I_c V_{CE} = 2.5	V_{CEO} (SUS) I_c = 200mA 300μS Pulse Volts	V_{CBO} I_c = 100mA Volts	F.B.S.O.A. I_c = 60A V_{CE} = 10V 1 Cycle	θ_{JC} P_D = 300W I_M = 300mA t = 1 sec. °C/W	SWITCH TIME I_c = 50A; V_{cc} = 300V I_{B1} = I_{B2} = 4.2A t_s μSec.	t_f μSec.
29	1.325	0.342	14.79	54.6	655.2	520	980	PASS	0.235	3.14	0.51
30	1.260	0.348	14.08	53.6	643.2	572	875	PASS	0.340	2.94	0.51
31	1.275	0.318	14.33	54.0	648	620	860	PASS	0.451	3.04	0.48
32	1.204	0.310	16.39	57.7	692.4	490	875	PASS	0.479	2.93	0.43
33	1.160	0.369	13.05	51.9	622.8	610	930	PASS	0.325	2.85	0.50
34	1.224	0.301	16.61	57.4	688	476	935	PASS	0.335	3.28	0.46
35	1.205	0.340	14.04	53.5	642	545	890	PASS	0.332	3.07	0.49
36	1.271	0.333	15.72	56.0	672	480	940	PASS	0.394	3.08	0.47
37	1.161	0.278	15.97	57.0	684	696	845	PASS	0.392	3.45	0.41
38	1.354	0.332	14.32	54.0	648	552	850	PASS	0.203	3.14	0.49
39	1.264	0.303	15.38	55.9	670.8	502	875	PASS	0.303	3.06	0.44
40	1.151	0.308	15.48	55.9	670.8	557	885	PASS	0.551	2.96	0.45
41	1.412	0.580	13.92	53.3	639.6	588	900	PASS	0.408	3.38	0.50
42	1.212	0.356	14.20	53.6	643.2	562	920	PASS	0.330	3.07	0.48
44	1.312	0.294	17.61	58.6	703.2	538	820	PASS	0.373	3.38	0.42
45	1.248	0.308	15.43	55.7	668.2	568	830	PASS	0.406	3.13	0.46
46	1.240	0.293	15.92	56.7	680.4	536	860	PASS	0.538	3.15	0.42
48	1.250	0.475	11.99	49.9	598.8	653	890	PASS	0.467	2.90	0.57
49	1.277	0.750	11.71	49.4	592.8	643	900	PASS	0.16	2.81	0.57
50	1.264	0.318	14.84	54.9	658.8	522	890	PASS	0.532	2.78	0.47
51	1.105	0.320	15.34	55.5	666	517	850	PASS	0.309	3.26	0.48
52	1.350	0.500	15.92	56.1	673.2	562	885	PASS	0.170	3.25	0.43
53	1.214	0.600	11.18	48.5	582	642	200	FAIL	0.514	2.54	0.64
54	1.201	0.259	19.30	61.6	739.2	516	840	PASS	0.465	3.67	0.36
55	1.168	0.540	11.5	49.1	589.2	585	890	PASS	0.346	2.67	0.63
56	1.220	0.292	15.8	56.4	673.2	569	870	PASS	0.533	3.34	0.45

Figure 24 (Continued), Final Test Data of Transistor Engineering Models

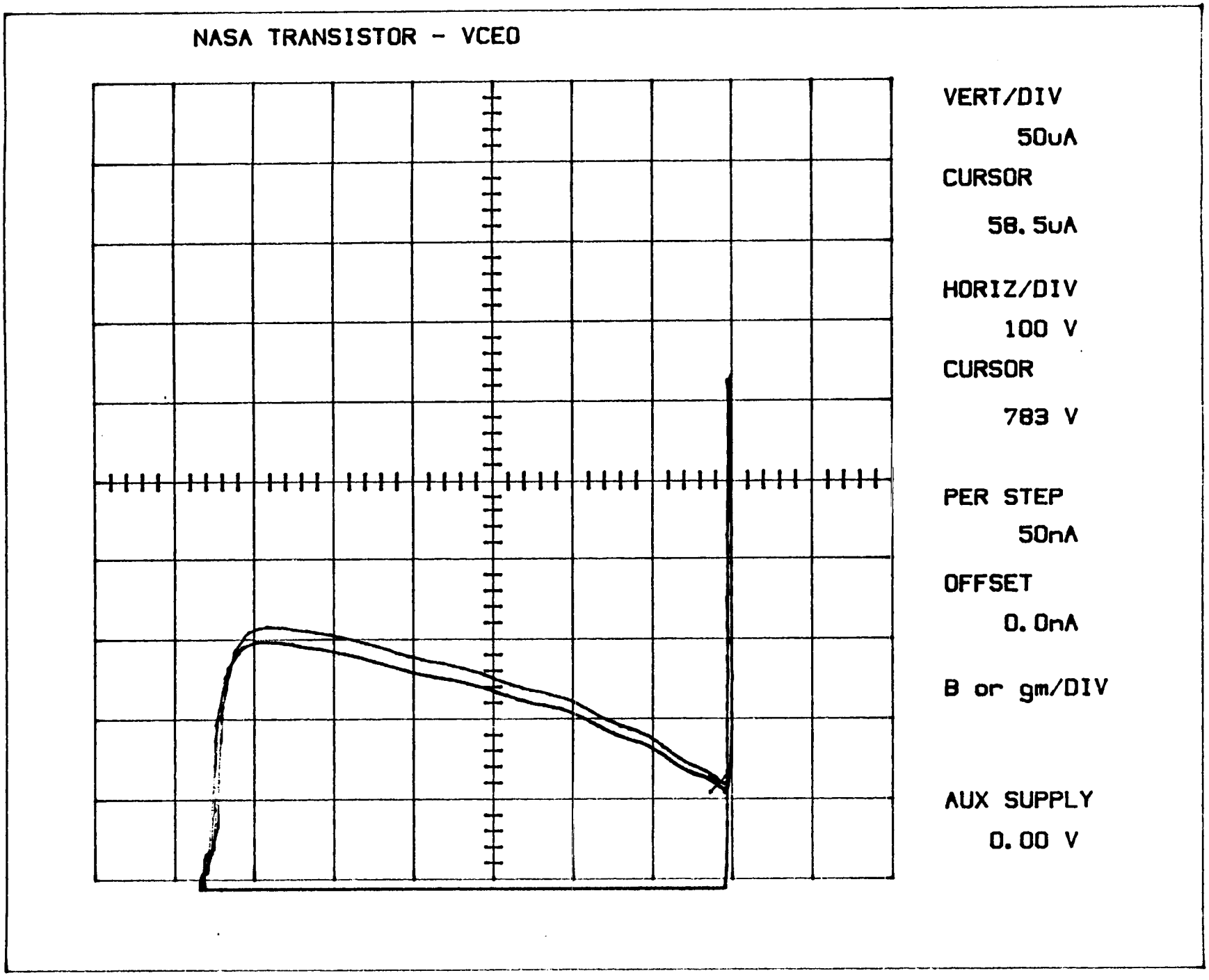

NASA TRANSISTOR - VCEO
VERT/DIV
50uA
CURSOR
58.5uA
HORIZ/DIV
100 V
CURSOR
783 V
PER STEP
50nA
OFFSET
0.0nA
B or gm/DIV
AUX SUPPLY
0.00 V

Figure 25

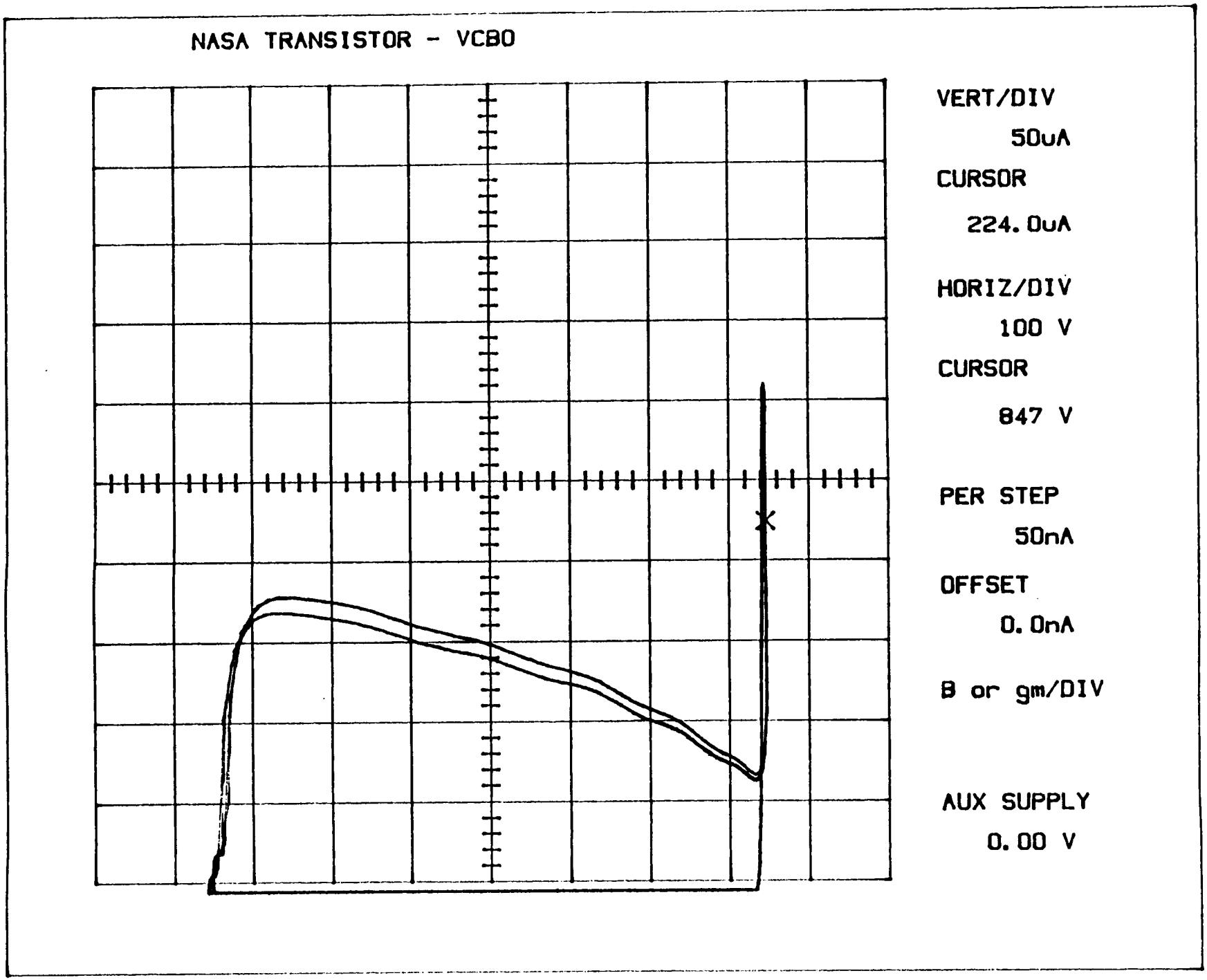

NASA TRANSISTOR - VCBO
VERT/DIV
50uA
CURSOR
224.0uA
HORIZ/DIV
100 V
CURSOR
847 V
PER STEP
50nA
OFFSET
0.0nA
B or gm/DIV
AUX SUPPLY
0.00 V

Figure 26

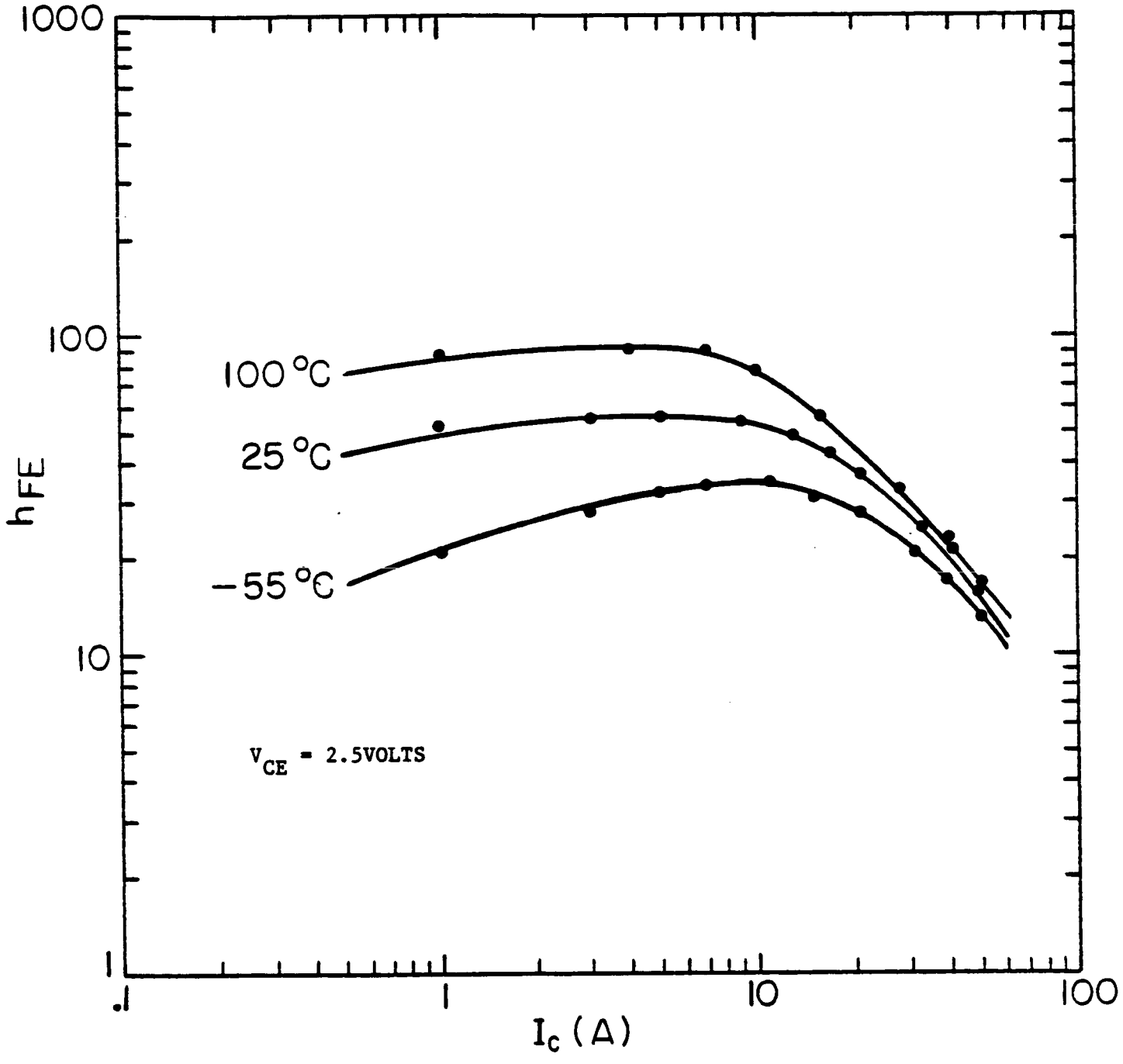


Figure 27, DC Current Gain (h_{FE}) vs. Collector Current (I_c)

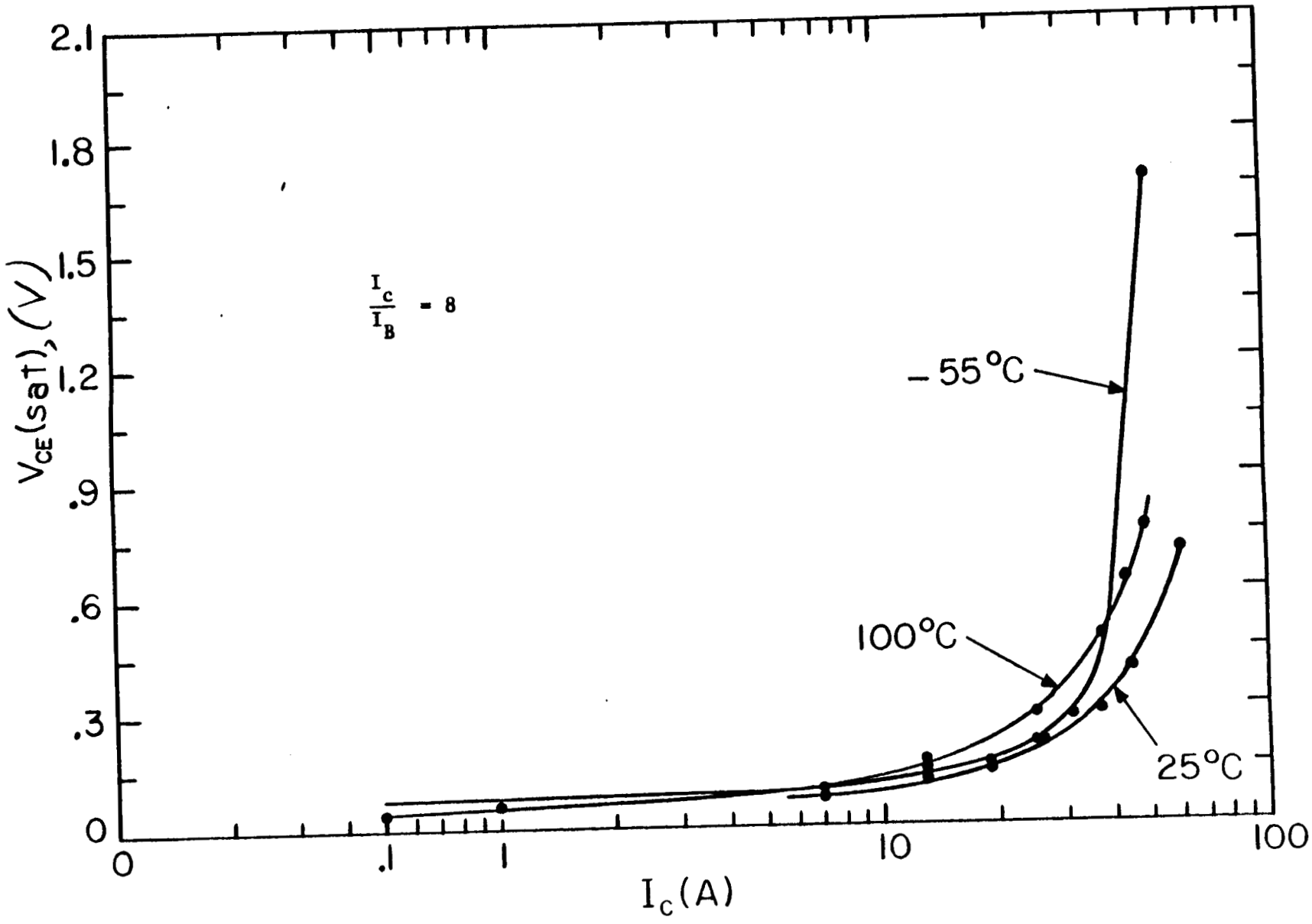


Figure 28, Collector - Emitter Saturation Voltage [V_{CE}(sat)] vs. Collector Current (I_c)

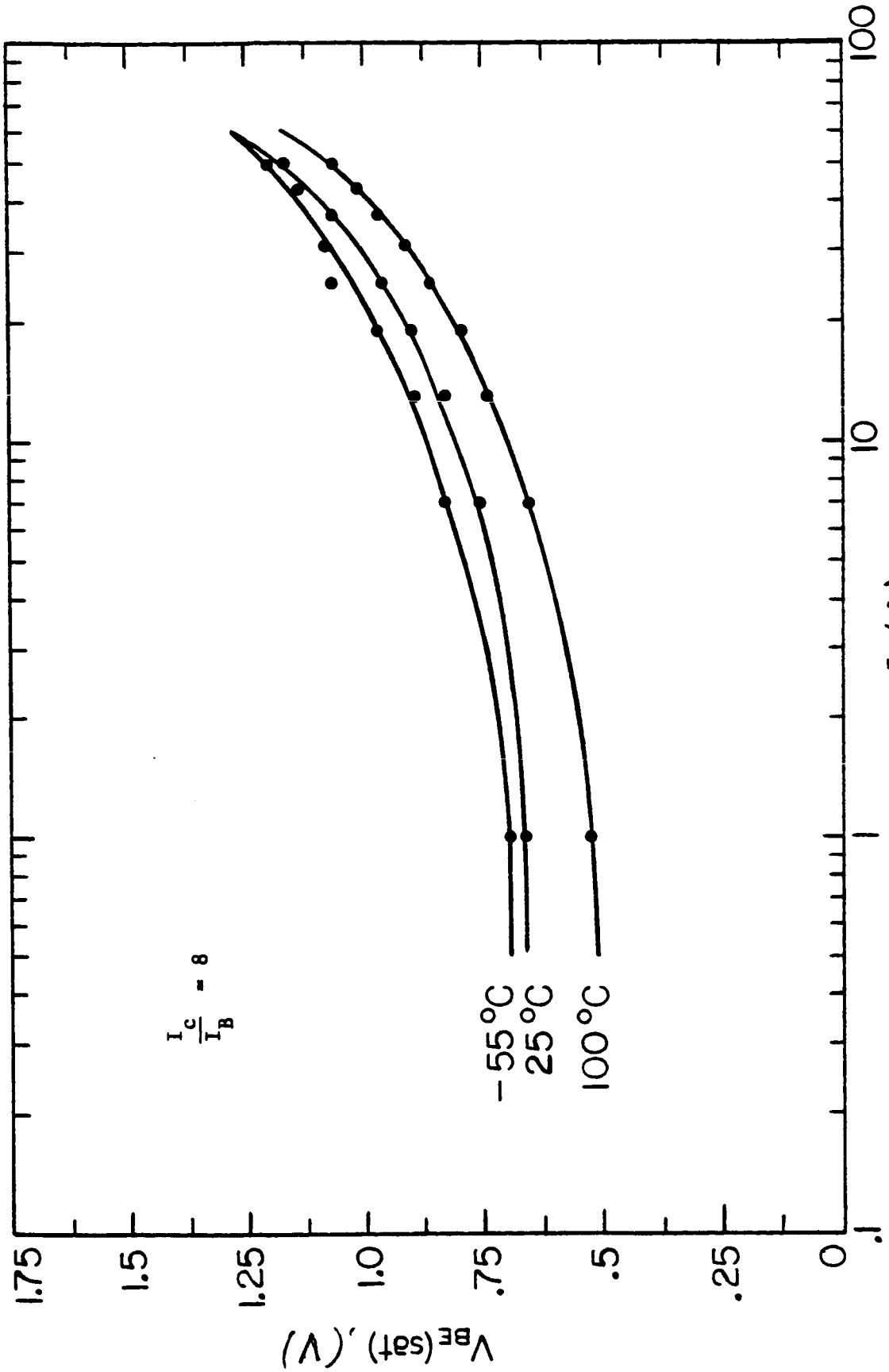


Figure 29, Base - Emitter Saturation Voltage [V_{BE} (sat)] vs. Collector Current (I_c)

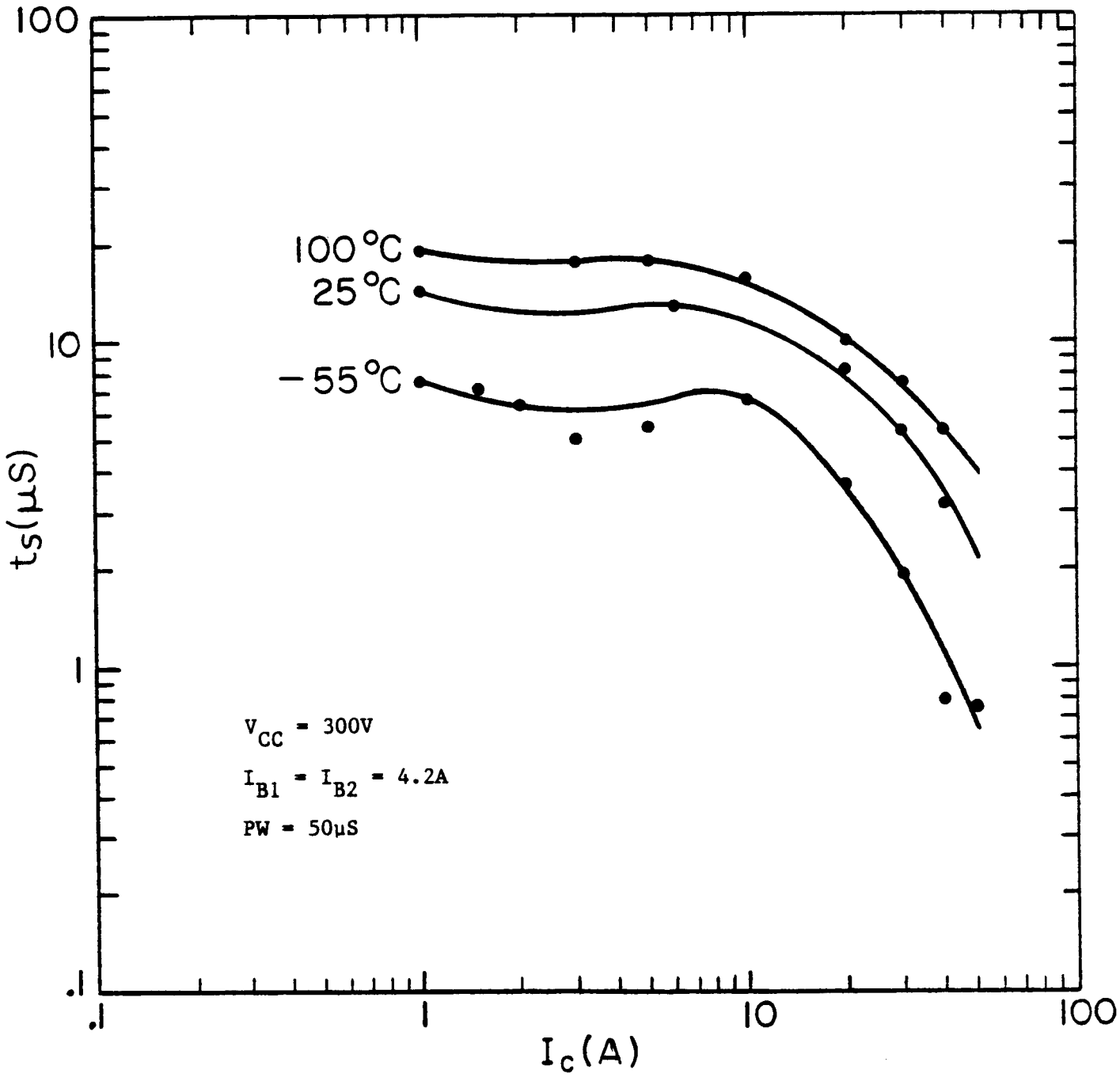


Figure 30. Storage Time (t_s) vs. Collector Current (I_c)

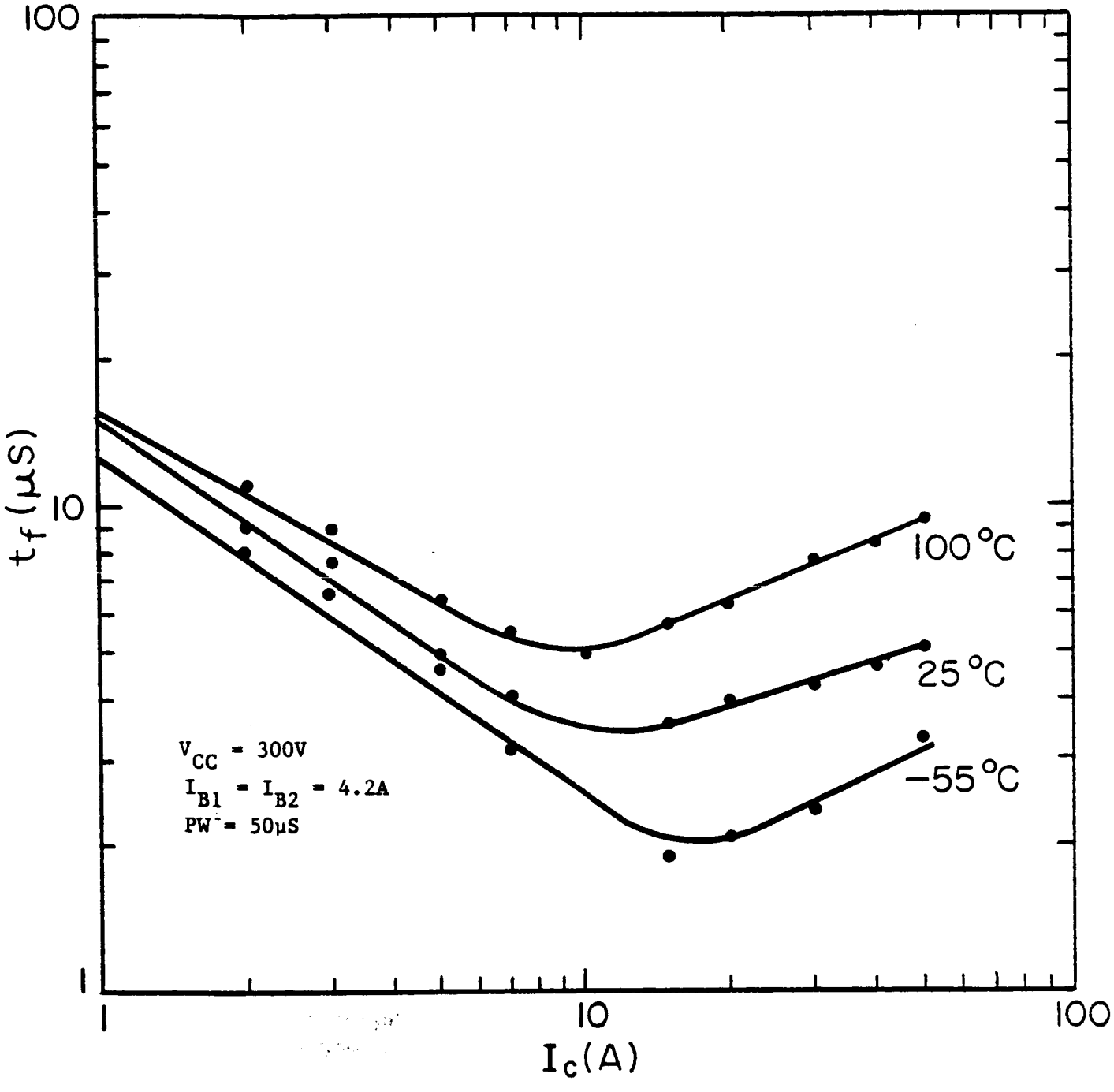
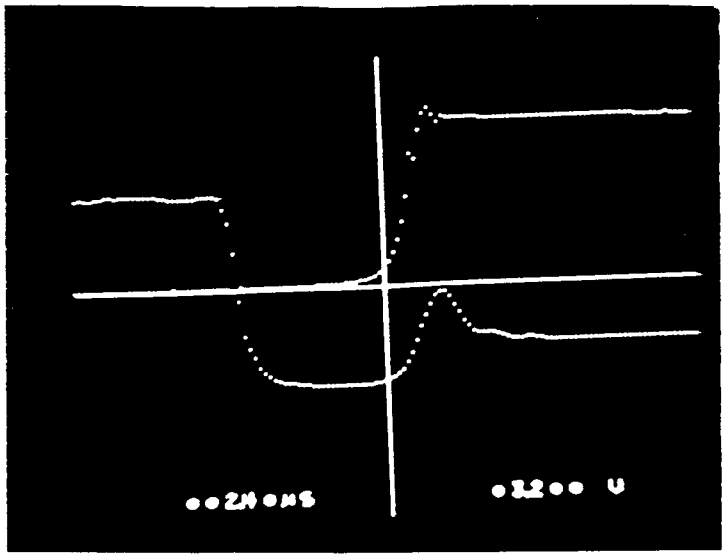


Figure 31, Fall Time (t_f) vs. Collector Current (Ic)

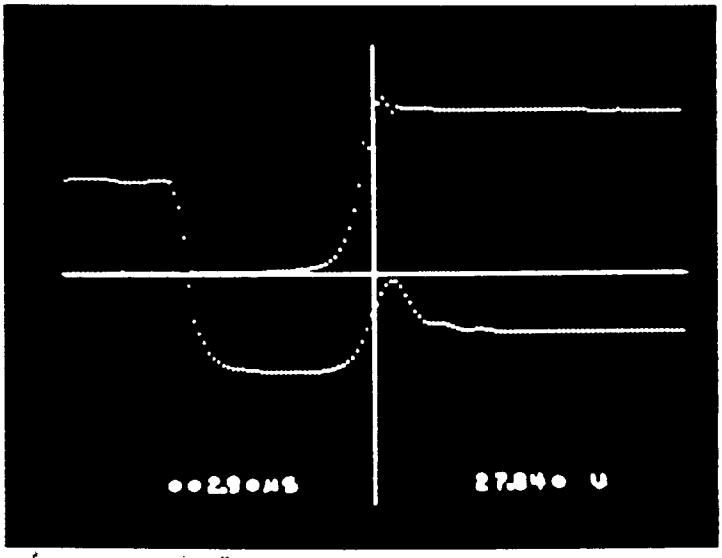


V x 10

$t_s = 2.4 \mu s$

Storage Time (t_s)

@ V_{cc} = 32V (approximately 10% of total)



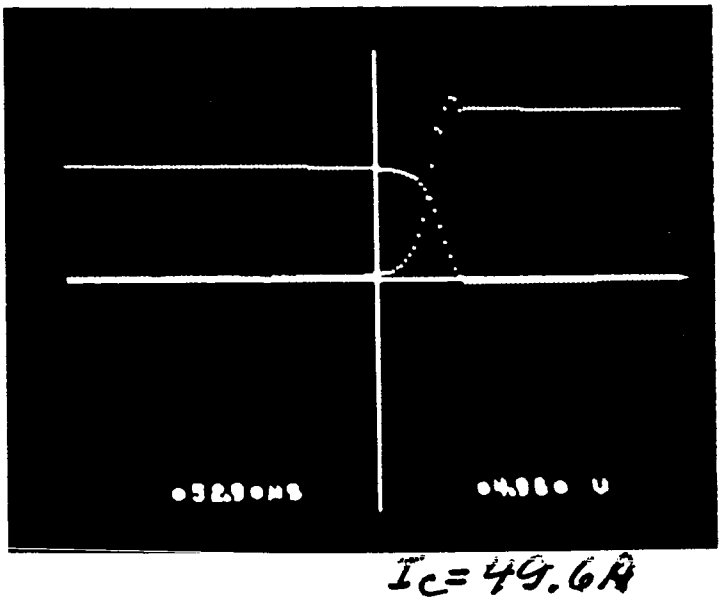
V x 10

$t_{off} = 2.5 \mu s$

Turn-off Time (t off)

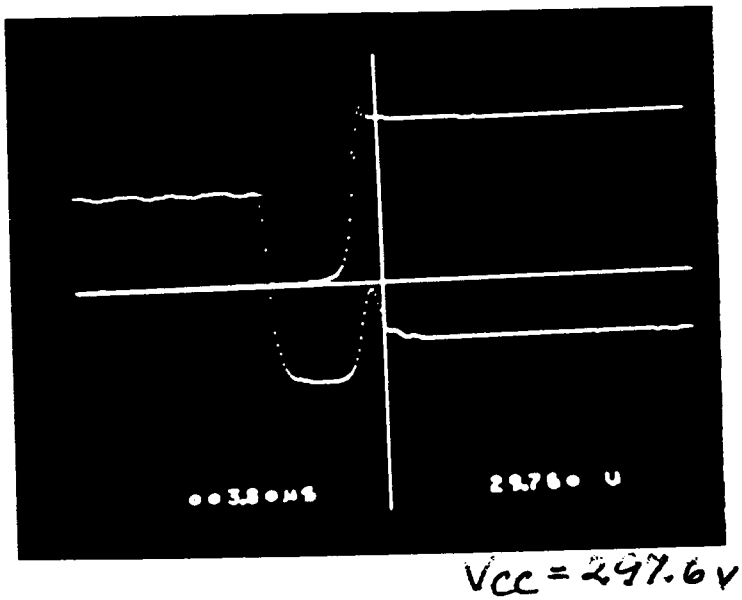
@ V_{cc} = 278.4V

Figure 32, Storage Time (t_s) and Turn-off Time (t off)



I x 10

Collector Current (I_c)
Amplitude Display



V x 10

Collector Voltage Supply (V_{cc})
Amplitude Display

Figure 33, Collector Current (I_c) and Collector Supply Voltace (V_{cc}) Display for Switching Time Measurements in Figure 32

C-2

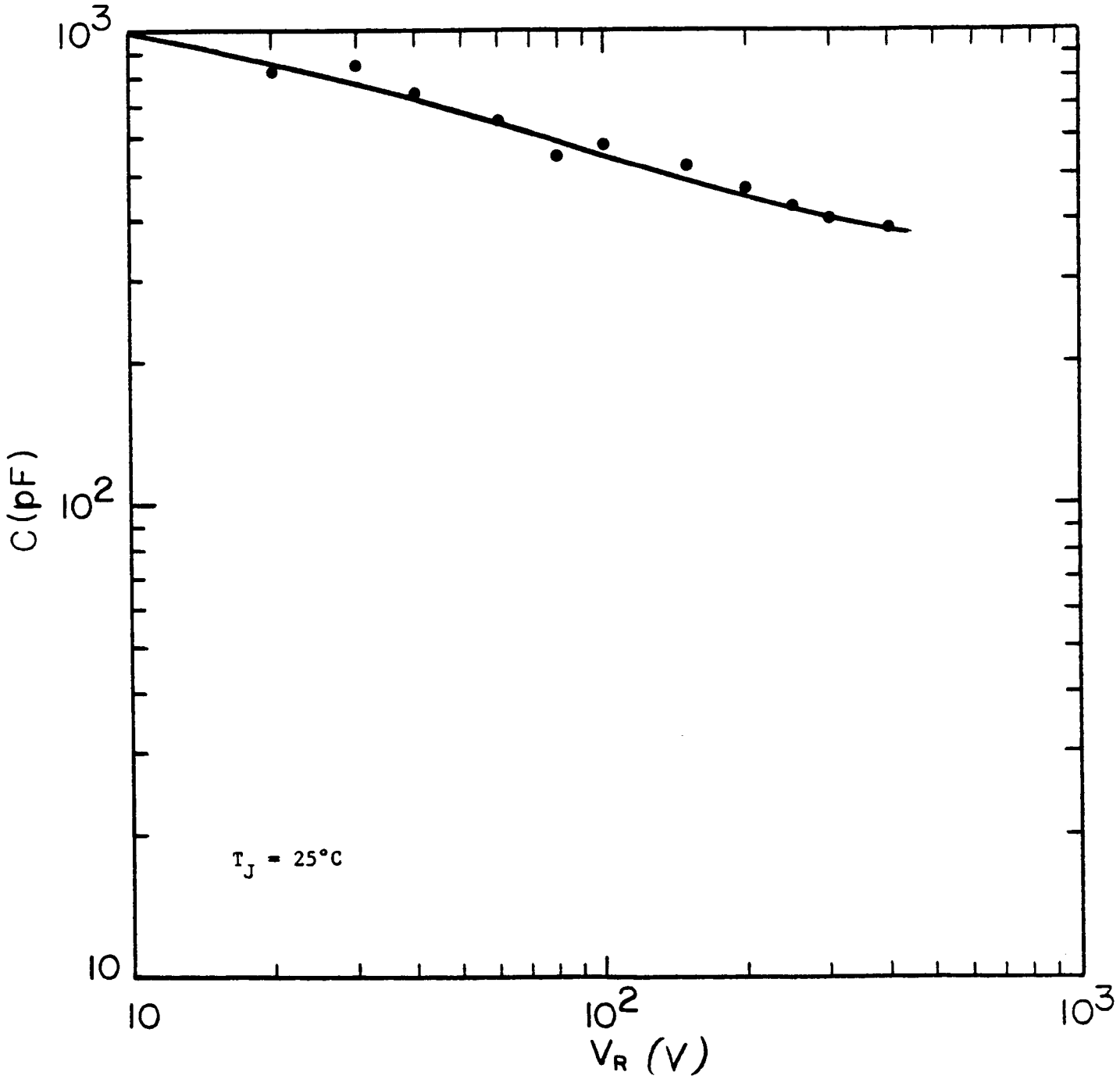


Figure 34, Diode Interterminal Capacitance (Anode to Cathode)

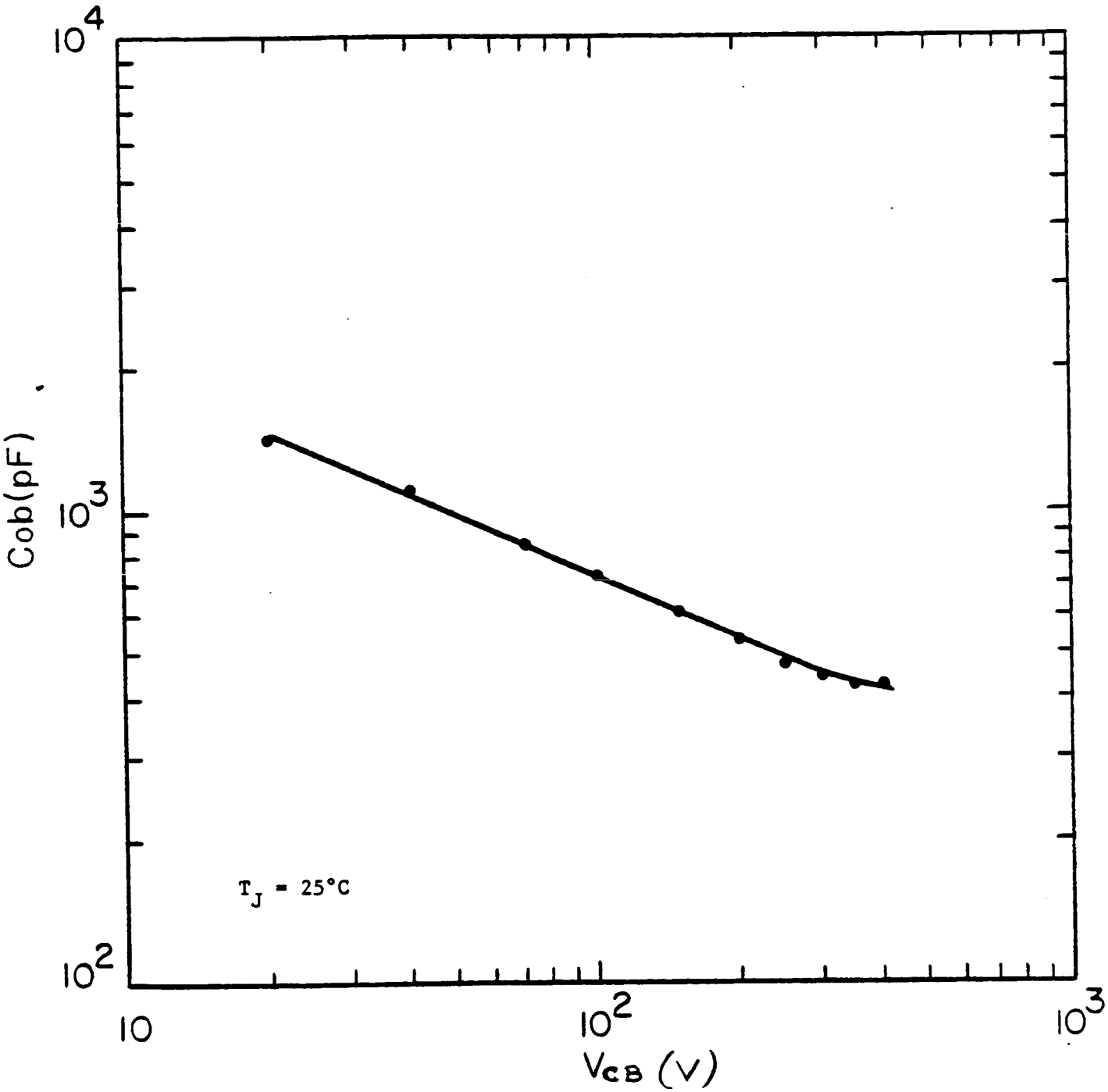


Figure 35, Transistor Interterminal Capacitance (Collector to Base)

DEVICE NUMBER	t_{rr} @ 125A di/dt = 25A/μS T_J = 25°C Nanoseconds	V_F @ 125A T_J = 25°C VOLTS	V_R @ 500μA T_J = 25°C VOLTS
21	537	1.59	250
22	600	1.36	20
23	580	1.42	440
24	611	1.35	490
25	585	1.32	1210
26	575	1.36	1290
27	544	1.60	1195
28	522	1.63	40
29	525	1.65	48
30	629	1.28	1320
31	525	1.62	1280
32	604	1.60	750
33	552	1.38	1250
34	582	1.36	1230
35	592	1.62	1240
36	545	1.43	1125
37	543	1.45	1005
38	562	1.44	790
39	609	1.34	1315
40	581	1.37	1300

Figure 36, Diode Evaluation at 125A Rating

7.3.3 Thermal Resistance

Thermal resistance is used to reference thermally sensitive characteristics of a device. It is also the bases of a circuit design for establishing and specifying thermal limits under operating conditions. The importance of it can not be over-emphasized.

It is essential that reliable thermal resistance measurements are obtained using standard measurement methods and to focus attention of both manufacturers and users on the thermal management of the high power semiconductor devices.

Diode Thermal Resistance Measurement

In order to measure thermal resistance of the diode, the forward voltage (V_F) is monitored with respect to temperature. This data relates the thermal resistance of the diode to the V_F of the diode.

Measurements are taken at a controlled 50°C. Since the readings are to reflect the junction to heat sink thermal resistance, it is necessary to control and hold the temperature of the heat sink at a constant 50°C. The temperature of the heat sink, after every measurement, is recorded. The equipment consists of an IBM-PC, an oven, a Fluke D.V.M., a constant current power supply, a relay matrix and an IEEE interface.

By using an IBM-PC and interface boards (with A-D's, parallel I/O and serial communications) this test is also automated. The test is started at a heating time of 10 ms and is finished with a 30 second heating time. Before every thermal resistance measurement, the PC monitors the heat sink temperature to insure a stable 50°C. Also, a delay between each test of 5

times the previous heating time is used to allow the junction to return to 50°C. The individual thermal resistance measurements consist of a cold V_F reading (taken at the selected current), an applied heating current (a selected dc current based on the chip size and for a selected period of time) and a hot V_F reading (taken with the same current used for the cold reading). Also, during the time the current is applied, a power dissipation measurement is taken. With this information and the K-factor obtained from the calibration test, the thermal resistance junction to heat sink is calculated.

$$R\theta_{JS}=\text{delta } T/PD$$

where $$\text{delta } T=(V_F \text{ cold}-V_F \text{ hot})K\text{-factor}$$
$$PD=\text{power dissipation}$$

Plots of the individual $R\theta_{JS}$ readings vs. time of diode samples are shown in Figures 37 and 38.

Transistor Thermal Resistance Measurement

The transistor thermal resistance tester is a self contained NPN transistor/darlington tester which measures the base-emitter voltage before and after a set power pulse has been applied. The tester then senses the change in the voltage from the base to the emitter (delta V_{BE}) and the change is displayed on the front panel, digital volt meter. This delta V_{BE} can be used to calculate the temperature rise and thus the thermal resistance ($R\theta_{JC}$) of the device. The tester can also heat the device up slowly and measure the base-emitter voltage at a preselected temperature. A plot of the junction temperature and V_{BE} can be made on the device under test.

The tester has a liquid cooled heat exchanger designed to

cool the devices during a 1 second and greater thermal resistance test. This heat exchanger was used to maintain the case temperature at 50°C when the $R\Theta_{JC}$ vs. time plots submitted in this report were generated. (Figure 39)

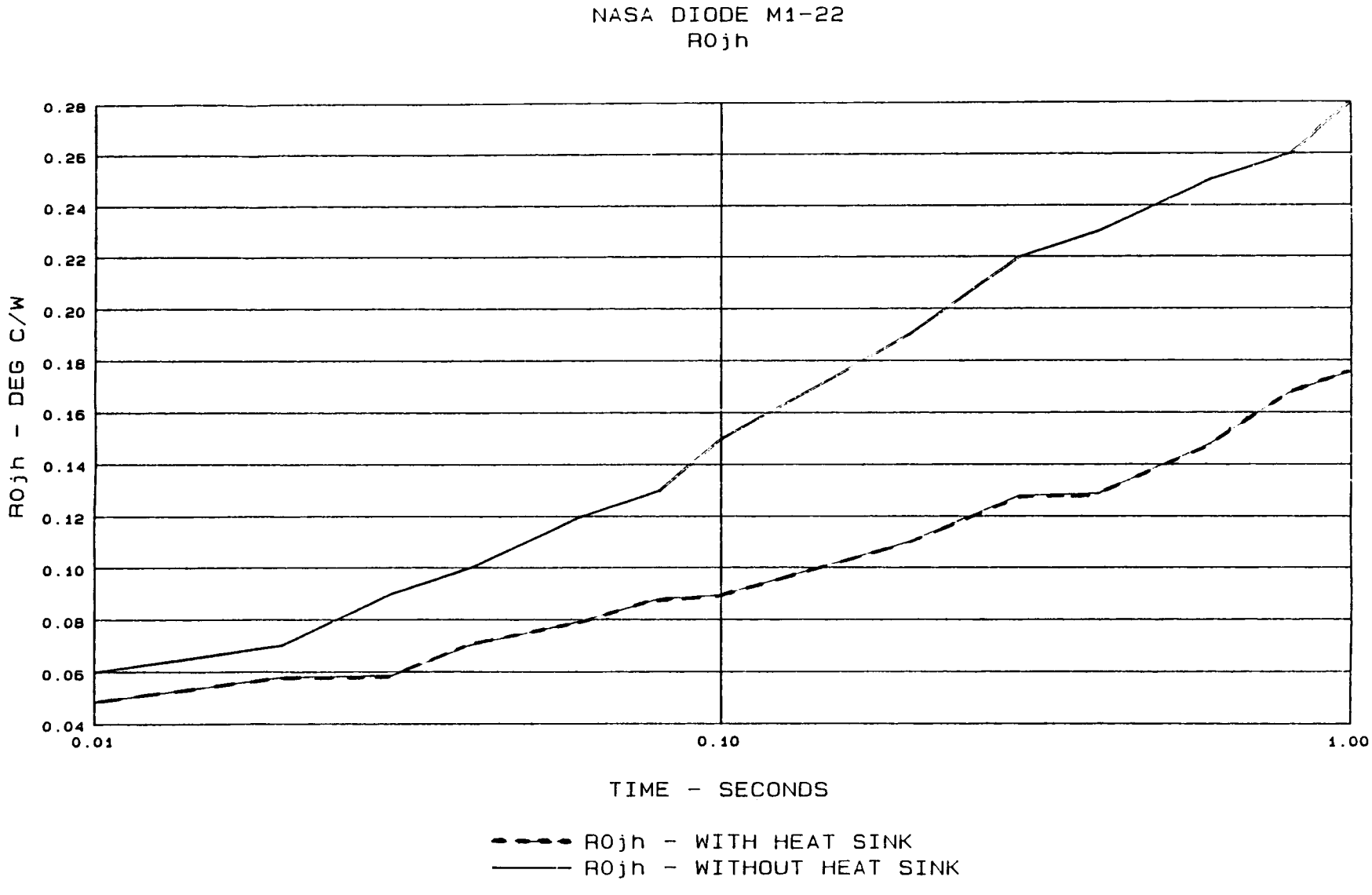


Figure 37, Diode Thermal Resistance (0-1 second)

M1_22

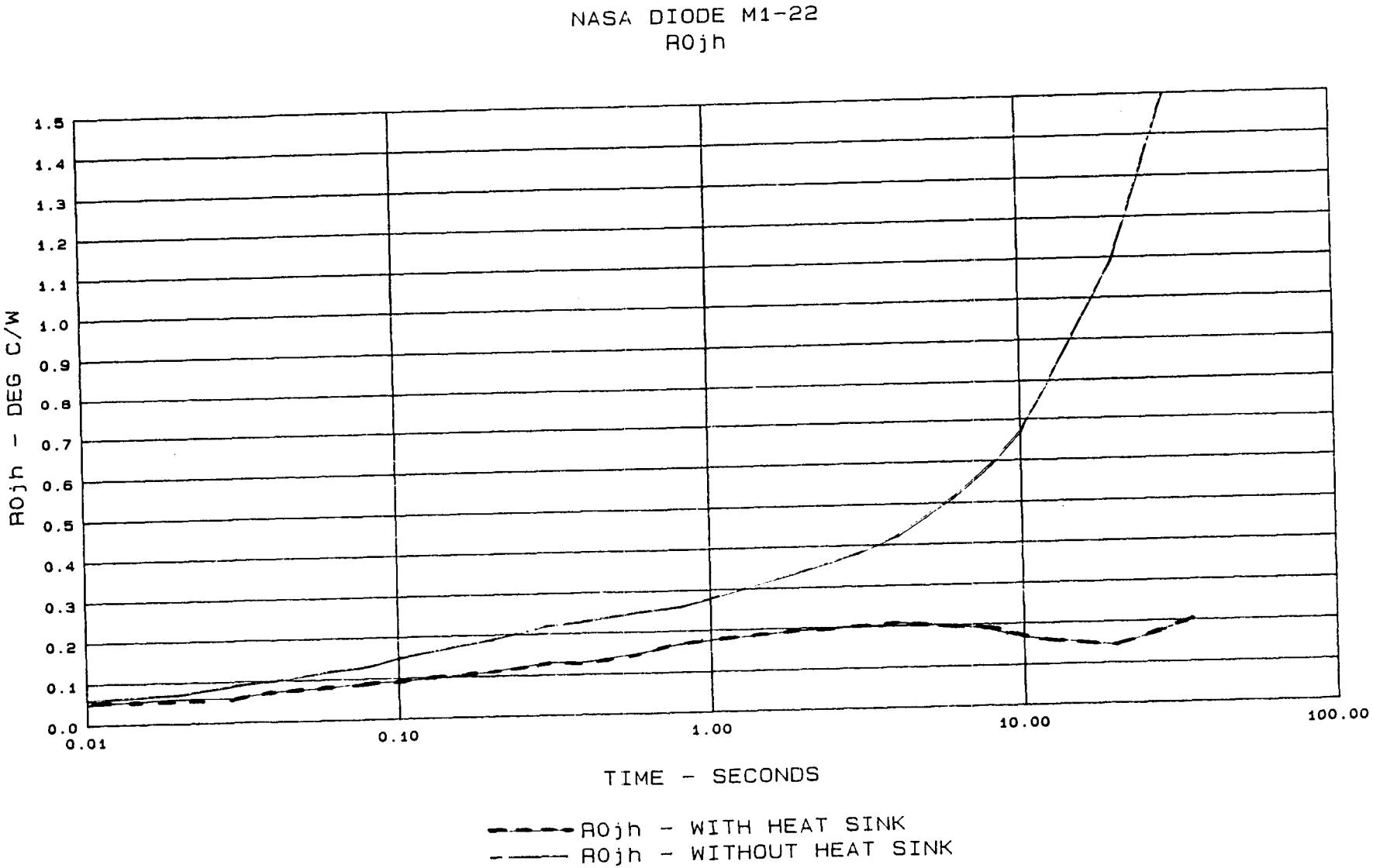


Figure 38, Diode Thermal Resistance (0 to 10^{+} seconds)

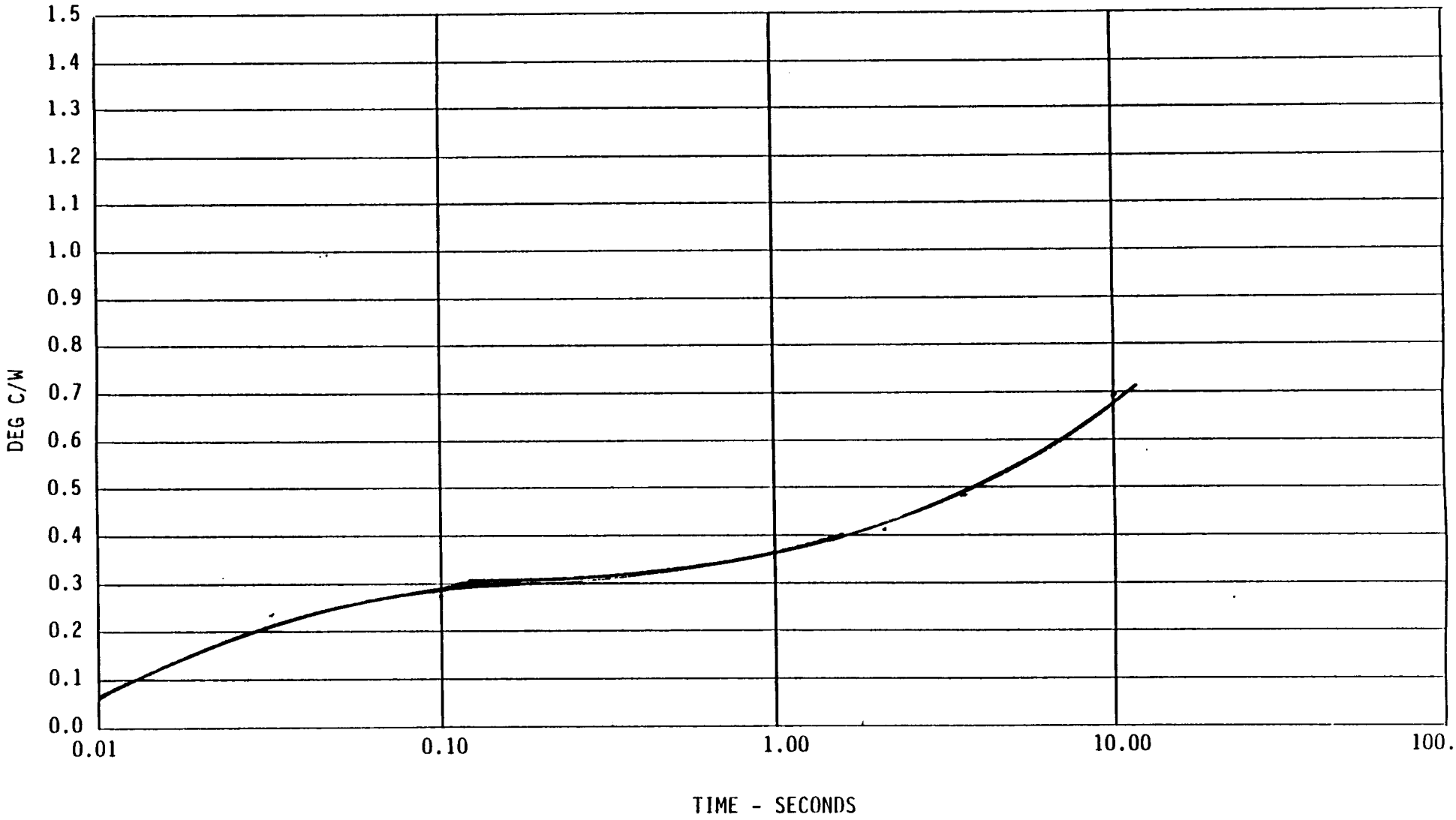


Figure 39, Transistor Thermal Resistance

8.0 RELIABILITY TESTS

To maintain uniform methods and have readily available standard references of the reliability evaluation, MIL-STD-750C (test methods for semiconductor devices) have been specified as the bases to define the methods, conditions and limits of the tests performed. Electrically tested and accepted random sample sets at a minimum of ten transistors and ten diodes have been evaluated for each of the reliability performance tests outlined in the plan.

Only the test method, major test conditions and the results are listed in the following outline. Complete documentation of the test processes, detailed conditions and the evaluation results on data acquisition is available at P.T.C. to NASA Project Manager for review.

8.1 Test Plan and Results

8.1.1 Environmental Tests

Thermal Shock (temperature cycling)

Method: 1051.2

Conditions: -65°C to 125°C, 5 cycles

Results: No failures

High Temperature Life (non operating)

Method: 1031.4

Conditions: 150°C, 500 hours

Interim electrical check points at 168, 304 and 500 hours

Results: No failures

Hermetic Seal (fine leak)

Method: 1071.2

Conditions: "H_1", (helium fine leak test, fixed method)

Reject limit: 1×10^{-7} at $m.cm^3/s$

Results: 3 failures of 20 units tested

8.1.2 Mechanical Characteristics Tests

Shock

Method: 2016.2

Conditions: 1) Acceleration of 50 G peak for 0.5 milliseconds

2) Six directions (+Z, -Z, +Y, -Y, +X, -X) of blows

Results: No visual damage

No electrical failures

Constant Acceleration

Method: 2006

Conditions: 50 G centrifugal force

Results: No physical damage

No electrical rejects

9.0 PROJECT CONCLUSIONS

The design, development, fabrication and evaluation of the power semiconductor package for the Space Station applications have been successfully completed.

The package specifications required new approaches in design, material selection and processing techniques. In choosing the metal components, and dielectric materials, particular attention has been given to the energy loss considerations, both electrical and thermal. New materials used for this type of application include liquid crystal polymer plastic and polymer (Parylene) coating.

The package outline fits within a rectangular envelope of 1.445 by 2.250 by 1.640 inches. The complete diode and transistor packages weigh 84.5 grams and 86.0 grams respectively. Electrical hardware supplied with each unit weighs additional 9.0 grams.

In accordance with NEMA standards, the diode and the transistor packages comply with the ratings of 1400 volts and 900 volts peak.

A number of problems encountered in the processing, resulting from particular material selection or component design, will be resolved during the proposed prototype fabrication of these devices as part of P.T.C.'s new POWERMODE product line. Some of the recommended and intended areas for improvements are solder reflow assembly, component plating, subassembly brazing and surface passivation of the chip.

Material improvements can be made by more directly evaluating: 1) Metglas R/S solder made by Allied Corporation, 2)

directly bonded copper to ceramic substrate made by Toshiba, Doduco and BBC, 3) external terminals made of chrome-copper or zirconium-copper to improve mechanical strength and electrical conductivity and, 4) the metallized ceramic plate made of aluminum nitride that is in the evaluation stages at several potential suppliers.

The unique package features developed under this contract will allow P.T.C. to enter the power semiconductor market with a new series of devices intended for the commercial market. P.T.C. will market them as the POWERMODE series, consisting of power transistors, darlingtons and diodes. This development will allow P.T.C. to compete in a market dominated by several foreign competitors.

The initial introduction of the POWERMODE series will include 50 ampere, 500 and 1000 volt transistors and 125 ampere, 1200 volt diode, followed by a 125 ampere, 500 volt darlington.

10.0 ACKNOWLEDGMENTS

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Darrell C. Devance

Gerry Ludlow

Lee Wagner

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12.0 APPENDICES

12.1 SPECIFICATIONS FOR SPACE STATION POWER SEMICONDUCTORS

SPECIFICATIONS FOR SPACE STATION POWER TRANSISTOR

Case Temperature = 25°C unless otherwise specified

SYMBOL	CHARACTERISTICS WITH TEST CONDITIONS	VALUE/UNITS
$V_{CEO}(sus)$	Collector-Emitter Sustaining Voltage @ I_C=200mA, I_B=0, 300 μs pulse	500 V
V_{CBO}	Collector-Base Voltage @ I_C=.300mA	600 V
$h_{FE}I_C$	Gain-Collector Current Product @V_{CE}=2.5V	600
$I_C(rated)$	Gain Rated Collector Current @h_{FE}=12, V_{CE}=2.5V	50A
$I_C(cont.)$	Continuous Collector Current	100A
$I_C(peak)$	Peak Collector Current, Pulsed	200A
h_{FE}	DC Current Gain @ I_C=50A, V_{CE}=2.5V (Pulsed with duty cycle<2%)	12
I_B	Base Current, continuous	17A
$V_{CE}(sat)$	Collector-Emitter Saturation Voltage @I_C=50A, I_B=6.25A	1.0V
$V_{BE}(sat)$	Base-Emitter Saturation Voltage @I_C=50A, I_B6.25A	1.3V
T_J	Operating and Storage Junction Temperature Range	-50 to 200°C
t_d	Turn-On Delay Time	0.1 μs
t_r	Rise Time (10 to 90% I_C)	1.0 μs
t_s	Storage Time (time from $I_B \leq 0$ to $0.9I_C$)	2.5 μs
t_f	Fall Time (90 to 10% I_C)	0.5 μs

All switching times measured with resistive load, supply voltage VCC=300V, I_C=50A, I_{B1}=I_{B2}4.2A using 50 to 100 μs pulses with duty cycle<2%.

12.2 SPECIFICATIONS FOR SPACE STATION DIODE

Case Temperture = 25°C unless otherwise specified

SYMBOL	CHARACTERISTICS WITH TEST CONDITIONS	VALUE/UNITS
V_R	DC Blocking Voltage, T_J=100°C (also called Peak Inverse Voltage, PIV)	1000V
V_{RSM}	Peak Non-repetitive Reverse Voltage, T_J=100°C	1200V
I_R	Reverse Leakage Current @V_R=1000V	
	@T_J=25°C	0.050mA
	@T_J=100°C	5mA
I_F	Average Forward Current @ T_J=100°C	50A
I_{FSM}	Non-repetitive Peak Surge Current (1/2 cycle, 60 Hz, Resistive Load)	600A
V_F	Forward Voltage @I_F=50A	1.5V
T_J	Operating Junction Temperature Range	-65 to 175°C
T_{STG}	Storage Temperature Range	-65 to 200°C
t_{rr}	Reverse Recovery Time @T_j=100°C I_F=50A, dI/dt=25A/μs (JEDEC Circuit)	0.5 μs
I_{RR}	Peak Reverse Recovery Current I_F=50A, dI/dt=25A/μs (JEDEC Circuit)	5A

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