NASA CONTRACTOR REPORT 177470

Advanced Components for Spaceborne Infrared Astronomy
Final Report

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Prepared for
Ames Research Center
under Contract NAS2-12154

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Space Administration

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ADVANCED COMPONENTS FOR SPACEBORNE INFRARED ASTRONOMY

CONTENTS

SUMMARY

Basic improvements in the technology of low noise read-out systems for low background infrared detectors have been demonstrated. Using discrete JFET integrating amplifiers at their optimum temperature of 55 K, read noise less than 7.5 electrons in 128 seconds of integration has been obtained. Two models of single channel integrators are now available, the JF-77 for use between 50 and 80 K and the JF-4 for lower temperatures. A 1 x 16 linear array of complete integrators on a single integrated circuit has been developed and will be made available in the near future. These devices offer the possibility of building large, extremely sensitive arrays of low background infrared detectors.

The successful operation of a superconducting stepper motor has been demonstrated. The motor shows a three fold increase in torque over conventional motors operating at room temperature. The success of the motor stems from the use of superconducting coils in conjunction with developments in bearing for cryogenic use, rare-earth rotors, and motor cooling techniques. The current state of development will allow for the rapid development of motors optimized for specific applications.

An electronic switch capable of resetting cooled JFET integrating amplifiers has been developed. JFET integrating amplifiers that use this switch have demonstrated read noise of less than 10 electrons. The JFET reset device exhibits an extremely high "open" impedance and low leakage current. Capacitance is sufficiently low so as not to impair amplifier sensitivity. The effects of transient switching charges are minimized by a compensation technique and variable transient current problems inherent to devices of this type are overcome by external circuitry. An n-channel model has been incorporated into a commercially available JFET integrating amplifier that is optimized for operation at either 4 K or 77 K. A p-channel model has been incorporated into the 16-channel integrating amplifier array.

STATEMENT OF TOTAL LABOR HOURS

In compliance with part 1, section F.3 of the contract, a statement of total labor hours is hereby included:

Main project	10,394 hours
Engineering change 1	1,805 hours
Total	12,199 hours

ADVANCED COMPONENTS FOR SPACEBORNED INFRARED ASTRONOMY

INTRODUCTION

This report is divided into three parts. The first part covers the main body of work carried out under the contract and is concerned with development of a new technology for detectors used in space experiments and other very low background applications. The second part is devoted to studies of techniques for the design and manufacture of small superconducting motors and actuators for use at very low temperatures encountered in certain space applications such as cryogenically cooled telescopes. The third part includes work on a new type of cryogenic reset switch using JFETs.

PART ONE: INTEGRATING JFET AMPLIFIER DEVELOPMENT

I. INTRODUCTION TO PART ONE

The primary objective of this project was to develop a new type of integrating amplifier in order to measure very small currents produced by sensitive infrared detectors. Performance requirements dictated that the completed product must operate at the very low temperatures to which the infrared detectors are cooled, 4 K or lower, and it must measure currents as small as one electron per second. As the result of this NASA SBIR contract this goal has been met and Infrared Laboratories now supplies single channel amplifiers which can be used to measure such extremely small currents in a routine fashion. In addition, an integrated circuit or "silicon chip" has been developed which contains 16 of these amplifiers. These devices will enable users to build both linear and two dimensional arrays consisting of infrared detectors attached to these read-out devices. By all indications this new technology will be suitable for use in future NASA missions and will find many other applications where very small amounts of electrical charge must be measured.

This report presents the background which led to the need for advancements in read-out technology and therefore to the initiation of this project. The report then summarizes the project activities and gives detailed descriptions of the products developed under the contract. Also included is a brief discussion of additional work that could lead to further product improvements.

II. BACKGROUND

The decision by NASA to build two cryogenically cooled infrared telescopes and place them in earth orbit to obtain observations of the sky at infrared wavelengths focused considerable attention on the then state of the art detector technology. The first of these projects, IRAS, was designed around 62 discrete infrared detectors using cooled MOSFET read-outs. The second project, the Space Lab 2 Infrared Telescope, was to use an alternate technology similar to that in use on ground based telescopes, namely cooled JFETS. A group of scientists at the Steward Observatory of the University of Arizona led by Frank Low was chosen by NASA to participate in both of these projects. The work carried out at Steward showed that selected JFET amplifiers could operate at LN-2 temperatures and were quite sensitive and highly reliable. In light of this work, the subsequent failure of the

IRAS focal plane due to the catastrophic failure of the MOSFET devices led to the decision to replace the MOSFETs with cooled JFET devices.

Infrared Laboratories was chosen to design and build the individual modules containing the JFET trans-impedance amplifiers. The flight qualified modules were delivered on time, at cost and within specification. The great scientific success of IRAS was due in large part to the timely development of this alternative technology for measuring the relatively small currents produced by IRAS' sensitive spaceborne infrared detectors. The trans-impedance amplifiers were made using selected, matched pairs of J230 transistors manufactured by Siliconix and had an effective read noise in one second of about 500 electrons. The two transistors and a heater resistor were suspended on dacron threads inside a light tight enclosure. The same design has since been used in the COBE satellite and a number of other applications.

Motivated by the success of IRAS and a desire to build even more sensitive equipment for future NASA missions, such as the Space Infrared Telescope Facility (SIRTF), the Steward group explored ways to make their amplifiers more sensitive. Experiments showed that a simple form of JFET integrating amplifier using a matched pair as a differential amplifier can reach a read noise in one second of 10 electrons (Low 1984). This represented an improvement in sensitivity of a factor of 50 relative to the earlier IRAS results. For reference, the circuit published by Low is shown in figure 1.

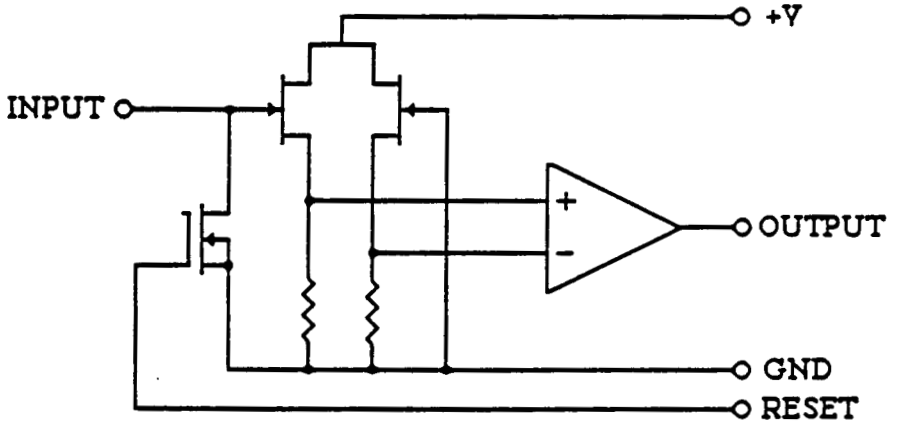

FIGURE 1. Simple JFET integrator, Low 1984

Two instruments were proposed to NASA based on this new method of building very sensitive hybrid arrays and NASA chose to support studies of both instruments. This research effort is continuing at the University of Arizona as part of the advanced detector program sponsored by NASA.

It was clear, however, that much work remained before practical devices could be made in quantity. Two important areas for improvement were immediately identified: (1) reduction of the operating temperature to reduce the problems associated with heating of the JFET devices to 70 K and (2) reduction of the read noise to levels below 10 electrons. This reduction is especially important for space applications where extended integration times as long as 500 seconds are necessary. Still other unresolved issues remained: (1) develop-

ment of a superior JFET based reset switch (2) allowance for compensation of deposited charge on the reset switch (3) simplified hybrid construction of large arrays (4) increased thermal stability of the basic circuit proposed by Low with respect to its thermal environment and (5) investigation of operation at temperatures as high as 80 K for applications that permit higher operating temperatures.

III. PROJECT SUMMARY

It was in the context described above that this SBIR project at Infrared Laboratories was begun in April 1985. The two major objectives of the Phase 2 contract were to reduce both the noise and operating temperature of JFETs used as simple integrators in the circuit developed by Low (1984). At first it was thought that a MOSFET would be used for the reset function. Later it was decided to explore the use of JFETs for this purpose and an engineering change was made. This part of the project is described in Part III of this report. Further modifications in the direction of the program took place when it was realized that, with the success of the JFET reset switch, it is possible to design and build an integrated circuit containing all the components on a single chip. Because a number of channels can be included on each chip, this greatly facilitates the construction of large arrays. It was soon realized that there would be a need for two product lines, the first consisting of single channel integrators for use with individual detectors and the second consisting of integrated circuits which would make possible the design and construction of large arrays. The following discussion recounts the efforts which led to the development of these products. The properties of the actual devices are reported in the section IV.

Initial tests were conducted using a simple circuit to investigate gain and DC stability below 77K. Satisfactory performance was recorded down to 40K (Low and Alwardi 1986) yet in order to build a practical system capable of operating in this regime it was necessary to improve the basic circuit. The balanced source follower with active load, as shown in Figure 2, was found to solve the problems associated with thermally induced drifts and the need for an output voltage level near ground (Low and Alwardi 1987). The two bias resistors included in the circuit provide reverse bias to control the channel current (I_{DS}), and add negative feedback. The circuit is stable without these resistors and they may be deleted if in the design of the JFETs it is possible to provide for the desired current in the channel without the use of reverse bias. The circuit found in Figure 2 is the basis upon which all work has been conducted.

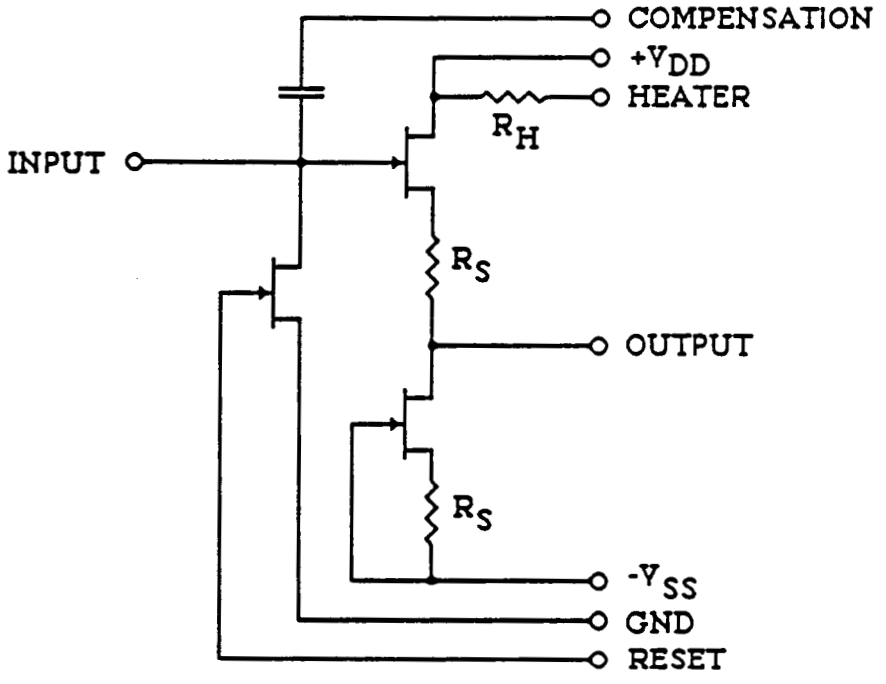

Figure 2. Improved JFET integrator circuit with JFET reset

Other important aspects of the circuit shown in Figure 2, are the JFET reset switch and the reset compensation capacitor. Their functions are, respectively, to discharge signal accumulated on the input gate of the integrator at the end of an integration cycle and to reduce the amount of injected charge left by the reset switch when it opens to begin the next integration cycle. Both of these enhancements are quite important and greatly improve the performance.

A somewhat similar circuit configuration, in which the active load is connected in order to achieve a voltage gain larger than unity, was studied. Despite its apparent advantage this circuit was abandoned because it suffers from the Miller effect which increases the input capacitance and degrades the performance of the integrator.

III. A. The Siliconix Developments

As originally proposed, a contract was negotiated with Siliconix to build a number of different types of JFETs using several geometries with systematic variation of critical processing parameters, such as doping levels in the channel and in the gate. Before the first phase of this work began it was decided to investigate the low temperature properties of several different types of standard production transistors to serve as a guide in the experiments that would be undertaken. Low temperature testing was carried out on two single JFET devices, the J230 and the J210/NZF, and on two monolithic dual devices, the U402 and the U440/NNZ. Siliconix supplied test samples of all these N-channel transistors and they were characterized both for noise performance as integrators and for operation at the lowest possible temperatures. The NNZ was favored since it consists of the matched JFET pair required in the new circuit of Low and Alwardi (1987). The NNZ has both a low input

capacitance and very high transconductance. Also, it has the highest doping levels of all possible candidate devices manufactured by Siliconix and it performed well in tests at temperatures as low as 30 K. A selection process carried out by Siliconix yielded NNZ devices with low enough pinch-off voltage to satisfy our requirements. All work with these devices was conducted at the die level. A pinch-off voltage near one volt is required in the circuit to minimize power dissipation, V_{DS}, and the value of reverse bias needed.

The first group of experiments at Siliconix were aimed at studying the effects of increasing the doping concentrations by a factor of up to 10 in the channel and in the gate using the standard NNZ mask set. Difficulties were encountered and several production runs of wafers were processed before functional devices were obtained. Unfortunately, the performance of these new NNZ based experimental devices was quite disappointing and further efforts along these lines were set aside. It became clear that in order to maintain pinch-off voltages low enough for the circuit to perform well, the thickness of the channel must be too small for acceptable control during processing. This appears to set a practical upper limit to the doping levels that may be used in these types of JFETs.

Since excellent performance was achieved using selected die from existing wafers, it was decided to base the single channel integrators on a supply of these units. The NNZ serves as the balanced source follower with active load and the NZF serves as the reset device. Performance is discussed below.

III. B. The Burr-Brown Developments

At the outset of the project, contact was made with Burr-Brown since they manufacture a line of low noise JFET input operational amplifiers using a proprietary process which gives room temperature noise performance quite similar to that measured for the best Siliconix devices. Tests showed that these devices function quite well as cryogenic amplifiers. At the request of Infrared Laboratories, experimental JFETs were made by Burr-Brown to address the issue of current noise in the contacts at low temperature. The results from these tests were inconclusive and the effort was temporarily set aside. The contacts that are used on all these devices do not differ significantly from the standard used in most room temperature devices.

Burr-Brown continued to make progress with the design of their JFET and they provided improved units for test as cryogenic amplifiers and switches. These results were quite encouraging and it was decided to pursue the design of an integrated circuit. Key elements in this decision were: (1) the fact that the Burr-Brown process provides the necessary isolation between each device on the chip and (2) the uniformity of the process is high enough that it appeared likely the yield would be high enough to produce the 48 transistors on each chip required for a 1 x 16 array.

With concurrence of the technical monitor, Dr. Craig McCreight, it was decided to reprogram resources to concentrate on the development of a 1 x 16 channel integrated circuit using all of the circuit refinements that had been proven out in the single channel integrators . In collaboration with the engineering staff at Burr-Brown, directed by Dr. William Lillis, a design was developed using their "minimum geometry" p-channel JFET. The detailed design of the integrated circuit that resulted from this effort is shown in Figure 3.

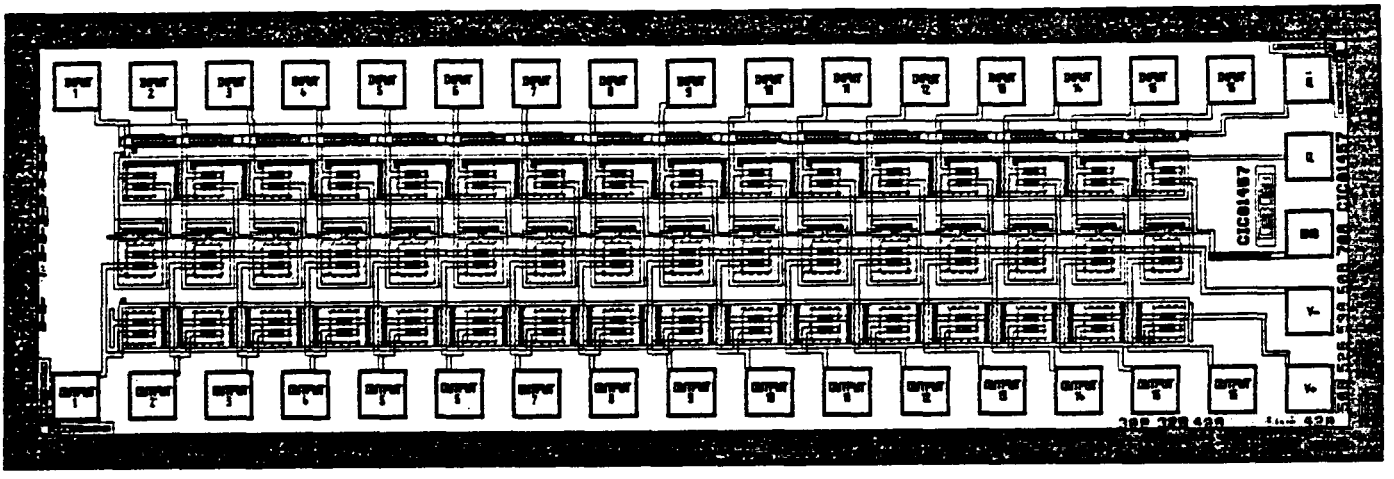

Figure 3. Final design of the 1 x 16 JFET integrator array

The circuit diagram is shown in Figure 4 and a photograph of the completed chip is shown in Figure 5. As can be seen, the basic circuit is the same as in Figure 2 but the 16 channels are connected by 5 common lines to minimize the external connections. The inputs and outputs are all arranged on opposite sides of the chip for isolation. Note that the two bias resistors used to limit the current in the circuit of Figure 2 are not included here. This requires that the current drawn by the two junction transistors be controlled in their manufacture. The size of the chip is 3.5 mm by 1.0 mm.

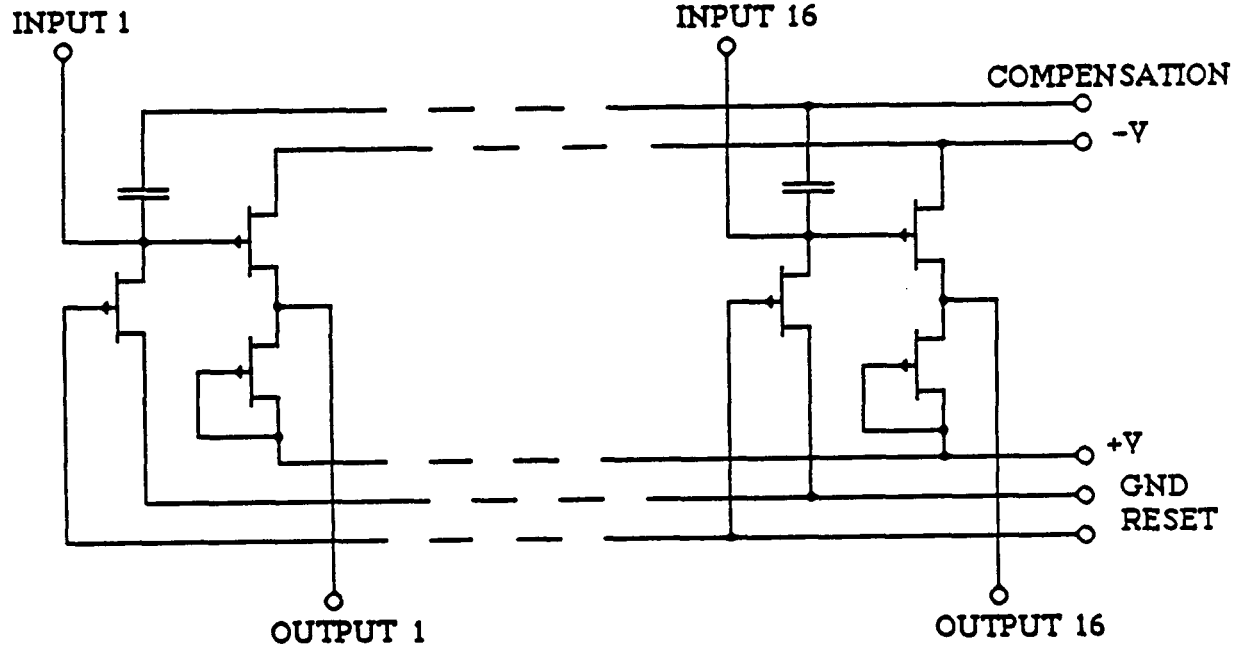

Figure 4. Circuit diagram of the 1 x 16 JFET integrator array

The first production run of wafers was completed in December 1987 and yielded functional devices with good characteristics. However, testing revealed three problems that required correction: (1) the gate structure was too small to provide full control of the channel current (2) the current at 77 K was too high for all intended applications and (3) the matching between the two transistors in each of the 16 amplifiers was not close enough to maintain the dc offset voltage within the specified range of a few millivolts. It was decided to modify the mask set and produce a second generation of chips.

The second generation 1 x 16 chips were completed in the final quarter of the contract. Twelve wafers were processed in order to cover the predicted range of parameters needed for operation over the full 80 to 50 K temperature range. Test samples from two wafers were studied at 77, 65 and 50 K and significant improvements were achieved in all areas relative to the first generation devices. The yield is of great significance for large array applications. Here the results are as predicted: more than 90 percent of the chips on the two wafers studied are functional and at least 50 percent meet the full set of specifications. Other performance characteristics are given in the next section of this report. Clearly there is much more testing to be completed before a final assessment can be made. However, it is established that the basic specifications for these devices have been met or exceeded. The marked improvement of the second generation of chips gives support to the view that future engineering changes may be undertaken with a high level of confidence.

III. C. The Infrared Laboratories Developments

In addition to the design and testing of both single and array versions of the JFET integrators, Infrared Laboratories personnel have been engaged in solving the problems of packaging these devices. There are two versions of the single channel devices, one designed for use over the temperature range 80 to 50 K, where the JFET resides at the same temperature as the infrared detector to which it is connected, and the second designed for the range below 50 K, where it is necessary for the the JFETs to be thermally isolated from the detector environment and heated to the optimum operating temperature of about 55 K.

III. C. 1. The JF-77

Figure 6 shows a photograph of the unit designed for applications where thermal isolation is not desired. This is the model JF-77. Note that the discrete devices are mounted on a circular substrate made of alumina using conventional wire bonds for the interconnections. The header is a standard 10-pin TO-5 type used for operational amplifiers and similar applications. The connections from the hybrid substrate to the header pins are made using gold plated Cu wire and silver conductive epoxy. In this design, the electrical leads provide the physical support of the hybrid circuit and insure very high thermal conduction to the header. The package is hermetically sealed with one atmosphere of argon.

III. C. 2. The JF-4

Figure 7 shows a photograph of the model JF-4 unit designed for applications where thermal isolation between the active components and the environment is needed. This is achieved by means of metalized pyrex glass rods used as the interconnections between the hybrid circuit and the header pins. In contrast to the JF-77 model, the support system provides a very high degree of thermal isolation, of order 1 to 2 microwatt/K for the temperature range of interest. The use of metalized pyrex in this fashion is a key element in this design and contributes greatly to the mechanical and thermal characteristics of this new system for packaging cryogenic components. Note the addition of a heater resistor that is used to maintain the optimal operating temperature.

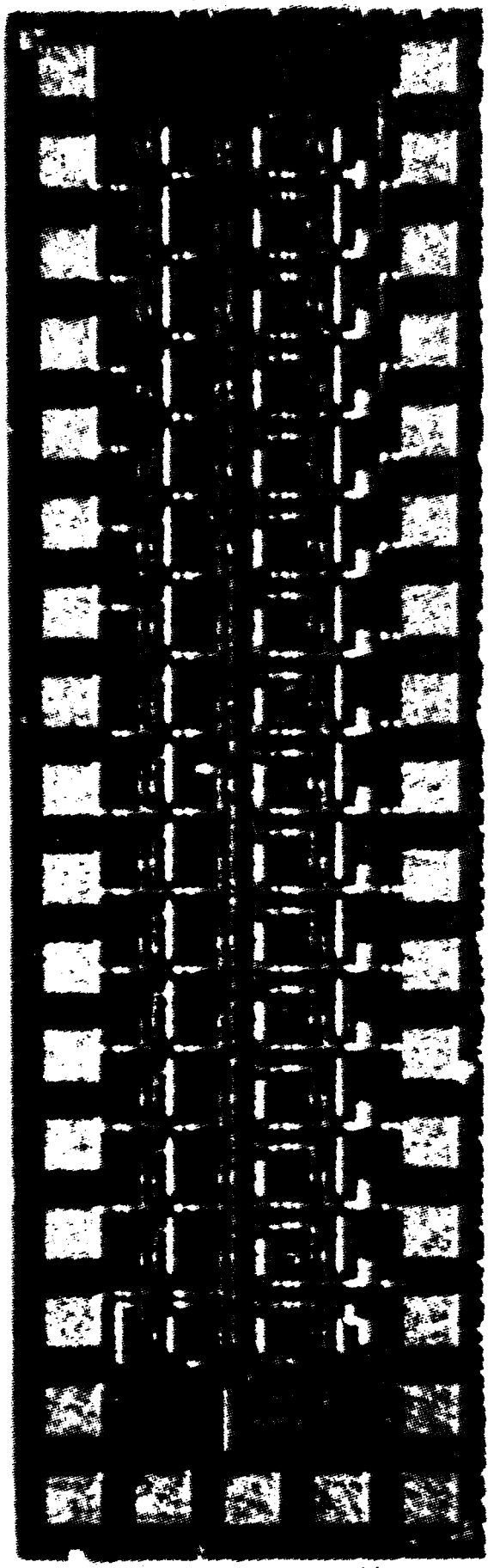

Figure 5. Photograph of the 1 x 16 integrator array.

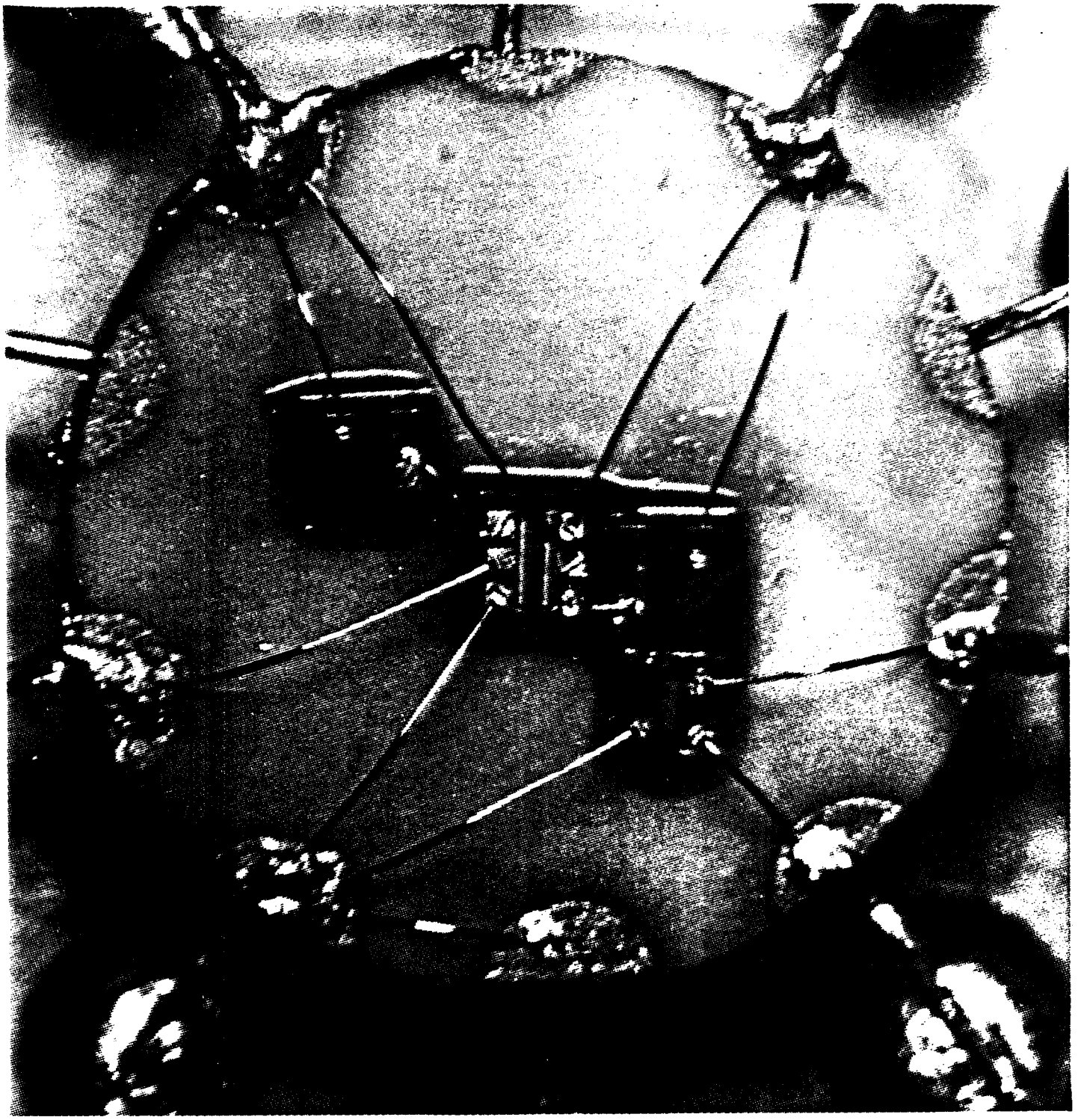

Figure 6. Photograph of the JF-77

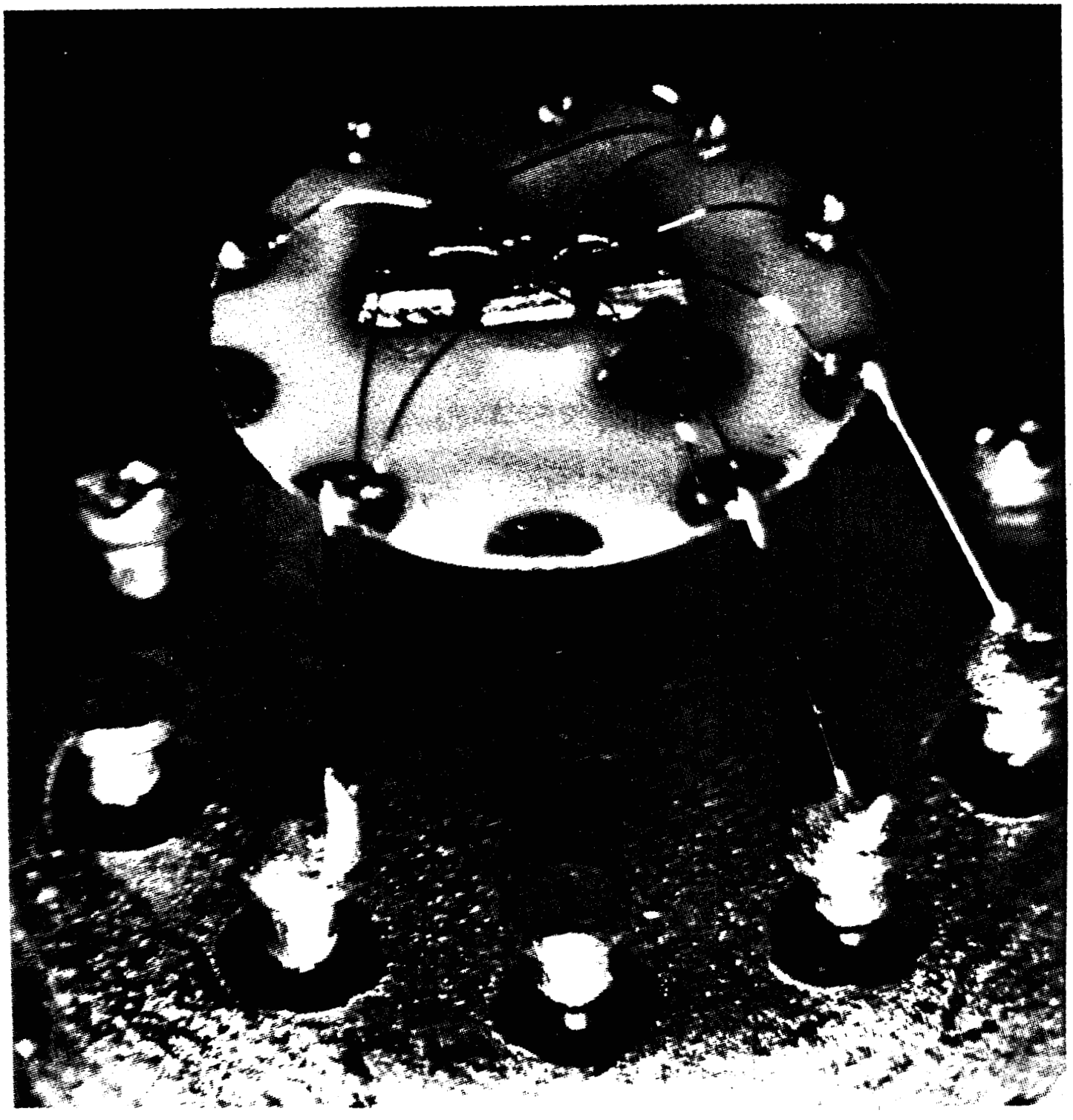

Figure 7. Photograph of the JF-4

An important consideration in the design of the JF-4 is its ability to withstand mechanical shock and vibration during the launch phase of spaceborne applications. Preliminary vibration tests have been carried out at room temperature using a sinusoidal amplitude of 0.5 cm at frequencies up to 100 Hz. No failures or resonances were encountered and a module has been supplied to a potential user who is in the process of making more quantitative tests. These tests are intended to demonstrate flight qualification for the Ariane launcher and will be carried out at low temperatures.

Another form of severe stress that was considered in the design is the thermal shock and differential contraction when the module is cooled to very low temperatures. Careful attention was given to using materials that are both thermally compatible and have low absolute values of expansion. The header is made of glass and a kovar alloy, a combination long used in cryogenic applications. The metalized pyrex glass rods share essentially the same expansion as the header and the alumina substrate. The only method that can be used to space qualify a design of this type is to conduct repeated thermal cycles to low temperatures at rates much higher than those that will actually be encountered. At the time of this report one unit has been subjected to 14 thermal cycles without failure. More testing is in progress.

III. C. 3. The 1 x 16 array

At present the packaging requirements for the 1 x 16 array are under study and will depend on the application. Because of the large number of connections and the need to achieve very high packing densities in large array applications, it is clear that conventional wirebonds must be replaced with bump bonds. The approach chosen to solve this problem is similar to the indium bump bonding used to mount large infrared array detectors to silicon read-out chips. Under this contract two pieces of equipment were designed and built for this purpose. A dedicated vacuum evaporator was designed, built and tested for producing indium films with a thickness in excess of 3 um. A "bump bonder" was designed and built which accurately aligns the indium coated contacts of the chip and of the substrate and then presses the contacts together. Work is in progress to produce the first indium bump bonded test devices. The objective is to mount the 1 x 16 integrator chip, along with a suitable CMOS multiplexer chip and heater resistor, on a small substrate which can be supported by either metalized pyrex structures or by other means depending on thermal requirements.

III. C. 4. The Laboratory Test System

In order to operate and test the many different cooled JFET devices, four test dewars and their associated warm electronics were designed and built at Infrared Laboratories. Early in the program it was essential to be able to vary the operating temperature smoothly and quickly while achieving good temperature stability at selected values. This capability was necessary in order to measure the temperature dependent properties of the devices under test. A special He dewar was designed with a variable temperature stage that maintains any temperature between 77 K and 4.2 K. Many similar dewars have since been built by Infrared Laboratories for other applications. The temperature of the stage is controlled by a heater, an accurate silicon diode thermometer, and a mechanically operated heat switch. This instrumentation is a valuable asset for characterizing new components as they become available. Now that the packaging of the JF-4 and JF-77 is fully developed, most of the testing is carried out using one of three dewars equipped to test multiple units during a single cool down. This increased efficiency is essential to economical production.

Figure 8 shows a block diagram of the warm electronics which were developed to operate and test the single channel devices. The test apparatus makes use of an IBM PC compatible computer and associated 12 bit A/D converter and software. The low noise analog amplifier was developed as part of this project and utilizes Burr-Brown's low noise, low frequency operational amplifier, the OP A111. The OP A111 uses the same P-channel JFET process used in the 1 x 16 integrating array. The first stage warm amplifier and the basic electronics controller / reset circuit have been packaged together in yet another new product called the RS-1. The RS-1 is sold to support users of the JF-77 and JF-4. The remaining apparatus is quite standard and readily assembled in most laboratories using infrared detectors.

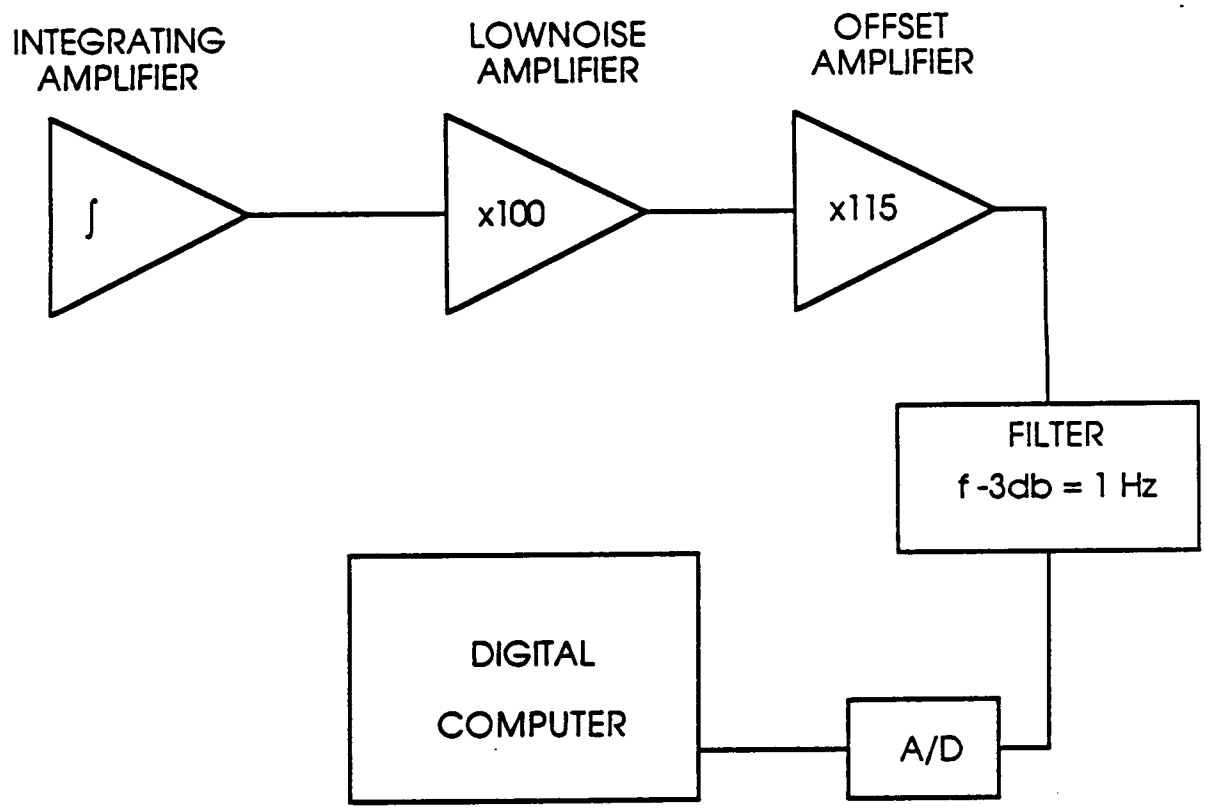

Figure 8. Block diagram of the test system

The application of the small digital computer as a data acquisition and analysis tool is central to the use of these new devices. To aide customers in the use of computers, Infrared Laboratories offers software support. The recommended mode of operation is to actuate the reset switch from a computer which then records and analyzes the data. Following a reset, the output from the low-pass, high gain dc amplifier is sampled at a rate of 4 samples/second, fast enough to avoid aliasing of the noise. These samples are displayed on a digital plotter and are recorded on floppy disk for further analysis. The accumulated charge on the gate of the cooled JFET is linearly proportional to the output voltage,

$$q = vC = (\text{output} / \text{gain}) \times C$$

where q is the charge in coulombs, v is the voltage in volts and C is the total capacitance in farads. The total capacitance is measured at the gate and includes contributions from the two transistors, the compensating capacitor, the wiring and, if present, the detector. For a single channel integrator the measured value of C is 7.5 pf. To convert a change in output voltage to a change in the charge stored on the input, the measured voltage should be multiplied by approximately 50 electrons/microvolt.

For a constant leakage current the plot of output voltage versus time is a positive or negative "ramp", depending on the sign of the leakage current. If a signal is introduced which takes the form of a constant current then the slope of the output voltage versus time will change and is proportional to the amplitude of the applied current. One method of computing the slope of the "ramp" is to fit a straight line to all of the samples taken over a specified integration time. Another way, which gives slightly better results, is to average all of the samples during the specified integration time and take successive differences as time progresses. After a number of successive integrations an accurate slope will be obtained, limited by the inherent fluctuations in the slopes. The "read noise" is defined in terms of statistical fluctuations in the slopes of many line segments of the ramp.

As an example, the algorithm used to compute the mean slope and its rms fluctuation for an integration time of one second is as follows. For each consecutive integration time there are four samples taken at precisely spaced intervals of 250 msec. Averages of the four samples are computed for each time segment of one second and successive differences are taken to give a number of independent measures of the slope which are one less than the number of seconds for which data are recorded. The current and the current noise are calculated from the mean and the standard deviation of the mean, respectively. If the total electronic gain and input capacitance are measured accurately these results give highly repeatable and accurate measures of current and read noise. The read noise is defined as the rms fluctuation of the current multiplied by the integration time. Given a sufficiently long period of continuous sampling of the ramp between resets it is possible to divide the data into various time segments corresponding to various integration times. Simple theory predicts that for an integrator with a "white" noise spectrum, the read noise will decrease as the square root of the integration time. If, however, there is 1/f noise present, as is typically the case, then the read noise may be nearly independent of integration time or even increase with integration time. The noisier devices tend to have read noise which increases with integration time and this is usually correlated with higher slopes corresponding to significantly higher leakage currents.

In order to measure the input capacitance of the JF-4 and JF-77, tests were performed using a small, 1 pf, capacitor made from metalized teflon sheet. After confirming the room temperature value, it was connected to the input pin of the device and the dewar was cooled to operating temperature. Charge can be induced on the gate through such a capacitor and it will be stored for very long periods. This test circuit consists of an almost purely capacitive voltage divider where the 1 pf capacitor is known and the input capacitance is to be measured. Independent measurements of the voltage gain are easily made using the reset switch in its "closed" condition. A typical value is 0.95. This means that input capacitance may then be calculated from the ratio of output to input signal and the value of the known capacitor.

IV. PRODUCT DESCRIPTIONS AND TEST RESULTS

This section of the report gives brief descriptions of the products that have been developed as the result of this contract or are planned for the near future.

IV. A. The JF-77

The JF-77 is a single channel integrating amplifier module designed for use with infrared detectors operating in the temperature range from 50 to 80 K. It consists of a balanced JFET integrating amplifier with a voltage gain of 0.90, an input capacitance of 7.5 pf and a read noise of less than 20 electrons. The charge compensated JFET reset switch provides for rapid and accurate reset of the input to ground potential and the device is designed for continuous non-destructive read-out by sampling the output. Output impedance is less than 100 K ohms. Power dissipation is less than 30 microwatt at a temperature of 77 K.

Table 1. Specifications for the JF-77 integrating JFET amplifier

ELECTRICAL SPECIFICATIONS		NOISE SPECIFICATIONS	
Package	Standard TO-5, 10pin	Spot Noise	< 350 nV/Hz$^{1/2}$
No. Active Leads	7		
Operating Temp	45K to 77K	Read Noise at 2 sec	< 20 e^-
Total Power	40 μW (aprox.)	32 sec	< 40 e^-
Supply Voltage	± 1.5 V	128 sec	< 50 e^-
Offset Voltage	15 mV Max		
Input Capacitance	7.5 pF		
Gate Current	< 20 e^-/sec		

IV. B. The JF-4

The JF-4 is a single channel integrating amplifier module designed for use with infrared detectors operating in the temperature range from 1 to 50 K. It consists of a balanced JFET integrating amplifier with a voltage gain of 0.90, an input capacitance of 7.5 pf and a read noise of less than 15 electrons. The charge compensated JFET reset switch provides for rapid and accurate reset of the input to ground potential and the device is designed for continuous non-destructive read-out by sampling the output. Output impedance is less than 100 K ohms. Power dissipation, including heater power, is less than 150 microwatt at a temperature of 4 K. With special modifications the total power consumption can be reduced to 60 microwatt.

Table 2. Specifications for the JF-4 integrating JFET amplifier

ELECTRICAL SPECIFICATIONS		NOISE SPECIFICATIONS	
Package	Standard TO-5, 10pin	Spot Noise	< 350 nV/Hz$^{1/2}$
No. Active Leads	8		
Operating Temp	1.2K to 45K	Read Noise at 2 sec	< 15 e$^-$
Total Power	100 μW (aprox.)	32 sec	< 20 e$^-$
Supply Voltage	± 1.5 V	128 sec	< 30 e$^-$
Offset Voltage	15 mV Max		
Input Capacitance	7.5 pF		
Gate Current	< 5 e$^-$/sec		

The test system described in section III.C.4 was used to measure the performance of a large number of preproduction and a few production units of the JF-4. The results reported below were obtained for a superior unit, serial number 109. Because of many changes that occurred during the development of the device, it is not possible to report extensive data on the full range of performance expected for these devices. This type of experience will be accumulated as the project proceeds into the normal production phase. The preliminary specifications presented in Table 2 were derived from the available test results and it is likely that yields of 50 percent or better will be experienced based on those performance limits. It is also clear that quite superior performance is now available for at least a few devices given a large enough sample from which to chose.

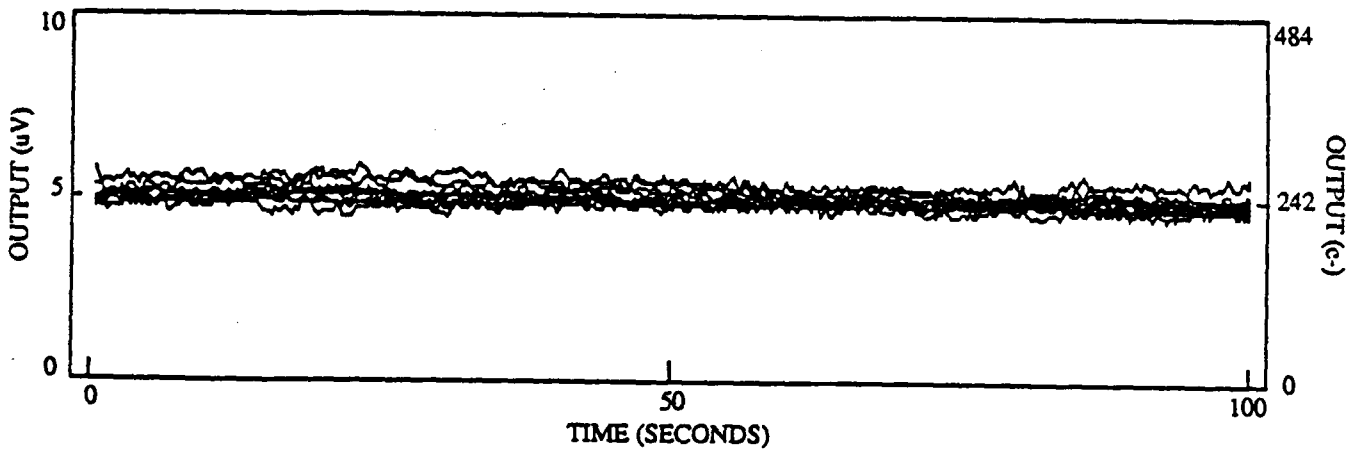

Figure 9.a. Output voltage vs time for warm electronics only (input shorted). Scale on left shows voltage refered to the input. Scale on right shows equivalent charge. Elapsed time 1024 seconds.

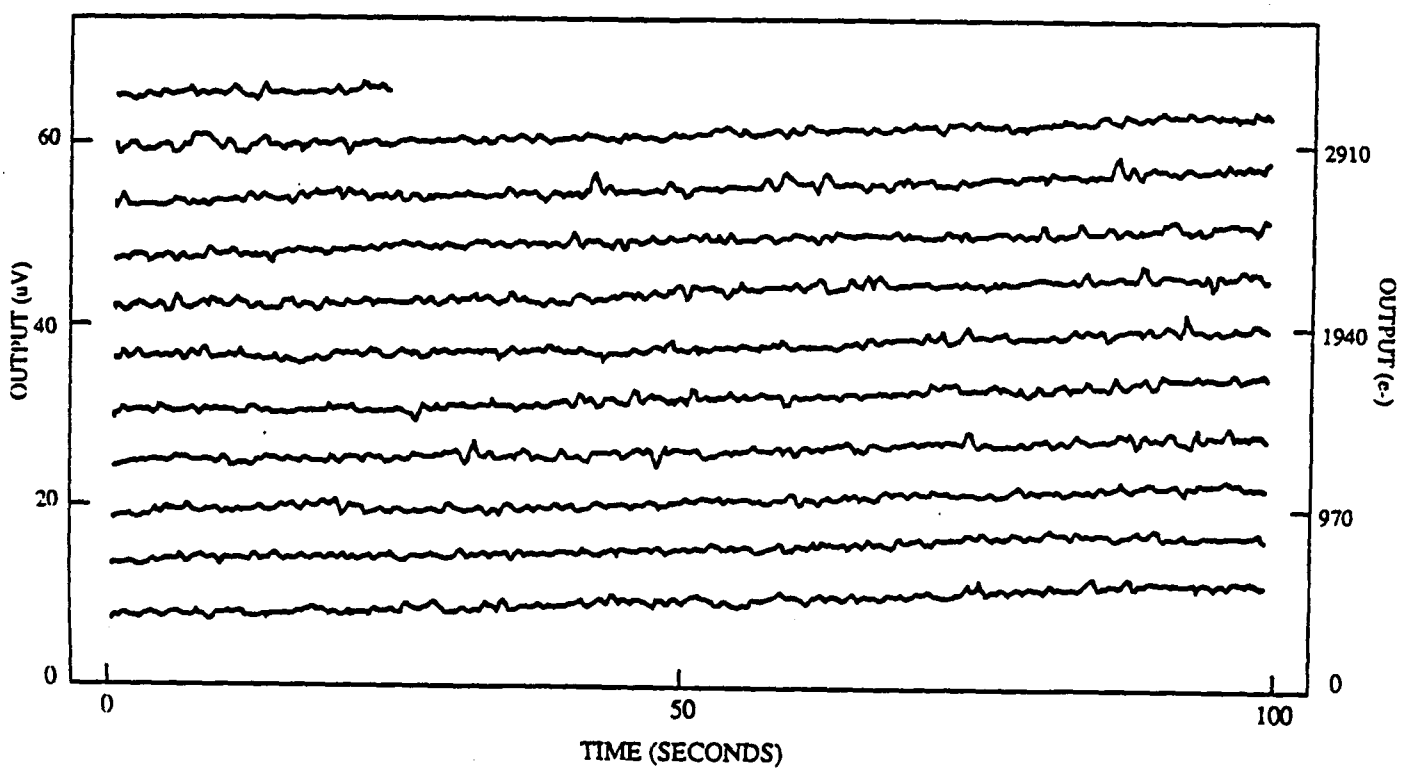

Figure 9.b. Output voltage vs time for JF-4/109. Scales and elapsed time are same as above.

Figure 9 shows an example of a computer generated plot of output voltage versus time for data taken in the standard manner for a period of 1,024 seconds. This is sufficient to permit the computation of read noise for integration times up to 128 seconds. Much longer integration times are possible but are not part of the routine test program. The operating conditions and summary of measured parameters are given in Table 3. For comparison, the output of the test system with its input shorted is included in Figure 9. This shows that for this very excellent device the noise performance of the test system is not negligible. The equivalent read noise of the test system is about 6 electrons.

Table 3. Electrical characteristics of the JF-4/109 integrating amplifier.

T (K)	I_{DS} (uA)	V_{OUT} (mV)	GAIN	INPUT CAP (pF)	DARK CRNT (e^-/s)	TOTAL POWER (uW)	SUPPLY (V)	READ NOISE (e^-)	OUTPUT IMPED (KΩ)
54	11.8	7.7	0.92	7.5	2.8	100	±1.5	15	~100

The data file used to construct the plot in Figure 9 was analyzed using the standard algorithm which produced the results listed in Table 4. The read noise listed for 128 seconds of integration is 7.5 electrons, the lowest value to be measured as part of this program. Furthermore, no correction has been made for the noise contribution of the test system. If this correction were made, assuming the two noise sources add quadratically, the resulting read noise would be only 5 electrons for integration times of 128 seconds. More work is needed to directly measure this extremely high sensitivity but it is clear that for selected single channel units the results indicate that read noise well below 10 electrons is possible.

Table 4. Read noise at different integration times for JF-4 / 109 at 54K.

Integration Time (sec)	Current Noise σ_I (e^-/s)	Read Noise σ_Q (e^-)
1	14.7	14.7
2	5.9	11.8
4	2.6	10.3
8	1.2	9.7
16	0.6	9.5
32	0.31	9.8
64	0.15	9.8
128	0.06	7.6

If the ultimate in low noise performance is required, it is necessary to optimize the operating temperature of the active devices. Figure 10 shows measurements of the read

noise as a function of temperature. Note that the heater power required to maintain the operating conditions is also included. The read noise reaches a minimum at about 55 K for the NNZ, NZF combination. It is also noteworthy that as the temperature is increased to 80 K both the leakage current and the read noise increase measurably.

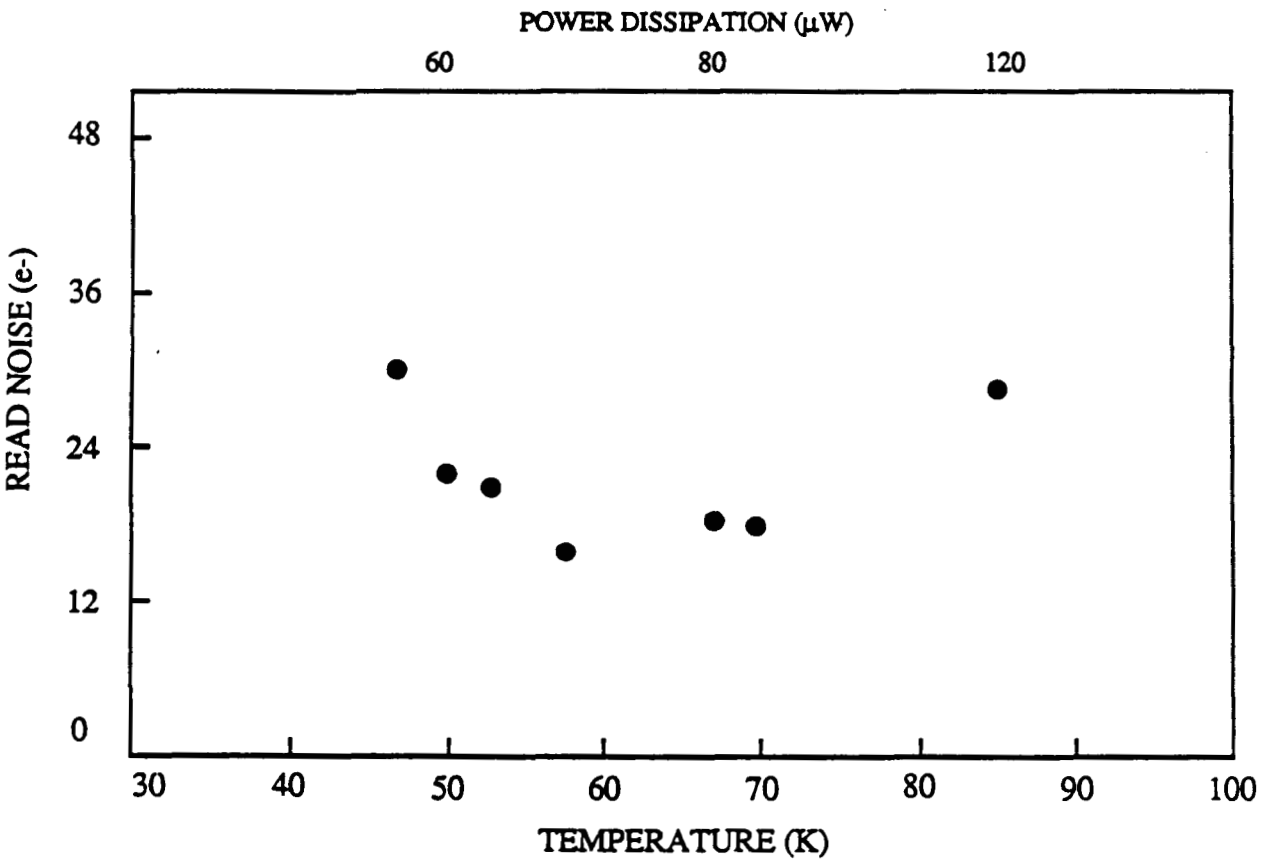

Figure 10. Read noise versus temperature of the active devices, integration time of 1 second

IV. C. The 1 x 16 JFET array

The 1 x 16 integrated circuit consists of a linear array of 16 independent JFET integrating amplifiers constructed on a single silicon chip which measures only 1mm x 3.5 mm. The five service lines, consisting of +/- supplies, ground, reset, and reset compensation, are connected to a common bus suitable for connection to additional chips of the same type thereby opening the possibility of very large arrays. The 16 input and 16 output lines are located on opposite sides of the chip for electrical isolation purposes. The output lines may be sampled by a suitable CMOS multiplexer located nearby or they may be brought out of the cold environment for signal processing at room temperature. At present only preliminary test results are available as summarized below. These data are adequate to show that the device is potentially valuable in a number of applications where arrays of infrared detectors must be read-out at very high sensitivity.

Table 5. Test data for six 1 x 16 JFET arrays. Devices were selected from two different wafers manufactured by Burr-Brown.

DEVICE #	T (K)	I_{DSS} (μA)	LEAKAGE (e^-/sec)	ΔV_O MAX (mV)	Read Noise (e^-) at Integration times (sec) of: 1	4	8	16	32	64
1-1	77	21.7	3-9	24.0	30	33	36	39	45	52
	66	9.4	<7	-	30	33	33	33	42	51
1-5	77	17.8	5-15	45.0	36	39	39	45	45	52
1-6	77	23.0	30	13.7	39	40	51	69	97	160
11-1	77	41.0	1-30	24.0	31	31	34	35	39	46
11-5	77	28.0	3-15	21.6	36	36	37	48	52	41
11-9	77	35.0	18	-	45	44	42	51	81	126

These results do not fully sample the range of wafers that have been produced. However, they do show that highly usable devices are available from this production run and that the most critical performance parameters have been successfully demonstrated. The noise is systematically higher than for the best single channel units but the same noise dependence with temperature appears to hold true. Further tests will be undertaken to explore the full range of noise performance in the complete sample of wafers that are now available.

It is quite critical to the use of these devices in large arrays that they be uniform in their essential parameters. Table 6 gives test results for many of the channels on device number 1-1. As can be seen, the performance of each individual channel corresponds closely to that of the others.

Table 6. Electrical characteristics of a typical JFET array

CHANNEL #	V_{OUT} (mV)	LEAKAGE (e^-/sec)	Read Noise (e-) at Integration times (sec) of: 1	2	4	8	16	32	64
2	32.9	13	36	37	36	37	49	50	41
3	21.5	7	36	36	39	43	45	57	63
4	20.4	9	37	42	42	40	48	45	59
5	18.3	8	37	37	42	44	44	34	34
6	19.7	3	37	39	43	52	55	72	90
7	20.1	13	42	42	42	33	42	46	67
8	13.2	11	39	42	42	46	48	51	65
9	19.2	6	39	39	44	44	42	45	36
10	34.8	11	37	20	44	45	51	41	46
11	24.5	9	39	42	42	46	57	90	142
12	30.8	10	37	39	42	46	55	52	57

Because it is not yet possible to test a complete array at temperatures below 65 K a number of special chips were used to study the characteristics of the devices at lower tem-

peratures using the dewar equipped with a variable temperature stage. These chips were included as test devices on each wafer and allow single unit cells to be isolated and studied individually. Table 7 gives test results down to 50 K, the lowest temperature tested.

Table 7. Electrical characteristics of a unit cell of the 1 x 16 integrating amplifier array at different temperatures.

T (K)	I_{DSS} (μA)	LEAKAGE (e^-/sec)	g_m (μS)	READ NOISE* (e^-)
300	100	---	150	---
77	28	15	70	30
62	5.5	9	12	17
50	1.12	2.3	---	19

*Read noise in 1 second of integration time.

V. CONCLUSIONS

It is clear from the results obtained so far that further work on the new technology developed here should yield even more dramatic performance than has been demonstrated in the present contract. It should be kept in mind, however, that the performance already achieved represents very significant progress relative to all other types of read-out technology applicable to spaceborne infrared astronomy. In summary, our main conclusions are:

1. Highly serviceable single channel integrators capable of measuring currents as low as 0.5 electrons/second have been demonstrated and are in the early stages of production.
2. The mechanism which controls the read noise is not well understood and appears to vary by as much as an order of magnitude from the best to the worst devices that have been tested. This suggests that a study of noise mechanisms in these devices might lead to a breakthrough in understanding. If such were the case, it would be possible to greatly improve the yield in terms of the lowest noise units and might lead to even lower read noises than have been found to date.
3. The first integrated circuit consisting of 16 isolated JFET integrators on a single silicon chip shows promise as a device which will be useful in the construction of very sensitive infrared arrays.
4. In order to fully utilize the integrated circuit array that has been demonstrated it may be necessary to extend the level of integration to linear arrays of larger size. It is also highly desirable to include on the integrator chip a low noise multiplexer. This would cut in half the number of separate devices needed to construct large arrays.

PART TWO: SUPERCONDUCTING MOTORS AND ACTUATORS

I. INTRODUCTION TO PART TWO

The goal of the superconducting motor effort was to develop an electro-mechanical actuator technology capable of addressing the very low power needs of future spaceborne projects. Actuators of this type are needed for the operation of a number of applications such as rotary mirrors, filter slides, and aperture changing wheels. Our research and development program has produced devices of sufficient maturity that instrument-specific actuators can be designed and fabricated rapidly. Performance evaluations of these actuators have given excellent results. Although the commercial market for these devices has been found to be quite limited, a need may be found in military or other government applications, such as cryogenically cooled infrared telescopes.

II. PROJECT SUMMARY

An initial project determination stated that a radical departure from conventional stepper motor technology was not necessary in order to develop successful superconducting stepper motors. It was felt that analysis of existing motors in the new cryogenic operating environment would isolate those areas where advancements were necessary. This approach established four topic areas that were addressed in detail over the course of the project:

A. Superconducting coil windings
B. Bearings for cryogenic use
C. Rare-earth rotors
D. Cooling of the motor

The ESCAP P310 conventional stepper motor was chosen as the unit upon which to base all developments. This unit was chosen because of its small size, the correspondingly strong holding torque of 3 oz-inches, and the availability of rare-earth magnetic rotor assemblies for this motor.

II. A. Superconducting coil windings

Initial tests were conducted on an unmodified ESCAP P310 at 300K, 77K, and 4.2K. In this configuration the motor had copper windings and a Sm:Co rotor. As expected, the power required to operate the motor at low temperatures was significantly reduced compared to the 300K values. The factory supplied copper wire coils were then removed and the motor rewound with 0.005" diameter NbTi superconducting wire to approximately the same number of turns as the original winding. This wire has a 0.002" thick copper overcoat to provide a thermal cooling path when the wire becomes superconducting. NbTi is capable of operating at the required magnetic field strengths at temperatures up to 9K. The detailed performance results for the superconducting coils are contained in Section III.

II. B. Bearings for cryogenic use

It became apparent during the first tests that bearing friction would play a major role in determining reliability. The bronze sleeve bearings with which the motor was originally equipped were not capable of operating properly at low temperatures. Teflon was chosen as an alternate bearing material and teflon sleeves were then substituted for the original bronze bearings. The results obtained with the new material were very favorable and indicated

further improvement was possible. After a thorough study of the expansion properties of the motor housing and bearing materials, a design was developed for a sleeve-type system using Rulon-J. This material is similar to teflon, but is filled with a glass component to eliminate "cold flow", a problem common with teflon. Additional advantages of this material include much longer wear characteristics and very low particulate production when used as a sleeve-type bearing.

II. C. Rare-earth rotors

In order to reduce the inertia of the rotor assembly while still providing a high magnetic field strength, the rare-earth alloy Samarium/Cobalt (Sm:Co) was chosen as the rotor material. This decision lead to some early problems since Samarium/Cobalt is inherently fragile in the thin configuration required and the Sm:Co rotor, with which the unmodified motor was equipped, violently self destructed when operated at low temperature. A modified rotor was designed and fabricated that withstood repeated thermal cycling without fracturing, and with no apparent change in magnetic properties.

II. D. Cooling of the motor

The relatively high current requirements of the motor necessitated substantial cooling capacity to provide rapid and uniform cooling of the motor. Four separate methods were simultaneously employed to achieve the desired results. The first step involved cementing all wires that lead to the motor to a liquid nitrogen cooled surface for a length of 10 cm. The leadwires providing current to the motor received additional cooling by means of a 8.5 cm long "trough" on the liquid helium cooled surface through which the wires passed and into which a thermally conductive epoxy was poured. The motor coils were cooled directly by wrapping each individual coil with copper tape that was in turn attached to the 4.2K surface. Finally the entire motor assembly was mounted inside a block of copper.

III. TEST RESULTS

The final version of the modified commercial stepper motor contained all the advancements described above. Test results for this motor are contained in this section. Figure 11 shows a cross-section of the motor. Materials are indicated to show their application for low temperature use. A photograph of the actual disassembled motor is shown in Figure 12.

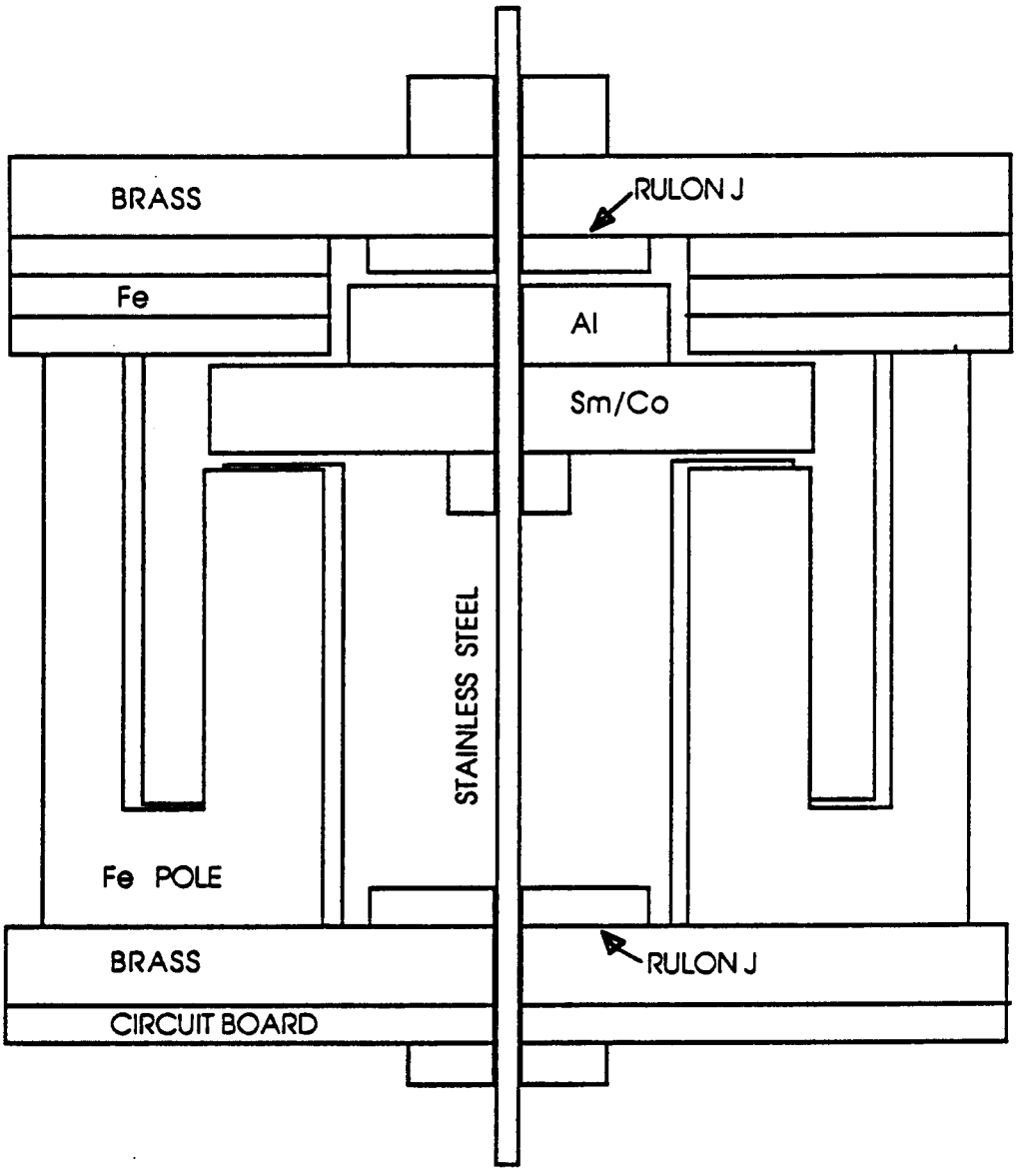

Figure 11. Motor cross-section.

Performance of the most advanced unit is shown in Figure 13, where pulse width and operating current are displayed. Table 8 utilizes these data and the coil drive circuit parameters to show the final minimum operating powers at various coil drive pulse widths. Table 8 also shows the total operating power dissipation. As can be seen, the motor power dissipation to its heat sink is very low using the superconducting configuration. About 40% of the total circuit power is dissipated in the leadwires, and the other 60% is consumed by the electronics itself. The actual torque produced by all superconducting motors constructed for this project was consistently three times the value which could be obtained in the normal-wire configuration. Section IV describes an alternative for reducing the high current/high power dissipation problem in the leadwires.

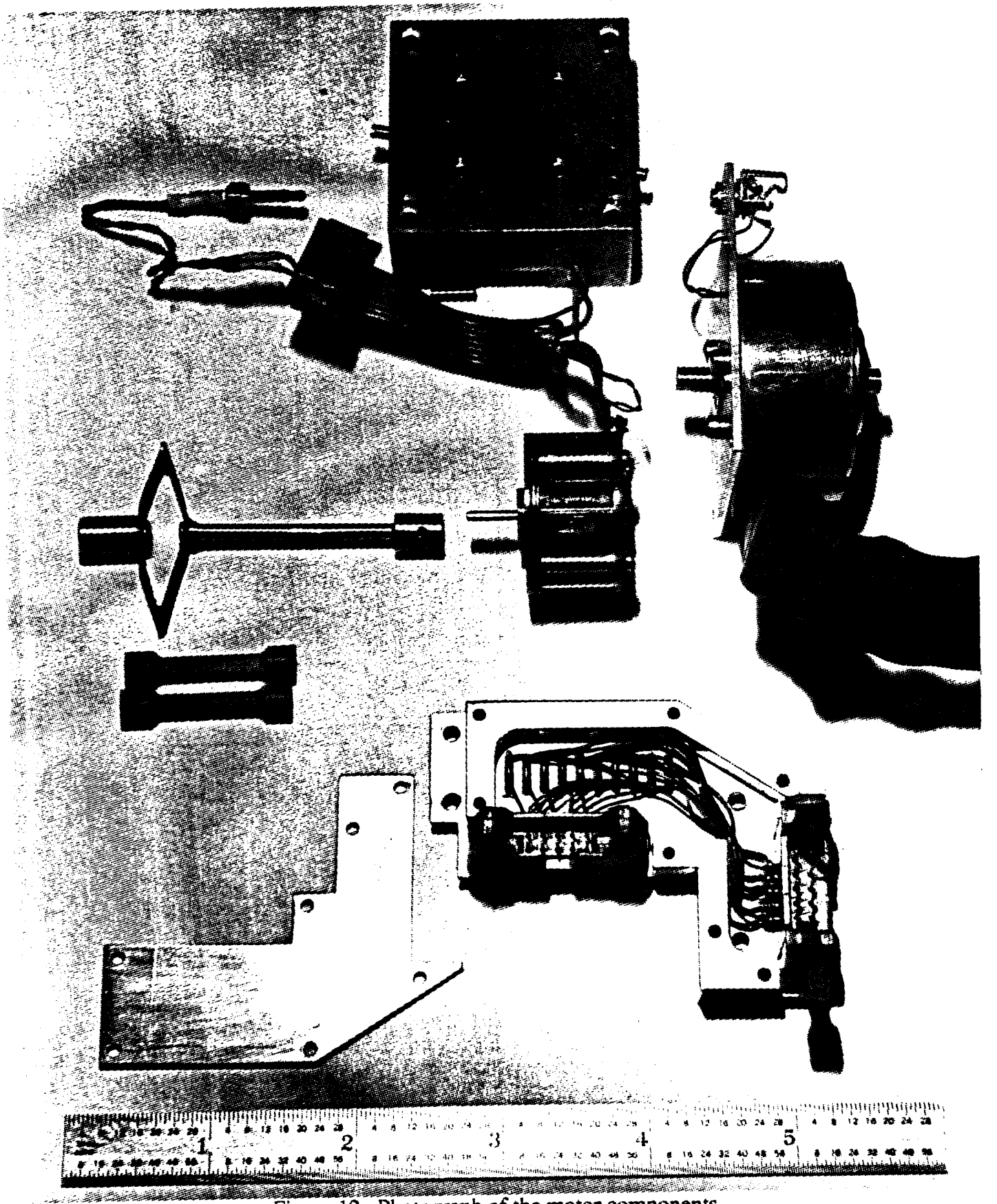

Figure 12. Photograph of the motor components.

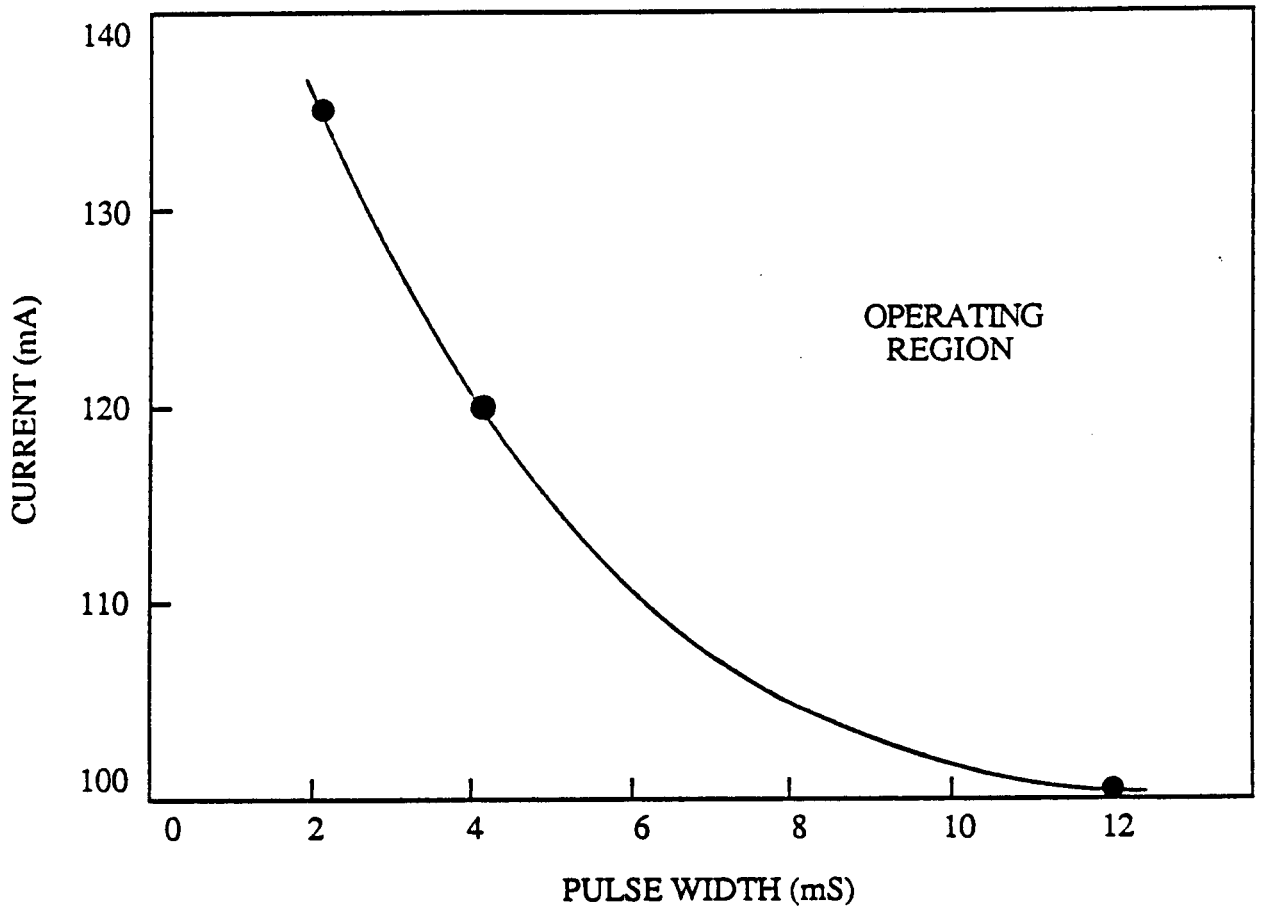

Figure 13. Operating current vs. pulse width for the most advanced motor model.

Table 8. Motor Parameters.

WINDING DRIVE PULSE WIDTH ΔT (ms)	WINDING CURRENT PEAK I (mA)	TOTAL POWER FOR ONE STEP P_c (mW)	ENERGY PER STEP E (mJ)	MOTOR POWER P_m (μW)
2	135	510	1.0	1.7
4	120	400	1.6	1.3
6	112	350	2.1	1.2
8	106	320	2.6	1.1
10	103	300	3.0	1.0
12	100	280	3.4	0.9

IV. CONCLUSIONS

It is clear from the results obtained during the course of this work that compact, low power motors can be successfully fabricated using appropriate bearing materials and superconducting wire. The relatively high power dissipation of the high-current wires leading to the motor's coils could be reduced substantially with the application of the new higher temperature superconductors if they can be fabricated into a suitable form. Since superconductors are, in general, poor thermal conductors, high currents could be carried with very low power dissipation and low thermal conductance to the motor cooling environment. An additional benefit of these higher temperature materials is operation of the superconducting motor over a wide range of operating temperatures.

At present there does not appear to be a significant market for low power cryogenic motors operated below 9K. However, it is likely that with the new era of high temperature superconductors, new application areas will be found for these devices.

PART THREE: RESET SWITCH DEVELOPMENT

I. INTRODUCTION TO PART THREE

This project began as the result of difficulties encountered in using various types of electronic switches to reset the cooled JFET integrating amplifier developed over the last several years (Low 1984). The first level requirements for the reset switch are: (1) it must quickly discharge the signal stored on the gate of the JFET integrating amplifier whenever the command for reset is given and (2) it must not degrade the performance of the JFET integrator either in the form of excess noise or in loss of signal during very long integrations. To accomplish all this requires a reset device with exceedingly high impedance when it is in the "open" state. There are other requirements which appeared difficult, if not impossible, to meet using standard types of solid state switches such as a simple MOSFET. However, it was the result of tests carried out at 77K with discrete MOS devices which showed degradation in the noise performance of the best JFET integrators that led to the exploration of alternatives.

It was realized that due to the very low leakage currents in JFET amplifiers at temperatures below 80K it might be possible to reset with a device very similar to that which serves as the amplifier itself. This led to the present proposal and, ultimately, to a highly acceptable solution of the problem. This report describes the results obtained in the testing and manufacture of both N-channel and P-channel JFET reset switches which are now used in products based on this research.

II. DESIGN GOALS

Read noise levels of less than 10 electrons are now possible with the best integrating amplifiers. Because of this the first level reuirement for the new reset switch was noise performance. Any leakage current in the reset switch not only increases the noise but may also cause a loss of accumulated charge during very long integrations. The reset action of the device is of concern since it is highly desirable that deposited charge following each reset be as low as possible and that the discharge of accumulated charge be accomplished quickly and repeatably during each reset. This places requirements on the "closed" impedance of the device and on its capacitance and drive requirements. It is assumed here that switching time is so short in all candidate solid state electronic devices that it may be considered infinitely short. These objectives were used to derive a set of design goals for a JFET reset switch.

It is particularly important that the reset JFET be of the same type as the amplifier if it is to be integrated into a solid state circuit at the time of processing. This is not necessary in the case of hybrid devices made from discrete components, as in some of our applications, however, it is a key feature in the fully integrated design of our 1 x 16 channel integrated circuit.

An important, but often overlooked, goal is to compensate the reset circuit so that when the switch opens it does not inject appreciable amounts of charge. This requirement is fully realized if the deposited charge following each reset is limited to the kTC charge arising from thermal fluctuations. In principle this is not a difficult requirement to meet and could be achieved in all simple reset circuits by the addition of a suitable capacitor driven out of phase with the reset. This is more fully explained below in Section 6. It is also important that the capacitance of the reset switch be less than that of the integrating amplifier to which it is attached since it will add to the total input capacitance and degrade the overall performance by reducing the voltage change produced by a given amount of charge deposited at the input. This is consistent with the requirement that the capacitance of the reset switch be small so that the deposited charge left behind after each reset be small enough to be easily compensated. In order to minimize the amount of charge that must be compensated it is also necessary that the voltage swing on the gate of the reset device be as small as possible.

Finally, it is clear that the temperature characteristics of the device used for reset be compatible with those of the amplifier.

In summary, the design goals are as follows:

- Extremely high "open" impedance: >> 1 E 14 ohm.
- Low capacitance: < 2 pf.
- Reasonably low "closed" impedance: < 1 E 5 ohm.
- Low pinch-off voltage: < 1.5 volt.
- Compatible processing requirements.
- Compatible temperature range of operation.

III. THE SILICONIX JFET SWITCHES

Since we had developed a close working relationship with Siliconix during our effort to improve the performance of their JFET amplifiers used as low temperature integrators, we first investigated their standard production devices to see if our requirements could be met without costly development of new devices. It was soon learned that their NZF type N-channel amplifier came closest to meeting our needs for low pinch-off voltage and low capacitance. Low temperature testing demonstrated that the device did not freeze out above 30K. Additional testing in the 30K to 77K range satisfactorily showed that basic switching and noise requirements were met. Table 1 summarizes the properties of the NZF relevant to its use as a reset switch. The NZF was chosen from the list of readily available devices as the most suitable switching transistor for use with the NNZ type of N-channel amplifier.

TABLE 1. The NZF reset switch parameters at 77K.

Pinch-off voltage	$\simeq 1.0 \pm 0.2$ V
Gate-to-Drain capacitance	= 1.5 pF
R_{on}	$\simeq 100$ kΩ
R_{off}	$> 10^{14}$ Ω

Because the NZF has a higher capacitance than some other types of JFET amplifiers, especially those with smaller geometries, it was decided to investigate a device that was physically smaller. Siliconix suggested their NT amplifier as a good candidate since it was the smallest unit that they manufactured. However, NT performance was disappointing and testing was discontinued.

IV. A RESET ANOMALY

All devices that were tested showed an unexpected type of anomalous behavior which had to be understood and circumvented. This effect arises when the reset switch is left "closed" for extended periods of time. It takes the form of a small transient current which flows onto the gate immediately after the switch is "opened". This current dies out completely after a few minutes and its amplitude depends on the length of time the switch has been in the "closed" state. Figure 1 depicts the phenomenon and shows, for comparison, a normal situation when the switch is closed only briefly.

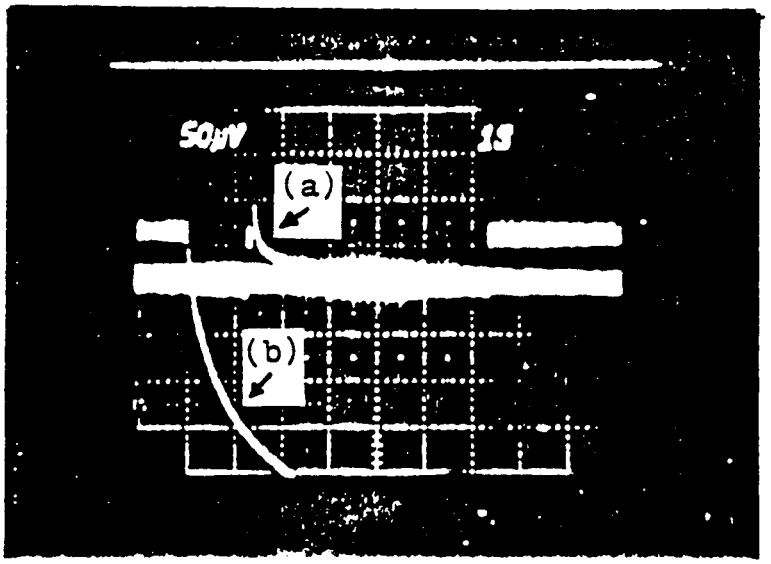

Figure 1. Anomalous behavior of the reset JFET:
a) The reset switch is left "closed" for 0.1 sec.
b) The reset switch is left "closed" for 1.0 sec.

A number of tests were carried out to characterize this strange phenomenon. It was found that among the many NZF devices that were tested, the size of the effect is quite variable from one unit to the next but that some effect is found in all devices. Other transistor types may have even larger anomalies of this same type. Fortunately, the solution to this problem is one that is simple and entirely satisfactory. The transient current is circumvented by minimizing the length of time that the switch is left in the "closed" position. Closing the switch for only a few milliseconds satisfactorily resets the amplifier while not allowing sufficient time for the anomaly to manifest itself. The problem is completely eliminated by this method. In those cases where it is desirable to leave the reset turned "on" for extended periods it is necessary to wait about one minute after the switch is "opened" for this anomalous current to decay. In these special cases, which are only associated with testing, a faster alternative is to apply a "fast" reset just after the switch is opened.

Since our solution is so easily implemented by means of external circuitry we have not attempted to find a more basic solution at the device level. The physics of this effect is not known but it may be related to anomalous dark currents in extrinsic silicon photoconductors (Young et al 1986).

V. THE BURR-BROWN RESET DEVICE

Our successful experience with the Siliconix devices led us to undertake the design of an integrated circuit which would incorporate the reset switch and integrating amplifier in a single unit cell which could be easily replicated to form a linear array of integrators. The proprietary process used by the Burr-Brown Corp. to manufacture their low noise P-channel amplifiers was chosen for this development. A complete unit cell was built and evaluated during the testing of discrete Burr-Brown samples. Experience with this unit showed that their devices performed satisfactorily as reset switches. No problems were encountered, although, we were interested to learn that the anomalous current described above were also present in all of the Burr-Brown units that were tested. An advantage for this type of device is that its geometry is smaller than that of the equivalent Siliconix devices resulting in smaller capacitances. Also, it was shown in the final integrated circuits that were built and tested that quite low pinch-off voltages are realized by the Burr-Brown process.

VI. RESET CHARGE COMPENSATION

As expected from earlier experience, when the reset switch "opens" there is a deposited charge much larger than the minimum calculated from kTC. This charge is highly repeatable and can be compensated by capacitively injecting an equal but opposite charge. This is accomplished by adding a small capacitor, about 0.5 pf, to the gate node and driving it with a precisely controlled waveform of polarity opposite to that used to operate the switch. Tests on single channel circuits made from discrete components showed this solution to be capable fo compensation down to the kTC level. This is illustrated in Figure 2.

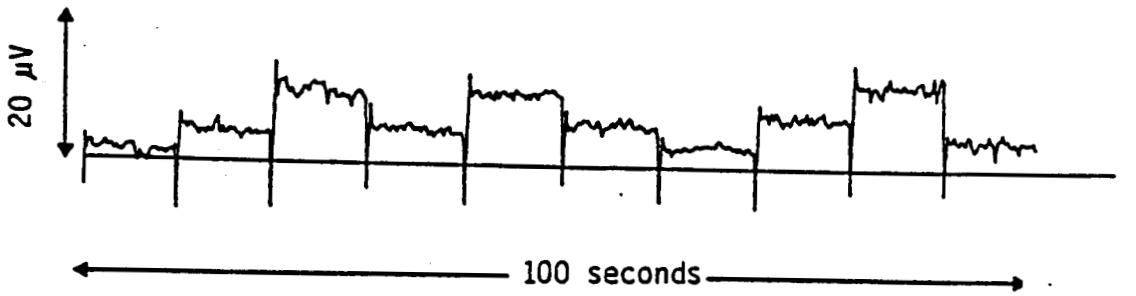

Figure 2. The output of the integrating amplifier after ten consecutive resets. After each reset the output is within 20 uV of the grounded gate level.

This means that this type of integrator will always begin its integration from a nearly zero state of charge. For some applications this is highly desirable. The small increase of capacitance was not seen as a significant price to pay for the improved performance. Thus, this feature was added to all of our production devices including the 1 x 16 integrated circuit.

VII. THE STANDARD CIRCUIT

Figure 3 shows the standard circuit used for the single channel production units, JF-77 AND JF-4. The unit cell in the 1 x 16 array is identical except for certain circuit values.

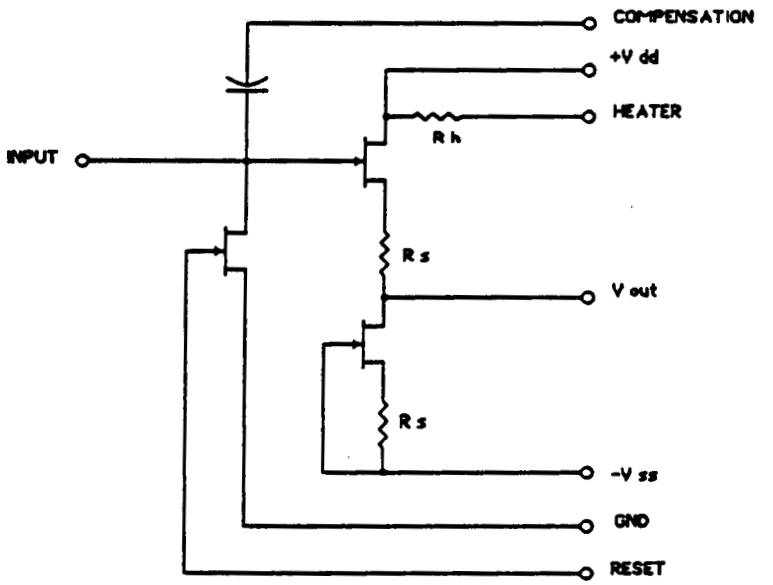

Figure 3. Circuit diagram of the JF-4 and the JF-77integrating amplifiers. The heater resistor R_H is not used in the JF-77 model.

VIII. THE WARM CIRCUITRY

Figure 4 shows the two versions of the warm control circuitry used to operate the JFET reset switches. As can be seen both the N and P-channel devices are operated from nearly identical circuits. The critical design feature of these two circuits is the use of batteries to provide extremely stable reference voltages. Special care must be given to the voltage that is used to drive the reset transistor itself since any fluctuation will be coupled directly onto the integrator through the capacitance of the JFET. Also note that the reset pulse is determined quite precisely from a stable source and that the compensation waveform is an inverted replica of the reset pulse. When the integration is taking place the compensation line is returned to ground, thus eliminating any source of noise or drift. As a convenience, a manual as well as an electrical mode of operation is provided and an optical isolator is used to eliminate noise from external control equipment such as computers.

The procedure used to adjust the compensation line is as follows: slowly vary the 50 kΩ potentiometer in increments as the output voltage from the integrator is monitored and as the reset switch is activated. The potentiometer is set to the value which results in the desired voltage level at the output. Once this initial adjustment is made no further changes are necessary unless circuit values are altered. Typical values for R_1 and R_2 are 10 kΩ and 20 kΩ, respectively.

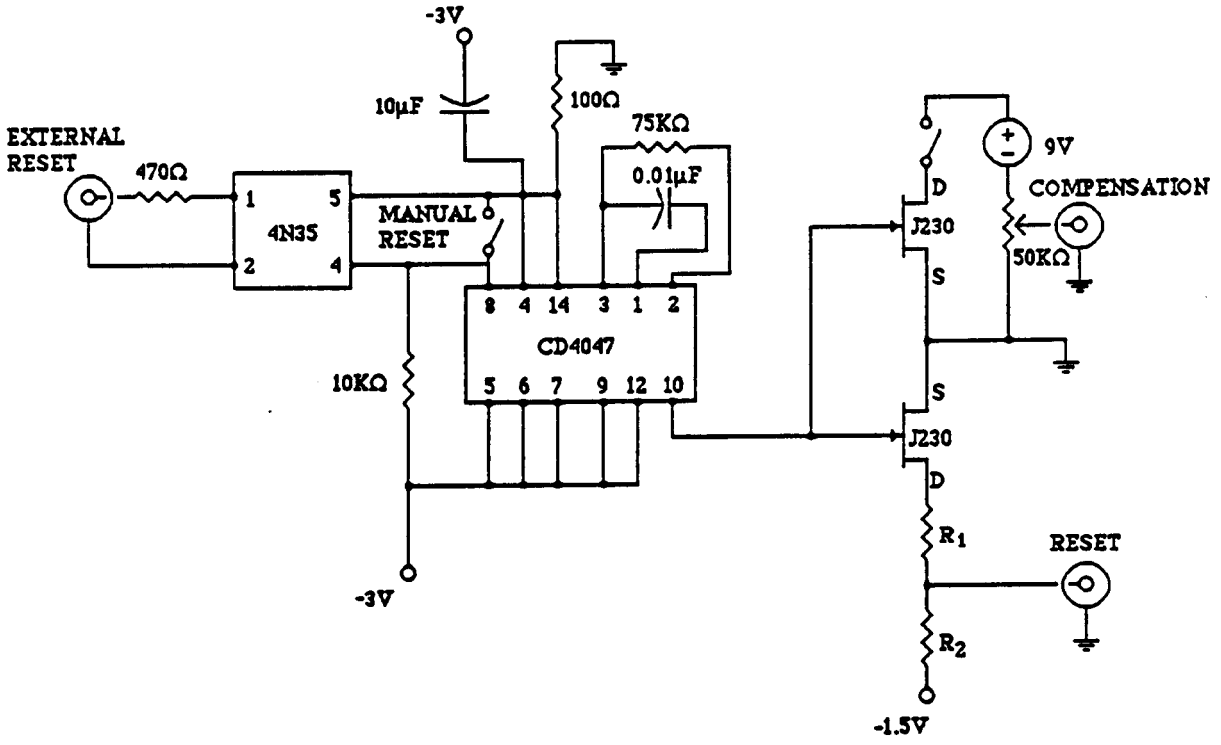

Figure 4.a. N-Channel reset controller for the JF-4 and the JF-77 integrating amplifiers. R_1 and R_2 are chosen to minimize the reset signal swing.

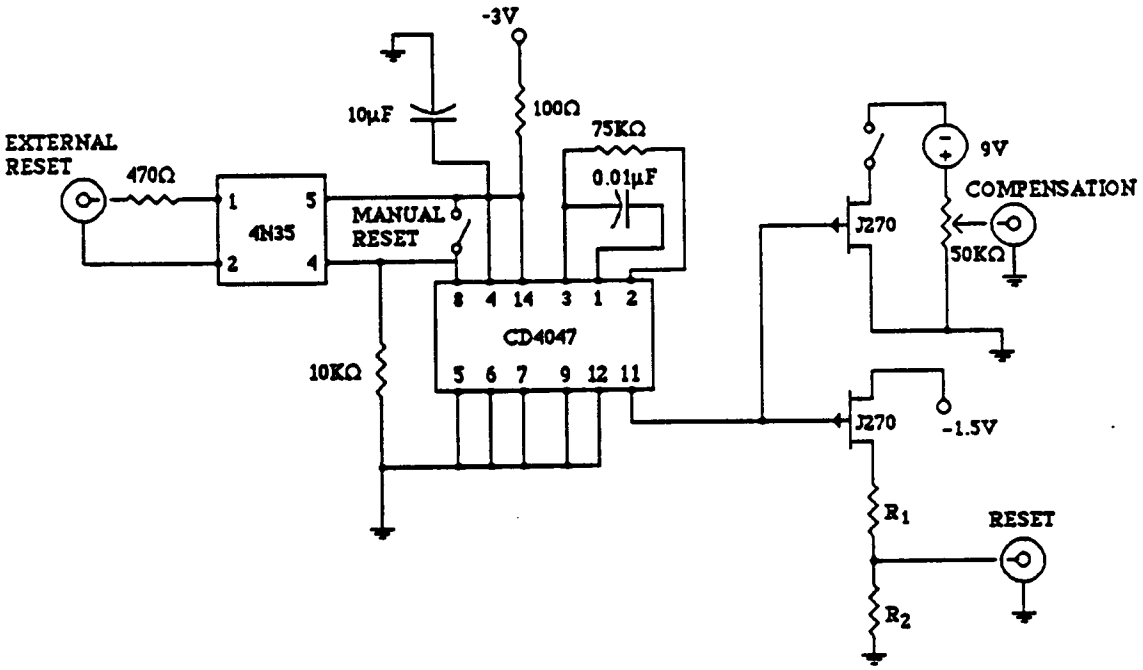

Figure 4.b. P-Channel controller for the Burr-Brown one by sixteen integrating amplifier array.

IX. CONCLUSION

Present JFET technology has been shown to be adequate for current applications. These applications include both discrete hybrid devices and integrated linear arrays. Further research may be necessary if breakthroughs in read noise occur in the future.

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16. Abstract

Basic improvements in the technology of low-noise readout systems for low-background infrared detectors have been demonstrated. Using discrete junction field-effect transistor (JFET) integrating amplifiers at their optimum temperature of 55 K, read noise less than 7.5 electrons (in 128 s of integration) has been obtained. Two versions of the integrating amplifier have been developed: one for use between 50 and 80 K, and the other for use at 4 K. A JFET reset switch has also been developed for these amplifiers. A 1 x 16 linear array of complete integrators has been developed on a single integrated circuit. These devices offer the possibility of building large, extremely sensitive arrays of low-background detectors.

A superconducting stepper motor has also been developed. The motor shows a three-fold increase in torque over conventional motors operating at room temperature. The success of the motor arises from the use of superconducting coils, bearings tailored for cryogenic use, rare-earth rotors, and improved cooling techniques. The current state of technology will allow the timely development of motors optimized for specific applications.

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