CR-182118

ADVANCED DEVELOPMENT OF DOUBLE-INJECTION, DEEP-IMPURITY SEMICONDUCTOR SWITCHES

M. H. Hanes
Semiconductor Processing Technology

Final Technical Report for the period
June 13, 1985 to December 15, 1987

Contract No. NAS 3-24637

NASA-Lewis Research Center
Space Systems Technology Office
21000 Brookpark Road
MS 301-3
Cleveland, Ohio 44135

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Westinghouse R&D Center
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NASA National Aeronautics and Space Administration

Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR 182118		

4. Title and Subtitle	
Advanced Development of Double-Injection, Deep-Impurity Semiconductor Switches	5. Report Date: 12-7-87
	6. Performing Organization Code: 87-9F0-DISQR-R1
7. Author(s): M. Hanes	8. Performing Organization Report No.
	10. Work Unit No. 506-41-41
9. Performing Organization Name and Address: Westinghouse R&D Center, 1310 Beulah Road, Pittsburgh, PA 15235	11. Contract or Grant No. NAS 3-24637
	13. Type of Report and Period Covered: Final Report 6/13/85 - 12/15/87
12. Sponsoring Agency Name and Address: NASA-Lewis Research Center, Space Systems Technology Office, 2100 Brookpark Rd., MS 301-3, Cleveland, OH 44135	14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

Deep-impurity, double-injection devices, commonly referred to as $(DI)^2$ devices, represent a unique class of semiconductor switches possessing a very high degree of tolerance to electron and neutron irradiation and to elevated temperature operation. These properties have caused them to be considered as attractive candidates for space power applications. This report describes the design, fabrication, and testing of several varieties of $(DI)^2$ devices intended for power switching. All of these designs were based upon gold-doped silicon material. Test results, along with results of computer simulations of device operation, other calculations based upon the assumed mode of operation of $(DI)^2$ devices, and empirical information regarding power semiconductor device operation and limitations, have led to the conclusion that these devices are not well suited to high-power applications. When operated in power circuitry configurations, they exhibit high-power losses in both the off-state and on-state modes. These losses are caused by phenomena inherent to the physics and material of the devices and cannot be much reduced by device design optimizations. $(DI)^2$ technology may, however, find application in low-power functions such as sensing, logic, and memory, when tolerance to radiation and temperature are desirable -- especially if device performance is improved by incorporation of deep-level impurities other than gold.

17. Key Words (Suggested by Author(s))		18. Distribution Statement
SILICON	SWITCHES	Publicly Available
GOLD	SEMICONDUCTORS	
DEEP IMPURITIES	RADIATION	
DOUBLE INJECTION		
POWER		

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No of pages	22. Price*
		119	

NASA FORM 1626 OCT 86

*For sale by the National Technical Information Service, Springfield, Virginia 22161

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1. SUMMARY

Deep-impurity, double-injection, $(DI)^2$ devices represent a unique class of semiconductor devices in which deep-level impurities are intentionally incorporated into the device material in order to obtain unusual properties and functions. It has been shown theoretically and experimentally that semiconductors containing large concentrations of deep levels are capable of switching from a low conductance state to a high conductance state when a certain potential, called the threshold voltage, is exceeded.

Other studies have shown that $(DI)^2$ devices possess very high immunity to the effects of electron and neutron irradiation, and that they may have the ability to function normally at elevated temperature. The best studied method for obtaining desirable deep-impurity properties is the incorporation of gold into silicon, and it was this method that was employed in these studies. This program has investigated $(DI)^2$ devices for possible applications in power switching, especially in space environments, where light weight, reliability, and radiation hardness are desirable attributes.

This program has built upon the foundations laid by previous Westinghouse programs and by fundamental work performed at the University of Cincinnati by Dr. Thurman Henderson and his students.

During this program, several varieties of $(DI)^2$ devices were investigated, devices were fabricated and tested, and the parameters of device performance were calculated. The processing of $(DI)^2$ devices, in particular the method of introducing gold into silicon, was studied and improved.

Calculations based upon the assumed mode of operation of $(DI)^2$ devices, along with empirical information regarding power semiconductor devices' operation and limitations, have led to the conclusion that

$(DI)^2$ devices are not well suited to high-power applications; the very phenomenon that is essential to the operation of $(DI)^2$ devices, space-charge-limited current injection, was shown to cause high off-state power dissipations which cannot easily be ameliorated.

2. INTRODUCTION

2.1 NASA REQUIREMENTS

Requirements for space station power systems are unique and stringent. In this environment, efficiency, reliability, and survivability are paramount. Weight, of course, is at a premium, and reliability is essential. In addition, all systems aboard space craft are subject to hostile environments, some natural and some man-made. In particular, for an SP100 powered station, it would be very useful to have the power electronics components in the vicinity of the nuclear power reactor. In this situation, they could be subject to high levels of radiation and to high temperature. Temperature is a particularly severe problem in space, since the only way to dispose of heat is through radiation.

Recent new proposals for space systems have arisen from the Civilian Space Technology Initiative and from Pathfinder. These include a return to the moon with the possible establishment of a permanent station there and a one to one and one-half year manned trip to Mars with 10-12 people. These programs will require electrical power systems of several MW characterized by light weight, radiation hardness, and tolerance to high temperature.

$(DI)^2$ devices, in addition to their tolerance for radiation and high temperatures, possess other potential advantages for space power systems. One of these is that they do not rely upon reverse biased p-n junctions for their operation. In principle, this implies that they are not constrained by the high field and temperature effects that limit p-n junction devices and therefore can be designed to operate at higher voltages, a distinct advantage in efficiency. Because the radiative cooling that must be used in space power systems rapidly becomes more efficient as the temperature is increased, the use of devices that operate at high temperature possesses distinct advantages.

2.2 PROGRAM OBJECTIVES

In anticipation of the benefits to be gained by the practical application of $(DI)^2$ devices in high-power circuitry, the following objectives were conceived for this program.

2.2.1 Overall Goals

The original overall goal of the program was to perform applied research and development studies of $(DI)^2$ doped silicon devices that operate in the 2-10 kV range. This goal was later extended downward to include the 500 V range and the possibility of forming "zero forward voltage drop" rectifiers. These studies were to include theoretical, analytical, and experimental investigations of processing, electrode topologies, and gating design. The program includes the fabrication of a set of experimental devices and evaluation testing of the experimental units. Delivery of deep-impurity switching devices meeting specification goals and documentation in a final report are to constitute demonstration of the technology.

The detailed goals of the programs have been:

<u>Analysis and $(DI)^2$ Switch Design</u>

Perform theoretical, analytical, and experimental investigations to identify and demonstrate $(DI)^2$ switch designs, specific device topologies and structures, optimum configurations, and methods for control of surface fields and breakdown. The switches shall meet, in so far as possible, the characteristics enumerated in "Specification Goals for $(DI)^2$ Silicon Switches" (hereafter referred to as Spec-goals).

Design, fabricate, and evaluate mask sets that provide the required electrode topology and device structure to attain specified current/voltage ratings and switching functions. Devise and study various cathode, anode, and gate geometries that are compatible with circular planar, vertical, or other possible structures.

Study optimum configurations and electrode geometries, compatible with optimum processes, to maximize threshold voltage (V_{th}) and minimize holding voltage (V_h). Determine feasibility, parameters, and design configurations to fabricate vertical devices at near the maximum voltage rating.

Study optimum configurations and electrode geometries compatible with developed processes, to maximize the threshold voltage to holding voltage ratio and to minimize leakage current at the threshold voltage. Determine feasibility, parameters, and design considerations to fabricate devices meeting the Spec-goals.

Study trade-offs of channel-doping levels, deep-impurity types, and electrode configurations to reduce current leakage in the pre-breakdown square law region. Explore methods to minimize power dissipation.

Study gate types and configurations with threshold voltage, holding voltage ratios, current rating, and gate power to determine feasibility for "zero forward voltage drop" devices.

Study and determine the feasibility of a 10 kV device. Perform required parametric trade-offs, propose a design with projected operating characteristics, and compare them to the Spec-goals.

Formulate $(DI)^2$ switch design trade-off options in terms of the required Spec-goals. These options to be submitted in written form and subsequently presented orally at NASA-Lewis Research Center. The NASA project manager shall review the design options and select one or more designs for sample $(DI)^2$ switches.

Study and design suitable packages that provide electrical contacts, thermal interfaces, environmental protection, and mechanical interfaces. These are to be included as part of the design trade-offs options submitted to NASA-Lewis.

Processing Investigations

Investigate and determine the necessary steps and techniques for the processing of shallow impurity compensated deep-impurity silicon switching devices to meet the Spec-goals. The investigations shall specifically be concerned with the quality and yield of the bulk material, base resistivity, surface preparations, ohmic contacts, insulation, and metallization.

$(DI)^2$ Switch Fabrication

Fabricate 100 sample $(DI)^2$ switches that meet the Spec-goals and conform to the NASA-Lewis approved designs as final deliverable items to NASA-LeRC. The specific device characteristics shall be made available to the NASA Project Manager for selections of the deliverable $(DI)^2$ switches. At the discretion of the NASA Program Manager, the sample switches may be required on a minimum of four uncut wafers with up to 64 units per wafer.

$(DI)^2$ Switch Testing and Evaluation

Devise a test plan delineating test equipment, specific tests, and evaluation procedures for the verification of $(DI)^2$ switches that meet the Spec-goals. The test plan is to provide for the determination of ratings and electrical parameter characterizations for each deliverable $(DI)^2$ switch. I-V characteristics are to be evaluated with emphasis on V_{th}, V_h, leakage currents at V_{th}, holding current, gate currents at switching, and switching times. The test plan is to be submitted to the NASA Program Manager for review and approval prior to testing and evaluation of deliverable $(DI)^2$ switches. Test and evaluate all deliverable $(DI)^2$ switches according to the approved Test Plan. Test data on each switch to be submitted at the time of delivery of the $(DI)^2$ switches.

Reporting Requirements

Prepare and submit technical narrative and financial reports on NASA Form 533P. Prepare and submit a Final Report.

2.3 SPEC-GOALS

Representative Spec-goals that have been addressed during this program are outlined on Table 1.

TABLE 1

REPRESENTATIVE SPECIFICATION GOALS FOR $(DI)^2$ SWITCHES

SYMBOL	CHARACTERISTICS WITH TEST CONDITION	VALUE	UNITS
V_{th}	Threshold Voltage	2000 min	Volts
	@Ianode = 50 mA, Igate = 0	10,000 max	
	@Ianode = 50 mA, Igate = 0	500 max	
V_h	Holding Voltage		
	@Ianode = Rated Value		
	Igate = 0	10	Volts
	Igate = TBD	1	
	@Ianode = I_a, Igate = 0	15	Volts
I_a	Conduction Current		
	@2000 V	5	Amperes
	@10,000 V	1	Amperes
	@500 V	10	Amperes
t_{sw}	Switching times	10	microsec
		50	microsec
P_t	Power Dissipation @T = 75C	50	watts
		100	watts

2.4 POWER SEMICONDUCTOR DEVICES

Westinghouse has an interest in the results of this program because of our experience in the design, manufacture, sale, and application of high-power semiconductors. Since most of the applications of high-power semiconductors are unfamiliar to all but electrical power engineers, Table 2 lists some of them (in no particular order), and they are discussed in some detail below.

TABLE 2

SOME INDUSTRIAL APPLICATIONS OF POWER SEMICONDUCTORS

Solar Energy Farms
High-Voltage Direct Current
Large Motor Controls
Transportation Engines
Phase Control (VAR Generators)
Small Motor Controls
Fusion Power Generation

Solar electric power-generating plants consist of an enormous number of individual solar cells generating power at a peak value of about 15 mW per square centimeter of cell area. These cells can be wired in series and parallel to produce several MW of dc power. In order for this power to be connected into the electrical power grid which covers the 48 states and much of Canada, it must be converted to 60 Hz, high voltage ac by means of power semiconductor switches and transformers.[a]

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a. The solar farm at Carissa Plains, CA, the largest in the U. S., covers 160 acres, generates 6.5 MW of peak power (eventually to be 16 MW), and uses nine 750 kVA inverters to convert solar cell-generated dc to ac. The voltage is raised in two stages to 115,000 V for connection to the power grid.

High-voltage, direct current (HVDC) power transmission is the most efficient means for transporting power over long distances. In this application, high-power semiconductor switches and rectifiers are used at the power-generating point to convert ac to mega-volt dc levels for transmission. At the load end of the transmission line, the dc is chopped by other switches in order to produce 60 Hz ac.

Large motors such as those used in steel mills, pumps, and mining operations may operate on more than 5,000 V (15,000 V would be preferred). Their speed is controlled by semiconductor switches. Transportation motors (electric railways) are a subset of large motors. In this country, they operate at about 600 V, but more efficient installations in Europe and Japan operate near 1,500 V.

Phase control of power at electric substations is used to deliver power efficiently to varying reactive loads. In this application, static VAR generators consisting of large banks of power semiconductor devices switch capacitor banks into and out of the power circuit at 60 Hz in order to compensate for the reactance of the load and maintain a constant voltage level.

Even small motors (less then 100 hp) such as those that run industrial pumps and blowers use power semiconductors to regulate motor speed and provide efficient operation.

Finally, the equipment to be used in fusion power generation will require large amounts of electrical input power to provide high magnetic fields, to resistively heat gas plasmas, and to energize lasers. Power semiconductor switches will be used to provide pulsed power in the giga-watt range.

The list in Table 2 above does not include applications in the high-voltage, low-power regime. This includes the use of electron and ion beams such as those used in oscilloscopes, travelling wave tubes, electron microscopes, and television sets; gas plasmas such as vapor lamps and plasma displays; or static electricity applications such as Kerr cells and copying machines. This partial list indicates that the range of applications for high-voltage semiconductor switches is enormous — from millions of amperes to nano-amperes.

Obviously, there are high-power semiconductor switches available today. The state of the art might be described in terms of a thyristor which is available for sale (on special order) by Powerex, Inc. Some of its specifications are listed in Table 3 below.

TABLE 3

POWER THYRISTOR SPECIFICATIONS

SYMBOL	CHARACTERISTICS AND CONDITIONS	VALUE	UNITS
V_{DRM}	Repetitive Peak Blocking Voltage	4,400	Volts
V_{RRM}	Repetitive Reverse Blocking Voltage	4,400	Volts
	RMS Forward Current 1/2 Cycle Surge Current	2,200 25,000	Amperes Amperes
V_{TM}	Forward drop at I_T = 3,000 A	2.50	Volts
I_{GT}	Gate Current to Trigger	150	mA
T_J	Operating Junction Temperature	-40 to +125 °C	
	Thermal Resistance to Case (Double-Sided Cooling)	.015 0.53	°C/W °C cm^2/W

This thyristor can block 4,400 V in the forward or reverse direction with a leakage current of less than 250 mA. In the conducting state, it will safely pass an average current of 1,400 A at a voltage drop of less than 2.5 V. It is triggered on by a gate pulse of only 150 mA. During operation in the OFF state, power loss in the thyristor could be as high as 1.1 kW; and power loss in the ON state is 3.5 kW. But this single device is capable of regulating up to 6.16 MW of power into a load. This power level is nearly the entire peak power output of the Carissa Plains solar farm, enough power to supply 8,800 homes. The power-handling capability of this single device is impressive, and it turns on in only eight microseconds (its turn-off time is 400 microseconds). The specifications of maximum p-n junction temperature and the thermal impedance between the junction and the case are also important, as will be shown later.

This device is sealed into a ceramic package which is about four inches in diameter and one and one-half inches high. The package weighs over two pounds. In order to maximize the conduction of heat from the device, it is clamped between solid copper heat sinks which are water cooled; the mounting force is 10,000 pounds. The silicon disk itself is nearly one millimeter thick, 67 mm in diameter, and has a base resistivity of 220 ohm-cm. (A 6 kV thyristor now being developed uses a silicon disk about 1.3 mm thick and five inches in diameter; its base resistivity is 400 ohm-cm.)

Now we compare this thyristor to what might be considered an ideal high-power switch. The characteristics of this ideal switch are listed in Table 4.

This ideal switch would be compact in volume, rugged, with low loss in both the ON and OFF states, capable of high-temperature operation, and fast switching; our thyristor fills these requirements fairly well. The ideal switch is easily triggered, and our thyristor looks good here too, except that there is no inherent high-voltage isolation between the gate signal and the high voltage level. The ideal switch has dV/dt, dI/dt and Q_{rr} parameters which are adequate for the switching speeds likely to be encountered; our thyristor is suitable for operation at frequencies less than one kHz. The ideal switch is bilateral, conducting current in either direction, and has gate turn-off capability; this particular thyristor has neither of these features. The ideal switch is simple to manufacture and so can be sold at a low price; our thyristor is difficult to manufacture to these specifications and it sells for a premium price.

TABLE 4

IDEAL SWITCH CHARACTERISTICS

COMPACT
EASILY TRIGGERED (HIGH-VOLTAGE ISOLATION)
BILATERAL
GATE TURN-OFF
LOW LOSS
FAST SWITCHING
LOW COST
SIMPLE MANUFACTURE
RUGGED
dV/dt, dI/dt, Q_{rr}
HIGH VOLTAGE

Finally, the ideal power switch has high-voltage capability. This is a very important attribute of the switch. In high-power switching applications, it is almost always preferable to switch a high-voltage to the load, rather than to switch a large current. But attaining high-voltage capability by placing devices in series requires that nearly every parameter of every device in the series string be carefully matched to every other device in the string. This is necessary in order to ensure that voltage and current transients will be shared equally and simultaneously among the devices. If they are not, a cascade of burned out devices may result. Even when the devices are carefully matched, high-power cushioning or snubber circuits must be used in parallel with each device in order to protect it during the switching process.

In principle, it should be possible to increase the voltage capability of a thyristor such as ours to arbitrarily high values simply by making the silicon disk thicker and of higher resistivity material. But if we simultaneously require high current capability, the thermal consequences must be considered. During normal operation, the 4,400 V thyristor conducts a peak current of 3,111 A, resulting in an instantaneous power dissipation of 7.7 kW and an instantaneous temperature rise of 116°C. The intrinsic electron concentration n_i equals the donor concentration at 152°C. Near this temperature, thermal runaway will occur.

For the 6 kV thyristor now being developed, the silicon wafer is thicker so the forward voltage drop is higher (for the same current density) and the thermal impedance is higher, so the temperature rise is worse — and the base resistivity of 400 ohm-cm means that n_i will equal the donor concentration at 138°C.

Clearly, a high-power thyristor of this type cannot be designed for arbitrarily high voltage; basic considerations of physics become limiting factors. These considerations are in addition to technological difficulties which are difficult to solve — difficulties in obtaining high-resistivity silicon of sufficient uniformity, and difficulties in preventing the high electric fields at the device edges from destroying the device through surface breakdown.

Clearly there is room for power semiconductor devices which are sufficiently different in nature that they are not limited by some of these factors. Several goals have been proposed to define areas of investigation into $(DI)^2$ principles. Some of these goals were listed in the previous section. The most ambitious of these goals is a 10 kV, 1 ampere switch with a maximum leakage current of 50 mA and a switching time of 10 microseconds.

Some results obtained in a previous program have shown that these goals are worth pursuing and simultaneously illustrate the wide range of possible applications of $(DI)^2$ devices. In the realm of high voltage, threshold voltages of well over 1 kV have been measured, although these same devices exhibited high holding voltages also. Gate-controlled switching has been achieved with reasonable gate currents and one microsecond switching time; and some devices have shown a tendency to operate at integrated circuit logic levels.

Other $(DI)^2$ characteristics such as extreme radiation hardness and high-temperature operation are almost certain to find application in areas that conventional devices cannot fill. Operation of $(DI)^2$ devices at temperatures as high as 420°C has been reported (conventional silicon devices are limited to about 200°C) and other devices were apparently not seriously degraded by irradiation to over 100 megarads (conventional radiation-hardened integrated circuits are limited to about one megarad). Both of these properties are of great interest to those who would like to operate semiconductor devices in hostile environments. In addition to serving as high-power devices, the $(DI)^2$ phenomena may find application in a new family of low-power integrated circuits and devices.

The bipolar high-power thyristor is a fairly mature technology, and further improvements in its operating parameters will be severely constrained by fundamental physical limitations. It could be hoped that $(DI)^2$ technology represents a new approach that will avoid some of these limitations and will provide a step function improvement in selected areas.

3. DEEP-IMPURITY DOUBLE-INJECTION DEVICES

3.1 SEMICONDUCTORS WITHOUT DEEP LEVELS

A pure semiconductor material such as silicon, germanium, or gallium arsenide has an atomic density which is near 5 E 22 atoms per cubic centimeter. These materials contain a characteristic concentration of mobile charge carriers (electrons and/or holes) which will be in the range 1 E 6 (gallium arsenide) to 1 E 13 (germanium) per cubic centimeter at ordinary temperatures. This charge density distinguishes them from insulators which may contain a few hundred or fewer carriers per cubic centimeter, and from metallic conductors which may contain on the order of 1 E 22 carriers per cubic centimeter.

The charge carrier density (more than zero but less than one charge carrier per atom) is explained by the presence of a "forbidden energy gap," a range of energies which are quantum mechanically forbidden to the electrons present on the constituent atoms. Electrons with energies equal to or greater than some characteristic energy called the conduction band edge are free to move through the crystal lattice. Electrons with energies less than another characteristic value called the valence band edge are firmly bound to their atoms. This is illustrated in an "energy band diagram" as shown in Figure 1. It is conventional to show electron energy as increasing upward in these diagrams.

An electron which acquires sufficient energy (e.g., thermal energy) to enter the conduction band leaves behind a positively charged atom. The positive charge (a hole) is also free to move through the crystal lattice in the conduction band. Both carriers contribute to electrical current when a potential is applied.

Semiconductors are made to be useful by incorporating certain impurities or "dopants" into some of the atomic sites in the crystal

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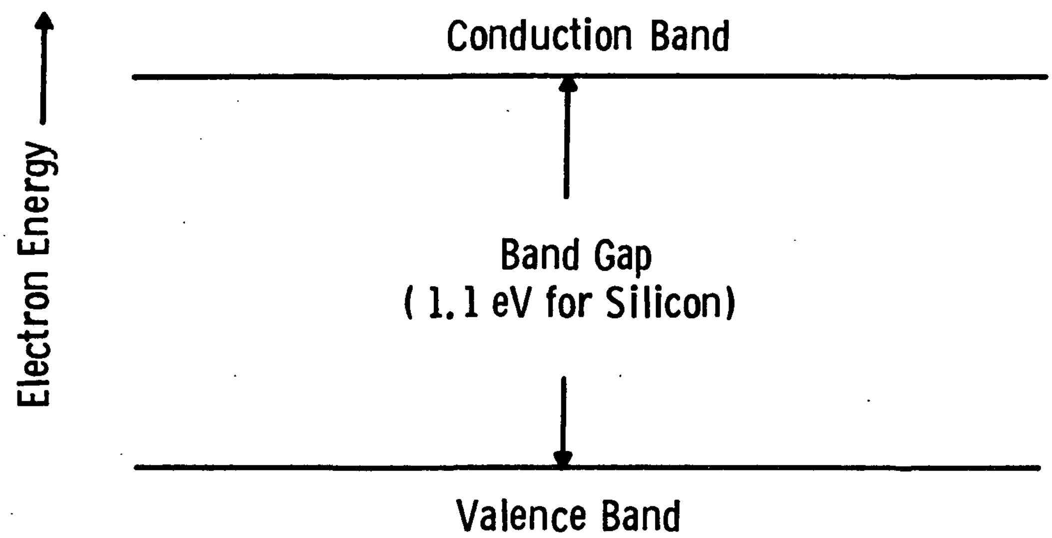

Figure 1. Band diagram of a pure semiconductor.

lattice. Atoms such as phosphorus or arsenic in silicon are easily ionized by "donating" an electron into the conduction band; these are called "n-type dopants" or donor atoms. Atoms such as boron or aluminum in silicon are easily ionized by "accepting" an electron from the silicon atoms; these are called "p-type dopants" or acceptor atoms. The doped semiconductor is described as "n type" or "p-type" depending upon which type of dopant predominates. N-type semiconductors conduct current principally by means of the movement of electrons; p-type semiconductors conduct current principally by holes. N-type and p-type semiconductors are illustrated by the band diagrams in Figure 2.

For practical purposes it can be assumed that every donor atom contributes a mobile electron to the crystal and every acceptor atom contributes a hole. By incorporating increasing concentrations of donors or acceptors into a silicon crystal, it is possible to reduce its resistivity from the 3 E 5 ohm-cm characteristic of pure silicon to any value down to less than 1 E -3 ohm-cm for silicon heavily doped with 1 E 20 dopant atoms per cubic centimeter. The "Fermi level" shown in Figure 2 is an energy level that represents a one-half probability that an electron of that energy will be in the conduction band.

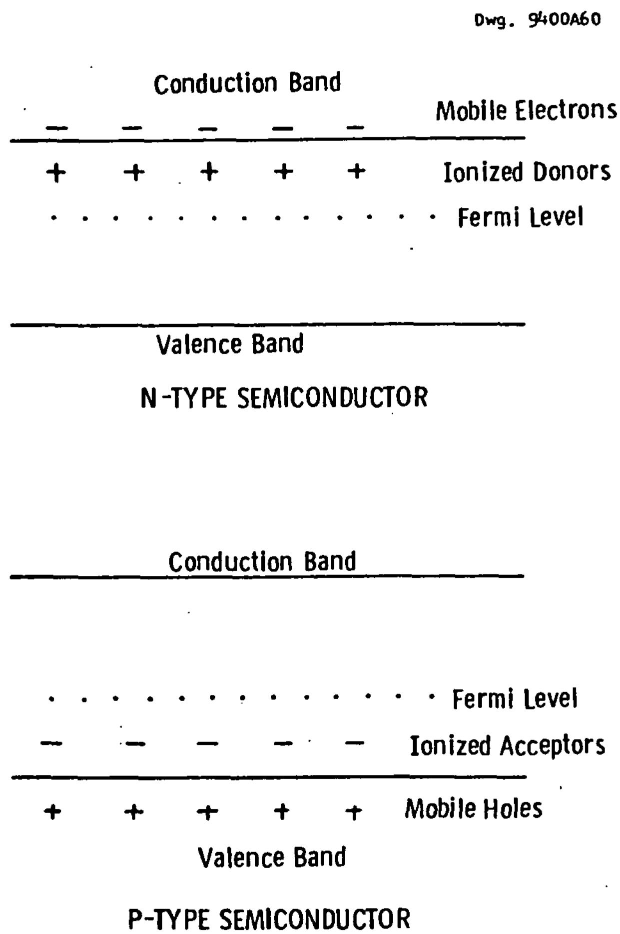

Figure 2. Band diagram of a doped semiconductor.

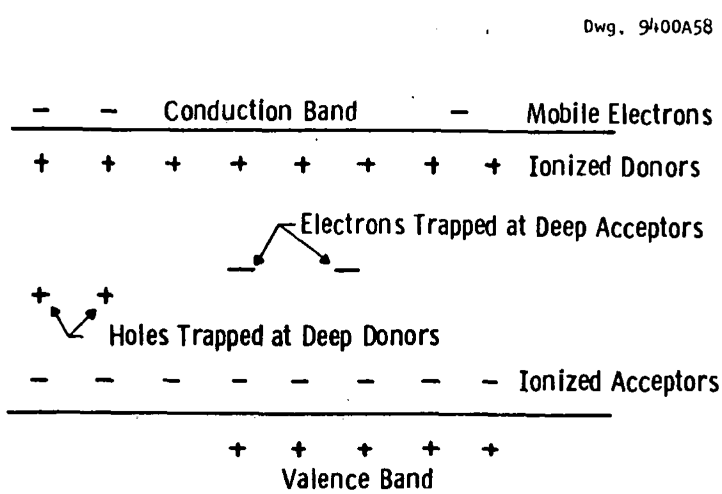

Figure 3. Band diagram of a doped semiconductor with deep-level dopants.

3.2 DEEP LEVELS — PRINCIPLES OF OPERATION

Another class of dopants called deep-level dopants are conventionally to be avoided in semiconductor technology. These dopants are usually heavy metals and are characterized by ionization energies which are larger than those of conventional donors and acceptors. The nature of these deep levels is illustrated in the band diagram of Figure 3.

A deep level can be either a deep donor or deep acceptor and often can function as either. They are deleterious to the operation of most semiconductor devices, contributing to leakage currents and reducing the gain of bipolar devices. Deep-level acceptors and donors are often called "traps" because a mobile electron or hole can lose energy by attaching itself to a deep-level atom.

It is the trapping ability of deep levels that finds application in deep-level, double-injection — $(DI)^2$ — devices. For example, if silicon containing 1 E 15 phosphorus atoms per cubic centimeter (and therefore having 1 E 15 mobile electrons per cubic centimeter) is doped with increasing concentrations of gold, more and more electrons are trapped at the gold atoms and removed from the conduction band. When the gold concentration reaches a value near 2 E 16/cc, essentially all of the mobile electrons will be trapped and the silicon will be a high-resistivity material. If now contacts are applied to the silicon and a voltage is applied, very little current will flow through the high-resistivity material and the $(DI)^2$ device would be described as being in an OFF state.

In order to understand the other characteristics of $(DI)^2$ devices, it is necessary to consider the conceptual device depicted in Figure 4.

This figure represents a piece of n-type silicon which has been doped with a deep-level atom such as gold, so that the silicon resistivity in the body of the device is quite high. At each end of the device is a contact; the n^+ contact is the cathode which consists of a region that has been very heavily doped with phosphorus (so that the relative gold concentration in this region is negligible) and is then contacted with a metal electrode. The p^+ region is similarly very

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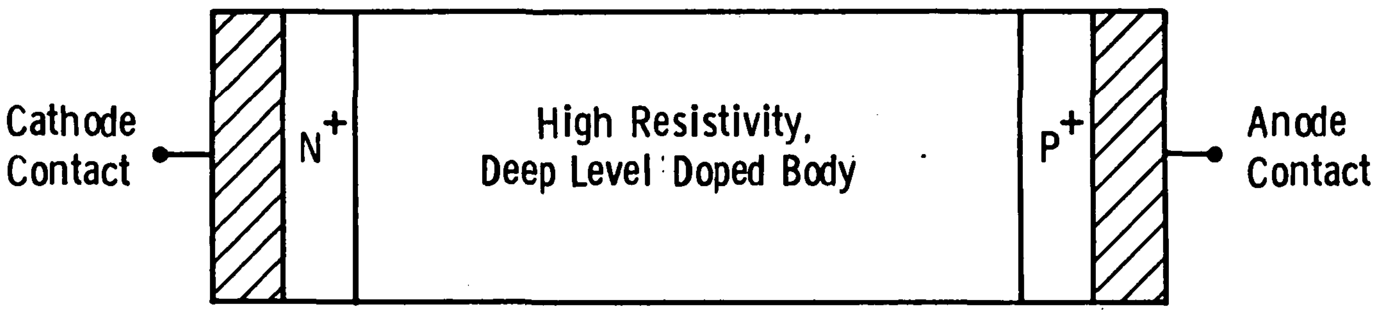

Figure 4. A $(DI)^2$ diode.

heavily doped with boron and has a metal electrode; it constitutes the anode. This device will be used to illustrate the principles of $(DI)^2$ operation.

With no voltage applied to the device, most of the electrons from the ionized donor (phosphorus) atoms have been trapped at the gold atom sites, leaving only a low electron concentration. As a small voltage is applied, ohmic current flows through the device, carried by the untrapped electrons. Because the resistivity is high, the current flow is small (Figure 5).

As the applied voltage is increased, another mode of current flow begins to become significant. This current is called the space-charge-limited current and is independent of the electron concentration in the material. In this mode, electrons which are present in the n^+ cathode are injected into the high-resistivity body and flow through the material under the influence of their own space charge. The following description of the space-charge-limited current follows that given by Ghandi.[b]

b. Sorab K. Ghandi, "Semiconductor Power Devices," John Wiley and Sons, New York (1977).

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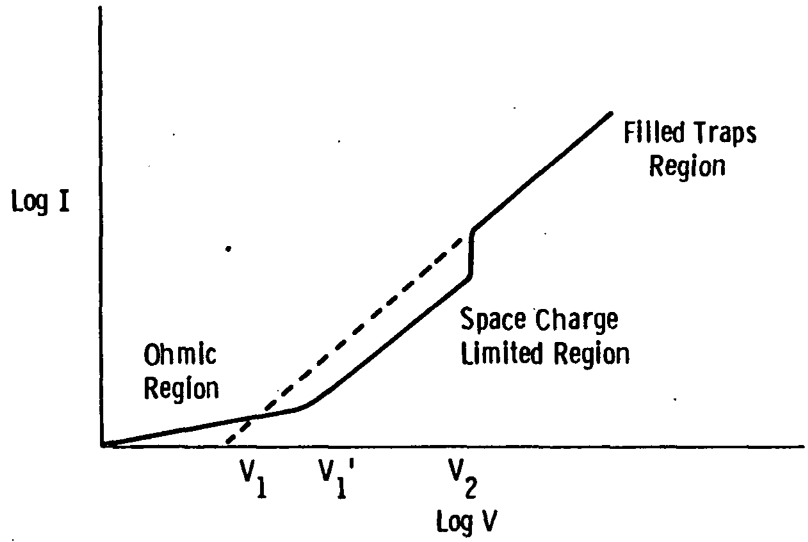

Figure 5. Current-voltage characteristics of a $(DI)^2$ diode.

We continue to assume that there is a single deep trapping level and that these trapping sites have been filled with electrons from the conduction band. When a voltage is applied across the device, electrons are injected into the body from the cathode and holes are injected from the anode. The electrons will not be trapped since the trapping sites are filled, but will flow under the influence of the electric field toward the anode. Holes injected from the anode, however, are readily trapped at the negatively charged trapping sites and are not able to traverse the length of the device before they are trapped; they cannot alter the injected electron space charge near the cathode and so the electron current is controlled by its own space charge. The transport equations for this process are

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{\rho}{\epsilon} = q\,\frac{n}{\epsilon} \qquad (1)$$

$$\text{and} \quad J = nq\mu E \qquad (2)$$

where V is the voltage, J is the current density, ρ is the charge density, q is the magnitude of the electronic charge, n is the electron concentration, E is the electric field, ϵ is the permittivity of silicon, and μ is the electron mobility.

Solving these equations gives

$$E^2 = \left(\frac{dV}{dx}\right)^2 = \left(\frac{2\ J}{\epsilon\ \mu}\right) x + E_c^2 \tag{3}$$

where E_c is the electric field at the cathode.

As J increases, the field at the cathode becomes smaller and eventually vanishes. This is the current density for which the current is entirely space charge limited. Solution of the above equation for the space-charge-limited condition in a device of length L gives

$$J_{scl} = \frac{9}{8}\ \frac{\epsilon\ \mu}{L^3}\ V^2 \tag{4}$$

As the voltage across the device increases further, the field across the device eventually becomes high enough that holes are injected faster than they are trapped. These holes reach the cathode where they reduce the electron space charge, permitting more electrons to be injected while the lifetime of holes increases. The process is regenerative and results in a negative resistance characteristic such as that illustrated in Figure 6.

Characteristic of this mode of operation is that, at some current density, J_B, the voltage is a minimum. At current densities above this value, the injection rate exceeds the recombination rate and space charge builds up again.

Other modes for obtaining a negative resistance exist. One of these is avalanche injection which can be envisioned as follows. Consider the same structure as before with the exception that the anode region is replaced with another n^+ contact. This contact is not capable of injecting holes into the device body, so double injection as described above cannot take place. However, we have shown that, under the space-charge-limited condition, the electric filed increases with distance from the cathode, reaching its maximum at the anode. If the applied voltage is high enough, this field can reach the avalanche breakdown field for silicon (~ 1.5 E 5 V/cm) and electron/hole pairs will be created. The electrons will be collected at the positive anode, but the holes will be "injected" into the device body, leading again to double injection and negative resistance.

Under some conditions, such as an inhomogeneity in the device body, another mode of negative resistance operation can take place. The electric field can be locally concentrated causing impact ionization, leading again to electron-hole pair production and essentially to double-injection conditions with negative resistance.

All of these processes which cause a negative resistance behavior result in current filaments; that is, the majority of the current flows in stable regions of the semiconductor of which the cross sectional area is less than the area available for current flow. That this must be true can be shown by again considering the I-V characteristic shown in Figure 6. Assume that a device of cross section A is momentarily biased at the point on the negative resistance part of the curve labeled X, corresponding to a current density J_X and therefore to a total current which is AJ_x. The voltage will tend toward its minimum value V_B where the negative differential resistance becomes zero, corresponding to stable operation. The current density increases to the value J_B, regardless of whether the total current is allowed to increase or not. This is accomplished by current flowing through a smaller cross-sectional area than before. In this condition, the resistivity of the smaller cross-sectional area is decreased further, while the resistivity of the rest of the device area increases. The process continues regeneratively until nearly all the current flows through the highly conductive filament, while the remainder of the current flows through the rest of the device at the much lower current density J_B' .

Curve 755114-A

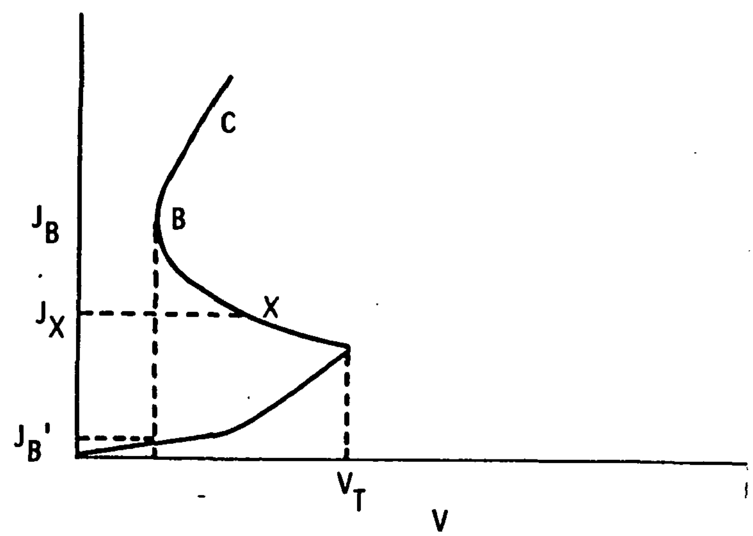

Figure 6. Negative resistance in a $(DI)^2$ diode.

The implications of this mode of operation of negative resistance devices is that, although it is convenient to assume the entire cross sectional area of a device as available for current flow and for efficient heat removal, this assumption is optimistic and the thermal characteristics of negative resistance devices are more complex.

3.2.1 High-Voltage $(DI)^2$ Switching Circuit

It would be desirable to have a high-power device which switches from a low-conductivity OFF state to a high-conductivity ON state in response to a triggering signal. The $(DI)^2$ diode that was described above, of course, is not triggerable but could still find use in a high-voltage switching circuit as described below.

The response of one particular $(DI)^2$ diode is shown in Figure 7. This oscillograph shows the voltage and current waveforms resulting from the application of a 400 V, 300 microsecond pulse to a deep-impurity, double-injection device. Because 400 V exceeds the threshold voltage of this particular device by only a small amount, the switching transition in this case is slow (about 50 microseconds); the oscillograph clearly shows the delay time, the switching process, and the high-current, low-voltage ON state of the device.

100 mA/Div.
100 V/Div.
50 μs/Div.

Wafer AU-1
Device 1-1 (999 Ohm in Series)

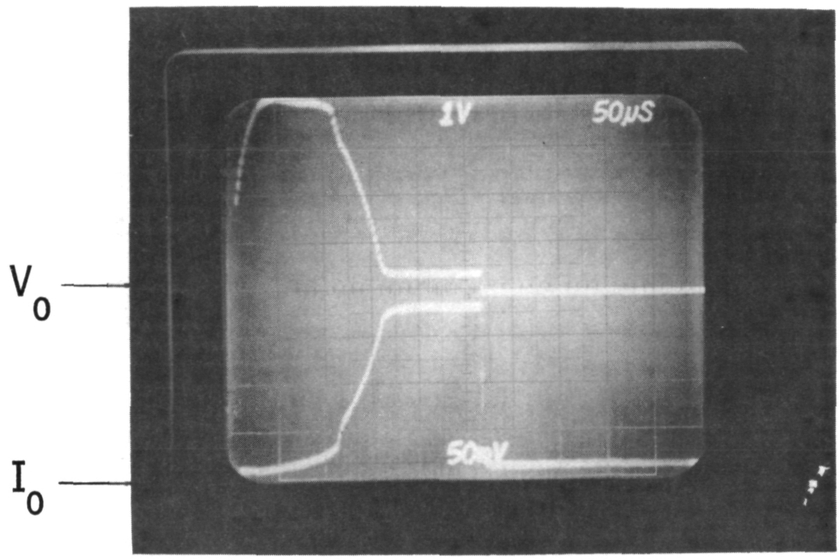

Figure 7. Oscillograph of the switching transition in a non-gated $(DI)^2$ device.

Note that the switching process in this device is initiated by the application of a voltage pulse; there is no third terminal to trigger the switching action.

Such a device can be used, along with a triggerable thyristor, in a high-voltage switch. The high-voltage capability is achieved through connecting several deep-impurity, double-injection devices in series with each other and with another, triggerable high-voltage device such as a thyristor. The triggerable device can be operated near ground potential in order to avoid insulation problems in the triggering circuit. The scheme is shown in Figure 8.

In operation, high voltage from a source such as a pulse-forming network would be applied across the high-voltage switch. This voltage would be near, but less than, the combined threshold voltages of the deep-impurity, double-injection devices; the current flowing through these devices would therefore be small. Equal voltage sharing between the deep-impurity, double-injection devices and the thyristor can be

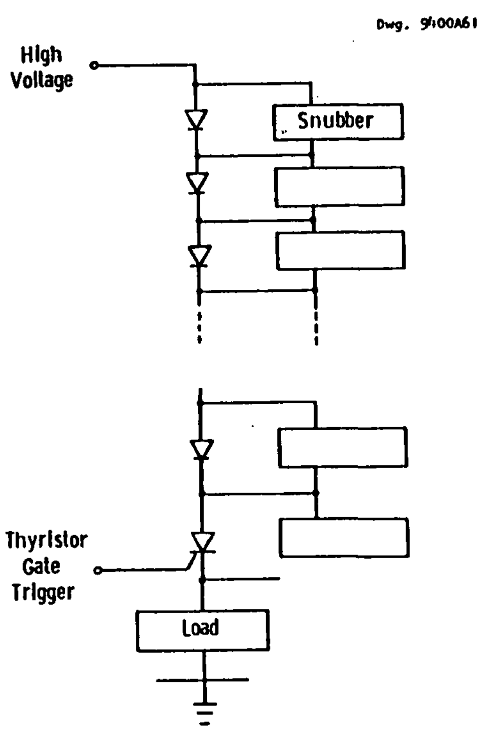

Figure 8. Schematic representation of a high-voltage switch using deep-impurity, double-injection devices along with a separate, triggerable thyristor.

accomplished through a resistive network in parallel with the high-voltage devices.

Triggering the thyristor ON causes the voltage across each of the deep-impurity, double-injection devices to increase to the threshold value, causing them to switch to the high-current, low-voltage mode, and the entire high-voltage switch switches to the ON condition, sending a high-current pulse through the load.

Because there is no method of turning the switch OFF, it will continue to conduct current as long as a sufficient voltage is maintained by the voltage source. This is the conventional mode of operation of thyristor circuits.

The advantages of this type of high-voltage switch over conventional high-voltage thyristor strings are:

a) Since only one of the devices in the series string requires a triggering signal, the difficulties inherent in sending trigger signals to those devices that are at high potentials relative to ground can be avoided.
b) Because the switching of one device in a series string automatically causes other devices in the string to switch without the necessity of simultaneously applying trigger signals to each device in the string, a high degree of switch reliability is obtained.
c) Deep-impurity, double-injection devices are, at least in principle, easy to fabricate since they do not require high-voltage p-n junctions. The ease of fabrication can be expected to provide cost savings compared to the fabrication of high-voltage thyristors.
d) Deep-impurity, double-injection devices can be made as lateral devices on a semiconductor wafer, thus avoiding the difficulties associated with double-sided diffusions and metallization required with high-voltage thyristors. It would even be possible to series connect several deep-

impurity, double-injection devices on a single wafer instead of separating them for individual packages as is required for high-voltage thyristors.

Since other investigations have shown that silicon deep-impurity, double-injection devices are capable of operating at higher temperatures (over 400°C), then those permissible for thyristor operation (125°C), such a high-voltage switch might be useful in certain high-temperature applications where conventional silicon devices cannot be used. It has also been shown that silicon deep-impurity, double-injection devices continue to operate normally after exposure to high doses of nuclear radiation (in excess of 100 mega-rads total dose). This characteristic would permit the use of deep-impurity, double-injection switches in applications involving nuclear fission or fusion reactors and in military or space applications.

3.2.2 Background of $(DI)^2$ Phenomena

Murray A. Lampert is given credit as the man who first described the phenomena which could be ascribed to traps and space-charge-limited current in solids. His work is summarized in a comprehensive book which he co-authored.[c]

Most of the interest in the practical applications of $(DI)^2$ devices has come from the work of a group headed by Professor H. Thurman Henderson at the University of Cincinnati. Students under Dr. Henderson's guidance have investigated an amazing variety of semiconductor devices based upon the principles of deep-level-compensated semiconductors and $(DI)^2$. Some possible applications of these devices have been shown to be in the areas of gas flow metering and magnetic field sensing as well as in current switching. A sophisticated computer-modelling program was developed for the analysis of $(DI)^2$ behavior. In view of the complex characteristics of $(DI)^2$ devices, this computer simulation has been the most reliable source of

c. "Current Injection in Solids," Murray A. Lampert and Peter Mark, Academic Press, New York (1970).

information relating to the characteristics of these devices.

Another worker in the field, Dr. W. T. Joyner of Hampden-Sydney College, has performed valuable work in the areas of radiation and temperature tolerance of $(DI)^2$ devices. He has reported that a total dose of 800 megarads (Si) causes only a 10-15% change in the threshold voltage, holding voltage, and leakage current of $(DI)^2$ devices, and that further irradiation results in very little further change.

3.2.3 Device Design

3.2.3.1 Computer Models

3.2.3.1.1 Basic Program. A simple computer program was written to illustrate some of the time-dependent characteristics of electron injection into a perfect insulator. The perfect insulator is a fairly good approximation to a $(DI)^2$ diode which has been heavily doped with gold to a high-resistivity state, in which the electron traps are filled so that further trapping of injected electrons can be neglected.

For purposes of these illustrative calculations, the diode was divided into five to fifty physical segments along the device length and the injection of a constant current was modelled as a fixed number of electrons entering the first physical segment during each short time interval, dt. Dr. Dennis Whitson of the University of Pennsylvania at Indiana, who previously worked on the NASA-sponsored $(DI)^2$ program, consented to review the model and the results. He believes it is accurate in its present form and for the physical constraints assumed in the analysis.

The program was written to calculate the electric field and the injected electron concentration throughout the body of the device as well as the anode voltage as a function of time. Steady-state operation was taken to be that condition where the electron current flowing out the anode connection was at least 99% of the electron current being injected into the cathode contact. Those computational parameters which limit the accuracy of the calculations are the number of sections into which the device is divided and the time increment employed between successive calculations. Surprisingly, the choice of these parameters was not crucial, as is shown in the set of representative calculations in Table 5.

It can be seen from Table 5 that the values of the terminal voltage are not much different whether 5 or 20 sections of the device are used in the calculations and whether the time interval is taken to be 1 E -10 or 1 E -11 seconds. The program that was used for these calculations and other tabulated results are recorded in the Appendix.

TABLE 5

INJECTION INTO INSULATING SILICON

(Sudden drift approximation. No donors or acceptors. No hole current. Electron mobility = 1248 cm^2/V-sec. No diffusion current. Iteration performed until current out > .99 of current in.)

AS A FUNCTION OF NUMBER OF SECTIONS AND d_t

I = 1 A, L = 0.1 cm, AREA = 1 cm^2

SECTIONS	d_t	TIME	FIELD	VOLTS
5	1E-09	1.70E-08	7.74E3	2.82E2
	1E-10	2.08E-08	1.08E4	3.82E2
	1E-11	2.13E-08	1.11E4	3.92E2
20	1E-09	6.00E-09	3.24E3	1.33E2
	1E-10	1.61E-08	1.07E4	3.65E2
	1E-11	1.76E-08	1.18E4	3.96E2

From calculations such as the above, the correct relationship among voltage, current density, and device length is obtained, i.e.,

$$J = C \frac{V^2}{L^3} \qquad (5)$$

Such a relationship can be used to calculate that, e.g., for a switch which is 1 mm^2 in area and is to have a threshold voltage of 10,000 V while conducting only 50 mA (current density of 5 A/cm^2), as is described in one of the Spec-goals, a device length of 0.5 cm is required.

3.2.3.1.2 Shieh's Program. A much more complete, rigorous, and sophisticated computer model was the subject of T. J. Shieh's Ph.D. thesis at the University of Cincinnati. Shieh considered all relevant modes of carrier generation and recombination as well as electrode effects in his analysis.

Although analytical descriptions of the behavior of $(DI)^2$ devices have been widely published, they are based upon simplifying assumptions that may mask the real device behavior. Therefore, the best source of information on the capabilities of gold-doped silicon $(DI)^2$ devices is Shieh's computer simulations. Results from some of these simulations are used later in this report.

3.2.3.2 Previous Devices

In previous Westinghouse investigations of $(DI)^2$ principles and applications, several different types of devices were fabricated. These are reviewed below.

3.2.3.2.1 Vertical Devices. A vertical $(DI)^2$ device is the most similar to the high-power thyristor; i.e., anode and cathode contacts are formed on opposing faces of a silicon wafer, as illustrated in Figure 9.

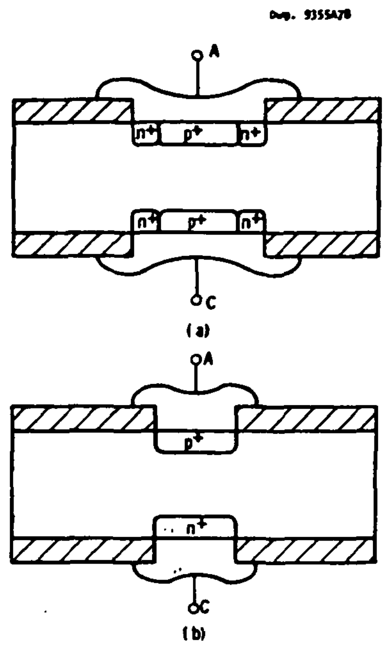

Figure 9. Schematic of a vertical $(DI)^2$ device.

Advantages of this design include a minimization of edge and surface effects; however, such a device is difficult to manufacture because it depends upon "through-the-wafer" mask alignments to form the opposing electrodes, and a third electrode for gating purposes would be difficult to incorporate. Other disadvantages arise from the large cross-sectional area available for current flow, while the area available for heat sinking remains small. The importance of this is discussed later under thermal considerations.

3.2.3.2.2 High-Voltage Planar Square Devices. During previous investigations, several wafers of the design called the "High-Voltage Planar Square" were completed and tested while others were partially processed. In this investigation, those partially processed wafers were completed through the fabrication process and the devices were tested. The High-Voltage Planar Square design includes a large number of devices on a single wafer. Some of these devices were designed as diodes, some as injection gate transistors, and still others as MOS gate transistors. A drawing showing the metallization pattern of a wafer of these devices is shown in Figure 10.

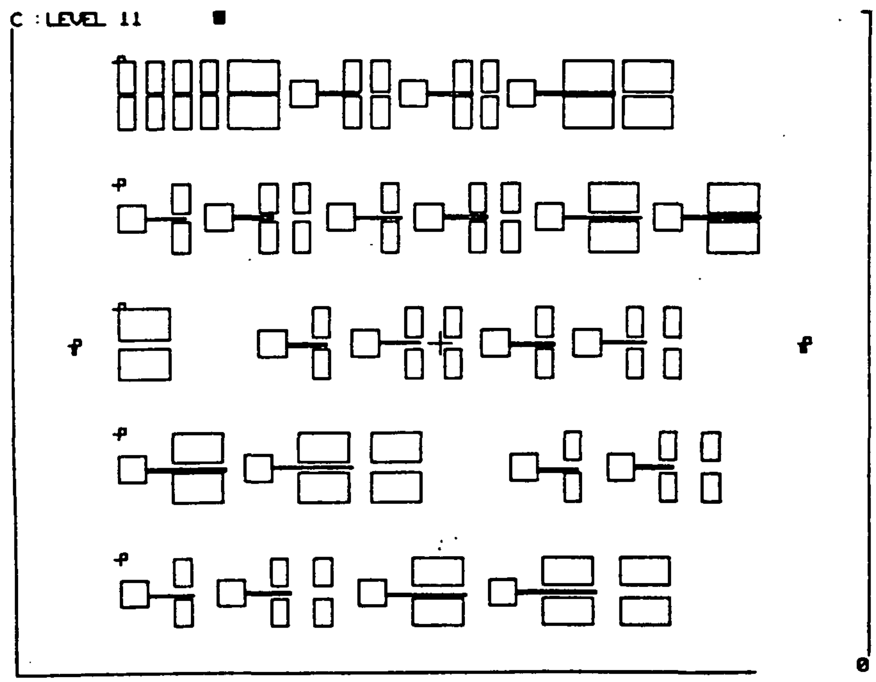

Figure 10. Metallization pattern for the High-Voltage Planar Square Devices.

Drawings of the masks for the High-Voltage Lateral Square $(DI)^2$ devices were reviewed, and the relevant dimensions of devices defined by these masks were recorded for future reference. These dimensions are included in Table 6 of this report for purposes of reference and documentation. The meanings of the dimensions are illustrated in the accompanying sketch (Figure 11).

The complete mask set for the High-Voltage Planar Square design consists of 11 different masks which can be used in different combinations in order to form different devices.

The first mask to be applied to wafers defines the boron diffusion and it can be either:

Mask #1, which defines the boron diffusion for those wafers on which the transistors will have MOS gates only, or

Mask #2, which defines the boron diffusion for wafers on which the transistors will have boron injection gates where the injection gate length is to be 60 μm, or

TABLE 6

DIMENSION OF THE HIGH-VOLTAGE PLANAR SQUARE MASK SET

DIMENSIONS (MICRONS) OF THE HIGH VOLTAGE PLANAR SQUARE MASKS FOR MOS GATES. THE SMALL GATED DEVICE IS 5-6 (REVERSED LEFT TO RIGHT FROM MASK DRAWINGS).

DEVICE NUMBER	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8
MASK #1, INSIDE (BORON) DIFFUSION FOR MOS GATES																			
BORON WIDTH	2250	2250	750	750	250	250	2250	750	250	250	250	2250	2250	750	750	750	250	250	250
BORON LENGTH	100	100	100	100	100	100	100	100	200	100	50	100	100	100	100	100	100	100	100
BORON/BORON DISTANCE	340	340	340	340	340	340	220	220	320	220	170	460	460	460	460	460	460	460	460
MASK #4, OUTSIDE (PHOS) DIFFUSION																			
PHOS WIDTH	2250	2250	750	750	250	250	2250	750	250	250	250	2250	2250	750	750	750	250	250	250
PHOS LENGTH	50	50	50	50	50	50	50	50	100	50	25	50	50	50	50	50	50	50	50
GAP FOR BORON	100	100	100	100	100	100	100	100	200	100	50	100	100	100	100	100	100	100	100
PHOS/PHOS DISTANCE	240	240	240	240	240	240	120	120	120	120	120	360	360	360	360	360	360	360	360
WIDTH/DISTANCE	9.38	9.38	3.13	3.13	1.04	1.04	18.8	6.25	2.08	2.08	2.08 -	6.25	6.25	2.08	2.08	2.08	0.69	0.69	0.69
MASK #5 OR #6, MOS GATE WINDOW																			
GATE LENGTH MASK #5		60		60		60						60	60		60	60		60	60
GATE LENGTH MASK #6		120		120		120						120	120		120	120		120	120
GATE WIDTH		2450		950		450						2450	2450		950	950		450	450
GATE TO DIFFUSION DISTANCE		60		60		60						150	100		150	100		150	100
MASK #7, ANODE AND CATHODE CONTACT ETCH FOR MOS GATE																			
WINDOW WIDTH	2250	2250	750	750	250	250	2250	750	250	250	250	2250	2250	750	750	750	250	250	250
WINDOW LENGTH	200	200	200	200	200	200	200	200	400	200	100	200	200	200	200	200	200	200	200

DEVICE NUMBER	3-1	3-2	3-3	3-4	3-5	3-6	3-7	4-1	4-2	4-3	4-4	4-5	4-6	5-1	5-2	5-3	5-4	5-5	5-6
MASK #1, INSIDE (BORON) DIFFUSION FOR MOS GATES																			
BORON WIDTH	750	750	750	250	250	250	2250	250	250	250	2250	2250	2250	2250	2250	2250	750	750	750
BORON LENGTH	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
BORON/BORON DISTANCE	580	580	580	580	580	580	460	700	700	700	580	580	580	700	700	700	700	700	700
MASK #4, OUTSIDE (PHOS) DIFFUSION																			
PHOS WIDTH	750	750	750	250	250	250	2250	250	250	250	2250	2250	2250	2250	2250	2250	750	750	750
PHOS LENGTH	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
GAP FOR BORON	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
PHOS/PHOS DISTANCE	480	480	480	480	480	480	360	600	600	600	480	480	480	600	600	600	600	600	600
WIDTH/DISTANCE	1.56	1.56	1.56	0.52	0.52	0.52	6.25	0.42	0.42	0.42	4.69	4.69	4.69	3.75	3.75	3.75	1.25	1.25	1.25
MASK #5 OR #6, MOS GATE WINDOW																			
GATE LENGTH MASK #5		60	60		60	60			60	60		60	60		60	60		60	60
GATE LENGTH MASK #6		120	120		120	120			120	120		120	120		120	120		120	120
GATE WIDTH		950	950		450	450			450	450		2450	2450		2450	2450		950	950
GATE TO DIFFUSION DISTANCE		210	120		210	120			210	120		210	120		210	120		210	120
MASK #7, ANODE AND CATHODE CONTACT ETCH FOR MOS GATE																			
WINDOW WIDTH	750	750	750	250	250	250	2250	250	250	250	2250	2250	2250	2250	2250	2250	750	750	750
WINDOW LENGTH	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200	200

MASK #10 OR #11, METAL. MASK #10 FOR 60 MICRON MOS OR INJECTION GATES, MASK #11 FOR 120 MICRON MOS OR INJECTION GATES.

DIMENSIONS (MICRONS) OF THE HIGH VOLTAGE PLANAR SQUARE MASKS FOR INJECTION GATES

DEVICE NUMBER	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8
MASK #2 OR #3, INSIDE (BORON) DIFFUSION AND BORON INJECTION GATE																			
BORON WIDTH	2250	2250	750	750	250	250	2250	750	250	250	250	2250	2250	750	750	750	250	250	250
BORON LENGTH	100	100	100	100	100	100	100	100	200	100	50	100	100	100	100	100	100	100	100
BORON/BORON DISTANCE	340	340	340	340	340	340	220	220	320	220	170	460	460	460	460	460	460	460	460
GATE LENGTH MASK #2		60		60		60						60	60		60	60		60	60
GATE LENGTH MASK #3		120		120		120						120	120		120	120		120	120
MASK #4, OUTSIDE (PHOS) DIFFUSION																			
PHOS WIDTH	2250	2250	750	750	250	250	2250	750	250	250	250	2250	2250	750	750	750	250	250	250
PHOS LENGTH	50	50	50	50	50	50	50	50	100	50	25	50	50	50	50	50	50	50	50
GAP FOR BORON	100	100	100	100	100	100	100	100	200	100	50	100	100	100	100	100	100	100	100
PHOS/PHOS DISTANCE	240	240	240	240	240	240	120	120	120	120	120	360	360	360	360	360	360	360	360
WIDTH/DISTANCE	9.38	9.38	3.13	3.13	1.04	1.04	18.8	6.25	2.08	2.08	2.08	6.25	6.25	2.08	2.08	2.08	0.69	0.69	0.69
MASK #8 OR #9, CONTACT WINDOWS FOR ANODE, CATHODE, AND INJECTION GATES																			
GATE LENGTH MASK #8		60		60		60						60	60		60	60		60	60
GATE LENGTH MASK #9		120		120		120						120	120		120	120		120	120
GATE WIDTH		2450		950		450						2450	2450		950	950		450	450
GATE TO DIFFUSION DISTANCE		60		60		60						150	100		150	100		150	100

DEVICE NUMBER	3-1	3-2	3-3	3-4	3-5	3-6	3-7	4-1	4-2	4-3	4-4	4-5	4-6	5-1	5-2	5-3	5-4	5-5	5-6
MASK #2 OR #3, INSIDE (BORON) DIFFUSION AND BORON INJECTION GATE																			
BORON WIDTH	750	750	750	250	250	250	2250	250	250	250	2250	2250	2250	2250	2250	2250	750	750	750
BORON LENGTH	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
BORON/BORON DISTANCE	580	580	580	580	580	580	460	700	700	700	580	580	580	700	700	700	700	700	700
GATE LENGTH MASK #2		60	60		60	60			60	60		60	60		60	60		60	60
GATE LENGTH MASK #3		120	120		120	120			120	120		120	120		120	120		120	120
MASK #4, OUTSIDE (PHOS) DIFFUSION																			
PHOS WIDTH	750	750	750	250	250	250	2250	250	250	250	2250	2250	2250	2250	2250	2250	750	750	750
PHOS LENGTH	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50	50
GAP FOR BORON	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100	100
PHOS/PHOS DISTANCE	480	480	480	480	480	480	360	600	600	600	480	480	480	600	600	600	600	600	600
WIDTH/DISTANCE	1.56	1.56	1.56	0.52	0.52	0.52	6.25	0.42	0.42	0.42	4.69	4.69	4.69	3.75	3.75	3.75	1.25	1.25	1.25
MASK #8 OR #9, CONTACT WINDOWS FOR ANODE, CATHODE, AND INJECTION GATES																			
GATE LENGTH MASK #8		60	60		60	60			60	60		60	60		60	60		60	60
GATE LENGTH MASK #9		120	120		120	120			120	120		120	120		120	120		120	120
GATE WIDTH		950	950		450	450			450	450		2450	2450		2450	2450		950	950
GATE TO DIFFUSION DISTANCE		210	120		210	120			210	120		210	120		210	120		210	120

MASK #10 OR #11, METAL. MASK #10 FOR 60 MICRON MOS OR INJECTION GATES, MASK #11 FOR 120 MICRON MOS OR INJECTION GATES.

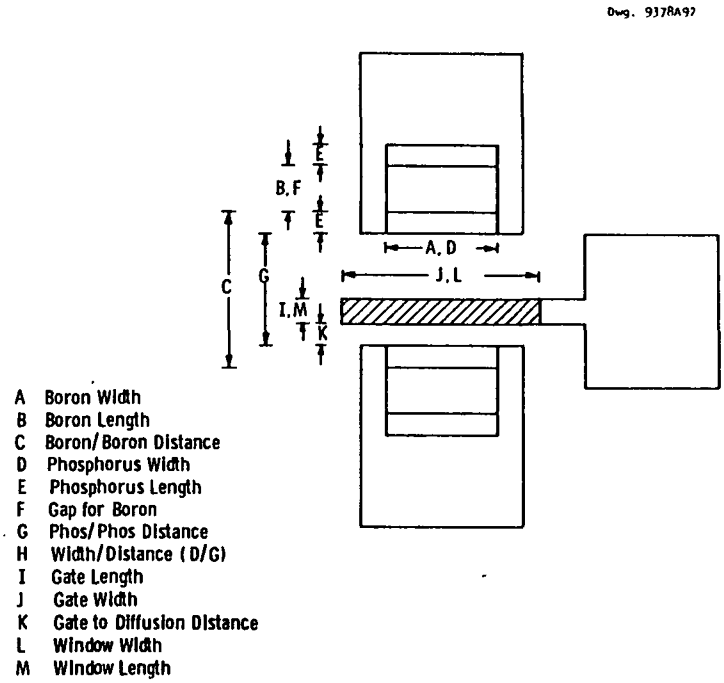

Figure 11. Dimensions of a High-Voltage Planar Square device.

Mask #3, which defines the boron diffusion for wafers on which the transistors will have boron injection gates where the injection gate length is to be 120 μm.

Mask #4 is the second mask to be applied and is the phosphorus diffusion mask. This mask is the same for all transistor designs.

The third mask to be applied is used only for wafers on which the transistors are to have MOS gates. It is either:

Mask #5, which opens gate windows for MOS gates that are 60 μm long, or

Mask #6, which opens gate windows for MOS gates that are 120 μm long.

The fourth mask to be applied opens the windows for metal contact. It is either:

Mask #7 for anode and cathode contact to wafers with MOS gate transistors, or

Mask #8 for contact to anode, cathode, and injection gate for wafers with injection gates of 60 μm length, or

Mask #9 for contact to anode, cathode, and injection gates for wafers with injection gate lengths of 120 μm.

The fifth mask to be applied defines the metal pattern. It is either:

Mask #10 for wafers on which the transistors have either injection gates or MOS gates with lengths of 60 μm, or

Mask #11 for wafers on which the transistors have either injection gates or MOS gates the length of which is 120 μm.

When the above masking options are combined with the various device dimensions that are defined on each wafer, and considering that there are many variations and options in starting material, the method of introducing deep levels, and the concentration of deep levels in each wafer, an overwhelming variety of devices can be produced.

3.2.3.3 Planar Annular

3.2.3.3.1 Transistors and Diodes. The principle device design investigated in this program has been a planar annular design. Features of this design are that one electrode (usually the emitter) is a circle which can be completely surrounded by a ring gate in close proximity to that electrode. The other electrode is also in the shape of a ring so that there are no edge effects to be considered. A drawing representative of this design is shown in Figure 12. In addition to transistors and diodes, several test structures consisting of resistance contacts and capacitor structures are included in the mask set. These structures and their use are discussed later.

The emitter and collector each can be any of seven types:

A solid shape formed during the first diffusion (normally boron).

A solid shape formed during the second diffusion (normally phosphorus).

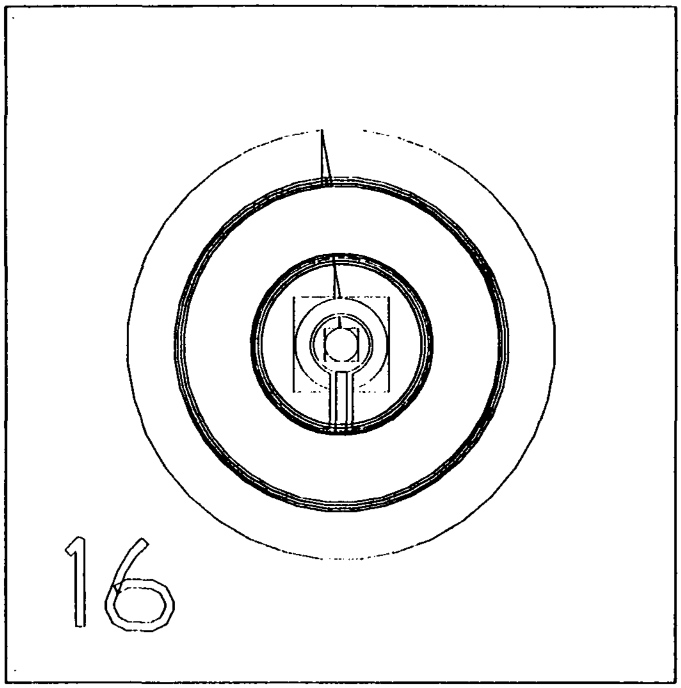

Figure 12. Representative planar annular $(DI)^2$ transistor.

Shieh electrode with the first diffusion surrounded by the second diffusion.

Reverse Shieh electrode with the second diffusion surrounded by the first diffusion.

Separate dots formed by the first diffusion.

Separate dots formed by the second diffusion.

Shieh electrode dots.

The gate can be any of four types:

A ring formed by the first diffusion to make an injection gate.

A ring formed by the second diffusion to make an injection gate,

A ring formed by the first and second diffusions to make a Shieh injection gate.

A depletion mode MOS gate.

An enhancement mode MOS gate.

Other rules that govern the device design are:

All "circles" are in reality 36-sided polygons.

All emitters are of 775 μm outside radius.

All collectors have an outside radius 60 μm greater than the inside radius.

All depletion, enhancement, and simple injection gates are 20 μm long.

All injection gates and depletion gates begin 20 μm from the emitter edge.

All normal Shieh electrodes have a 20 μm long, second diffusion ring on the channel side; a 10 μm space; a 20 μm long, first diffusion ring; and a 10 μm space (the rest of the electrode is formed by the second diffusion).

All Shieh injection gates are 80 μm long, consisting of 20 μm of the second diffusion, a 10 μm space, 20 μm of the first diffusion, a 10 μm space, and 20 μm of the second diffusion.

Reverse Shieh electrodes and gates interchange the positions of the first and second diffusions.

All simple dots are 40 μm long (radially) and 20 μm wide.

All Shieh dots are a 20 μm square of the first diffusion surrounded by a 10 μm space and a square of the second diffusion (the outside dimension of this square is 80 μm).

Test capacitors have a 775 μm radius and overlap the contact diffusion by 20 μm. The Shieh and reverse Shieh contacts for capacitors have a 60 μm wide inner ring and the capacitor overlaps this ring by 20 μm.

3.2.3.3.2 Dot Electrodes. The purpose of using dots and Shieh dots as emitters and collectors in some of the transistors was to evaluate the importance of filament current in $(DI)^2$ devices. Presumably, a current filament must have a minimum cross-sectional area in order to be stable. If the electrodes are of this size or smaller, then the formation of current filaments would not be possible, and more predictable operation might result. The dot contacts also can be expected to improve self-heating effects in devices.

3.2.3.3.3 Capacitors. Capacitors using the gate oxide as a dielectric were incorporated into the design to serve as test structures to determine conductivity type, should it become necessary. The wafer contact for the capacitors can be either from the first diffusion, the second diffusion, or of the Shieh type in order to make certain that an ohmic contact would be available on any wafer.

3.2.3.3.4 Resistivity Monitors. Three sets of diffused contact regions are incorporated into the mask in order to allow resistivity measurements on unmetallized wafers. Each set consists of two 1 mm x 10 mm rectangles formed by the first and second diffusions so that ohmic contact will be made regardless of whether the wafer is n-type or p-type. The rectangles are separated by 1 mm.

The function of the resistivity test patterns in the mask set is to permit the wafer resistivity to be monitored during the gold diffusion processes. At the gold diffusion step, these diffused regions are bare silicon and can be contacted by probes.

A major difficulty encountered in these studies has been the four-point probe measurement of silicon which has attained high resistivity due to the compensating effects of substitutional gold. The difficulty arises from the extremely high contact resistance at the probe tips which requires a very high impedance voltmeter for measurement. Although a conventional four-point probe tester was modified to use very high-impedance voltmeters, the high impedance of the system made it very sensitive to electrical noise in the constant current supply. Diffused contact regions are incorporated into the mask set in order to enable more accurate measurement of completed or partially completed wafers during the gold diffusion process.

The design of the diffused regions is such that, at the measurement voltage, any space-charge-limited injected current will always be less than the ohmic current, even for intrinsic silicon. The space-charge-limited current density is given by

$$J = \frac{9}{8} \epsilon \epsilon_o \mu \frac{V^2}{L^3} \qquad (6)$$

which, for these structures (L = 0.1 cm) is approximately 3 E -5 A/cm^2 with 5 V applied. The minimum ohmic current density (for "intrinsic" N-type silicon) would be approximately 2 E -4 A/cm^2, a value sufficiently greater than the injected current such that it can be assumed that only ohmic current is being measured as long as the measuring voltage is reasonably low.

A summary of the features of each device and test pattern in the mask set is given in Table 7.

3.2.3.4 Design for Low Holding Voltage

As a result of discussions during the May 11, 1987, coordination meeting at NASA/Lewis, increased attention was paid to the holding voltage of $(DI)^2$ devices. In order to develop an investigation scheme of the holding voltages, the computer-modeling data of Shieh (along with some additional unpublished data by N. K. Min) were tabulated along with some derived quantities and are listed in Table 8.

In this table:

Column 1 ("PHOS") lists the shallow donor used in the device modeling.

Column 2 ("GOLD") lists the gold concentration.

Column 3 ("GOLD/PHOS") lists the ratio of gold concentration to shallow donor concentration.

Column 4 ("LENGTH") is the distance, in μm, between the anode and cathode of the modeled device.

Column 5 ("RESISTIVITY") is the estimated resistivity (from Bullis' graph) of the compensated silicon.

Column 6 ("Vt") is the threshold voltage near 300°K predicted by the computer model.

TABLE 7

FEATURES OF THE DEVICES AND TEST STRUCTURES OF THE PLANAR ANNULAR DESIGN

NO.	EMITTER DIFFUSION	COLLECTOR DIFFUSION	E-C SPACE	GATE
1	2	2	160	NONE
2	2	2	160	NONE
3	2	2	160	NONE
4	2	2	640	NONE
5	SHIEH	SHIEH	160	NONE
6	SHIEH	SHIEH	160	NONE
7	SHIEH	SHIEH	160	NONE
8	SHIEH	SHIEH	160	NONE
9	SHIEH	SHIEH	640	NONE
10	SHIEH	SHIEH	640	NONE
11	SHIEH	SHIEH	20	ENHANCE
12	SHIEH	SHIEH	160	DEPLETE
13	SHIEH	SHIEH	160	SHIEH
14	SHIEH	SHIEH	160	1
15	SHIEH	SHIEH	640	1
16	SHIEH	SHIEH	640	2
17	SHIEH	SHIEH	160	2
18	SHIEH	SHIEH	640	SHIEH
19	SHIEH	SHIEH	640	DEPLETE
20	SHIEH	SHIEH	40	ENHANCE
21	1	2	20	ENHANCE
22	1	2	160	DEPLETE
23	1	2	160	SHIEH
24	1	2	160	1
25	1	2	640	1
26	1	2	640	2
27	1	2	160	2
28	1	2	640	2
29	1	2	640	DEPLETE
30	1	2	40	ENHANCE
31	1_DOTS	2_DOTS	20	ENHANCE
32	1_DOTS	2_DOTS	160	DEPLETE
33	1_DOTS	2_DOTS	160	SHIEH
34	1_DOTS	2_DOTS	160	1
35	1_DOTS	2_DOTS	160	2
36	1_DOTS	2_DOTS	640	SHIEH
37	1_DOTS	2_DOTS	640	DEPLETE
38	1_DOTS	2_DOTS	40	ENHANCE
39	SHIEH_DOT	SHIEH_DOT	20	ENHANCE
40	SHIEH_DOT	SHIEH_DOT	160	DEPLETE
41	SHIEH DOT	SHIEH DOT	160	SHIEH
42	SHIEH_DOT	SHIEH_DOT	160	1
43	SHIEH_DOT	SHIEH_DOT	160	2
44	SHIEH_DOT	SHIEH_DOT	640	SHIEH
45	SHIEH_DOT	SHIEH_DOT	640	DEPLETE
46	SHIEH_DOT	SHIEH_DOT	40	ENHANCE
47	2	2	20	ENHANCE
48	2	2	160	DEPLETE
49	2	2	160	SHIEH
50	2	2	160	1
51	2	2	640	1
52	2	2	640	2
53	2	2	160	2
54	2	2	640	SHIEH
55	2	2	640	DEPLETE
56	2	2	40	ENHANCE
57	1	2	20	NONE
58	1	2	160	NONE
59	GATE OXIDE CAPACITOR TO DIFFUSION 1			
60	GATE OXIDE CAPACITOR TO DIFFUSION 2			
61	GATE OXIDE CAPACITOR TO SHIEH			
62	GATE OXIDE CAPACITOR TO REV_SHIEH			
63	1	2	160	NONE
64	1	2	640	NONE
65	1	2	640	NONE
66	1	2	40	NONE
67	REV_SHIEH	REV_SHIEH	160	DEPELETE
68	REV_SHIEH	REV_SHIEH	160	SHIEH
69	REV_SHIEH	REV_SHIEH	160	1
70	REV_SHIEH	REV_SHIEH	160	2
71	REV_SHIEH	REV_SHIEH	640	SHIEH
72	REV_SHIEH	REV_SHIEH	640	DEPLETE
73	2_DOTS	2_DOTS	160	SHIEH
74	2_DOTS	2_DOTS	160	1
75	2_DOTS	2_DOTS	160	2
76	2_DOTS	2-DOTS	640	SHIEH
77	1_BARS	1-BARS	1000	TOP LEFT OF WAFER
78	2_BARS	2_BARS	1000	TOP RIGHT OF WAFER
79	1_BARS	1-BARS	1000	MIDDLE LEFT OF WAFER
80	2_BARS	2_BARS	1000	MIDDLE RIGHT OF WAFER
81	1_BARS	1-BARS	1000	BOTTOM LEFT OF WAFER
82	2_BARS	2_BARS	1000	BOTTOM RIGHT OF WAFER

TABLE 8

COMPUTER-CALCULATED PARAMETERS OF $(DI)^2$ DEVICES
AND SOME DERIVED QUANTITIES RELATING TO LOW HOLDING VOLTAGE

PHOS	GOLD	GOLD/PHOS	LENGTH	RESISTIVITY	Vt	Vh	Vt/Vh	J@Vt	J@Vh	P@Vt	P@Vh	P/VOLT^2
5.0E+14	1.0E+15	2.00	200	2.00E+04	50.0	13	3.85	4	80	200	1040	5.00E-05
5.0E+14	1.0E+15	2.00	300	2.00E+04	150.0	35	4.29	4.5	130	675	4550	5.00E-05
5.0E+14	1.0E+15	2.00	400	2.00E+04	350.0	70	5.00	6	200	2100	14000	5.00E-05
5.0E+14	1.0E+15	2.00	500	2.00E+04	600.0	120	5.00	6	220	3600	26400	5.00E-05
5.0E+14	8.0E+14	1.60	100	1.00E+04	4.5	3	1.80	0.7	26	3	65	1.00E-04
5.0E+14	1.0E+15	2.00	100	2.00E+04	5.5	3	1.83	1.2	40	7	120	5.00E-05
5.0E+14	1.2E+15	2.40	100	2.30E+04	7.5	5	1.67	2	55	15	240	4.35E-05
5.0E+14	1.6E+15	3.20	100	4.00E+04	10.5	6	1.91	4	85	42	468	2.50E-05
5.0E+14	2.0E+15	4.00	100	5.00E+04	15.0	8	1.94	6.3	130	95	1008	2.00E-05
5.0E+14	2.4E+15	4.80	100	5.50E+04	19.8	11	1.84	10	200	198	2150	1.82E-05
5.0E+14	2.8E+15	5.60	100	7.50E+04	24.5	16	1.58	13	230	319	3565	1.33E-05
5.0E+14	2.9E+15	5.80	100	8.00E+04	27.0	18	1.52	15	240	405	4260	1.25E-05
5.0E+14	8.0E+14	1.60	200	1.00E+04	44.0	12	3.67	3	50	132	600	1.00E-04
5.0E+14	1.0E+15	2.00	200	2.00E+04	55.0	16	3.44	4.5	75	248	1200	5.00E-05
5.0E+14	1.2E+15	2.40	200	2.30E+04	66.0	21	3.14	6	100	396	2100	4.35E-05
5.0E+14	1.6E+15	3.20	200	4.00E+04	90.0	32	2.81	9	200	810	6400	2.50E-05
5.0E+14	2.0E+15	4.00	200	5.00E+04	106.0	48	2.21	12	300	1272	14400	2.00E-05
5.0E+14	2.4E+15	4.80	200	5.50E+04	140.0	76	1.84	18	450	2520	34200	1.82E-05
5.0E+14	2.8E+15	5.60	200	7.50E+04	168.0	108	1.56	25	650	4200	70200	1.33E-05
5.0E+14	2.9E+15	5.80	200	8.00E+04	176.0	116	1.52	30	750	5280	87000	1.25E-05
5.0E+14	8.0E+14	1.60	300	1.00E+04	145.0	30	4.83	4.5	100	653	3000	1.00E-04
5.0E+14	1.0E+15	2.00	300	2.00E+04	170.0	40	4.25	5.2	130	884	5200	5.00E-05
5.0E+14	1.2E+15	2.40	300	2.30E+04	195.0	50	3.90	6.5	200	1268	10000	4.35E-05
5.0E+14	1.6E+15	3.20	300	4.00E+04	245.0	85	2.88	8.5	400	2083	34000	2.50E-05
5.0E+14	2.0E+15	4.00	300	5.00E+04	295.0	140	2.11	11	620	3245	86800	2.00E-05
5.0E+14	2.4E+15	4.80	300	5.50E+04	365.0		---	15		5475	---	1.82E-05
5.0E+14	2.8E+15	5.60	300	7.50E+04	445.0		---	20		8900	---	1.33E-05
5.0E+14	2.9E+15	5.80	300	8.00E+04	470.0		---	25		11750	---	1.25E-05
5.0E+13	1.0E+15	20.00	200	2.80E+05	33.0	29	1.14	10	75	330	2175	3.57E-06
1.0E+14	1.0E+15	10.00	200	1.30E+05	32.0	26	1.23	7.5	62	240	1612	7.69E-06
2.0E+14	1.0E+15	5.00	200	7.00E+04	35.0	22	1.59	5	62	175	1364	1.43E-05
7.5E+15	7.6E+15	1.01	203	7.00E+02	680		---			---	---	1.43E-03
1.0E+12	1.0E+15	1000.00	203	9.00E+04	12		---			---	---	1.11E-05
1.0E+13	1.0E+15	100.00	203	2.00E+05	14		---			---	---	5.00E-06
5.0E+14	1.0E+15	2.00	203	2.00E+04	47		---			---	---	5.00E-05
8.0E+14	1.0E+15	1.25	203	5.00E+02	53		---			---	---	2.00E-03
9.0E+14	1.0E+15	1.11	203	4.00E+02	52		---			---	---	2.50E-03
5.0E+13	7.6E+15	152.00	203	6.00E+04	270		---			---	---	1.67E-05
5.0E+14	7.6E+15	15.20	203	2.10E+05	280		---			---	---	4.76E-06
6.0E+15	7.6E+15	1.27	203	6.00E+03	490		---			---	---	1.67E-04
6.5E+15	7.6E+15	1.17	203	5.00E+03	600		---			---	---	2.00E-04
7.1E+15	7.6E+15	1.07	203	3.00E+03	370		---			---	---	3.33E-04
7.2E+15	7.6E+15	1.06	203	2.00E+03	375		---			---	---	5.00E-04
7.3E+15	7.6E+15	1.04	203	1.80E+03	520		---			---	---	5.56E-04
7.4E+15	7.6E+15	1.03	203	1.60E+03	680		---			---	---	6.25E-04
7.5E+15	7.6E+15	1.01	203	1.40E+03	680		---			---	---	7.14E-04
5.0E+14	7.6E+15	15.20	203	6.00E+04	290		---			---	---	1.67E-05
8.0E+14	7.6E+15	9.50	203	1.00E+05	330		---			---	---	1.00E-05

PHOS	GOLD	GOLD/PHOS	LENGTH	RESISTIVITY	Vt	Vh	Vt/Vh	J@Vt	J@Vh	P@Vt	P@Vh	P/VOLT^2
6.2E+15	7.6E+15	1.23	203	4.00E+03	450		----			----	----	2.50E-04
6.4E+15	7.6E+15	1.19	203	3.50E+03	510		----			----	----	2.86E-04
6.7E+15	7.6E+15	1.13	203	3.00E+03	610		----			----	----	3.33E-04
6.9E+15	7.6E+15	1.10	203	2.50E+03	410		----			----	----	4.00E-04
7.0E+15	7.6E+15	1.09	203	2.00E+03	310		----			----	----	5.00E-04
1.0E+15	7.6E+15	7.60	203	1.00E+05	420		----			----	----	1.00E-05
2.0E+15	7.6E+15	3.80	203	5.00E+04	650		----			----	----	2.00E-05
3.0E+15	7.6E+15	2.53	203	4.00E+04	860		----			----	----	2.50E-05
6.0E+15	7.6E+15	1.27	203	3.00E+04	860		----			----	----	3.33E-05
7.0E+15	7.6E+15	1.09	203	2.50E+04	930		----			----	----	4.00E-05
7.4E+15	7.6E+15	1.03	203	2.00E+04	1040		----			----	----	5.00E-05
1.0E+15	3.8E+15	3.80	203	5.00E+04	180		----			----	----	2.00E-05
2.0E+15	3.8E+15	1.90	203	1.30E+04	350		----			----	----	7.69E-05
2.5E+15	3.8E+15	1.52	203	1.00E+04	460		----			----	----	1.00E-04
3.4E+15	3.8E+15	1.12	203	5.00E+03	630		----			----	----	2.00E-04
3.5E+15	3.8E+15	1.09	203	4.00E+03	550		----			----	----	2.50E-04
3.6E+15	3.8E+15	1.06	203	3.00E+03	500		----			----	----	3.33E-04
1.0E+15	6.2E+15	6.20	203	7.30E+04	300		----			----	----	1.37E-05
2.0E+15	6.2E+15	3.10	203	4.30E+04	560		----			----	----	2.33E-05
3.0E+15	6.2E+15	2.07	203	4.00E+04	840		----			----	----	2.50E-05
4.0E+15	6.2E+15	1.55	203	1.00E+04	840		----			----	----	1.00E-04
5.0E+15	6.2E+15	1.24	203	5.00E+03	870		----			----	----	2.00E-04
6.0E+15	6.2E+15	1.03	203	2.00E+03	950		----			----	----	5.00E-04
1.0E+15	5.3E+15	5.30	203	6.50E+04	250		----			----	----	1.54E-05
2.0E+15	5.3E+15	2.65	203	3.00E+04	450		----			----	----	3.33E-05
3.0E+15	5.3E+15	1.77	203	1.30E+04	820		----			----	----	7.69E-05
4.0E+15	5.3E+15	1.33	203	8.00E+03	810		----			----	----	1.25E-04
4.5E+15	5.3E+15	1.18	203	7.00E+03	880		----			----	----	1.43E-04
5.1E+15	5.3E+15	1.04	203	1.00E+03	930		----			----	----	1.00E-03
1.0E+15	5.0E+15	5.00	203	6.00E+04	240		----			----	----	1.67E-05
2.0E+15	5.0E+15	2.50	203	2.50E+04	460		----			----	----	4.00E-05
3.0E+15	5.0E+15	1.67	203	1.30E+04	810		----			----	----	7.69E-05
4.0E+15	5.0E+15	1.25	203	5.00E+03	860		----			----	----	2.00E-04
4.5E+15	5.0E+15	1.11	203	4.00E+03	870		----			----	----	2.50E-04
4.8E+15	5.0E+15	1.04	203	3.50E+03	850		----			----	----	2.86E-04
5.0E+14	1.0E+15	2.00	100	2.00E+04	5	3	1.67			----	----	5.00E-05
5.0E+14	1.0E+15	2.00	200	2.00E+04	60	20	3.00			----	----	5.00E-05
5.0E+14	1.0E+15	2.00	300	2.00E+04	200	30	6.67			----	----	5.00E-05
5.0E+14	1.0E+15	2.00	400	2.00E+04	300	70	4.29			----	----	5.00E-05
5.0E+14	1.0E+15	2.00	500	2.00E+04	500	100	5.00			----	----	5.00E-05
5.0E+14	1.0E+15	2.00	600	2.00E+04	700	120	5.83			----	----	5.00E-05
4.0E+14	1.0E+15	2.50	200	1.00E+04	49	17	2.88	4.5	75	221	1275	1.00E-04
6.0E+14	1.0E+15	1.67	200	4.00E+03	62	16	3.88	4.5	87	279	1392	2.50E-04
8.0E+14	1.0E+15	1.25	200	1.00E+03	69	14	4.93	4.2	100	290	1400	1.00E-03
1.0E+15	1.0E+15	1.00	200	2.00E+02	60	13.5	4.44	3.7	115	222	1553	5.00E-03
5.0E+13	2.0E+15	40.00	200	3.00E+05	102	100	1.02	38	230	3876	23000	3.33E-06
1.0E+14	2.0E+15	20.00	200	2.50E+05	98	86	1.14	30	220	2940	18920	4.00E-06
2.0E+14	2.0E+15	10.00	200	1.30E+05	98	70	1.40	25	220	2450	15400	7.69E-06

PHOS	GOLD	GOLD/PHOS	LENGTH	RESISTIVITY	Vt	Vh	Vt/Vh	JQVt	JQVh	PQVt	PQVh	P/VOLT^2
4.0E+14	2.0E+15	5.00	200	6.00E+04	108	55	1.96	14	240	1512	13200	1.67E-05
6.0E+14	2.0E+15	3.33	200	3.00E+04	122	46	2.65	11	260	1342	11960	3.33E-05
8.0E+14	2.0E+15	2.50	200	2.50E+04	136	42	3.24	8.5	300	1156	12600	4.00E-05
1.0E+15	2.0E+15	2.00	200	1.80E+04	155	39	3.97	8	350	1240	13650	5.56E-05
1.5E+15	2.0E+15	1.33	200	1.00E+04	202	34	5.94	6.2	440	1252	14960	1.00E-04
2.0E+15	2.0E+15	1.00	200	4.00E+01	190	32	5.94	5.5	600	1045	19200	2.50E-02
3.0E+14	6.0E+14	2.00	200	1.00E+04	24	10	2.40	1.3	25	31	250	1.00E-04
4.0E+14	8.0E+14	2.00	200	1.30E+04	38	13	2.92	2.4	45	91	585	7.69E-05
5.0E+14	1.0E+15	2.00	200	2.00E+04	55	16	3.44	3.5	75	193	1200	5.00E-05
6.0E+14	1.2E+15	2.00	200	2.50E+04	72	20	3.60	5	120	360	2400	4.00E-05
7.0E+14	1.4E+15	2.00	200	1.50E+04	90	25	3.60	6	180	540	4500	6.67E-05
8.0E+14	1.6E+15	2.00	200	1.20E+04	112	29	3.86	6.8	250	762	7250	8.33E-05
9.0E+14	1.8E+15	2.00	200	1.80E+04	133	34	3.91	7.5	300	998	10200	5.56E-05
1.0E+15	2.0E+15	2.00	200	1.80E+04	155	38	4.08	8	350	1240	13300	5.56E-05
				GRADIENT								
5.0E+14	1.0E+15	2.00	200	-0.40	22.5	15	1.50	4.5	69	101	1035	5.00E-05
5.0E+14	1.0E+15	2.00	200	0.00	55	15	3.67	4.5	82	248	1230	5.00E-05
5.0E+14	1.0E+15	2.00	200	0.40	130	15	8.67	3	94	390	1410	5.00E-05
5.0E+14	1.0E+15	2.00	200	0.80	202	15	13.47	2.5	100	505	1500	5.00E-05
5.0E+14	1.0E+15	2.00	200	1.00	190	15	12.67	2	104	380	1560	5.00E-05
5.0E+14	1.0E+15	2.00	300	0.00	170	33	5.15	5.5	133	935	4389	5.00E-05
5.0E+14	1.0E+15	2.00	300	0.20	270	32	8.44	4	139	1080	4448	5.00E-05
5.0E+14	1.0E+15	2.00	300	0.40	450	31	14.52	3	146	1350	4526	5.00E-05
5.0E+14	1.0E+15	2.00	300	0.60	740	29	25.52	2.5	160	1850	4640	5.00E-05

Column 7 ("Vh") is the holding voltage (when available) predicted by the computer model.

Column 8 ("Vt/Vh") is the ratio of the predicted threshold voltage to the predicted holding voltage.

Column 9 ("J@Vt") is the predicted current density at the threshold voltage (where available).

Column 10 ("J@Vh") is the predicted current density at the holding voltage (where available).

Column 11 ("P@Vt") is a relative number related to the calculated dissipated power in the device at the threshold voltage (the product of the threshold voltage and the current density at the threshold voltage).

Column 12 ("P@Vh") is a relative number related to the calculated dissipated power in the device at the holding voltage (the product of the holding voltage and the current density at the holding voltage).

Column 13 ("P/VOLT") is a relative number which is related to the power dissipated in the device in the resistive regime below the threshold voltage (the reciprocal of the estimated resistivity).

The last nine lines in Table 8 represent modeling of devices with a gold concentration gradient; column 5 gives the values of the gradient instead of the compensated resistivity.

Since many of the numbers contained in these tables were estimated from graphic representations of the computed data, the accuracy of the absolute values of the numbers are merely moderate. However, from the tabulated data it is possible to deduce some of the factors that will affect the holding voltage of $(DI)^2$ devices, and it is possible to evaluate how some other parameters are simultaneously affected.

First, it is obvious that the lower threshold voltages are obtained from the shorter devices (e.g., see lines 1, 2, 3, 4, and 6 in Table 8). The shorter devices also have lower threshold voltages and lower ratios of threshold voltage to holding voltage. The shorter devices have lower current densities at the threshold and holding voltages.

Secondly, lines 5-11 in Table 8 on page 41 indicate that lower holding voltages are obtained with lower gold/phosphorus ratios (lower compensated resistivities). At the same time, the threshold voltages are lower and the ratio of threshold voltage to holding voltage is fairly constant. The current densities are lower for the lower gold/phosphorus ratios.

Thirdly, lines 7-14 in Table 8 on page 43 show that lower holding voltages are obtained with higher resistivity starting material when the gold/phosphorus ratio is maintained at a constant value. Simultaneously, the threshold voltage, the ratio of threshold voltage to holding voltage, and the current densities become lower as the starting material resistivity is increased.

In summary, those device and material parameters (within the ranges that have been modelled) that will tend to give the lowest holding voltages are (a) short devices, (b) low gold-to-phosphorus ratios, and (c) high-resistivity starting material. At the same time, threshold voltage, ratio of threshold voltage to holding voltage, and current densities are also predicted to be lower. Of these, the lower threshold voltage appears to be the most serious loss in terms of the design of a practical device.

The following device design is proposed for achieving low holding voltage while preventing the device from switching at low threshold voltages: starting material of approximately 10 ohm-cm (5 E 14 phosphorus/cc), compensated with 1 E 15/cc gold to increase the resistivity to approximately 20,000 ohm-cm; N^+ injection gate close to and completely surrounding a P^+ anode, and an N^+ cathode approximately 100 μm distant from the anode. These parameters (except for the injection gate) are the same as those in line 6 of Table 8 on page 41, which predict a holding voltage of 3 volts and a threshold voltage of 5.5 volts.

This device without a gate would switch ON at a very low negative cathode voltage. It is proposed that the N^+ gate be biased a few volts positive (reverse biased) with respect to the anode, which is considered to be ground. Under this condition, all electron current injected at the cathode would be removed at the gate, and the anode would be prevented from injecting holes. This would allow a high negative potential to be applied to the cathode without resulting in double-injection switching.

Switching to a low-resistance state could be initiated by reducing the gate potential to zero or below, allowing electron current to flow to the anode and allowing holes to be injected. Presumably, the device, once ON, could be turned OFF by again applying a positive potential to the gate. In order to do this, the gate supply would have to be capable of drawing a fairly high current, comparable to the device ON current, for a short period of time. The proposed device structure is illustrated in Figure 13.

In order to calculate some operating parameters of the proposed device, we assume an anode perimeter of 3.14 mm, anode-to-gate spacing of 10 μm, gate width of 10 μm, and anode-to-cathode spacing of 100, 200, and 300 μm (which includes the 10 μm gate). We have further assumed

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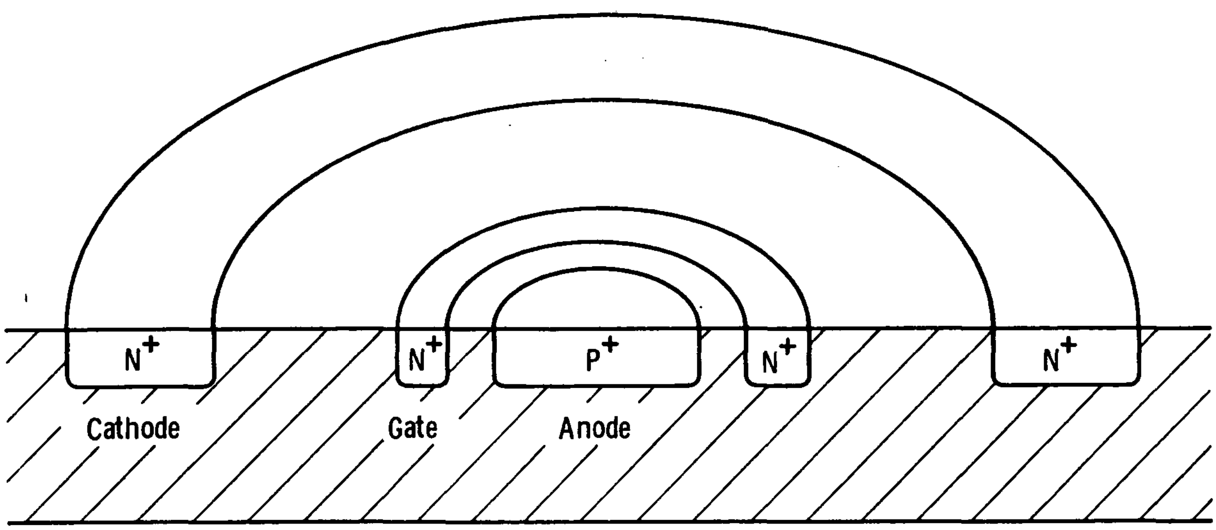

Fig. 1—Gates (DI) ^{2} device

Figure 13. Gated normally on (DI)^2 device.

that the appropriate currents effectively flow only in 20 μm of silicon near the device surface and that the holding voltage and the current densities are the same as those for the non-gated device of lines 1, 2, and 6 in Table 8 on page 41.

The operating parameter of principal interest is the current which must flow through the gate in order to prevent electrons from reaching the anode. This current consists of ohmic current flowing from the cathode to the gate, space-charge-limited current injected from the cathode to the gate, and leakage current flowing in the reverse-biased anode junction.

The ohmic current for this device will be given by

$$I_{ohmic} = \frac{w\,d}{\rho\,\ell}\,V \tag{7}$$

where w is the width of the channel, ℓ is the distance from cathode to gate, d is the depth of effective current flow in the device, and V is the potential difference between cathode and gate. The leakage current flowing in the reverse-biased junction will be much less than one milliampere, according to a graph in Shieh's thesis.

The space-charge-limited current will be

$$I_{scl} = w\,d\,\frac{9}{8}\,\epsilon\,\epsilon_o\,\mu\,\frac{V^2}{\ell^3} \tag{8}$$

and the major component of the gate current will be the space charge limited current. In some cases, this current will be higher than the anode-cathode current when the device switches ON.

Table 9 lists some of the calculated parameters of the proposed series of devices, assuming a gate potential of +5 V with respect to the anode.

TABLE 9

CALCULATED DEVICE CHARACTERISTICS
OF THE GATED, NORMALLY ON $(DI)^2$ DEVICE

ANODE-CATHODE SPACING (μm)	AVERAGE CHANNEL WIDTH (μm)	CATHODE-GATE SPACING (μm)	CATHODE-GATE POTENTIAL (V)	CATHODE-GATE SCL CURRENT (mA)	HOLDING VOLTAGE (V)	ON-STATE CURRENT (mA)
100	3460	80	505	311.0	3	27.7
			405	200.0		
			305	113.0		
			205	51.2		
			105	13.4		
			55	3.7		
200	3770	180	505	42.3	13	60.3
			405	27.2		
			305	15.4		
			205	7.0		
			105	1.8		
			55	0.5		
300	4080	280	505	16.7	35	106.0
			405	10.7		
			305	6.1		
			205	2.8		
			105	0.7		
			55	0.2		

4. THERMAL CONSIDERATIONS

Up to this point, we have alluded to the importance of designing for the removal of heat from the device, but have not yet described the problem quantitatively. This section presents some calculations of the importance of power dissipated as heat.

4.1 10 kV DEVICES

Thermal problems are most severe for high-voltage devices since they will naturally have high power dissipations. In this program, devices with threshold voltages as high as 10 kV have been considered, and these high-voltage devices are described first.

4.1.1 Vertical 10 kV Devices

Vertical devices, as described in an earlier section, are most like conventional high-power thyristors. They present special difficulties when implemented as $(DI)^2$ devices because of the difficulty in fabrication (requiring through-the-wafer mask alignment) and in finding a way to make a gate contact. The following calculations show the severity of the thermal problems with high-voltage, vertical devices.

Consider a high-voltage switch made from gold-compensated n-type silicon which is in the shape of a cube. Electrodes are at opposing faces of this cube. This would be the equivalent of a mesa structure device. It is enlightening to perform some calculations on the thermal characteristics of this device while it is in the OFF state near its threshold voltage. The ohmic leakage current is given by

$$I_{resistive} = \frac{V}{R} = \frac{V}{\rho}\frac{A}{L} \quad (11)$$

where R is the device resistance, ρ is the resistivity, A is the cross-section area, and L is the length of the device. The power dissipated in the device is

$$p = IV = \frac{V^2}{R} = \frac{AV^2}{\rho L} \tag{12}$$

The heat capacity of the device is

$$C = \text{Volume} \bullet \text{Density} \bullet \text{Specific Heat} \tag{13}$$

where the density will be taken to be 2.33 g/cc, and the specific heat will be taken to be 0.7 J/°C. If there is no path for heat to leave the device, its temperature will rise when voltage is applied. The adiabatic rate of rise of temperature in the device is

$$dT/dt = P/C \tag{14}$$

But let's assume that one electrode of the device, consisting of one face of the cube, is attached to a heat sink that will maintain the temperature of that electrode at a temperature of T_o. Then at steady state, the temperature of the device at some distance y from the electrode can be found by integrating

$$dT/dx = \frac{p(t-x)}{1.5\ A} \tag{15}$$

where 1.5 W/cm-°C is the thermal conductivity of silicon (at 300°K), A is the area, and t is the total device thickness.

This gives

$$T = T_o + \frac{P}{1.5\ A}\left(t\ y - \frac{y^2}{2}\right) \tag{16}$$

If our device is truly a cube, it will have four sides, each consisting of a rectangle. These sides must be passivated in some way so that surface-charging effects are not caused by ambient conditions. The most effective method of passivating silicon surfaces is by the growth of thermal oxide on the surfaces. The thermal oxide will contain some amount of positive fixed charge. If the oxide is carefully grown on these sides, and the faces are oriented in the optimum (100) plane, then it will be possible to lower the fixed oxide charge to 5 E 10/cm^2. Unless this fixed charge is balanced by negative traps, it will be balanced by an electron accumulation layer in the silicon. The channel mobility of the electrons in this accumulation layer will be on the order of 600 cm^2/V-sec. At the threshold voltage, the off-state current flowing in this accumulation layer will be

$$\begin{aligned} I &= E\ \mu\ N\ q\ W \\ &= 600\ V\ 5 \times 10^{10}\ 1.6 \times 10^{-19}\ \frac{W}{L} \end{aligned} \tag{17}$$

where E is the electric field, μ is the electron mobility, N is the charge density, q is the electron charge, W is the channel width, L is the device length, and V is the applied voltage. The power dissipation due to this channel current will be

$$P_{channel} = V\ I = 4.8 \times 10^{-6}\ V^2\ \frac{W}{L} \tag{18}$$

Another source of leakage current, and therefore off-state power dissipation, is the space-charge-limited current, which is not considered here. We now use these equations to calculate thermal effects.

The highest resistivity that can be obtained in silicon at room temperature is 3 E 5 ohm-cm. If we use this material for a 10 kV diode, then the resistive leakage current in the off state, blocking 10 kV, is given by equation (12). We assume now that the actual dimensions of the device are such that it is a 1 mm cube. For this device,

$$I_{resistive} = 3.3 \times 10^{-3} \text{ A} \tag{19}$$

and the power dissipated in the device is

$$P = IV = 33.3 \text{ W} \tag{20}$$

The heat capacity of the device is given by equation (13) and is

$$C = 1.63 \times 10^{-3} \text{ J/°C} \tag{21}$$

so the adiabatic rate of rise of temperature in the device is given by equation (14) and is

$$dT/dt = P/C = 2.04 \times 10^{4} \text{ °C/sec} \tag{22}$$

which means, for example, that the temperature would rise 200°C in 10 ms.

Now assume that one electrode of the device is attached to a heat sink which will maintain the temperature of that electrode at a temperature of T_o. Then the steady-state temperature of the device at some distance y from the heat sink is given by equation (16), so the temperature of the electrode opposite the heat sink (y = 0.1 cm) would be

$$T = T_o + 11.1\text{°C} \tag{23}$$

Now assume that the device switches ON and begins to conduct 10 A of current (1000 A/cm^2). If we wish to maintain the power dissipation at 33 W or less, then the forward voltage drop of the device must be 3.3 V or less, meaning that the ratio of threshold voltage to holding voltage must be at least 3000.

In actual practice, a silicon resistivity of 3 E 5 ohm-cm is difficult to obtain; a more representative resistivity would be on the order of 5 E 4 ohm-cm. If this material is used to form the 1 mm cube device, the power dissipation in the off state would be 200 W, the adiabatic rate of temperature rise would have been 1.23 E 5°C/sec, and the temperature of the electrode opposite the heat sink at steady state would be T_o + 67°C.

Considering now the channel current due to the electron accumulation layer, given by equation (17),

$$I_{channel} = 0.192 \text{ A} \tag{24}$$

The power dissipation in the OFF-state due to this channel current will be 1.92 kW, and the temperature rise at the electrode away from the heat sink will be 64°C. So it can be seen that the channel current leakage in a mesa device can be the limiting factor in designing high-voltage devices.

The channel leakage current can be reduced by increasing the length of the device, but this is not helpful in removing the heat due to power dissipation. For example, if the device is made to be 1 mm square in area, but with with a distance of 1 cm between the electrodes, the channel current is reduced to 19.2 mA and the power dissipation is reduced to 192 W. However, because one end of the device is now farther from the heat sink, the temperature rise at that electrode would now be 6,400°C. Note that this analysis has not considered that component of off-state power dissipation that would be due to space-charge-limited current.

We must conclude from this example that because (1) there is always a positive fixed charge associated with the silicon surface, and

(2) this fixed charge will induce an electron channel at the surface, and (3) the power dissipation in the OFF state due to this channel can be very large, and (4) increasing the electrode-electrode distance causes a very considerable temperature rise, that the mesa structure is not suitable for $(DI)^2$ devices designed for high-voltage applications.

4.1.2 Planar 10 kV Devices

Analysis of the vertical mesa structure $(DI)^2$ design shows the importance of maximizing the area available for heat sinking. The heat sink area can be increased with respect to the area available for current conduction by using a lateral design such that the direction of current flow is parallel to the heat sink.

We now consider the thermal implications of lateral designs and, as an example, consider designs in which the area available to the heat sink is held constant while the length and width of the device are varied. For convenience, we assume silicon is 1 mm thick in the direction perpendicular to the heat sink plane and to the direction of current flow.

In this case, we consider two types of material — the first has a realistic resistivity of 5 E 4 ohm-cm, the second has infinite resistivity. The third source of leakage current, space-charge-limited current, is now considered along with resistive current.

The space-charge-limited current density is given by

$$\begin{aligned} J_{SCL} &= \frac{9}{8} \mu \epsilon \frac{V^2}{L^3} \\ &= 1.47 \times 10^{-9} \frac{V^2}{L^3} \text{ A/cm}^2 \text{ for silicon} \end{aligned} \tag{25}$$

The power dissipation for some 1 mm thick, 10 kV devices with differing lengths and widths but with a constant heat sink area of 25 cm^2 are given in Tables 10 and 11.

TABLE 10

POWER DISSIPATION IN A LATERAL $(DI)^2$ DEVICE
WITH SILICON RESISTIVITY = 5 E 4 OHM-CM

L (cm)	W (cm)	CURRENT AREA (cm^2)	INJECTED J (A/cm^2)	INJECTED I (mA)	OHMIC I (mA)	POWER (W)	POWER DENSITY (W/cm^2)
1.0	25.0	2.50	147.0	367.0	500	8670	346.0
2.0	12.5	1.25	18.4	23.0	125	1480	59.2
2.5	10.0	1.00	9.4	9.4	80	894	35.8
2.8	8.93	0.893	6.7	6.0	64	697	27.9
3.0	8.33	0.833	5.4	4.5	55.0	600	24.0
3.2	7.81	0.781	4.5	3.5	48.8	523	20.9
3.3	7.57	0.757	4.1	3.1	45.9	490	19.6

TABLE 11

POWER DISSIPATION IN A LATERAL $(DI)^2$ DEVICE
WITH INFINITE SILICON RESISTIVITY

L (cm)	W (cm)	CURRENT AREA (cm^2)	INJECTED J (A/cm^2)	INJECTED I (mA)	OHMIC I (mA)	POWER (W)	POWER DENSITY (W/cm^2)
1.0	25.0	2.50	147.0	367.0	0	3670	147.0
1.5	16.7	1.67	43.5	72.7	0	727	29.1
1.6	15.6	1.56	35.9	56.0	0	560	22.4
1.7	14.7	1.47	30.0	44.0	0	440	17.6

The significance of the numbers in the last column, dissipated power divided by heat sink area, lies in the fact that the thermal impedance between a semiconductor power device and its heat sink is, in optimum cases, approximately 1.0°C cm^2/W.[d] Therefore, the power density in W/cm^2 is numerically equal to the difference in temperature between the device and its heat sink. From these numbers we see that a $(DI)^2$ device designed for 10 kV threshold voltage should be a lateral device with an anode-cathode distance of approximately 1.0 cm or more.

4.2 SHIEH'S MODELLED DEVICES

In his Ph.D. dissertation, Shieh used computer simulation to model some of the parameters of $(DI)^2$ switches. The dependence of these parameters was calculated as a function of several material properties, having assumed default values for data such as the electron and hole trapping properties of the gold impurity and the electron and hole mobilities in gold-doped silicon. Although he did not explicitly calculate the power levels and the ratios of threshold voltage to holding voltage, it is possible to infer from his published graphs what these values would be. The following tables are based upon such inferences.

The tabulated values are:

threshold voltage, V_t, in volts
threshold current density, J_t, in amps per square centimeter
holding voltage, V_h, in volts
holding current density, J_h, in amps per square centimeter
the ratio of threshold voltage to holding voltage, V_t/V_h
dissipated power at the threshold, P_t, in watts
dissipated power at holding, P_h, in watts
the power density for threshold P_t/V in watts per cc
the power density for holding P_h/V in watts per cc

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d. Ghandi, p. 8

These latter two values are important for considerations of removing heat from the device. The referenced figure numbers refer to graphs in Shieh's dissertation.

In order for a switch to be able to continuously hold off voltage in the off state, it must be capable of dissipating the off-state power. If we assume a planar device made in silicon which is 10 mils (2.54 E -2 cm) thick and in contact with a heat sink in which the thermal impedance is 1.0°C per watt per square centimeter, and if we assume that a 100 degree rise in device temperature is tolerable, then the maximum off-state power density (P_t/V) which can be tolerated is 4000 watts per cc of device. Few of the devices modeled by Shieh have an off-state power density this low.

In order for the switch to be efficient, it should have a high threshold voltage to holding voltage ratio (V_t/V_h). An examination of Tables 12 through 20 indicates the following for the range of material parameters and designs modeled by Shieh:

As device length increases, V_t/V_h increases, but Pt/V increases.

As the gold concentration increases, P_t/V increases and V_tV_h decreases.

As phosphorus concentration increases with Au = 1 E 15, P_t/V is approximately constant and V_t/V_h increases.

As phosphorus concentration increases with Au = 2 E 15, P_t/V decreases and V_t/V_h increases.

As phosphorus concentration increases with Au = 2 x the phosphorus concentration, P_t/V increases but V_t/V_h increases.

As COEA increases, P_t/V increases and V_t/V_h increases.

From the above, it appears that it would be beneficial to simulate the properties of short devices with higher phosphorus (and gold) concentrations than were considered by Shieh.

TABLE 12

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figure 4.4)

As a function of length L (in μm), with N_D = 5 E 14, Au = 1 E 15

L	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
200	50	4	15	80	3.3	200	1.2E3	1.0E4	6.0E4
300	160	5	35	130	4.6	800	4.6E3	2.7E4	1.5E5
400	350	6	50	200	7.0	2100	1.0E4	5.3E4	2.5E5
500	600	6	130	230	4.6	3600	3.0E4	7.2E4	1.5E6

TABLE 13

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.6a and 4.6b)

As a function of gold concentration with N_D = 5 E 14 and L = 100 μm

Au	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
8.0E14	4.0	1.3	2.5	25	1.6	5.2	62.5	520	6.3E3
1.2E15	7.5	2.0	4.0	55	1.9	15.0	220	1.5E3	2.2E4
1.6E15	11.0	4.0	6.0	85	1.8	44.0	510	4.4E3	5.1E4
2.0E15	15.0	6.2	8.0	130	1.9	93.0	1.0E3	9.3E3	1.0E5
2.4E15	19.5	10.0	12.5	190	1.6	195.0	2.4E3	2.0E4	2.4E5
2.8E15	24.5	14.0	15.5	230	1.6	343.0	3.6E3	3.4E4	3.6E5
3.0E15	27.0	16.0	18.0	250	1.5	432.0	4.5E3	4.3E4	4.5E5

TABLE 14

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.7a and 4.7b)

As a function of gold concentration with N_D = 5 E 14 and L = 200 μm

Au	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
8.0E14	44	3.0	12	50	3.7	132	600	6.6E3	3.0E4
1.0E15	56	4.5	16	75	3.5	252	1.2E3	1.3E4	6.0E4
1.2E15	66	6.0	20	100	3.3	395	2.0E3	2.0E4	1.0E5
1.4E15	78	8.0	25	150	3.1	624	3.8E3	3.1E4	1.9E5
1.6E15	90	9.0	32	200	2.8	810	6.4E3	4.1E4	3.2E5
1.8E15	102	12.0	39	250	2.6	1.2E3	9.8E3	6.1E4	4.9E5
2.0E15	112	14.0	46	300	2.4	1.6E3	1.4E4	7.8E4	6.9E5
2.2E15	126	16.0	60	390	2.1	2.0E3	2.3E4	1.EE5	1.2E6
2.4E15	140	19.0	75	420	1.9	2.7E3	3.2E4	1.3E5	1.6E6
2.6E15	154	20.0	92	520	1.7	3.1E3	4.8E4	1.5E5	2.4E6
2.8E15	168	25.0	109	610	1.5	4.2E3	6.7E4	2.1E5	3.3E6

TABLE 15

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.8a and 4.8c)

As a function of gold concentration with N_D = 5 E 14 and L = 300 μm

Au	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
8.0E14	140	4.5	30	100	4.7	630	3.0E3	2.1E4	1.0E5
1.0E15	170	5.5	35	145	4.9	935	5.1E3	3.1E4	1.7E5
1.2E15	195	6.5	50	200	3.9	1.3E3	1.0E4	4.3E4	3.3E5
1.4E15	220	8.0	70	270	3.1	1.8E3	1.9E4	6.0E4	6.3E5
1.6E15	245	9.0	85	400	2.9	2.2E3	3.4E4	7.3E4	1.1E6
1.8E15	270	10.0	110	500	2.5	2.7E3	5.5E4	9.0E4	1.8E6
2.0E15	295	12.0	135	600	2.2	3.5E3	8.1E4	1.2E5	2.7E6
2.2E15	325	14.0	---	---	---	4.6E3	-----	1.5E5	
2.4E15	365	15.0	---	---	---	5.5E3	-----	1.8E5	
2.6E15	405	17.0	---	---	---	6.9E3	-----	2.3E5	
2.8E15	445	20.0	---	---	---	8.9E3	-----	3.0E5	
3.0E15	485	22.0	---	---	---	1.1E4	-----	3.6E5	

TABLE 16

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.9a and 4.9c)

As a function of N_D with Au = 1 E 15 and L = 200 μm

N_D	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
5.0E13	32	10.0	29	75	1.1	320	2.2E3	1.6E4	1.1E5
6.0E13	32	9.0	28	70	1.1	288	2.0E3	1.4E4	9.8E4
8.0E13	32	8.5	27	65	1.2	272	1.8E3	1.4E4	8.8E4
1.0E14	31	7.5	26	60	1.2	233	1.6E3	1.2E4	7.8E4
2.0E14	35	5.0	22	63	1.6	175	1.4E3	8.8E3	6.9E4
4.0E14	48	4.5	17	78	2.8	216	1.3E3	1.1E4	6.6E4
6.0E14	61	4.5	15	88	4.1	275	1.3E3	1.4E4	6.6E4
8.0E14	69	4.2	14	100	4.9	290	1.4E3	1.5E4	7.0E4

TABLE 17

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.10a and 4.10c)

As a function of N_D with Au = 2 E 15 and L = 200 μm

N_D	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
5.0E13	102	40	100	250	1.0	4.1E3	2.5E4	2.0E5	1.3E6
6.0E13	101	38	96	245	1.1	3.8E3	2.4E4	1.9E5	1.2E6
8.0E13	100	37	90	230	1.1	3.7E3	2.1E4	1.9E5	1.1E6
1.0E14	98	35	86	220	1.1	3.4E3	1.9E4	1.7E5	9.5E5
2.0E14	98	27	70	220	1.4	2.7E3	1.5E4	1.3E5	7.5E5
4.0E14	106	15	52	240	2.0	1.6E3	1.5E4	8.0E4	7.5E5
6.0E14	121	11	46	260	2.6	1.3E3	1.3E4	6.7E4	6.5E5
8.0E14	136	9	42	350	3.2	1.2E3	1.5E4	6.1E4	7.5E5
1.0E15	154	8	39	370	4.0	1.2E3	1.4E4	6.2E4	7.0E5
1.5E15	201	6	34	420	5.9	1.2E3	1.4E4	6.1E4	7.0E5
1.8E15	194	6	32	500	6.1	1.2E3	1.6E4	5.8E4	8.0E5

TABLE 20

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.14a and 4.14b)

As a function of COEA, the gold concentration gradient, with COEB = 1 E 15 and L = 300 μm. N_D is 5 E 14. The gold concentration at the anode is (1 - COEA)xCOEB; at the cathode, it is (1 + COEA)xCOEB.

COEA	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
0.0	160	5.5	33	133	4.8	880	4.4E3	2.9E4	1.5E5
0.1	210	4.5	32	135	6.6	950	4.3E3	3.2E4	1.4E5
0.2	275	4.0	32	139	8.6	1.1E3	4.4E3	3.7E4	1.5E
0.3	350	3.5	31	142	11.0	1.2E3	4.4E3	4.0E4	1.5E
0.4	450	3.0	31	146	15.0	1.4E3	4.5E3	4.7E4	1.5E5
0.5	590	3.0	30	154	20.0	1.8E3	4.6E3	6.0E4	1.5E5
0.6	740	2.5	29	160	26.0	1.9E3	4.6E3	6.3E4	1.5E5

4.3 LOWER VOLTAGE DEVICES

It is obvious that power dissipation in high-voltage $(DI)^2$ devices must be considered in their design. The following section attempts to present reasonable voltage levels for practical $(DI)^2$ designs.

4.3.1 Silicon Devices

It has been shown that power dissipation in high-voltage devices is a serious problem. A fundamental consideration in the application of $(DI)^2$ devices to high-power circuits is the significant power dissipation in the OFF state. The power generated by "leakage currents" must be removed in order to prevent the device from overheating. The following describes the limitations that off-state power dissipation impose upon device design and operation.

A typical thermal impedance between the high-voltage junction of a high-power silicon thyristor and its copper heat sink is 1.0°C cm^2/W. (This thermal impedance is equivalent to a 4.0 cm thickness of copper, a 1.3 cm thickness of silicon, or a 0.4 cm thickness of GaAs, so it can be

TABLE 18

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.11a and 4.11c)

As a function of N_D with Au = 2 x N_D and L = 200 μm

N_D	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
3.2E14	25	1.4	10	30	2.5	35	300	1.8E3	1.5E4
4.0E14	38	2.2	13	43	2.9	84	559	4.2E3	2.8E4
5.2E14	58	4.0	16	82	3.9	232	1.3E3	1.2E4	6.6E4
6.0E14	72	5.0	20	120	3.6	360	2.4E3	1.8E4	1.2E5
7.2E14	95	6.1	25	200	3.8	580	5.0E3	2.9E4	2.5E5
8.0E14	112	7.0	29	250	3.9	784	7.3E3	3.9E4	3.6E5
9.2E14	136	7.9	34	300	4.0	1.1E3	1.0E4	5.4E4	5.1E5
1.0E15	155	8.0	38	360	4.1	1.2E3	1.3E4	6.2E4	6.9E5

TABLE 19

COMPUTER-SIMULATED POWER DISSIPATION FACTORS
(Figures 4.12a and 4.12c)

As a function of COEA, the gold concentration gradient, with COEB = 1 E 15 and L = 200 μm. N_D is 5 E 14. The gold concentration at the anode is (1 - COEA)xCOEB at the cathode, it is (1 + COEA)xCOEB.

COEA	V_t	J_t	V_h	J_h	V_t/V_h	P_t	P_h	P_t/V	P_h/V
-0.6	17	8.5	15	57	1.1	145	8.5E2	7.2E3	4.3E4
-0.4	24	4.5	15	69	1.6	108	1.0E3	5.4E3	5.2E4
-0.2	30	4.5	15	79	2.0	135	1.2E3	6.8E3	5.9E4
0.0	55	4.5	15	82	3.7	248	1.2E3	1.2E4	6.2E4
0.2	88	4.0	15	88	5.9	352	1.3E3	1.8E4	6.6E4
0.4	130	3.0	15	94	8.7	390	1.4E3	2.0E4	7.1E4
0.6	170	2.5	15	96	11.3	425	1.4E3	2.1E4	7.2E4
0.8	202	2.0	15	100	13.5	404	1.5E3	2.0E4	7.5E4
1.0	193	2.0	15	104	12.9	386	1.6E3	1.9E4	7.8E4

appreciated that it is the dominant thermal impedance in common device/package designs.)

If we assume that we can attain the same thermal impedance in a $(DI)^2$ device and package, we can calculate the effects of self-heating for various device configurations and conditions.

Power dissipation in a $(DI)^2$ device in the OFF state is caused by two "leakage current" components — resistive current and space-charge-limited (SCL) current. In general, resistive current will dominate in low-resistivity devices and at low voltages; SCL current will dominate in high-resistivity devices and at high voltages. In the following, we consider only very high-resistivity devices in order to minimize off-state power loss due to resistive currents. Under these conditions, the SCL current is the limiting parameter at high voltages.

As an example, consider the silicon $(DI)^2$ device in Figure 14. Its thickness, t, is 0.1 cm (0.04 inches); its width, W, is 1.0 cm; and its length, L (anode to cathode distance) is 0.5 cm. At an applied voltage V, the resistive current is

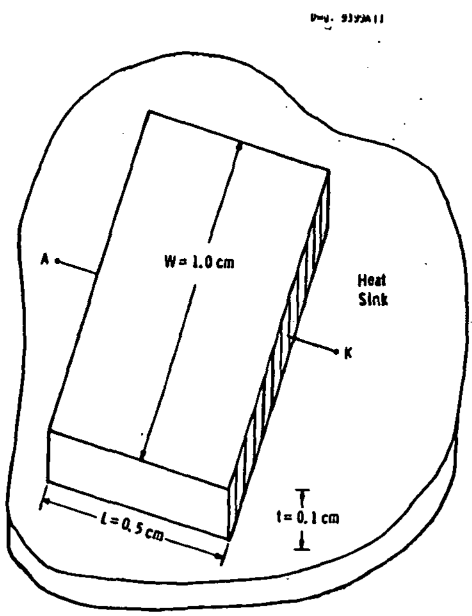

Figure 14. Example of a $(DI)^2$ diode.

$$I_{RES} = \frac{V}{\rho} \frac{wt}{L} \tag{9}$$

where ρ is the bulk resistivity of the silicon. The SCL current is

$$I_{SCL} = \frac{9}{8} \epsilon \mu wt \frac{V^2}{L^3} \tag{10}$$

where ϵ and μ are the permittivity and electron mobility in silicon (1.0 E-12 F/cm and 1500 cm^2/V sec).

The maximum bulk resistivity obtainable in silicon at room temperature is 3 E+5 ohm cm. Assuming this maximum resistivity for the device in Figure 14, the leakage currents and power dissipation for several voltages are shown in Table 21.

TABLE 21

LEAKAGE CURRENTS AND POWER DISSIPATION IN A SILICON 0.5 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area ($Watts/cm^2$)
100	6.67 E-5	1.35 E-5	8.02 E-5	8.02 E-3	1.60 E-2
200	1.33 E-4	5.40 E-5	1.87 E-5	3.74 E-2	7.48 E-2
400	2.67 E-4	2.15 E-4	4.83 E-4	1.93 E-1	3.86 E-1
800	5.33 E-4	8.64 E-4	1.40 E-3	1.12	2.24
1600	1.07 E-3	3.46 E-3	4.53 E-3	7.24	14.5
3200	2.13 E-3	1.38 E-2	1.60 E-2	51.1	102

(The heat sink area is 0.5 cm^2.)

Since the thermal impedance between the device and the heat sink was taken to be 1.0°C cm^2/W, the numbers in the last column are equal to the temperature difference between the device and its heat sink. Since a 100°C rise in device temperature might seem to be a reasonable upper limit, calculations were not done for applied voltages that would cause heating much above that temperature. A decrease in the thickness of the device would decrease the power dissipation (and therefore decrease self-heating) since the leakage currents scale inversely as the thickness. An increase in the anode-cathode spacing of the device would provide two power dissipation benefits at a given voltage — (1) more heat sink area would be available for device cooling; (2) less power would be dissipated since the resistive current scales inversely as the device length, and the SCL current scales inversely as the cube of the device length. Changing the width of the device would have no effect on self-heating since both the heat sink area and the leakage currents scale directly with the width.

Similar calculations were made for silicon devices with anode-cathode spacings of 0.1, 0.2, and 1.0 cm. The data are shown in Tables 22 through 24.

4.3.2 GaAs Devices

The resistive current component can be reduced by the use of a wide bandgap material such as GaAs. The maximum resistivity obtainable in GaAs is 1 E +8 ohm cm. Devices made in this high-resistivity material would have negligible resistive leakage currents, but the SCL currents would be higher than those of silicon because of the higher electron mobility (8500 cm^2/V sec) of GaAs. Calculated power dissipation data for GaAs devices with anode-cathode spacing of 0.1, 0.2, 0.5, and 2.0 cm are given in Tables 25 through 28.

Some of these data points in the regions of interest are plotted in Figure 15. This plot illustrates the regions for which practical $(DI)^2$ devices might be designed.

TABLE 22

LEAKAGE CURRENTS AND POWER DISSIPATION
IN A SILICON 0.1 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area ($Watts/cm^2$)
10	3.33 E-5	1.69 E-5	5.02 E-5	5.02 E-4	5.02 E-3
20	6.67 E-5	6.75 E-5	1.34 E-4	2.68 E-3	2.68 E-2
40	1.33 E-4	2.70 E-4	4.03 E-4	1.61 E-2	1.61 E-1
80	2.67 E-4	1.08 E-4	1.35 E-3	1.08 E-1	1.08
160	5.33 E-4	4.32 E-3	4.85 E-3	7.76 E-1	7.76
320	1.07 E-3	1.73 E-2	1.84 E-2	5.88	58.8
640	2.13 E-3	6.92 E-2	7.14 E-2	45.7	457

(The heat sink area is 0.1 cm^2.)

TABLE 23

LEAKAGE CURRENTS AND POWER DISSIPATION
IN A SILICON 0.2 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area ($Watts/cm^2$)
100	1.67 E-4	2.11 E-4	3.78 E-4	3.78 E-2	1.89 E-1
200	3.34 E-4	8.44 E-4	1.18 E-3	2.36 E-1	1.18
400	6.68 E-4	3.38 E-3	4.04 E-3	1.62	8.09
800	1.34 E-3	1.35 E-2	1.48 E-2	11.9	59.4
1600	2.67 E-3	5.40 E-2	5.67 E-2	90.7	453

(The heat sink area is 0.2 cm^2.)

TABLE 24

LEAKAGE CURRENTS AND POWER DISSIPATION IN A SILICON 1.0 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area (Watts/cm^2)
100	3.33 E-5	1.69 E-6	3.50 E-5	3.50 E-3	3.50 E-3
200	6.67 E-5	6.76 E-6	7.35 E-5	1.47 E-2	1.47 E-2
400	1.33 E-4	2.70 E-5	1.60 E-4	6.40 E-2	6.40 E-2
800	2.67 E-4	1.08 E-4	3.75 E-4	3.00 E-1	3.00 E-1
1600	5.33 E-4	4.33 E-4	9.66 E-4	1.55	1.55
3200	1.07 E-3	1.73 E-3	2.80 E-3	8.96	8.96
6400	2.13 E-3	6.92 E-3	0.05 E-3	57.9	57.9
10000	3.33 E-3	1.69 E-2	2.02 E-2	202	202

(The heat sink area is 1.0 cm^2.)

TABLE 25

LEAKAGE CURRENTS AND POWER DISSIPATION IN A GaAs 0.1 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area (Watts/cm^2)
10	1.00 E-7	1.11 E-4	1.11 E-4	1.11 E-3	1.11 E-2
20	2.00 E-7	4.44 E-4	4.44 E-4	8.88 E-3	8.88 E-2
40	4.00 E-7	1.78 E-3	1.78 E-3	7.12 E-2	7.12 E-1
80	8.00 E-7	7.10 E-3	7.10 E-3	5.68 E-1	5.68
160	1.60 E-6	2.84 E-2	2.84 E-2	4.54	45.4
320	3.20 E-6	1.14 E-1	1.14 E-1	36.4	364

(The heat sink area is 0.1 cm^2.)

TABLE 26

LEAKAGE CURRENTS AND POWER DISSIPATION IN A GaAs 0.2 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area ($Watts/cm^2$)
100	5.00 E-7	1.39 E-3	1.39 E-3	1.39 E-1	6.94 E-1
200	1.00 E-6	5.55 E-3	5.55 E-3	1.11	5.55
400	2.00 E-6	2.22 E-2	2.22 E-2	8.88	44.4
800	4.00 E-6	8.88 E-2	8.88 E-2	71.0	355

(The heat sink area is 0.2 cm^2.)

TABLE 27

LEAKAGE CURRENTS AND POWER DISSIPATION IN A GaAs 0.5 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area ($Watts/cm^2$)
100	2.00 E-7	8.87 E-5	8.89 E-5	8.89 E-3	1.78 E-2
200	4.00 E-7	3.55 E-4	3.55 E-4	7.10 E-2	1.42 E-1
400	8.00 E-7	1.42 E-3	1.42 E-3	5.68 E-1	1.14
800	1.6 E-6	5.68 E-3	5.68 E-3	4.54	9.08
1600	3.2 E-6	2.27 E-2	2.27 E-2	36.3	72.7
3200	6.4 E-6	9.08 E-2	9.08 E-2	291	581

(The heat sink area is 0.5 cm^2.)

TABLE 28

LEAKAGE CURRENTS AND POWER DISSIPATION IN A GaAs 1.0 cm LONG $(DI)^2$ DEVICE

Applied Voltage (Volts)	Resistive Current (Amperes)	SCL Current (Amperes)	Total Current (Amperes)	Power (Watts)	Power/Area (Watts/cm^2)
100	1.00 E-7	1.11 E-5	1.12 E-5	1.12 E-3	1.12 E-3
200	2.00 E-7	4.44 E-5	4.46 E-5	8.92 E-3	8.92 E-3
400	4.00 E-7	1.78 E-4	1.78 E-4	7.12 E-2	7.12 E-2
800	8.00 E-7	7.10 E-4	7.11 E-4	5.69 E-1	5.69 E-1
1600	1.60 E-6	2.84 E-3	2.84 E-3	4.55	4.55
3200	3.20 E-6	1.14 E-2	1.14 E-2	36.4	36.4
6400	6.40 E-6	4.55 E-2	4.55 E-2	291	291
10000	1.00 E-5	1.11 E-1	1.11 E-1	1110	1110

(The heat sink area is 1.0 cm^2.)

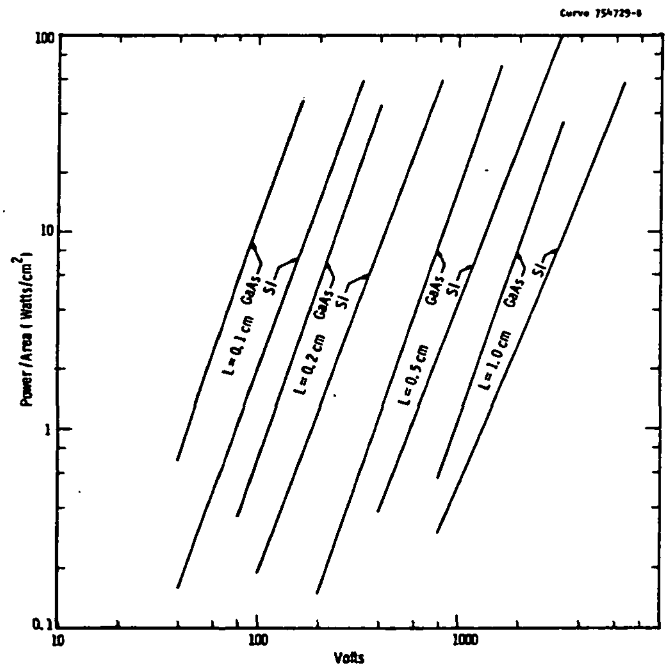

Figure 15. Off-state power dissipation per square centimeter for silicon and gallium arsenide $(DI)^2$ diodes for various anode-cathode spacings as a function of voltage.

5. DEVICE PROCESSING

5.1 STANDARD PROCESS

The standard processing conditions used to fabricate the planar annular $(DI)^2$ devices is outlined below.

1. Thermal oxidation to mask boron diffusion. Oxide thickness to be 4600 Å. 1100°C, 35 minutes, wet oxygen.
2. Photolithography, mask 1. Etch through masking oxide.
3. First diffusion pre-dep. 980°C, boron tribromide, 40 minutes source, 40 minutes soak. Target 15 ohms/square.
4. First diffusion drive and grow oxide to mask second diffusion. 1100°C, 40 minutes dry oxygen, 11 minutes wet oxygen. Target oxide thickness 2470 Å.
5. Photolithography, mask 2. Etch through masking oxide.
6. Second diffusion pre-dep. 1050°C, phosphorus oxychloride, 25 minute source, 25 minute soak. Target 15 ohms/square.
7. Second diffusion drive and oxidation. 1100°C, 14 minutes wet oxygen, 40 minutes dry oxygen. Target junction depths 5.0 μm.
8. Photolithography, mask 3. Etch windows for MOS gate oxide growth.
9. Oxidation to grow gate oxide. 1000°C, 10 minutes wet oxygen, 20 minutes dry oxygen. Target oxide thickness of 1000 Å.
10. Lap backs of wafers to remove diffusions and thin wafers. Target to remove at least 10 μm of silicon.
11. Gold diffusion of wafers. Various conditions and targets.
12. Photolithography, mask 4. Etch contacts to emitters, collectors, and injection gates.

13. Metallization, aluminum, vacuum evaporated. Target 4 μm of aluminum.
14. Photolithography, mask 5. Define metal pattern.
15. Reactive ion etch aluminum.
16. Wet etch aluminum residues.
17. Sinter metal. 450°C, 30 minutes in hydrogen.

5.2 GOLD DOPING

Gold, as an element which forms the deep levels in silicon, is the most studied and best understood of the deep-level dopants. It is for that reason, and the fact that gold is convenient to use, that it was used in this investigation.

5.2.1 Previous Methods

Methods of introducing the gold into silicon were investigated in previous programs. The most widely used method (as employed for lifetime killing in fast switching power devices and integrated circuits) has been to coat the bare silicon surface with a thin film of gold deposited either by vacuum evaporation or by a wet chemical displacement reaction, heat the wafers for a specified period of time at a particular temperature in order to diffuse the gold into the silicon wafer, and then remove unreacted gold from the wafer surface. This method causes a molten silicon-gold eutectic to form at the gold-silicon interface as gold diffuses into the silicon wafer. Subsequent removal of the gold-silicon system remaining on the wafer surface is often difficult, leaving a stained surface of uncertain composition.

This method has been found useful in creating fast-switching devices in which the desired gold concentration is on the order of 1 E 12 to 1 E 14 per cubic centimeter, and where it is not required that the gold be uniformly distributed throughout the silicon wafer. This method was used in previous $(DI)^2$ investigations but was found to be difficult to control.

A new method was investigated in a previous $(DI)^2$ program in which the wafer to be gold doped was placed in a furnace with an inert atmosphere and in close proximity to another "gold-source" silicon wafer that had been previously coated with gold. This method appeared to give better control over the gold-doping process but was very sensitive to the previous history of the gold-source wafer. All methods of gold doping of silicon have been based mostly upon empirical data and have not always been satisfactory.

5.2.2 Kickout Mechanism

A series of papers published in 1980-1984 [1-12] has clarified the mechanism of gold diffusion in silicon and has enabled a more rational approach to the process. This mechanism has implications for the processing of gold-doped $(DI)^2$ devices.

The qualitative characteristics of gold diffusion in silicon are now believed to be as described below. In this description, X_i represents an atom in an interstitial site, X_s represents an atom in a substitutional site, X^{eq} represents the equilibrium concentration of X, I is a silicon interstitial, and V is a silicon vacancy.

The correct qualitative description of the silicon-gold system is now believed to be:

a) The diffusivity of interstitial gold is much higher than the diffusivity of substitutional gold.

b) The solid solubility of substitutional gold is much greater [1-8,10-12] or less [9] than the solubility of interstitial gold.

c) Interchange between gold in substitutional sites and gold in interstitial sites proceeds through a "kickout" mechanism involving a silicon self-interstitial,

$$Au_i = Au_s + I \quad (26)$$

instead of by a dissociative mechanism involving a silicon vacancy as had been previously believed:

$$Au_i + V = Au_s \tag{27}$$

d) Only the gold in substitutional sites is electrically active.

The diffusion of gold into defect-free silicon (no internal sources or sinks of self interstitials) can then be described as follows:

1) Gold (presumed to be from an infinite source such as an evaporated film on the silicon surface) diffuses rapidly throughout the crystal; and the equilibrium of equation (26) is established everywhere in the crystal. At this early stage, the concentration of substitutional gold is quite low. Silicon interstitials are generated according to equation (26), making the concentration of silicon self-interstitials much higher than its equilibrium concentration and keeping the reaction (26) shifted strongly toward the left.
2) The silicon interstitials begin to diffuse rapidly to the silicon surfaces where they are annihiliated; this produces a concentration profile of interstitials which is initially high in the interior of the wafer and low at the wafer edges. Because of the low concentration of silicon interstitials at the surface, reaction (26) proceeds toward the right in these regions, and the substitutional gold concentration approaches its solid solubility limit. In the interior of the wafer, where the silicon interstitial concentration is still high, the concentration of Au_s remains low, giving rise to the well-known "tip-up" effect.

3) At later times, as more gold continues to diffuse interstitially into the wafer, and the silicon interstitials produced by reaction (26) continue to diffuse out, the concentration of Au_s in the center of the wafer increases, approaching the solid solubility limit.

In summary, the incorporation of gold into substitutional sites is controlled by the diffusion of silicon interstitials. As a consequence, the gold concentration profile is symmetrical about the center of the wafer, and the shape of the profile does not depend upon whether the gold is diffused from one side of the wafer or from both sides of the wafer simultaneously.

Stolwijk et al. [10,12] used neutron activation analysis and mechanical sectioning to deduce the mechanism described above. By fitting their data to equations predicted by the "kick-out" mechanism, they were able to derive the solid solubility limit of substitutional gold and derived an effective diffusivity, D^*, defined as

$$D^* = (C_I^{eq} D_I)/C_s^{eq} \qquad (28)$$

The values of these parameters are given in Table 29 and are plotted as a function of reciprocal temperature in Figure 16.

TABLE 29

CALCULATED VALUES OF D^* AND C_s^{eq}

Temperature (°C)	D^* (cm^2/sec)	C_s^{eq} (cm^{-3})
800	1.55 E -12	5.8 E 14
900	2.04 E -11	3.4 E 15
1000	2.23 E -10	1.5 E 16
1098	1.55 E -09	4.8 E 16

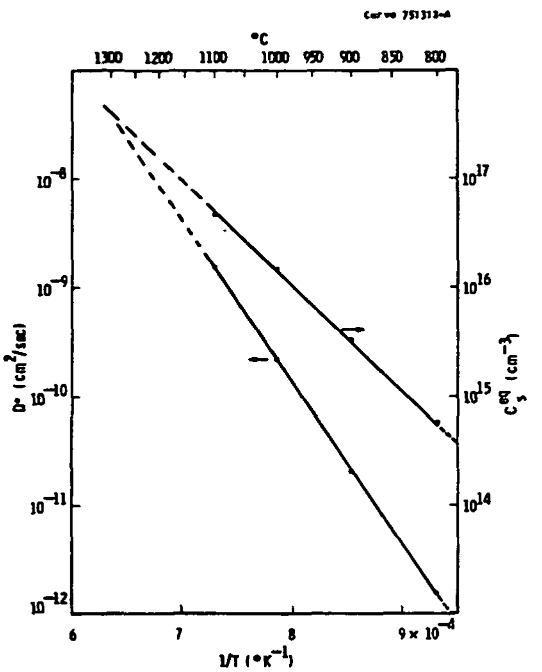

Figure 16. Values of D^* and C_s^{eq} (from Ref. 10) plotted against reciprocal temperature.

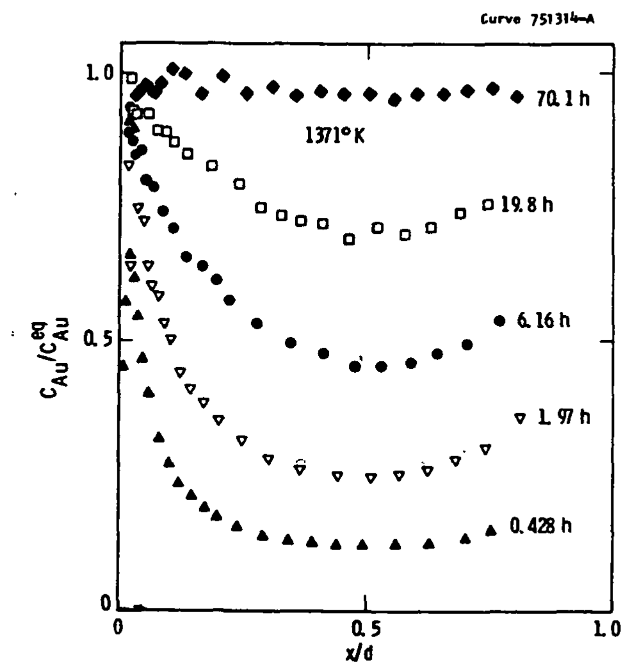

Figure 17. Penetration profiles of gold into silicon (from Ref. 12).

A representative plot of some data due to [10] is shown in Figure 17.

The significance of D^* is that the ratio of gold concentration in the center of the wafer to the concentration at the wafer surface (which is nearly the solid solubility limit) is given by

$$\frac{C_s}{C_s^{eq}} = \frac{2}{d} \quad (\pi D^* t)^{1/2} \qquad (29)$$

where d is the thickness of the wafer and t is the time of diffusion.

The ratio of substitutional gold at distance x into the wafer to the concentration at the wafer center (where x = d/2), C_s^m, is given by

$$\text{erf} \left[\ell n \left(\frac{C_s}{C_s^m} \right)^{1/2} \right] \frac{\frac{d}{2-x}}{\frac{d}{2}} \qquad (30)$$

5.2.2.1 Implications for Light Gold Doping of Silicon Wafers

If the above mechanism, equations, and values are correct, then it should be possible to calculate the conditions necessary in order to obtain a uniform concentration of gold. For example, in order to obtain a light gold doping (e.g., 6 E 14 cm^{-3}) in a silicon wafer of 15 mil (3.81 E -2 cm) thickness, it would be necessary to perform the diffusion at the temperature (800°C) where 6 E 14 is the solid solubility, and the time required for the substitutional gold concentration in the wafer center to reach 80% of the gold concentration at the wafer surfaces would be 4.7 E 7 seconds. It would be difficult to introduce a small amount of gold as a "pre-dep" step using an evaporated gold source and drive the gold at a higher temperature because of the residual high concentration of gold that would remain in the solidified gold-silicon eutectic region.

5.2.2.2 Heavy Gold Doping of Silicon Wafers

The situation for heavy gold doping is not so formidable. Calculation of the time required for the gold concentration in the center of the wafer to reach 80% of the concentration at the wafer surfaces, for various surface concentrations, is shown in Table 30.

It should be noted that, according to the experimental results of [1-12] and their interpretation of the gold diffusion mechanism, rapid quenching of silicon after gold diffusion is not necessary to freeze gold atoms into substitutional sites, although it can be presumed that very slow cooling of wafers might result in the undesirable precipitation of gold atoms as a second phase.

5.2.3 Properties of Gold

Calculations based upon assumed chemical and physical properties of the gold-silicon system at high temperatures indicate that controlled gold doping of silicon should be attainable by vapor transport of gold between a gold surface and a silicon wafer in close proximity in a furnace with an inert atmosphere, as was investigated in a previous program. The assumed mechanism for gold transport is that the stagnant atmosphere between the gold surface and the silicon wafer is saturated with gold at its vapor pressure, and that this causes the gold concentration at the silicon wafer surface to be near the solid solubility value.

Relevant properties of the system are listed in Table 31. It is quite possible that some of the values listed here are inaccurate, but any reasonable inaccuracy should have little effect upon the practicality of the method. In this table the vapor pressure of gold at several temperatures is listed. From the vapor pressure can be calculated the rate at which vaporized gold atoms would be leaving the gold surface. At equilibrium, these gold atoms would strike any other surface at the same rate. The solid solubility of gold in silicon is given for the same temperatures, as is the square root of the diffusion

TABLE 30

TIME REQUIRED TO OBTAIN NEARLY UNIFORM GOLD CONCENTRATION

T (°C)	C_s^{eq} (cm^{-3})	D^*	TIME REQUIRED
796	5 E 14	1.3 E -12	1.5 years
832	1 E 15	4.2 E -12	7 months
921	5 E 15	4.5 E -11	19 days
977	1 E 16	1.3 E -10	7 days
1097	5 E 16	1.5 E -09	14 hour
1160	1 E 17	4.4 E -09	4.7 hrs

TABLE 31

PROPERTIES OF THE GOLD/SILICON SYSTEM
GOLD MP = 1064°C At Wt = 197 DENSITY = 19.3 g/cm^3

Temp °C	Au Vapor Pressure (mm)	Atoms Striking/ Leaving Surface (cm^{-2}/sec)	Solid Solubility (cm^{-3})	$D^{1/2}$ ($\mu m/hr^{1/2}$)	$D^{1/2}$ ($cm/sec^{1/2}$)
900	2.0E-7	1.5E13	3E15	2E2	3.3E-4
950	1.0E-6	7.0E13	6E15	3E2	5.0E-4
1000	5.0E-6	3.5E14	1E16	4E2	6.7E-4
1050	2.0E-5	1.4E15	2E16	4E2	6.7E-4
1100	9.0E-5	6.1E15	3E16	5E2	8.3E-4
1150	2.0E-4	1.3E16	5E16	6E2	1.0E-3
1200	5.0E-4	3.3E16	7E16	8E2	1.3E-3
1250	1.0E-3	6.4E16	1E1	8E2	1.3E-3
1280	1.5E-3	9.5E16	1E17	9E2	1.5E-3
1300	2.0E-3	1.3E17	1E17	1E3	1.7E-3
1350	6.0E-3	3.7E17	9E16	1E3	1.7E-3
1380	9.0E-3	5.5E17	3E16	1E3	1.7E-3

constant of gold at those temperatures (this value is given in two different sets of units).

From these values, it is possible to calculate parameters for the gold doping process. The following example is given. To dope a 0.5 mm (19.7 mil) thick silicon wafer with 5 E 15 cm^{-3} gold requires 2.5 E 14 gold atoms per square centimeter of wafer area. At 950°C, the solid solubility of gold in silicon, C_s, is 6 E 15, and $D^{1/2}$ = 5 E - 4 $cm/sec^{1/2}$. The quantity of gold that would diffuse into the wafer in time, t, is given by diffusion theory as

$$Q\ (t) = \frac{2}{\sqrt{\pi}}\ (Dt)^{1/2}\ C_s \tag{31}$$

so the time required to diffuse that number of gold atoms into the silicon is given by

$$\sqrt{t} = \frac{\sqrt{\pi}\quad Q}{2\ C_s\ \sqrt{D}} = 74\ \sqrt{sec} \tag{32}$$

or

$$t = 5.45\ E\ 3\ sec = 91\ minutes \tag{33}$$

The "junction depth" is also given by diffusion theory and is equal to

$$X_j = (Dt)^{1/2} = 0.37\ mm \tag{34}$$

Some auxiliary calculations show that some implicit assumptions are valid. For example, the amount of gold that would be lost from the gold source and would be deposited on the silicon surface during this time is given by

$$N = (7\ E\ 13)(5.45\ E\ 3) = 3.82\ E\ 17\ \text{atoms/cm}^2$$
$$= 1.2\ E\ 4\ \text{gm/cm}^2 \quad (35)$$
$$= 644\ \text{Å/cm}^2$$

so we can be sure that the source of gold will not be depleted during the diffusion.

We also note that the number of gold atoms striking the silicon surface during this time (3.82 E 17) is much higher than the number of gold atoms entering the silicon (2.5 E 14), so we can be sure that the silicon surface remains saturated with gold, as is required by the diffusion equation.

As another example, if it is desired to gold dope an existing Pennsilco 10 ohm-cm (N_D = 5 E 14) silicon wafer which is 0.011 inches (or 0.28 mm) thick with sufficient gold that the gold concentration is equal to the donor concentration, 1.4 E 13 Au atoms/cm^2 is required. The calculated time for this diffusion would would be inconveniently short at 900°C, so we extrapolate data to 850° and estimate the vapor pressure of Au to be 5 E -8 mm, the solid solubility to be 1.5 E 15, $D^{1/2}$ to be 3 E -4 cm/$s^{1/2}$, and the atoms striking the surface to be 4 E 12/cm^2-sec. Then $t^{1/2}$ = 27.57 $s^{1/2}$ so t = 760 s = 12.7 minutes. The diffusion depth $(Dt)^{1/2}$ = .083 mm. The total Au atoms striking the surface during the process is 4 E 12 * 760 s = 3 E 15, which is much more than the amount of gold diffused into the silicon, so we can assume that the surface remained saturated.

The values of the parameters used in these calculations are plotted against reciprocal temperature in Figures 18 to 23. The calculated silicon resistivity as a function of donor density and gold concentration is from the data of Thurber et al.[e]

In order to minimize leakage currents in $(DI)^2$ devices, it is necessary to reduce the ohmic current as much as possible. This implies the necessity of doping the silicon to its maximum resistivity.

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e. Replotted from data of Thurber et al., NTIS AD-760 150, January 1978.

For example, consider a silicon wafer which is .020 inch (5 E -2 cm) thick and 2 ohm-cm n-type (2.5 E 15 phosphorus/cm^3). Gold doping this wafer to obtain the maximum resistivity requires a gold concentration of approximately 5 E 16 cm^3 (Figure 18). From Figure 19, it is seen that gold has this solid solubility in silicon at a temperature of 1440°K (1170°C). At this temperature, the vapor pressure of gold is approximately 2 E -4 mm (Figure 20), and gold vapor atoms at that pressure leave or strike a surface at a rate of 1.3 E 16 atoms/cm^2/sec (Figure 21). From Figure 22 it is seen that the diffusion constant of gold at that temperature is 1 E -6. The amount of gold that would then diffuse into the wafer during time, t, while the surface concentration remains constant at C_s is given by Equation (31). The value of this expression for a time of 60 sec is 4.4 E 14 /cm^2 for a surface concentration corresponding to the solid solubility of gold.

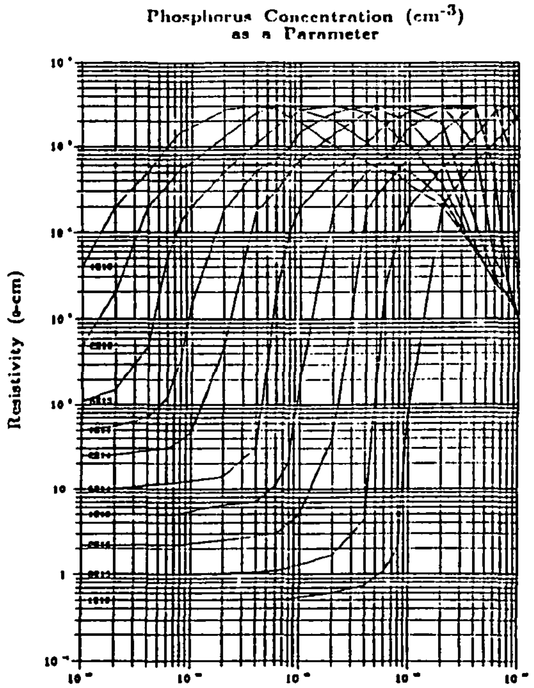

Figure 18. Calculated resistivity of silicon as a function of gold concentration with phosphorus concentration as a parameter.

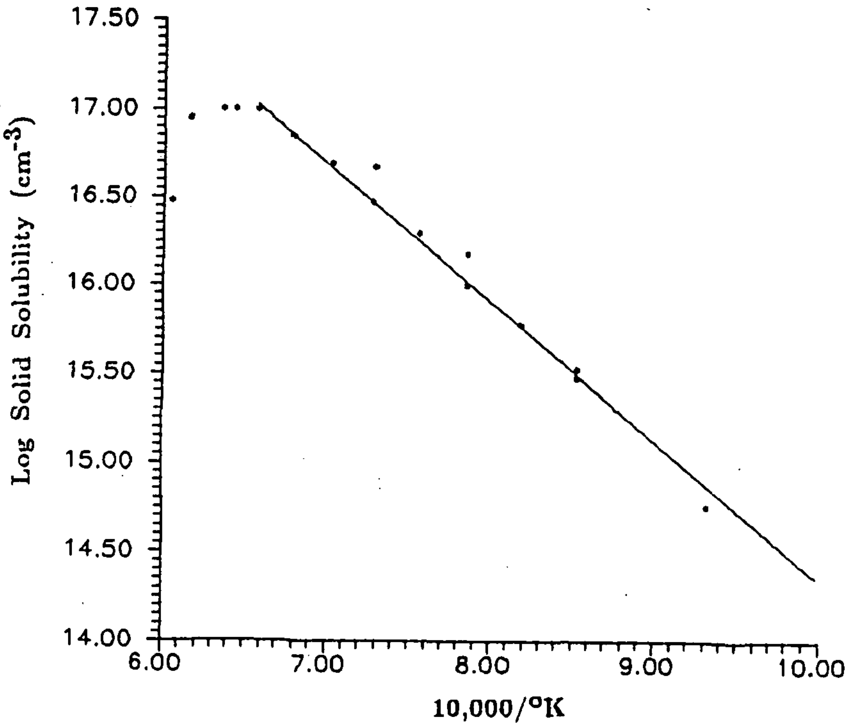

Figure 19. Arrhenius plot of the solubility of gold in silicon.

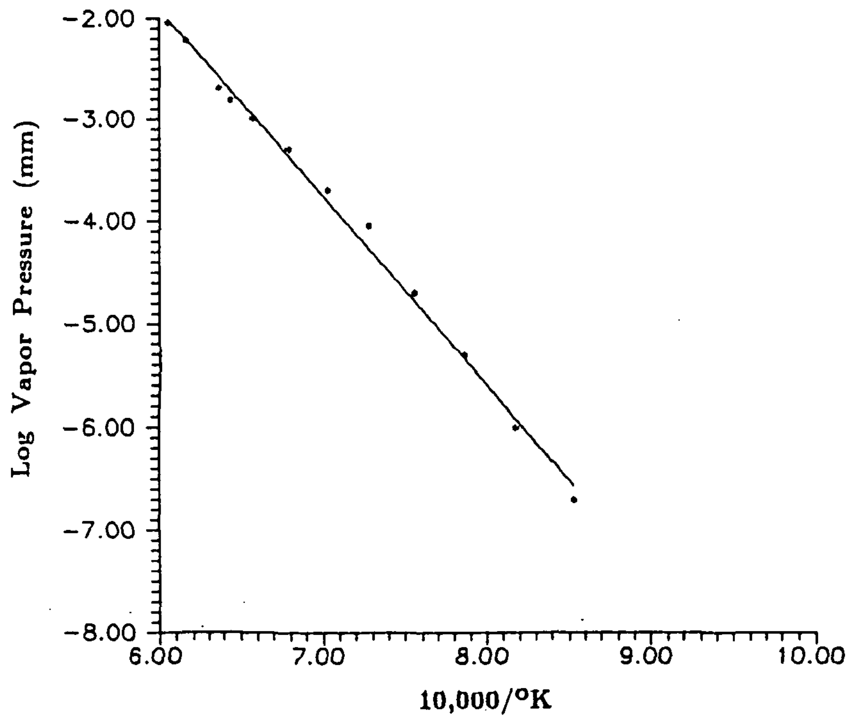

Figure 20. Arrhenius plot of the vapor pressure of gold.

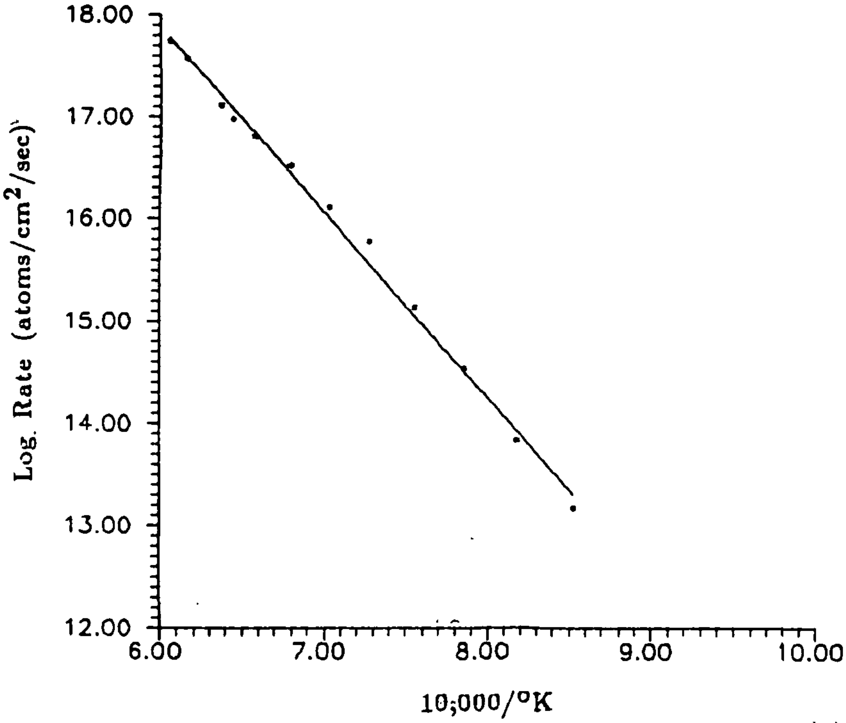

Figure 21. Arrhenius plot of the rate at which gold vapor atoms leave or strike a surface.

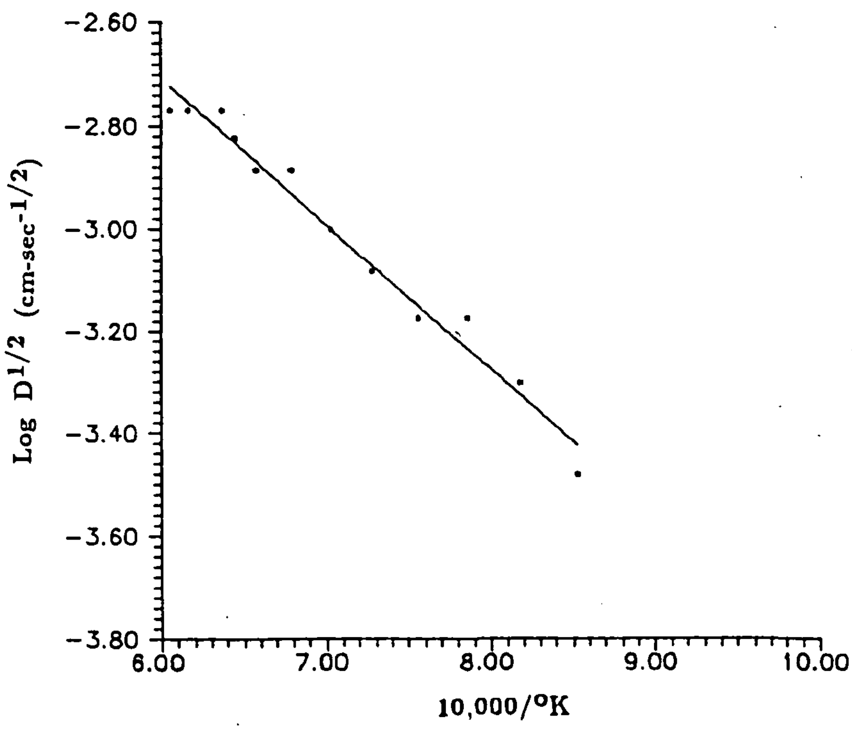

Figure 22. Arrhenius plot of the diffusion constant of gold in silicon.

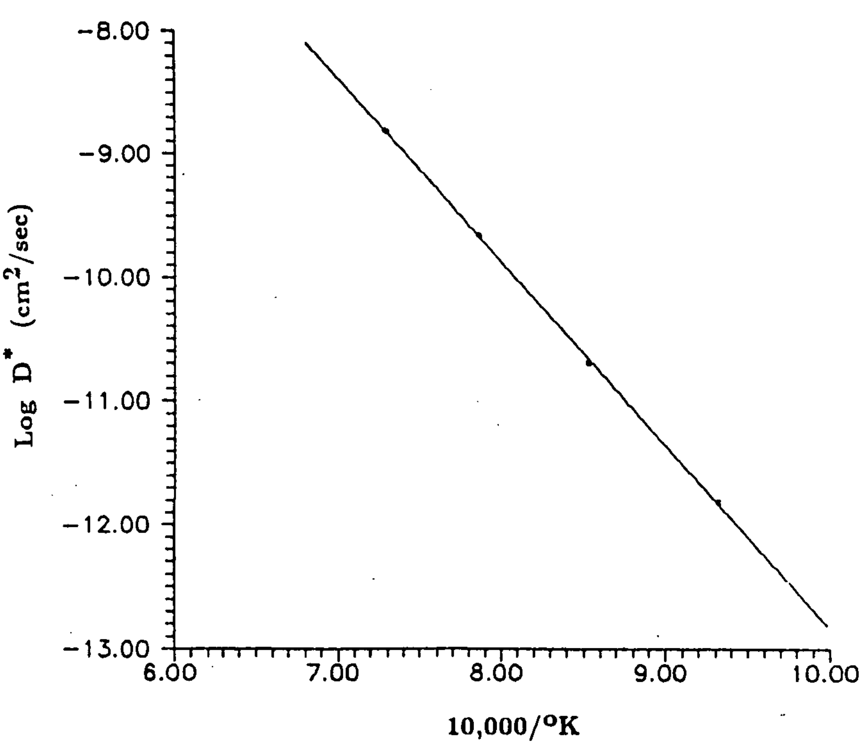

Figure 23. Arrhenius plot of the effective diffusion constant D^*.

Since this value is much less than the number of gold atoms that would be striking the surface of the silicon in the first 60 sec (7.8 E $17/cm^2$) it is safe to assume that there will always be enough gold vapor present to keep the silicon surface saturated.

An effective diffusion constant that reflects the rate at which interstitial gold becomes substitutional gold via the "kickout" mechanism as defined by Stolwijk et al. is

$$D^* = \frac{C_I^{eq} D_I}{C_s^{eq}} \tag{36}$$

where the subscript I denotes the concentration and diffusion constant of silicon interstitials, and C_s^{eq} is the solid solubility of gold. The value of D^* is 5E -9 cm^2/sec and can be obtained from extrapolating the data of Figure 23 to the temperature of interest. D^* can be used to calculate the concentration of substitutional gold at the center of a wafer of thickness d (assuming that the surfaces of the wafers are saturated) by the relation

$$C_s = C_s^{eq} \frac{2}{d} \quad (\pi D^* t)^{1/2} \tag{37}$$

According to these data, the concentration of substitutional gold in the center of a 5 E -2 cm thick wafer after one hour would be about 1.5 E 16/cm^3. This concentration of gold in the wafer (referring to Figure 18 again) would correspond to a resistivity of about 6 E 4 ohm-cm in the wafer center. (Resistivity at the wafer surfaces would be 3 E 5 ohm-cm, the maximum value.)

In order to raise the gold concentration in the center of the wafer to a value that would give a resistivity of 1.5 E 5 ohm-cm (4 E 16/cm^3), the wafer would have to be diffused for a time of 17 hours. It would be convenient to shorten this time by diffusing the gold at a temperature higher than the temperature at which it was deposited. This would be difficult to do by the gold coating method unless the gold-silicon eutectic region was first mechanically or chemically removed prior to the diffusion step. The gold vapor system described here should be much easier and more reproducible.

5.2.3.1 Gold Foil Doping Source

In one method of gold doping consistent with the principles outlined above and developed during this program, the source of gold is a pure gold foil which completely covers the top of a one-inch high hollow cylinder of fused silica. The wafer to be doped is placed at the bottom of this cylinder on a flat silica plate. The assembly is pushed into a furnace with a low nitrogen flow for a predetermined time. The reasoning behind this process is that the stagnant ambient between the gold foil and the wafer becomes saturated with gold vapor, which then reacts with and diffuses into the silicon wafer. The arrival rate of gold atoms at the silicon surface is sufficiently low that no appreciable gold accumulates on the silicon surface and staining of the surface is avoided. The total amount of gold diffused into a wafer is controlled by the time and temperature of the furnace.

For example, in one set of experiments, wafers were diffused (doped) at 910° and 1000°C for 15, 30, or 60 minutes. The wafers were then removed from the furnace, cleaned in aqua regia, and their sheet resistances and spreading resistance profiles were measured. The wafers were annealed in a nitrogen atmosphere for 60 minutes and remeasured.

In the following summary of results, D1 represents the area density (atoms/cm^2) of donors in the original wafer in atoms/cm^2, as determined by four-point probe measurement, and D2 represents the donor density after gold diffusion (doping). DELTA1 is the difference between D1 and D2, and is presumed to be equal to the area density (atoms/cm^2) of gold atoms in substitutional sites as long as the gold concentration remains considerably less than the donor concentration.

WAFER	D1	TEMP	TIME	TYPE	D2	DELTA1
DIS2-1	1.34 E13	1000	15	N	4.48 E12	8.92 E12
DIS2-2	6.10 E12	910	15	N	4.23 E12	1.87 E12
DIS2-3	9.63 E12	1000	30	P&N	4.33 E09	9.63 E12
DIS2-4	5.68 E12	910	30	N	2.37 E12	3.31 E12
DIS2-7	5.94 E12	910	60	N	1.31 E11	5.81 E12
DIS2-10	1.26 E13	1000	60	P	-5.02 E09	1.26 E13

Spreading resistance measurements made on the wafers after annealing at 1000°C showed that the resistivity was fairly uniform throughout the wafers. Four-point probe measurements made after the nitrogen anneal are summarized below. D3 represents the area density of donors after the anneal and DELTA2 is the difference between D1 and D3.

WAFER	TYPE	D1	D3	DELTA1	DELTA2
DIS2-1A	N	1.34 E13	1.66 E12	8.92 E12	1.17 E13
DIS2-2A	N	6.10 E12	2.65 E12	1.87 E12	3.45 E12
DIS2-3A	N	9.63 E12	2.64 E09	9.63 E12	9.63 E12
DIS2-4A	N	5.68 E12	6.34 E11	3.31 E12	5.05 E12
DIS2-7A	N	5.94 E12	1.25 E10	5.81 E12	5.93 E12
DIS2-10A	N	1.26 E13	1.05 E09	1.26 E13	1.26 E13

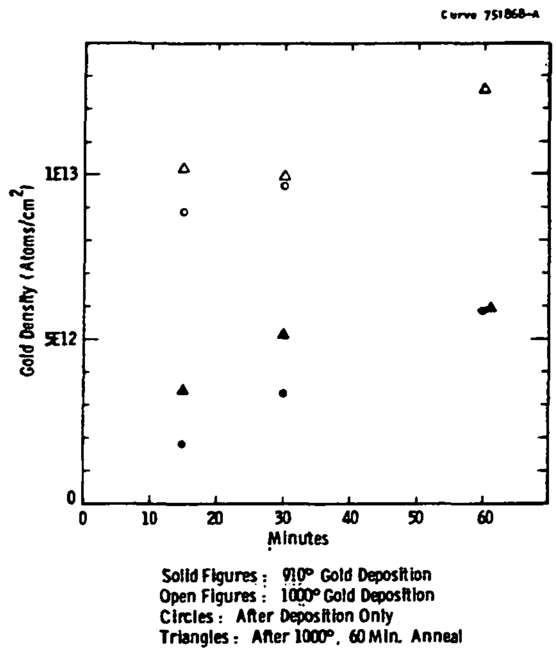

Figure 24. Area density of substitutional gold atoms after doping and annealing.

These results are plotted in Figure 24.

The solid solubilities of gold at 910° and 1000°C are believed to be 3.0 E 15 and 1.5 E 16 atoms/cm^3, corresponding to area densities of 8 E 13 and 4 E 14 atoms/cm^2, respectively. So we conclude that the wafers were doped with gold to levels which are still comfortably below the solubility limit.

Another aspect of this experiment was masking against gold doping. A part of each wafer was covered with 2000 Å of thermal oxide and 1500 Å of silicon nitride (it had been previously found that oxide alone was not a good barrier to gold diffusion). After each wafer was gold diffused and annealed, these layers were etched away and the sheet resistivity of the underlying silicon was measured. It was found that the resistivity of the masked areas was only slightly higher than the sheet resistivity of the unmasked areas had been before the gold diffusion. We conclude that silicon nitride is an effective diffusion barrier against gold.

5.2.3.2 Molten Gold Doping Source

Since gold melts at 1064°C, the gold foil method of introducing gold cannot be used at temperatures much above 1000°C. For these temperatures, the same fused silica cylinder was used, but molten gold was used as the source. The source was contained in a fused silica cup at the bottom of the cylinder; the wafer to be diffused was placed on the top of the cylinder so that the cylinder was completely covered.

Measurements made on wafers diffused in this way are tabulated in Table 32. The wafers in this experiment were a part of a Planar Annular device design run, and so had the diffused resistivity monitors for measuring high-resistivity silicon.

In this table, the conductance type and resistivity of the starting wafers are indicated in columns 5 and 6. The gold deposition process and the drive (anneal without gold source) times and temperatures are shown in column 2.

Measured resistance (in ohms) between two N^+ diffused regions are shown in column 3 and between two P^+ diffused regions are shown in column 4. An "R" indicates that the contacts showed rectifying characteristics (and so the "resistance" is actually a carrier generation leakage current). It is assumed that the region between the two contacts is the same conductivity type as the contacts which did not give rectifying characteristics, and that type is shown in column 5. A question mark indicates that the current-voltage characteristics between the N contacts and between the P contacts were so similar that no type determination could be made.

The wafer resistivity is calculated from the dimensions of the space between the contacts (0.1 squares) and the thickness of the wafers (0.026 to 0.029 cm). The calculated resistivity (in ohm-cm) is shown in column 6.

It is believed that the gold concentration required to produce the maximum final resistivity in wafers of this initial resistivity is approximately 7 E 15 per cubic centimeter.

TABLE 32

RESISTIVITIES OBTAINED IN RUN NUMBER DIS01

WAFER	PROCESS	R(N-N)	R(P-P)	TYPE	RESISTIVITY
DIS01-11	NONE			N	15.2
	DEP 1100, 60 min	5.00E4	3.85E5(R)	N	1.38E3
	DRV 1100, 120 min	6.25E5(R)	1.43E5	P	3.93E3
DIS01-12	NONE			N	18.1
	DEP 1100, 120 min	8.62E5(R)	1.09E5	P	2.91E3
	DRV 1100, 120 min	8.62E5(R)	6.2E4	P	1.68E3
DIS01-13	NONE			N	14.
	DEP 1100, 120 min	1.61E5(R)	5.00E4	P	1.33E3
	DRV 1100, 120 min	5.00E5(R)	3.57E4	P	946
DIS01-14	NONE			N	9.43
	DEP 1100, 12 min	71.4	3.33E7(R)	N	18.8
	DRV 1100, 120 min	167	5.00E6(R)	N	43.8
DIS01-16	NONE			N	9.51
	DEP 1100, 24 min	192	1.11E6(R)	N	51.5
	DRV 1100, 120 min	1.67E4	2.38E6(R)	N	4.47E3
DIS01-18	NONE			N	14.2
	DEP 1100, 48 min	6.85E3	8.33E5(R)	N	1.88E3
	DRV 1100, 120 min	1.04E5	4.76E5(R)	N	2.85E4
DIS01-19	NONE			N	13.9
	DEP 1100, 48 min	1.52E5	7.14E5(R)	N	4.16E4
	DRV 1100, 120 min	2.50E5	2.22E5	?	6.85E4
DIS01-20	NONE			N	18.1
	DEP 1100, 48 min	1.92E5	5.88E5(R)	N	5.26E4
	DRV 1100, 120 min	2.86E5	2.86E5	?	7.83E4

An alternative method for introducing the proper number of gold atoms, and homogenizing the gold concentration throughout the silicon wafer, would be to soak the silicon in the presence of excess gold at the temperature for which the solid solubility is the desired gold concentration. For wafers of the initial resistivity considered here, that temperature would be approximately 950°C, and the time required for homogenization at that temperature would be unacceptably long.

The deposition and drive processes used here allow higher processing temperatures, thus greatly reducing the times required. Since the solid solubility of gold in silicon at 1100°C is approximately 3 E 16 per cubic centimeter, it is necessary to regulate the gold deposition time in order to limit the number of gold atoms to the desired value. The parameters necessary to predict what this deposition time should be for silicon wafers of various thicknesses and initial dopings are not well known at this time, so an empirical approach is required.

Interpretation of the data in Table 32 is that, for wafers of this initial doping and thickness, a gold deposition of 48 minutes at 1100°C introduces approximately the correct amount of gold into the wafer to achieve maximum resistivity. An anneal of two hours at 1100°C is sufficient to homogenize the gold concentration in the silicon. Shorter gold deposition times result in lower ultimate gold concentration, producing wafers of lower resistivity; longer gold deposition times introduce sufficient gold to convert the silicon to P type with a concomitant decrease in resistivity from the theoretical maximum value (3 E 5 ohm-cm). Some of the N-type resistivities listed in this table are believed to be the highest yet achieved by gold doping in the deep-impurity programs at Westinghouse.

The molten gold source has been the principle method for gold doping comparatively low-resistivity wafers. Control and reproducibility of the gold-doping process appear to be satisfactory.

Because the high resistivities produced by gold doping make measurement by four-point probe difficult, the specially designed diffused contacts on the wafers are necessary for the determination of resistivity and conductivity type.

6. DEVICE TESTING

6.1 PROBE MODIFICATION FOR HIGH VOLTAGE

Wafer testing was performed on a manual probing station such as that commonly used for IC testing. The probes and their connections were modified with extra electrical insulation in order to permit testing at voltages exceeding 2000 V. A micarta disc was placed between the $(DI)^2$ wafers and the wafer chuck to prevent electrical arcing between the chuck and the tested devices.

6.2 LOW-POWER, HIGH-VOLTAGE TESTING

Low-power measurements were made with a Tektronix 576 curve tracer. This instrument is capable of up to 1500 V either ac, dc, or pulsed. It cannot simultaneously provide high current and high-voltage.

Some measurements were made with the 576 curve tracer using a Tektronix 176 pulsed high-current fixture. This fixture has a maximum voltage capability of only 350 V but is capable of furnishing high pulsed (300 μs) current. It has often been improperly used by investigators who were unaware that although the gate current is pulsed, the voltage applied to the transistor collector is not pulsed, but is dc; so although the CRT display seems to indicate that no power is being dissipated in the device between gate pulses, there is, in fact, a constant power dissipation due to any leakage current in the transistor. It is speculated that some $(DI)^2$ switching that has been previously reported was actually due to high temperature caused by power dissipation in the tested device. For this reason, the pulsed high-current fixture is of limited use in the testing of high-voltage (as opposed to high-current) transistors.

6.3 HIGH-POWER TESTING SYSTEM

High-power testing was accomplished using a Cober pulsed power supply. In this measurement mode, current was measured with a Tektronix P6042 current probe and the pulsed voltage was measured separately with an oscilloscope.

7. RESULTS

7.1 DIODES WITH LOW POWER PULSE

All diode structures on the wafers of the Lateral High-Voltage design that were completed in the previous program were tested for threshold voltage using a 300 microsecond high-voltage pulse from the Cober supply. The low-voltage resistance between anode and cathode of the same devices was measured separately with the 576 curve tracer. These data were analyzed for correlation between resistance, threshold voltage, device structure, and device processing.

7.2 LOW-POWER TESTS OF HIGH-VOLTAGE LATERAL SQUARE DEVICES

Low-power measurements were made on some completed High-Voltage Lateral Square devices. It is to be expected that the low-power conductivity of these devices would be proportional to the ratio of the channel width to the channel length for all devices fabricated on any one wafer (D/G in Figure 9). Significant deviation from this expected behavior was observed on some wafers and is attributed to inadequate control of the gold-doping process. Figure 25 illustrates the results of these measurements on a wafer which had no intentionally introduced deep levels. The solid line in the figure depicts the expected behavior for material of 100 ohm-cm, the nominal resistivity of the wafer. The observed deviation from strictly ohmic behavior might be attributed to spreading of current outside the geometrical channel region; this effect would be expected to result in an apparent higher conductivity for devices with low width-to-length ratios.

Figure 26 shows the results of similar measurements made on wafers which had been gold diffused at three different temperatures. The behavior of the wafers diffused at 1070° and at 1080°C corresponds to effective resistivities of 1 E 5 to 5 E 5 ohm-cm. The erratic behavior

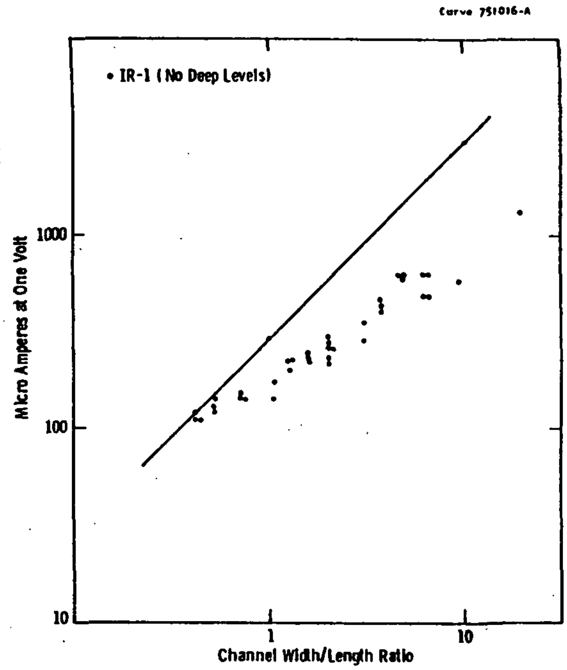

Figure 25. Measured low-power conductance of High-Voltage Lateral Square devices on a wafer without deep levels (DI LS IR-1).

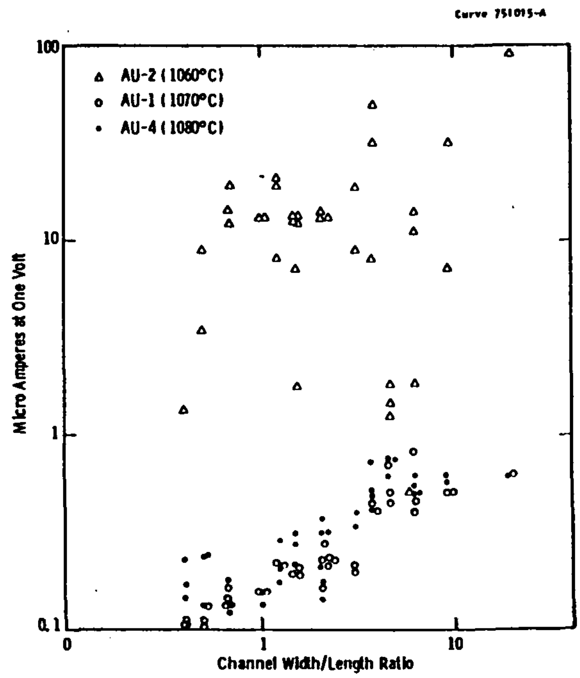

Figure 26. Measured low-power conductance of High-Voltage Lateral Square devices on wafers with differing gold diffusions.

of the wafer which was diffused at 1060°C must be attributed to an uncontrolled and nonuniform gold diffusion. It was concern over such anomalies that prompted further investigations of gold diffusion technology.

7.2.1 Statistical Analysis

An attempt was made to find a correlation between the wafer resistivity as determined by low-voltage I-V measurements on High-Voltage Lateral Square devices and the threshold voltages of those devices when they were tested at high-voltage.

Because of the large amount of scatter in the data, there was no obvious correlation between threshold voltage and the other parameters, and the data were analyzed with statistical computer software (ECHIP). The number of data points (150 x 5 matrix) was too large for analysis in one batch, so it was split into three data groups which were called AU1, AU2, and AU3.

The results of the analyses performed by this program are in the form of simulated three-dimensional plots such as are shown in Figures 27-43. The statistical program analyzes the data which in this case were the width-to-length ratio of the diode (W/L), the resistivity of the channel as computed from the channel dimensions and the low-voltage I-V measurement, and the threshold voltage which had been measured by the high-voltage pulse method. From the data, the software calculates a relationship (if any) among these data and displays what that relationship might be. In each plot, the computed value of the threshold voltage is displayed in a band labeled with a letter (A, B, C, ---). Dots or commas are used to indicate bands between the values shown by the letters. In these figures, the ordinate is the device length (in microns) and the abscissa is the log of the calculated resistivity. The ratio of the device width to the device length, W/L, is a parameter. The value for W/L is indicated at the lower right of each plot.

The characteristics of the plots are dependent upon the form of the relationship (linear, factorial, or quadratic) to which the data are fitted. For example, Figure 27 shows that the measured threshold

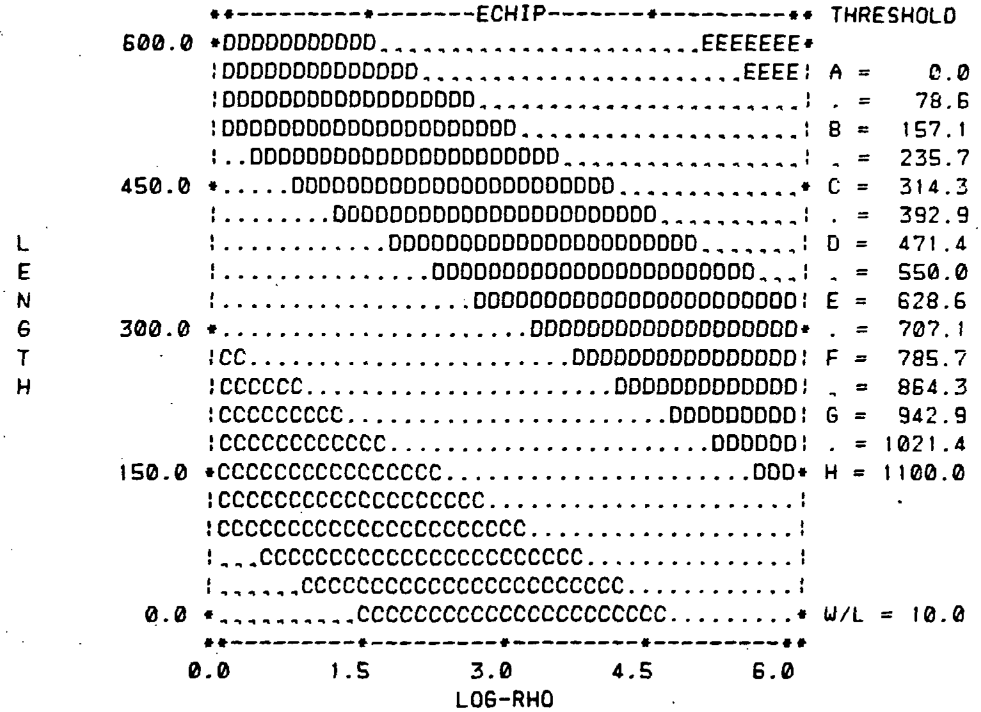

Figure 27. Data Group AU1. Linear Model, W/L = 10.0.

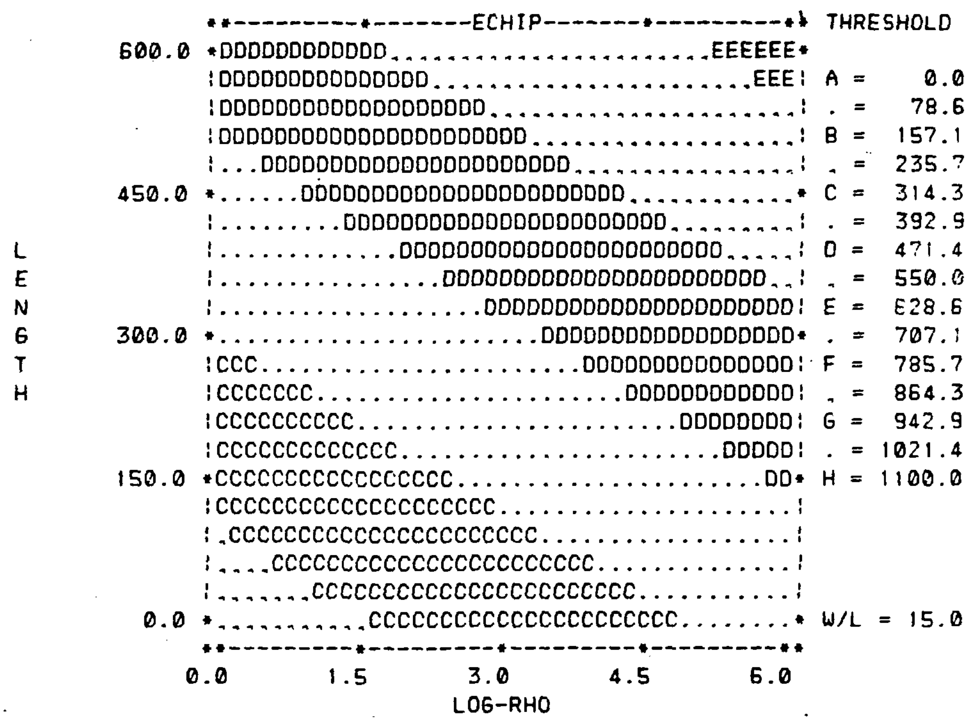

Figure 28. Data Group AU1. Linear Model, W/L = 15.0.

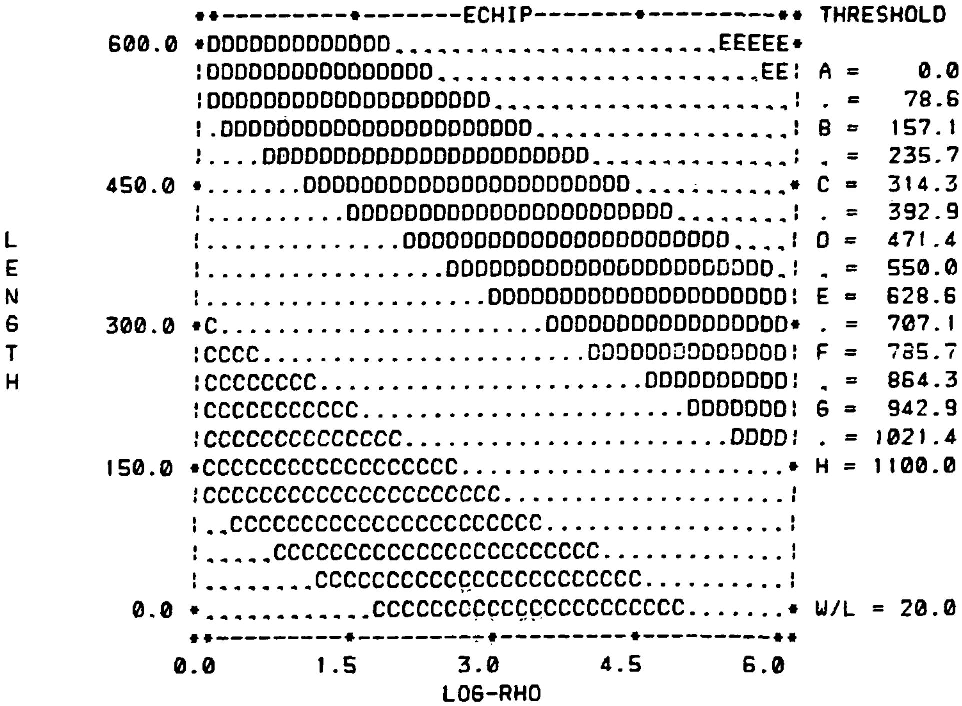

Figure 29. Data Group AU1. Linear Model, W/L = 20.0.

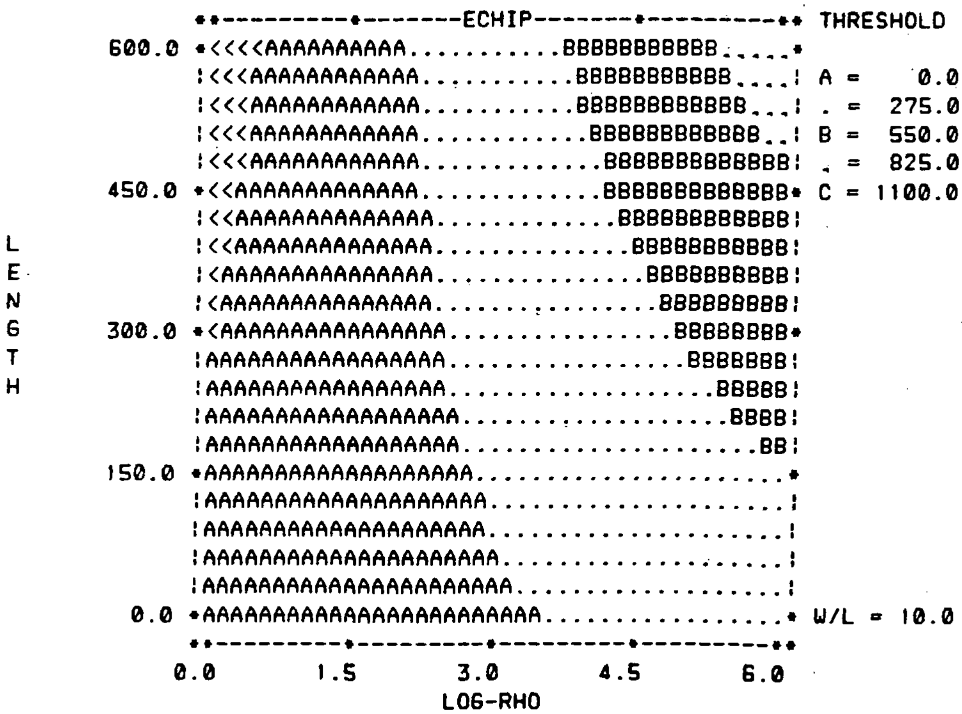

Figure 30. Data Group AU1. Factorial Model, W/L = 10.0.

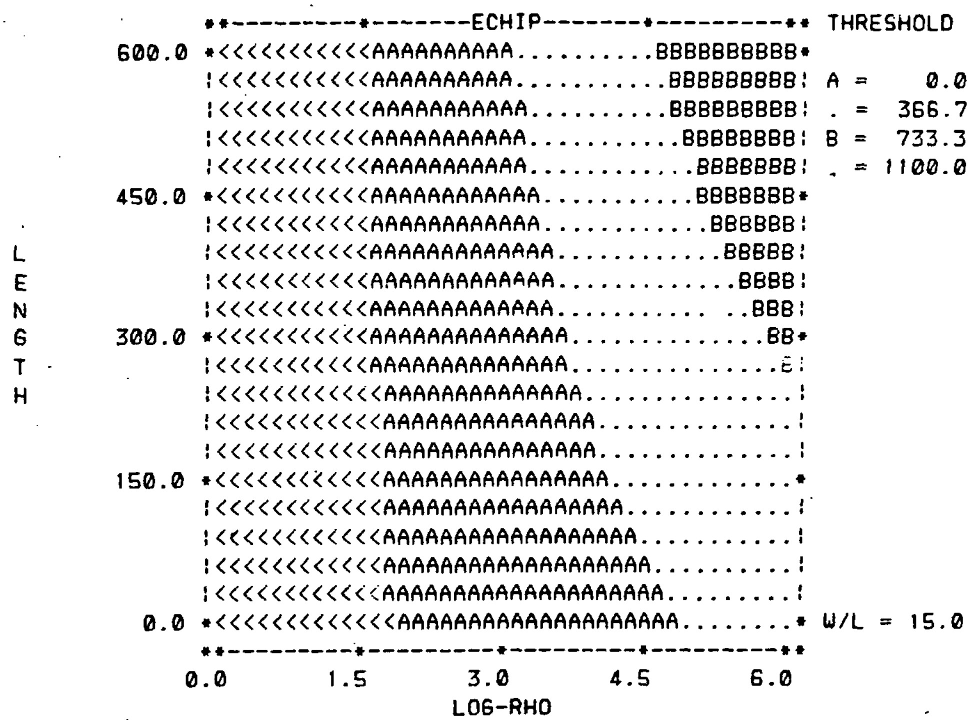

Figure 31. Data Group AU1. Factorial Model, W/L = 15.0.

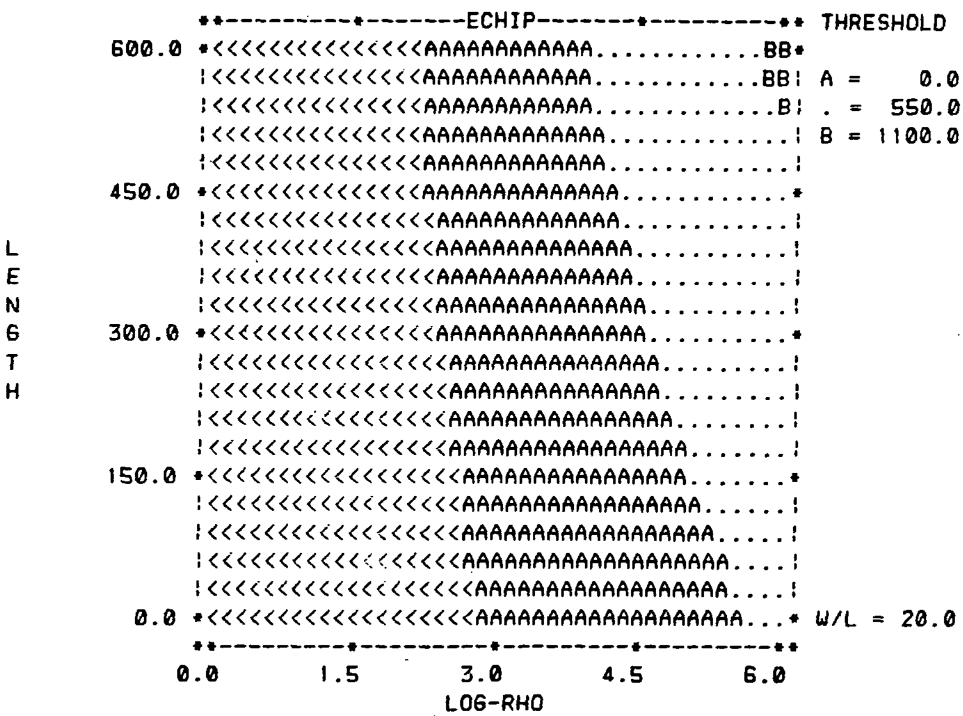

Figure 32. Data Group AU1. Factorial Model, W/L = 20.0.

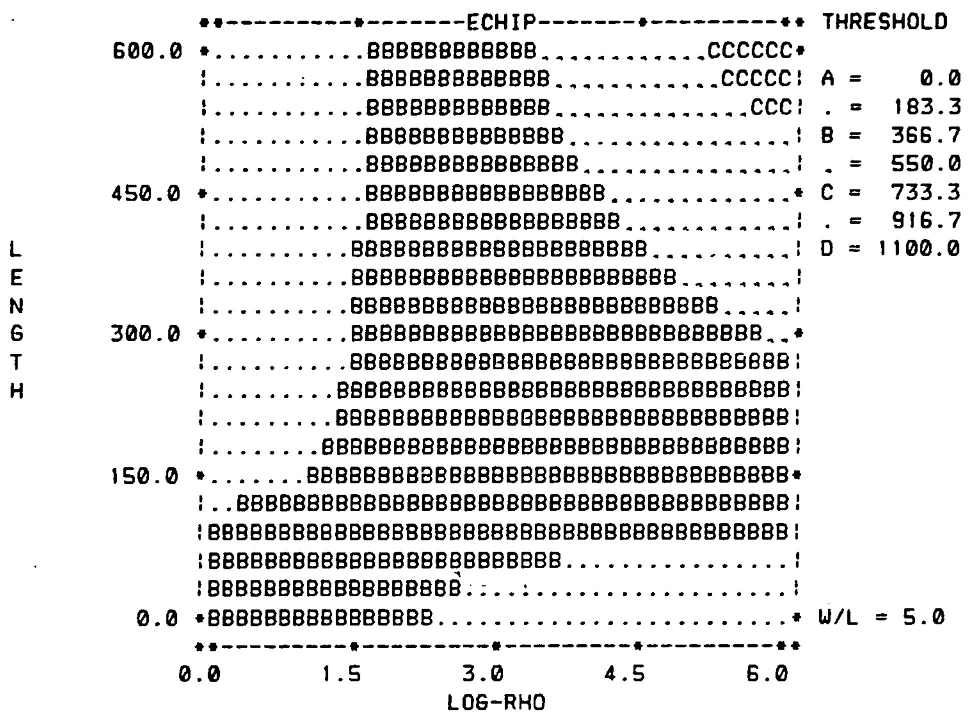

Figure 33. Data Group AU1. Factorial Model, W/L = 5.0.

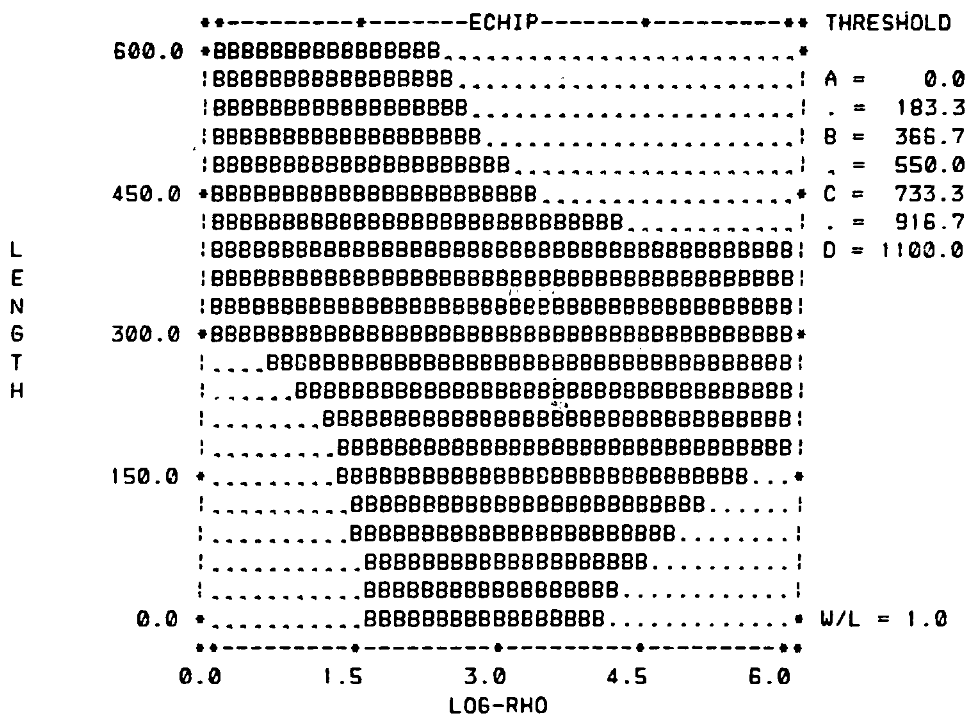

Figure 34. Data Group AU1. Factorial Model, W/L = 1.0.

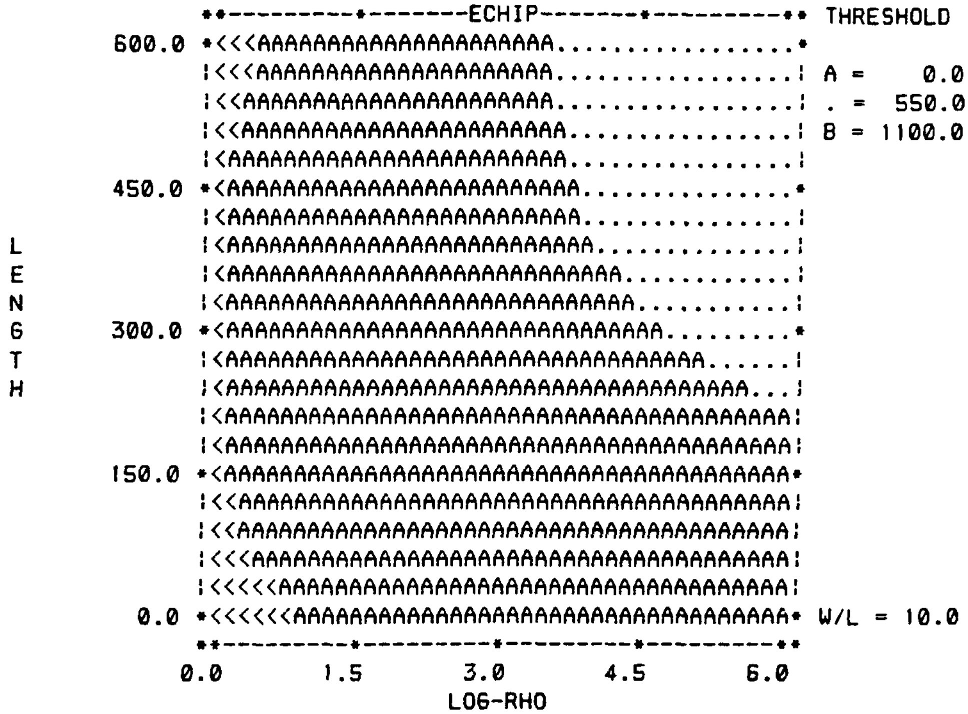

Figure 35. Data Group AU1. Quadratic Model, W/L = 10.0.

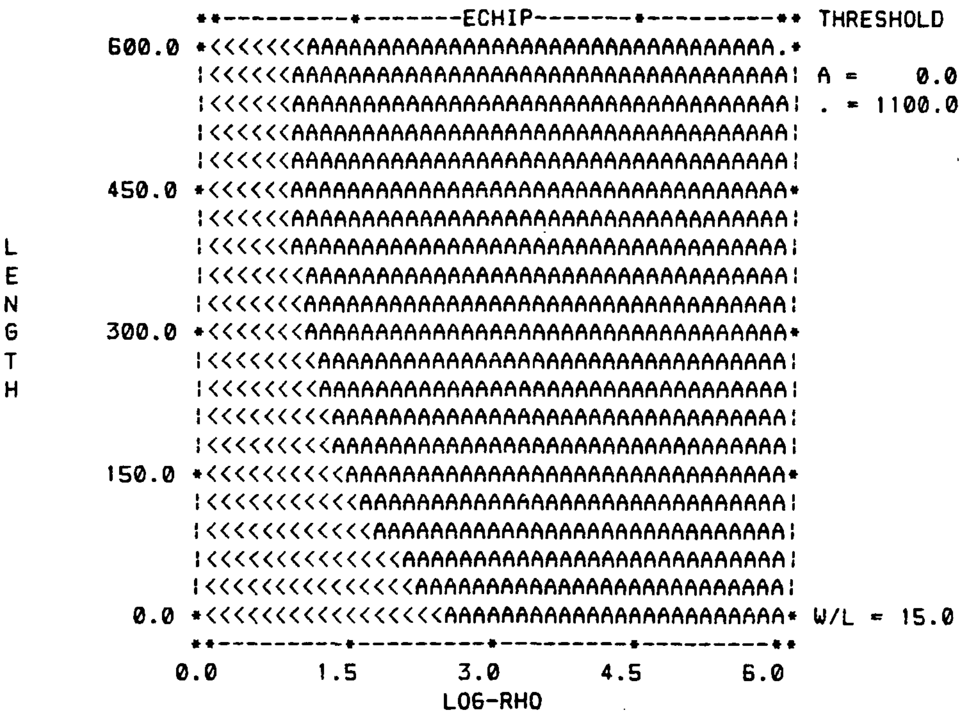

Figure 36. Data Group AU1. Quadratic Model, W/L = 15.0.

```
          **---------*--------ECHIP--------*----------** THRESHOLD
   600.0 *<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAA........*
    L    |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAA.......|  A =    0.0
         |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAA.......|  . = 1100.0
         |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAA......|
         |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAA.....|
   450.0 *<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAA....*
         |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA...|
 L       |<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA..|
 E       |<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
 N       |<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
 G 300.0 *<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA*
 T       |<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
 H       |<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
         |<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
         |<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
   150.0 *<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAA*
         |<<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAA|
         |<<<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAA|
         |<<<<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAA|
         |<<<<<<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAA|
     0.0 *<<<<<<<<<<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAA* W/L = 20.0
         **---------*----------*----------*--------**
         0.0       1.5        3.0        4.5       6.0
                             LOG-RHO
```

Figure 37. Data Group AU1. Quadratic Model, W/L = 20.0.

```
          **---------*--------ECHIP--------*----------** THRESHOLD
   600.0 *....DDDDDDDDDDD,,,,,,,,,,,,,EEEEEEEEEEE...*
         |.......DDDDDDDDDDDD,,,,,,,,,,,EEEEEEEEEEEE|  A =    0.0
         |............DDDDDDDDDDD,,,,,,,,,,,,EEEEEEE|  . =  122.2
         |CCC............DDDDDDDDDDD,,,,,,,,,,,,,EEE|  B =  244.4
         |CCCCCCC...........DDDDDDDDDDDD,,,,,,,,,,,,|  , =  366.7
   450.0 *CCCCCCCCCC.............DDDDDDDDDDD,,,,,,,,*  C =  488.9
         |,,,CCCCCCCCCCC.............DDDDDDDDDDD,,,,|  . =  611.1
 L       |,,,,,,CCCCCCCCCCCC...........DDDDDDDDDDDDD|  D =  733.3
 E       |,,,,,,,,,,,CCCCCCCCCCC............DDDDDDDD|  , =  855.6
 N       |BB,,,,,,,,,,,,CCCCCCCCCCC.............DDDD|  E =  977.8
 G 300.0 *BBBBBB,,,,,,,,,,,,CCCCCCCCCCCC............*  . = 1100.0
 T       |BBBBBBBBB,,,,,,,,,,,,,CCCCCCCCCCC.........|
 H       |..BBBBBBBBBBB,,,,,,,,,,,,,CCCCCCCCCCC.....|
         |.....BBBBBBBBBBBB,,,,,,,,,,,CCCCCCCCCCCCC.|
         |.........BBBBBBBBBBB,,,,,,,,,,,,CCCCCCCCCC|
   150.0 *A............BBBBBBBBBBB,,,,,,,,,,,,,CCCCC*
         |AAAAA...........BBBBBBBBBBBB,,,,,,,,,,,,CC|
         |AAAAAAAA............BBBBBBBBBBB,,,,,,,,,,,|
         |<AAAAAAAAAAA............BBBBBBBBBBB,,,,,,,|
         |<<<<AAAAAAAAAAAA............BBBBBBBBBBBB,,|
     0.0 *<<<<<<<<AAAAAAAAAAA.............BBBBBBBBBB* W/L = 10.0
         **---------*----------*----------*--------**
         0.0       1.5        3.0        4.5       6.0
                             LOG-RHO
```

Figure 38. Data Group AU2. Linear Model, W/L = 10.0.

```
         **----------*--------ECHIP-------*----------** THRESHOLD
   600.0 *BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB*
         |BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB| A =    0.0
         |BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB| . =  366.7
         |BBBBBBBBBBBBBBBBBBBBBBBBBBBBBBB..........| B =  733.3
         |BBBBBBBBBBBBBBBBBBBBBBBBB................| , = 1100.0
   450.0 *BBBBBBBBBBBBBBBBBBBB.....................*
         |BBBBBBBBBBBBBBBBB........................|
L        |BBBBBBBBBBBBBBB..........................|
E        |BBBBBBBBBBBBBB...........................|
N        |BBBBBBBBBBBB.............................|
G  300.0 *BBBBBBBBBBB..............................*
T        |BBBBBBBBBB...............................|
H        |BBBBBBBBB...............................A|
         |BBBBBBBB.............................AAAA|
         |BBBBBBBB..........................AAAAAAA|
   150.0 *BBBBBBB.........................AAAAAAAAA*
         |BBBBBBB.......................AAAAAAAAAAA|
         |BBBBBB.......................AAAAAAAAAAAA|
         |BBBBBB.....................AAAAAAAAAAAAAA|
         |BBBBBB....................AAAAAAAAAAAAAAA|
     0.0 *BBBBB...................AAAAAAAAAAAAAAAAA* W/L = 10.0
         **----------*---------*---------*----------**
         0.0        1.5       3.0       4.5       6.0
                              LOG-RHO
```

Figure 39. Data Group AU2. Factorial Model, W/L = 10.0.

```
         **----------*--------ECHIP-------*----------** THRESHOLD
   600.0 *AAAAAAAAAAAAA............................*
         |AAAAAAAAAAAA.............................| A =    0.0
         |AAAAAAAAAAA..............................| . =  550.0
         |AAAAAAAAAAA..............................| B = 1100.0
         |AAAAAAAAAA...............................|
   450.0 *AAAAAAAAAA...............................*
         |AAAAAAAAAA..............................A|
L        |AAAAAAAAAA............................AAA|
E        |AAAAAAAAAA..........................AAAAA|
N        |AAAAAAAAAA.......................AAAAAAAA|
G  300.0 *AAAAAAAAAA....................AAAAAAAAAAA*
T        |AAAAAAAAAAA................AAAAAAAAAAAAAA|
H        |AAAAAAAAAAAAA.........AAAAAAAAAAAAAAAAAAA|
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA|
   150.0 *AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<*
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<|
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<|
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<|
         |AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<|
     0.0 *AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<<<* W/L = 10.0
         **----------*---------*---------*----------**
         0.0        1.5       3.0       4.5       6.0
                              LOG-RHO
```

Figure 40. Data Group AU2. Quadratic Model, W/L = 10.0.

```
         **----------*--------ECHIP--------*----------** THRESHOLD
   600.0 *CCCCCCCCCCCCCC,,,,,,,,,,,,,,,,BBBBBBBBBBB*
         |CCCCCCCCCCCC,,,,,,,,,,,,,,,,BBBBBBBBBBBBB| A =    0.0
         |CCCCCCCCCC,,,,,,,,,,,,,,,BBBBBBBBBBBBBBB.| . =  157.1
         |CCCCCCC,,,,,,,,,,,,,,,,BBBBBBBBBBBBBBB...| B =  314.3
         |CCCCC,,,,,,,,,,,,,,,BBBBBBBBBBBBBBBB.....| , =  471.4
   450.0 *CCC,,,,,,,,,,,,,,,BBBBBBBBBBBBBBBB.......* C =  628.6
         |,,,,,,,,,,,,,,,,BBBBBBBBBBBBBBB..........| . =  785.7
L        |,,,,,,,,,,,,,BBBBBBBBBBBBBBBB............| D =  942.9
E        |,,,,,,,,,,,BBBBBBBBBBBBBBB...............| , = 1100.0
N        |,,,,,,,,BBBBBBBBBBBBBBBB...............AA|
G  300.0 *,,,,,,BBBBBBBBBBBBBBBB...............AAAA*
T        |,,,,BBBBBBBBBBBBBBB................AAAAAA|
H        | ,BBBBBBBBBBBBBBB...............AAAAAAAAA|
         |BBBBBBBBBBBBBBB...............AAAAAAAAAAA|
         |BBBBBBBBBBBB................AAAAAAAAAAAAA|
   150.0 *BBBBBBBBBB...............AAAAAAAAAAAAAAA<*
         |BBBBBBB................AAAAAAAAAAAAAAA<<<|
         |BBBBB...............AAAAAAAAAAAAAAAA<<<<<|
         |BB................AAAAAAAAAAAAAAA<<<<<<<<|
         |................AAAAAAAAAAAAAAA<<<<<<<<<<|
     0.0 *.............AAAAAAAAAAAAAAAA<<<<<<<<<<<<* W/L = 10.0
         **----------*----------*----------*----------**
        0.0        1.5        3.0        4.5        6.0
                            LOG-RHO
```

Figure 41. Data Group AU3, Linear Model, W/L = 10.0.

```
         **----------*--------ECHIP--------*----------** THRESHOLD
   600.0 *BBBBBBBBBBB..................AAAAAAAAAAAA*
         |BBBBBBBBB...................AAAAAAAAAAAAA| A =    0.0
         |BBBBBBBB...................AAAAAAAAAAAAAA| . =  550.0
         |BBBBBBB...................AAAAAAAAAAAAAAA| B = 1100.0
         |BBBBBB...................AAAAAAAAAAAAAAAA|
   450.0 *BBBB....................AAAAAAAAAAAAAAAAA*
         |BBB....................AAAAAAAAAAAAAAAAAA|
L        |B.....................AAAAAAAAAAAAAAAAAAA|
E        |.....................AAAAAAAAAAAAAAAAAAAA|
N        |....................AAAAAAAAAAAAAAAAAAAAA|
G  300.0 *...................AAAAAAAAAAAAAAAAAAAAA<*
T        |.................AAAAAAAAAAAAAAAAAAAAAAA<|
H        |................AAAAAAAAAAAAAAAAAAAAAAA<<|
         |...............AAAAAAAAAAAAAAAAAAAAAAA<<<|
         |.............AAAAAAAAAAAAAAAAAAAAAAAA<<<<|
   150.0 *............AAAAAAAAAAAAAAAAAAAAAAAA<<<<<*
         |..........AAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<|
         |.........AAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<|
         |.......AAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<|
         |.....AAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<<|
     0.0 *...AAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<<<<* W/L = 10.0
         **----------*----------*----------*----------**
        0.0        1.5        3.0        4.5        6.0
                            LOG-RHO
```

Figure 42. Data Group AU3, Factorial Model, W/L = 10.0.

```
         **---------*-------ECHIP-------*---------** THRESHOLD
   600.0 *A..............BBBBBBBBBBB..............A*
         |AAA...................................AAA| A =    0.0
         |AAAA.................................AAAA| . =  366.7
         |AAAAA...............................AAAAA| B =  733.3
         |AAAAAA.............................AAAAAA| , = 1100.0
   450.0 *AAAAAAAA.........................AAAAAAAA*
         |AAAAAAAAA.......................AAAAAAAAA|
L        |AAAAAAAAAAA...................AAAAAAAAAAA|
E        |<AAAAAAAAAAA.................AAAAAAAAAAA<|
N        |<<AAAAAAAAAAAAA...........AAAAAAAAAAAAA<<|
G  300.0 *<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<*
T        |<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<|
H        |<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<|
         |<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<|
         |<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<|
   150.0 *<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<*
         |<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<|
         |<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<|
         |<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<<|
         |<<<<<<<<<AAAAAAAAAAAAAAAAAAAAAAA<<<<<<<<<|
     0.0 *<<<<<<<<<<AAAAAAAAAAAAAAAAAAAAA<<<<<<<<<<* W/L = 10.0
         **---------*---------*---------*---------**
        0.0       1.5       3.0       4.5       6.0
                           LOG-RHO
```

Figure 43. Data Group AU3, Modified Quadratic Model, W/L = 10.0.

voltage is found to increase with either the device length or the log of the resistivity (threshold voltage is indicated in volts), while W/L is held constant at 10.0.

Figures 28 and 29 show that this dependence on length and resistivity is not much affected if W/L assumes values of 15.0 or 20.0 instead. Figures 30 to 34 show the results of fitting the same data group to a factorial model. When fitted to that model, the data indicate that resistivity is the strongest factor affecting threshold voltage. Again, W/L has little effect.

Figures 35 to 37 show that when the data are fitted to a quadratic model, the threshold voltage is quite insensitive to device length and only weakly dependent upon device resistivity. Figures 38 to 40 display the results of the analysis of the second data group, which are similar to the analysis of the first data group.

Figures 41 to 43 show the results of analysis of the third data group. In this case there appears to be an inverse relationship between resistivity and threshold voltage, while the effect of device length is positive. This relationship appears to be true whether the data are fitted to a linear model, a factorial model, or a quadratic model.

It must be concluded from these analyses that the data scatter is too great to quantitatively predict the dependence of threshold voltage upon any of the parameters investigated, even when a large data base is analyzed.

A representative curve obtained during these high-power measurements is shown in Figure 44. Since a pulsed power supply is used in the measurements, the data are obtained as points rather than a smooth curve. In the particular case shown, the power was increased until the device burned out because of dissipated power at high current.

7.3 HIGH-POWER TESTING

The high-power pulse system using the Cober pulser was used to test a wide variety of Planar Annular devices. Surprisingly, some kind of negative resistance characteristic was found in many devices in which it was not to be expected. Applied voltage was increased to the point that obvious thermal runaway was incipient.

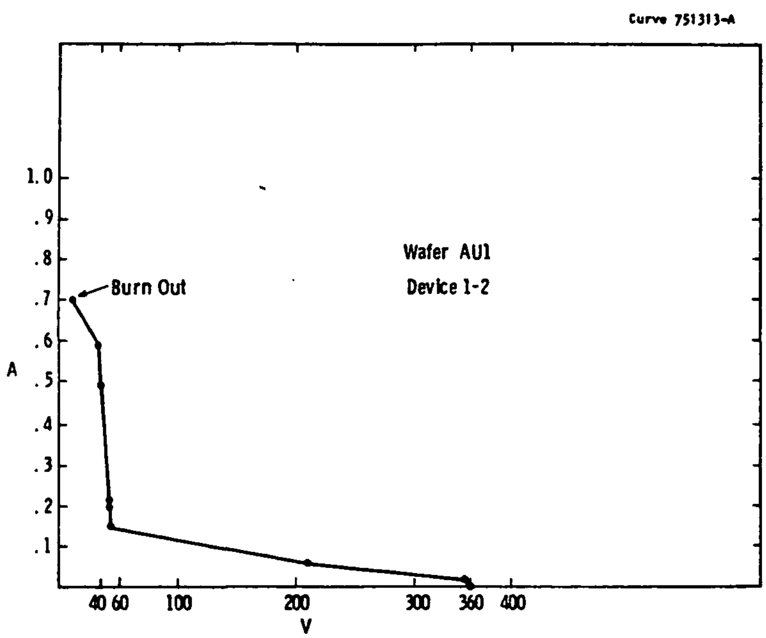

Figure 44. Current-voltage relation of a High-Voltage Lateral Square device obtained from a pulsed (300 μsec) power supply.

7.3.1 Switching Behavior

Switching behavior or negative resistance was found to occur in many of the Planar Annular devices that were fabricated during this program. No high-voltage devices were found to be sensitive to gate control of the switching process. In many cases, small changes could be made in the threshold voltage by either grounding or floating the gate; in some cases, there was an effect from introducing current at an injection gate, but all of these could be explained on the basis that the gate was simply acting as an auxiliary anode or cathode.

The I-V plots shown in Figures 45-54 are typical, but by no means exhaustive, of the results. Some devices were symmetrical, switching nearly identically with the emitter either positive or negative with respect to the collector. Other devices switched in either direction but with quite different characteristics.

The notations at the top of each figure refer to the structure of the device indicating, respectively, the conductivity type of the emitter (N, P, or Shieh diffusion); the conductivity type of the collector; the emitter-collector spacing in μm; and the type of gate (N, P, or Shieh injection gate).

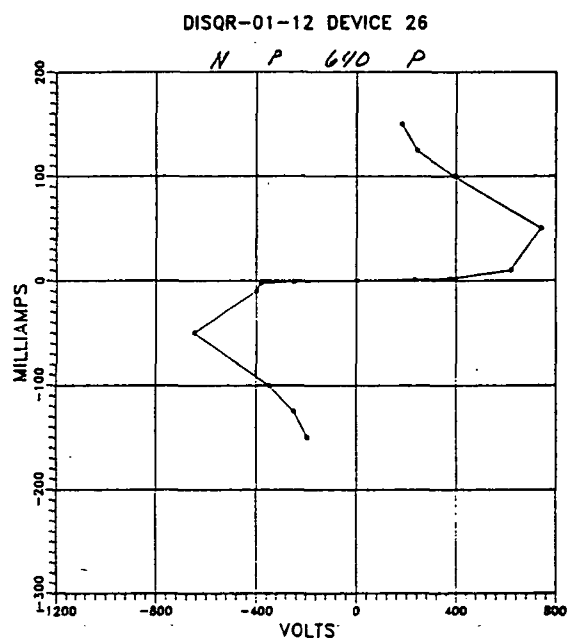

Figure 45. Pulsed I-V characteristics of a planar annular $(DI)^2$ device with N emitter, P collector, 640 μm emitter-collector space, and P injection gate.

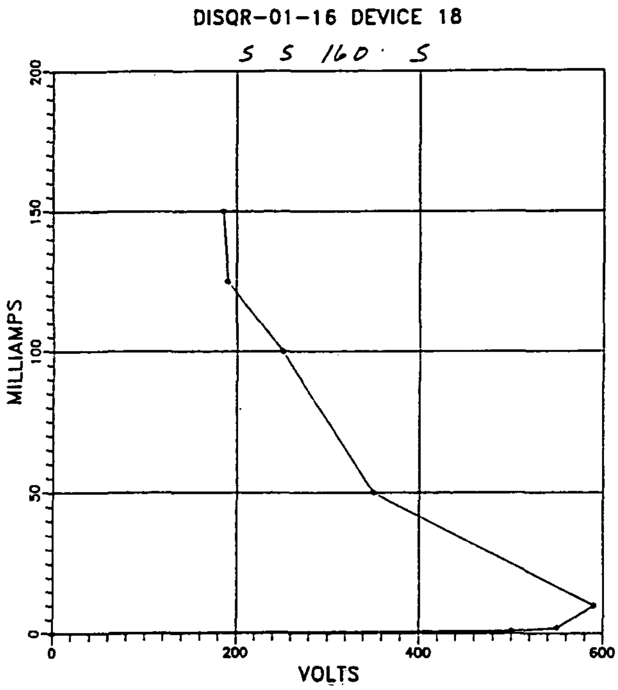

Figure 46. Pulsed I-V with Shieh emitter, Shieh collector, 160 μm emitter-collector space, and Shieh injection gate.

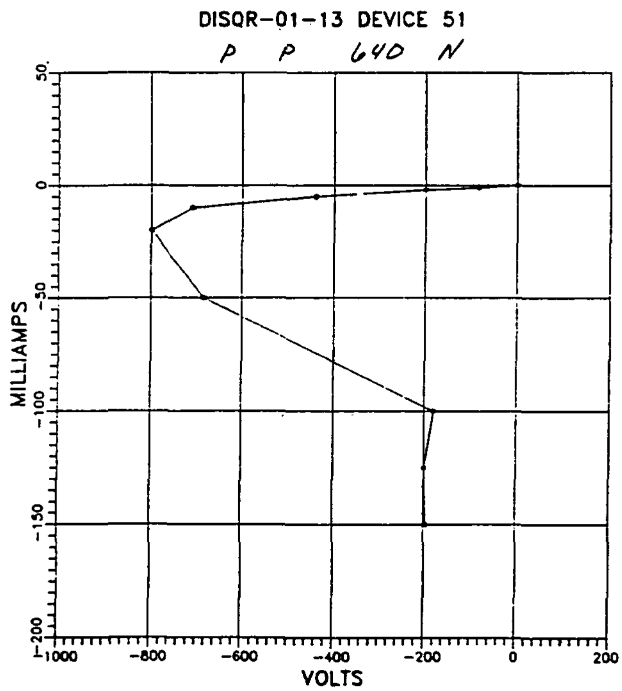

Figure 47. Pulsed I-V with P emitter, P collector, 640 μm emitter-collector space, and N injection gate.

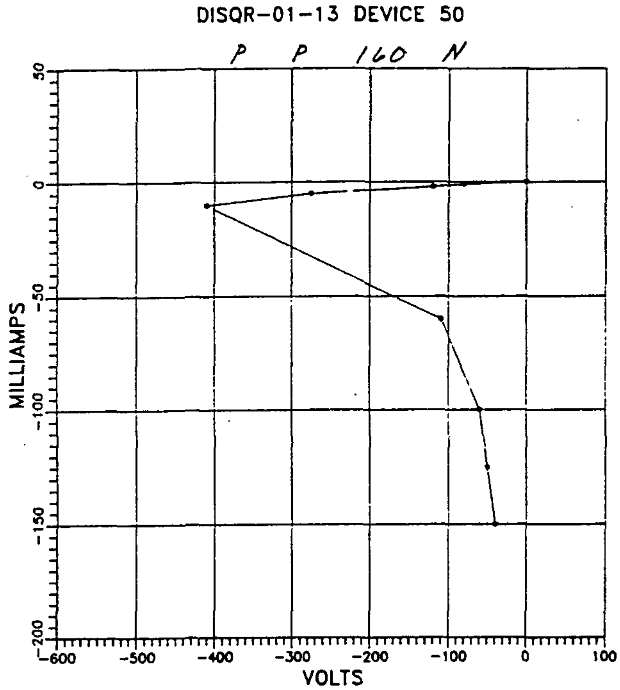

Figure 48. Pulsed I-V with P emitter, P collector, 160 μm emitter- collector space, and N injection gate.

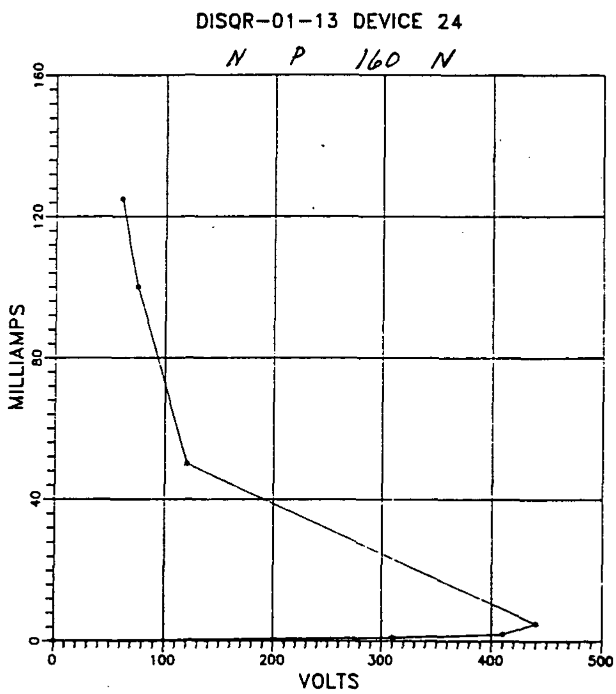

Figure 49. Pulsed I-V with N emitter, P collector, 160 μm emitter-collector space, and N injection gate.

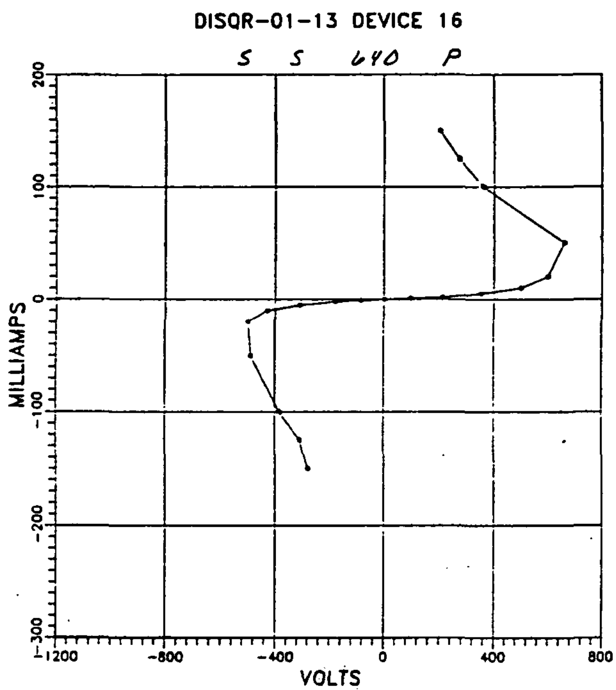

Figure 50. Pulsed I-V with Shieh emitter, Shieh collector, 160 μm emitter-collector space, and P injection gate.

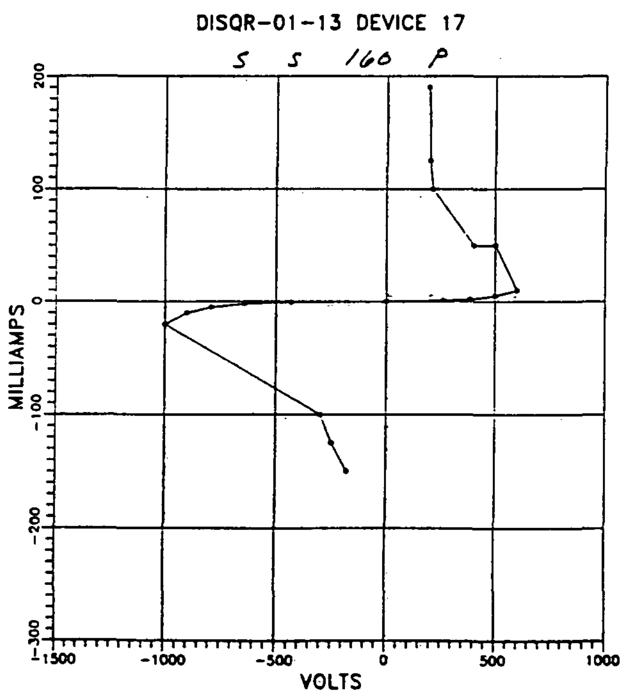

Figure 51. Pulsed I-V with Shieh emitter, Shieh collector, 640 μm emitter-collector space, and P injection gate.

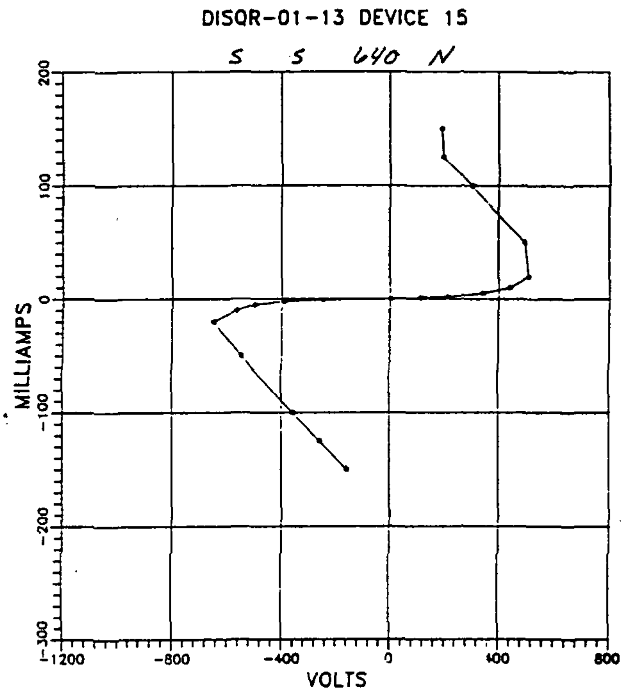

Figure 52. Pulsed I-V with Shieh emitter, Shieh collector, 640 μm emitter-collector space, and P injection gate.

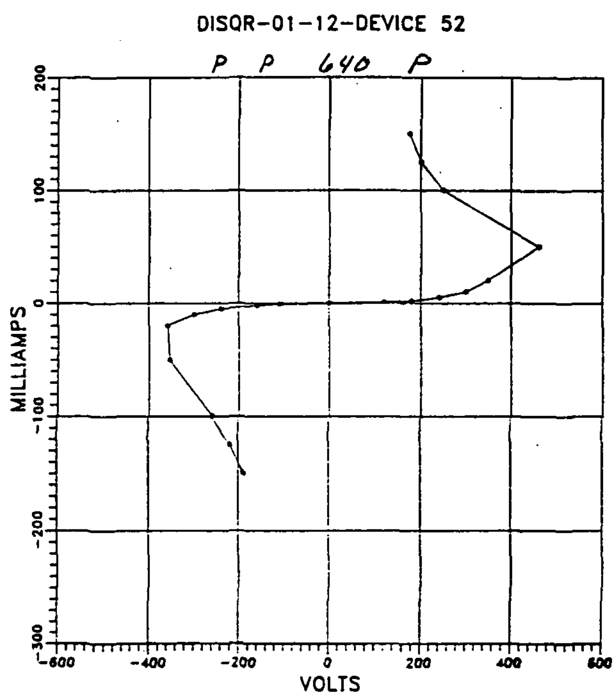

Figure 53. Pulsed I-V with P emitter, P collector 640 μm emitter-collector space, and P injection gate.

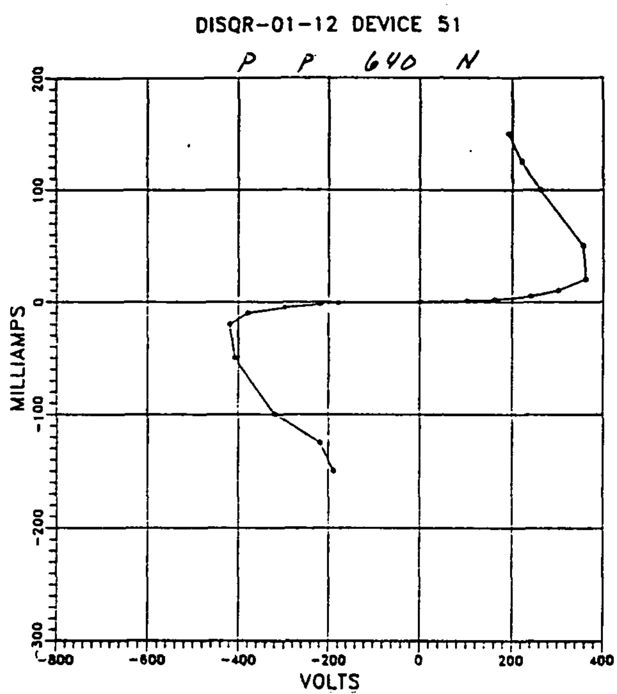

Figure 54. Pulsed I-V with P emitter, P collector, 640 μm emitter-collector space, and N injection gate.

In general, those devices with the larger emitter-collector spacings have the highest threshold voltages (up to 1000 V) and holding voltages.

7.4 LOW HOLDING VOLTAGE WITH LOW THRESHOLD

During the latter part of this program, emphasis was shifted from high threshold voltage and high threshold-to-holding voltage ratios toward those devices which might exhibit low holding voltages. Analysis has shown that these are achieved with initially high-resistivity wafers with light gold doping.

Wafers intended for this purpose are still being characterized. Representative devices from these wafers will be scribed out and mounted in transistor packages for delivery to NASA. The measurement data obtained from these devices will be included in this report as an appendix.

Packages for completed devices were obtained from Powerex, Inc. These have been modified with alumina base plates for insulation of devices from the package base.

8. CONCLUSIONS

Deep-impurity, double-injection $(DI)^2$ devices constitute a unique class of semiconductor switches. Their principle mode of operation is inherently binary, switching from OFF state to ON state without the necessity of external feedback circuitry or auxiliary amplifiers. Their resistance to radiation effects and to high temperature qualify their use in hostile environments where other common semiconductor devices cannot survive.

This program investigated the use of $(DI)^2$ devices as high-power switches. This report has shown, analytically and experimentally, that in high-power applications, the properties of $(DI)^2$ devices are such that they dissipate relatively large amounts of power in the OFF state, and that when they are pushed to those power levels which are required, the heat generated by this power dissipation cannot be removed rapidly enough to prevent device destruction.

It remains to be determined if the unusual properties of $(DI)^2$ operation can be incorporated into other applications which do not involve high power levels.

9. REFERENCES

1. Gosele et al., Appl. Phys. 23, 361 (1980).

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10. ACKNOWLEDGEMENTS

The author wishes to acknowledge the support and guidance of L. R. Lowry, program manager for this investigation. J. B. McNally, J. R. McKee, M. J. Testa, G. A. Madia, W. Cifone, J. M. Bronner, and A. J. Zigarovich all contributed to aspects of device fabrication. R. J. Fiedor designed the electrical test systems and performed the device testing. G. Markle and B. B. Visser patiently typed the reports throughout this program and G. S. Law edited and produced these reports. Dr. Arthur Milnes, of Carnegie-Mellon University, contributed expert advice in aspects of the deep-level analysis.

We would like to acknowledge the patience, understanding, and support of Messrs. Ira Myers and Gale Sundberg of NASA/Lewis throughout the program.

APPENDIX I

BASIC program simulating electron injection into insulating silicon.

```
10 REM                          THIS IS 906DI.BAS
20 LPRINT CHR$(24)                                          'clears print buffer
30 REM     XSEL is the number of excess electrons in the volume which is
40 REM      defined by AREA x DX
50 REM     The base concentration is NB
60 REM     The temperature is TEMP
70 REM     The current is I
80 REM     The length of the device is L
90 REM     The number of sections is N%
100 REM     The time interval is DT
110 REM    The number of electrons flowing into a section is EIN
120 REM    The number of electrons flowing out of a section is EOUT
130 DIM XSEL(100)
140 AREA = 1
150 TEMP = 300
160 CURRENT = 1!
170 NB = 0                                                 '5e12 is 1000 ohm-cm n type
180 N% = 20                                                'number of sections
190 LAST% = 4000                                           'number of time intervals
200 L = .1                                                 'total length of device
210 DT = 1E-11                                             'increment of time
220 DX = L/N%
230 Q = 1.602E-19                                          'electron charge
240 PERM = 8.854E-14*11.8                                  'permittivity of silicon
250 MUE = 1250                                             'low field mobility
260 D = MUE*1.38E-23*TEMP/Q                                'electron diffusivity
270 LPRINT "                ", DATE$, TIME$
280 LPRINT USING "J = ##.#^^^^ AMP/cm^2";CURRENT/(AREA);
290 LPRINT USING "     L = ##.#^^^^ cm";L;
300 LPRINT USING "     DELTAT = ##.#^^^^ sec";DT
310 LPRINT USING "     DELTAX = ##.#^^^^ cm";DX;
320 LPRINT USING "     AREA = ##.#^^^^ cm^2";AREA;
330 LPRINT USING "     NB = ##.##^^^^";NB
340 LPRINT USING "          #### SECTIONS";N%;
350 LPRINT USING "     #### TIME INTERVAL LIMIT";LAST%
360 LPRINT
370 LPRINT "SECT   TIME     EIN        EOUT       ELCONC     FIELD      VOLTS
380 FOR T = 1 TO LAST%
390 IF EOUT > .99*CURRENT*DT/Q THEN LAST% = T
400 PRINT USING "#####";T;
410 PRINT USING "  ##.##^^^^";EOUT;
420 PRINT USING "  ##.##^^^^";CURRENT*DT/Q;
430 PRINT USING "  ##.##^^^^";T*DT
440 FLD = 0
450 VOLT = 0
460 FOR I = 1 TO N%
470 EIN = EOUT
480 IF I = 1  THEN EIN = CURRENT*DT/Q
490 XSEL(I) = XSEL(I) + EIN
500 N1 = XSEL(I)
```

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BASIC - continued

```
510                                            IF N1 < 1! THEN N1 = 0!
520 IF FLD > 1E-09 GOTO 560
530 N2 = N1/(N1*MUE*Q*DT/(AREA*DX*PERM) + 1)
540                                            IF N2 < 1! THEN N2 = 0!
550 GOTO 610
560 A = MUE*FLD/DX - MUE*NB*Q/PERM
570 B = Q*MUE/(AREA*DX*PERM)
580 NUM = A*N1
590 DEN = A*EXP(A*DT) + B*N1*(EXP(A*DT) - 1)
600 N2 = NUM/DEN
610 EOUT = N1 - N2
620 RHON2 = Q*N2/(AREA*DX)
630 RHONB = Q*NB
640 NFLD = DX*(RHON2 - RHONB)/PERM
650 FLD = FLD + NFLD
660 VOLT = VOLT + FLD*DX/2
670 XSEL(I) = N2
680 IF T = LAST% THEN GOSUB 890
690 NEXT I
700 IF LAST% = T GOTO 730
710 IF EOUT >.99*CURRENT*DT/Q THEN LAST% = T
720 NEXT T
730 LPRINT
740 LPRINT "             ", DATE$, TIME$
750 LPRINT USING "I=####"; CURRENT;
760 LPRINT USING "   L=#.##"; L;
770 LPRINT USING "   DELTAT=##.^^^^"; DT;
780 LPRINT USING "   DELTAX=##.^^^^"; DX;
790 LPRINT USING "   AREA=#.##";AREA;
800 LPRINT USING "   NB=##.##^^^^";NB
810 LPRINT USING "                    ##### TIME ITERATIONS";LAST%
820 LPRINT
830 LPRINT
840 LPRINT
850 LPRINT
860 LPRINT
870 LIST 140-210
880 END
890 LPRINT USING " ###";I;
900 LPRINT USING " +#.##^^^^";T*DT;
910 LPRINT USING " +#.##^^^^";EIN;
920 LPRINT USING "  +#.##^^^^";EOUT;
930 LPRINT USING "  +#.##^^^^";XSEL(I)/(AREA*DX);
940 LPRINT USING "  +#.##^^^^";FLD;
950 LPRINT USING "  +#.##^^^^";VOLT
960 RETURN
```

AS A FUNCTION OF TOTAL TIME

I = 1 A   L = 0.1 cm   AREA = 1 cm^2

SECTIONS	dt	TIME	FIELD	VOLTS
20	1E-11	5E-09	4.79E3	2.23E2
	10E-09	9.54E3	3.65E2	
	15E-09	1.17E4	3.95E2	
	17.6E-09*	1.18E4	3.96E2	

*Terminated when current out > .99 X current in

AS A FUNCTION OF LENGTH

I = 1 A   20 SECTIONS   AREA = 1 cm^2

LENGTH	dt	TIME	FIELD	VOLTS
.05 cm	1E-10	1.09E-8	7.19E3	1.24E2
	1E-11	1.2E-8	8.32E3	1.40E2
0.10	1E-11	1.76E-8	1.18E4	3.96E2
0.20	1E-10	2.35E-8	1.56E4	1.06E3
1E-11	2.5E-8	1.68E4	1.12E3	

AS A FUNCTION OF CURRENT DENSITY

LENGTH = 0.1   AREA = 1 cm^2 20 SECTIONS

CURRENT	dt	TIME	FIELD	VOLTS
0.1	1E-10	5.5E-8	3.65E3	1.23E2
	3E-11	5.6E-8	3.75E3	1.25E2
1.0	1E-11	1.76E-8	1.18E4	3.96E2
10	1E-10	4.0E-9	2.59E4	9.34E2
	1E-11	5.5E-9	3.65E4	1.23E3

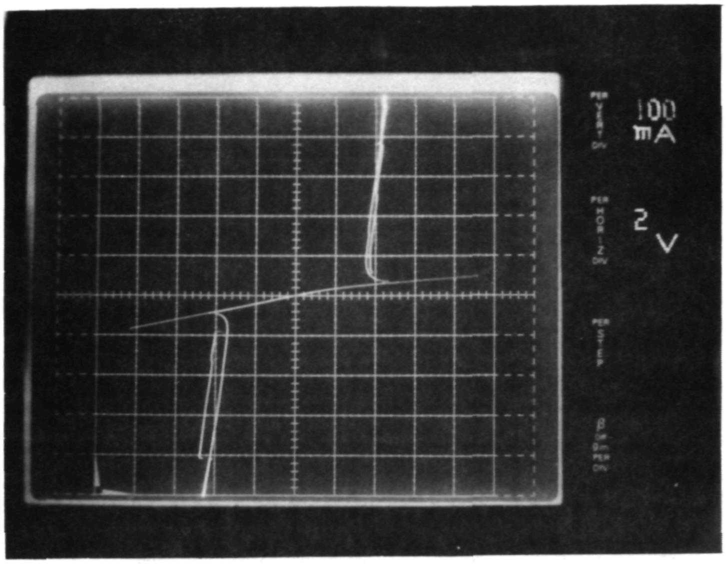
From the above calculations, $J = CV^2/L^3$ so it can be calculated that, for a switch which is 1 mm^2 in area and is to have a threshold voltage of 10,000 V while conducting only 50 mA (current density of 5 A/cm^2), this requires a length of 0.504 cm.

APPENDIX II

A number of devices illustrative of those fabricated during this investigation were mounted and wire bonded to TO-3 headers. These devices were chosen from those lot runs expected to exhibit how holding voltages (with concomitant low threshold voltages). These mounted devices were delivered to the NASA program manager. The electrical characteristics of these devices are shown in the following oscillographs from a Tektronix 576 curve tracer. The accompanying notations refer to the device structure as described in the main body of this report and to noteworthy characteristics of individual devices.

The device emitters were wire bonded to the header case (ground), the gates were bonded to pin "E," and the collectors were bonded to pin "B."

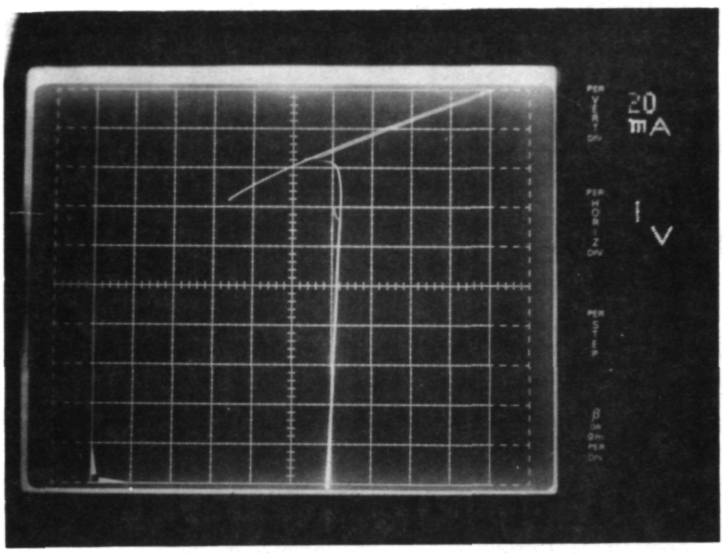
The device parameters of threshold voltage, current at threshold, and holding voltage can be read from the oscillographs. Since gate signals did not significantly change any of these parameters, these tests were performed with gates open (disconnected).



DEVICE 02-9-20

S S 4D ENH

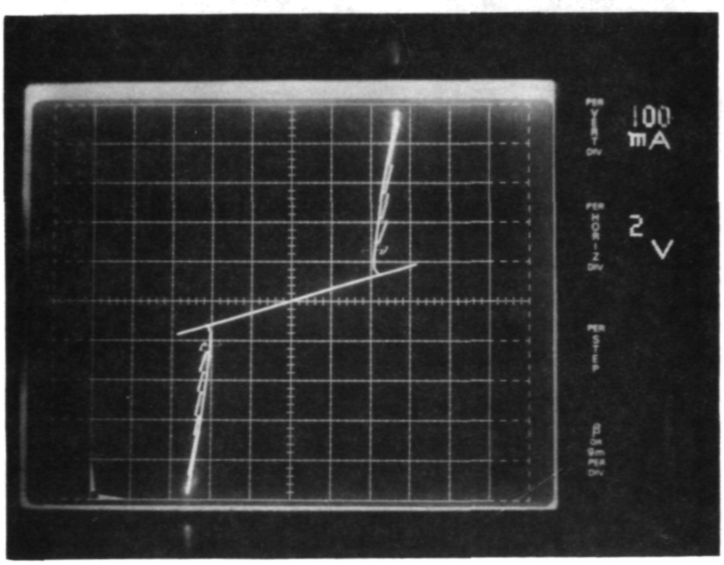
Nearly symmetrical in forward and reverse polarities. Low holding voltage.



DEVICE 02-9-23

P N 160 S

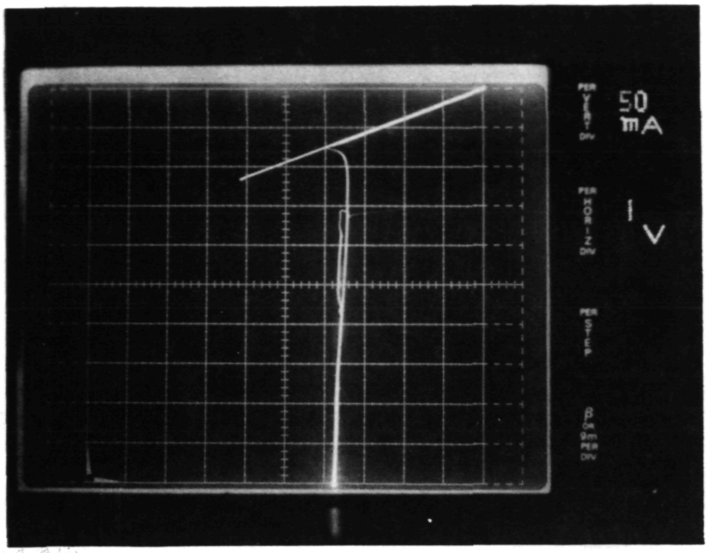
Switches in forward direction only. Low holding voltage.



DEVICE 02-9-46

SD SD 40 ENH

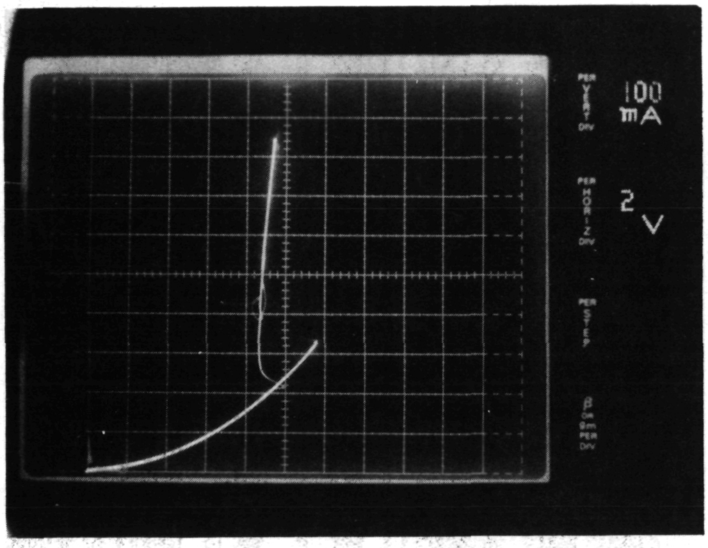
Shieh electrode dots switch serially.



DEVICE 02-9-49

N N 160 S

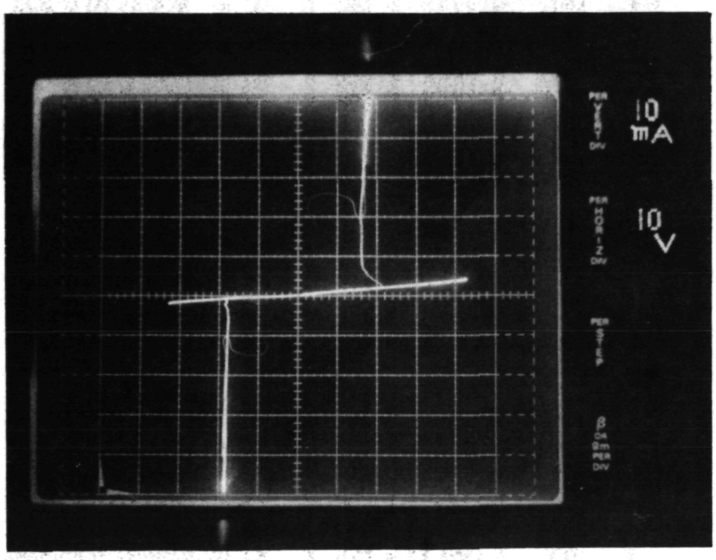
Switches in only one direction.



DEVICE 02-9-68

RS RS 160 S

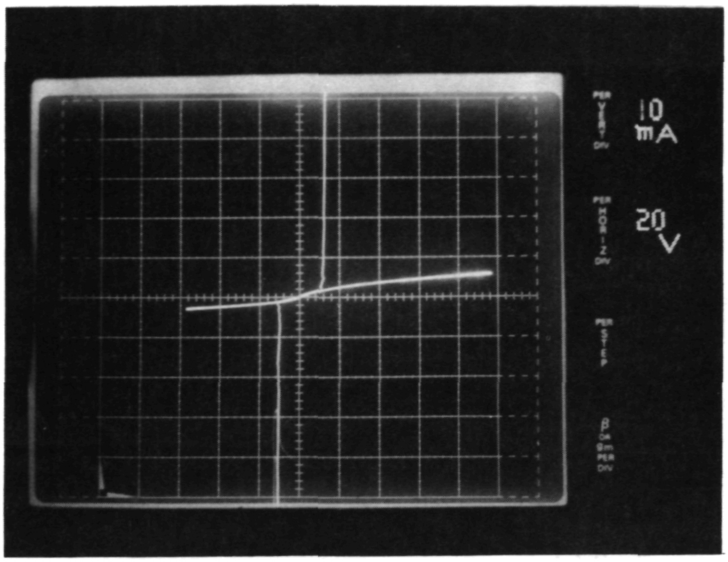
Switches in only one direction.
Super-linear I-V to threshold voltage.



DEVICE 02-10-5

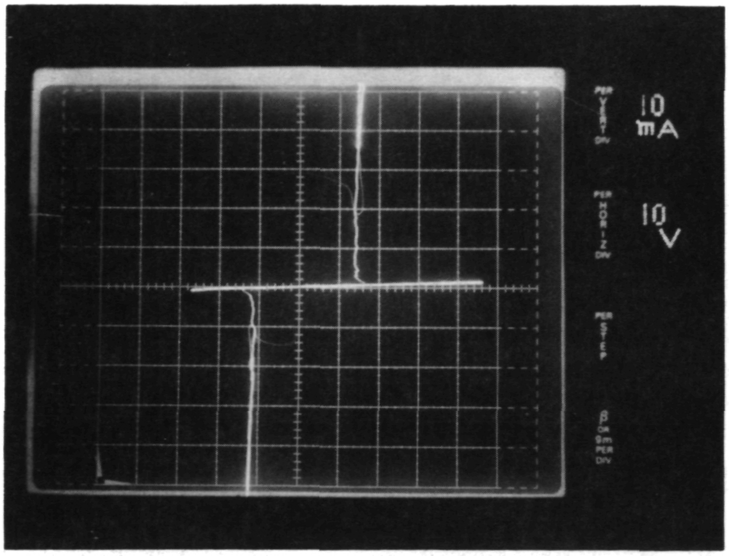
S S 160 NONE

Symmetrical switching.



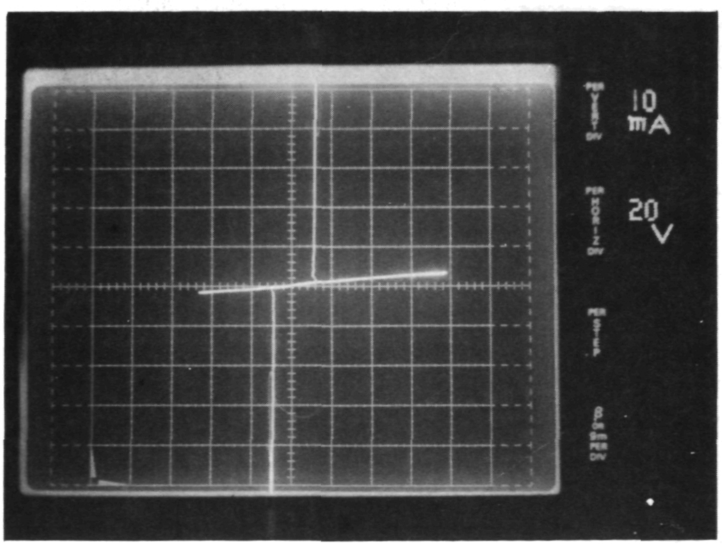
DEVICE 02-10-6
S S 160 NONE

Same structure as 02-10-5 but higher threshold voltage



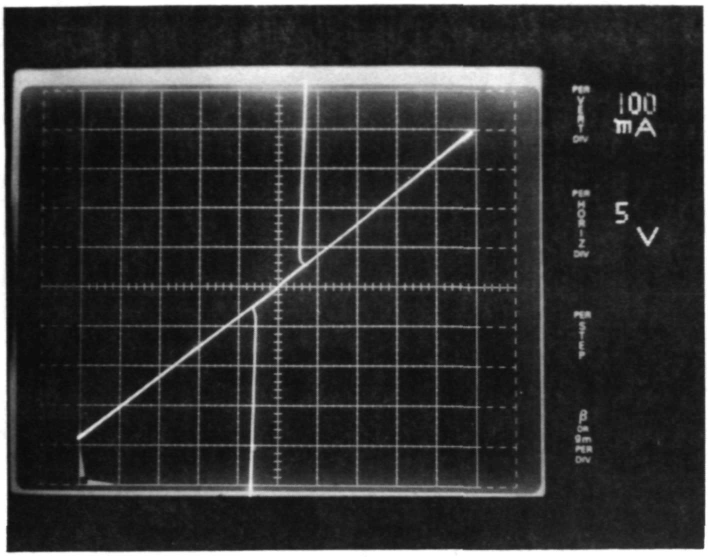
DEVICE 02-10-7
S S 160 NONE

Same structure as 02-10-5 and similar characteristics



DEVICE 02-10-8
S S 160 NONE

Same structure as 02-10-6 and similar characteristics

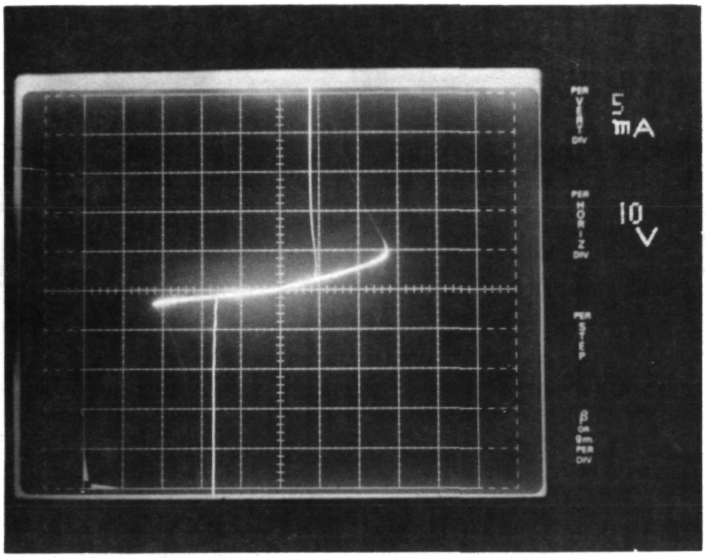


DEVICE 02-10-11

S S 20 ENH

Low threshold voltage.

High OFF state power

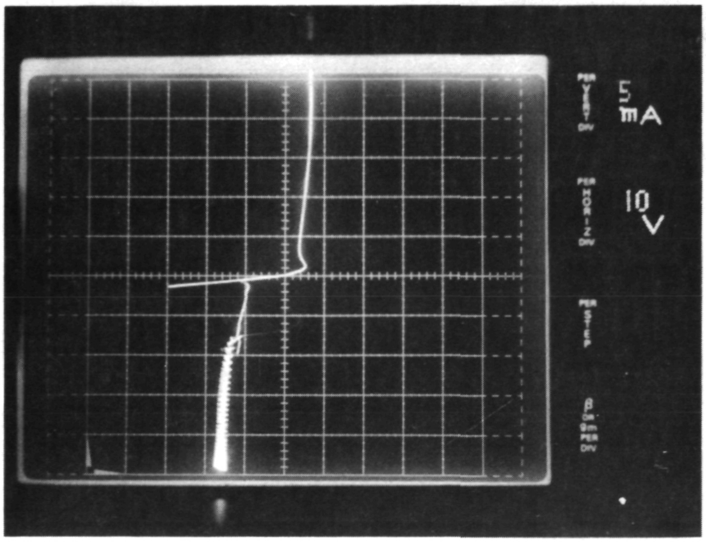


DEVICE 02-10-12

S S 160 DEP

Slow switch in one polarity,

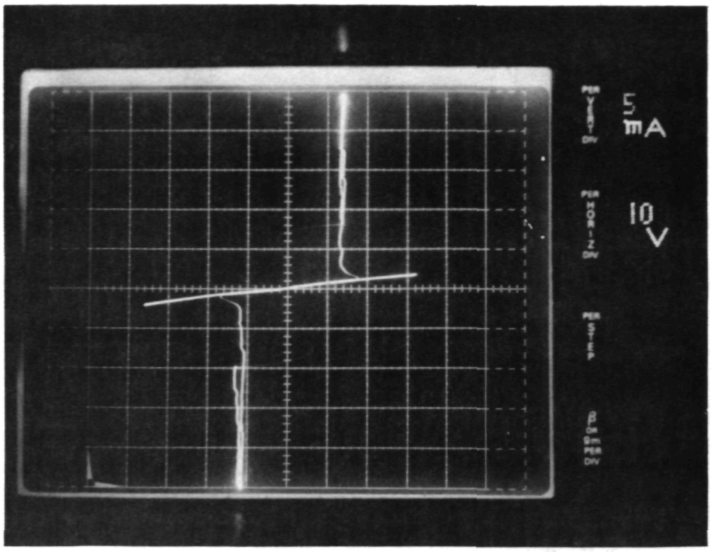
fast in the other



DEVICE 02-10-13

S S 160 S

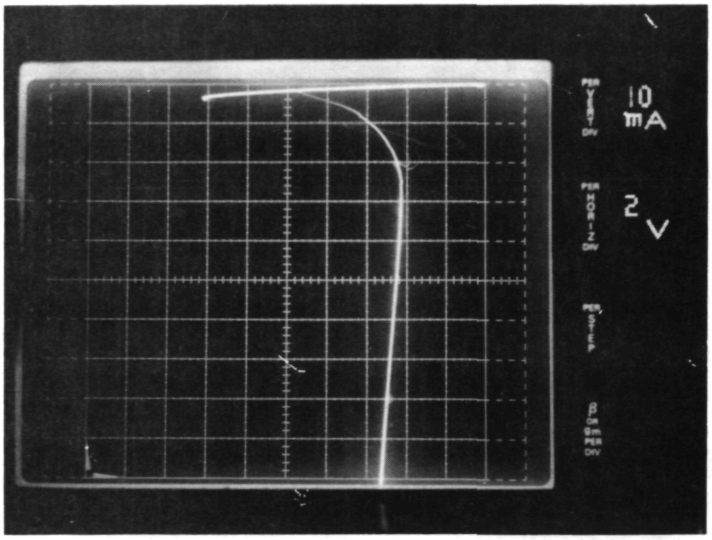
Asymmetric switch



DEVICE 02-10-14

S S 160 P

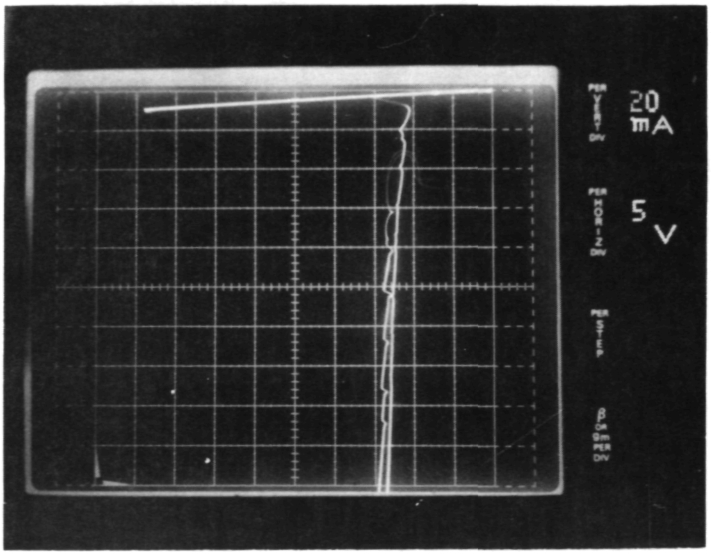
Low threshold to holding voltage ratio.



DEVICE 02-10-27

P N 160 N

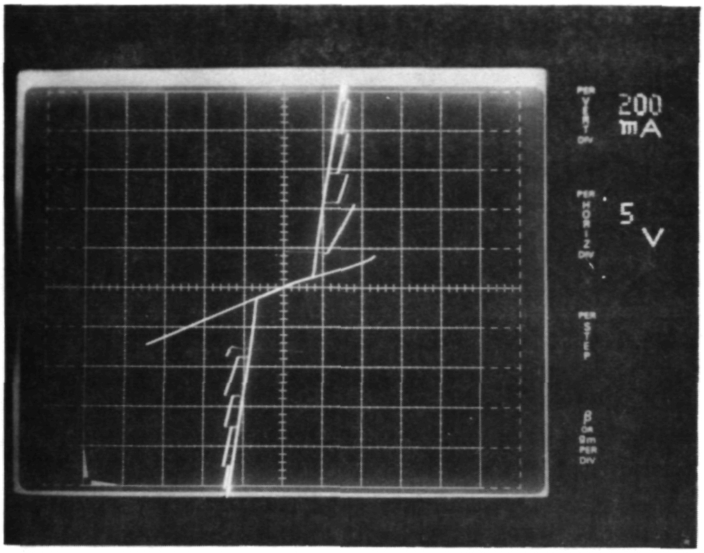
Slow switch. Switches only in forward polarity



DEVICE 02-10-3

PD ND 160 S

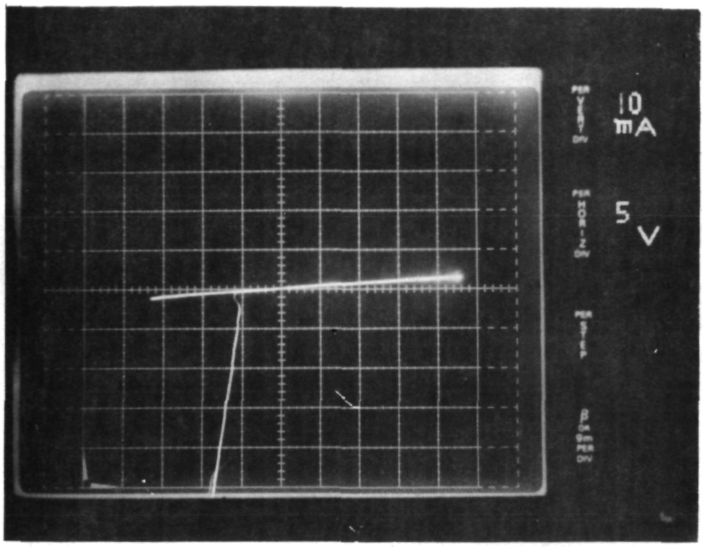
Switches only in forward polarity. Dot electrodes switch serially.



DEVICE 02-10-39

SD SD 20 ENH

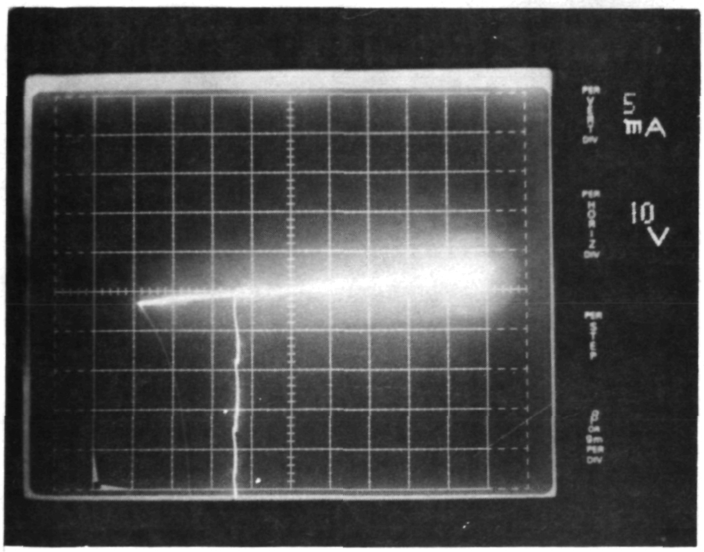
Switches symmetrically. Shieh dots switch serially.



DEVICE 02-10-41

SD SD 160 S

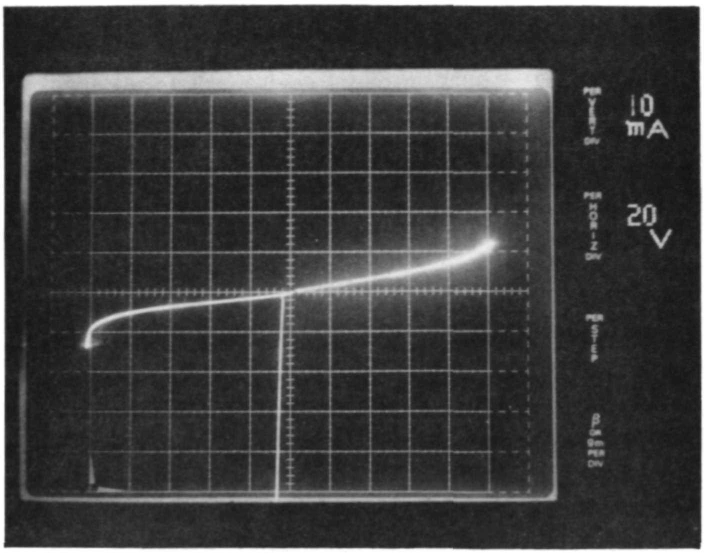
Switches in only one polarity.



DEVICE 02-10-42

SD SD 160 P

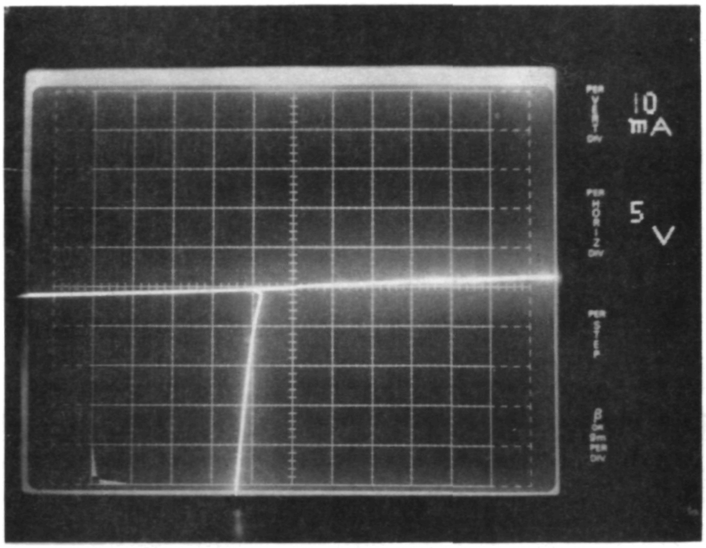
Switches in only one polarity.



DEVICE 02-10-46

SD SD 40 ENh

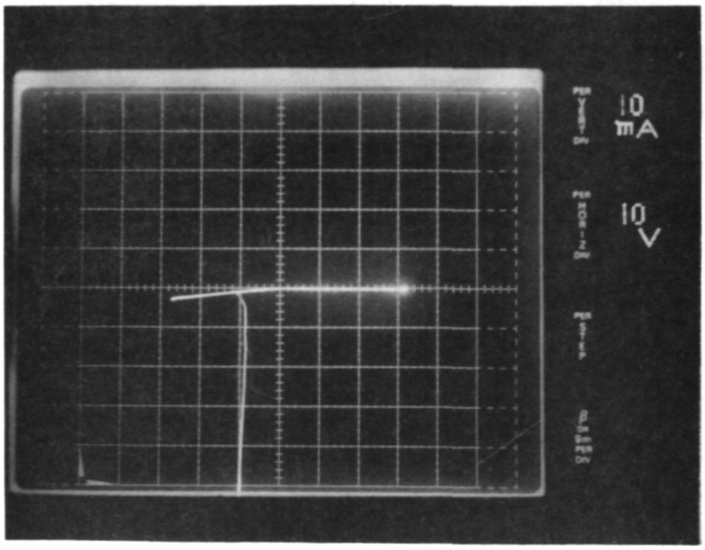
Switches in only one polarity. High threshold to holding voltage ratio.



DEVICE 02-10-46

SD SD 40 ENH

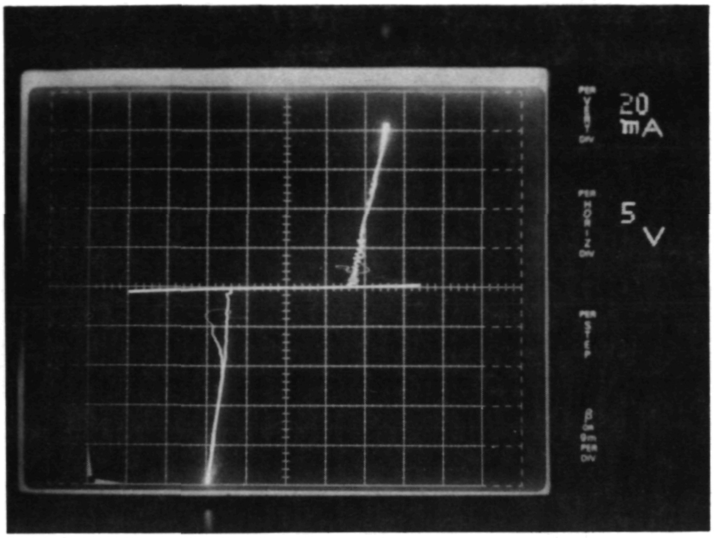
Same device as above. Shows low holding voltage.



DEVICE 02-10-58

P N 160 NONE

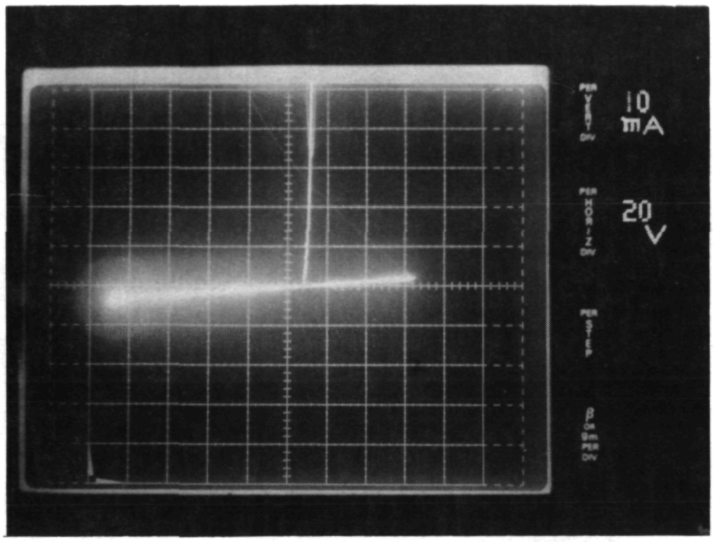
Switches only in forward polarity.



DEVICE 02-10-67

RS RS 160 DEP

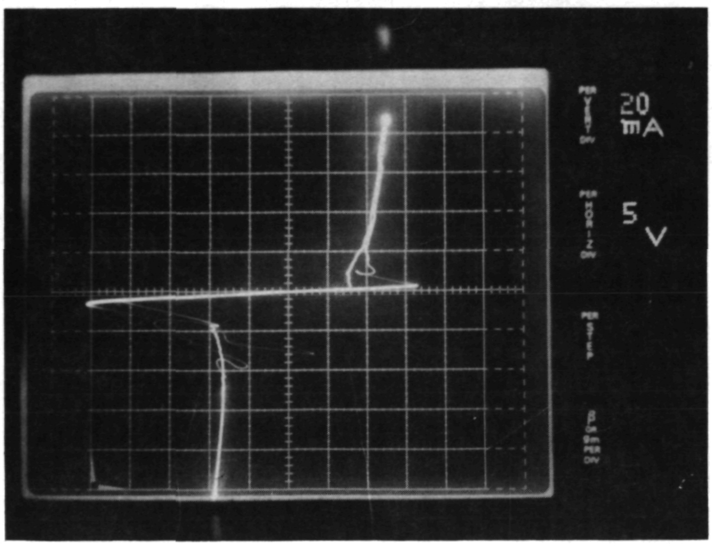
Symmetrical switching.



DEVICE 02-10-68

RS RS 160 S

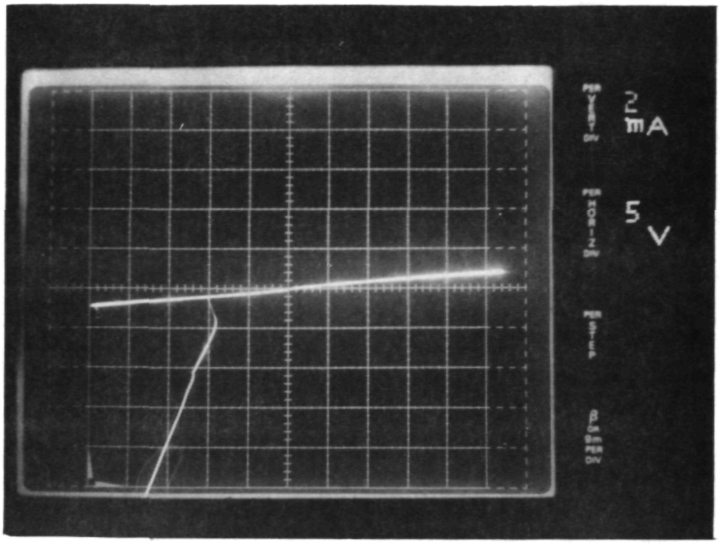
Switches in only one polarity.



DEVICE 02-10-70

RS RS 160 N

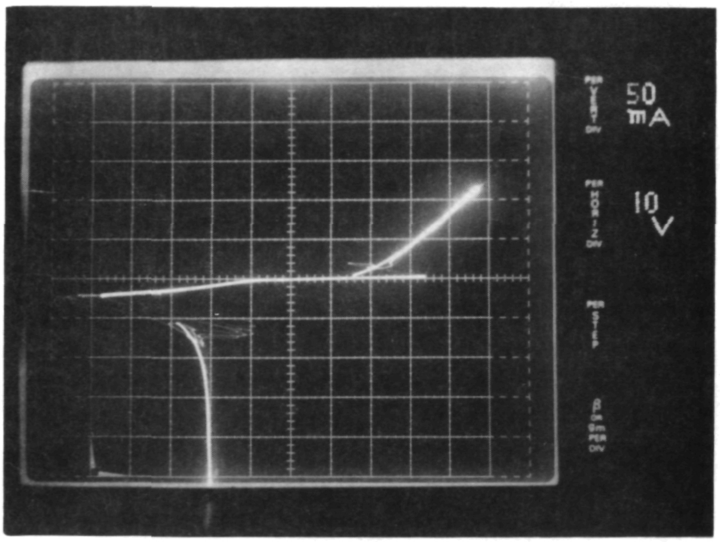
Symmetrical, slow switching.



DEVICE 02-10-73

ND ND 160 S

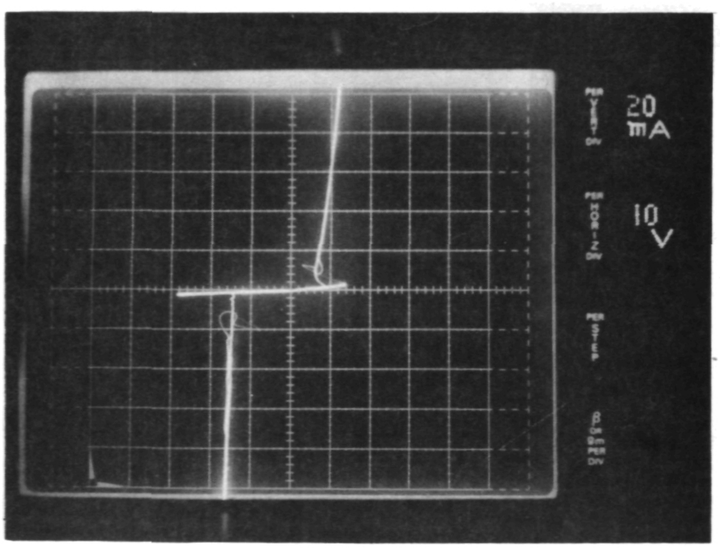
Switches in only one polarity.
High ON resistance.



DEVICE 02-10-74

ND ND 160 P

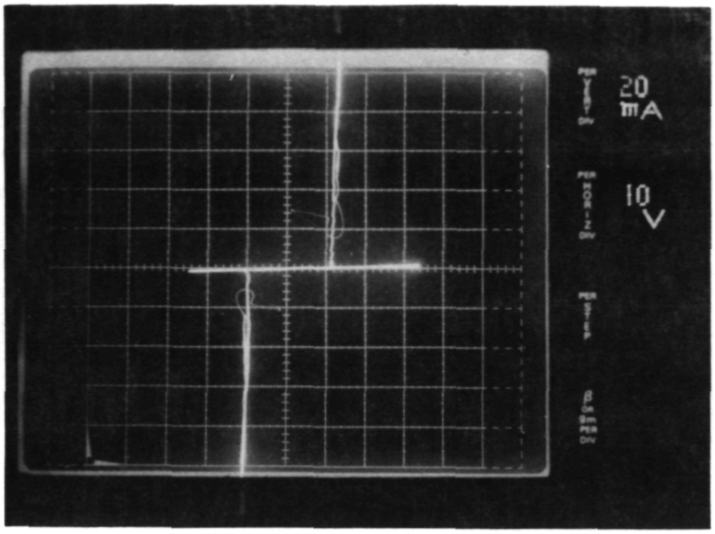
Asymmetric in ON and OFF state resistance.



DEVICE 02-11-5

S S 160 NONE

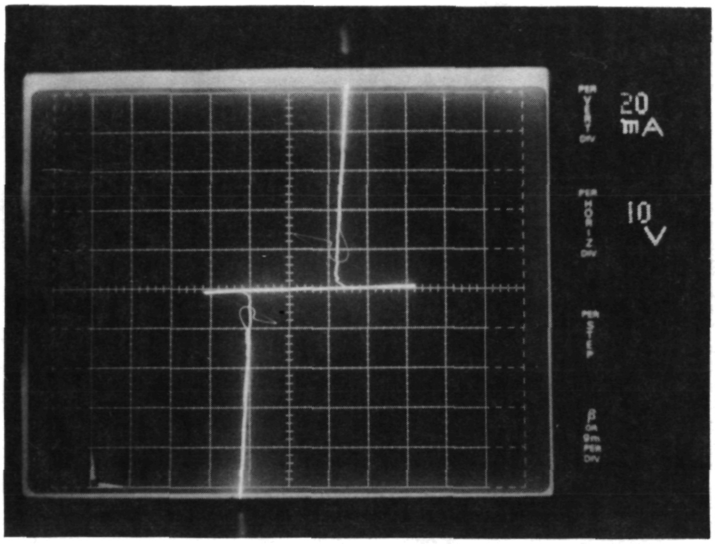
Symmetric switching.



DEVICE 02-11-6

S S 160 NONE

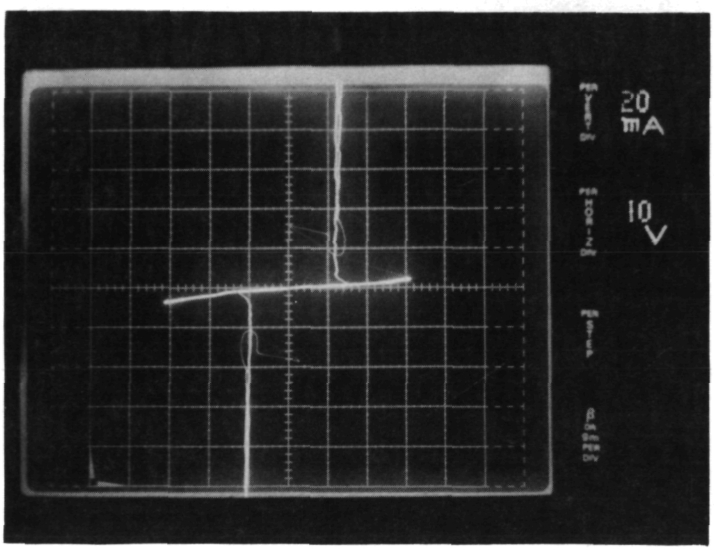
Symmetric switching. Low ON state resistance.



DEVICE 02-11-7

S S 160 NONE

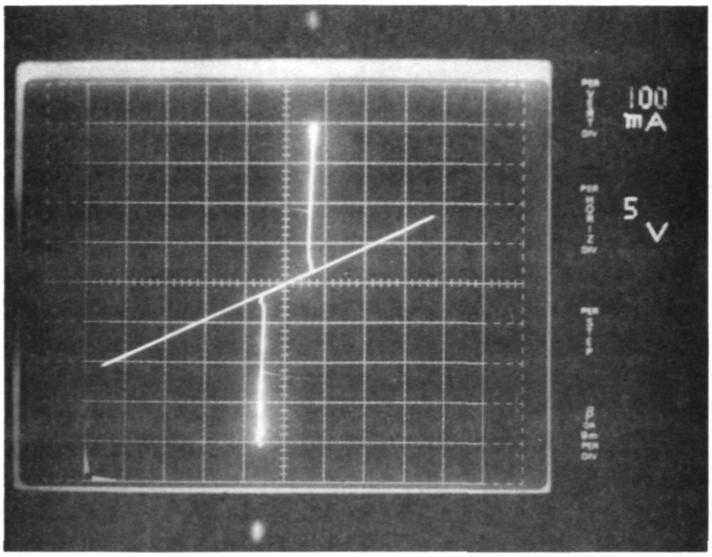
Same structure as 02-11-6. Similar characteristics.



DEVICE 02-11-8

S S 160 NONE

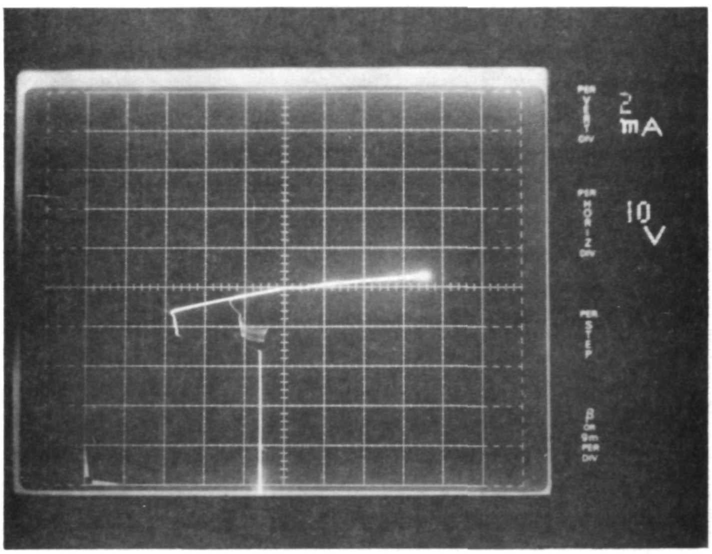
Same structure as 02-11-6. Similar characteristics.



DEVICE 02-11-11

S S 20 ENH

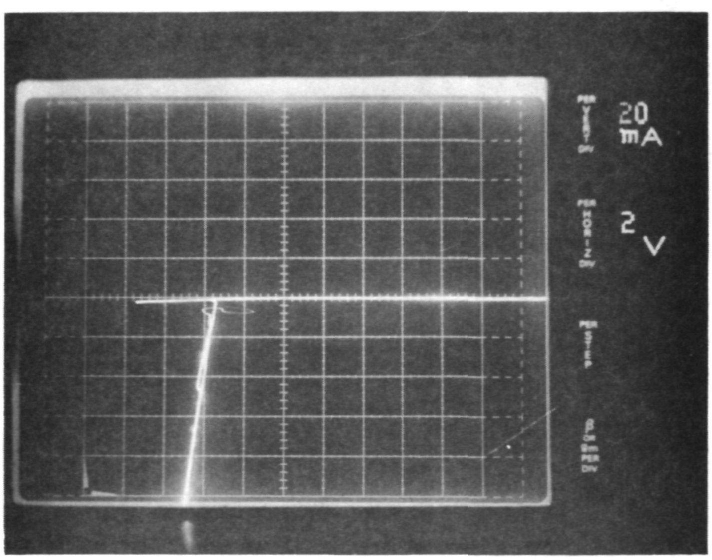
Low threshold voltage, high OFF state power. Consistent with 20 μm spacing.



DEVICE 02-11-13

S S 160 S

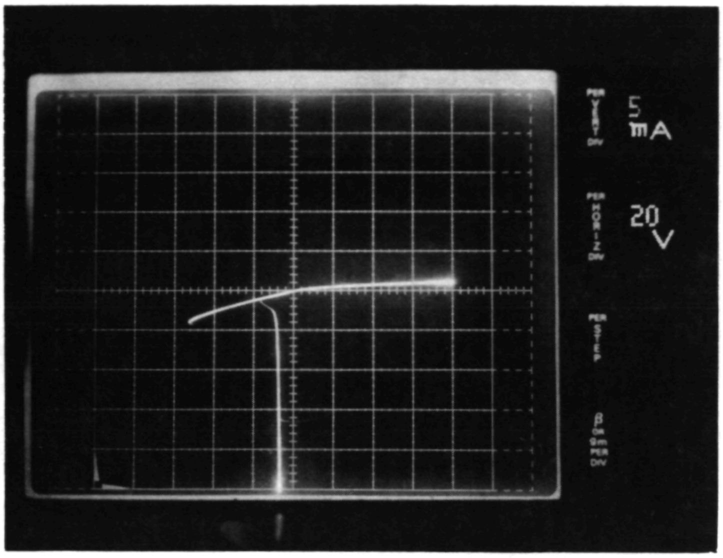
Switches in only one polarity.



DEVICE 02-11-22

P N 160 DEP

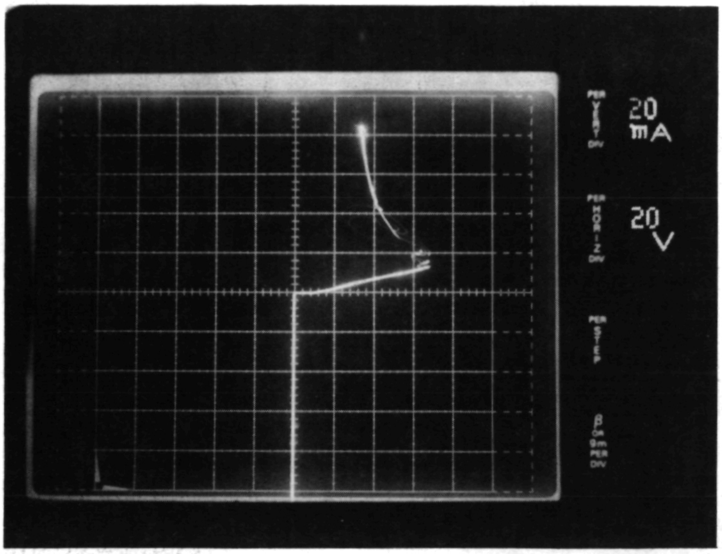
Switches in only forward polarity. Low holding voltage.



DEVICE 02-11-27

P N 160 N

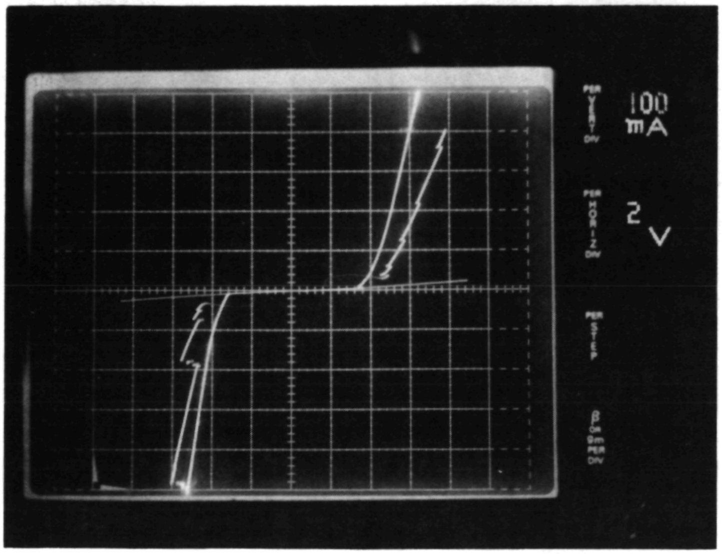
Switches only in forward polarity.



DEVICE 02-11-31

PD ND 20 ENH

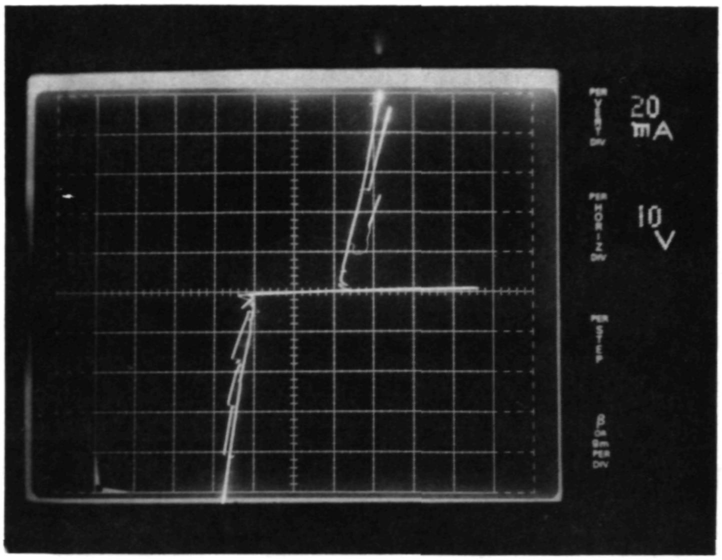
Slow switching in reverse polarity.



DEVICE 02-11-39

SD SD 20 ENH

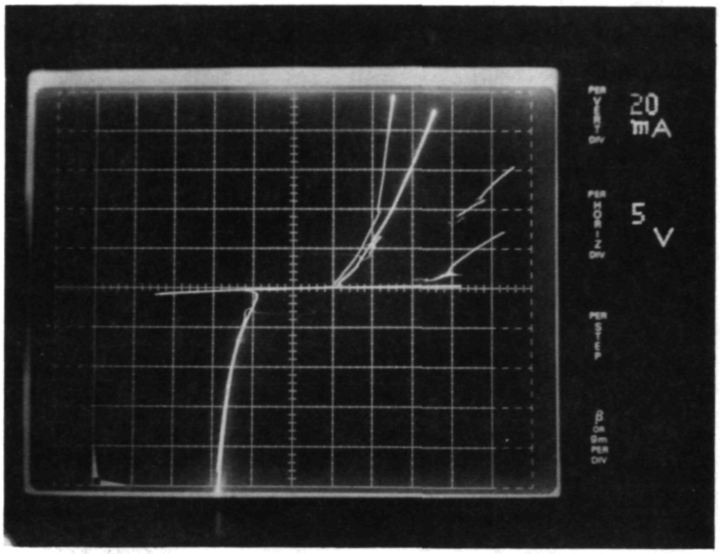
Symmetric switching. Low threshold voltage. Shieh dots switch serially.



DEVICE 02-11-40

SD SD 160 DEP

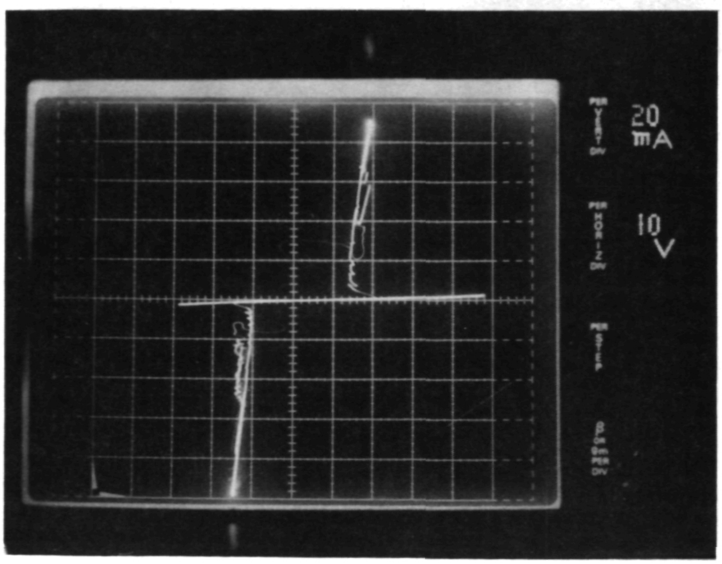
Asymmetric threshold voltage.
Shieh dots switch serially.



DEVICE 02-11-41

SD SD 160 S

Shieh Dots switch serially.



DEVICE 02-11-42

SD SD 160 P

Shieh dots switch serially.

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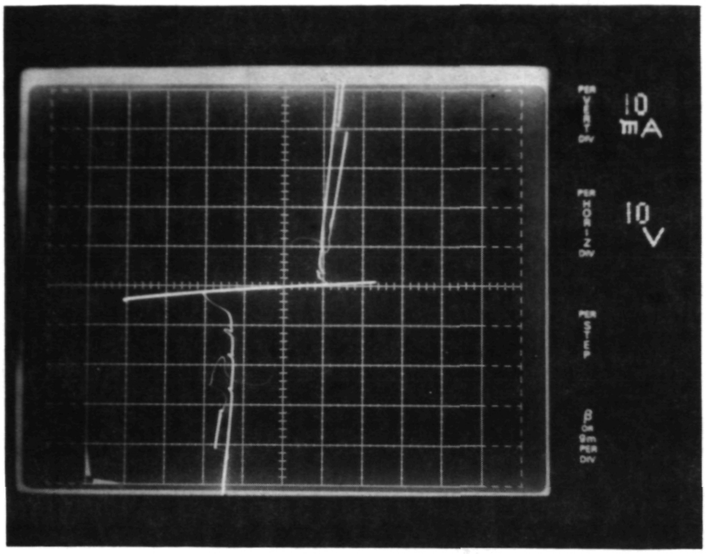
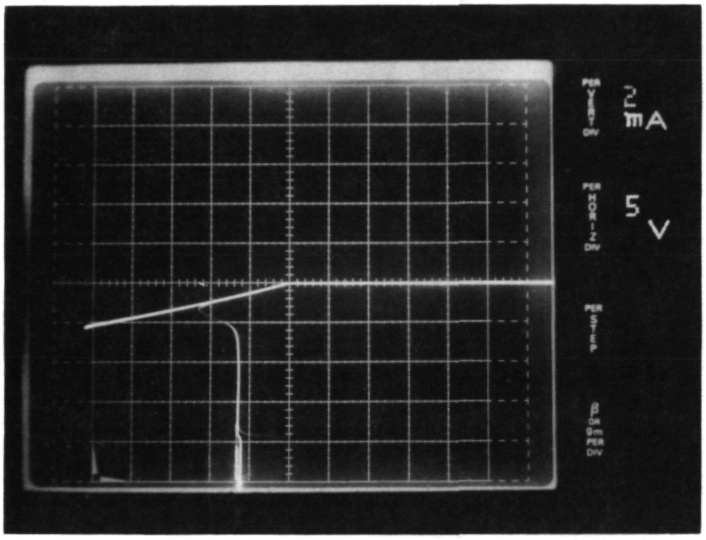


DEVICE 02-11-43

SD SD 160 N

Shieh dots switch serially.



DEVICE 02-11-58

P N 160 NONE

Switches only in forward polarity.

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