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DEVELOPMENT OF A CODED 16-ARY CPFSK COHERENT DEMODULATOR

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ABSTRACT

Theory and hardware are described for a proof-of-concept 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK) digital modem. The 16 frequencies are spaced every 1/16th baud rate for 2 bits/sec/Hz operation. Overall rate ¾ convolutional coding is incorporated. The demodulator differs significantly from typical quadrature phase detector approaches in that phase is coherently measured by processing the baseband output of a frequency discriminator. Baud rate phase samples from the baseband processor are decoded to yield the original data stream. The method of encoding onto the 16-ary phase nodes, together with convolutional coding gain, results in near QPSK performance. The modulated signal is of constant envelope; thus the power amplifier can be saturated for peak performance. The spectrum is inherently bandlimited and requires no RF filter.

MODEM OVERVIEW

We discuss a bandwidth efficient constant envelope modem: 16-ary Continuous Phase Frequency Shift Keying (16-CPFSK). Error-correction coding is applied to reduce the performance disadvantage relative to AM schemes. The modem is designed for 200 mb/s TDMA application with 100 mHz adjacent channel spacing.

Theoretical Considerations

Two novel theoretical techniques are used in this 16-CPFSK modem: I) coherent phase measurements obtained by processing an FM discriminator baseband output; II) Modulation via a closed-loop linearized VCO. Refer to Figure 1 in the following discussion.

Obtaining coherent phase from a discriminator. A discriminator outputs $\phi'(t)$, where $\phi(t)$ is the signal's phase modulation. Integration of $\phi'(t)$ recovers the desired signal, $\phi(t)$. Implementation of the integration has several practical problems: 1) Integrator output can grow without bound; 2) Initial phase, $\phi(0)$, must be determined; 3) AGC is needed on the baseband signal. Regarding problem 1), fortunately, we need only know phase Mod-2π. Thus the growth problem is avoided by integrating Mod-2π. How can such an integrator be implemented? It is essential only that we obtain $\phi(nT)$, phase at baud time intervals. An integrator yielding ϕ(nT) can be implemented as a T-interval Integrate-and-Dump (I&D) sampled by an A/D which feeds a digital accumulator that rolls over Mod-2π. The I&D is actually a lowpass Half-Nyquist filter in this modem, but the conceptual picture remains useful.

Problem 2)--acquiring initial unknown phase, $\phi(0)$, is handled by first observing for each baud time, the phase error to the closest one of the 16-CPFSK phase nodes (Mod-2π) equally spaced in the accumulator. This phase error is filtered by a lowpass loop filter whose output is subtracted from the

accumulator input. The initial phase error, $\phi(0)$, appears as a DC component of the error and is eliminated by the baseband loop. Frequency offset (DC offset from the discriminator) also is eliminated by this baseband loop, the equations for which are identical to those for a PLL.

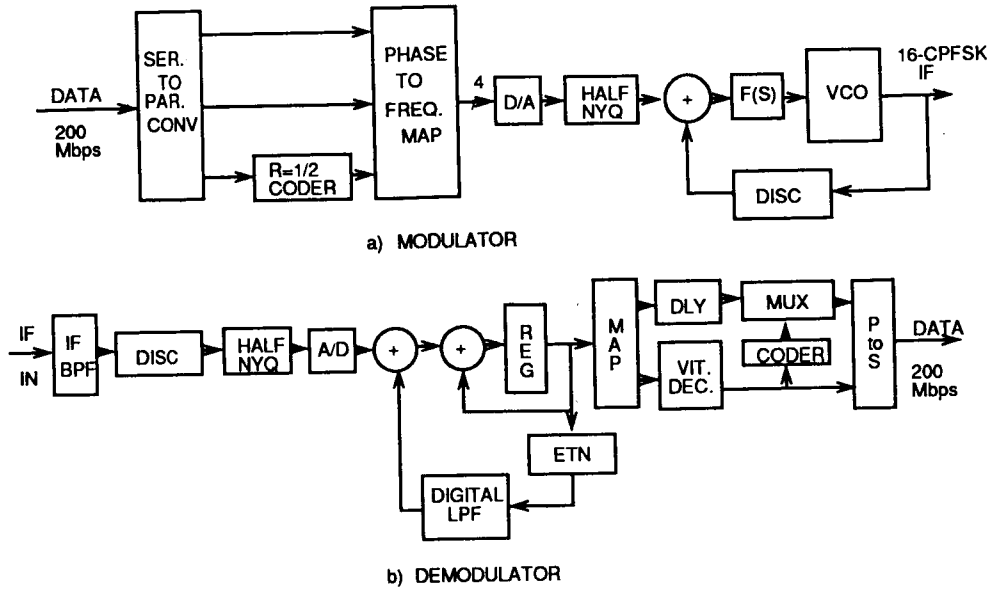

Fig. 1. Basic modem block diagram

Problem 3), AGC, is handled as shown in Figure 1. The accumulator phase error is correlated with input samples, and baseband gain is adjusted to zero the correlation.

Linearized VCO modulator. Figure 1 shows the closed-loop-linearized VCO modulator. The baseband filter output is applied through a feedback summer to the VCO. F(s) is a wideband loop filter. The output of the VCO is immediately converted back to baseband by the discriminator (DISC) and subtracted from the baseband input modulating signal to generate a correction signal in the closed loop. The VCO is thus modulated with small error between the baseband modulating signal and the output of the DISC. If the modulator DISC is identical to the demod DISC, this modulator linearizes the baseband signal path through the modem's VCO/DISC combination.

Brief Description of Modem Operation.

As shown in Figure 1, incoming data is split into 3 parallel bit streams. The 2 MSBs are passed unaltered to modulator MSB positions. The LSB bit stream is coded by a rate ½, K=7 convolutional encoder. The 2 resulting coded branch bits go to the 2 LSB positions of the modulator. The 4 bits produced by this encoding process specify one of 16 symbol-ending phases (Mod-2π) from the 16-CPFSK modulator. Half-Nyquist filtering is employed at the VCO baseband on 16-ary impulses to produce the IF signal at the modulator. At the demod the IF signal is filtered and passed to the DISC. The DISC baseband signal is Half-Nyquist filtered and sampled at symbol rate by an 8-bit A/D. The Half-Nyquist filter completes shaping begun at the VCO, producing an overall Nyquist response to 16-ary impulses. The A/D samples feed the accumulator, whose output is $\phi(nT)$. These phase samples feed a Viterbi decoder for demodulation of the original 3 data streams.

Figure 2 shows the 16-CPFSK phase nodes, along with the mapping of coded 4-bit groups onto them. Any set of 4 adjacent phases contains all 4 rate ½ code branches and has good distance structure. This fact forms the basis for our decoding strategy, to wit: retain only the 4 phase nodes nearest the received coherent phase measurement; then let the Viterbi decoder determine which of these 4 phases is most likely to have been transmitted. The 2 modulator MSBs associated with the decoder's decision are output as 2 of the decoded bits. The third bit decision is the data bit decision made by the decoder. These 3 bits form the total output data bit stream.

Figure 3 shows performance predicted for the coded 16-CPFSK modem.

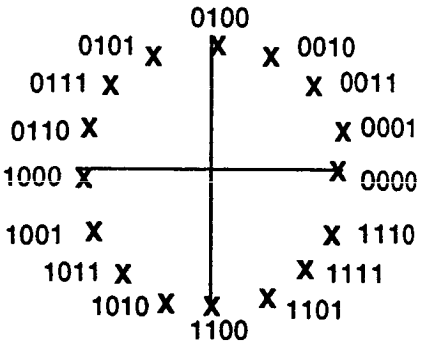

Fig. 2. 16-CPFSK phase nodes.

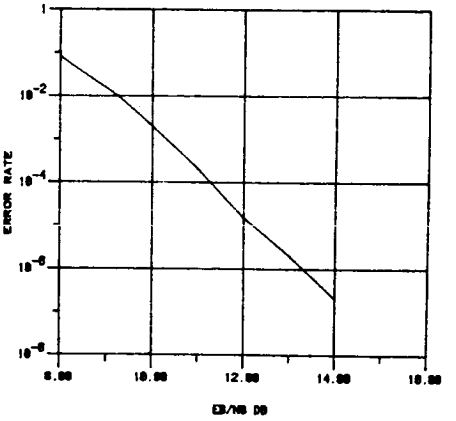

Fig. 3. Modem performance.

DIGITAL BASEBAND PROCESSING

We now discuss the Coherent Baseband Phase Detector (CBPD) hardware. Figure 4 depicts the four major functional portions of the CBPD circuitry: 1) Baseband Preprocessor, 2) Phase Accumulator/DC Restore Loop, 3) AGC Loop, and 4) Timing and Control.

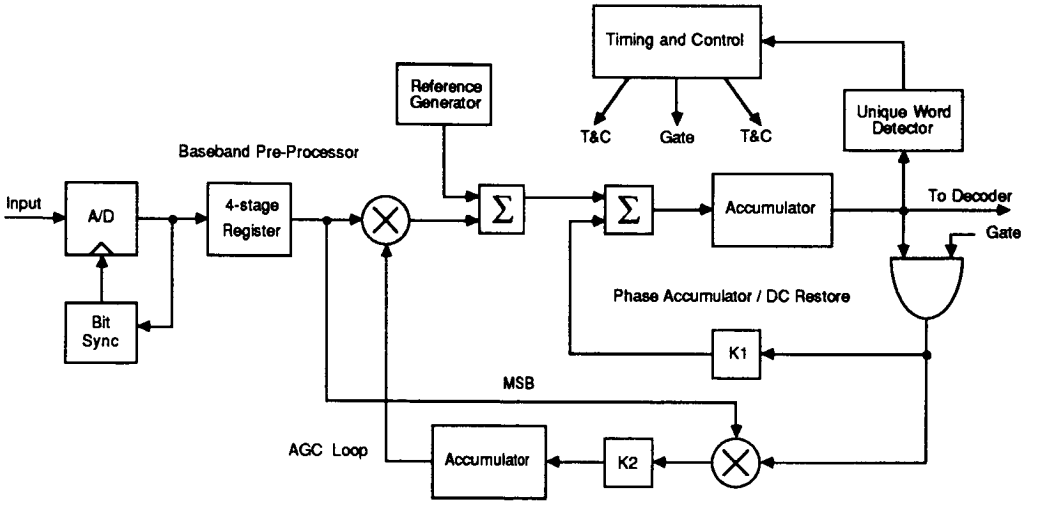

Fig. 4. Coherent Baseband Phase Detector.

Baseband Preprocessor

The filtered (Raised Cosine, 25% excess bandwidth) output of the frequency discriminator is sampled at symbol rate by an 8-bit A/D converter. The samples are sequentially stored in 4 registers to allow detection of an "all f_0's" portion of the TDMA preamble. If detected, the remaining registers in the phase detector circuitry operate normally; otherwise, these registers are asynchronously held low. The output of the fourth register, along with a 16-bit attenuation factor, K, are input to a 16 × 16 ECL multiplier, which provides AGC on any gain variation at the output of the limiter/discriminator (± 6.25% max.). At the output of the multiplier, a binary number is added to the 12-bit two's complement product such that when an f_0 is received, zero is output to the phase accumulator circuit.

Phase Accumulator/DC Restore Loop

An error term, proportional to DC offset in the discriminator output (which results from frequency offset in the IF), is subtracted from the 12-bit number output from the baseband preprocessor. The "DC restored" value is then accumulated by a 12-bit accumulator, completing the implementation of an integrator. The output of the 12-bit accumulator represents 360° of coherent phase (Mod-2π).

The DC restore loop is constructed in the following fashion. During the data portion of a burst (following the preamble and unique word), the transmitted phase constellation is restricted to that of 4-ary signalling (90° spacing) on every fourth transmitted symbol (called a "tracking" symbol). During the tracking symbols, the 10 LSBs, of the accumulator output, directly represent the error in hitting a phase node (error-to-node). Thus, a modulo 90° (±45°) phase detector characteristic is displayed by the 10 LSBs of accumulator output during the tracking symbol. To control DC offsets out of the discriminator, the error-to-node is multiplied by a gain factor, KL, and subtracted from the input to the coherent phase accumulator. This processing is equivalent to a 1st-order PLL correction. For a 1st order control loop with open loop gain, K, the loop noise equivalent bandwidth is given by: $B_L = K/4$ (Gardner, 1979). During the data portion of a burst, with KL = 1/4, and corrections being applied to the loop on every fourth symbol, $B_L = R_S/64$ MHz, where R_S = the symbol rate.

Phase acquisition for independent bursts is accomplished during the all-f_0's portion of the preamble. Initially, the phase accumulator is zeroed. After the all-f_0's portion of the preamble has been detected by the Baseband Preprocessor, the DC restore loop is allowed to update during every symbol interval (providing maximum loop gain, and thus wide loop bandwidth). This processing acquires $\phi(0)$ and initial DC offset at the discriminator output. Since the loop corrects on every symbol, the loop gain is four times that of the "tracking" loop gain, and thus, $B_L = R_S/16$ MHz. Transport delay in the digital control loop is minimized to maintain stable closed loop response for wide loop bandwidths.

AGC Loop

An error term, proportional to gain missetting, is derived by correlating a delayed version of the discriminator sign output with the error-to-node signal. The gain error is filtered by a digital accumulator, and a detector bias (1.0) is added at the accumulator output. The resulting AGC correction factor, KA, is 1 ± 0.0625. The input to the CBPD circuit is scaled by KA using a 16×16 ECL multiplier. Thus, fine decision-directed AGC is provided, which prevents "walkoff" of the coherent phase accumulator.

The loop bandwidth of the AGC loop is given by; $B_L = K/4$, where K = Open Loop Gain. During the all-f_0's portion of the preamble, the AGC loop updates on every symbol and the open loop gain is $R_S/16$. Like the DC Restore loop, the AGC loop updates on every fourth symbol during tracking, so that the open loop gain is ¼ that of acquisition. Thus, $B_L = R_S/64$ during acquisition and $B_L = R_S/256$ during tracking.

Timing and Control

The major portion of the baseband timing control circuit is the Unique Word (UW) detector. The UW consists of six unique symbols immediately following the preamble. The UW is detected when the 6 symbols fill the UW detector correlator cells, allowing one symbol error. The UW, when detected, establishes a second level time tick for burst processing (first level is symbol synchronization). The UW detector establishes the gating clock used to update the control loops on every fourth symbol during the data portion of a burst.

BASEBAND ENCODER/MODULATOR

In the baseband encoder, the data stream (at 200 Mbps) is partitioned into 3-bit symbols. The two MSBs are used directly, and the LSB is rate ½, K=7 convolutionally encoded to produce a 4-bit symbol. This overall rate ¾ code, combined with the CPFSK characteristic, promotes good bandwidth efficiency.

With 3-bit symbols, the symbol rate is reduced to 1/3 the 200 Mbps data bit rate, allowing use of off-the-shelf ECL and eliminating need for custom ICs or GaAs technology.

Figure. 5 shows a block diagram of the encoder/modulator. The input data buffer translates the 200 Mbps serial data stream into a parallel 11-bit word, allowing the input data RAM to operate at 1/11th of the input bit rate. The ECL RAM input buffer is configured as a FIFO. After buffering, the data is read out of the FIFO and partitioned into three, 3-bit groups, and one 2-bit group. Each 3-bit group is operated on as previously described (2 MSBs unaltered; LSB R=½ encoded) to produce 4-bit coded symbols. The remaining 2 bits are treated as MSBs and two zero bits are appended to form the fourth 4-bit symbol. This is done as previously described to aid the demodulator in maintaining carrier lock.

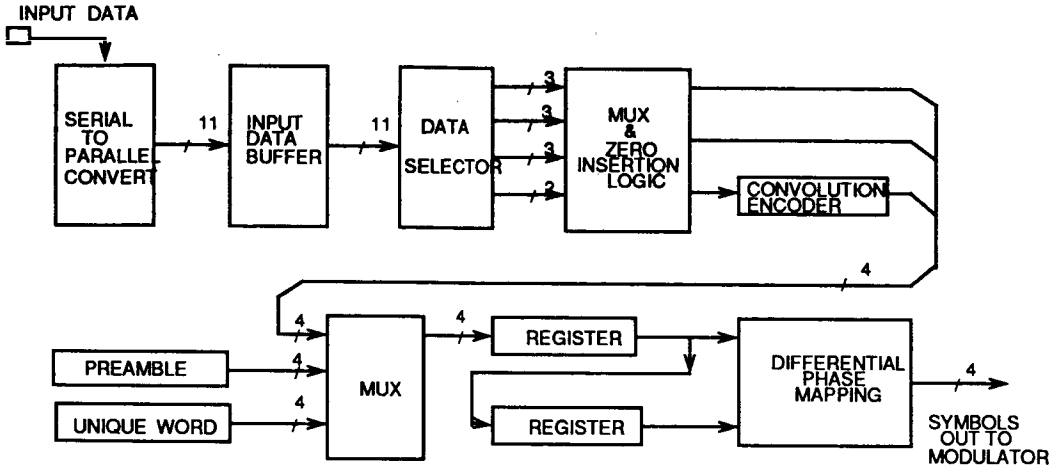

Fig. 5. Encoder block diagram.

Preamble/Unique Word

Prior to sending data, a TDMA preamble is sent. The preamble is a 32-symbol pattern alternating between the two peak frequencies of the 16-CPFSK signal, followed by 32 symbols of lowest frequency, which allows symbol synchronization and coherent phase acquisition.

A 6-symbol unique word to flag start-of-data follows the preamble. Encoded data symbols immediately follow the unique word. The preamble, unique word, and encoded data are all selected via the mux function shown in Figure 5.

Symbol Mapping

With CPFSK, transmitted frequency symbols convey "differential" phase information rather than absolute phase. For example, if the previous encoded 4-bit symbol produced a phase value of Φ_5 and the next 4-bit symbol represented phase Φ_{10}, then the modulated frequency sent out for the current symbol time is that needed to swing phase from Φ_5 to Φ_{10}. The mapping function shown in Figure 5 provides this operation. Two registers address the mapping PROM. One contains the previous 4-bit encoded symbol and the other contains the current 4-bit symbol. This provides the mapping PROM with sufficient information to determine the required frequency to transmit such that the received phase point will be that specified by the current 4-bit symbol.

Encoder Termination Sequence

At the end of the input buffered data, six zeroes are appended to the data stream sent to the convolutional encoder. This forces the encoder to start and end in state 000000 each TDMA burst. At the receiver, the Viterbi decoder function exploits this *a priori* knowledge by forcing the decoder to begin in state 000000 on every burst.

BASEBAND DEMODULATOR

Major baseband demodulator functions are highlighted in Figure 6. The 7-bit phase measurements, as received from the CBPD, are rate buffered and sent to the mapping function, which determines the 4 signal phase points closest to each demodulated value. This homes in on a quadrant of adjacent phase points retained as likely decision candidates.

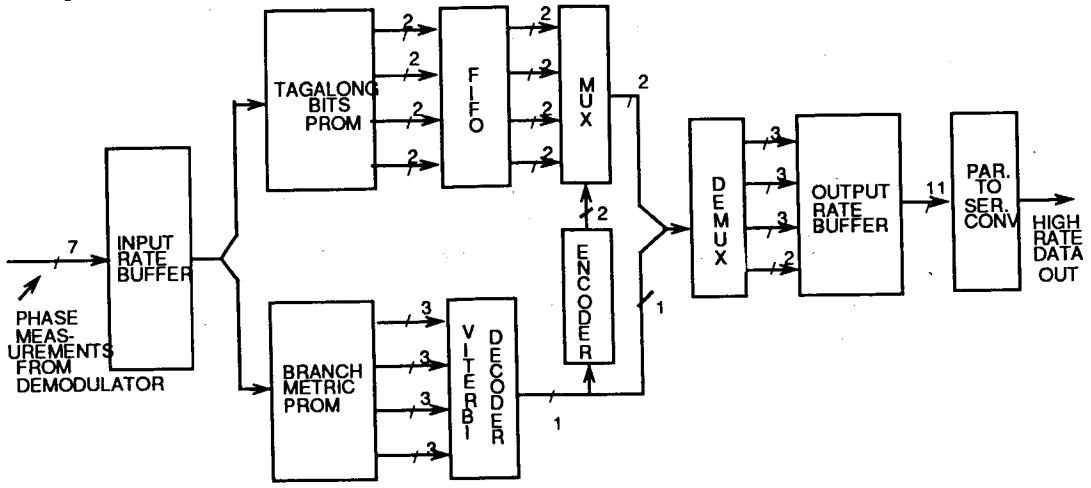

Fig. 6. Decoder block diagram.

The phase distances of these 4 candidate nodes from a given demodulated phase point serve as branch metrics to the Viterbi decoder for the four (00, 01, 10, 11) LSB R=½ code-branch bit pairs. The decoder uses these metrics directly to determine which of the four candidates was most likely transmitted.

As noted already, ANY four consecutive nodes in the signal constellation always contain the values 00, 01, 10, an 11 for the encoded LSB portion; and the two unencoded MSBs simply "tag along" with the respective encoded LSB values. These MSB tag-along bits are sent to a FIFO buffer whose length equals the throughput delay of the Viterbi decoder.

Viterbi Decoder

The four candidate branch metrics described above are fed directly into a R=½, K=7 Viterbi decoder to recover the coded third of the total data bit stream. The decoder output data is then re-encoded to produce an error-corrected 2-bit symbol pair (code branch). This pair selects the corresponding tag-along MSB bit pair from the tag-along FIFO. These tag-along MSB bits are regrouped with the corresponding output data bit from the Viterbi decoder to form the recovered 3-bit data group.

Final Processing

The recovered 3-bit data groups are collected. On every fourth group, only two tag-along bits are recovered (because the LSBs were forced to 00 back at the encoder to support phase tracking). In addition, the 000000 coder termination sequence is removed from the recovered data bit sequence.

The recovered data bits are then rate buffered in another FIFO whose output is then parallel-to-serial converted. This reconstructs the original data stream at the original high speed data bit rate (200 Mbps).

Parallelism in the design of the encoder/modulator and decoder/demodulator allows the use of lower speed, lower cost technology for most internal processing operations. High data rate parts are limited to the encoder/modulator input and to the decoder/demodulator output.

REFERENCES

Gardner, F.M. 1979. Phaselock Techniques. John Wiley & Sons, New York, New York.