Final Report:

Analog MOS Integrated Circuits

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I. INTRODUCTION

The goal of this project is to design single-chip low-pass filters with constant group delay in the pass band and 60 dB minimum attenuation in the stop band. The desired 3dB frequencies are (in Hz):

2.5, 5, 10, 20, 40, 80, 160, 320

A filter class that satisfies the constant delay (linear phase) requirement while providing quite a narrow transition band is the Bessel-Chebyshev filters [1]. It was found that the 7th order Bessel-Chebyshev response satisfied the requirements of the filter. The filter transfer function is

$$H_a(s) = K \frac{(s^2+8.329^2)(s^2+10.57^2)(s^2+19.31^2)}{s^7+28s^6+378s^5+3150s^4+17325s^3+62370s^2+135135s+135135} \qquad (1)$$

where K is a normalization constant so that $H(0) = 1$. The 3dB frequency (normalized) is at $\Omega =$ 2.286. The denominator is the 7th order Bessel polynomial. The magnitude and phase plots of $H_a(j\Omega)$ are shown in figure 1.

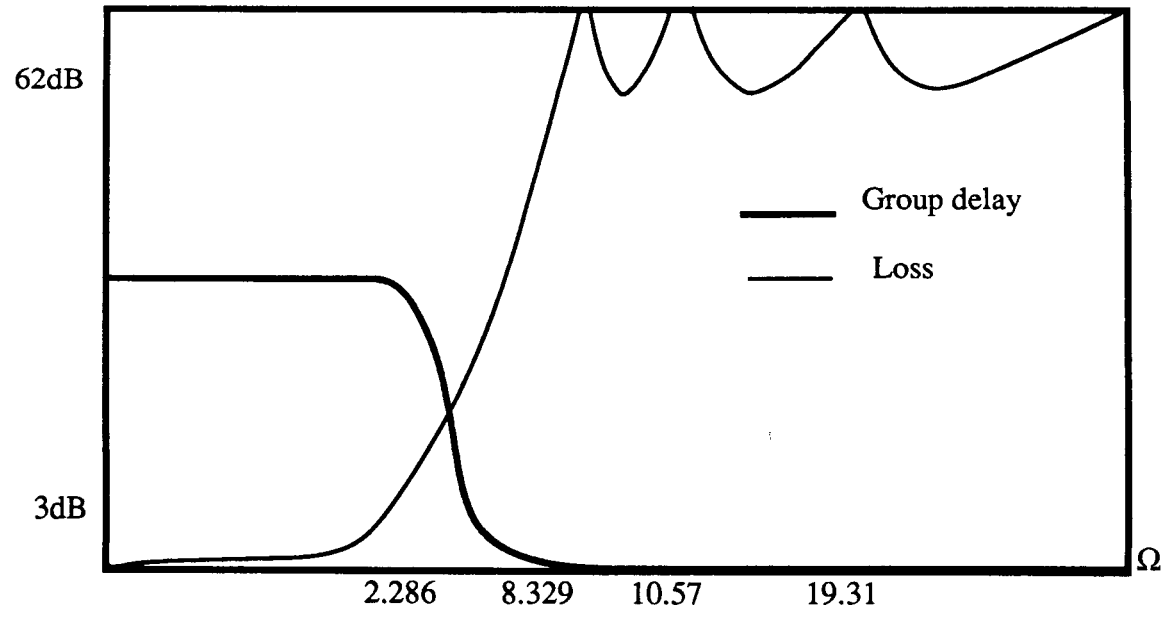

Figure 1. Loss and group delay of the 7th order Bessel-Chebyshev filter

The implementation was as a switched-capacitor (SC) network. These are sampled data systems, but the signal amplitude is not quantized [2]. The SC technique allows high order filters to be integrated on silicon with very good accuracy. The shape of the transfer function depends on the capacitor ratios which are quite precisely controlled. The frequency axis can be scaled by changing the system clock frequency.

II. CASCADE SYNTHESIS

The transfer function in equation (1) can be expressed as the product of lower order functions of s, namely bilinear and biquadratic functions. The desired transfer function is obtained when circuits realizing these simpler functions are cascaded. The rest of this section describes the design steps.

A. Factorization of the transfer function:

The numerator of (1) is already factorized, the denominator can be factorized using the Newton-Raphson root-finding algorithm. The poles and zeros of (1) are given below:

$p_0 =$ -4.9717869

$p_1 =$ -2.6856769+ j5.4206941 $\qquad$ $p_4 =$ -2.6856769- j5.4206941

$p_2 =$ -4.0701392+ j3.5171760 $\qquad$ $p_5 =$ -4.0701392- j3.5171760

$p_3 =$ -4.7582905+ j1.7392861 $\qquad$ $p_6 =$ -4.7582905- j1.7392861

$z_0 = \infty$

$z_1 =$ j8.329 $\qquad$ $z_4 =$ -j8.329

$z_2 =$ j10.57 $\qquad$ $z_5 =$ -j10.57

$z_3 =$ j19.31 $\qquad$ $z_6 =$ - j19.31

Therefore, the transfer function can be decomposed into one bilinear and three biquadratic functions.

B. Pairing of poles and zeros:

After we pair z_i and p_i to form the bilinear factor, there remains the issue of pairing the remaining three complex conjugate pairs of poles with the three complex conjugate pairs of zeros.

Out of the many possible pairings of poles and zeros some result in transfer functions that are less sensitive to element nonidealities of the actual circuit implementation. It is known that the magnitude of a bounded transfer function is not sensitive to element variations at the frequencies where it achieves its maximum [3]. Motivated by this property, we can define our objective in the pairing of poles and zeros as that the magnitude of the transfer function of each of the building blocks must be *as flat as possible in the pass band* of the filter [4].

The flattest blocks occur when the pole-zero pairs are (p_1, z_1), (p_2, z_2), (p_3, z_3). The Q factors of each block (pole) are as follows:

$Q_1 = 1.126, \ (p_1)$

$Q_2 = 0.661, \ (p_2)$

$Q_3 = 0.532, \ (p_3)$

C. Ordering of the blocks:

As it is with the pairing of poles and zeros, different orderings of the blocks result in different sensitivities to the nonidealities in the implementation. The objective is again to have *the flattest possible response in the pass band at the output of the each block* . It turns out that the best ordering is $(p_0, z_0) \rightarrow (p_1, z_1) \rightarrow (p_2, z_2) \rightarrow (p_3, z_3)$. Let us define the transfer functions for each block:

$$H_{0a}(s) = k_0 \frac{1}{s+4.9717869} \tag{2}$$

$$H_{1a}(s) = k_1 \frac{(s^2+8.329^2)}{(s^2+5.3713538s+36.5967852)} \tag{3}$$

$$H_{2a}(s) = k_2 \frac{(s^2+10.57^2)}{(s^2+8.1402784s+28.9365601)} \tag{4}$$

$$H_{3a}(s) = k_3 \frac{(s^2+19.31^2)}{(s^2+9.5165906s+25.6664902)} \tag{5}$$

D. Mapping to the discrete time domain:

We have dealt with the continuous-time frequency transfer function until now. We use the bilinear mapping to the discrete-time complex frequency, z, domain:

$$s = \frac{2}{T}\frac{z-1}{z+1} \tag{6}$$

where T is the sampling period and the continuous- and discrete-time complex frequencies are respectively,

$$s = \Sigma + j\Omega$$

$$z = re^{j\omega T}$$

From (6) we obtain

$$\omega T/2 = \arctan(\Omega T / 2) \tag{7}$$

If ΩT is very small then the relationship between ω and Ω is almost linear.

Applying (6) to (2) through (5) gives the transfer functions to be realized. The numerical values

depend on the particular value of T.

E. Filter sections:

We realized the filter as a cascade of one bilinear and three biquadratic sections.

The circuit diagram of the bilinear filter section is shown in figure 2.

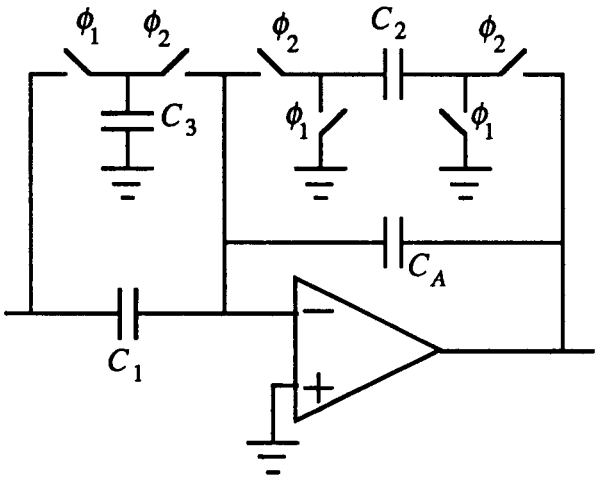

Figure 2. The bilinear SC section.

The transfer function in terms of the capacitor values is given below (C_A is set to 1):

$$H_0(z) = -\frac{C_1 z+(C_3-C_1)}{(1+C_2)z-1} \tag{8}$$

The circuit diagram of the high-Q biquadratic filter section is shown in figure 3.

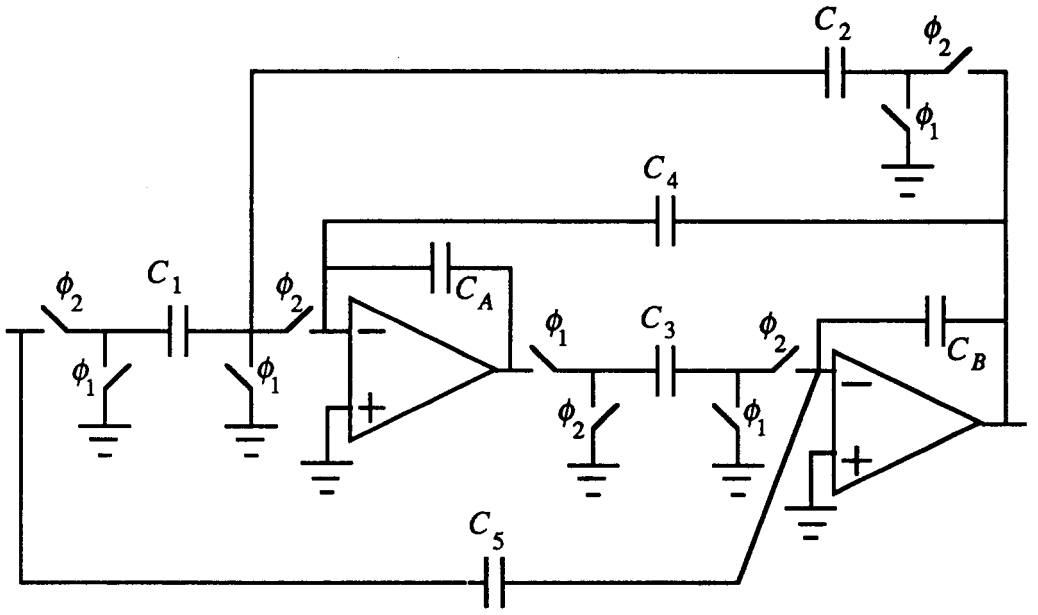

Figure 3. The high-Q biquadratic SC section.

The transfer function in terms of the capacitor values is given below (C_A and C_B are set to 1):

$$H_1(z) = -\frac{C_5z^2+(C_1C_3+-2C_5)z+C_5}{z^2+(C_2C_3+C_3C_4-2)z+(1-C_3C_4)} \tag{9}$$

The circuit diagram of the low-Q biquadratric filter sections is shown in figure 4.

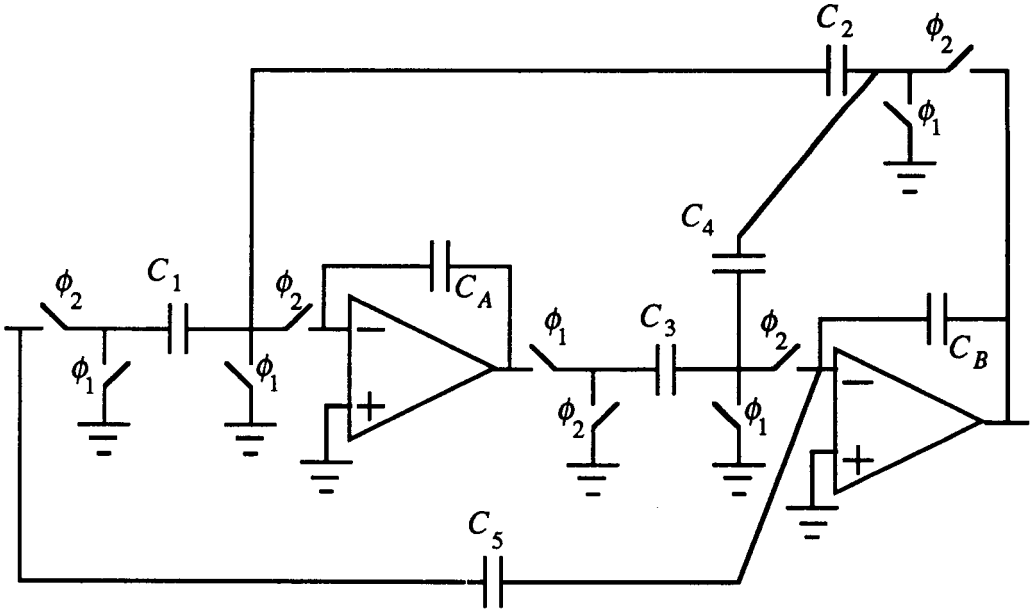

Figure 4. The low-Q biquadratic SC section.

The transfer function in terms of the capacitor values is given below (C_A and C_B are set to 1):

$$H_{2,3}(z) = - \frac{C_5 z^2 + (C_1 C_3 + -2C_5) z + C_5}{(1+C_4) z^2 + (C_2 C_3 - C_4 - 2) z + 1} \qquad (10)$$

The calculated capacitor values are such that when the clock frequency ($1/T$) is 10 kHz, the 3 dB frquency is 40 Hz. The capacitors are also scaled for maximum dynamic range and minimum size. The resulting values are shown in Table 1.

TABLE 1
Capacitor values for 3 dB frequency at 40 Hz with 10 kHz clock

	Capacitor	Value (in unit capacitors)
Bilinear Section	C_A	35.58923
	C_1	1.0
	C_2	2.0
	C_3	2.0
High-Q Biquadratic Section	C_A	7.28401
	C_B	31.98662
	C_1	1.0
	C_2	1.0
	C_3	1.0
	C_4	13.34987
	C_5	16.40688
1st Low-Q Biquadratic Section	C_A	25.58748
	C_B	10.68347
	C_1	1.0
	C_2	1.0
	C_3	1.0
	C_4	1.0
	C_5	2.90374
2nd Low-Q Biquadratic Section	C_A	33.72466
	C_B	13.62551
	C_1	1.0
	C_2	1.0
	C_3	1.50305
	C_4	1.50305
	C_5	1.0

F. Filter sections with reduced capacitor spread:

A second filter was designed to realize much lower passband edge frequencies with moderate clock speeds. We used capacitive voltage dividers to reduce the capacitor spread to realizable levels. The filter has 3 dB loss at 2.5 Hz when operated with 10 kHz clock.

The circuit diagrams for the filter sections with capacitive voltage dividers (*T*-sections) are shown in Figures 5 through 7.

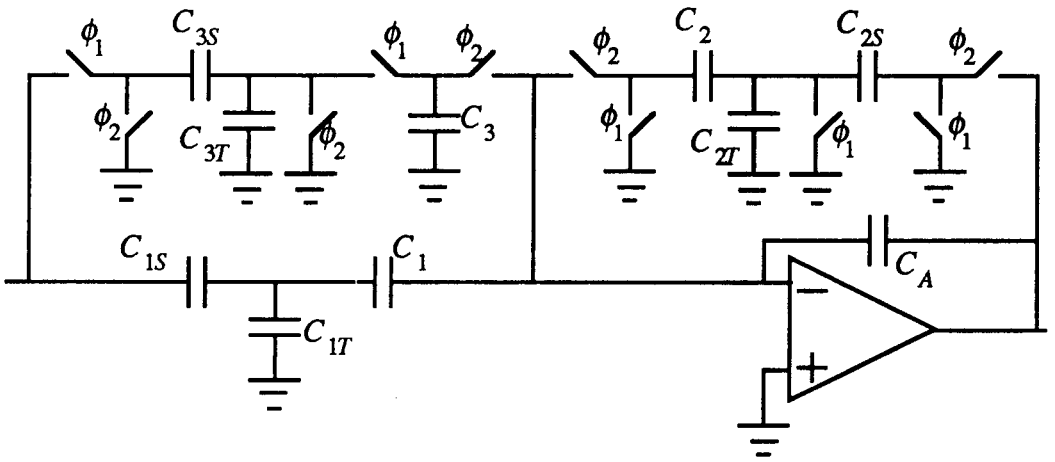

Figure 5. Bilinear section with voltage dividers.

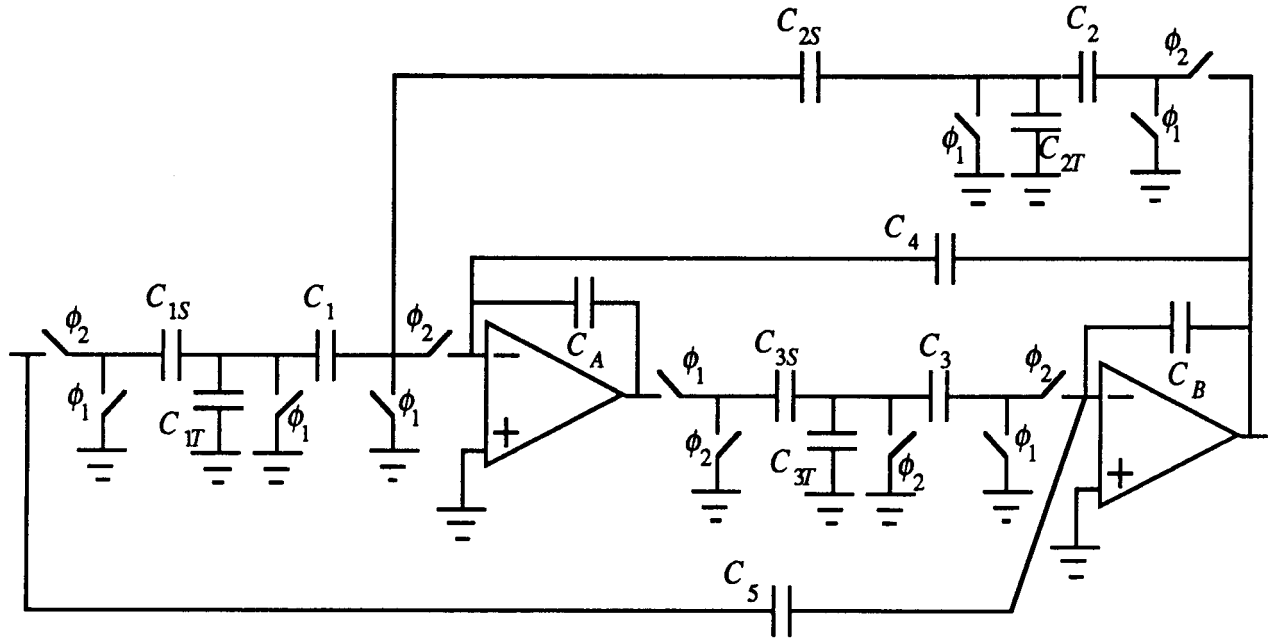

Figure 6. High-Q biquadratic section with voltage dividers.

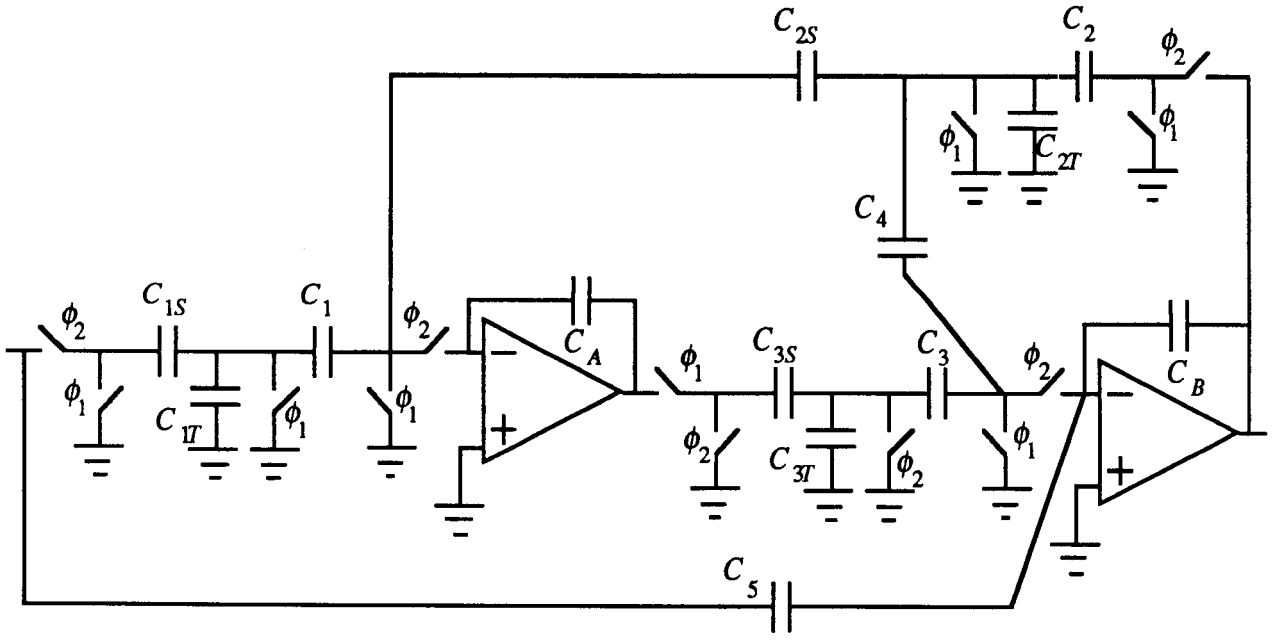

Figure 7. Low-Q biquadratic section with voltage dividers.

The capacitor values are given in Table 2.

TABLE 2
Capacitor values for 3 dB frequency at 2.5 Hz with 10 kHz clock

	Capacitor	Value with T	Value without T
Bilinear Section	C_A	23.19570	584.42578
	C_1	1.0	1.0
	C_{1S}	1.0	
	C_{1T}	23.19570	
	C_2	1.43863	2.0
	C_{2S}	1.43863	
	C_{2T}	23.19570	
	C_3	1.43863	2.0
	C_{3S}	1.43863	
	C_{3T}	23.19570	
High-Q Biquadratic Section	C_A	4.87619	114.64308
	C_B	21.51080	505.73633
	C_1	1.0	1.0
	C_{1S}	1.0	
	C_{1T}	21.51080	
	C_2	1.0	1.0
	C_{2S}	1.0	
	C_{2T}	21.51080	
	C_3	1.0	1.0
	C_{3S}	1.0	
	C_{3T}	21.51080	
	C_4	9.08509	213.59784
	C_5	11.32699	266.30664
1st Low-Q Biquadratic Section	C_A	19.25835	409.40088
	C_B	8.38634	178.27975
	C_1	1.0	1.0
	C_{1S}	1.0	
	C_{1T}	19.25835	
	C_2	1.02497	1.0
	C_{2S}	1.02497	
	C_{2T}	19.25835	
	C_3	1.0	1.0
	C_{3S}	12.0	
	C_{3T}	19.25835	
	C_4	1.02497	1.0
	C_5	2.17828	46.30406

2nd Low-Q Biquadratic Section	C_A	26.28833	539.59912
	C_B	14.85170	152.42438
	C_1	1.18146	1.0
	C_{1S}	1.18146	
	C_{1T}	26.28833	
	C_2	1.0	1.0
	C_{2S}	1.5	
	C_{2T}	26.28833	
	C_3	1.70085	1.0
	C_{3S}	1.70085	
	C_{3T}	26.28833	
	C_4	2.0	1.0
	C_5	1.02569	10.52675

As can be seen from Table 2, the overall capacitor area is reduced by a power of 2.

III. FABRICATION AND TEST RESULTS

Both of the designs were fabricated as a single chip using 5-μm double-poly CMOS process provided by MOSIS, a federal government supproted agency. We obtained the samples in March 1988. Table 3 gives some of the physical properties of the fabricated chips:

TABLE 3
Some Physical Properties of the Fabricated Filter

Technology:	p-well CMOS, double poly
Minimum feature size:	5 μm
Chip size:	6800 μm X 4595 μm (265 mil X 179 mil)
Unit capacitor:	0.978 pF
Power supplies:	±5 V
Power consumption:	280 mW
Clock input:	±5 V square-wave with 50% duty cycle
Package:	40 pin ceramic DIP

The chip phograph is shown in Figure 8.

The yield was somewhat low, around 50%. This could have been due to the large size of the chip by typical MOSIS standards. The frequency domain measurments were done using a network analyzer. The magnitude and phase response plots are provided at the end of the section. The

results for both sets of filters are in close agreement with the design values. Due to the limitations of the network analyzer the plots do not show the response in the 0 to 5 Hz range. Because of this limitation, the plots for the filter with the voltage dividers were obtained with 160 kHz clock frequency.

The manual testing at DC showed that the filter with voltage dividers had quite high output offset voltage, around 0.8 V. But the other filter had much lower output offset, around 20 mV. We have found that the offset voltage can be reduced by adjusting the rising and falling times of the input clock signal.

The filter that was designed to give 40 Hz passband edge at 10 kHz clock operated without problems for clock frequencies in the range 625 Hz to 100 KHz.

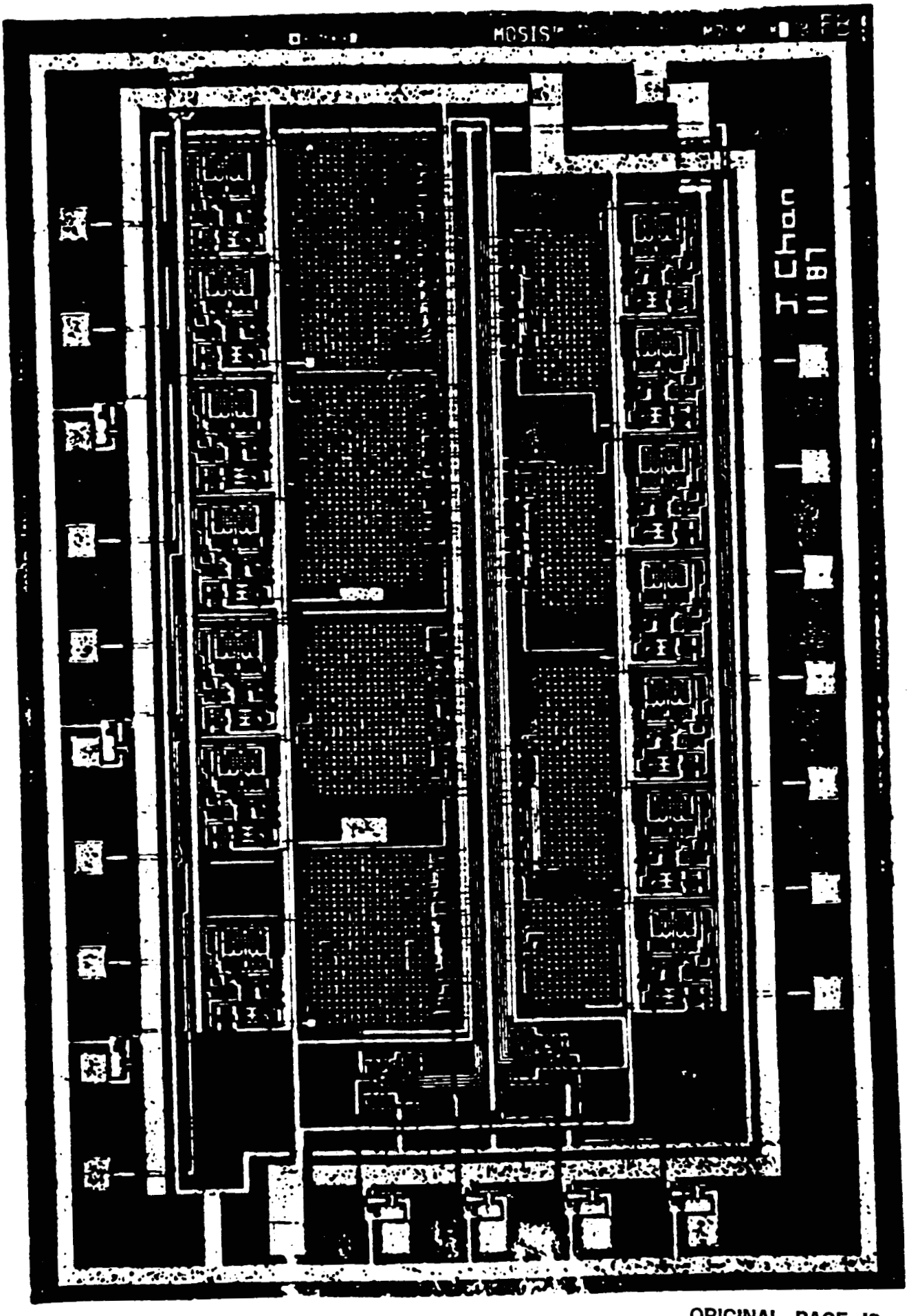

Figure 8. Enlarged photograph of the chip.

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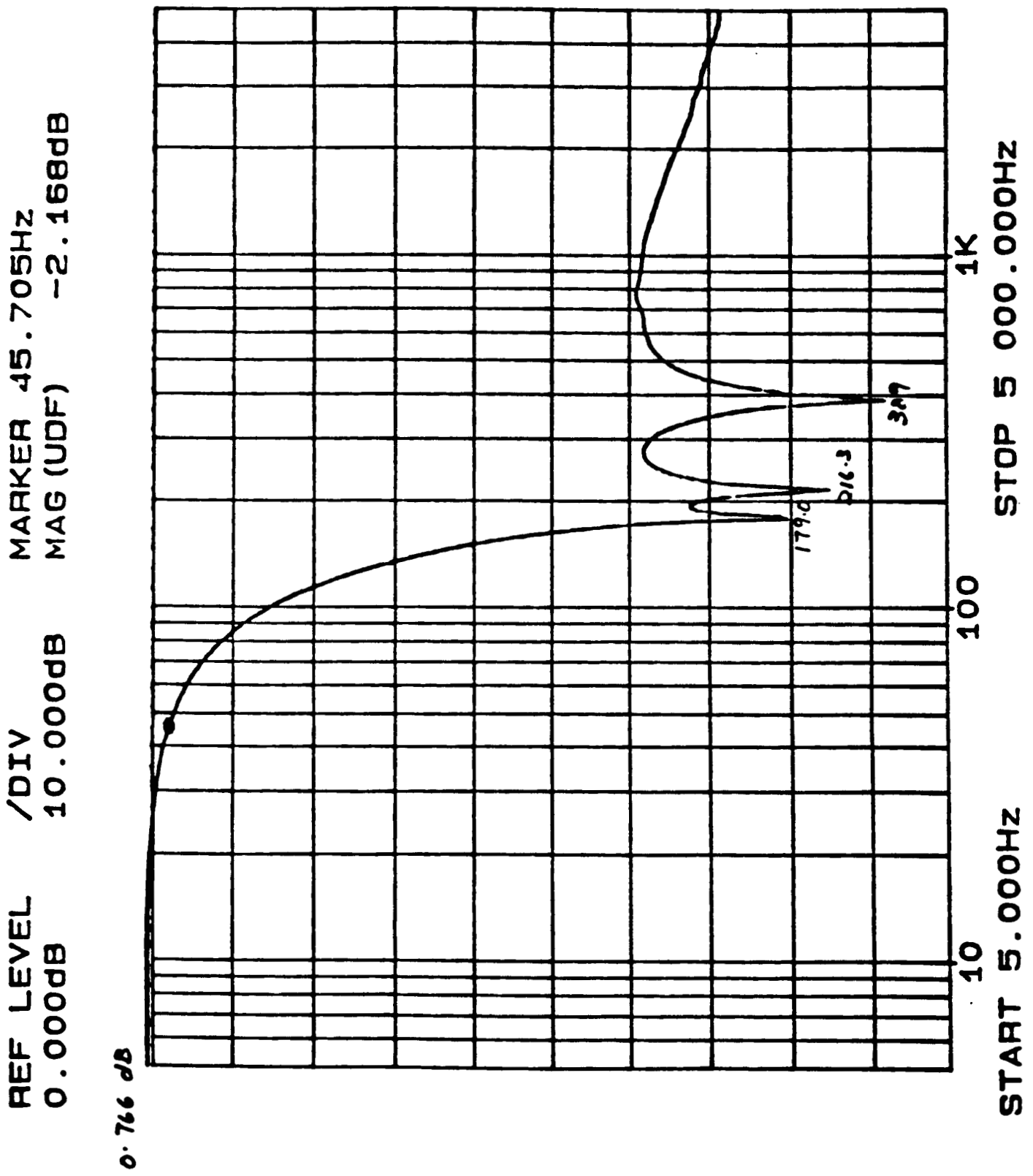

Figure 9. Magnitude response of the 40 Hz design with 10 kHz clock.

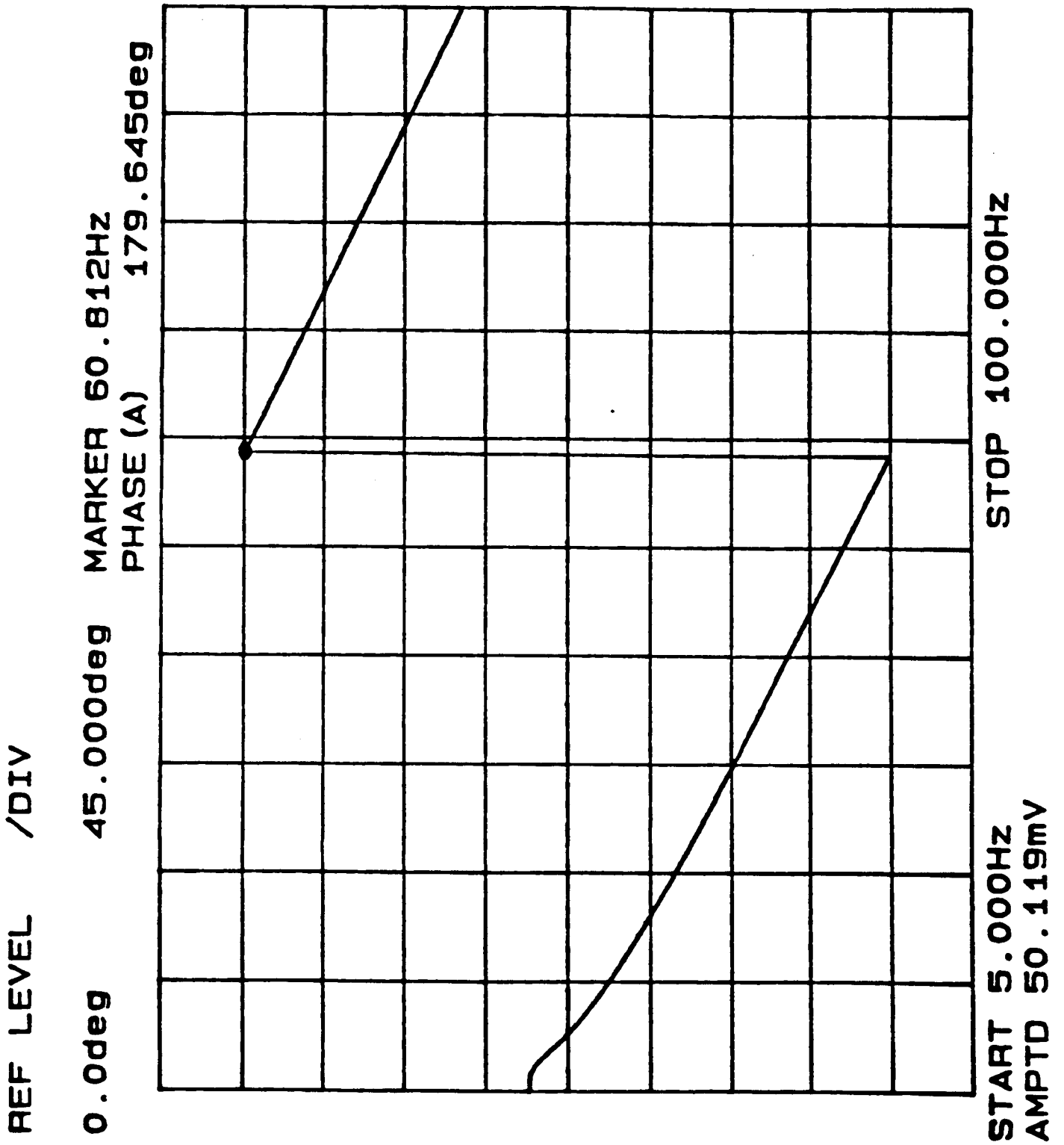

Figure 10. Phase response of the 40 Hz design with 10 kHz clock.

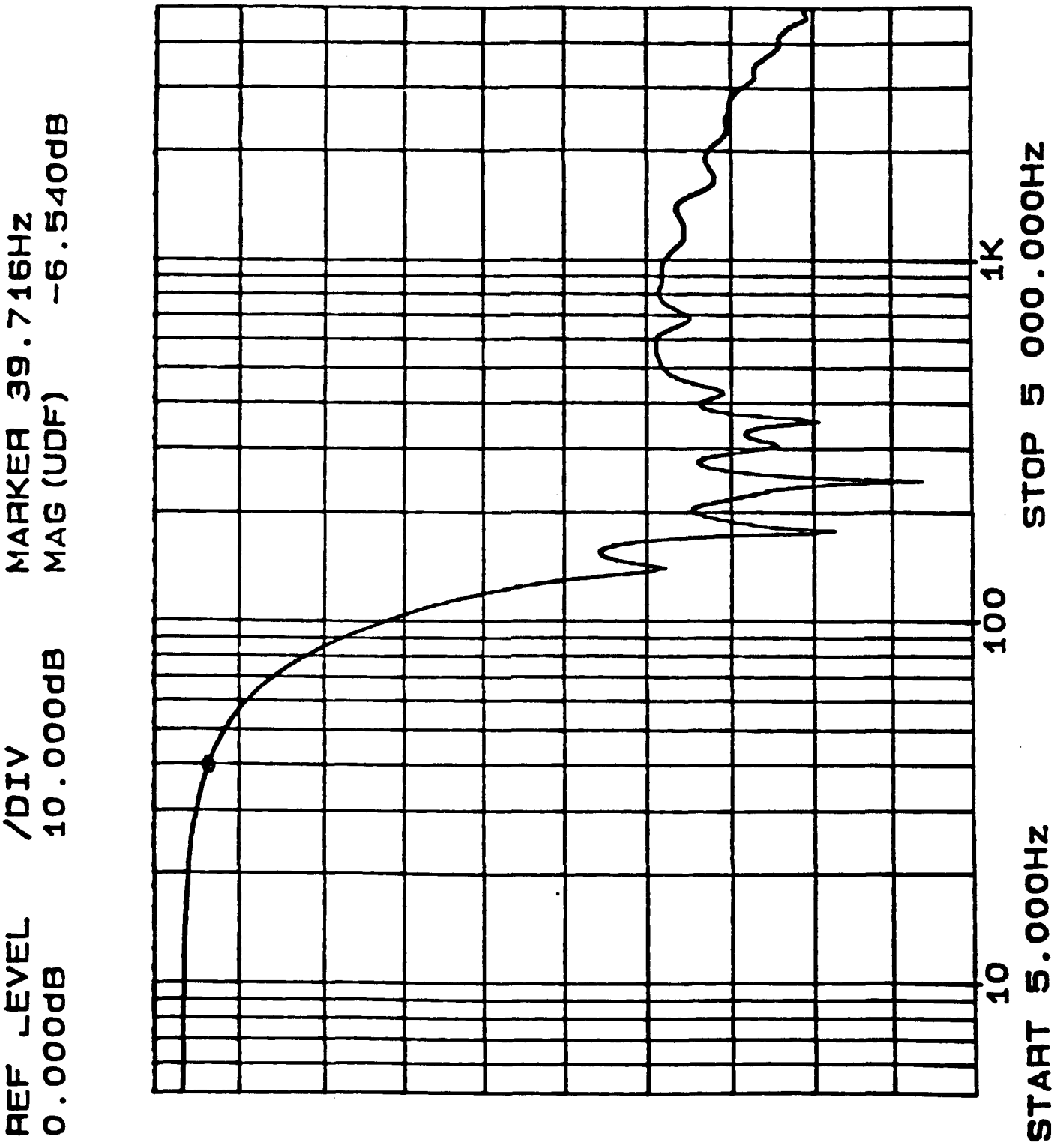

Figure 11. Magnitude response of the 2.5 Hz design with 160 kHz clock.

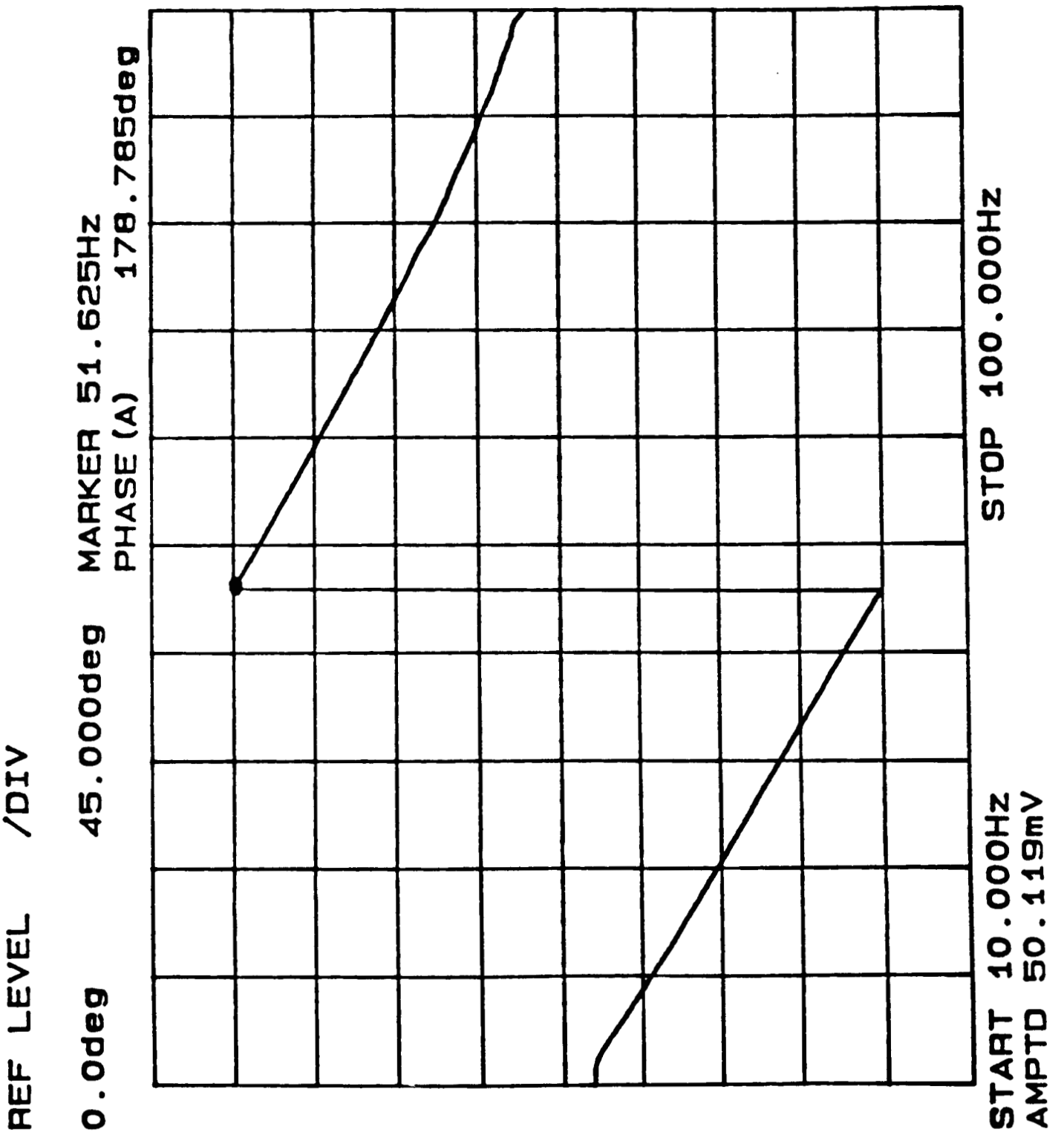

Figure 12. Phase response of the 2.5 Hz design with 160 kHz clock.

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