CR 182243

20 GHz LOW NOISE, LOW COST RECEIVER FOR DIGITAL SATELLITE COMMUNICATION SYSTEM, GROUND TERMINAL APPLICATIONS

CONTRACT NAS3-24244

FINAL REPORT

PREPARED BY:

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15 DECEMBER 1988

PREPARED FOR:

NASA-LEWIS RESEARCH CENTER

CLEVELAND, OHIO 44135

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16. Abstract

Abstract

This final report describes a 45 month effort for the development of a 20 GHz, low-noise, low-cost receiver for digital, satellite communication system, ground terminal applications. Six proof-of-concept receivers were built in two lots of three each. Performance was generally consistent between the two lots. Except for overall noise figure, parameters were within or very close to specification. While the noise figure was specified as 3.5 dB, typical performance was measured at 3.0 to 5.5 dB, over the full temperature range of -30°C to + 75°C.

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1.0 INTRODUCTION

This is the Final Report for the NASA Lewis Research Center 20 GHz Receiver program, Contract NAS3-24244. The first part of the report is an executive summary, which describes the technical progress in a narrative fashion, showing the evolution of the receiver's design, fabrication and test. After the executive summary, four of the task reports are repeated for the reader's convenience: The Receiver Design (Task I) Report, the Breadboard Test and Analysis (Task II) Report, the Proof of Concept Test and Analysis (Task VI) Report, and the Proof of Concept Test Report for the Second Build. Since the Test Reports summarize the raw data, that data is not be repeated in this report.

Six Proof Of Concept Receivers were built in two lots of three each. Performance was generally consistent between the two lots, and except for overall noise figure, parameters were within or very close to specification. While the noise figure was specified as 3.5 dB, typical performance was measured at 3.0 to 5.5 dB over the full temperature range of $-30^{o}C$ to $+75^{o}C$.

2.0 EXECUTIVE SUMMARY

2.1 OVERVIEW

This contract (NAS3-24244) is for the development of a low noise, low cost 20 GHz ground terminal receiver. Six proof of concept (POC) receivers were delivered to be used in the POC demonstration of the Advanced Communications Technology Satellite (ACTS). The study began in March 1985, and concluded in December 1988. The original contract was for three receivers, but was modified for three additional receivers in May 1988.

The receiver function is to amplify and translate, with minimum noise contribution, an input signal in the 17.7 to 20.2 GHz frequency band to an intermediate frequency (IF) of 3.37 GHz. The receiver is comprised of two subassemblies. The first subassembly is the receiver module, which contains all of the signal amplification, conversion, and filtering circuits along with their respective DC regulator and control circuits. The receiver module is the main product of the work done on the contract. The second subassembly is the local oscillator and its DC circuitry, which is used for selecting one of two channels by providing the local oscillator signal for the mixer in the receiver module. The local oscillator was developed under a subcontract to Communications Techniques of Whippany, NJ.

The objective of this contract was to develop a 20 GHz receiver which a) provides the performance required for high burst rate TDMA digital satellite communications of the 1990's, b) utilizes designs and implementation techniques which result in significantly reduced cost such as making use of Monolithic Microwave Integrated Circuits (MMIC), and c) provides an advanced data base for development of products to be utilized in specific systems.

The program was divided into ten tasks, consisting of:

I- Receiver Design

II- Breadboard Development

III- POC Model Planning and Specifications

IV - POC Model Design and Test Plan

V- Fabrication of POC Models

VI- Proof of Concept Test and Analysis

VII- Product Assurance

VIII- Work Plan

IX- Reports

X- Reserved Engineering (later deleted)

In Task I, a preliminary design of the receiver was generated, including analysis of expected specification compliance and margins. In Task II, the various components described in Task I were breadboarded, including the MMIC components. Task III set the specifications for the components to be used in the POC model, taking into account breadboard results obtained in Task II. In Task IV, the breadboard results and POC specs were used for a detailed design phase, ending with a CDR. Task V was the fabrication and functional test of the POC models. In Task VI, the receivers were tested according to the plan generated in Task IV, and a Test and Analysis Report was generated. Task XIII was the work plan generated at the beginning of the job. Task IX encompassed the reports throughout the job, including monthly and task reports, as well as this report. Task X was Reserved Engineering. This task was eventually deleted in favor of building three additional receivers.

2.2 TASK I SUMMARY

The design architecture developed in Task I is shown in Figure 2.2-1. The design used a Low Noise Amplifier (LNA) which includes a waveguide to microstrip transition and two 1/3 micron FETs. The device chosen was an NE04500 FET from NEC, which had sidewall metallization for improved RF grounding. Unpackaged chips were selected because package technology had not yet reached the 20 GHz domain. The LNA was followed by two MMIC RF Amplifier (RFA) chips. At the time of Task I, this chip was in fabrication as part of the Harris MMIC IR&D. The front end configuration was driven by the expected noise performance of the MMIC chips, proved inferior to the receiver noise figure requirements. The design allowed the MMIC chips to provide bulk gain prior to the lossy frequency conversion components, while the two LNA stages set the system noise figure.

The location of the receiver preselect filter was a compromise between minimizing input losses (preceding the LNA) for noise figure considerations, eliminating out of band input signals that can cause receiver intermodulation products or gain saturation and rejecting image band noise generated by wideband LNA modules. The chosen preselection method was a quartz microstrip bandpass filter located after the MMIC RFAs and before the downconverter mixer. This allowed a low cost microstrip implementation instead of a waveguide design. The distributed, coupled line configuration could not be implemented in MMIC because of its large size. A MMIC design using lumped elements was not practical due to the low Q of those elements, which would cause high insertion loss and poor out of band rejection. The distributed MIC filter gave the best performance at the lowest cost.

A MMIC Image Reject Mixer (IRM) was chosen to provide the

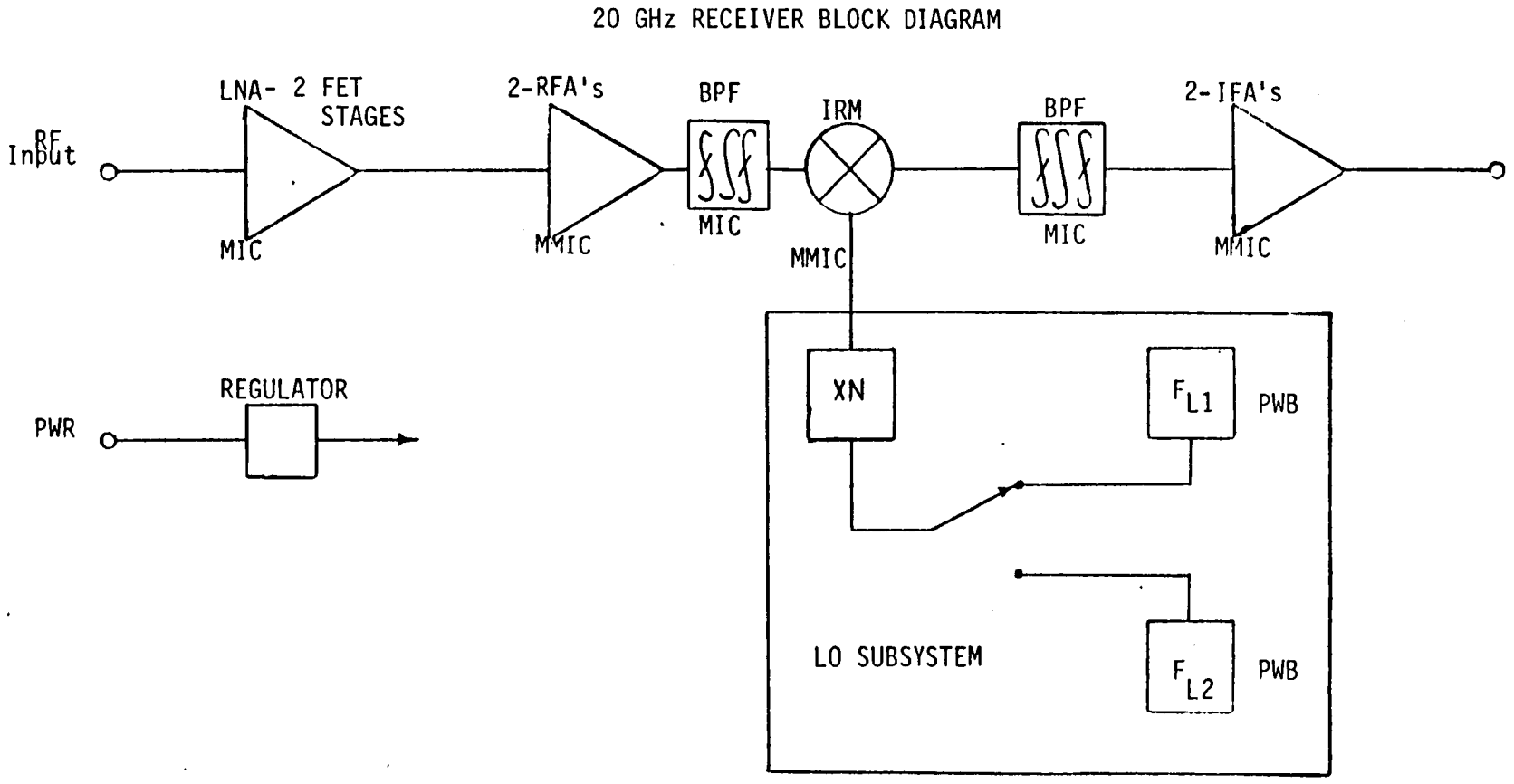


FIGURE 2.2-1 TASK I DESIGN ARCHITECTURE

frequency translation to the 3.37 GHz IF. This was chosen because of the ease of design and fabrication in MMIC form. At the time of Task I, this chip was also in fabrication as part of the Harris MMIC IR&D. The mixer includes a MIC IF hybrid to combine the IRM quadrature output. Image reject properties were not critical due to performance of the input preselect filter and the WR-42 waveguide input, which cut off all image signals.

The two local oscillator signals required to downconvert the RF input bands are generated by an oscillator using two distinct low noise crystal oscillators as references. The desired LO signal is determined by switching between these two references. The local oscillator subsystem is a standard, purchased, off the shelf design housed in a separate module next to the receiver module.

The downconverted signal is selected by using a microstrip bandpass filter similar to the preselect filter. At the PDR, it was determined that the modem had a narrower filter, and that one would not be required for the receiver.

The signal is amplified by two MMIC IF Amplifiers (IFA). These had already been developed on the Harris MMIC IR&D.

A significant amount of time was spent in Task I choosing a design topology for the LNA. Originally, it was thought that a device could be found that would have an optimum noise match point and 1.7:1 VSWR at the same input impedance. It was found that no FET could provide an optimal noise match and an acceptable input VSWR simultaneously. This left two options; a single ended design using a waveguide isolator on the input, or a balanced design, which using hybrid couplers on the input and output of two parallel stages. The hybrid couplers cause the reflections of the parallel amplifiers to cancel each other, resulting in a low VSWR. The balanced approach requires twice the material and labor for fabrication, making it contrary to the program's low cost objective. The single ended approach was favored, but there was much concern about interstage impedance effects. Noise Parameters were not available for any devices at 20 GHz, so it was decided to carry both design topologies on to Task II, where a Harris effort measured the noise parameters of the selected FET, conducted computer aided analysis of performance of single ended and balanced amplifiers, conducted a special design review, and selected the single ended approach.

Table 2.2-1 is a compliance matrix generated for the Task I PDR, showing the specifications from the contract, and the expected performance of the receiver as designed. Figure 2.2-2 shows the gain, noise figure, and intercept point budgets forecast in Task I. The complete Receiver Design Report is included the appendix, and the results are summarized in the compliance matrix.

TABLE 2.2-1 COMPLIANCE MATRIX, TASK I (PAGE 1 OF 3)

TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
INPUT RF BAND	3.2.2.1 (3.2.1)	17.7-20.2	17.7-20.2	-----	GHz	3.0
SUBBAND #1	3.2.2.1 (3.2.1)	19.4953±0.166	19.4953±0.166	-----	GHz	3.1/3.6
SUBBAND #2	3.2.2.1 (3.2.1)	19.9600±0.166	19.9600±0.166	-----	GHz	3.1/3.6
OUTPUT IF BAND	3.2.2.2 (3.2.2)	3373.056±0.166	3373.056±0.166	-----	MHz	3.0
LOCAL OSCILLATOR SETTABILITY	3.2.2.2 (3.2.2)	±20	±20	-----	KHz	3.5
LOCAL OSCILLATOR LONG TERM DRIFT	3.2.2.2 (3.2.2)	±1.2	±1.0	±0.2	PPM/YR	3.5
NOISE FIGURE	3.2.2.3 (3.2.3)	3.5	4.0	-0.5	dB	3.1
RF TO IF GAIN	3.2.2.4 (3.2.4)	30	31.8	1.8	dB	3.1
INBAND OVERDRIVE	3.2.2.5 (3.2.5)	0	>10	>10	dBm	3.1
GAIN RIPPLE	3.2.2.6 (3.2.6)	±0.75	±0.57	±0.18	dB/150 MHz	3.3
GAIN SLOPE	3.2.2.7 (3.2.7)	0.5	0.19	0.31	dB/10 MHz	3.3
INPUT VSWR	3.2.2.8 (3.2.8)	1.7:1	1.46:1	2.8 dB RL	-------	3.2
OUTPUT VSWR	3.2.2.9 (3.2.9)	1.5:1	1.44:1	0.9 dB RL	-------	3.2

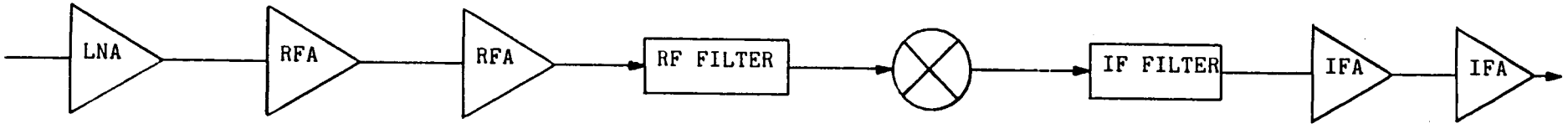
TABLE 2.2-1 COMPLIANCE MATRIX, TASK I (PAGE 2 OF 3)

TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
GROUP DELAY	3.2.2.10 (3.2.10)					3.3
0 PARABOLIC		±0.1	0.007	0.093	ns/MHz^2	
0 RIPPLE		5.0	1.01	3.99	ns(p-p)	
IMAGE REJECTION	3.2.2.11 (3.2.11)	40	>50	>10	dB	3.6
AM-PM CONVERSION	3.2.2.12 (3.2.12)	0.5	0.22	0.28	Deg/dB	3.4
INPUT 1 dB GAIN COMPRESSION	3.2.2.13 (2.2.13)	-40	-39.2	0.8	dBm	3.1
INPUT 3rd ORDER IP	3.2.2.14 (3.2.14)	-30	-29.2	0.8	dBm	3.1
OUT OF BAND REJECTION (<15.7 & >22.2 GHz)	3.2.2.15 (3.2.15)	45	>55	10	dB	3.6
SPURIOUS RESPONSE	3.2.2.16 (3.2.16)	-45	-45	0	dBc	3.6

TABLE 2.2-1 COMPLIANCE MATRIX, TASK I (PAGE 3 OF 3)

TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
PHASE NOISE (SSB >1K Hz)	3.2.2.17 (3.2.17)	-70	-78	8	dBc/Hz	3.5
DC POWER	3.2.2.18/22/23 (3.2.18/20/21)	TBD ±10% SURGE <2X REVERSE POLARITY PROTECTION	±15 ±10% SURGE <2X REVERSE POLARITY PROTECTION	----- -----	VOLTS AMPS	3.7
CONNECTORS	3.2.2.19 (3.3.3/4)					3.8
o RF INPUT		WR 42/COVER	WR 42/COVER	-----	-----	
o IF OUTPUT/ LO INPUT		SMA FEMALE	SMA FEMALE OR COMPATABLE	-----	-----	
o DC		COMMERCIALLY AVAILABLE	COMMERCIALLY AVAILABLE	-----	-----	
RECEIVED POWER	3.2.2.20 (3.2.19)	-80 TO -60	UP TO -56.4	-----	dBm	3.4/3.6
MECHANICAL CONFIGURATION	3.2.2.21 (3.3.1/2/5/7)	ANTENNA MOUNTABLE	ANTENNA MOUNTABLE	-----	-----	3.8
ENVIRONMENT	3.2.3 AND 3.3.2.2 (3.3.6)	$-30 \leq T_A \leq +75$	$-30 \leq T_A \leq +75$	-----	°C	3.1

RECEIVER PERFORMANCE OVER TEMPERATURE
(SINGLE ENDED LNA)



G_{MAX}	15.5	12.5	12.5	-1.6	-7.5	-1.4	12.75	-6	12.75 dB
G_{MIN}	13.5	9.5	9.5	-3.5	-7.8	-3.0	10.25	-6	10.25 dB
$^1P_{O\ MIN}$	12.2	20.0	20.0	---	5.0	---	26.0	--	26.0 dBm
NF_{MAX}	3.45	4.8	4.8	---	8.5	---	4.4	--	4.4 dB

SPEC
-----
30 dB
-30 dBM
3.5 dB

PREDICTED PERFORMANCE

G_{MAX} = 49.5 dB
G_{MIN} = 32.7 dB
$^1P_{IN\ EQ}$ = -29.2 dBm MIN
NF_{EQ} = 3.75 dB (398° K) MAX

FIGURE 2.2-2 TASK I BUDGETS

2.3 TASK II SUMMARY

Task II was the breadboard development phase of the program. The receiver's circuits were designed and breadboarded to verify their predicted performance. These results were then used to model the overall receiver performance and modify the design in Task IV, POC Design.

LOW NOISE AMPLIFIER

The market was surveyed for available low noise devices during the preliminary design phase, and the NEC device NE04500G was selected as the device for the LNA. In parallel with the 20 GHz Receiver Program, Harris' IR&D was investigating HEMT FET devices. A Gould HEMT (H503) was selected for investigation on the IR&D. Since both devices would be evaluated at the same time, The results would be compared to select the best overall device for use in the NASA Receiver.

Two test fixtures were built to characterize the LNA devices, one made in coax and the other in waveguide. The coax fixture was made using Wiltron K connectors, and was found to be inadequate for use because of excessive VSWR. The waveguide fixture, based on microstrip flags suspended in waveguide, was much superior and is shown in Figure 2.3-1. Using this test fixture a method of calculating the FET's noise parameters based on measured noise figures was implemented. Characterization of the low noise FET parameters (F_{min}, r_n, g_{opt}, and b_{opt}) was accomplished by measuring the FET's noise figure with various source impedances presented to its input. Connecting the various stub "dots" of the input circuit to the transmission line in a methodical fashion results in various impedances being presented to the FET's input. Once a minimum of four data points have been measured, the noise figure equation shown below was solved yielding all four defining noise parameters.

$$F = F_m + r_n/g_s \left[(g_s-g_o)^2 + (b_s-b_o)^2 \right]$$

where:

F_m is the minimum device noise figure

r_n is the device noise resistance

g_o and b_o are the optimum matching impedance to obtain F_m

g_s and b_s are the source impedance presented to the device.

However, a much better fit was obtained by continuing these measurements until all stub lengths were connected (one at a time), and then performing a least squares best fit (LSBF) algorithm on the data to fit the noise figure equation.

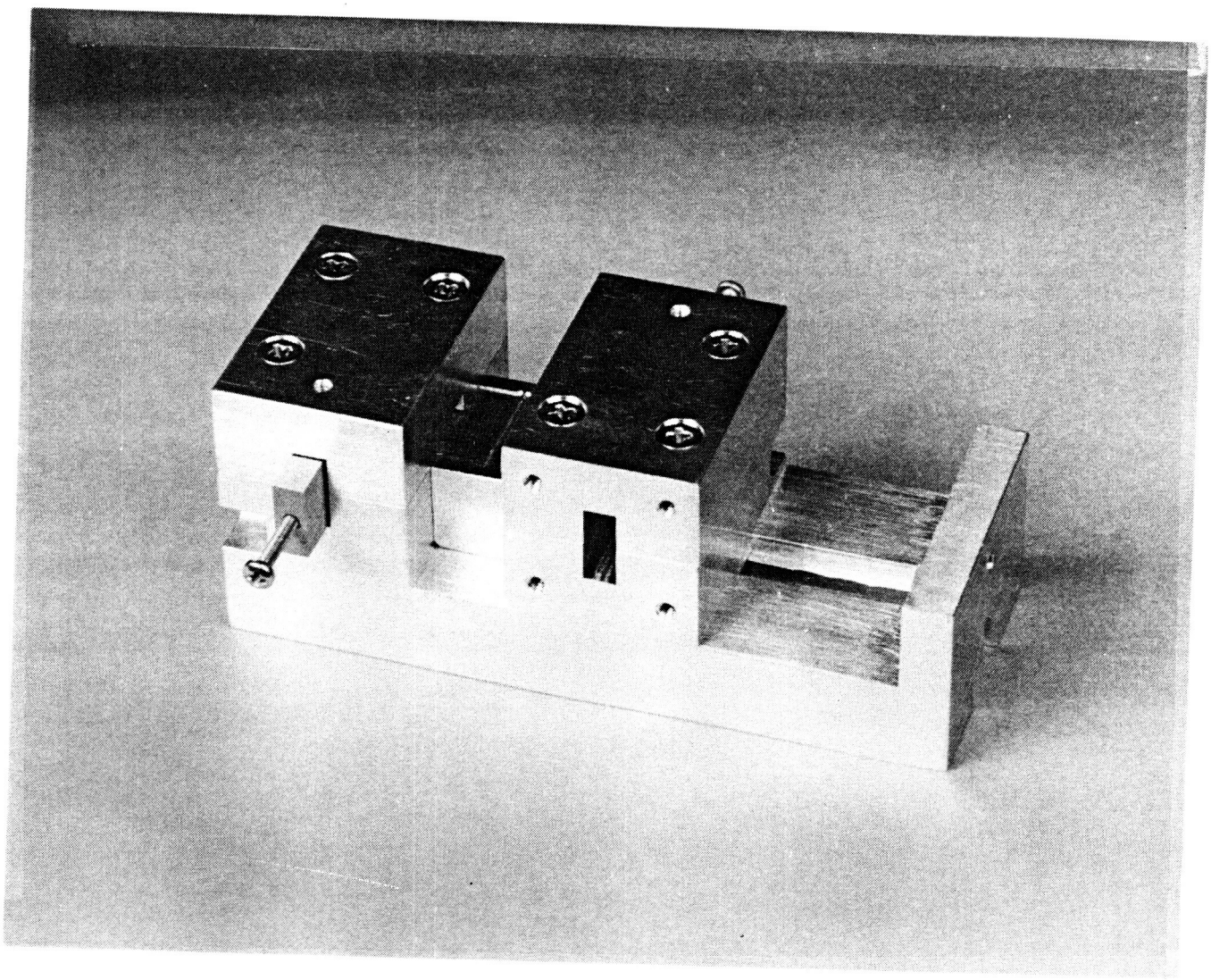


FIGURE 2.3-1 WAVEGUIDE TEST FIXTURE FOR LNA AND DEVICE EVALUATION

Typically, measurements were taken at seven different points, and extreme mismatches were deleted from the LSBF. This method reduces most of the measurement error and allows an accurate LNA design to be performed.

One caution in using this approach is to ensure the model of the source impedance circuit is accurate. The computer prediction (SuperCOMPACT software in this case) of source impedance is the value used - not a measurement of impedances. Super- Compact's model was sufficiently accurate, as the breadboard data in following paragraphs indicate.

Using the data gathered above, a three stage breadboard LNA was designed, fabricated, and tested. FET bonding technique was found to be a critical problem. For devices as small as these HEMTs, only thermal compression bonding should be used. The use of ultrasonic bonding was found to induce micro-cracks in the FET structure. Figure 2.3-2 shows the LNA breadboard as built in the waveguide test fixture with the end piece covers removed, revealing the waveguide to microstrip transitions. A waveguide isolator is included in the measurement as in the final receiver. Figure 2.3-3 compares the measured results of the breadboard to predicted performance at room temperature. Excellent agreement was obtained for noise figure over the noise bandwidth while the gain slightly exceeded prediction over the same band. These results give a high degree of credibility to the noise parameter characterization procedure as described above.

After the LNA breadboard testing was completed, Harris again performed an industry survey of existing, available FETs. However, this time (more than one year after our first survey) several HEMT manufacturers were offering acceptable devices.

Harris selected the NEC HEMT (NE 20200) as the replacement for the Gould device. This HEMT has both higher gain and lower noise figure than the Gould HEMT. It was available from stock with a complete set of S and noise parameters through 30 GHz. Therefore, the long detailed process of noise parameter characterization was not required for this HEMT, and an LNA with superior performance was incorporated into the receiver design. The new LNA was designed during Task IV (POC Design), and fabricated during Task V (POC Fab).

MMIC RF AMPLIFIER

The RFA testing was completed, with very good results obtained. A single-ended design was fabricated for NASA, and a balanced design was fabricated on our internal IR&D program which shared the same wafer. Figure 2.3-4 is a picture of the balanced amplifier. Both amplifier types exhibit similar gain response and reverse isolation qualities. However, the balanced amplifier shows a significant improvement in VSWR over that of the single ended design. VSWRs of 2.0:1 to 3.0:1 were encountered for the single-ended RFA, while the balanced RFA typically did not exceed

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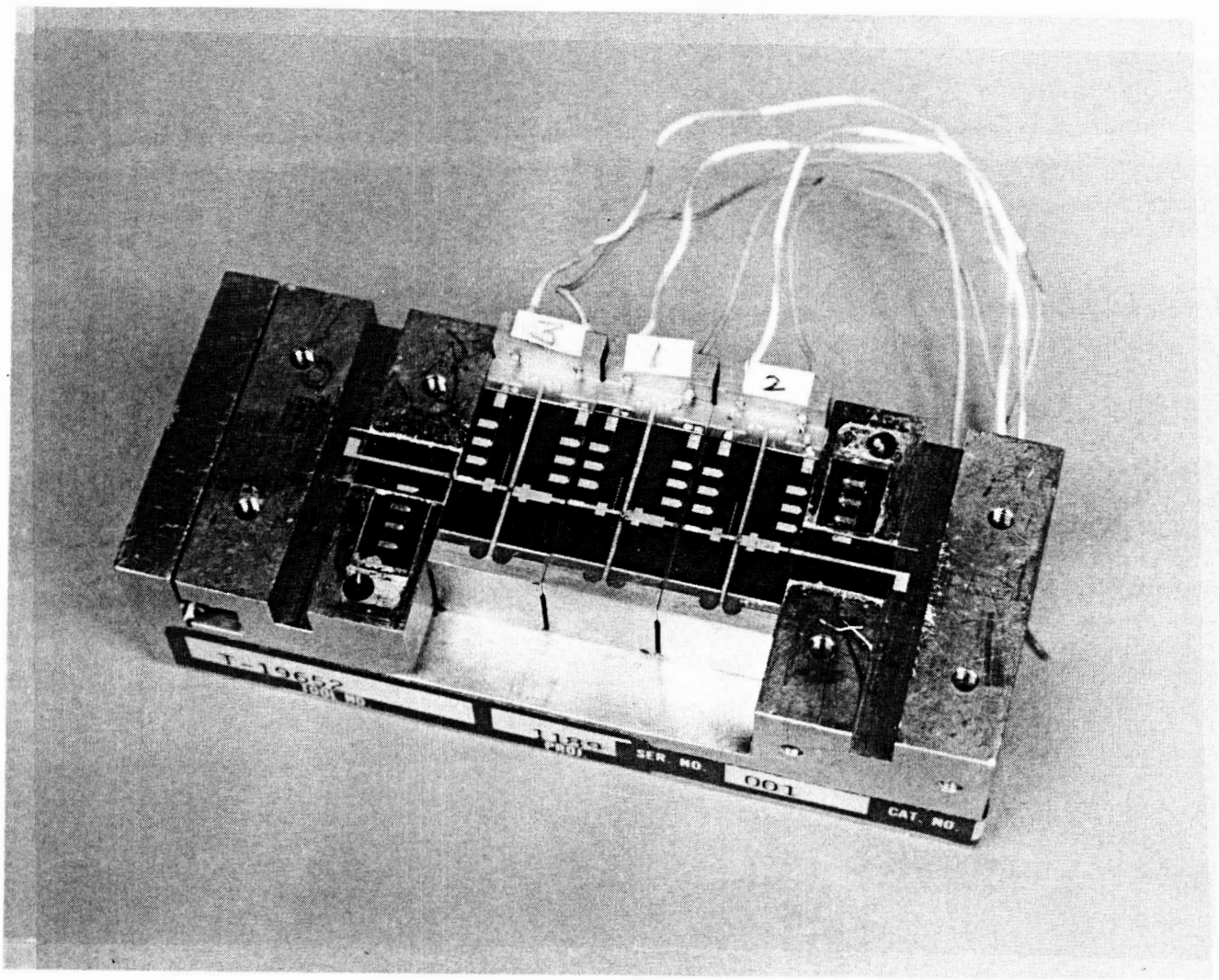

FIGURE 2.3-2 BREADBOARD LNA IN TEST FIXURE

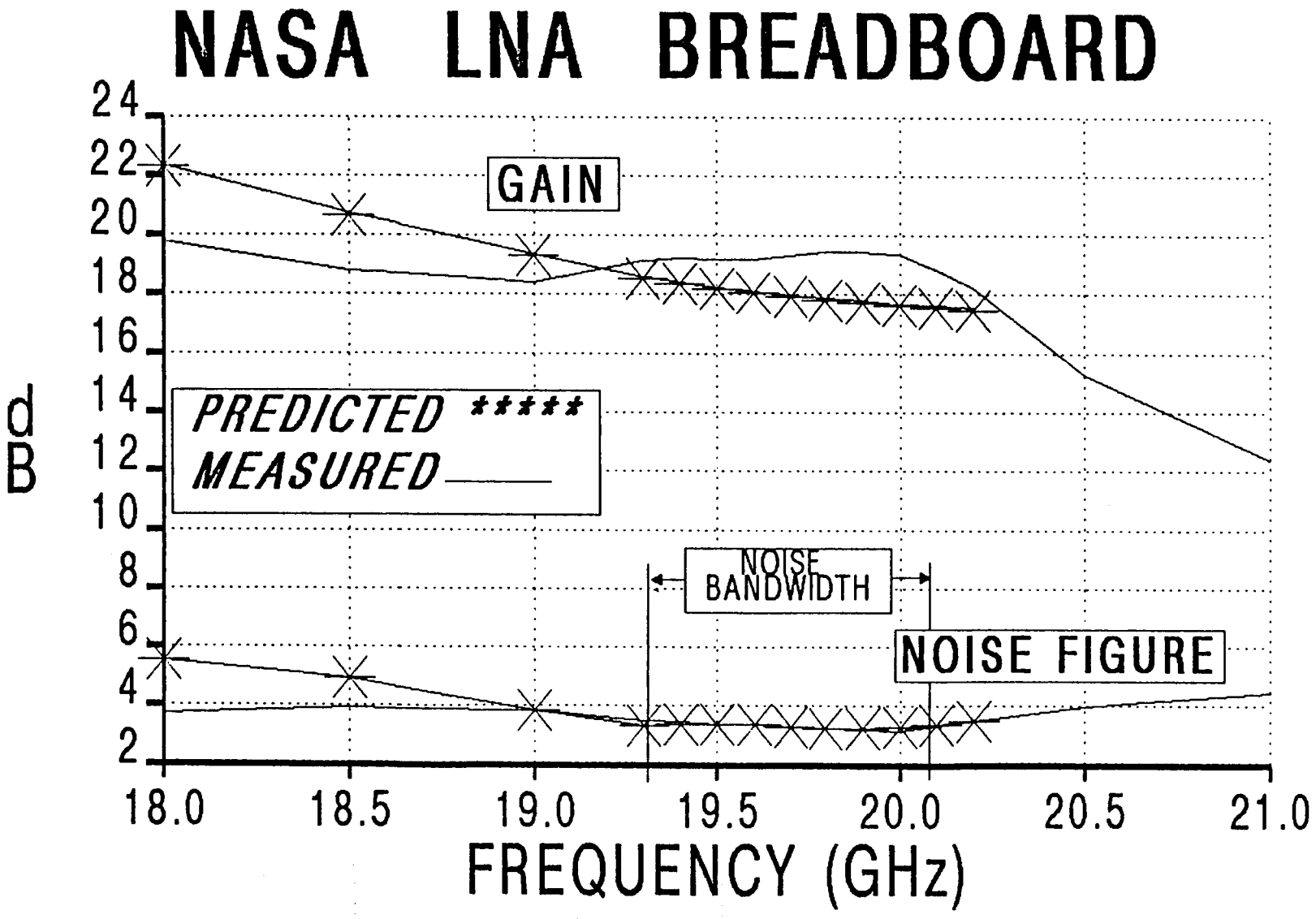
NASA LNA BREADBOARD
GAIN
PREDICTED *****
MEASURED ——
NOISE BANDWIDTH
NOISE FIGURE
dB
24
22
20
18
16
14
12
10
8
6
4
2
18.0
18.5
19.0
19.5
20.0
20.5
21.0
FREQUENCY (GHz)

FIGURE 2.3-3

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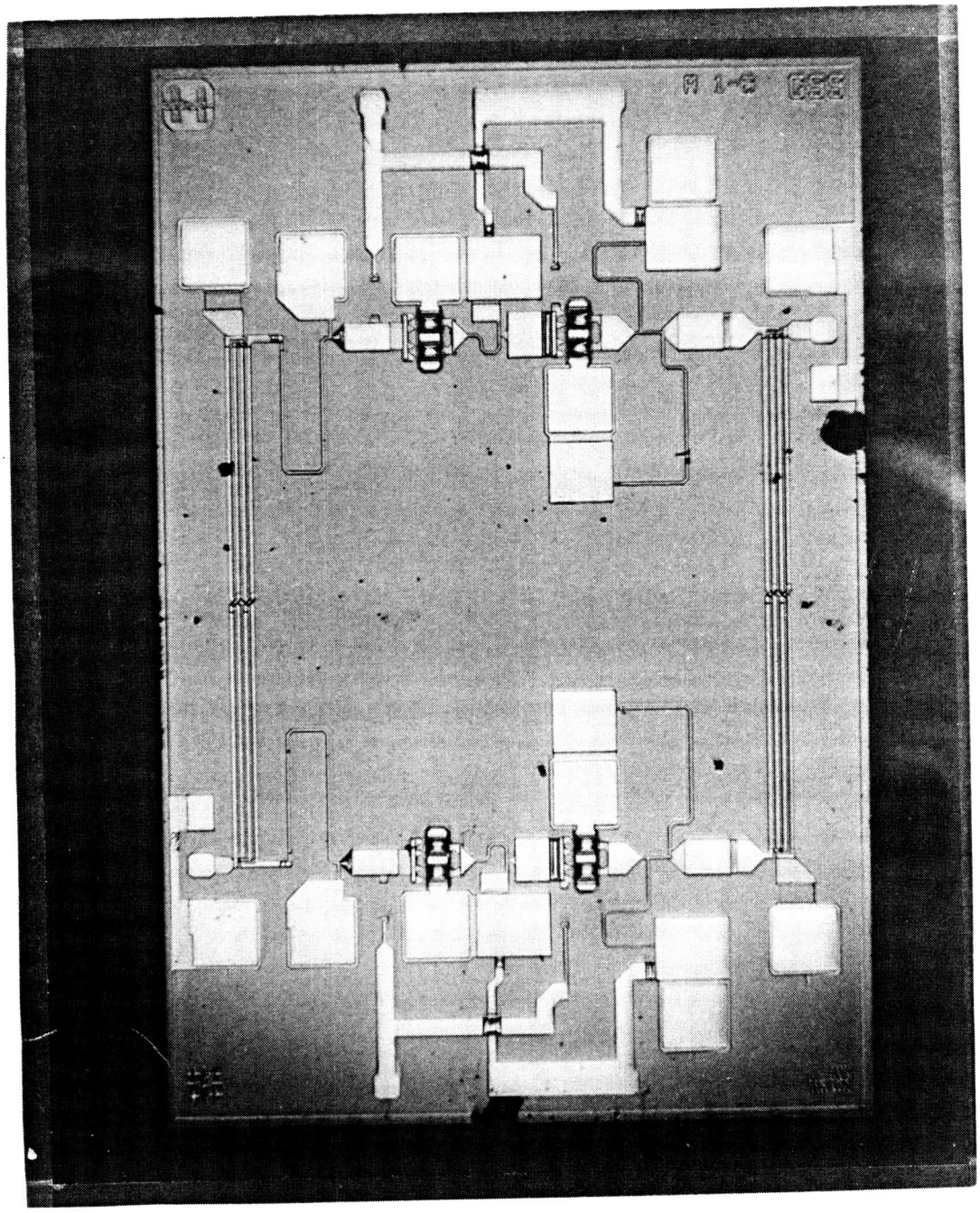


FIGURE 2.3-4 BALANCED 20 GHz MMIC AMPLIFIER

1.4:1. Because of this improvement in VSWR performance, the balanced RFA was selected as the baseline MMIC amplifier.

The RF yield of the balanced amplifiers was found to be in excess of 25% on all three wafers fabricated. All amplifiers from the first wafer probed show a good grouping of performance data as shown in Figure 2.3-5. The second and third wafers were probed giving similar mean values for the amplifier to those obtained from the first wafer. Noise figure performance was not as good as expected (9 dB vs. 5 dB), but this had virtually no impact on receiver noise figure performance, as analysis will show.

RF BANDPASS FILTER

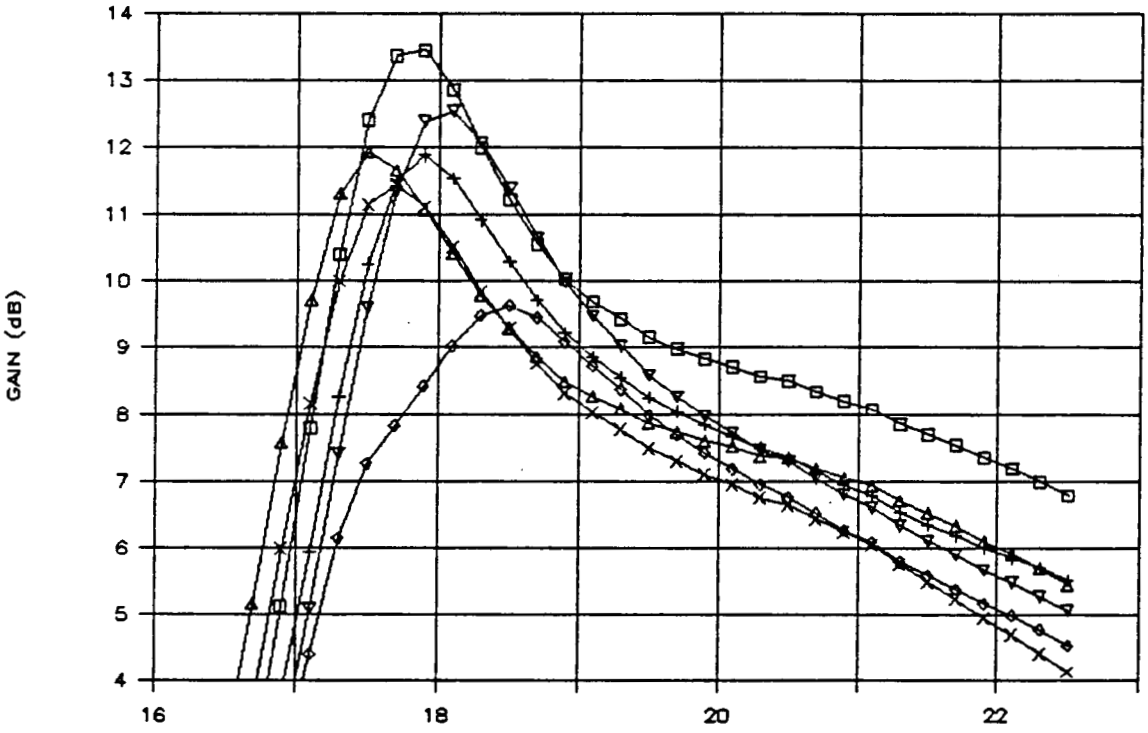
Test results for the breadboard RF filter show it to be within the allocated specifications on all but the VSWR and insertion loss requirements at the band edges. We believe these out-of-spec areas, which have only a minor effect on the overall receiver performance, to be due to the coaxial connectors used on the test fixtures. Coaxial connectors were required to determine the filter's out of band rejection.

The breadboard filter designed and fabricated was a five pole Chebychev microstrip coupled line filter on a 10 mil thick fused quartz substrate. Due to narrow coupled line spacings (1.1 mil), a glass mask was fabricated to insure artwork accuracy. Figure 2.3-6 is a picture of the filter in its test fixture, and Figure 2.3-7 shows the wideband response for the same filter. The out-of-band rejection at frequencies of 14 GHz (Image) and 22.2 GHz are well within the requirements of 40 and 20 dB, respectively. The filter requirement could have been met with a four pole filter since the balanced RFA has a steep low frequency roll-off and the mixer has good spur performance which reduces the required out-of-band rejection needed.

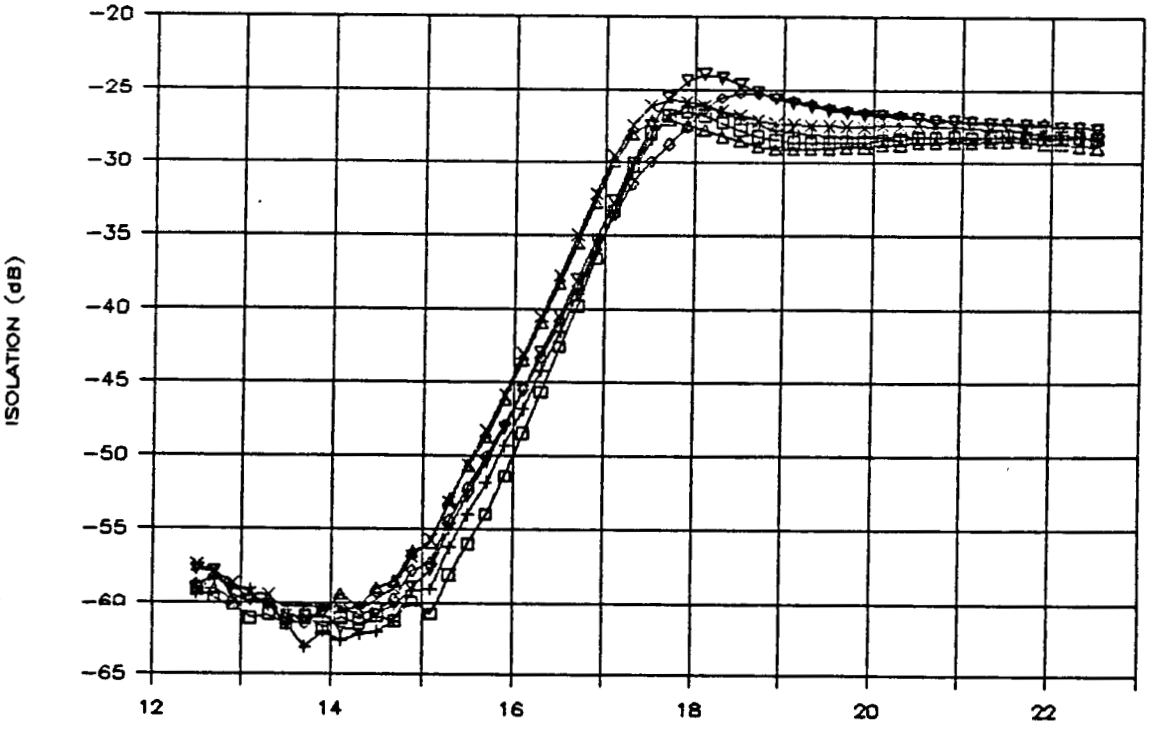
MMIC IMAGE REJECT MIXER

The test results for the MMIC IRM show adequate overall mixer performance such that an additional design iteration (and MMIC wafer run) was not necessary. The mixer block diagram is shown in Figure 2.3-8, and a picture of the fabricated MMIC is shown in Figure 2.3-9. The IRM uses three Lange couplers in its design which is the same coupler used in the balanced RFA. There are two IF outputs, in quadrature, requiring a hybrid to recombine them. The hybrid combines those signals created by the undesired image input so that the quadrature inputs cancel each other and the result goes to the terminated port. The desired signals are combined in phase and the sum is sent to the output port. Since the balanced RFA performed well, it was expected that the IRM couplers would also perform well. The data taken on the IRM verifies that it is basically a Class II mixer (higher conversion loss, intercept point and LO drive required) and that the balance and isolation qualities are acceptable for the NASA-Lewis

BALANCED AMPLIFIER'S GAIN



BALANCED AMPLIFIER'S REVERSE ISOLATION



□ 84-6 + C8-1 ◇ D9-1 △ A9-6 X D5-4 ▽ D5-7

FIGURE 2.3-5

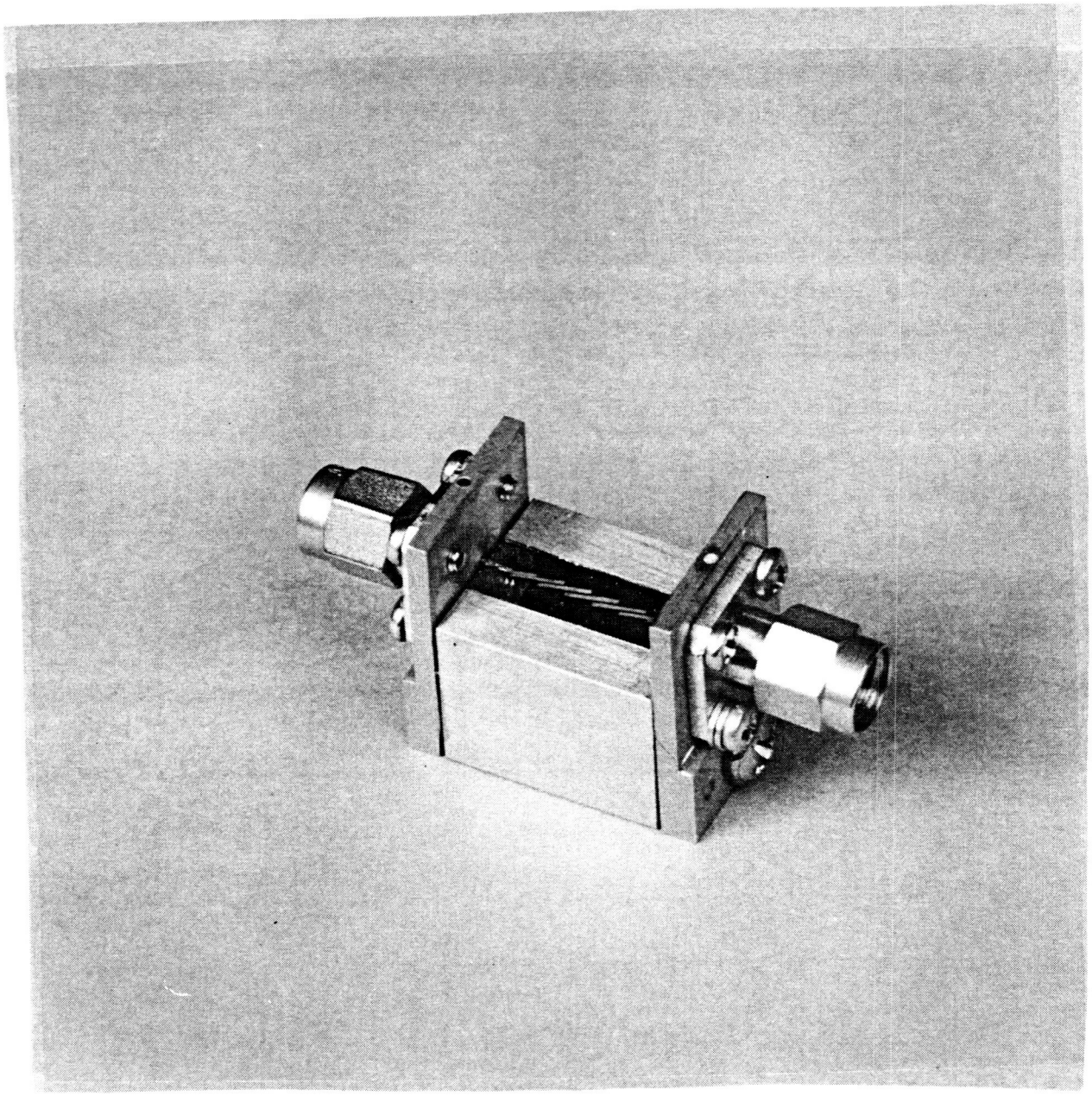


FIGURE 2.3-6 20 GHz RF BANDPASS FILTER

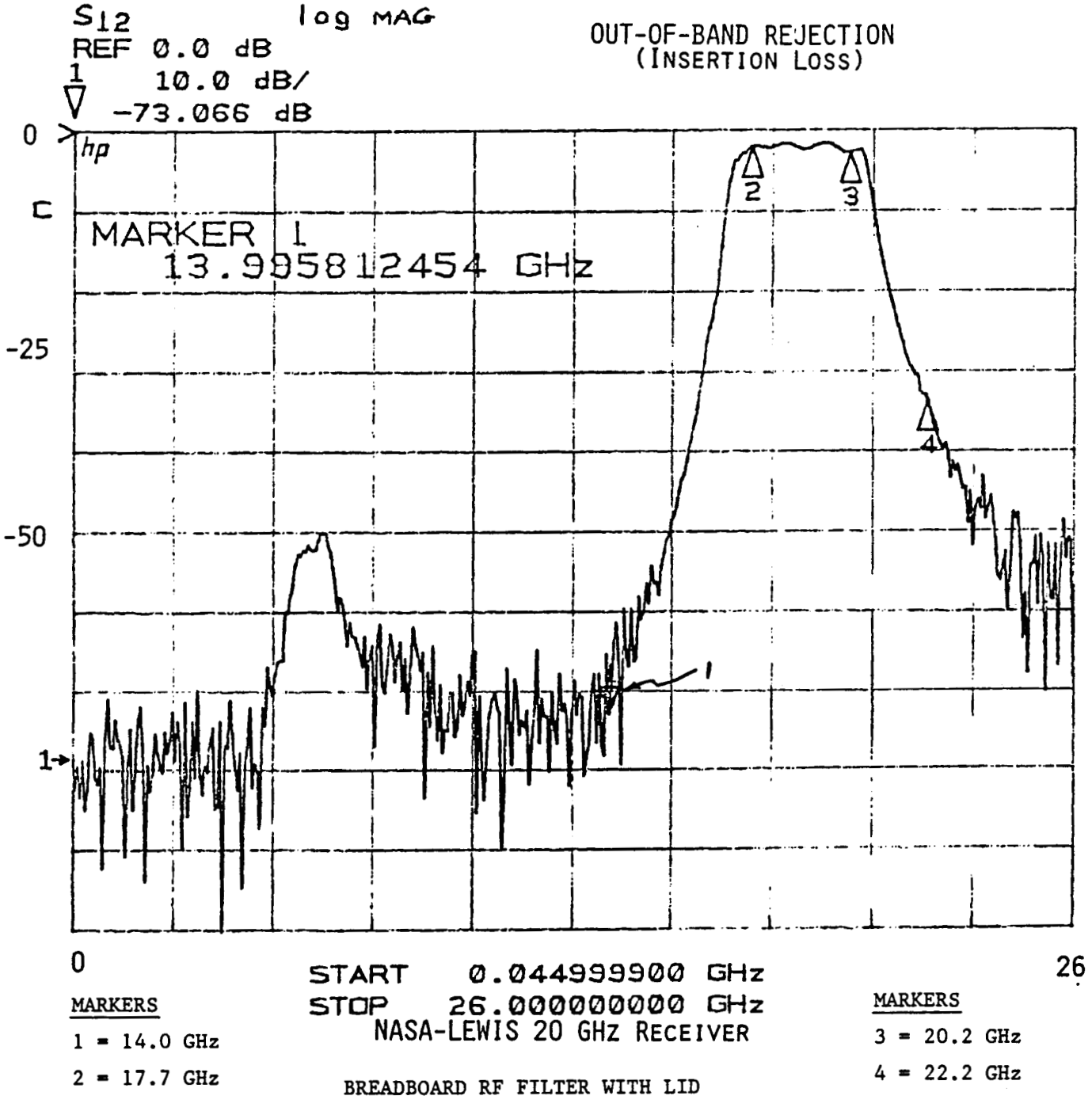

S12
log MAG
REF 0.0 dB
1
10.0 dB/
-73.066 dB
OUT-OF-BAND REJECTION
(INSERTION LOSS)
0
-25
-50
hp
MARKER 1
13.995812454 GHz
2
3
4
1
0
26
START 0.044999900 GHz
STOP 26.000000000 GHz
NASA-LEWIS 20 GHz RECEIVER
MARKERS
1 = 14.0 GHz
2 = 17.7 GHz
MARKERS
3 = 20.2 GHz
4 = 22.2 GHz
BREADBOARD RF FILTER WITH LID

FIGURE 2.3-7

NASA IMAGE REJECT MIXER

(1/2 MICRON MMIC)

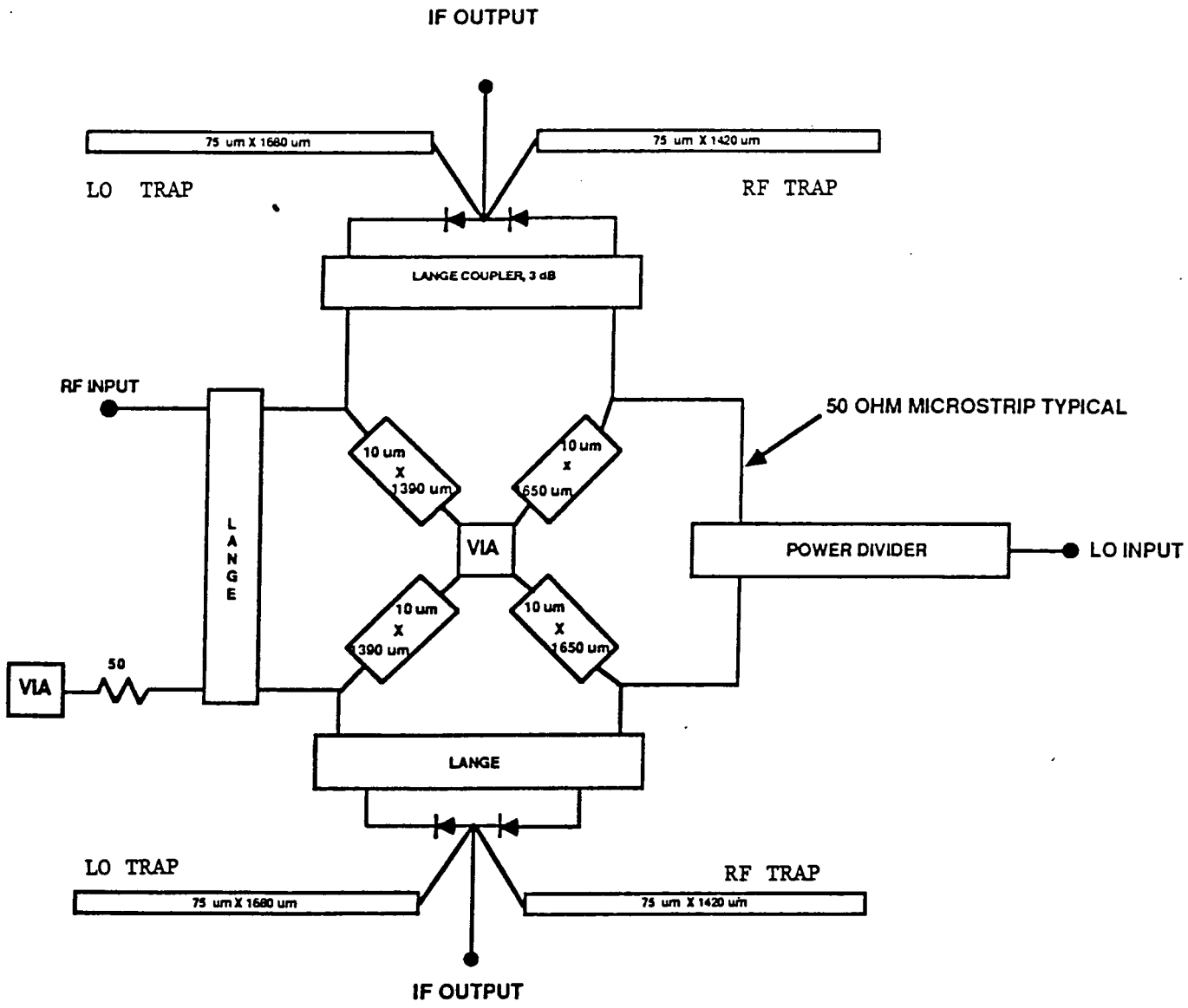


FIGURE 2.3-8

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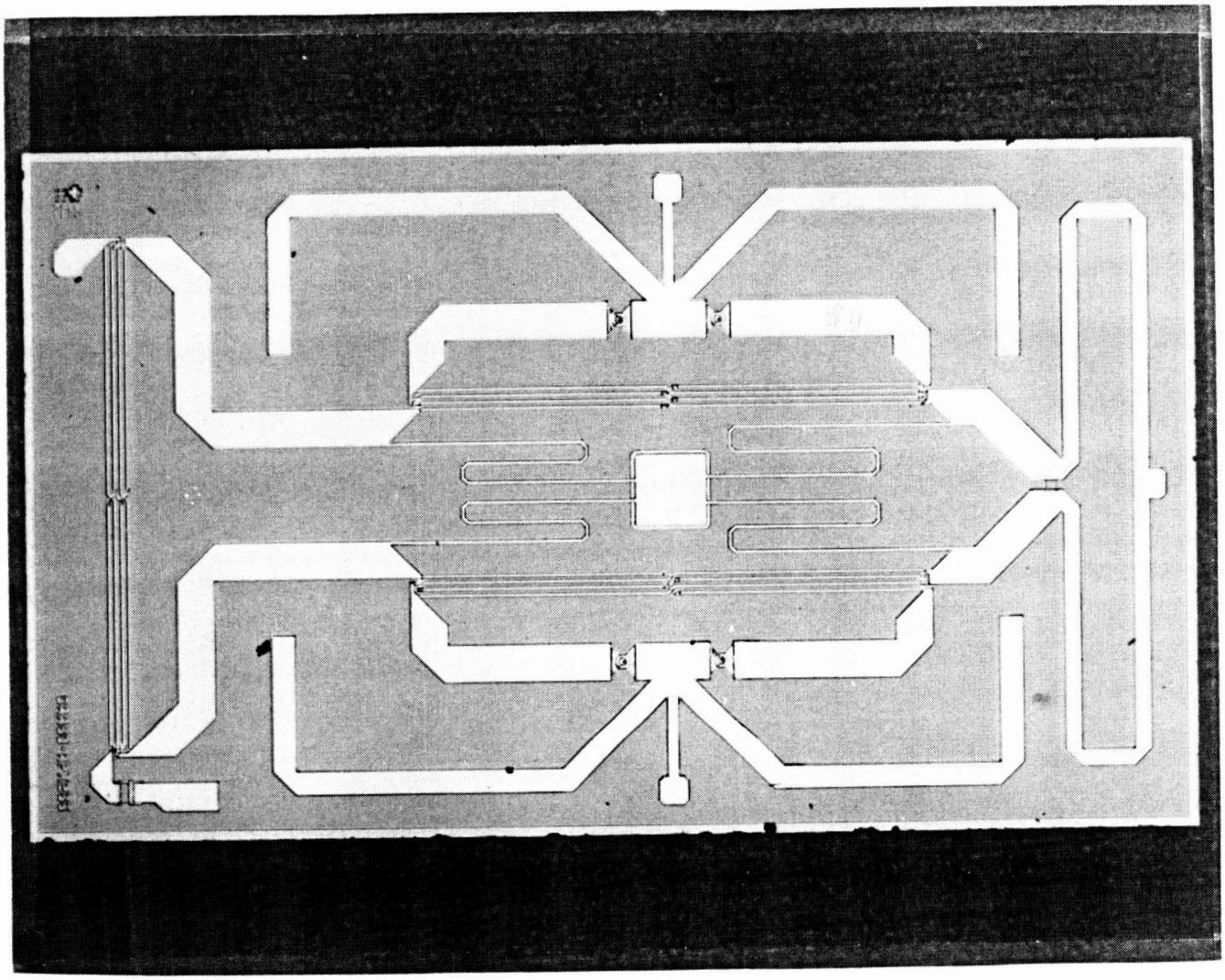

FIGURE 2.3-9 MMIC IMAGE REJECT MIXER

20 GHz POC receivers.

Figure 2.3-10 shows conversion loss versus frequency. The graph plots the mixer's conversion loss versus IF frequency for six different fixed LO frequencies across the band. A high local oscillator power of +17 dBm was found to give the best results for both conversion loss and intercept point. HP BASIC and Lotus spreadsheet programs were written to automatically take the data, correct for test fixture insertion losses and minimize errors. Each data point, signified by each symbol on the lines plotted, was measured four times and averaged to minimize the influence of noise and any oscillator power fluctuations, etc. The programs and methods used to gather the IRM data were used to develop the automated gain and ripple testing in the POC Test Plan.

Actual measurements were made from the RF input to the I and Q IF outputs. However, the data displayed is for the IRM with an ideal quadrature hybrid connected at its output, although the impact of a non-ideal hybrid was found to be insignificant. Hybrid errors had more of an effect on image rejection, a feature that was not necessary due to the preselect filter and input waveguide.

The graph shows the conversion loss is approximately 13 dB for a +17 dBm LO drive. This measurement was taken using a power meter, and it was later determined that there was no low pass filter in the measurement system allowing local oscillator leakage to contaminate the measurement. Subsequent measurements in Task V showed a typical insertion loss of 16 dB for the mixer. Part of the gain ripple is due to VSWR ripple from the coaxial test fixture used in measuring the IRM's performance.The VSWR of the test fixture is not as good as the microstrip ribbon bonds which were used in the integrated POC receivers.

Figure 2.3-11 gives the spur chart developed for in-band and out-of-band spurious signals for the NASA-Lewis frequency plan. The IRM as used in the POC receivers has a maximum input power level of -12 dBm. Therefore, the highest spur level is be -46 dBc (-44 dBc due to the 2x3 spur less 2 dB from being backed off 2 dB in drive from -10 dBm).

HYBRID/BANDSTOP FILTER

The IF Hybrid/Bandstop Filter is used to combine the quadrature outputs of the IRM. The Bandstop Filter rejects the LO frequencies and prevents over-driving the MMIC IF amplifier which follows the hybrid. A bandpass filter is not required as one is contained within the modem used with the POC receiver. Figure 2.3-12 is a picture of the breadboard IF Hybrid/Bandstop Filter. This circuit operates from 3.1 to 3.6 GHz with low loss and rejects 14.3 to 16.8 GHz leakage signals from the local oscillator.

Figure 2.3-13 gives the measured performance of the breadboard

IMAGE REJECT MIXER CONVERSION LOSS

(+17 dBm LO)

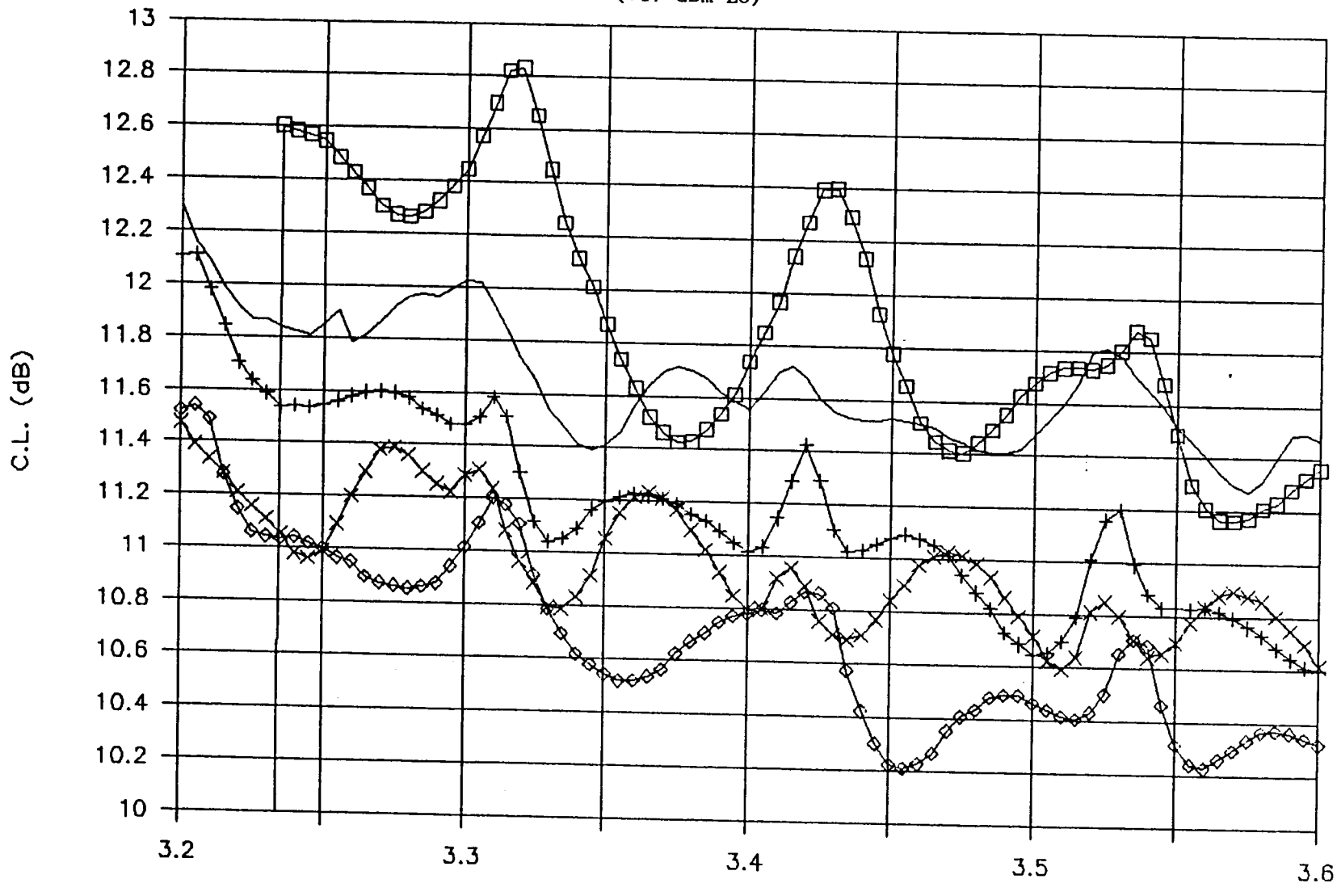

FIGURE 2.3-10

IRM SPUR CHART

(dB BELOW CARRIER)

RF FREQUENCY MULTIPLE (M)						
	5					>56
	4				>60	>60
	3			>61	>59	
	2		46 / 52	44 / 60		
	1					
	0	1	2	3	4	5

LO FREQUENCY MULTIPLE (N)

LO @ +12 dBm RF @ −10 dBm / LO @ +17 dBm RF @ 0 dBm	LO @ +12 dBm RF @ −10 dBm

FIGURE 2.3-11

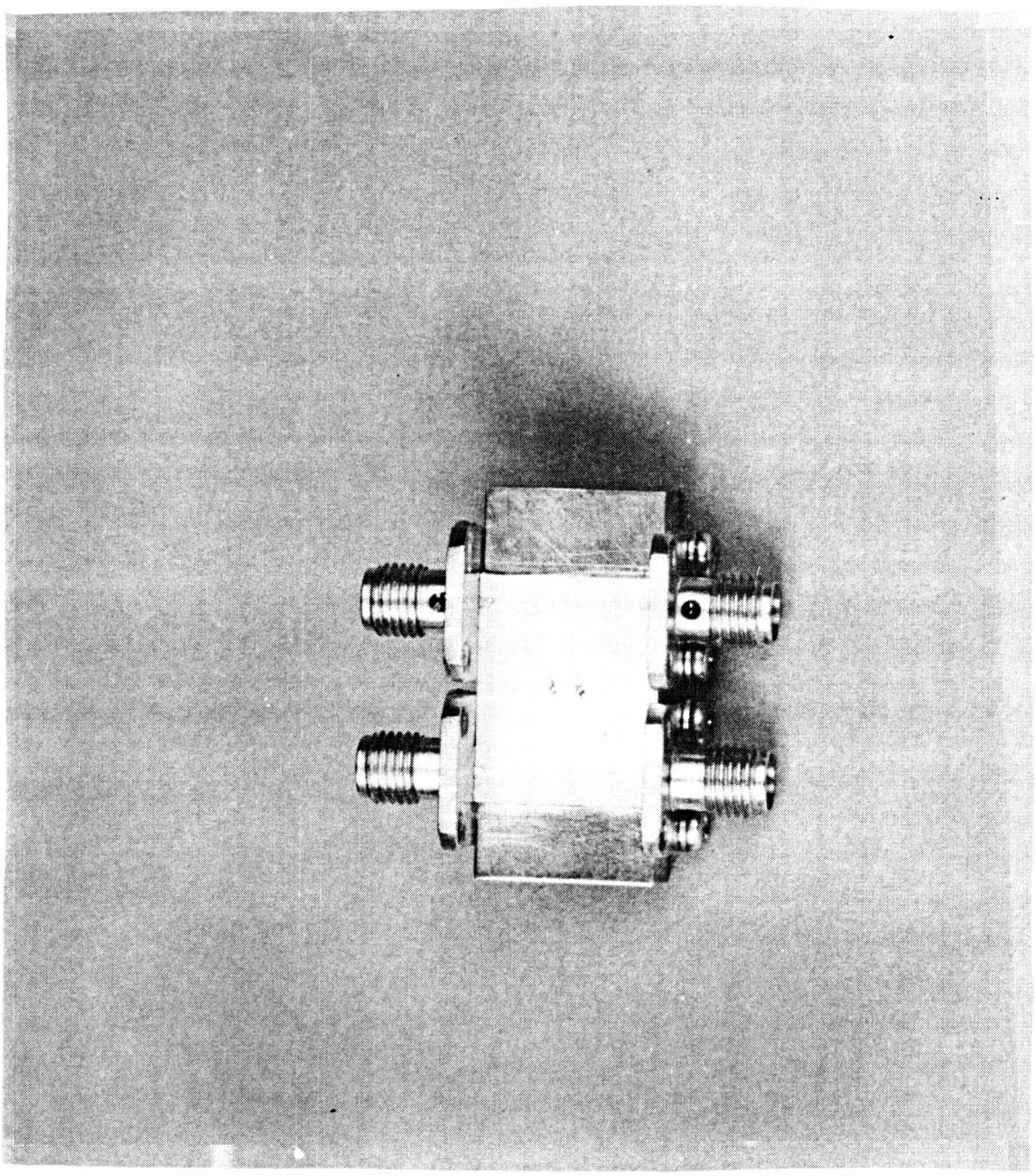

FIGURE 2.3-12 IF HYBRID/ BANDSTOP FILTER

IF HYBRID AND BANDSTOP FILTER

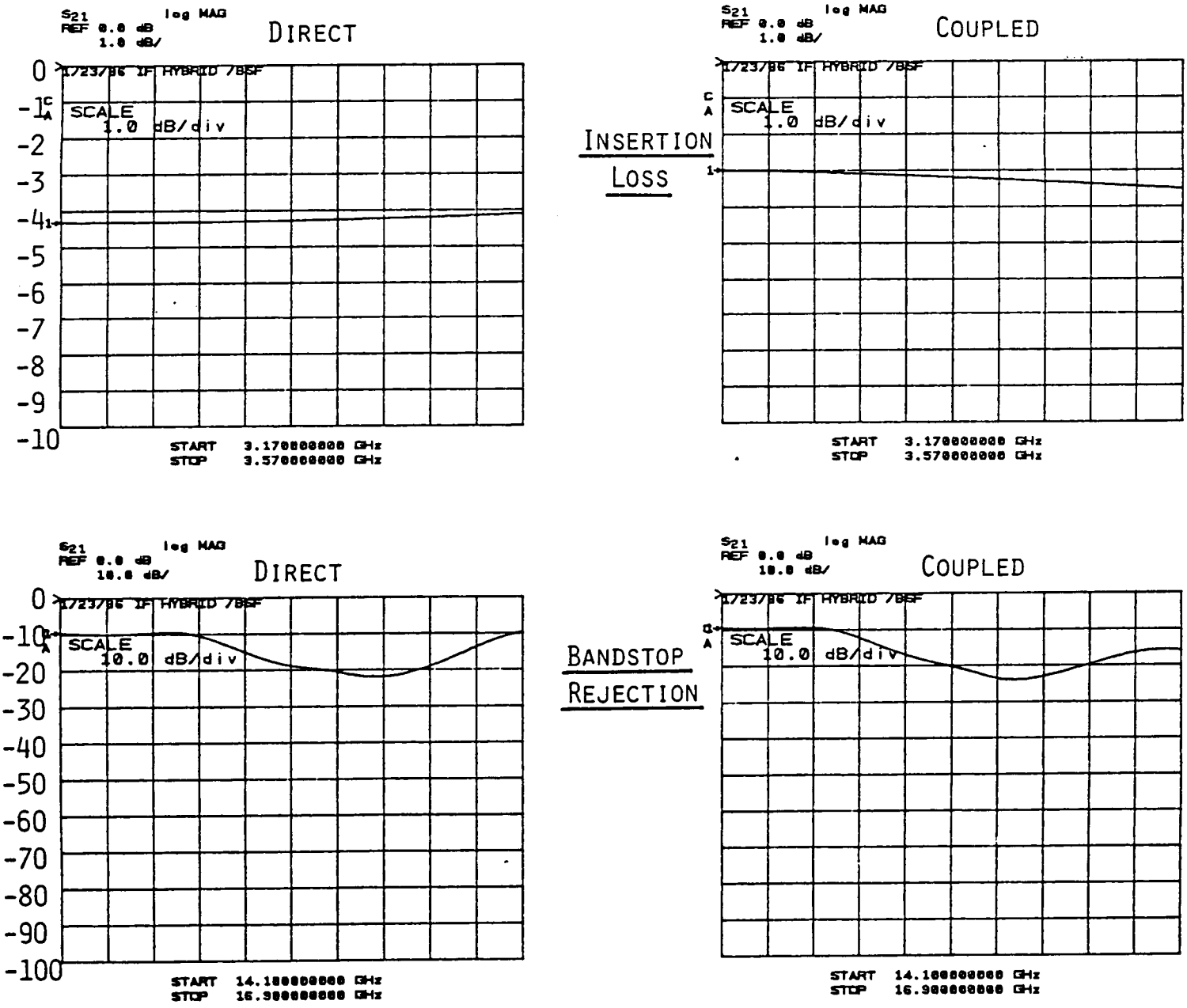

FIGURE 2.3-13

Hybrid/BSF. It can be seen that the coupler is overcoupled by not obtaining balanced direct and coupled port insertion loss performance. This resulted from the circuit being slightly over-etched during fabrication. This was later corrected by adjusting the coupler line widths and spacings to account for the overcoupling. Also, an additional BSF stub was later added during Task IV to realize a flatter rejection of approximately 20 dB over the entire LO band.

DC REGULATOR

The DC regulators in the receiver use +/-15 volts from the outboard power supply to produce the required voltages at each functional block within the receiver. Since the final voltages were not available during the breadboard phase, broad ranges of voltages and currents were established. Therefore, a general regulator design was derived and tested at various voltage and current levels.

Figure 2.3-14 shows the schematic for a positive regulator used for LNA drain bias. These regulators have a slow turn-on circuit (a 2N2907 at the output side of the LM317 regulator) which allows the negative gate bias voltages to stabilize before the drain voltage is applied. The positive regulator ICs give approximately a one volt step output at turn-on, independent of the slow turn on circuitry. The output diodes in the positive regulators ensure that the overall regulator's output is kept at zero volts at turn on and rises slowly to the desired value. This prevents possible burn-outs at turn on.

A transistor at the input of each regulator IC (LM317/337) and the two diodes which are in parallel with the current limiting resistor, R_{C1}, limit the initial current surge at turn on to less than twice the nominal operating current. The diode immediately before the regulator IC provides reverse polarity protection in conjunction with the current limiting transistor.

One resistor, R_{C1},is a select at test resistor. Its value depends on the I-V (current-voltage) relationships of the two input current limiting diodes. Its value is selected to give a turn-on surge current to nominal current ratio of approximately 1.5:1. This leaves a +/- 0.5 V margin for temperature variations. A potentiometer is used for each unique FET drain voltage and for each FET gate bias.

IMPACTS ON POC RECEIVER DESIGN

The POC Receiver's performance using the measured breadboard data for all components but the LNA was predicted and is shown in Table 2.3-1. Data for the LNA's performance was taken from a Super-COMPACT prediction based on the replacement HEMT FET (NE 202) from NEC. The receiver analyzed consisted of an external (waveguide) input circulator, four stage HEMT LNA, one balanced RFA, RF filter, IRM, Hybrid/BSF, and an IF amplifier. A block

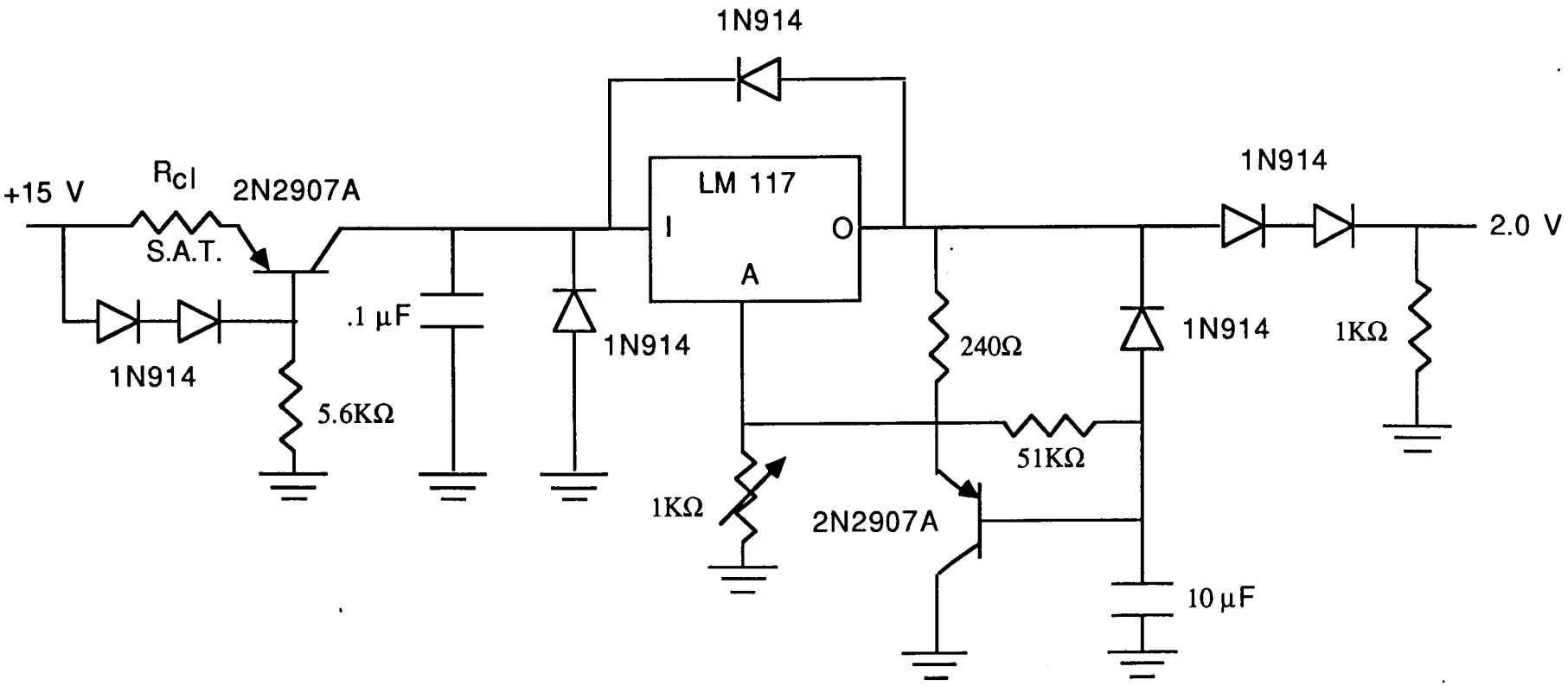

FIGURE 2.3-14 POSITIVE DC REGULATOR SCHEMATIC

PREDICTED 20 GHz RECEIVER PERFORMANCE

BASED ON BREADBOARD DATA & NEW 1/3 um HEMT

PERFORMANCE OVER TEMPERATURE — 18 GHz DATA ********** — SPECIFICATIONS (-30 oC < TA < +75 oC)

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	36.3	47.3	1.92	160.8	-32.9	30.0	3.5	-30.0
-25.0	35.7	46.7	2.21	192.0	-31.9	30.0	3.5	-30.0
0.0	35.1	46.1	2.50	226.0	-31.0	30.0	3.5	-30.0
25.0	34.5	45.5	2.81	263.3	-30.1	30.0	3.5	-30.0
50.0	33.9	44.9	3.11	304.0	-29.3	30.0	3.5	-30.0
75.0	33.3	44.3	3.43	348.6	-28.5	30.0	3.5	-30.0
100.0	32.7	43.7	3.75	397.5	-27.7	30.0	3.5	-30.0

PERFORMANCE OVER TEMPERATURE — 19 GHz DATA ********** — SPECIFICATIONS (-30 oC < TA < +75 oC)

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	35.3	46.8	1.92	161.2	-31.3	30.0	3.5	-30.0
-25.0	34.7	46.2	2.21	192.5	-30.3	30.0	3.5	-30.0
0.0	34.1	45.6	2.51	226.6	-29.5	30.0	3.5	-30.0
25.0	33.5	45.0	2.81	264.0	-28.6	30.0	3.5	-30.0
50.0	32.9	44.4	3.12	304.8	-27.8	30.0	3.5	-30.0
75.0	32.3	43.8	3.43	349.4	-27.0	30.0	3.5	-30.0
100.0	31.7	43.2	3.75	398.3	-26.2	30.0	3.5	-30.0

PERFORMANCE OVER TEMPERATURE — 20 GHz DATA ********** — SPECIFICATIONS (-30 oC < TA < +75 oC)

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	33.3	43.8	1.94	162.8	-28.9	30.0	3.5	-30.0
-25.0	32.7	43.2	2.23	194.5	-27.9	30.0	3.5	-30.0
0.0	32.1	42.6	2.53	229.3	-26.9	30.0	3.5	-30.0
25.0	31.5	42.0	2.84	267.3	-26.0	30.0	3.5	-30.0
50.0	30.9	41.4	3.15	308.9	-25.1	30.0	3.5	-30.0
75.0	30.3	40.8	3.47	354.5	-24.2	30.0	3.5	-30.0
100.0	29.7	40.2	3.79	404.4	-23.4	30.0	3.5	-30.0

4 STAGE LNA AND BB MMICS MEET SPEC

TABLE 2.3-1

diagram of the new receiver baseline design is shown in figure 2.3-15. The receiver's performance was analyzed at 18, 19 and 20 GHz. In all but the 18 GHz case, all specifications were met. The only exception was for intercept (compression) point at 18 GHz, and then only at low temperatures.

Predicted overall receiver performance was compliant with the NASA-Lewis specifications (except for intercept point performance at cold temperatures). Therefore, no additional MMIC design iterations were required. The MMICs could have been improved, but their improvement was not required for successful POC receiver integration and test.

Task III, POC Plans and Specs, was a relatively short task. The main outputs were revisions of the various specifications written in Task I, most importantly the Local Oscillator Specification, since this was a purchased item. Also, the Interface Control Document and Receiver Proof of Concept Test Plan were written.

2.4 TASK IV SUMMARY

Task IV was the final POC design phase, which culminated in the CDR at Lewis Research Center. During this task, the new LNA was designed, the receiver module package was designed, and the DC Regulator printed wiring card was laid out. Some of the components that were breadboarded were redesigned during this phase. Extensive electrical, mechanical, and thermal modeling were conducted.

The baseline electrical design was based on the breadboard data taken during Task II, with the exception of the LNA, which was a new design. The new LNA was simulated on SuperCOMPACT, and reviewed at CDR.

Receiver budgets were modeled for noise figure, gain, intercept point, VSWR, AM-PM conversion, gain ripple, group delay, phase noise, and spurious response. The receiver design was found to be spec compliant except for intercept point at low temperature at 18 GHz.

Gain, noise figure, and intercept point were predicted over temperature using a Lotus spreadsheet template. The template used well-known exponential relationships to vary each component's gain, noise figure and intercept point over temperature. Given the expected LNA results, a gain of 30.3 dB with a 3.47 dB noise figure was predicted at 20 GHz. Because of the higher gain at cold temperatures, input intercept point was expected to be -32 dBm at 18 GHz. The results of this simulation are shown in Table 2.3-1.

Three provisions for gain control were added to the receiver

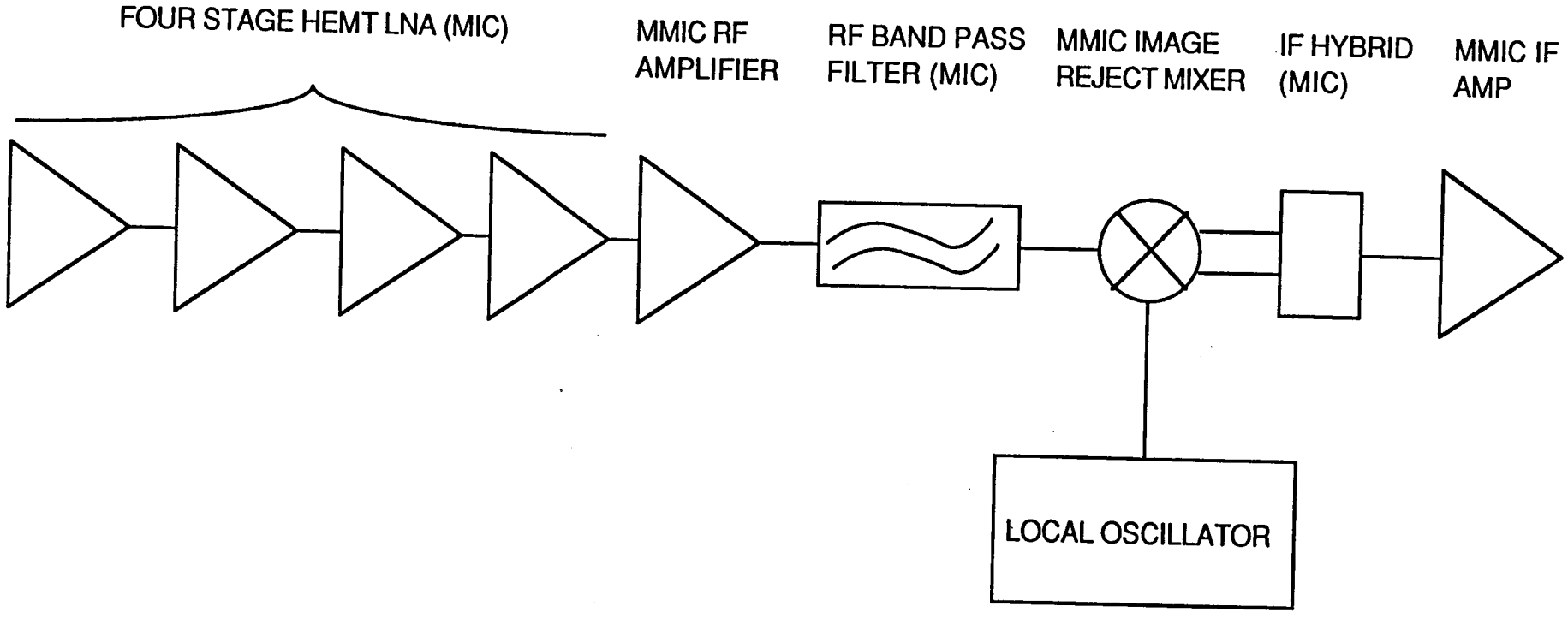

FIGURE 2.3-15 REVISED RECEIVER DESIGN BLOCK DIAGRAM

during the design task. The first was a thermistor controlled adjustment of the gate bias of the last LNA stage, so that the gate bias would be made more negative at cold temperatures, lowering the drain current and gain of the FETs. This would lower the power level into the mixer, the component that establishes intercept point. Also, a small length of transmission line was added before the mixer so that RF absorber material could be used to reduce gain if the LNA gain was as high as SuperCOMPACT predicted. If the LNA gain was 40 dB, the intercept point would miss specification by 6 dB. A provision was also made for an IF attenuator to control overall gain over temperature. A PIN diode attenuator and driver circuit were designed, and space was allocated in the receiver design and regulator PWB. In the event the attenuator was not used, a DC block substrate could be inserted in its place to DC isolate the mixer and the MMIC IF amplifier. The receivers delivered on this contract used the DC block.

The LNA was designed using a quartz substrate and unpackaged HEMT chips for the best 20 GHz performance. The baseline design was to use four identical stages so that the stage with the lowest noise figure could be selected as the first stage. The simulation of the amplifier stages took into account gain, noise figure, output VSWR, gain flatness, stability, and cascadability. Optimizations were done with identical amplifiers cascaded, so that interstage effects could be eliminated. Because of the device's high gain, stability was a definite design consideration, especially at frequencies below the band of interest. After investigating many possible circuit topologies, low pass networks shunted to ground were used on both the input and output of each stage. These networks also provided impedance matching and DC bias for the transistors.

Figure 2.4-1 is a plot of the simulation results for gain and noise figure of two cascaded stages. Four cascaded stages were predicted to provide 40 dB of gain, while the receiver model called for only 34.4 dB. The noise figure had a -.01 dB margin, to be made up for in the receiver by the excess gain.

The other component that was redesigned in Task IV was the IF hybrid/ bandstop filter. The version breadboarded in Task II was overcoupled, producing less than optimal combining. Over-etching was part of the problem, and a more tolerant cross section with wider coupled lines and more spacing was selected. The first bandpass filter design had low rejection for the LO band, so an extra open stub was added to the design, which was then modified empirically for 20 dB of rejection across the band.

Another major design effort on Task IV was the packaging design. Because of the developmental nature of many of the components, especially the LNA, a circuit subcarrier approach was used. Individual components, such as a single LNA stage, or a MMIC chip with interconnect substrate, were placed on carriers made of metal whose thermal expansion coefficient matched that of the

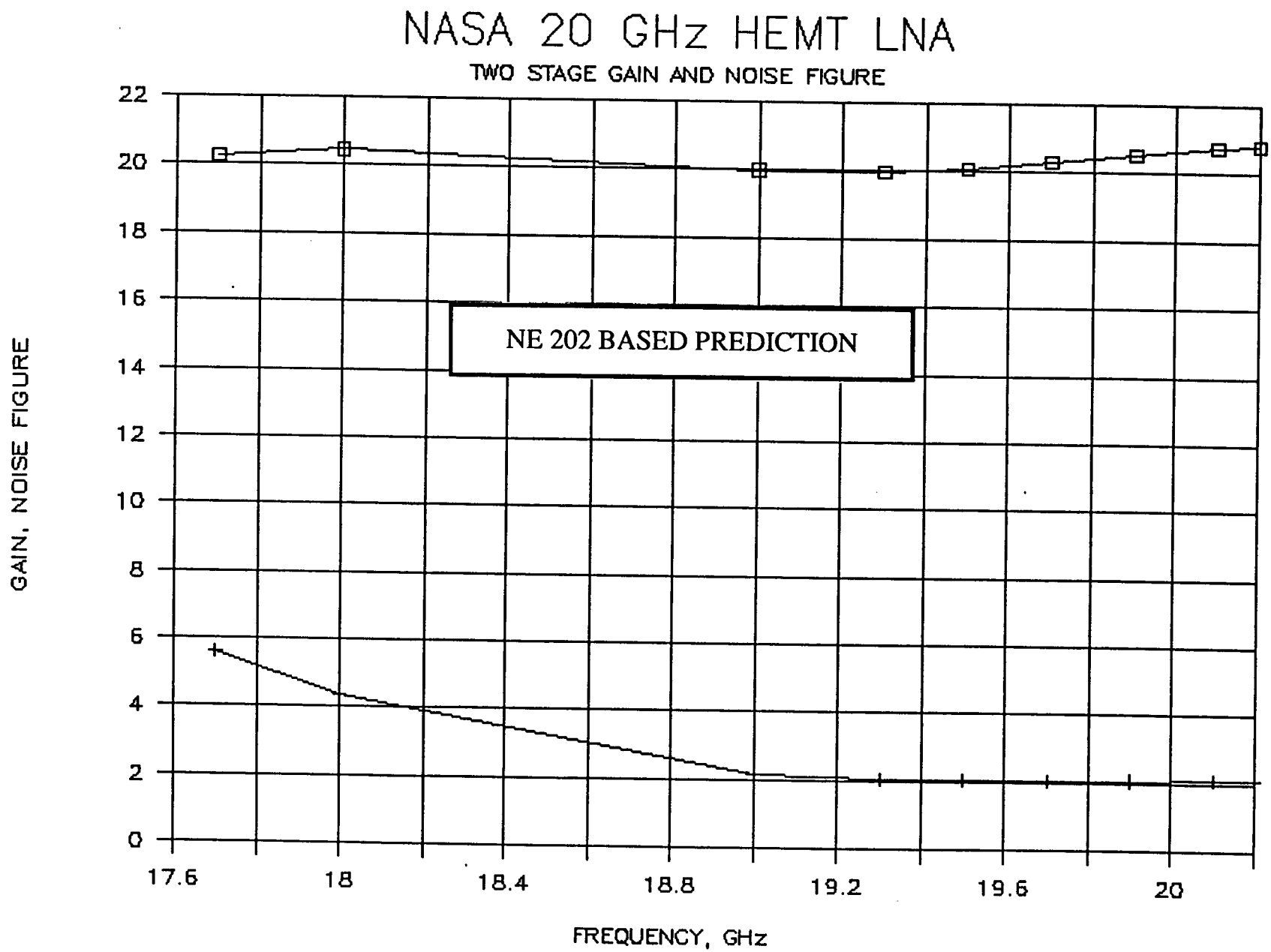
NASA 20 GHz HEMT LNA
TWO STAGE GAIN AND NOISE FIGURE
NE 202 BASED PREDICTION
GAIN, NOISE FIGURE
22
20
18
16
14
12
10
8
6
4
2
0
17.6
18
18.4
18.8
19.2
19.6
20
FREQUENCY, GHz

FIGURE 2.4-1

substrate material. Invar was used with quartz substrate, while aluminum was used for the Duroid 6010 soft substrate. The Invar was also beneficial for the LNA and MMIC chips because its expansion coefficient is close to that of Gallium Arsenide. The carriers are held down by 0-80 screws and D, lock, and flat washers. The circuits are interconnected by soldered gold ribbons.

The receiver module was designed with two cavities- one for RF and IF components, and one for the DC regulator board. The cavities were connected electrically by soldered-in glass feed-throughs. The local oscillator is external to the receiver module, and the signal is fed in via an SMA connector with external seal and coax in the DC cavity. This coax is connected to a sparkplug SMA connector feeding to a specially designed 90 degree launchers to the image reject mixer carrier assembly. The input of the receiver module is WR-42 waveguide, extended to provide for attaching a circulator. The waveguide to microstrip transition uses a glass bead feed-through, sliding contact in waveguide, dielectric probe cover, and adjustable short. This method allows sealing the RF cavity from the outside environment, unlike most similar transitions. The IF output is an SMA sparkplug connector. The RF cavity lid is attached with conductive epoxy, and the DC cavity lid uses flathead screws and an "O" ring. The package is designed to keep moisture out of both cavities. It is not a hermetic design, but is sufficient to prevent contamination from the environment.

A thermal analysis was conducted for the receiver, and it was determined that a finned heat sink plate was required because of the power dissipation of the local oscillator, as specified by the vendor. The original size estimate was 20 inches square, later modified to 14 inches square when it was found that local oscillator power dissipation was typically lower than specified, especially at high temperature where the crystal ovens are not turned on.

2.5 TASK V SUMMARY

In Task V, the receivers and their subassemblies were fabricated and tested. This included machining of carriers, receiver module housing, baseplate, and assorted top level parts. Substrates were fabricated and the individual circuit assemblies were built and tested, where applicable. The receivers were then assembled and functionally tested. Figure 2.5-1 depicts the top level assembly of the receiver, including the local oscillator and baseplate. Figure 2.5-2 shows the receiver module with the RF cavity exposed. The results from the testing were presented at a review held at Harris.

The RF and IF circuit carriers were machined individually, due to the low quantities required (three for most, twelve for LNA). The overall receiver housings were fabricated on a numerically controlled mill because of their complexity. A numerically

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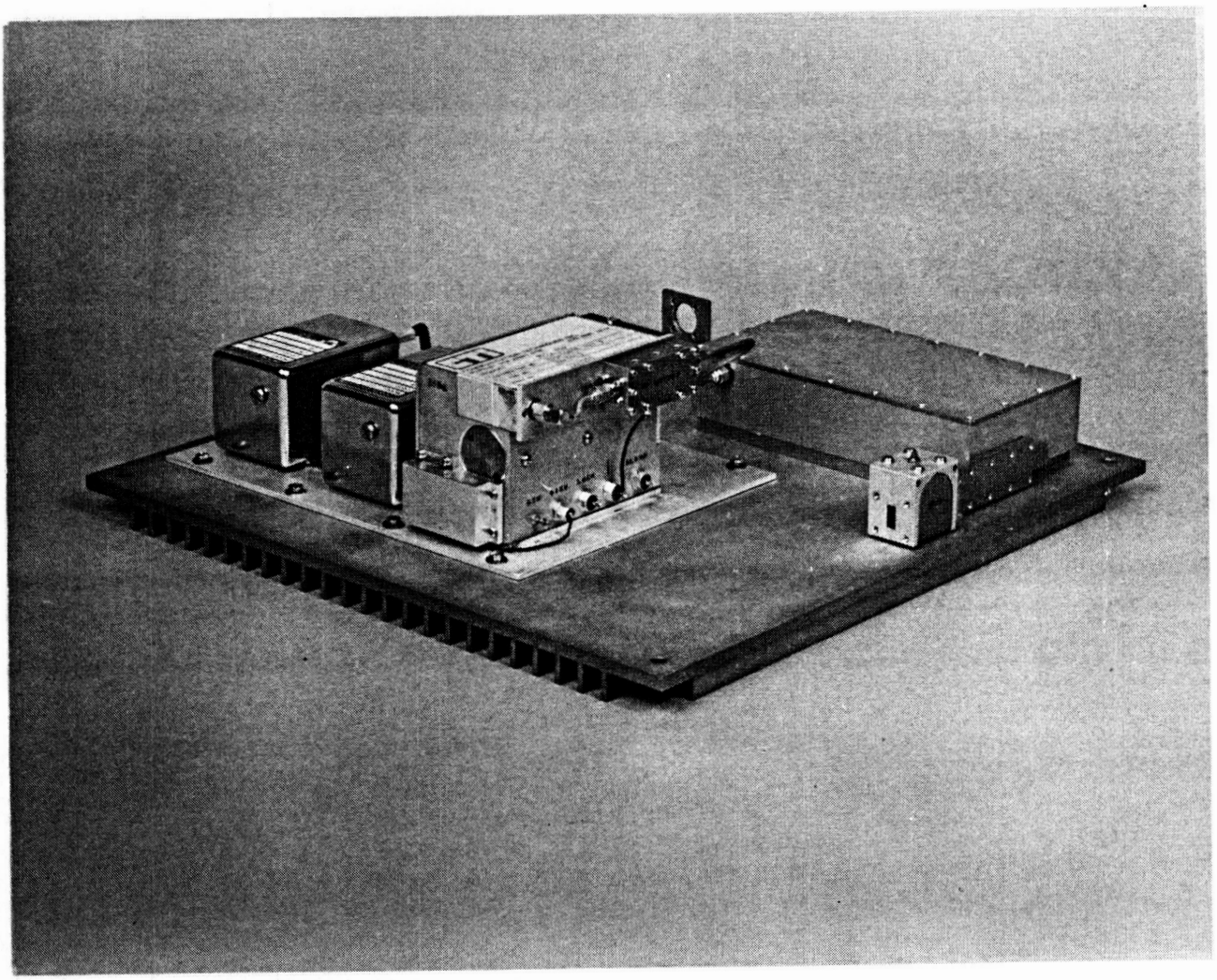

FIGURE 2.5-1 20 GHz RECEIVER TOP LEVEL ASSEMBLY

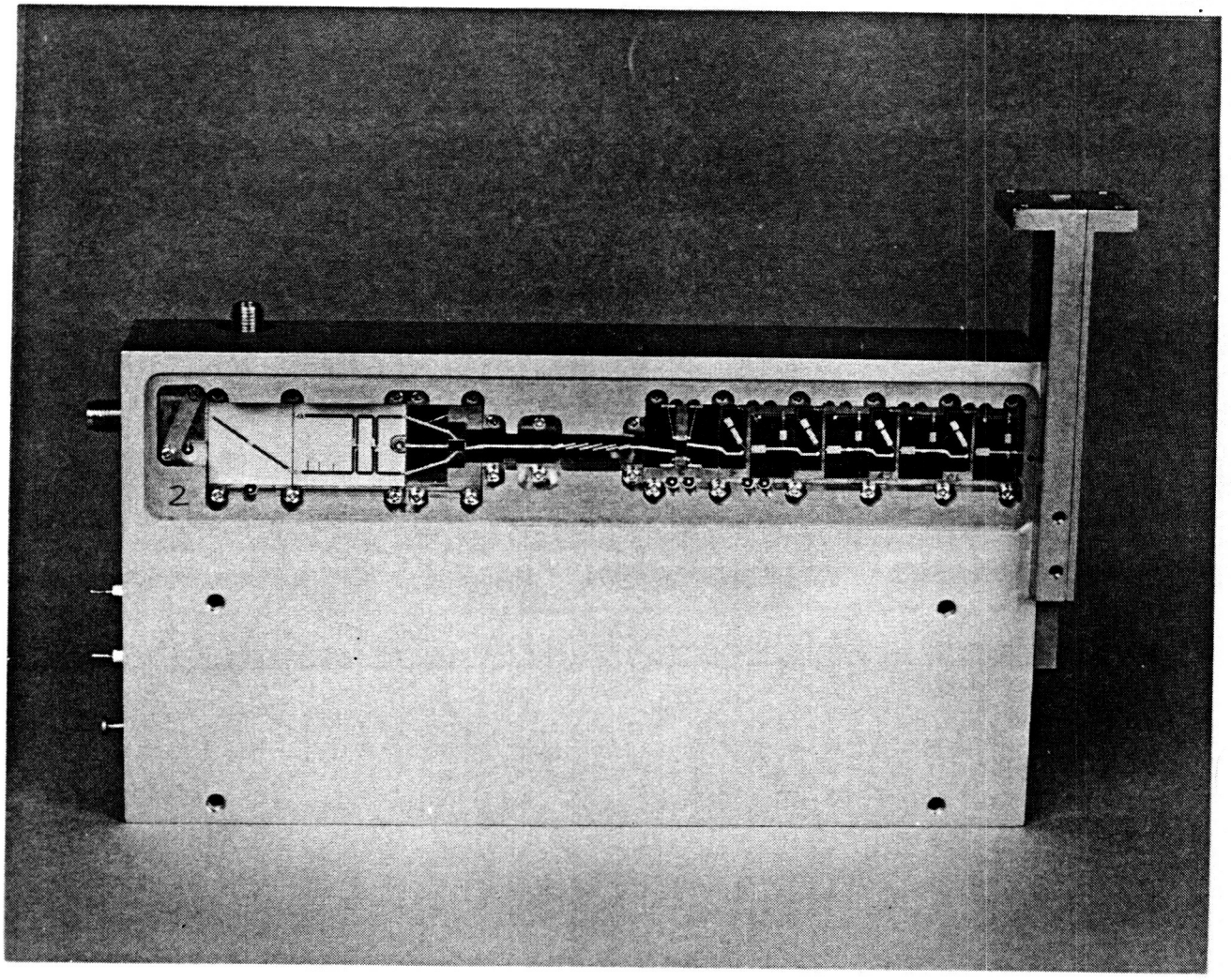

FIGURE 2.5-2 20 GHz RECEIVER MODULE WITH RF CAVITY EXPOSED

controlled mill was also used for the finned baseplate, due to the amount of repetitive cutting.

Almost all of the assembly and test work was done in the design engineering laboratories. GaAs device mounting and wire bonding were done in the engineering hybrid laboratory. Two different chemical labs were used for substrate etching, and quartz substrates were diced at another hybrid lab within Harris.

Since most of the component designs were proved in earlier tasks in the program, an abbreviated test plan was used for the RF and IF assemblies. The most extensive tests were conducted on the LNA, because the new design had not been tested during the breadboard stage. Gain, noise figure, and return loss were tested for both single and cascaded stages.

LNA measurements indicated that noise figure approached expected performance, but gain was quite low. Single stage noise figure in the required frequency bands (19.3 - 20.1 GHz) was typically 2.1 to 1.9 dB on average, as opposed to a simulated 1.8 dB. Single stage gain was typically 6.5 dB as compared to a specified 7.9 dB and a simulated 10 dB. When multiplied by four, this represented a significant gain degradation for the receivers and increased later stage noise figure contributions. The cascaded noise figures were from 1.7 to 2.6 dB. Cascaded gain was 26 db in the noise figure band and 30 dB from 18 GHz - 19.3 GHz.

The MMIC RF amplifiers had a 20 GHz spec of 6.5 dB gain and 10 dB noise figure. All of the chips used met or exceeded this.

Three of the components were not tested, due to their simplicity. The RF attenuator is simply a 50 ohm line, and the DC block is a 50 ohm line with a blocking capacitor. The RF bandpass filter is a printed circuit using a glass mask, so circuit accuracy is inherent.

The MMIC mixer and the MIC hybrid were tested together to determine overall system gain. According to the receiver budgets, 16 dB of conversion loss was allocated for the combination, and they met that spec.

The MMIC IFA specification was for gain of 13.0 dB +/- 1.25 db. The gain, including test fixture, for the chips used was 11 to 12 dB, which is slightly out of spec. Output VSWR for the IFA, which establishes the receiver output VSWR, was 1.4, compared to a spec of 1.5.

The local oscillators from CTI were compliant to the purchase specification, according to vendor tests and certificate of compliance. The units were functionally tested upon receipt.

After initial receiver assembly, the units were tested and aligned on Task V. For the first three units, noise figure was measured on the noise figure meter, and gain, gain ripple, gain

slope, and 1 dB compression point were measured on the automated gain setup, which is shown in Figure 2.5-3. The second three units were tested for noise figure and gain on the noise figure meter. All Task V tests were conducted at ambient temperature. Alignment was done while testing on the HP 8970 noise figure meter, which displays gain and noise figure simultaneously.

The manufacturing tests on the receivers were primarily a subset of the POC tests in Task VI. An additional test was done during Task V for the first three receivers. This was a gain test over an extended IF range (2 to 4 GHz) using the provided local oscillator inputs. The tests showed the receivers to have increasing gain below the specified IF frequency (3.185 GHz), due to increased RF and IF gain at lower frequencies. There was a roll off in higher frequency IF gain due to roll off of both RF and IF gain.

2.6 TASK VI SUMMARY

Proof of Concept testing was done at -30°C, 25°C, and 75°C on the receivers for many of the tests. Key data is presented here in graphical form. A model of the receiver was set up using data from the components as measured during Task V, and this model shows agreement with the measured performance. This model is used for analysis that shows what changes can improve future receiver performance. Recommendations for design modifications for production and follow-on technology development are presented.

This summary will present an overview of POC receiver data over temperature for the following: Noise Figure, Gain, Input Third Order Intercept Point, and Spurious Response. The data is presented in summary form except for gain and noise figure, which are presented graphically, with the specifications shown on the graphs.

The receiver technical goals called for 30 dB of gain minimum and 3.5 dB noise figure maximum over a temperature range -30°C to 75°C. The receivers fell short of this goal, as the graphs of noise figure and gain indicate (Figures 2.6-1 and 2.6-2). An analysis showing the problem areas in the receiver included in this summary.

The specification for gain ripple was +/- 1.5 dB per 150 MHz. There were several variances in the first build lot of the receivers, mostly at cold temperatures. The second build lot was compliant.

Gain slope is specified at 0.5 dB per 10 MHz maximum. There were variances in both lots of receivers, mostly at high temperatures. The first lot had more variation, as the gain was in general less uniform.

The intercept point specification is -30 dBm minimum. All the receivers met this over temperature, except for three instances

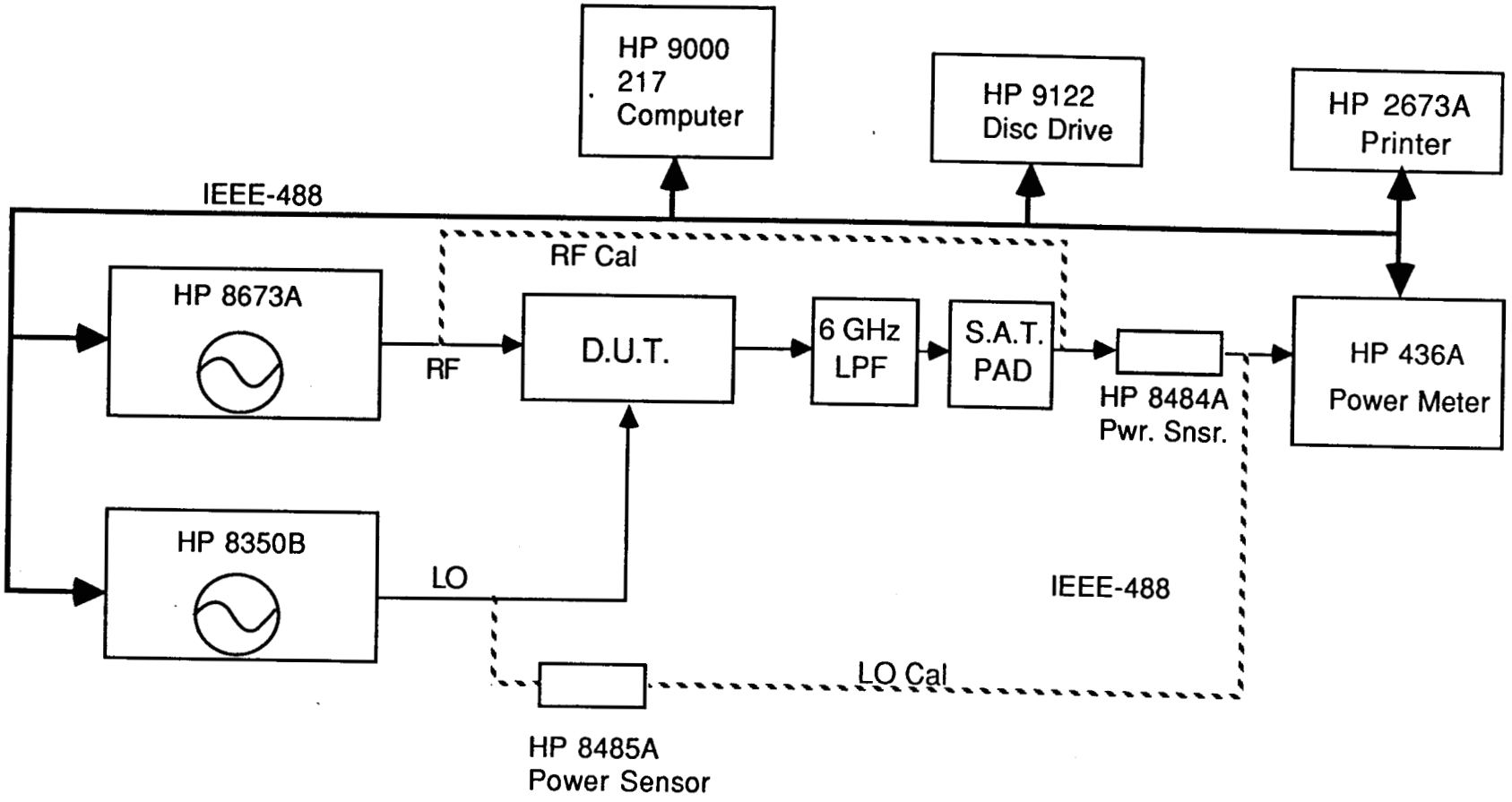

Figure 2.5-3 RF/IF Gain Test Setup

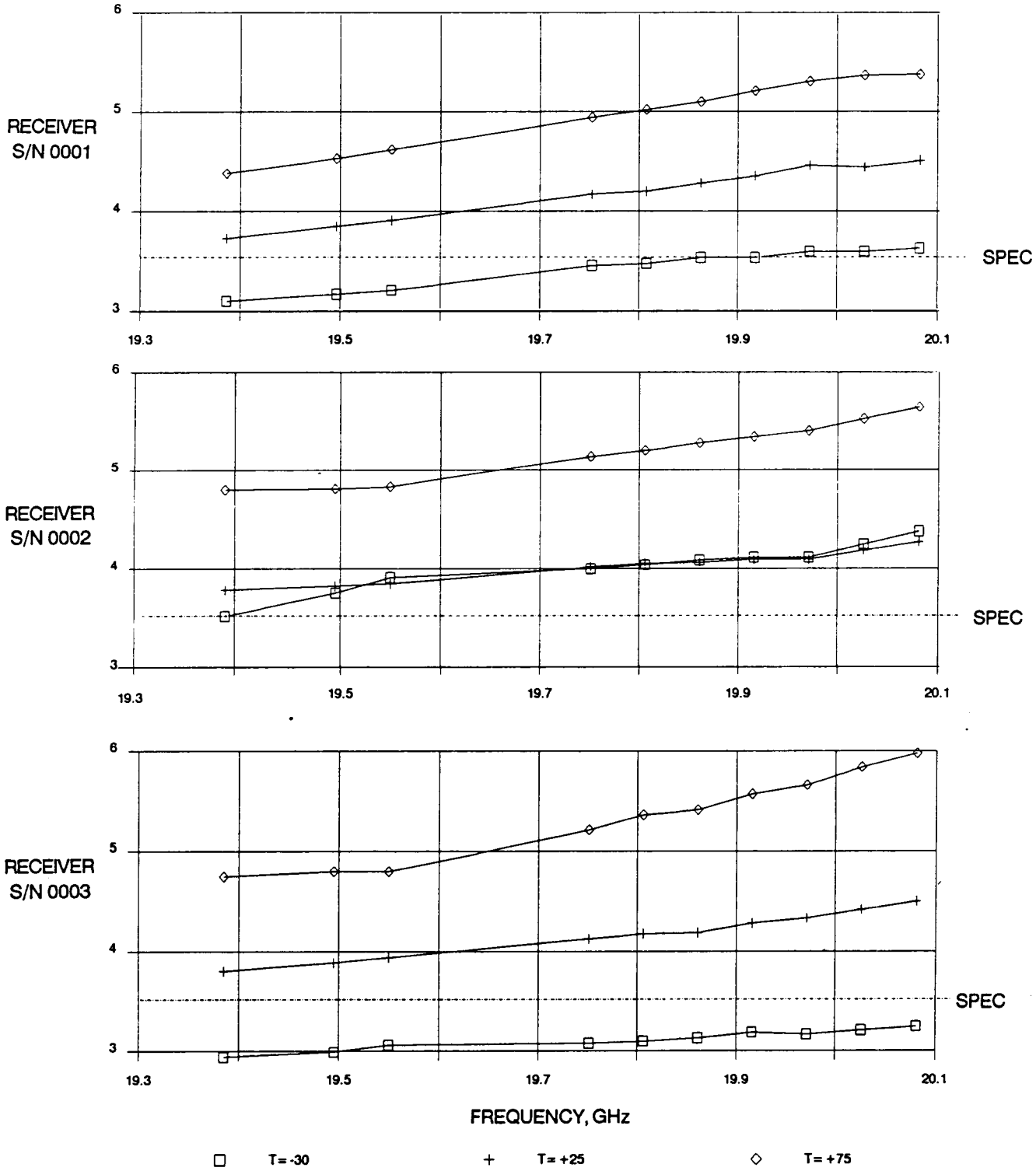

FIGURE 2.6-1 20 GHz RECEIVER NOISE FIGURE (dB) OVER TEMPERATURE (PAGE 1 OF 2)

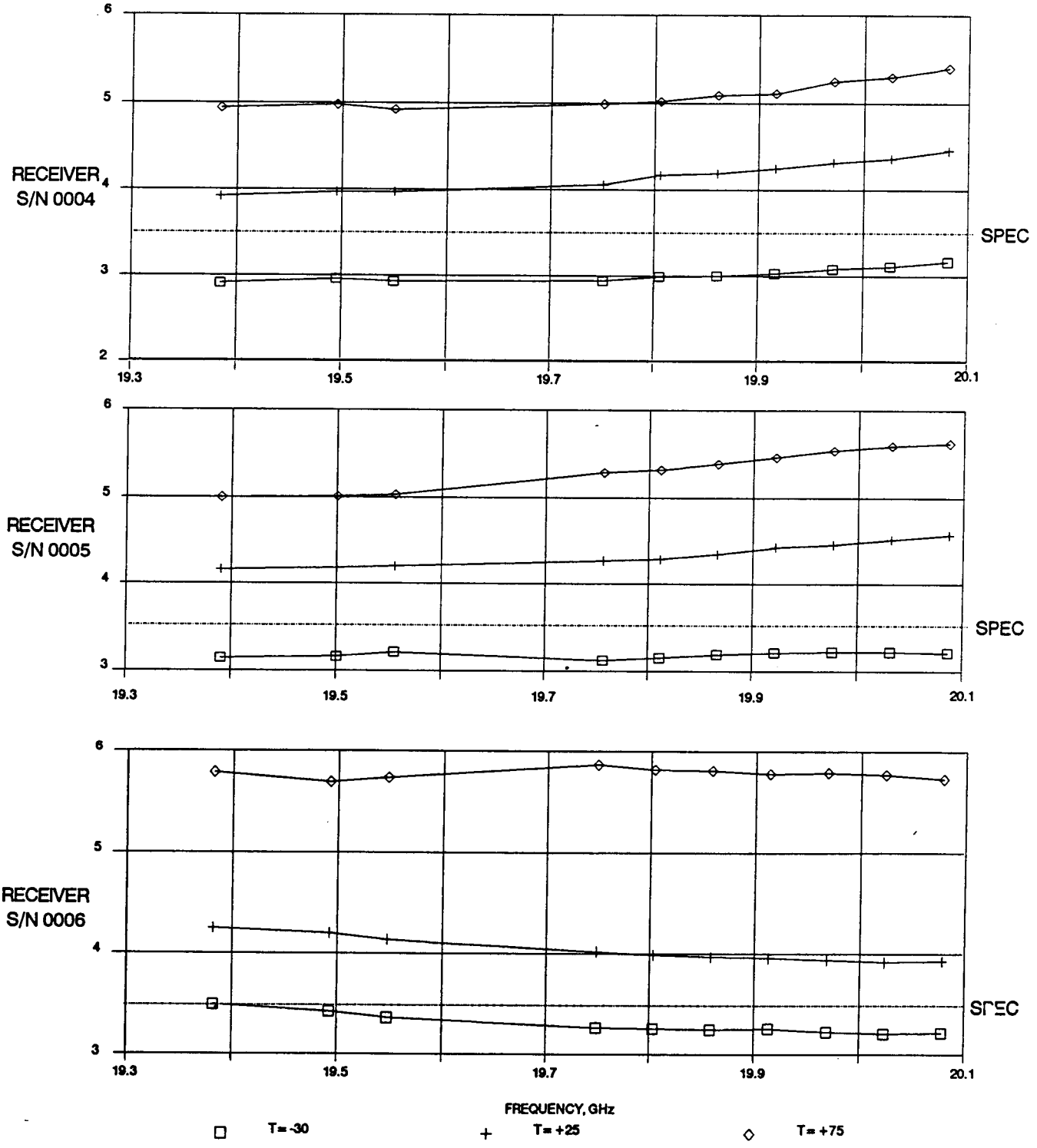

FIGURE 2.6-1 20 GHz RECEIVER NOISE FIGURE (dB) OVER TEMPERATURE (PAGE 2 OF 2)

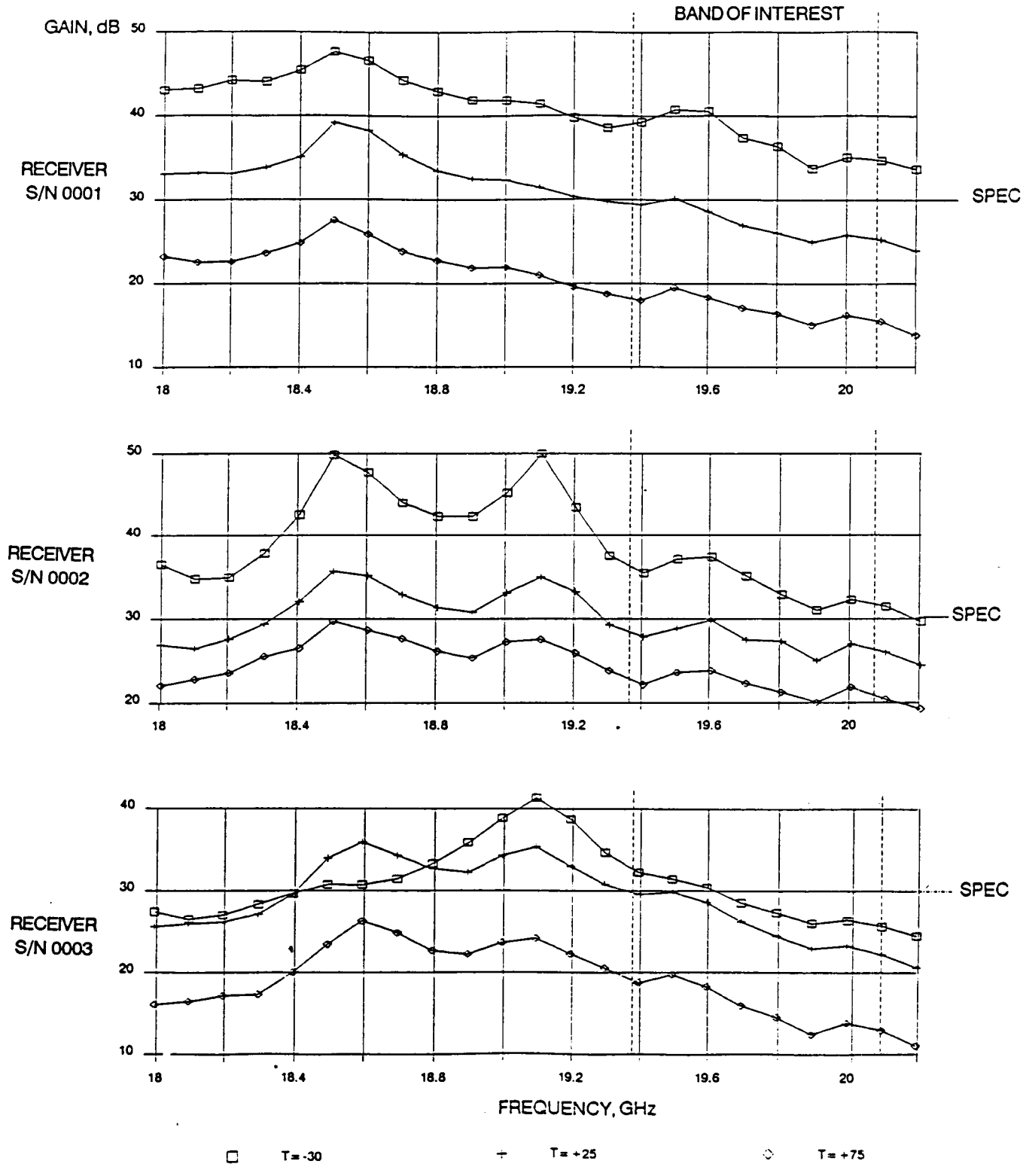

FIGURE 2.6-2 20 GHz RECEIVER GAIN (dB) OVER TEMPERATURE (PAGE 1 OF 2)

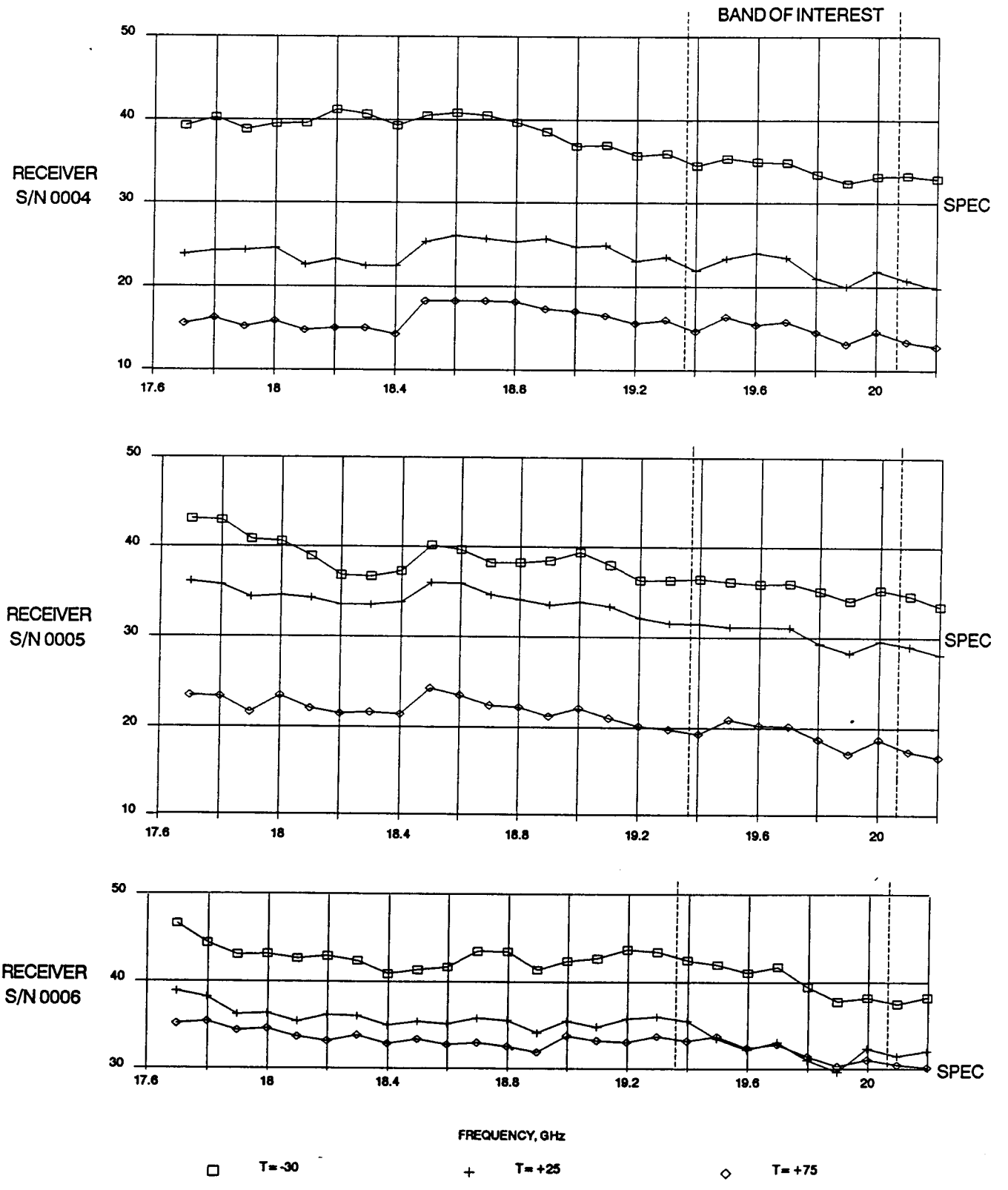

FIGURE 2.6-2 20 GHz RECEIVER GAIN (dB) OVER TEMPERATURE (PAGE 2 OF 2)

at cold temperature, where the minimum point was -33.03 dBm. These variances occurred at the receiver gain peaks and were limited to one of the five frequency points measured per receiver. Gain compression was tested at 20 GHz at ambient, and all receivers were compliant.

Input and output VSWRs were good. The input circulator insured that VSWR was under the 1.7:1 specification. The output VSWR specification was 1.5:1 and four of the receivers were compliant. The worst case VSWR was 1.66:1.

The maximum measured peak-to-peak group delay was 2.61 ns, compared to a 5 ns specification. This wide margin was due to the fact that the IF filter, which would have been the limiting factor for bandwidth, was deleted.

Image rejection was excellent. In fact, no images were detected in any of the receivers. This is due to the performance of the bandpass filter and the image frequency being below the WR-42 waveguide cutoff frequency of 14.05 GHz.

The spurious response specification was -45 dBc, and all of the tested spurs were compliant except the 2 X -2 and -2 X 2 spurs, which were as high as -31.3 dBc. A primary cause for this is the high local oscillator power required to drive the mixer (+20 dBm).

ANALYSIS OF MEASURED DATA

The performance of one of the receivers (S/N 0002) was analyzed using the data for the various components from Task V (POC Fabrication) at room temperature at 20 GHz and performing a cascaded analysis using a LOTUS spreadsheet to simulate receiver performance. The model has a reasonable correlation with the measured performance of the receiver. Some of the values used were estimates that were confirmed by the model. These components are: input W/G transition, RF attenuator, and DC block. The RF filter data was taken from the breadboard task, and the IFA data from the Harris internal IR&D project.

There was an unexpected problem with the noise sources used in the noise figure measurements of the first three receivers and their components. A noise source is imprinted with an Excess Noise Ratio (ENR) corresponding to sample frequencies in the band. It is generally assumed that interpolation can be used for frequencies between those specified. Any error in the imprinted ENR causes an identical error in the measured noise figure. During the breadboard and receiver fabrication phases of the contract, a waveguide noise source from MSC was used. A new HP 346C noise source was received at the end of Task V, after the receivers had been assembled. This new source yielded higher measurements than those obtained with the MSC device. At the Task V review, both results were presented, with more confidence in the HP results accurate because of the newness of the source and

its calibration. Subsequently, another HP 346C source was obtained, and the measurement results were found to agree with the first HP 346C, with a maximum deviation of .05 dB, well within the published accuracy of +/- 0.2 dB.

Unfortunately, since the receivers were already assembled, they would have had to have been disassembled to measure the components for noise figure with the new source. Therefore, the model of the performance was done using the data measured with the MSC noise source. Since it is assumed that the measurement errors are absolute, the MSC measured data was used in the model. Despite the lack of accuracy in some of the data used in the analysis model, major factors in determining the receiver performance are shown.

In Table 2.6-1, results are shown for measurements with both sources and the analysis model for room temperature at 20 GHz. The gain data was taken by the noise figure meter, but the gain that was reported earlier was taken by the automated gain setup.

	GAIN	NOISE FIGURE
HP MEASURED	27.84	4.2
MSC MEASURED	26.26	3.5
MODEL SIMULATION	25.8	3.5

TABLE 2.6-1 ROOM TEMPERATURE COMPARISON

Table 2.6-2 displays the difference in gain and noise figure over temperature as measured, and as predicted by the analysis model. Receiver S/N 002 had one unusual phenomenon- the noise figure did not decrease at reduced temperature. This may be attributed to a change in HEMT noise parameters, S-parameters, or mechanical changes in the aluminum housing. The noise figure did decrease in the other two receivers, and the lower temperature delta from receiver S/N 001 is presented. As the noise figure changes were slightly more than predicted, it appears that the temperature coefficient used for HEMTs was slightly low.

	GAIN	NOISE FIGURE
POC MEASURED -30°C	+6.04	-1.2
MODEL SIMULATION -30°C	+4.4	-1.0
POC MEASURED +75°C	-4.98	+1.3
MODEL SIMULATION +75°C	-5.0	+0.9

TABLE 2.6-2 GAIN AND NOISE FIGURE VARIATIONS OVER TEMPERATURE

Table 2-6.3 shows the analysis model at room temperature, and shows the sensitivity of the components' performance on the receiver performance noise figure and intercept point. The model shows the input waveguide to microstrip connection to have 0.7 dB of loss, which directly affects the noise figure. This loss should be 0.2 to 0.3 dB. This transition was not tested or optimized, so this would be a good future development activity.

A reduction of LNA noise figure in the first or second stages would of course be beneficial. The sensitivity analysis shows that the third and fourth LNA stages can have I_{DS} optimized for gain instead of noise figure for best results. Experience with aligning the receivers confirms this. A future design might optimize the third and fourth stage input matching for gain. In the current design, the LNA stages are identical, individually fabricated and tested, and are selected so that the best noise figures are in the first stages.

The effects of changes on the front end of the receiver are not surprising. One would expect the changes in LNA gain and noise figure to affect overall receiver performance. What is more interesting is the effects of the output stages of the receiver. In the cascaded analysis, the IFA contribution raises the system noise figure by 0.3 dB. One would not expect this, as the front end would normally overwhelm this contribution. The combination of low LNA gain and a mixer with high insertion loss leaves only 13.8 dB gain in front of the IFA, which has a 6.0 dB noise figure. The sensitivity analysis shows that the IFA noise figure raises the overall receiver noise figure .08 dB/dB. Thus more gain is desirable before the IFA. The sensitivity analysis shows that lowering the mixer conversion loss would similarly lower the noise figure on a .08 dB/dB basis (assuming the mixer noise figure also is reduced). This is significant because of the high MMIC mixer conversion loss (16 dB), and the commercial availability of better mixers (conversion loss of 8 dB). Also,

NASA 20 GHz RECEIVER SENSITIVITY ANALYSIS

P IN = -60.0 dBm

#	ELEMENT	GAIN (dB)	NF (dB)	IPO (dBm)	GCAS (dB)	NFCAS (dB)	IPICAS (dBm)	POUT (dBm)
1	ISOLATOR	-0.2	0.2	100.0	-0.2	0.2	100.2	-60.2
2	W/G TRANS.	-0.7	0.7	100.0	-0.9	0.9	97.5	-60.9
3	LNA 1	6.5	1.7	15.0	5.6	2.6	9.4	-54.4
4	LNA 2	6.4	1.9	15.0	12.0	3.0	2.1	-48.0
5	LNA 3	6.3	1.8	15.0	18.3	3.1	-4.4	-41.7
6	LNA 4	5.9	1.9	15.0	24.2	3.1	-10.4	-35.8
7	RFA	8.0	7.1	23.0	32.2	3.1	-12.9	-27.8
8	RF FILTER	-2.0	2.0	100.0	30.2	3.1	-12.9	-29.8
9	RF ATTEN	-0.2	0.2	100.0	30.0	3.1	-12.9	-30.0
10	MIXER/HYBRID	-16.0	16.0	8.5	14.0	3.2	-13.6	-46.0
11	DC BLOCK	-0.2	0.2	100.0	13.8	3.2	-13.6	-46.2
12	IFA	12.0	6.0	23.0	25.8	3.5	-14.0	-34.2

SENSITIVITIES

CASCADED EQUIVALENTS

GAIN eq = 25.8 dB
NF eq = 3.45 dB
IP IN eq =-13.95 dBm

		*** S L O P E S (dB/dB) ****			
#	ELEMENT	NFeq/ Gi	NFeq/ NFi	IPeq/ Gi	IPeq/ IPi
1	ISOLATOR	-0.53	0.47	-1.00	0.00
2	W/G TRANS.	-0.44	0.56	-1.00	0.00
3	LNA 1	-0.17	0.83	-1.00	0.00
4	LNA 2	-0.10	0.19	-1.00	0.02
5	LNA 3	-0.09	0.04	-0.98	0.09
6	LNA 4	-0.08	0.01	-0.89	0.33
7	RFA	-0.07	0.01	-0.55	0.33
8	RF FILTER	-0.07	0.00	-0.22	0.00
9	RF ATTEN	-0.07	0.00	-0.22	0.00
10	MIXER/HYBRI	-0.06	0.02	-0.22	0.14
11	DC BLOCK	-0.06	0.02	-0.08	0.00
12	IFA	0.00	0.08	-0.08	0.08

TABLE 2.6-3

recent work has produced MMIC mixers with performance superior to the MIC mixers. Because we bought the best HEMTs commercially available, it is doubtful that we could obtain another 8 dB of gain with an LNA redesign. The analysis also shows that the mixer loss contributes very little (0.1 dB) to the noise figure, but allows output stages to contribute to the overall noise figure. Therefore, an increase in LNA gain would be little more beneficial than reduced mixer conversion loss.

Temperature analysis was performed for both the receiver as built and with a mixer with a conversion loss of 8 dB. With the new mixer, the predicted noise figure improved by 0.4 dB at 25°C and 0.6 dB at 75°C. A greater change of the noise figure at 75°C was expected due to the lowered LNA gain at elevated temperatures, which makes the reduced mixer conversion loss more significant in overwhelming later stage contributions. The noise figure improvement was predicted to be 0.1 dB at -30°C.

The most significant deficiencies with receiver performance are, of course, the gain and noise figure. The LNA gain contributes to both of these parameters. Generally, the gain was about 2 dB low per LNA stage, which is 8 dB total per receiver. The analysis shows that this raises the noise figure at ambient temperatures by at least 0.3 dB, and at high temperature by 0.5 dB.

When this analysis was done at the end of the first build lot, it was difficult to determine absolutely if the LNA noise figure was higher than originally projected, because it was measured using an inaccurate noise source. The measured noise figure was close to what was expected when measured with the bad MSC diode source, and since the new HP source generally gave higher numbers, one would assume the LNA noise figure is higher than expected. Manufacturing tests during the second build confirmed this.

The effects of the input transition on gain and noise figure are obvious. The insertion loss adds directly to the noise figure. The effects of the mixer conversion loss on noise figure were detailed above.

Another shortcoming in the receiver performance is the high variation of gain over temperature. Design analysis predicted a variation of 10 dB over the specified temperature range. The measured data shows a typical variation of 20 dB, however. It is generally accepted that amplifier gain changes by -0.01 dB per degree centigrade per stage of amplification. This assumption was also applied to the mixer. It is known from the spurious response tests that the mixers do not function well at high temperature, and may be the cause of some of the additional loss. No temperature measurements have been made on the individual components fabricated during Task V.

A provision for gain compensation was put in the receiver in the place of the DC block component. Since voltage controlled variable attenuators suitable for insertion in the receiver have

an insertion loss of 2.5 dB minimum, it was decided not to include them to avoid further degradation of the low receiver gain. As the sensitivity analysis shows, this loss would increase the noise figure approximately 0.2 dB.

RECOMMENDATIONS

Recommendations for product development will focus on two primary concepts: improvement of the current design, and taking advantage of advancing technology. No matter which of the two focuses are chosen, it is recommended that systems applications allow some margin for receiver performance, as opposed to depending on the state of the art for noise figure. This will allow lower production costs.

The development of C band TVRO terminals is a good analogy. In the 1970's, a low noise amplifier cost thousands of dollars for 120°K noise temperature (1.5 dB noise figure). As the GaAs FET technology matured, prices began to drop, but the amplifiers remained fairly costly due to their labor intensity. It was found that the same design yielded LNAs with noise temperatures from 70°K to 140°K, due to the variations in the FET noise performance. The lower temperature components obviously commanded a higher price, as they were used in high quality video terminals, while the high temperature LNAs were used where an exceptionally high signal to noise ratio was not needed (e.g. data transmission). A single design allowed a manufacturing atmosphere to develop which drove the prices down further. As assembly costs dropped, device performance continued to rise, while device cost declined. The low cost allowed the consumer to enter the market, and 120°K LNAs now cost under $100.00 when produced in significantly large quantities.

A wider performance margin can allow the use of cheaper and more workable components such as packaged HEMTs and soft substrates. Harris is currently conducting an IR&D program to investigate the feasibility of a soft substrate and packaged HEMTs in a 20 GHz amplifier, with a goal of developing a receiver with a 6 dB noise figure over a narrower band. This approach can also allow the integration of components such as the stages of the LNA and bandpass filter on one substrate. On this program, LNA stages were produced on separate carriers so that we could better characterize their performance, and put the best ones in the first stages. If the LNA, RFA, and bandpass filter were on one carrier, the number of substrates needed for those components would be reduced from thirteen to five. With the soft substrate approach, only one substrate would be required. This reduction would significantly reduce overall costs with no substantial compromise in performance.

A performance margin will allow a quarter micron MMIC front end to used in the receiver. The device technology has improved significantly since the initial design phase of this contract, and quarter micron foundry service is now available.

As the analysis section of this report shows, any future product development should include improvement of the waveguide transition. The new transition should have a fixed short to improve mechanical stability. The transition should of course have lower insertion loss.

The mixer should also be improved. The MMIC Image Reject Mixer has 16 dB of loss, while many mixers are now commercially available with 8 dB of loss. The MMIC mixer requires a +20 dBm LO drive, while the commercially available mixers require only +10 dBm. The only advantage of the current mixer is the image rejection capability, which is not needed due to the filtering already built into the receiver.

A smaller local oscillator should be developed. In the current receiver, the local oscillator is much larger than the receiver module, due to the two ovenized crystal reference sources. Reducing the local oscillator size would have a direct effect on receiver size and weight.

Casting the main portion of the receiver housing would facilitate production. A cast housing would be significantly less expensive than a machined housing. Using more integrated carriers would reduce the cost further. The use of a totally aluminum housing, without subcarriers, is discouraged because the high thermal coefficient of aluminum will cause the brittle GaAs devices to fracture. Invar carriers are used in the receiver to avoid failures caused by thermal expansion.

In the area of follow-on technology development, HEMT MMIC is a promising emerging technology. Single stage low noise amplifiers have been fabricated, and development work is being funded by DOD agencies such as RADC.

Future modifications in device periphery are also promising. Mitsubishi has developed a "mushroom" gate periphery that has demonstrated a 1.0 dB noise figure at 18 GHz. Future commercial release of devices with smaller gate widths will also allow lower noise figures.

CONCLUSION

The development of the 20 GHz Receiver has demonstrated that MMIC technology can significantly reduce the size, weight, and production cost of ground terminal receiver components. With further product design engineering, this technology is well suited for application in the 20 GHz frequency band, and normal production techniques will produce satisfactory yield to enable the production of low-cost, high performance 20 GHz receivers.

NASA-LEWIS

20 GHZ LOW NOISE RECEIVER

DESIGN REPORT

CONTRACT # NAS3-24244

16 JULY 1985

HARRIS

HARRIS CORPORATION GOVERNMENT COMMUNICATION SYSTEMS DIVISION
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1.Ø INTRODUCTION

This contract (#NAS3-24244) is for the development of a low noise, low cost 2Ø GHz ground terminal receiver. Three proof of concept (POC) receivers will be delivered which will be utilized in the POC demonstration of the Advanced Communications Technology Satellite (ACTS). The period of this study is 26 months starting 13 March, 1985.

The receiver (shown in Figure 1) translates and amplifies, with minimum noise contribution, the input signal within the frequency band of 17.7 to 2Ø.2 GHz to an intermediate frequency (IF) of 3.37 GHz. It is comprised of two subassemblies. The first subassembly contains all signal amplification, conversion, and filtering circuits along with their respective DC regulator and control circuits. The second subassembly contains a local oscillator and its DC regulator circuitry. The receiver is capable of manually selecting one of two different input frequencies without replacing the local oscillator subassembly. The receiver is designed for antenna mounting.

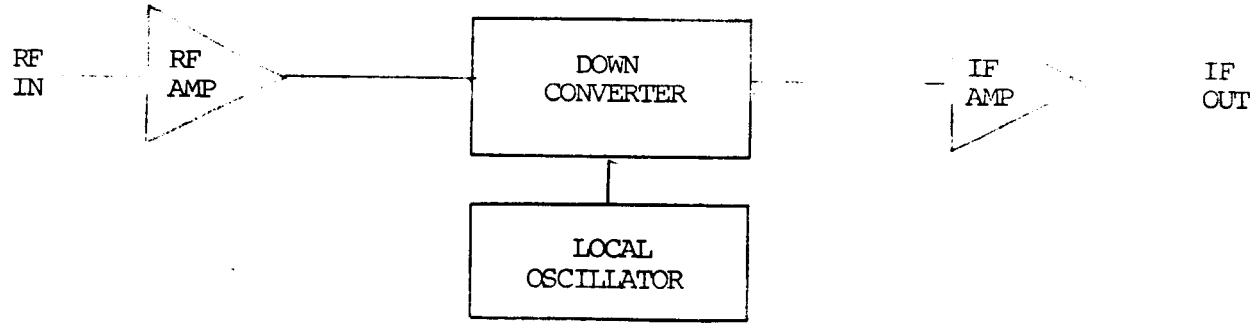


Figure 1. Receiver Functional Block Diagram

The objective of this contract is to develop the 2Ø GHz receiver described above which: a) provides the performance required for high burst rate TDMA

digital satellite communications systems of the 1990's, b) utilizes designs and implementation techniques which result in significantly reduced costs for such receivers such as making maximum use of Monolithic Microwave Integrated Circuits (MMIC), and (c) provides an advanced data base for development of products to be utilized in specific systems.

Harris Government Satellite Communication Division (GSCD) is providing the necessary personnel, facilities, equipment, services, and material to analyze, design, fabricate, and test three proof-of-concept 20 GHz receivers.

This design report is divided into three sections; Introduction (1.0), Receiver Design Overview (2.0), and Receiver Design and Analysis (3.0). The material contained herein follows the same general flow as that presented at the Preliminary Design Review and Breadboard Development Design Review. Section 2.0, Receiver Design Overview, details the partitioning and major design tradeoffs of the receiver. It concludes with a specification compliance matrix which cross-references each specification to its applicable portion of section 3.0. This final section, Receiver Design and Analysis, presents the baseline design with the necessary equations and rationale for performing the analysis of the cascaded receiver components.

2.0 RECEIVER DESIGN OVERVIEW

The 20 GHz Receiver design is summarized in the following paragraphs. Paragraph 2.1 discusses the receiver partitioning between MMIC and MIC. Paragraph 2.2 presents noise figure tradeoffs, and 2.3 contains the specification compliance matrix cross-referenced to section 3.0.

2.1 Partitioning

The design architecture selected for the 20 GHz Receiver is shown in the block diagram in Figure 2.1-1. The design uses a Low Noise Amplifier (LNA) that incorporates a waveguide to microstrip transition preceding two 1/3 micron discrete FET amplifier stages which are followed by a 2 chip MMIC RF amplifier. This front end configuration is driven by the noise figure limitations of present and near term MMIC amplifier developments.

The location of the receiver RF preselector is a compromise between minimizing input losses (preceding the LNA) for noise figure considerations, eliminating out-of-band input signals that can cause receiver intermodulation products or gain saturation and rejecting image band noise generated by the wideband LNA modules.

In the selected design a microstrip preselector filter precedes the receiver downconverter mixer and is tasked with rejecting out-of-band signals, image frequency inputs and image band noise generated by the broadband low noise amplifier stages. Locating the preselector at the input to the mixer instead of at the receiver input reduces the filter loss impact upon noise figure and allows a low cost microstrip implementation instead of a waveguide design. The filter which is a distributed, coupled line design cannot be implemented in MMIC form due to its large size. Alternate designs that use MMIC lumped elements are not practical due to the Low Q's (high filter insertion loss) that can be realized with MMIC elements. Therefore the selected approach is a distributed MIC filter giving the best performance and lowest cost.

20 GHz RECEIVER BLOCK DIAGRAM

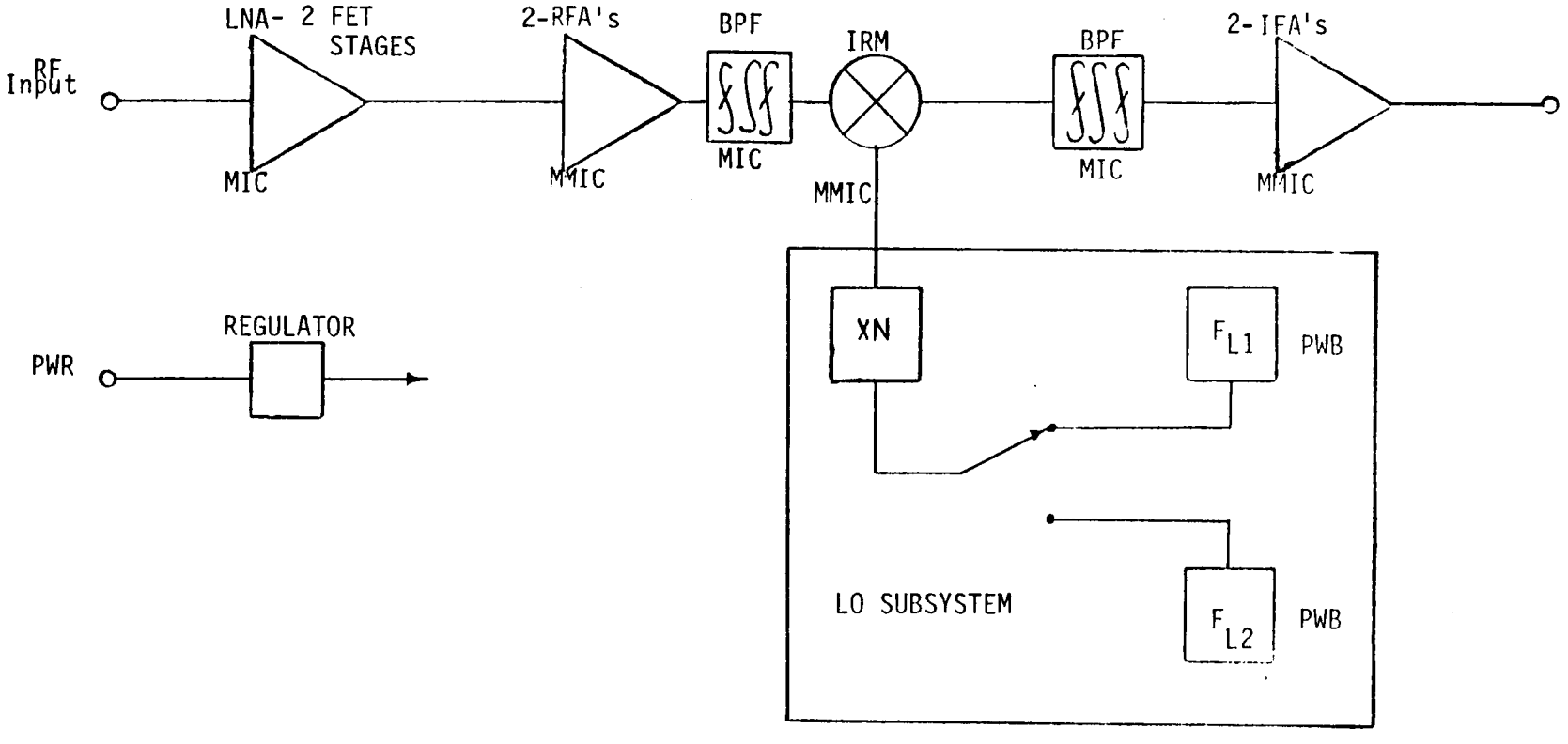


FIGURE 2.1-1

An MMIC Image Reject Mixer (IRM) is used to provide the frequency translation to the fixed IF of 3.373 GHz. An IRM is used because of its ease of design and fabrication and low cost in MMIC form. Its image rejection properties are not actually required as the input preselect filter attenuates these frequencies to below the specified level by itself.

The two local oscillator frequencies required to downconvert the RF input bands are generated by multiplication of low noise crystal sources. The desired output LO carrier frequency is manually selected by switching between two crystal reference oscillators. The local oscillator subsystem is a standard off-the-shelf design and will be housed in a separate module mounted next to the LNA/downconverter portion of the receiver.

The downconverted IF signal is selected by a multi-pole microstrip bandpass filter similar to the RF preselector and amplified to the required level by two MMIC IF amplifiers. The IF filter provides rejection to the alternate data channel signal and other undesired outputs that result from other signals which are inband to the receiver preselect filter.

2.1.1 Alternate Configuration

The IF filter is not strictly required by the receiver as long as one exists in the overall system. Most likely a more stringent IF filter with a narrower bandwidth will be contained in the modem to maximize its received signal to noise ratio prior to detection. If this is the case, a production cost savings would result by deleting the receivers IF bandpass filter and replacing it with a low pass design that rejects the sum signal and local oscillator.

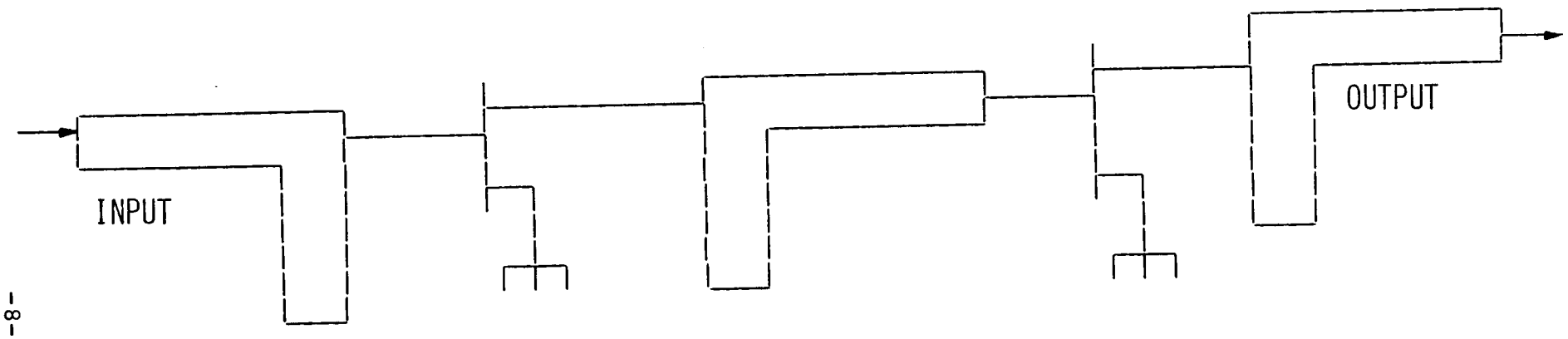
2.2 Design Driver Trades

The key design driver in the 20 GHz receiver is of course the noise figure requirement. Close behind this is the available gain from the FETs when tuned for minimum noise figure. The FET's maximum gain, which is desired to reduce the following stages noise contribution, does not occur when it is tuned for minimum noise figure. The difference between the maximum available gain and the gain available from the FET when it is tuned for minimum noise figure is accounted for in the VSWR loss of the input matching network cascaded with the FET. The relationship between noise figure and gain is shown in figure 2.2-1 for a single ended LNA approach using the device parameters from an NE 673 FET at 18 GHz. A noise matched first stage noise figure of 2.5 dB is obtained but at the expense of gain (resulting in a 5:1 VSWR). Similarly, a good VSWR match can be made (high gain) but at the expense of noise figure. The noise figure and gain matches of FETs tend to move together at higher frequencies, and as the FET gate lengths become smaller this match approaches the system impedance of 50 ohms. For the devices available on the market today, matching will not permit both minimum noise figure and input VSWR specifications to be achieved simultaneously. A different circuit topology than that shown in Figure 2.2-1 must be used.

2.2.1 Single-Ended LNA With Input Isolator

Two basic LNA approaches are being considered for the NASA-Lewis 20 GHz Receiver. The first is a single-ended approached with an input waveguide isolator. This design provides an input match while allowing the LNA input

SINGLE ENDED LNA
(WITHOUT ISOLATOR)



INPUT MATCH
(GAIN, NOISE)

INTERSTAGE MATCH

OUTPUT MATCH
(VSWR)

- INPUT MATCHING MUST BE FOR NOISE FIGURE OR VSWR - CAN NOT ACCOMODATE BOTH
- EXAMPLE: NE673 @ 18 GHz

NOISE MATCH	VSWR MATCH
NF = 2.5 dB	NF = 5.38 dB
VSWR = 5 : 1	VSWR = 1.7 : 1

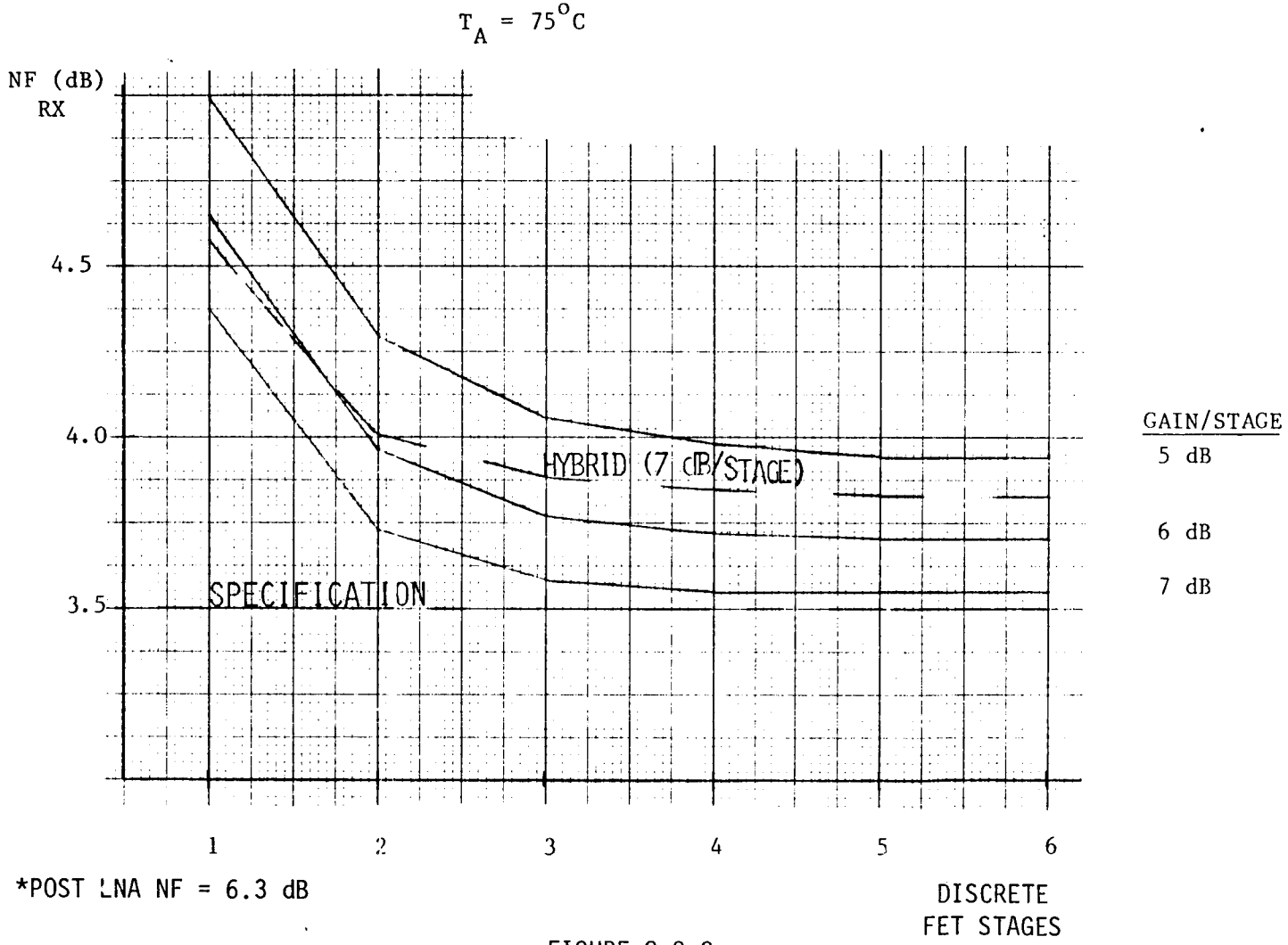
FIGURE 2.2-1

to be designed for minimum noise figure. This provides a maximum of design flexibility but degrades the input noise figure by the insertion loss of the isolator. This approach has the potential for being the lowest noise design pending S-parameter and noise match characterization of the selected FET. The disadvantage of the single ended design is that it does not permit optimum interstage matching to occur. Either a conjugately matched output that maximizes the preceding stage gain or an optimum noise match can be provided for the succeeding stage-but not both simultaneously. An accurate prediction of the overall receiver noise figure cannot be made for this approach until the devices that will be used have been fully characterized. Figure 2.2-2 shows the expected, overall receiver noise figure at the elevated ambient temperature of 75°C as a function of the resulting gain per stage when each stage is tuned for minimum noise figure versus the number of discrete FET stages used in the LNA. The device used in the generation of this graph is an NEC NE04500G which is discussed in paragraph 3.1. Figure 2.2-3 shows the post LNA noise figure presented to the LNA as a function of the number of RFAs used. Using more than two RFAs has a negligible affect on the overall receiver noise figure.

2.2.2. Hybrid Coupled (Balanced) LNA

A second method that can be used to simultaneously meet the conditions of input match and optimum noise match is a hybrid coupled LNA input. A quadrature coupler (Lange coupler) is used to split the input into in-phase and quadrature channels which are amplified and recombined by a second

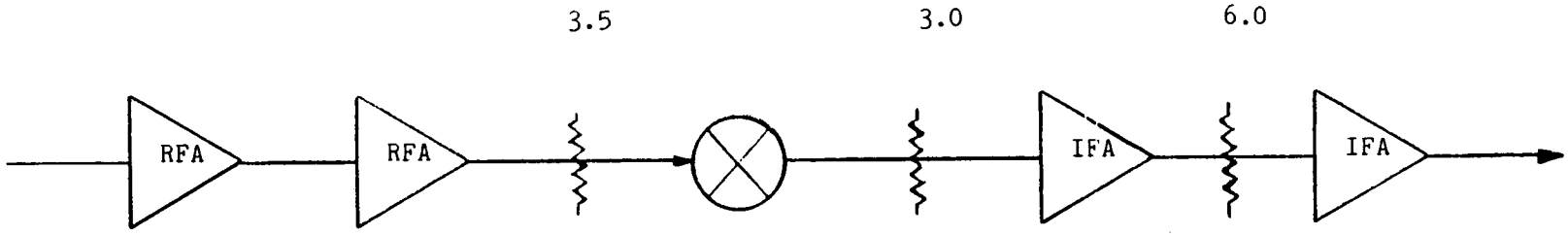
HYBRID VERSUS SINGLE ENDED LNA
NOISE FIGURE PERFORMANCE*



*POST LNA NF = 6.3 dB

FIGURE 2.2-2

POST LNA RECEIVER NOISE



G	9.5	9.5	-7.8	10.25	10.25	dB
NF	4.8	4.8	8.5	4.4	4.4	dB

NF_{EQ} = 10.7 dB (1 - RFA)

= 6.3 dB (2 - RFAs)

= 5.3 dB (3 - RFAs)

= 5.15 dB ($\geq$5 - RFAs)

FIGURE 2.2-3

quadrature hybrid. This approach is shown in figure 2.2-4. Any reflection resulting from the difference between optimum noise match and a matched (conjugate) load is absorbed by the isolated port of the hybrid. This applies to the LNA input as well as between stages effectively isolating each stage. The resistive losses of the hybrid coupled amplifier are approximately the same as for the isolator input design, impacting the input noise figure by the same amount. The hybrid coupled input LNA has one additional superior performance characteristic. The input intercept point and 1 dB gain compression level are each increased by approximately 3 dB. For the 20 GHz Receiver these parameters are not first order design drivers therefore noise figure considerations still dominate.

The disadvantages of the hybrid LNA approach are increased interstage losses and double the number of FETs and tuning adjustments required. This architecture can be used to accurately predicted the receiver noise figure in the absence of FET noise and S parameters as long as the minimum noise figure and the associated gain are provided by the FET manufacture. Figure 2.2-2 shows the predicted receiver performance using a hybrid LNA. It is clear that the lowest noise design cannot be chosen until the device characterization is completed during the breadboard phase.

Paragraph 3.1 presents a detailed noise figure, gain and input intercept point analysis for the overall receiver using both LNA configurations. The receiver analyzed throughout section 3.0 contains two discrete FETs followed by two RFAs and other circuits as shown in Figure 2.1-1.

HYBRID LNA

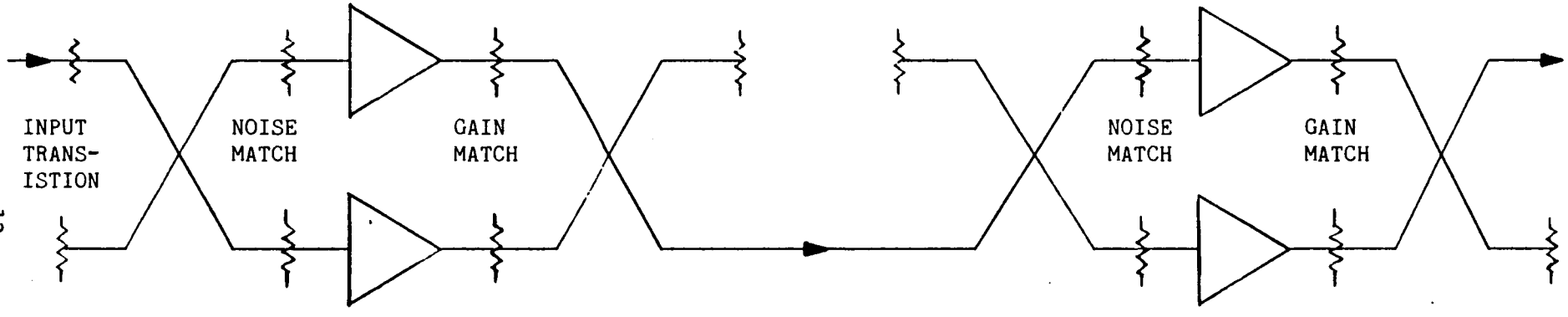


FIGURE 2.2-4

2.2.3 Future Trends

Two new transistor types are currently being developed in research labs that have demonstrated a significant improvement in minimum noise figure, associated gain and input matching. These are the High Electron Mobility Transistor (HEMT) and the Heterojunction Bipolar Transistor (HBT). The former is similar to a MESFET structure shown in Figure 2.2-5 with carrier flow in an undoped, high (enhanced) mobility, channel allowing extremely high frequency and low noise operation. The latter has a vertical structure shown in figure 2.2-6 which is similar to a bipolar junction transistor with very then (0.05 to 0.1 um), controlled layers formed by epitaxial growth.

These transistors are mentioned here to show the potential improvement to be gained in the near future. Several articles have been published recently demonstrating the HEMT's performance improvement. These transistors exhibit approximately a 0.3 dB improvement in device noise figure and a 1 dB gain increase at 20 GHz as compared to MESFETs. In addition its input impedance's real part is approximately 20 ohms as compared to 6 ohms for the MESFET permiting much easier front end and interstage matching. All this means that the 20 GHz receiver, if implemented with HEMT technology in the LNA, could have approximately 0.4 dB less noise figure, may not require an input circulator, and may be able to be implemented as a less complicated single-ended approach since the interstage matching problem is greatly reduced. It must be pointed out, however, that the present design does not use HEMT or HBT technology because of its present commercial unavailability. If in the future it becomes

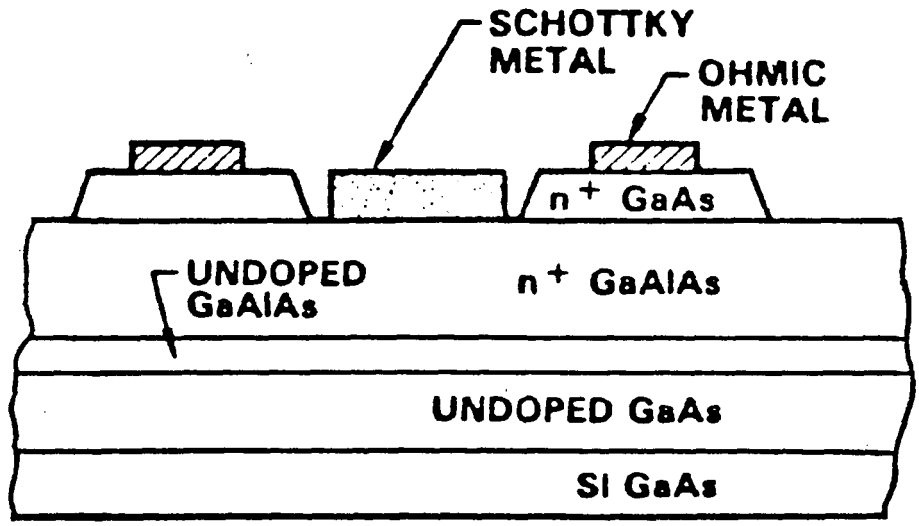


FIGURE 2.2-5 HEMT Structure

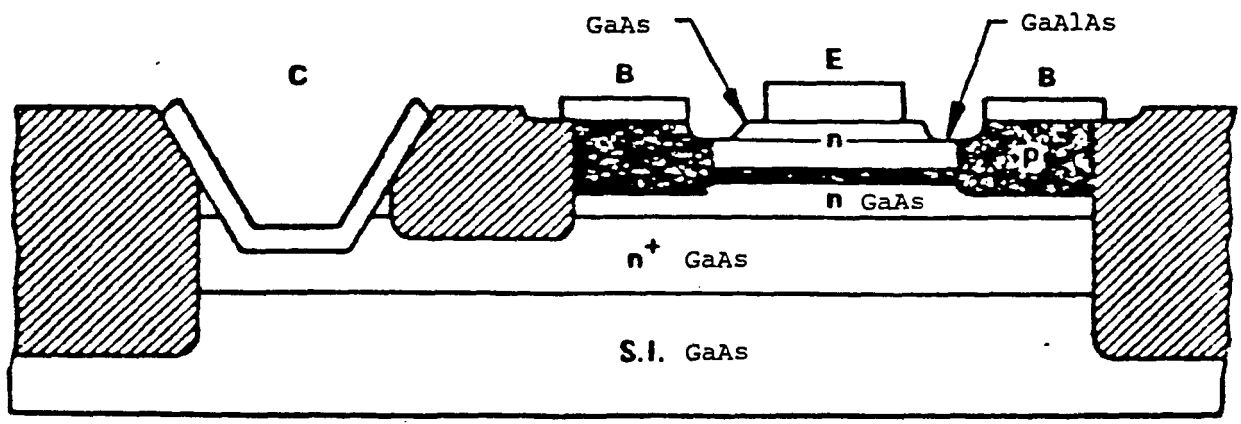


FIGURE 2.2-6 HBT Structure

possible to obtain these devices, Harris would welcome an add on to the present contract for a new LNA.

2.3 Specification Compliance

Figure 2.3-1 is a specification compliance matrix cross referencing NASA-Lewis' requirements, Harris' internal specifications, and the subparagraphs of this report which discuss the individual parameter predictions. One area is currently shown to be out of spec. This is the overall receiver noise figure at the 75°C elevated ambient temperature. The prediction is based on a two stage hybrid LNA design and can be improved by increasing the number of discrete LNA stages and by reducing the maximum ambient temperature. However, increasing LNA stages also increases tuning time, materials and cost in production. Also, as shown in Figure 2.2-2, the amount of improvement in overall receiver noise figure quickly diminishes after the second discrete FET is added. The 3.5 dB noise figure can be met at 44°C for a three stage hybrid LNA. If during the FET characterization in the Task II Breadboard Development Phase a single-ended LNA can be implemented, the maximum ambient temperature at which the receiver will meet a 3.5 dB noise figure would increase above 44°C.

3.0 RECEIVER DESIGN AND ANALYSIS

This section presents detailed analysis of the baseline design presented in section 2.0. Each of the following paragraphs discuss a portion of the design applicable to the individual specification called out

FIGURE 2.3-1

COMPLIANCE MATRIX

TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
INPUT RF BAND	3.2.2.1 (3.2.1)	17.7-20.2	17.7-20.2	-----	GHz	3.0
SUBBAND #1	3.2.2.1 (3.2.1)	19.4953±0.166	19.4953±0.166	-----	GHz	3.1/3.6
SUBBAND #2	3.2.2.1 (3.2.1)	19.9600±0.166	19.9600±0.166	-----	GHz	3.1/3.6
OUTPUT IF BAND	3.2.2.2 (3.2.2)	3373.056±0.166	3373.056±0.166	-----	MHz	3.0
LOCAL OSCILLATOR SETTABILITY	3.2.2.2 (3.2.2)	±20	±20	-----	KHz	3.5
LOCAL OSCILLATOR LONG TERM DRIFT	3.2.2.2 (3.2.2)	±1.2	±1.0	±0.2	PPM/YR	3.5
NOISE FIGURE	3.2.2.3 (3.2.3)	3.5	4.0	-0.5	dB	3.1
RF TO IF GAIN	3.2.2.4 (3.2.4)	30	31.8	1.8	dB	3.1
INBAND OVERDRIVE	3.2.2.5 (3.2.5)	0	>10	>10	dBm	3.1
GAIN RIPPLE	3.2.2.6 (3.2.6)	±0.75	±0.57	±0.18	dB/150 MHz	3.3
GAIN SLOPE	3.2.2.7 (3.2.7)	0.5	0.19	0.31	dB/10 MHz	3.3
INPUT VSWR	3.2.2.8 (3.2.8)	1.7:1	1.46:1	2.8 dB RL	-------	3.2
OUTPUT VSWR	3.2.2.9 (3.2.9)	1.5:1	1.44:1	0.9 dB RL	-------	3.2

FIGURE 2.3-1

COMPLIANCE MATRIX CONTINUED

TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
GROUP DELAY	3.2.2.10 (3.2.10)					3.3
0 PARABOLIC		±0.1	0.007	0.093	ns/MHz^2	
0 RIPPLE		5.0	1.01	3.99	ns(p-p)	
IMAGE REJECTION	3.2.2.11 (3.2.11)	40	>50	>10	dB	3.6
AM-PM CONVERSION	3.2.2.12 (3.2.12)	0.5	0.22	0.28	Deg/dB	3.4
INPUT 1 dB GAIN COMPRESSION	3.2.2.13 (2.2.13)	-40	-39.2	0.8	dBm	3.1
INPUT 3rd ORDER IP	3.2.2.14 (3.2.14)	-30	-29.2	0.8	dBm	3.1
OUT OF BAND REJECTION (<15.7 & >22.2 GHz)	3.2.2.15 (3.2.15)	45	>55	10	dB	3.6
SPURIOUS RESPONSE	3.2.2.16 (3.2.16)	-45	-45	0	dBc	3.6

FIGURE 2.3-1

COMPLIANCE MATRIX CONTINUED

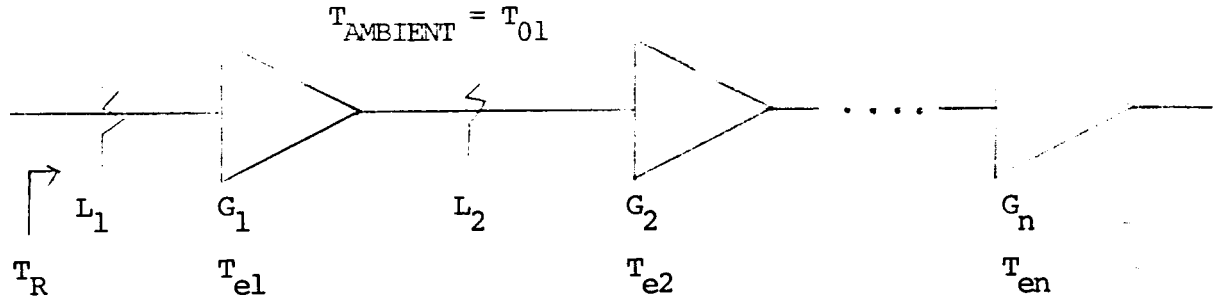
TITLE	PARAGRAPH NASA SOW (HARRIS SPEC)	SPEC	PREDICTION	MARGIN	UNITS	REPORT PARAGRAPH
PHASE NOISE (SSB >1K Hz)	3.2.2.17 (3.2.17)	-70	-78	8	dBc/Hz	3.5
DC POWER	3.2.2.18/22/23 (3.2.18/20/21)	TBD +10% SURGE <2X REVERSE POLARITY PROTECTION	+15 +10% SURGE <2X REVERSE POLARITY PROTECTION	----- -----	VOLTS AMPS	3.7
CONNECTORS	3.2.2.19 (3.3.3/4)					3.8
o RF INPUT		WR 42/COVER	WR 42/COVER	-----	-----	
o IF OUTPUT/ LO INPUT		SMA FEMALE	SMA FEMALE OR COMPATABLE	-----	-----	
o DC		COMMERCIALLY AVAILABLE	COMMERCIALLY AVAILABLE	-----	-----	
RECEIVED POWER	3.2.2.20 (3.2.19)	-80 TO -60	UP TO -56.4	-----	dBm	3.4/3.6
MECHANICAL CONFIGURATION	3.2.2.21 (3.3.1/2/5/7)	ANTENNA MOUNTABLE	ANTENNA MOUNTABLE	-----	-----	3.8
ENVIRONMENT	3.2.3 AND 3.3.2.2 (3.3.6)	$-30 \leq T_A \leq +75$	$-30 \leq T_A \leq +75$	-----	^{o}C	3.1

in the specification cross reference matrix of section 2.0. The following topics are analyzed in the paragraphs indicated:

- Ø Noise Figure/Gain/Intercept Point (3.1)
- Ø VSWR (3.2)
- Ø Gain Ripple/Group Delay (3.3)
- Ø AM-PM Conversion (3.4)
- Ø Phase Noise/LO Stability and Drift (3.5)
- Ø Spurious Response (3.6)
- Ø DC Power Distribution (3.7)
- Ø Packaging (3.8)

3.1 Cascaded Noise Figure, Gain, and Input Intercept Point

The overall receiver noise figure is most strongly dependent upon the input losses preceding the first active gain stage and secondly on the gain of that first stage as shown below



$$NF_{eq} \triangleq 10 \text{ Log } \left(\frac{T_R}{T_O} + 1\right)$$

$$T_R = (L_1 - 1)T_{01} + T_{e1}L_1 + \frac{(L_2 - 1)L_1T_{01}}{G_1}$$

$$+ \frac{T_{e2}L_1L_2}{G_1} + \ldots + \frac{T_{en}L_1L_2\cdots}{G_1G_2\cdots}$$

$$T_o = 290^oK$$

Since all the above variables are greater than unity, L_1 (input loss) and T_{e1} (effective noise temperature of the first stage) add directly to T_R and hence to the overall noise figure. G_1, however, reduces the noise effect of every following stage. This is why the selection and tuning of the first stages is so important.

Harris has examined the available FETs and chosen the NEC NE04500G as first choice and the Toshiba JS8830-AS as second. The Toshiba device is the only quarter micron FET currently available. Both Hughes and Avantek produce quarter micron devices, but they won't be available for approximately one year.

The features that lead to the selection of the NEC device are:

- Proven gate geometry (0.3 micron gate length)
- Shortened gate width (from 280 to 200 microns)
- Wrap around ground (sidewall metalization)
- Improved version of NE673 device offering 1.9 dB NF at 18 GHz
- Measured noise figure of 2.2 dB at 20 GHz

- Measured associated gain of 7.5 dB at 20 GHz

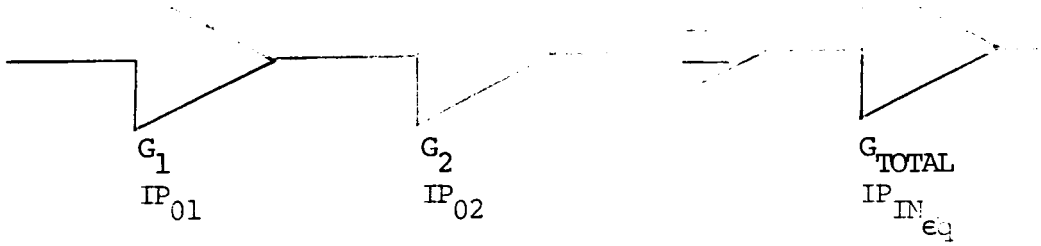
This device is shown in figure 3.1-1.

The Toshiba device selected as a backup has the following characteristics:

- 0.25 micron gate length
- Noise figure at 18 GHz = 2.0 dB
- Extrapolated 2.2 dB noise figure at 20 GHz
- Extrapolated 7.8 dB associated gain at 20 GHz
- No sidewall metalization
- 280 micron gate - width

The main reason this device was not the primary selection was that its noise figure and associated gain at 20 GHz were predicted by extrapolating 18 GHz data where the NEC device performance is supported by measured performance characteristics.

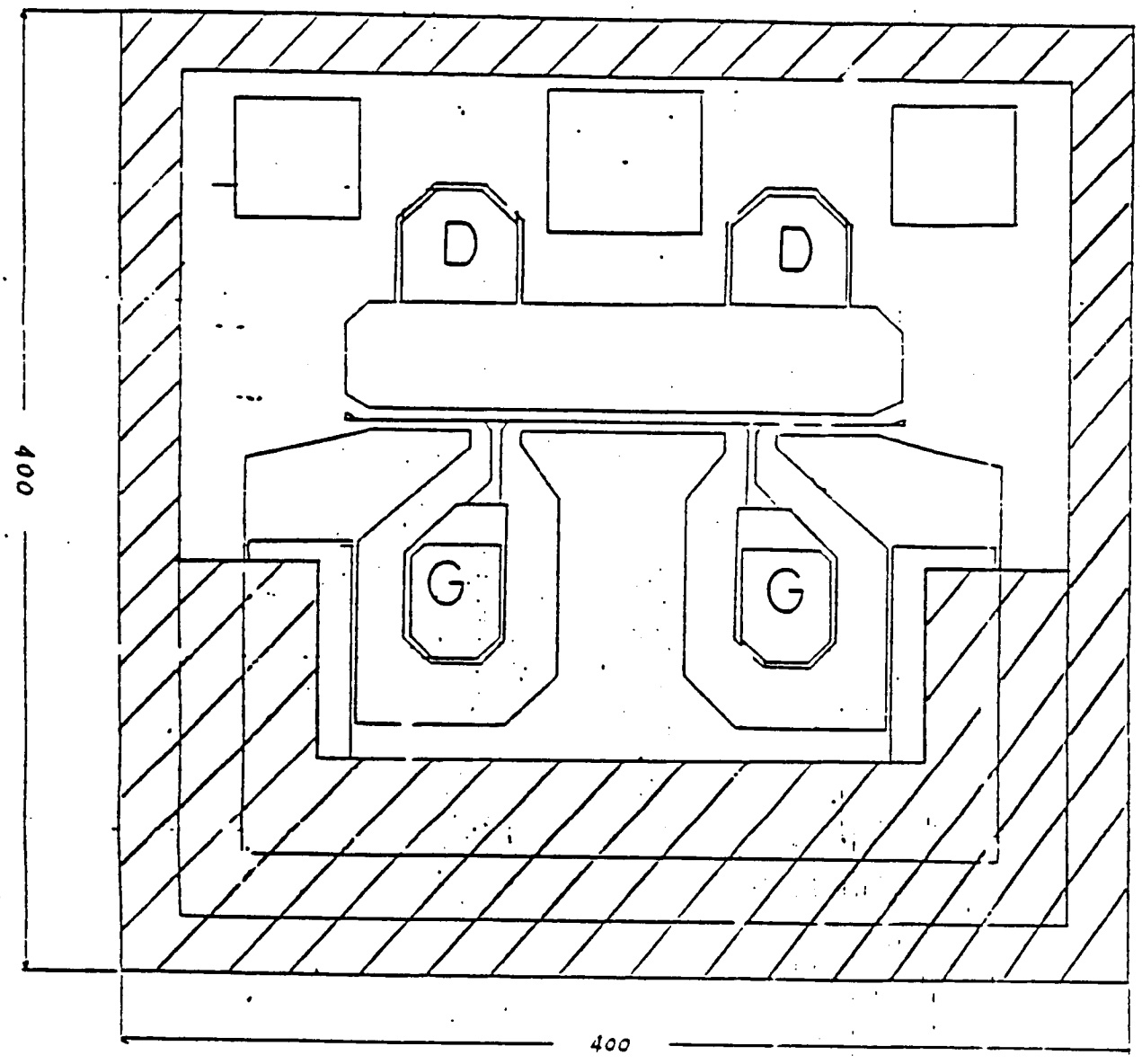
The following two paragraphs show the cascaded effects of both the hybrid and single-ended LNA receiver. The input intercept point is calculated as follows:



$$1P_{\emptyset_{eq}}(dBm) = IP_{\emptyset 2} - 10 \log \{1 + 10^{-(IP_{\emptyset 1} + G_2 - IP_{\emptyset 2})/10}\}$$

FIGURE 3.1-1

NE 04500G FET



- 0.3 MICRON GATE LENGTH
- 200 MICRON GATE WIDTH
- SIDEWALL METALIZATION ALLOWS WRAP AROUND GROUND
- MINIMUM NOISE FIGURE AT 20 GHz: 2.2 dB
- ASSOCIATED GAIN AT 20 GHz: 7.5 dB

$$IP_{in_{eq}} = IP_{o_{eq}} - G_1 - G_2$$

3.1.1 Hybrid (Balanced) LNA Configuration

Figures 3.1-2,-3 and -4, depict the hybrid LNA's performance over temperature, the overall receiver's performance over temperature and the receiver's nominal performance at room temperature, respectively. Both noise figure (temperature) and gain of an active device vary over temperature. The gain variation exhibited by the FETs is approximately -Ø.1 dB/1Ø°C, giving a 1 dB downward gain change from -3Ø°C to +75°C. Noise figure effects are somewhat more complicated as shown below:

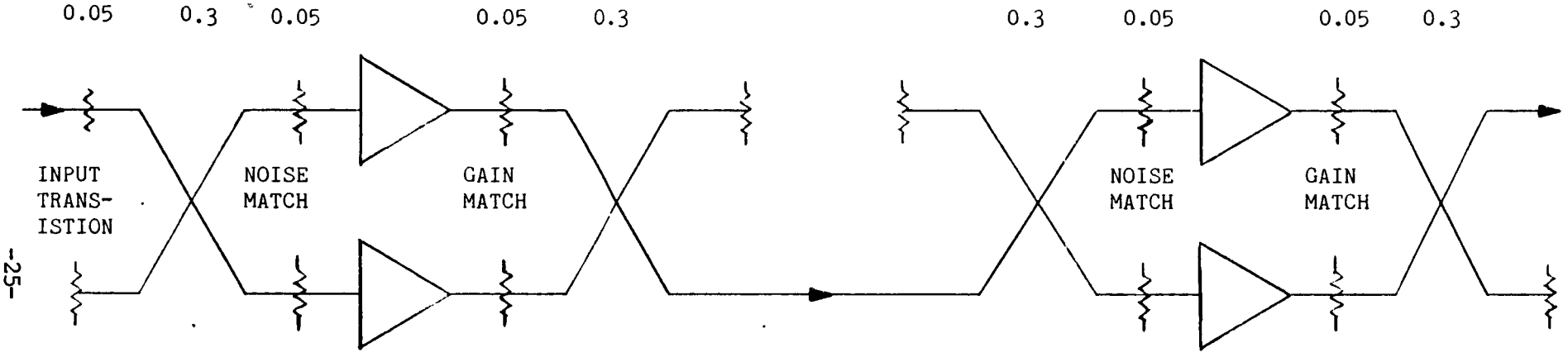
$$T_e(T_A) = T_{e2}\Big|_{T_{A2}} = T_{e1}\Big|_{T_{A1}} \left(\frac{T_{A2}}{T_{A1}}\right)^{1.5}$$

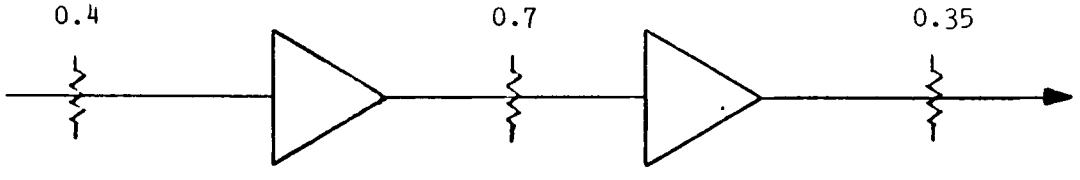
where T_{A1} and T_{A2} are the ambient temperature at which T_{e1} is measured and T_{e2} is calculated, respectively. The exponent is an experimentally determine parameter equal to 1.5 for the type of FETs used in the receiver. The total gain variation shown is for a receiver with no gain compensation. In the final design some form of gain compensation will be implemented, most likely in the bias supply as described in paragraph 3.7. This compensation will not only reduce the predicted maximum gain spread but will also improve the input intercept point.

FIGURE 3.1-2

HYBRID LNA

PERFORMANCE OVER TEMPERATURE



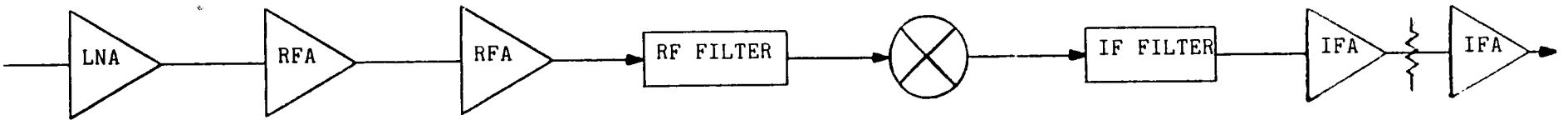


G_{MAX}	-0.4	8.0	-0.7	8.0	-0.35	dB
G_{MIN}	-0.4	7.0	-0.7	7.0	-0.35	dB
$1P_{O\ MIN}$	---	13.0	---	13.0	----	dBm
NF_{MAX}	---	2.71	---	2.71	----	dB

G_{MAX} = 14.55 dB
G_{MIN} = 12.55 dB
$1P_{O\ EQ}$ = 11.9 dBm MIN.
NF_{EQ} = 3.69 dB MAX.

FIGURE 3.1-3

RECEIVER PERFORMANCE OVER TEMPERATURE
(HYBRID LNA)



G_{MAX}	14.55	12.5	12.5	-1.6	-7.5	-1.4	12.75	-6	12.75 dB
G_{MIN}	12.55	9.5	9.5	-3.5	-7.8	-3.0	10.25	-6	10.25 dB
$1P_{O\ MIN}$	11.9	20.0	20.0	---	5.0	---	26.0	--	26.0 dBM
NF_{MAX}	3.69	4.8	4.8	---	8.5	---	4.4	--	4.4 dB

SPEC	

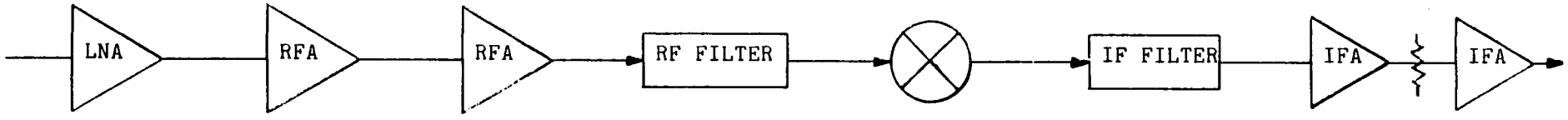
30	dB
-30	dBm
3.5	dB

PREDICTED PERFORMANCE

G_{MAX} = 48.6 dB
G_{MIN} = 31.8 dB
$1P_{IN\ EQ}$ = -28.2 dBm MIN
NF_{EQ} = 4.01 dB (440° K) MAX

FIGURE 3.1-4

NOMINAL RECEIVER PERFORMANCE AT ROOM TEMPERATURE
(HYBRID LNA)



G_{MAX}	13.55	11.0	11.0	-2.5	-7.8	-2.2	11.5	-6	11.5	dB
$1P_O$	11.9	20.0	20.0	---	5.0	---	26.0	--	26.0	dBm
NF	3.03	4.0	4.0	---	7.5	---	3.7	--	3.7	dB

G_{EQ} = 40.0 dB
$IP_{IN\ EQ}$ = -22.5 dBm
NF_{EQ} = 3.21 dB (318° K)

3.1.2 Single-Ended LNA Configuration

Figures 3.1-5, -6, and -7 depict the Single-Ended LNA's performance over temperature, the overall receiver's performance over temperature and the receiver's nominal performance at room temperature, respectively. The cascaded effects are calculated in the same manner as for the hybrid LNA. Similarly gain compensation will be added to this approach, again improving the input intercept point.

In the Single-Ended LNA analysis optimum interstage matching is assumed resulting in the best performance being obtained for comparision to the hybrid LNA. Since the S parameters of the devices have not yet been characterized, a lower limit cannot be assigned for this approach. However, once the individual devices are characterized and a realistic analysis performed, a decision will be made choosing the best LNA approach. Until that time, both LNA configurations are being carried as viable options.

3.1.3 Burnout

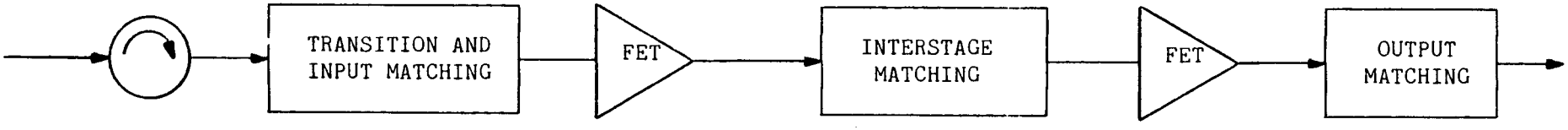
A first order approximation to the input power level at which the devices will be damaged is dependent upon their biasing voltages and the characteristic impedance of the transmission medium. To prevent burnout, V_{GS} must be held below 0V. For a 50 ohm system and -1V bias on the gate, the maximum input power without damage is:

$$P < V_p^2/2R = 1/100 = 0.01W$$

$$P < 10 \text{ dBm}$$

FIGURE 3.1-5

SINGLE ENDED LNA
PERFORMANCE OVER TEMPERATURE

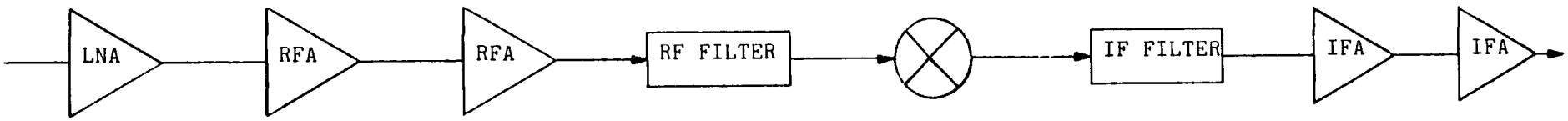


GAIN MAX	-0.2	-0.1	8.0	-0.1	8.0	-0.1	dB
GAIN MIN	-0.2	-0.1	7.0	-0.1	7.0	-0.1	dB
$1P_O$ MIN	---	---	13.0	---	13.0	---	dBm
NOISE FIGURE MAX	---	---	2.71	---	2.71	---	dB

GAIN MAX = 15.5 dB
GAIN MIN = 13.5 dB
$1P_{O\ EQ}$ = 12.2 dBm MIN.
NOISE FIGURE $_{EQ}$ = 3.45 dB (351° K) MAX

FIGURE 3.1-6

RECEIVER PERFORMANCE OVER TEMPERATURE
(SINGLE ENDED LNA)



G_{MAX}	15.5	12.5	12.5	-1.6	-7.5	-1.4	12.75	-6	12.75 dB
G_{MIN}	13.5	9.5	9.5	-3.5	-7.8	-3.0	10.25	-6	10.25 dB
$1P_{O\ MIN}$	12.2	20.0	20.0	---	5.0	---	26.0	--	26.0 dBm
NF_{MAX}	3.45	4.8	4.8	---	8.5	---	4.4	--	4.4 dB

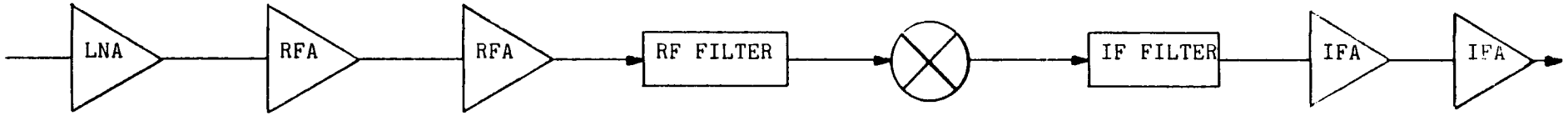
SPEC
-----
30 dB
-30 dBM
3.5 dB

PREDICTED PERFORMANCE

G_{MAX} = 49.5 dB
G_{MIN} = 32.7 dB
$1P_{IN\ EQ}$ = -29.2 dBm MIN
NF_{EQ} = 3.75 dB (398° K) MAX

FIGURE 3.1-7

NOMINAL RECEIVER PERFORMANCE AT ROOM TEMPERATURE
(SINGLE ENDED LNA)



G_{MAX}	14.5	11.0	11.0	-2.5	-7.8	-2.2	11.5	-6	11.5	dB
IP_O	12.2	20.0	20.0	---	5.0	---	26.0	--	26.0	dBm
NF	2.82	4.0	4.0	---	7.5	---	3.7	--	3.7	dB

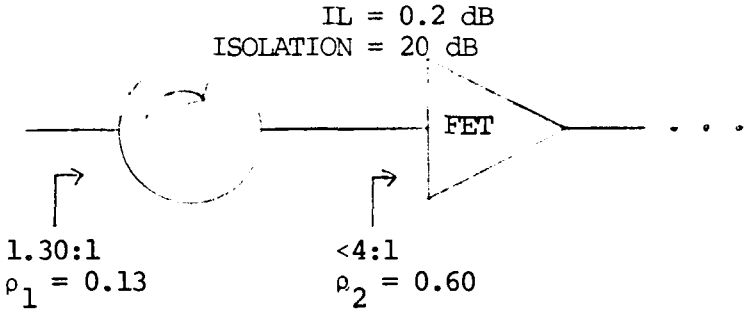
G_{EQ} = 41 dB
$IP_{IN\ EQ}$ = -23.5 dBm
NF_{EQ} = 2.97 dB (285° K)

This level provides 10 dB of margin over the specified 0 dBm burnout level for the single-ended LNA and 13 dB margin for the balanced LNA approach. Once the LNA FETs and their matching circuitry have been characterized and designed, a more accurate burnout level can be obtained. A 10 dB margin using the above approximation is adequate to insure compliance when taking the input matching circuit into account.

3.2 VSWR

3.2.1 Single-Ended LNA Input

For the Single-Ended LNA Receiver the input VSWR is calculated as follows:



$$\rho_{in}(max) = \rho_1 + \alpha\beta\rho_2 \frac{(1 - \rho_1^2)}{(1 + \alpha\beta\rho_1\rho_2)}$$

$\alpha = 10^{-L_F/20}$, L_F = Insertion loss of isolator

$\beta = 10^{-L_R/20}$, L_R = Isolation of isolator

$\rho_{in}(max) = 0.188$

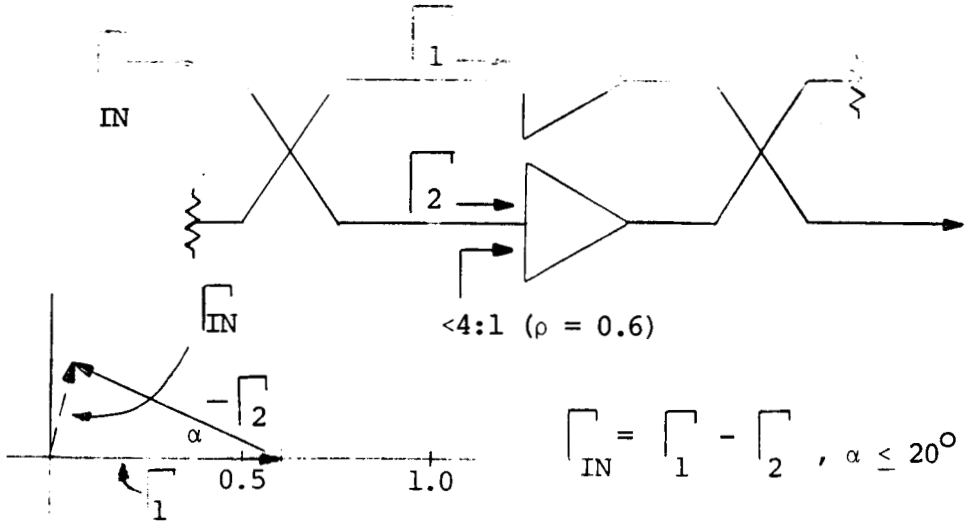
$VSWR_{in}$ = 1.46:1 maximum (14.5 dB Return Loss)

$VSWR_{spec}$ = 1.7:1 maximum (11.7 dB Return Loss)

These equations determine the worst case input VSWR based on multiple reflections adding in phase. This approach has a minimum return loss margin of 2.8 dB.

3.2.2 Hybrid (Balanced) LNA Input

The hybrid LNA receiver input VSWR is calculated as shown below with the use of a vector diagram.



For a maximum FET noise figure match of 4:1 VSWR and placing a limit of 20° maximum between matched FET input reflection coefficient angles, Γ_{IN} becomes:

$$|\Gamma_{IN}| = 0.208 \text{ or } VSWR_{IN} = 1.53:1$$

To find the maximum input VSWR for this approach, the difference in reflection coefficient magnitudes must also be taken into account. For a

VSWR range looking into the matched FETs of 3:1 to 4:1, the overall reflection at the receiver input becomes:

$$|\Gamma_{IN}| = |\Gamma_1| - |\Gamma_2| = 0.6 - 0.5 = 0.1, \alpha = 0^{\circ}$$

Γ_1: VSWR = 4:1; Γ_2: VSWR = 3:1

Taken both of these effects together the overall RSS'D input VSWR of the receiver becomes:

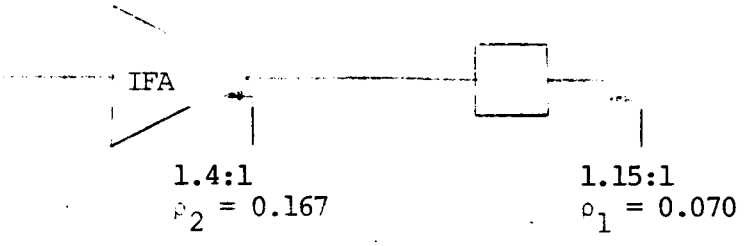
$$|\Gamma_{IN}|_{TOTAL} = |\Gamma_{IN}|^2_{\alpha} - |\Gamma_{IN}|^2_{AMPLITUDE} = 0.231$$

$$VSWR_{IN} = 1.60:1 \text{ MAXIMUM}$$

The use of statistically RSS'ing the individual components is justified for two reasons. First, it is unlikely that the reflections from both FETs will be of equal and opposite magnitude and phase from reference at the same frequency. Second, great care must be taken in tuning the first LNA stage to achieve the minimum noise figure. Once the noise performance is optimized, the matched FETs will track very closely in phase and amplitude. Even though each FET can vary $\pm 10^{\circ}$ from reference phase, as a tuned pair, they will track.

3.2.3 Receiver Output VSWR

The output VSWR of the receiver is determined primarily by the IFA's output and secondly by the IF output connector. Since the location of the IFA is not fixed with respect to the connector and the IF bandwidth is relatively small, the output VSWR can be tuned by IFA placement. This allows the output VSWR to be calculated by RSS'ing the IFA and connector's VSWR as shown below.



$$\rho_{out}^2(RSS) = \rho_1^2 + (\alpha\beta\rho_2)^2(1 - \rho_1^2)^2$$

$\alpha = \beta = 1$ = Loss Between Components

$\rho_{out} = 0.180$

$VSWR_{out} = 1.44:1$ (14.9 dB Return Loss)

$VSWR_{spec} = 1.5:1$ (14.0 dB Return Loss)

Margin = 0.9 dB Return Loss

3.3 GAIN RIPPLE AND GROUP DELAY

Figure 3.3-1 lists the gain ripple, gain slope, parabolic group delay and group delay ripple specifications as they have been partitioned among all the receiver elements. Partitioning of the gain ripple specifications was based on the percentage bandwidth that 150 MHz and 10 MHz were at each element. The LNA and RF filter were both allocated more due to noise matching at the LNA which is not as flat over frequency as gain matching and due to the tuning difficulties at 20 GHz for multiple pole filters. Both filters were allocated more gain slope to account for rolloff at the bandedges.

Gain variations in the receiver are minimized by computer aided design and optimization of receiver components. Variation of gain is the result of the summing of component gain variations and cascaded VSWR effects. All of the amplitude variations are small and uncorrelated and add in an RSS fashion. The MMIC circuits do not have sufficient Q to produce gain variation approaching the 1.5 dB maximum peak to peak variation over 150 MHz. The design of the MIC components also do not allow these variations due to the broadband design approach. Component VSWR's are also low enough not to affect a large increase in ripple. All components are designed to have a flat (zero dB) gain slope over the operating frequency band and therefore, will not approach the maximum slope of 0.5 dB per 10 MHz.

The receiver's group delay performance is well within the required limits because it does not contain the limiting IF bandpass filter of the system. The allocated entries made in the group delay columns are all much

FIGURE 3.3-1
RECEIVER GAIN RIPPLE AND GROUP DELAY

			GROUP DELAY (OVER ANY 100 MHz)	
	GAIN RIPPLE dB/150 MHz	GAIN SLOPE dB/10 MHz	PARABOLIC ns/MHz^2	RIPPLE ns PEAK-TO-PEAK
LNA	± 0.30	0.05	0.001	0.1
RFA 1	± 0.10	0.05	----	---
RFA 2	± 0.10	0.05	----	---
RF FILTER	± 0.20	0.1	0.001	0.1
IRM	± 0.20	0.05	----	---
IF FILTER	± 0.20	0.1	0.005	1.0
IFA 1	± 0.20	0.05	----	---
IFA 2	± 0.20	0.05	----	---
VSWR	± 0.13	0.05	----	0.2
PEAK	----	---	0.007	---
RSS	± 0.57	0.194	----	1.03
SPEC	± 0.75	0.5	0.1	5.0
MARGIN	± 0.18	0.306	0.093	3.97

greater than predicted based upon bandwidth. The lines which do not have entries are negligible and wouldn't be large enough to be measured.

The IF filter is the principal contributor to the receiver group delay distortion budget.

The group delay can be written as a series.

$$Tgd = A_{\emptyset} + A_1 f + A_2 f^2 + A_3 f^3 + \ldots + A_n f^n$$

The $A_{\emptyset}$ term represents the fixed center frequency delay of the filter and is usually of no concern. The remaining terms represent delay distortion (variation from constant delay). For most filter designs (minimum phase networks), the second order term (parabolic delay) gives a good fit to the delay envelope for offset frequencies up to approximately 80% of the 3 dB bandwidth. The coefficient of the parabolic delay term can be found by fitting a parabola to the normalized (W_c = 1 radian) low pass filter group delay distortion that is obtained from the pole locations of the selected transfer function:

$$Tgd = \frac{d\phi}{dw} = -\sum_{i=1}^{n} \frac{\sigma_i}{\sigma_i^2 + (w - \omega_1)^2}$$

Plots of several filter delay characteristics and the derivation of the parabolic delay coefficient are shown in Figure 3.3-2.

Parabolic Delay Coefficient

$$\Delta tgd = KF^2$$

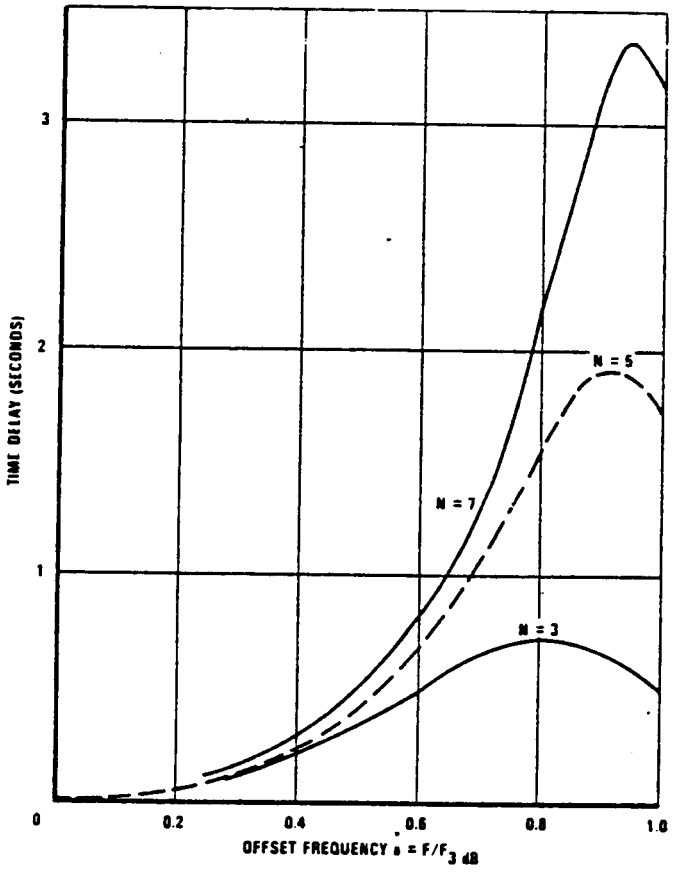
$$K = \frac{\Delta tgd}{F^2}$$

For a bandpass filter with bandwidth BW the delay is

$$\Delta tgd = \frac{\Delta tgd\ (lowpass)}{\pi BW}$$

at a frequency offset $a = \frac{BW}{BW_{3\ dB}}$

$$A_2 = K = \frac{\Delta^T \quad x\ 10^3}{\pi a^2\ (BW)^3} \quad \frac{ns}{(MHz)^2}$$



GROUP DELAY DISTORTION FOR BUTTERWORTH LOW PASS FILTER $W_{3\ dB} = 1$

13542-10

Figure 3.3-2 Group Delay Distortion

Note that the delay coefficient is inversely proportional to the cube of bandwidth. As an example, if the IF filter were selected to be a 5-pole Butterworth with a 3 dB bandwidth of 332 MHz, the coefficient of the parabolic delay would be:

$$A_2 = \frac{1.55257 \times 10^{3}}{\pi(0.8)^2(332)^3} = 2.1 \times 10^{-5} \frac{\text{ns}}{(\text{MHz})^2}$$

This is several orders of magnitude smaller than the receiver specification of Ø.1 ns per $(\text{MHz})^2$. The actual IF filter will be a 5-pole Chebyshev with a 3 dB bandwidth greater than 332 MHz.

Group delay ripple will not axceed approximately 1Ø% of the center frequency delay as a general rule of thumb.

$$T_{gd} @ f_c \approx \frac{1}{BW_{3dB}} = \frac{1}{332 \text{ MHz}} = 3.0 \text{ ns}$$

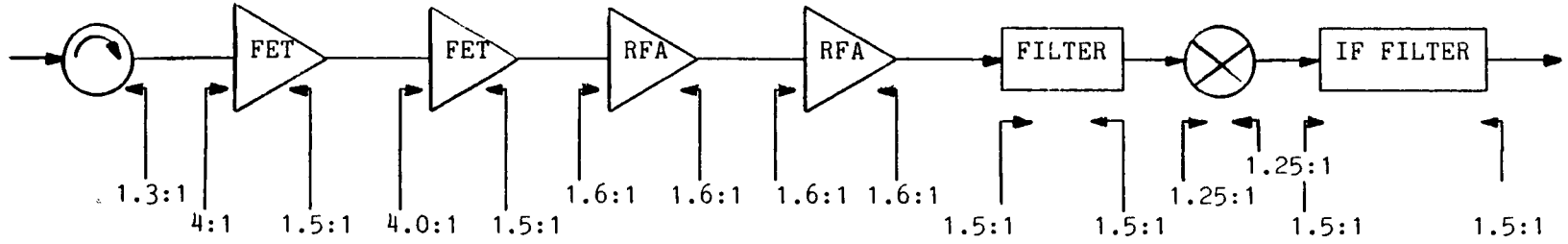
$$\text{G.D. Ripple} \approx \pm(T_{gd} @ f_c) \times 0.1 = \pm 0.3 \text{ ns}$$

VSWR makes a contribution to gain and phase (group delay) ripple also. Figure 3.3-3 shows the individual contributors throughout the receiver. The following equations were used to calculate these ripples.

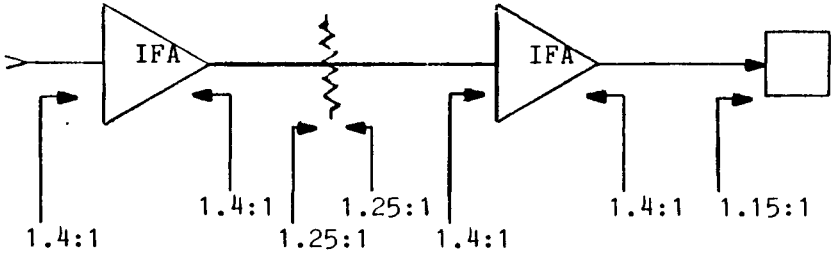
$$A_G = \pm 10 \text{ Log} \left\{ \frac{1 + \alpha\beta\rho_1\rho_2 \sin(\frac{2\pi L (BW)}{vc})}{1 - \alpha\beta\rho_1\rho_2 \sin(\frac{2\pi L (BW)}{vc})} \right\}, \text{ argument in radians}$$

FIGURE 3.3-3

RECEIVER GAIN AND PHASE RIPPLE DUE TO VSWR



ΔG	$\pm$0.077°	$\pm$0.061 dB	$\pm$0.070	$\pm$0.027	$\pm$0.023	$\pm$0.011	$\pm$0.011	dB
$\Delta \phi$	$\pm$0.510 dB	$\pm$0.401	$\pm$0.463	$\pm$0.178	$\pm$0.154	$\pm$0.074	$\pm$0.074	DEG.



$\pm$0.017 dB	$\pm$0.009	$\pm$0.009	$\pm$0.011	dB
$\pm$0.111°	$\pm$0.062	$\pm$0.062	$\pm$0.076	DEG.

$\Delta G = \pm 0.13$ dB/150 MHz

$\Delta \phi = \pm 0.85°$/150 MHz

$$\Delta G = \pm 10 \text{ Log } \left(\frac{1 + \alpha\beta\rho_1\rho_2}{1 - \alpha\beta\rho_1\rho_2}\right), \text{ dB}$$

$$\text{for } \frac{2\pi\ell\,(BW)}{\gamma c} \geq \pi/2$$

$$\Delta\phi = \pm\alpha\beta\rho_1\rho_2 \frac{180^\circ}{\pi}, \text{ degrees}$$

$$\text{for } \frac{4\pi\ell\,(BW)}{\gamma c} \geq \pi$$

where: γc is the velocity of propagation along the transmission line (m/s)

ℓ is the interstage separation (m)

BW is the bandwidth over which the ripple is calculated (HZ)

α and β are the forward and reverse path losses, respectively, between stages

ρ_1 and ρ_2 are the respective stage reflection coefficients

To find group delay ripple in time from phase ripple, the following equation is used:

$$\phi_{error} < \Delta f\ \Delta t\ 180^\circ$$

or

$$\Delta t > \frac{\phi_{error}}{\Delta f(180^\circ)}$$

C-2

where: ϕ_{error} is the deviation from linear phase over Δf given a Δt (differential group delay) measured over Δf.

Typically the value of ϕ_{error} predicted by the approximation given in the first equation is 60% larger than actual. This means that the Δt predicted needs to be increased by approximately 60% or

$$\Delta t \approx \pm \frac{1.6\phi_{err}}{\Delta f(180^{\circ})}$$

$$\phi_{err} = \frac{0.85^{\circ}}{75\ MHz} \times 50\ MHz = 0.567^{\circ}$$

$$\Delta t \approx \pm \frac{1.6(0.567^{\circ})}{50\ MHz(180^{\circ})} = \pm 0.1\ nsec \text{ over any 100 MHz bandwidth}$$

3.4 AM-PM CONVERSION

AM-PM conversion represents a cross modulation product that results in the change in output phase of each signal component of a multi-carrier signal as a function of the input amplitude envelope. For small signal conditions (back-off of 10 dB or more from saturation) the phase modulation induced by envelope fluctuations is proportional to input power.

$$\phi(A) \cong \frac{K}{2} A^2 t$$

Spilker[1] has shown that for small A the peak phase error can be expressed in degrees/dB of AM as:

$$K_p \cong 26.4\ KPs\ (^{\circ}/dB) \text{ where } Ps \triangleq \frac{A^2}{2}$$

Each active device must be measured to establish the value of K which will vary from unit to unit. To meet a requirement of 0.5 degrees/dB, the Receiver input level must be approximately 17 dB below the 1 dB gain compression level (assumes K=1). For the current design this represents an input power of -56.4 dBm. Since the maximum input level specified is -60 dBm, AM-PM conversion is not a first order design driver. Figure 3.4-1 derives the predicted AM-PM conversion level for the current design.

3.5 LOCAL OSCILLATOR

The 20 GHz Receiver requires two frequency stable, low noise local oscillator inputs to downconvert the two input digital data channels. The two LO frequencies are:

F_1 = 16.122244 GHz ± 20 KHz

F_2 = 16.586944 GHz ± 20 KHz

The POC requirement for an IF accuracy of ±20 KHz and a long term stability of $\pm 5.9 \times 10^{-6}$ forces the local oscillator frequency to be derived from a temperature stabilized crystal source. A frequency plan for generating the required output frequencies while meeting the requirement for low phase noise is shown in Figure 3.5-1. One of two crystal oscillators in the 100 MHz frequency range is multiplied to the 16 GHz frequency range via an L-band phase locked source and a x16 diode multiplier. In this circuit

[1]J.J. Spilker, Digital Communications by Satellite; pp. 254-264, Prentice Hall Information Theory Series.

AM-PM CONVERSION

$K_P \cong 26.4\ KP_S\ (^O/dB)$

(WHERE P_S IS THE INPUT POWER RELATIVE TO THE 1 dB GAIN COMPRESSION POINT EXPRESSED IN NUMERIC FORM.)

P_{IN} (1 dB GAIN COMP.)	-39.2 dBm
P_{IN} (MAX)	-60.0 dBm
P_S	-20.8 dB (0.0083)
K_P (K=1, WORST CASE)	0.22 ^{O}/dB
SPECIFICATION	0.5 ^{O}/dB
MARGIN	0.28 ^{O}/dB

FIGURE 3.4-1

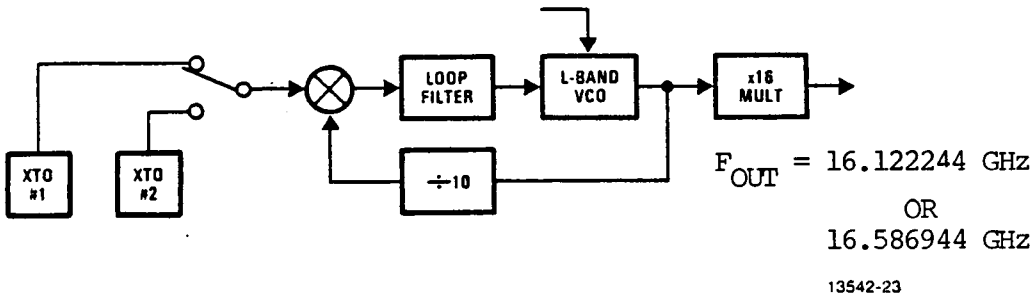


Figure 3.5-1. Local Oscillator Frequency Plan

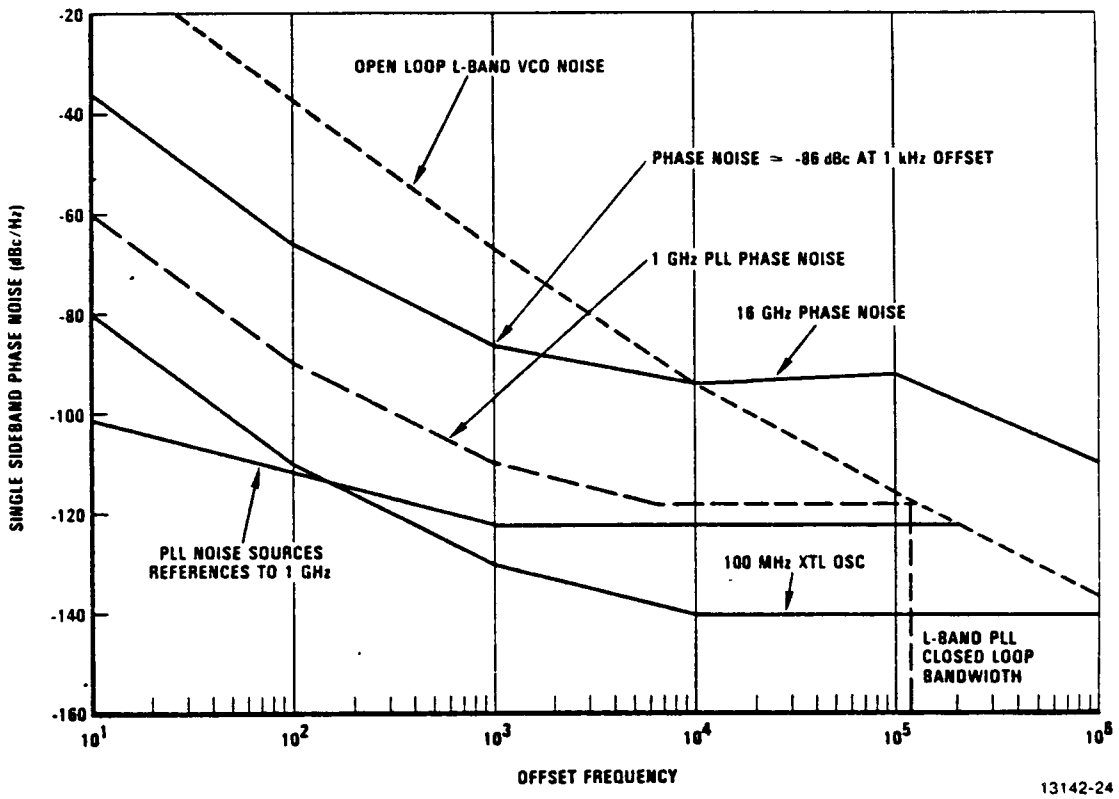


Figure 3.5-2. LO Phase Noise Estimate
(Lower Bound)

configuration, the L-band phase locked source acts as a "clean-up" loop (tracking filter) that reduces the phase noise of the output for frequency offsets greater than approximately 100 KHz.

A lower bound on the local oscillator phase noise can be estimated as shown in Figure 3.5-2. The high Q reference crystal oscillator establishes the output phase noise for low offset frequencies. Additive noise sources in the phase detector, divider and multiplier increase the noise floor for frequencies above about 10 KHz. The closed loop bandwidth of the L-band "clean-up" loop is selected to be approximately one hundred kilohertz for minimum integrated noise. The final x16 multiplier increases the output phase noise at 16 GHz by 24 dB. The estimated optimum performance of the LO source is -86 dBc/Hz single sideband phase noise at offsets greater than 1 KHz. This performance is 16 dB better than required by the receiver specification. To keep the overall receiver cost low, the purchased LO will be specified to have the predicted performance shown in Figure 3.5-3.

3.6 SPURIOUS RESPONSE

3.6.1 Full Inband Spurious Response

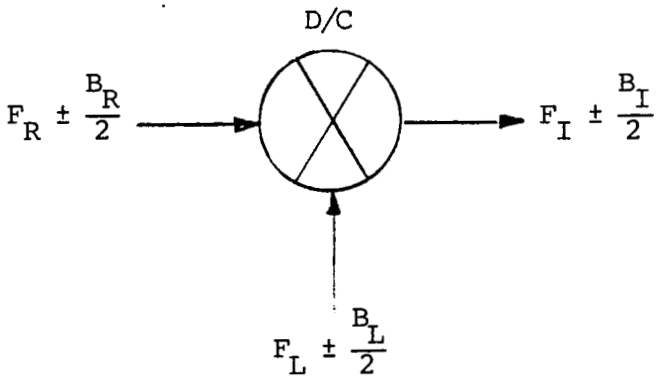
Once frequencies are selected for a given frequency conversion it is a simple matter to perform a spur analysis which will show whether or not the resulting spurs are within acceptable limits. For some frequency plans many combinations of frequencies may be tried until acceptable spur levels are obtained. However, what is needed is a method by which the optimum frequency plan can be derived.

FIGURE 3.5-3
LOCAL OSCILLATOR SSB PHASE NOISE

OFFSET	SPEC	PREDICTION	MARGIN	UNITS
100 Hz	---	-56	---	dBc/Hz
1 KHz	-70	-78	8	dBc/Hz
10 KHz	-70	-80	10	dBc/Hz
100 KHz	-70	-90	20	dBc/Hz
1 MHz	-70	-100	30	dBc/Hz

NON-INVERTING DOWNCONVERSION (SELECTED APPROACH)

Consider the following general downconversion stage,



where B_R is the total RF bandwidth, B_L is the total bandwidth over which the LO is hopped or tuned ($B_L = \emptyset$ for fixed frequency conversion), and B_I is the total IF bandwidth within which spurs are to be minimized. For the non-inverting case,

$$F_I = F_R - F_L \qquad (1)$$

and undesired outputs occur when

$$M(F_R \pm \frac{B_R}{2}) + N(F_L \pm \frac{B_L}{2}) = F_I \pm \frac{B_I}{2} \qquad (2)$$

where M and N are the spur product orders for other than M = 1 and N = -1, the desired IF output.

If Equation (1) is substituted into (2) and then solved for F_L, an expression can be obtained which gives LO frequencies causing spurs as follows:

Unusable LO center frequencies where F_R is known.

$$F_L \neq F_R \frac{(1-M)}{(1+N)} \pm \left[\frac{|M|B_R + |N|B_L + B_I}{2(1+N)}\right], \; N \neq -1 \qquad (3)$$

Unusable LO center frequencies where F_I is known.

$$F_L \neq F_I \frac{(1-M)}{(N+M)} \pm \left[\frac{|M|B_R + |N|B_L + B_I}{2(N+M)}\right], \; N \neq -M \qquad (4)$$

By plotting all the unusable LO center frequencies due to the M x N spur products, "holes" will appear which are the acceptable LO frequencies to choose from for spurious free operation. Figures 3.6-1 and -2 show these M x N spur product levels over their respective excluded (unusable) LO center frequencies for the full ACTS downlink frequency range.

The actual spur level produced in the receiver's mixer is a function of the drive level to the mixer. Figure 3.6-1 is based on an input carrier level of -10 dBm at the mixer, and Figure 3.6-2 is for a -20 dBm input. The -20 dBm input is slightly greater than the maximum level expected at the mixer given a -60 dBm receiver input. The amount each spur is decreased by reducing the drive level is given by:

$$M - 1 \text{ (dBc/dB)},$$

where M is the multiple of the RF input frequency.

FIGURE 3.6-1

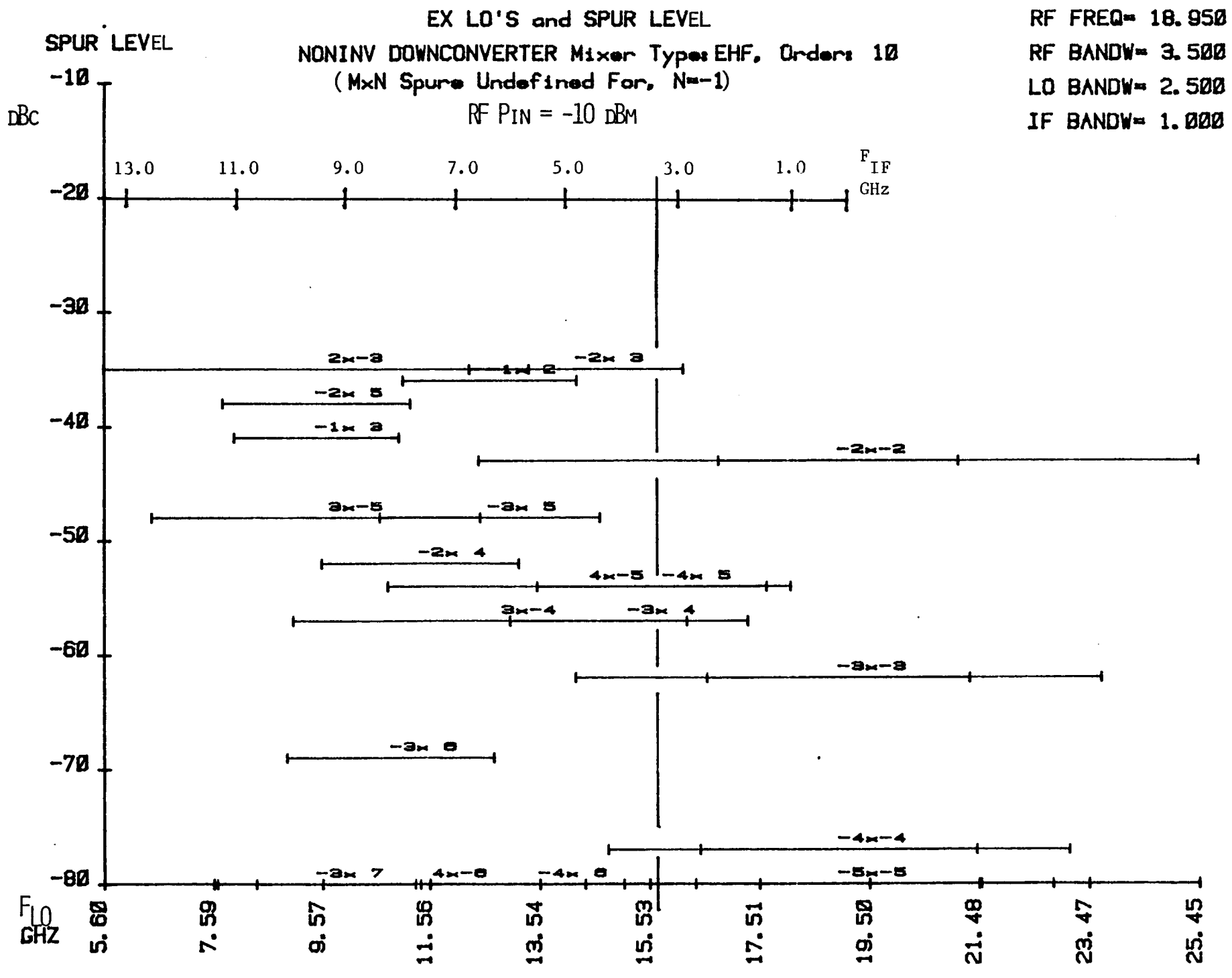
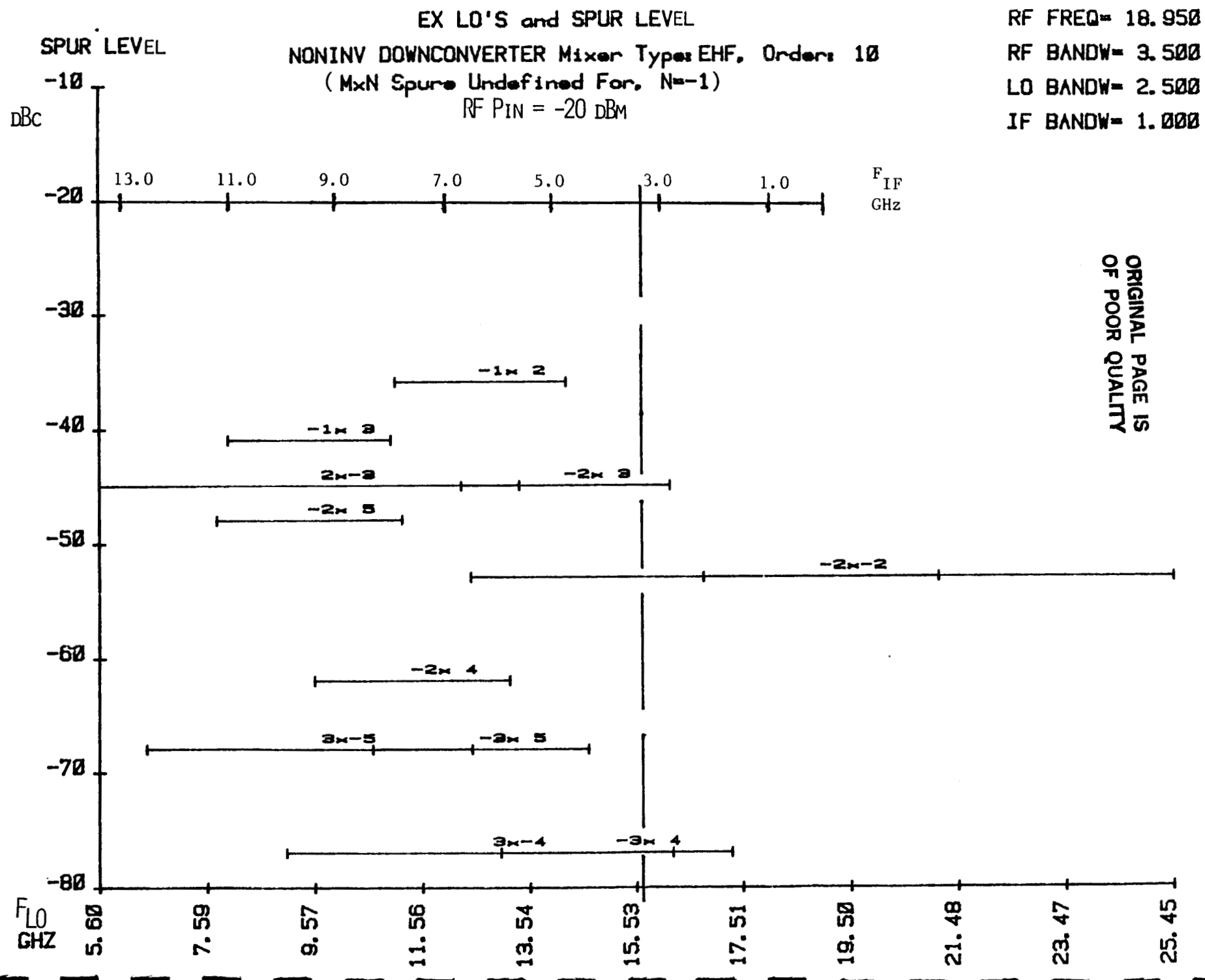

EX LO'S and SPUR LEVEL
NONINV DOWNCONVERTER Mixer Type: EHF, Order: 10
(MxN Spurs Undefined For, N=-1)
RF PIN = -10 DBM
RF FREQ= 18.950
RF BANDW= 3.500
LO BANDW= 2.500
IF BANDW= 1.000
SPUR LEVEL
DBc
-10
-20
-30
-40
-50
-60
-70
-80
13.0
11.0
9.0
7.0
5.0
3.0
1.0
F IF
GHz
2x-3
1x 2
-2x 3
-2x 5
-1x 3
-2x-2
3x-5
-3x 5
-2x 4
4x-5
-4x 5
3x-4
-3x 4
-3x-3
-3x 6
-4x-4
-3x 7
4x-6
-4x 6
-5x-5
F LO
GHZ
5.60
7.59
9.57
11.56
13.54
15.53
17.51
19.50
21.48
23.47
25.45

FIGURE 3.6-2



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OF POOR QUALITY

To obtain the typical spur levels given in the above figures (since data on the MMIC mixer won't be available until the breadboard development phase of Task II), three EHF catalog mixers from Watkins Johnson were used to generate an EHF mixer spur chart shown in Figure 3.6-3. This chart contains the worst spur levels (dBc) of the three combined mixers. A level of -20 dBc was used for each M x N product having no data available in the chart.

One final comment is needed on the excluded LO/spur level figures regarding the RF and IF bandwidths used. These figures are used to dipict inband generated spurs. The RF bandwidth required is 2.5 GHz, but 3.5 GHz is used to enable spurs to be shown which are caused from frequencies just outside the inband RF range. As it turns out no additinal spurs are incountered by increasing the RF bandwidth to 3.5 GHz. The IF bandwidth is set to 1.0 GHz which is the IF filter's 45 dB bandwidth. The IF filter's attenuation mask is shown in Figure 3.6-4.

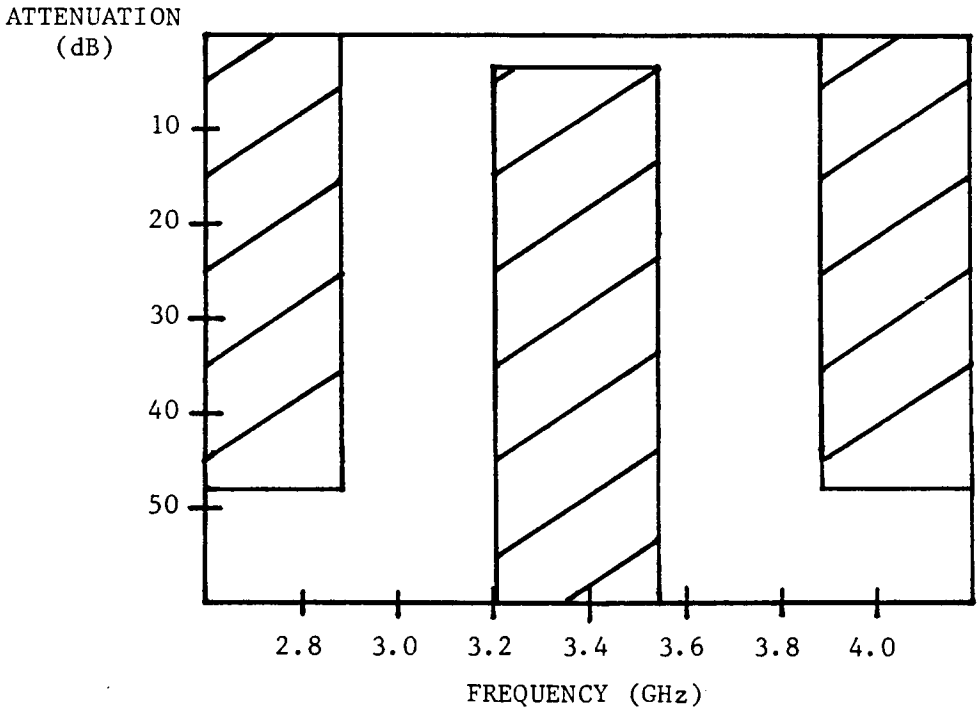
Notice that figures 3.6-1 and -2 may have M x N spurs which are undefined for N = -1. This is so because when N = -1, equation (3) becomes unbounded. When equation (4) is used to plot excluded LOs versus spur level given the IF center frequency of 3.37 GHz, there are no spurs with N = -1 in the ACTS frequency band. Therefore the spurs to be controlled are -2 x 3, |2| x |2|, and |3| x |4|. For an input level to the mixer of -20 dBm, only the -2 x 3 and |2| x |2| products are of concern. If the IF center frequency were lowered to less than 2.8 GHz, only the |2| x |2|products would be inband and at a typical -53 dBc level. However, the spurs generated for the ACTS 3.373 GHz will be managed to no more than -45 dBc as shown in Figure 3.6-2.

COMBINED SPUR CHART - WJ M14, M14A, M20, MIXERS FOR PIN = -10 dBm

M \ N	0	1	2	3	4	5	6	7	8
7				52	69	74	>80	>80	>80
6				>80	>80	>80	>80	>80	79
5			>80	>80	45	>80	>80	>80	>80
4			>80	65	77	54	>80	53	>80
3	50	>80	>80	62	57	48	69	>80	>80
2	38	42	43	35	52	38	63		
1	20	0	36	41					
0									

FIGURE 3.6-3

IF FILTER ATTENUATION MASK



- 6 POLE CHEBYSHEV
- DUROID 6010 SUBSTRATE
- 3.0" X 0.5" X 0.025"

FIGURE 3.6-4

INVERTING DOWNCONVERTER

The equations governing the inverting downconverter's spur generation are derived in a similar fashion to the non-inverting case.

$$F_L \neq F_R \frac{(1+M)}{(1-N)} \pm \left[\frac{|M|B_R + |N|B_L + B_I}{2(1-N)}\right]; \; N \neq 1$$

$$F_L \neq F_i \frac{(1+M)}{(N+M)} \pm \left[\frac{|M|B_R + |N|B_L + B_I}{2(N+M)}\right]; \; N \neq -M$$

Figures 3.6-5 and -6 show the M x N spur product levels over their respective excluded LO center frequencies for the inverting downconverter approach. Although the typical performance of the inverting downconverter is slightly better (by 8 dB) than the non-inverting approach, they both will satisfy the receiver's -45 dBc specification. As higher frequency LOs are more expensive, the non-inverting configuration is chosen for the NASA-Lewis receiver.

3.6.2 Out Of Band Rejection

Figures 3.6-7 and -8 show the receiver's out of band rejection to frequencies above 22.2 GHz (3.6-7) and below 15.7 GHz (3.6-8). To meet the requirement of 45 dB rejection, an RF filter is used having the attenuation characteristics of Figure 3.6-9. FOUT, LO and FOUT, HI show the starting and stopping frequencies of a spur which passes through the defined IF bandpass filter (FB1 and FB2). FI, LO and Fl, HI are the input RF frequencies at which a spur crosses the defined IF filter bandedges (FB1 and

FIGURE 3.6- 5

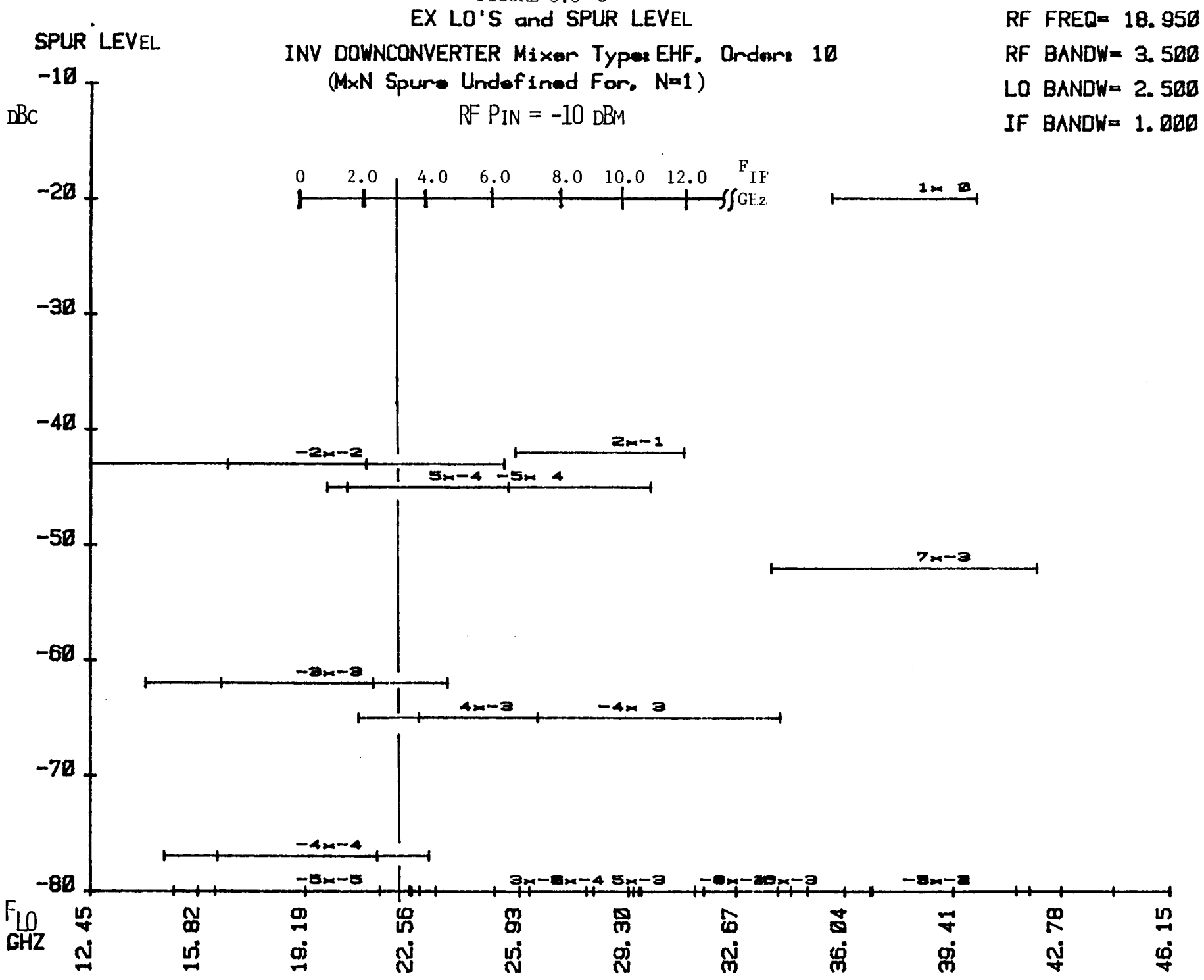

EX LO'S and SPUR LEVEL
INV DOWNCONVERTER Mixer Types EHF, Orders 10
(MxN Spurs Undefined For, N=1)
RF PIN = -10 DBM
RF FREQ= 18.950
RF BANDW= 3.500
LO BANDW= 2.500
IF BANDW= 1.000
SPUR LEVEL
DBc
-10
-20
-30
-40
-50
-60
-70
-80
0
2.0
4.0
6.0
8.0
10.0
12.0
F IF
GHz
1x 0
-2x-2
2x-1
5x-4
-5x 4
7x-3
-3x-3
4x-3
-4x 3
-4x-4
-5x-5
3x-3x-4
5x-3
-3x-3
-3x-3
F LO
GHZ
12.45
15.82
19.19
22.56
25.93
29.30
32.67
36.04
39.41
42.78
46.15

FIGURE 3.6- 6

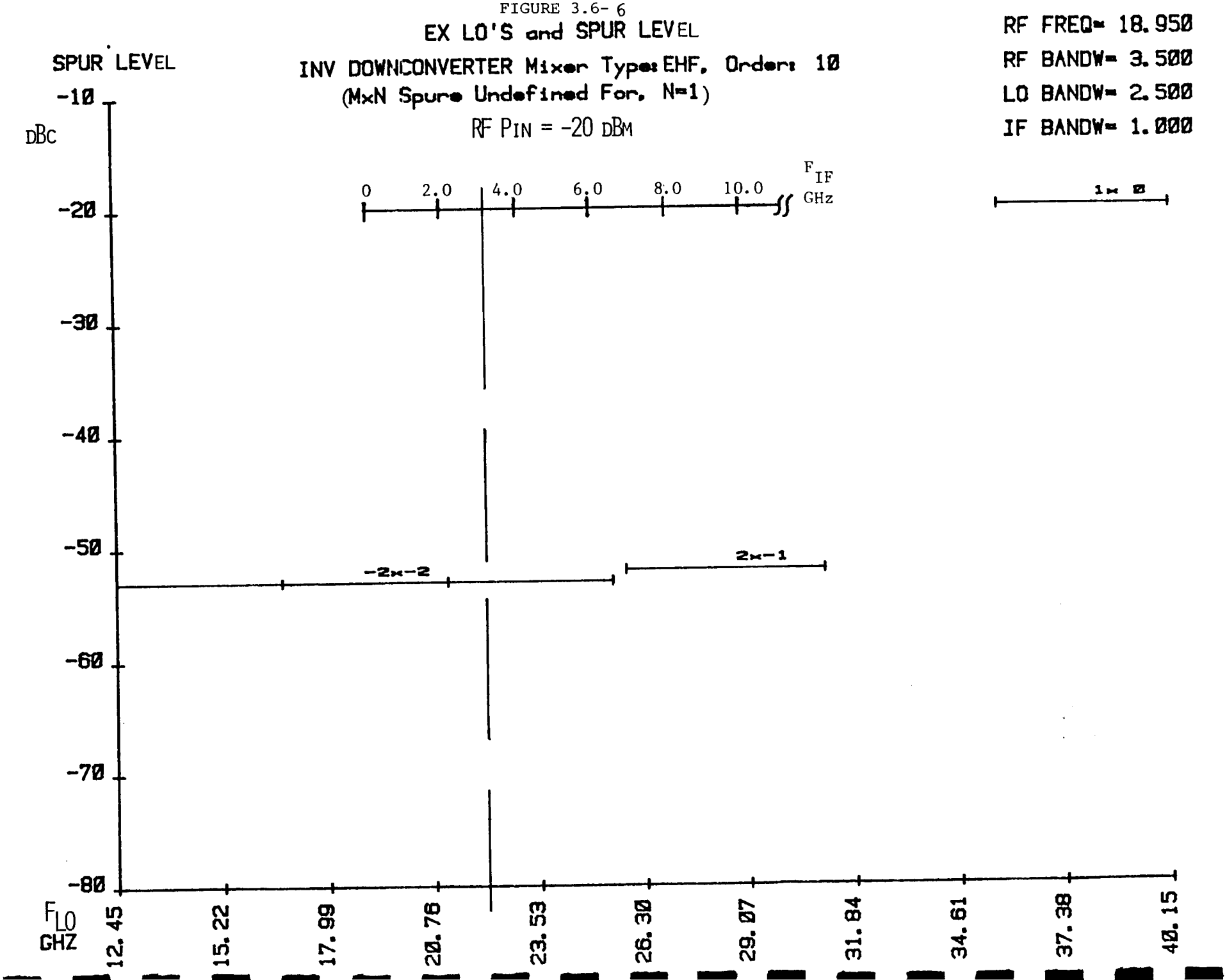
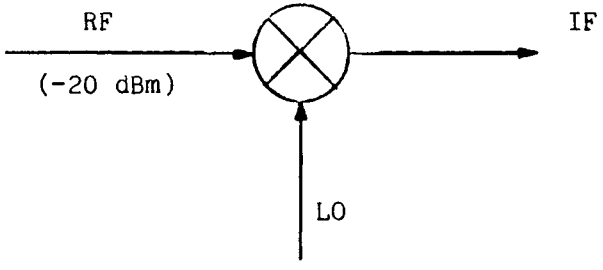

EX LO'S and SPUR LEVEL
INV DOWNCONVERTER Mixer Type: EHF, Order: 10
(MxN Spurs Undefined For, N=1)
RF PIN = -20 DBM
RF FREQ= 18.950
RF BANDW= 3.500
LO BANDW= 2.500
IF BANDW= 1.000
SPUR LEVEL
DBc
-10
-20
-30
-40
-50
-60
-70
-80
0
2.0
4.0
6.0
8.0
10.0
F IF
GHz
1x 0
-2x-2
2x-1
F LO
GHZ
12.45
15.22
17.99
20.76
23.53
26.30
29.07
31.84
34.61
37.38
40.15

FIGURE 3.6-7

OUT OF BAND REJECTION
F_{RF} > 22.2 GHz

ENTER F11, F12: 22.2, 40
ENTER F21, F22: 14.3, 16.8
ENTER FB1, FB2: 2.873, 3.873

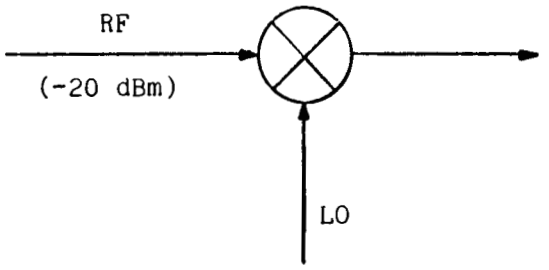


ENTER MAXIMUM ORDER: 6

M	N	FOUT, LO	FOUT, HI	F1, LO	F1, HI	SPECIFIED SPUR LEVEL (dBc)	RFA & FILTER (dB)	REJECTION (dB)
-1	2	-11.40	11.40	24.73	30.73	---	55	55
1	-2	-11.40	11.40	31.47	37.47	---	60	60
-1	3	2.90	28.20	39.03	40.00	---	60	60
-2	3	-37.10	6.00	22.20	23.77	-45	30	75
2	-3	- 6.00	37.10	22.89	27.44	-45	35	75
-2	4	-22.80	22.80	26.67	32.67	---	65	65
2	-4	-22.80	22.80	30.04	35.54	---	60	65

FIGURE 3.6-8
OUT OF BAND REJECTION
F_{RF} < 15.7 GHz

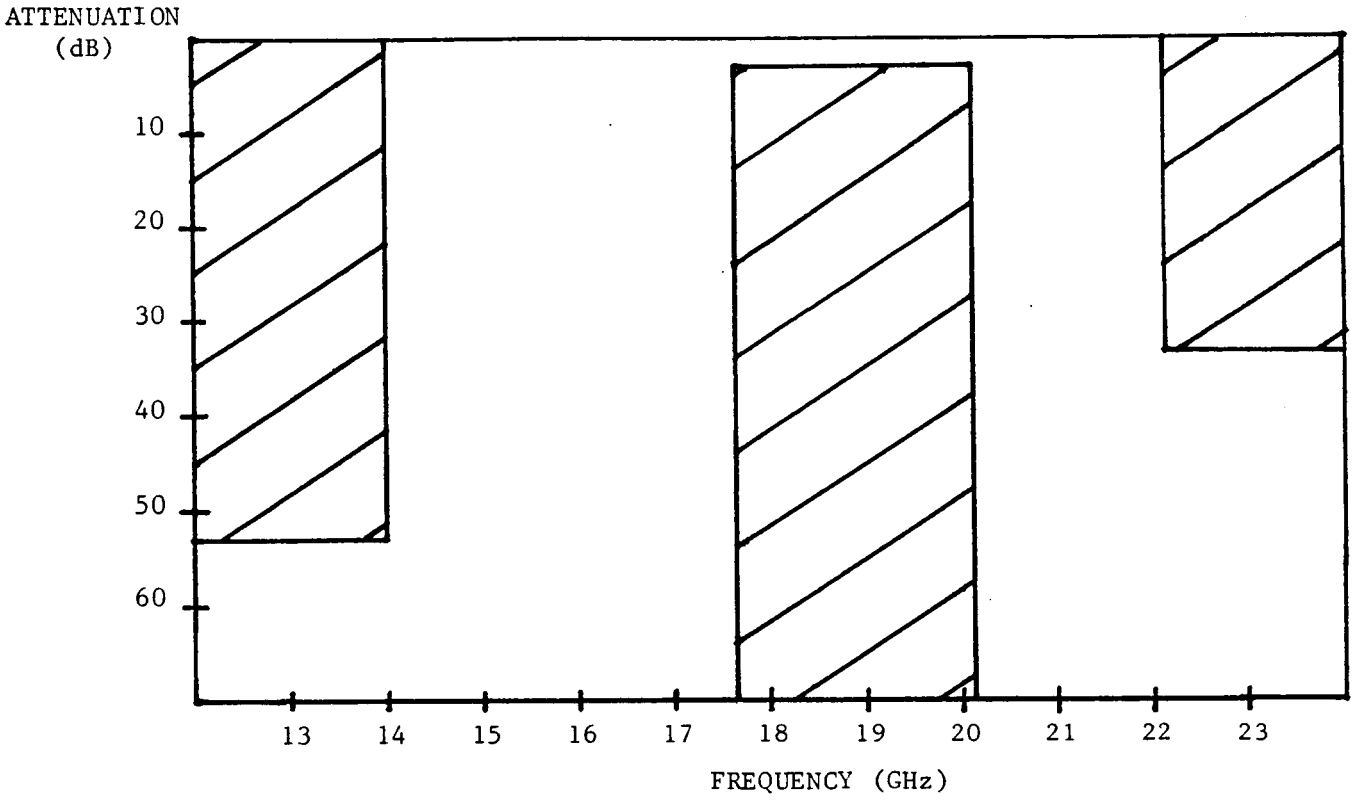
ENTER F11, F12: 10, 15.7
ENTER F21, F22: 14.3, 16.8
ENTER FB1, FB2: 2.873, 3.873



ENTER MAXIMUM ORDER: 6

M	N	FOUT, LO	FOUT, HI	F1, LO	F1, HI	SPECIFIED SPUR LEVEL (dBc)	RFA & FILTER (dB)	REJECTION (dB)
-1	1	- 1.40	6.80	10.43	13.93	0	50	50
2	-1	3.20	17.10	10.00	10.34	---	70	70
-2	2	-2.80	13.60	12.36	15.36	-45	30	75
-3	2	-18.50	3.60	10.00	10.24	---	70	70
3	-2	- 3.60	18.50	10.49	12.49	---	60	60
-3	3	- 4.20	20.40	13.01	15.70	-45	30	75
3	-3	-20.40	4.20	15.26	15.70	-45	30	75

RF FILTER ATTENUATION MASK



- 5 POLE CHEBYSHEV
- FUSED QUARTZ SUBSTRATE
- 0.75" X 0.25" X 0.010"

FIGURE 3.6-9

FB2) with the LO frequencies being such as to allow the maximum difference between F1, HI and LO. This range of input frequencies producing a spur within the IF filter is defined as:

$$F_{RF\ SPUR} = \frac{F_{IF} - NF_{LO}}{M} \pm \frac{1}{2|M|}\,(B_{IF} + |N|B_{LO})$$

The specified spur level column is the spec level placed on the mixer for the respective M x N product. Only those products shown in Figure 3.6-1 which cross the IF_C = 3.373 GHz have a specified level. The RFA and filter column lists the minimum rejection of the combined RFA and RF filter to the FI, LO to FI, HI frequencies. Finally, the overall out of band rejection is the summation of these two columns.

3.6.3 Subband Spurious Response

Figure 3.6-10 and -11 show the subband spurious responses for 19.96 GHz and 19.50 GHz, respectively. These figures are a subset of the full ACTS frequency band shown in Figure 3.6-1 and -2. Note that the highest spur level (a -2 x 3 product) does not show up in these two subbands. This is because the LO frequency is fixed and not tuned over its entire 2.5 GHz range in these cases.

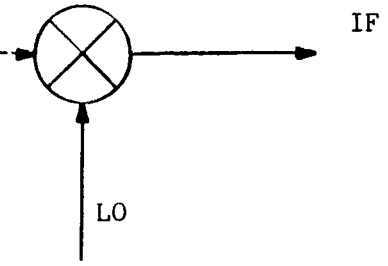
3.6.4 Adjacent Channel Rejection

Figure 3.6-12 shows the nominal IF filter response translated to the RF input and the resulting rejection to the adjacent channel. The power

FIGURE 3.6-10

INBAND IRM GENERATED SPURIOUS RESPONSE

ENTER F11, F12: 17.7, 20.2
ENTER F21, F22: 16.587, 16.587
ENTER FB1, FB2: 2.873,3.873



ENTER MAXIMUM ORDER: 10

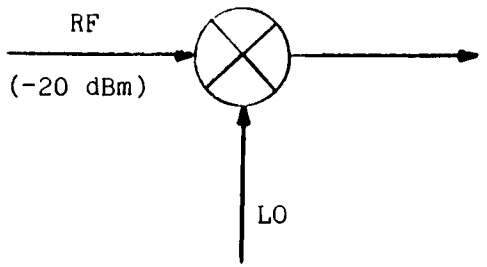
M	N	FOUT, LO	FOUT, HI	F1, LO	F1, HI	SPECIFIED SPUR LEVEL (dBc)	TYPICAL LEVEL (dBc)
2	-2	2.23	7.23	18.02	18.52	-45	-53
3	-3	3.34	10.84	17.70	17.88	-45	-82
-4	5	2.13	12.13	19.77	20.02	-45	-84

BAND 1 SINGLE TONE INTEMODULATION ANALYSIS

FIGURE 3.6-11

INBAND IRM GENERATED SPURIOUS RESPONSE

ENTER F11, F12: 17.7, 20.2
ENTER F21, F22: 16.122, 16.122
ENTER FB1, FB2: 2.873,3.873



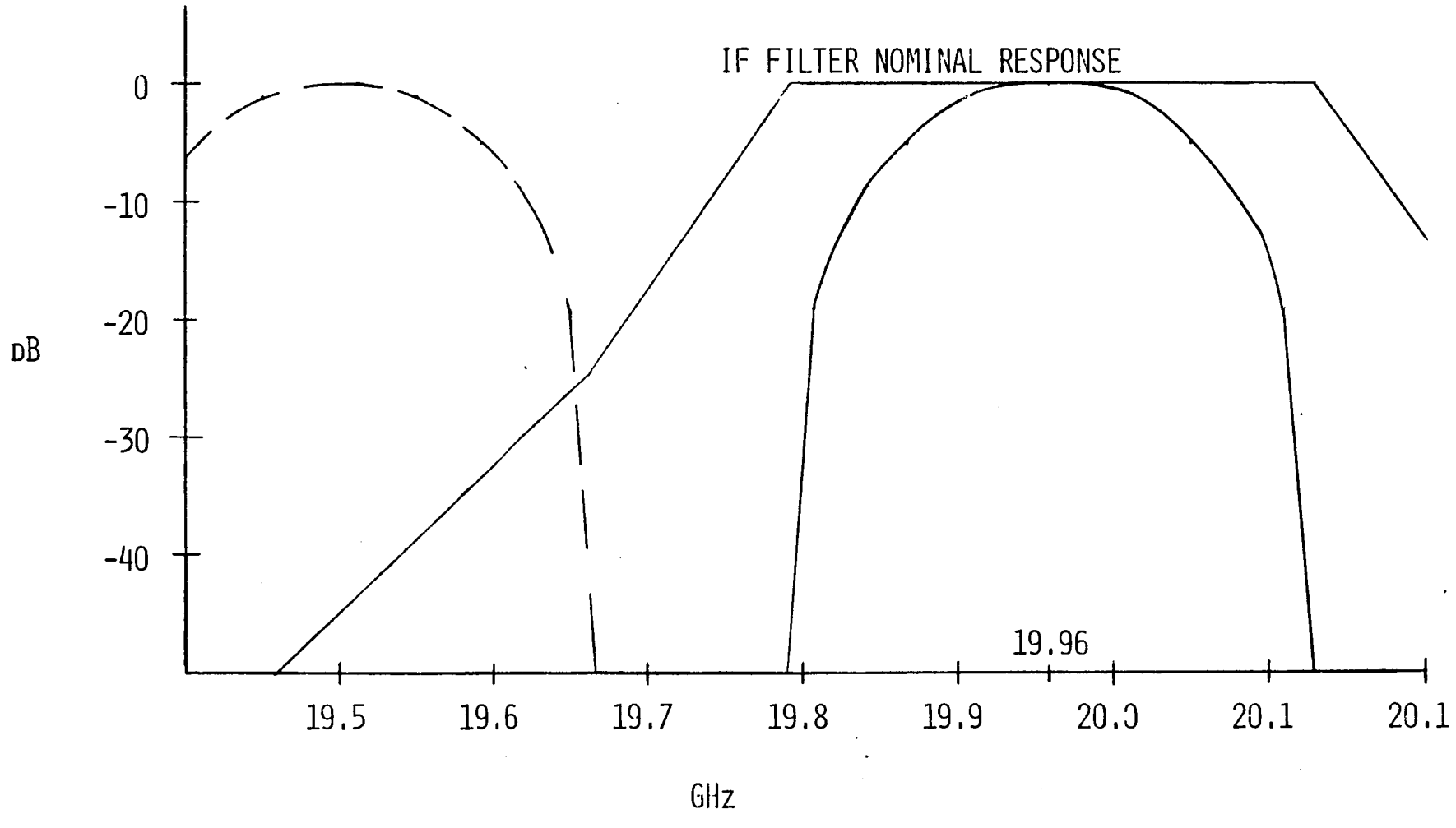
ENTER MAXIMUM ORDER: 10

M	N	FOUT, LO	FOUT, HI	F1, LO	F1, HI	SPECIFIED SPUR LEVEL (dBc)	TYPICAL LEVEL (dBc)
2	-2	3.16	8.16	17.70	18.06	-45	-53
-4	5	-.19	9.81	19.18	19.43	-45	-84

BAND 2 SINGLE TONE INTERMODULATION ANALYSIS

FIGURE 3.6-12

ADJACENT CHANNEL REJECTION



spectral density of each channel is assumed to be of(sin x)/x form filling the full 332 MHz wide channel from null to null. This rejection will be even greater as the signals pass through the more narrow IF filter within the modem.

3.7 DC POWER

Figures 3.7-1 through -3 show the DC power distribution, positive and negative regulators respectively. As shown in Figure 3.7-1 ±15 VDC has been selected for the receiver operating voltages. The LO will be specified to run off ±15 VDC, also, but if significantly increased costs results from the LO vendor(s), a different voltage will be required for the LO to keep unit production costs low. The positive regulators used will have a slower turn on than the negative regulators to insure stable FET power up at turn on and also to limit the turn on current surge in conjunction with L1. Temperature compensation will be added by placing diodes in series with the output voltage sampling resistors, R1 and R2 in Figure 3.7-3.

3.8 MECHANICAL CONFIGURATION

Figures 3.8-1 and -2 dipict the overall receivers mounting arrangement, I/O connections and outline dimensions. Figure 3.8-3 dipicts the receiver's signal path circuitry layout. EMI/RFI Gaskets are being provided for each cover and waveguide input. The top part of this housing contains all RF circuits through the image reject mixer, and the bottom half contains all IF components. Bias circuitry is housed in a separate compartment along side the signal path compartments. The overall housing will be a machined part

FIGURE 3.7-1
20 GHz RECEIVER BIAS PLAN

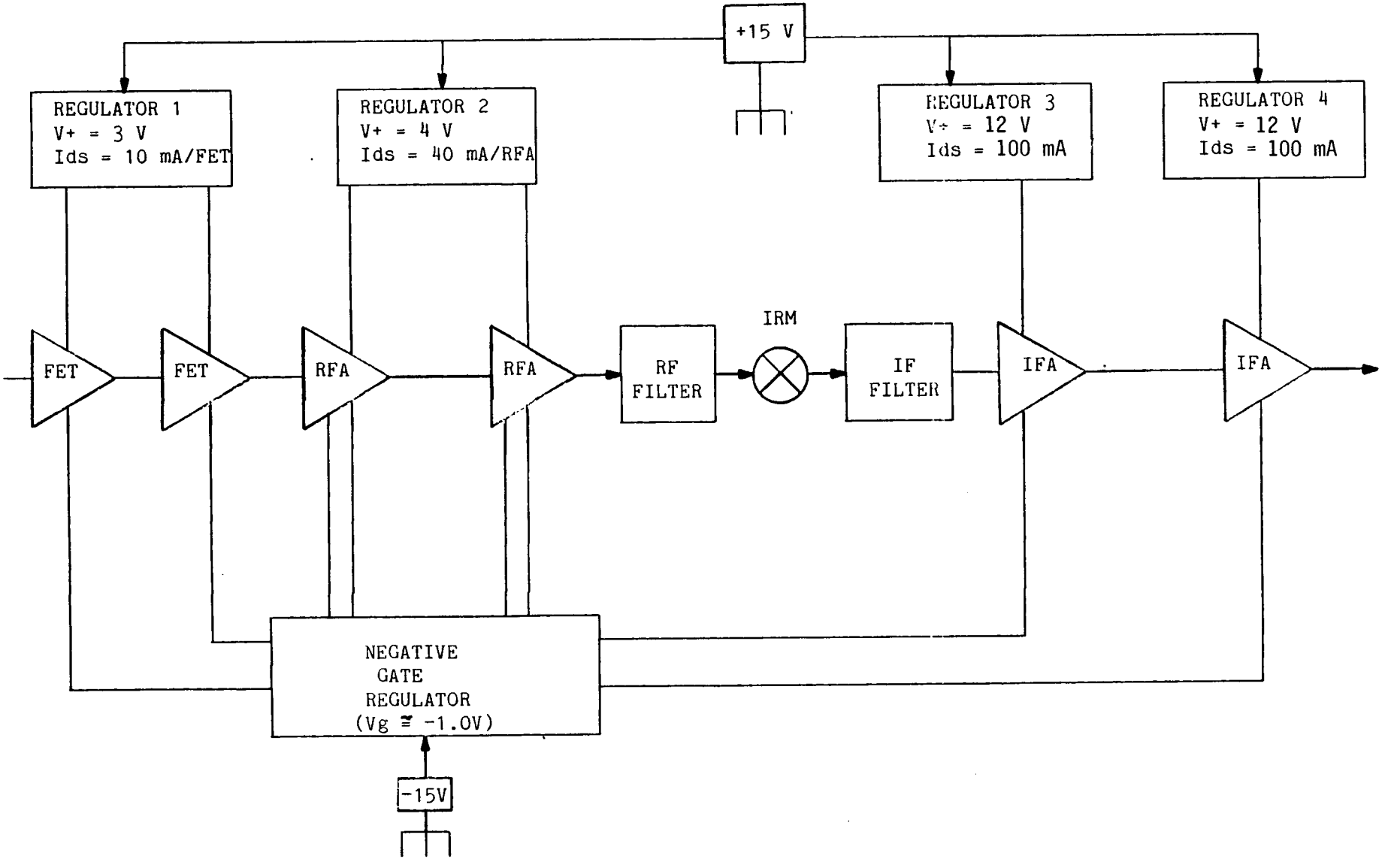
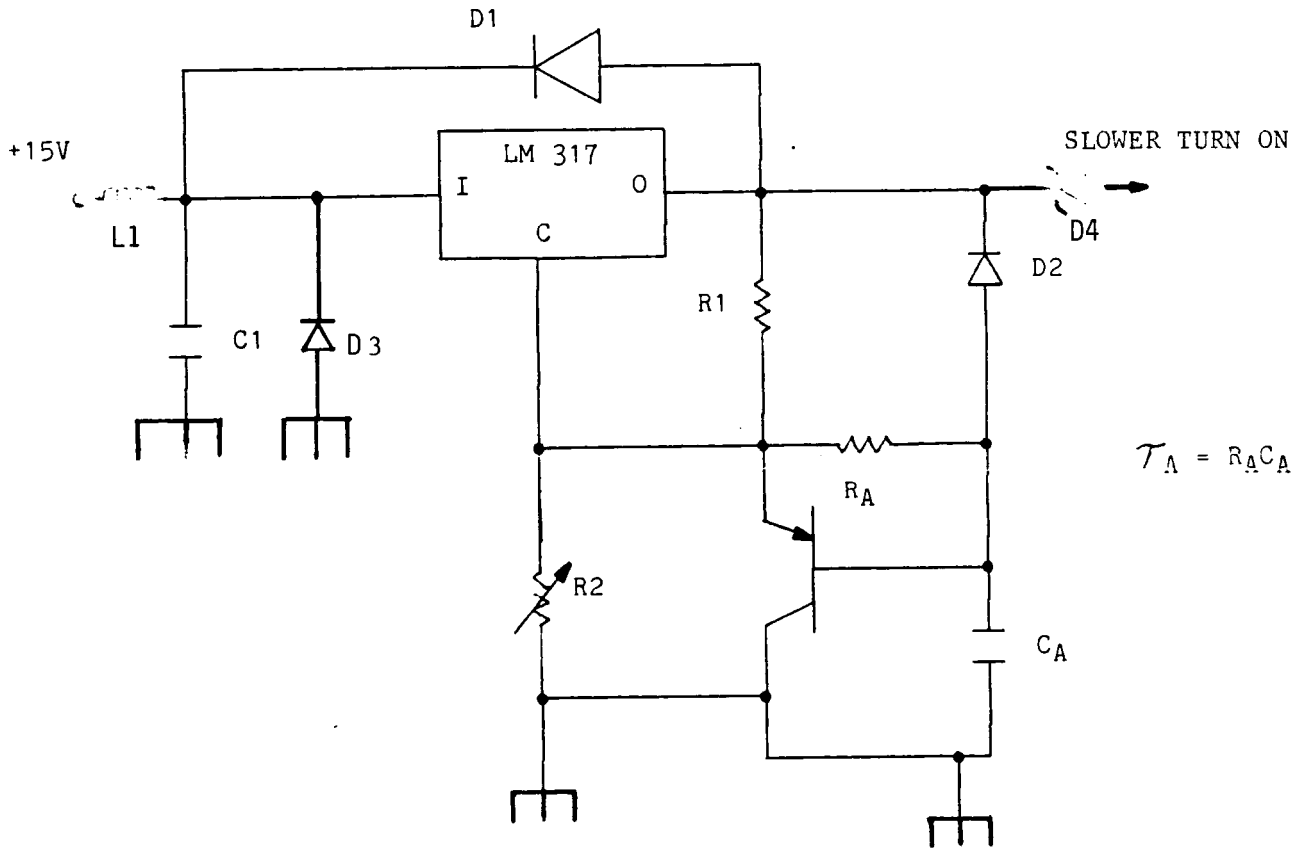


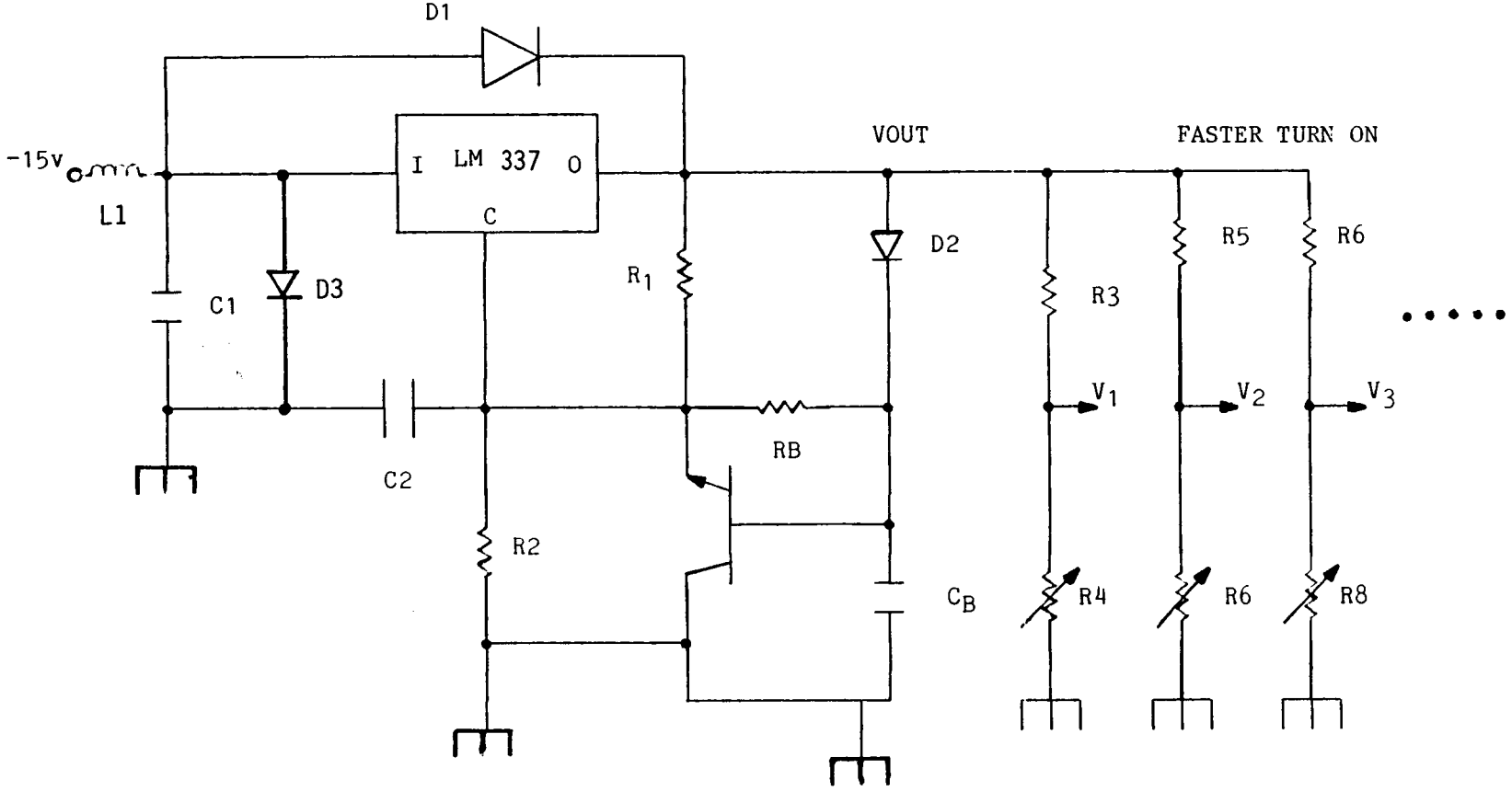
FIGURE 3.7-2

POSITIVE REGULATOR



ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE 3.7-3
NEGATIVE REGULATOR



$\tau_B = R_B C_B$

$\tau_A > \tau_B$

FIGURE 3.8-1
MOUNTING AND CABLING CONFIGURATION

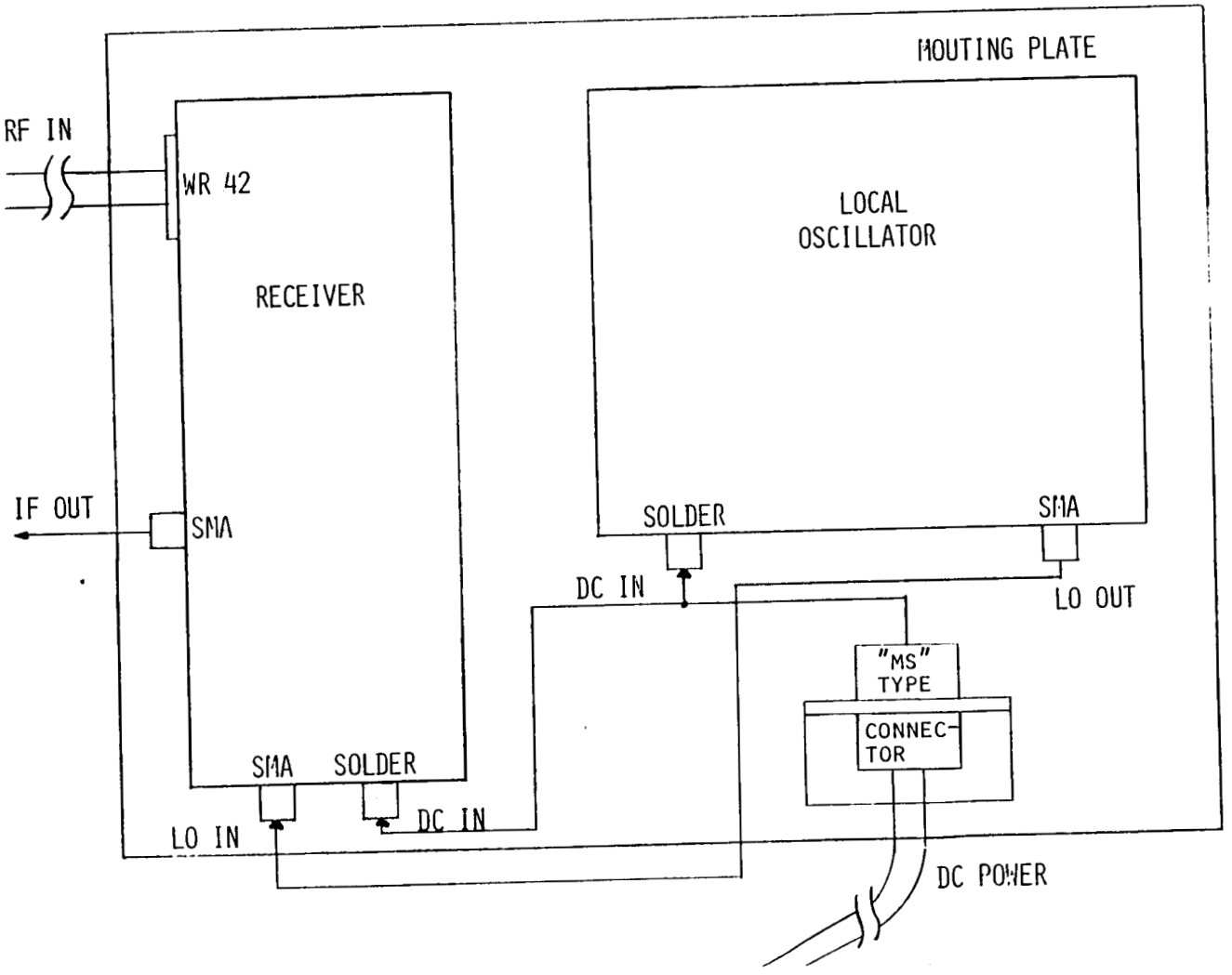


FIGURE 3.8-2

20 GHz LOW NOISE RECEIVER ASSEMBLY
MAXIMUM OUTLINE DIMENSIONS

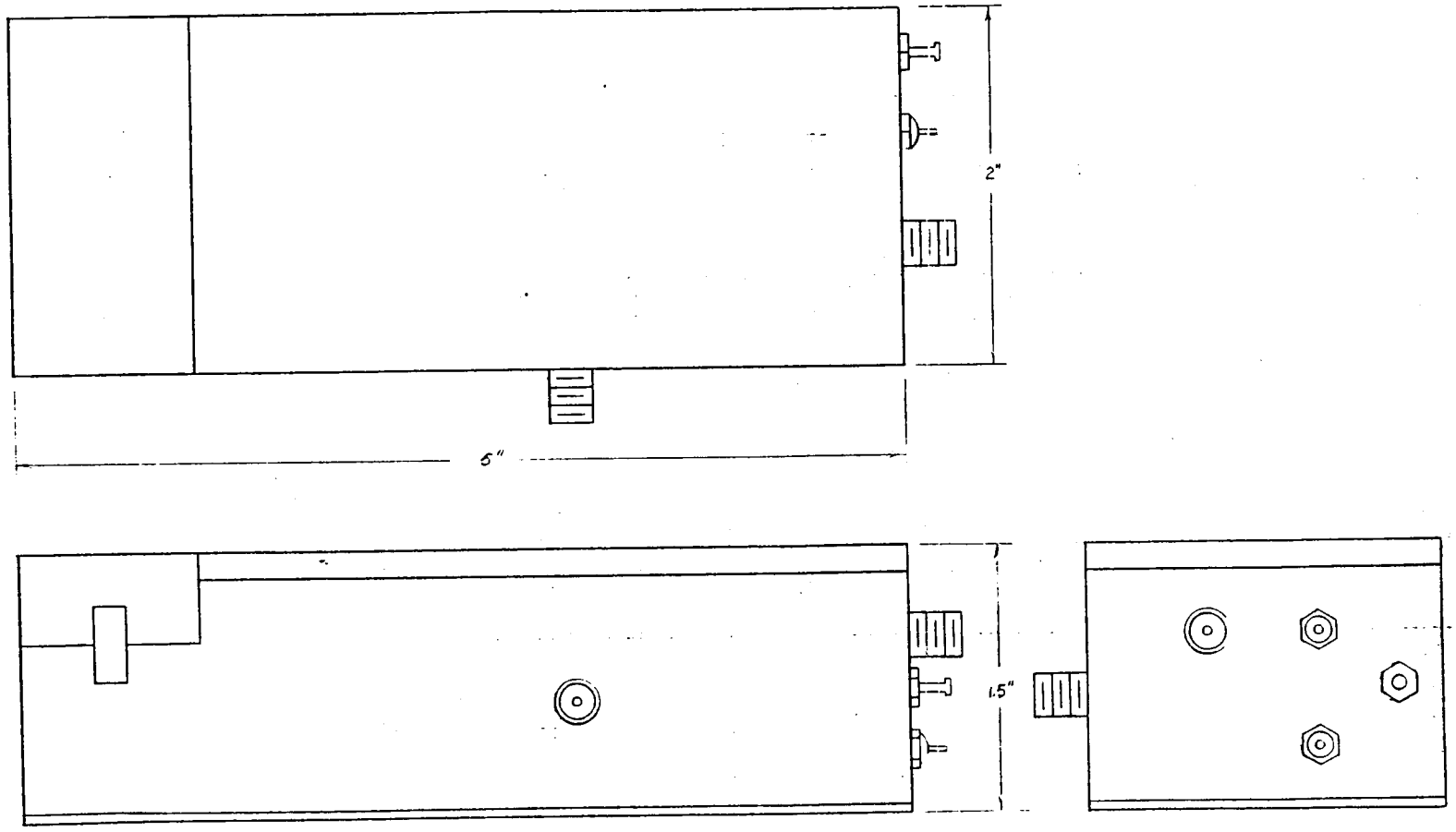
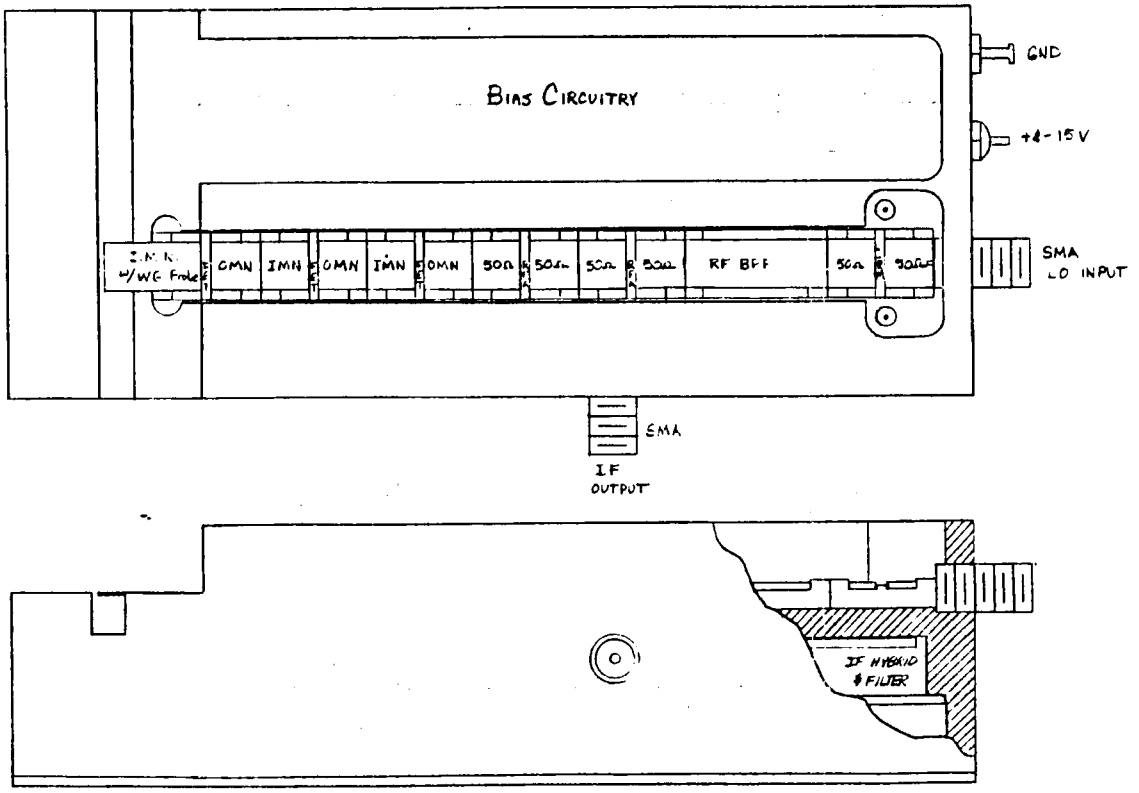


FIGURE 3.8-3

20 GHz LOW NOISE RECEIVER ASSEMBLY TOP REMOVED

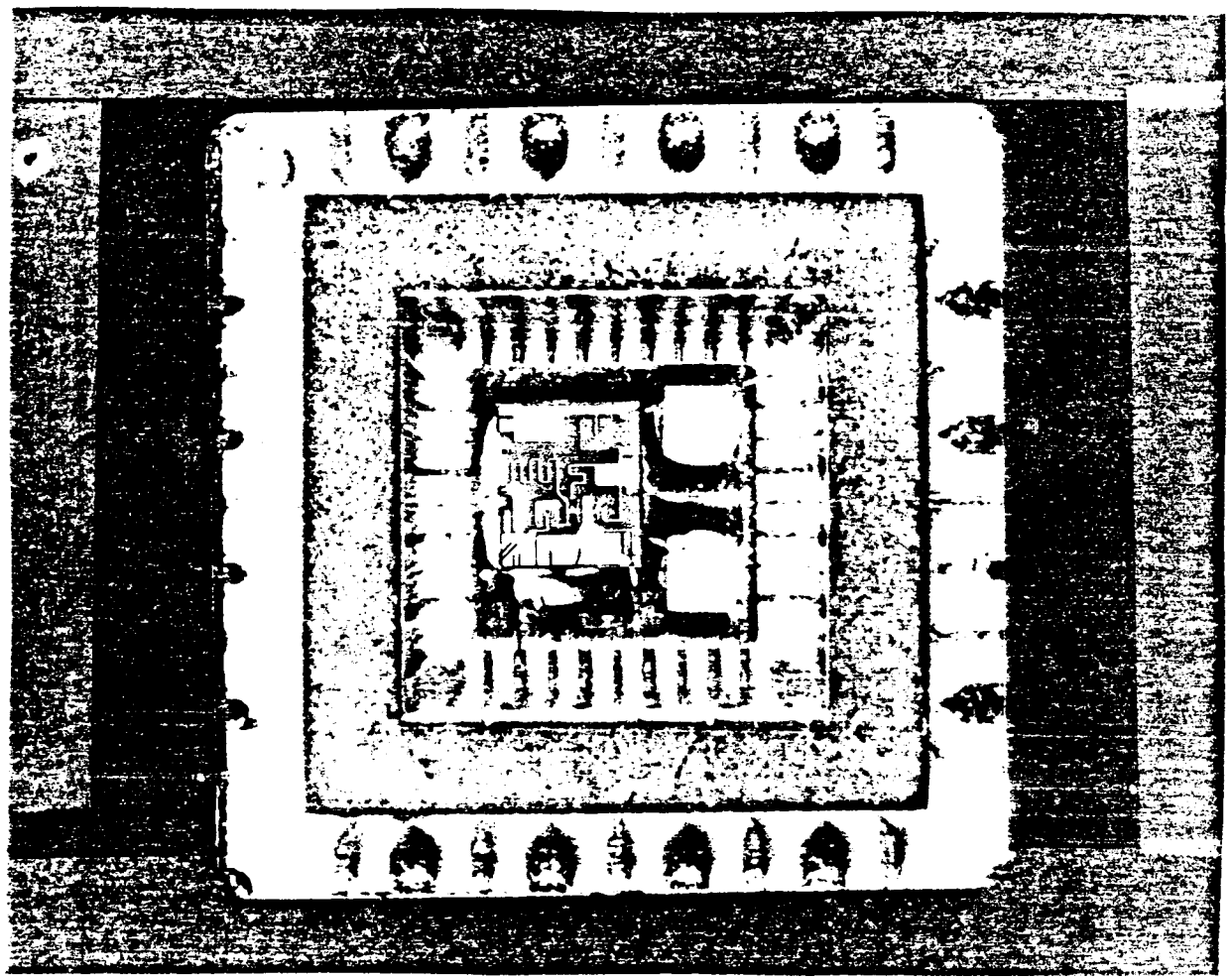


made from drawings which can be used to produce cast housings in production quantities for cost reduction.

Figure 3.8-4 shows a MMIC leadless chip carrier (LCC) developed by Harris which will be used for the IF amplifiers. We are currently extending this MMIC packaging concept to beyond 20 GHz. If feasible during the POC design time frame, the RF amplifier and image reject mixer would also be packaged in an LCC. The current baseline plan is to have these circuits bonded to the substrate like the discrete LNA FETs.

FIGURE 3.8-4

LEADLESS MMIC CHIP CARRIER



- EASY HANDLING
- SOLDERABLE
- HERMITIC PACKAGE

NASA-Lewis

POC 20 GHz RECEIVER

BREADBOARD DEVELOPMENT

TEST REPORT

10 JULY 1987

HARRIS

HARRIS CORPORATION GOVERNMENT COMMUNICATION SYSTEMS DIVISION
P.O. BOX 91000, MELBOURNE, FLORIDA 32902 (407) 729-2222

TABLE OF CONTENTS

1.0 INTRODUCTION

This report describes and interprets the data taken during the breadboard development phase (Task II) of the NASA-Lewis 20 GHz Receiver Program. Sections 2.0 through 7.0 describe the circuits which were breadboarded and proceed from the LNA through the receiver including the DC regulator. Section 8.0 concludes the report with an assessment of the impacts of the breadboard performance on the overall POC receiver performance.

2.0 LOW NOISE AMPLIFIER

During the proposal time frame an NEC (NE 673) FET (which was not released at that time) was selected as the baseline device to be used in the receiver's LNA. Since that time the device was released, but it was targeted and optimized for a different frequency band than that of ACTS. Harris surveyed the available low noise devices on the market during the preliminary design phase and selected the NEC device NE04500G for its replacement. In parallel with the NASA POC 20 GHz Receiver Program, Harris' IR&D was investigating HEMT FET devices. A Gould HEMT (H503) was selected for investigation on the IR&D. Since both devices would be evaluated at the same time, Harris decided to select the best overall FET for use in the NASA Receiver.

Figure 2-1 shows the two device types evaluated at Harris. Gain and Noise Figure averages are shown for each device versus frequency. The data for each device was taken over frequency with each device tuned for optimum performance at 20 GHz. The data includes the input/output matching circuits and is representative of a single LNA stage performance. A single stage amplifier in the receiver would have a higher noise figure over the ACTS frequency band than that shown at 20 GHz due to the effects of a broadband input matching circuit. The Gould HEMT FET has superior gain and noise performance over the ACTS frequency band and was selected to be used in the breadboard LNA.

Two test fixtures were built to characterize the LNA devices, one made in coax and the other in waveguide. The waveguide fixture is much superior and is shown in Figures 2-2 and 2-3. Using this test fixture a method of calculating the FET's noise parameters based on measured noise figures was implemented. Characterization of the low noise FET parameters (F_{min}, r_n, g_{opt}, and b_{opt}) was accomplished by measuring the FET's noise figure with various source impedances (Zs) presented to its input. Connecting the various stub "dots" of the input circuit to the transmission line in a methodical fashion results

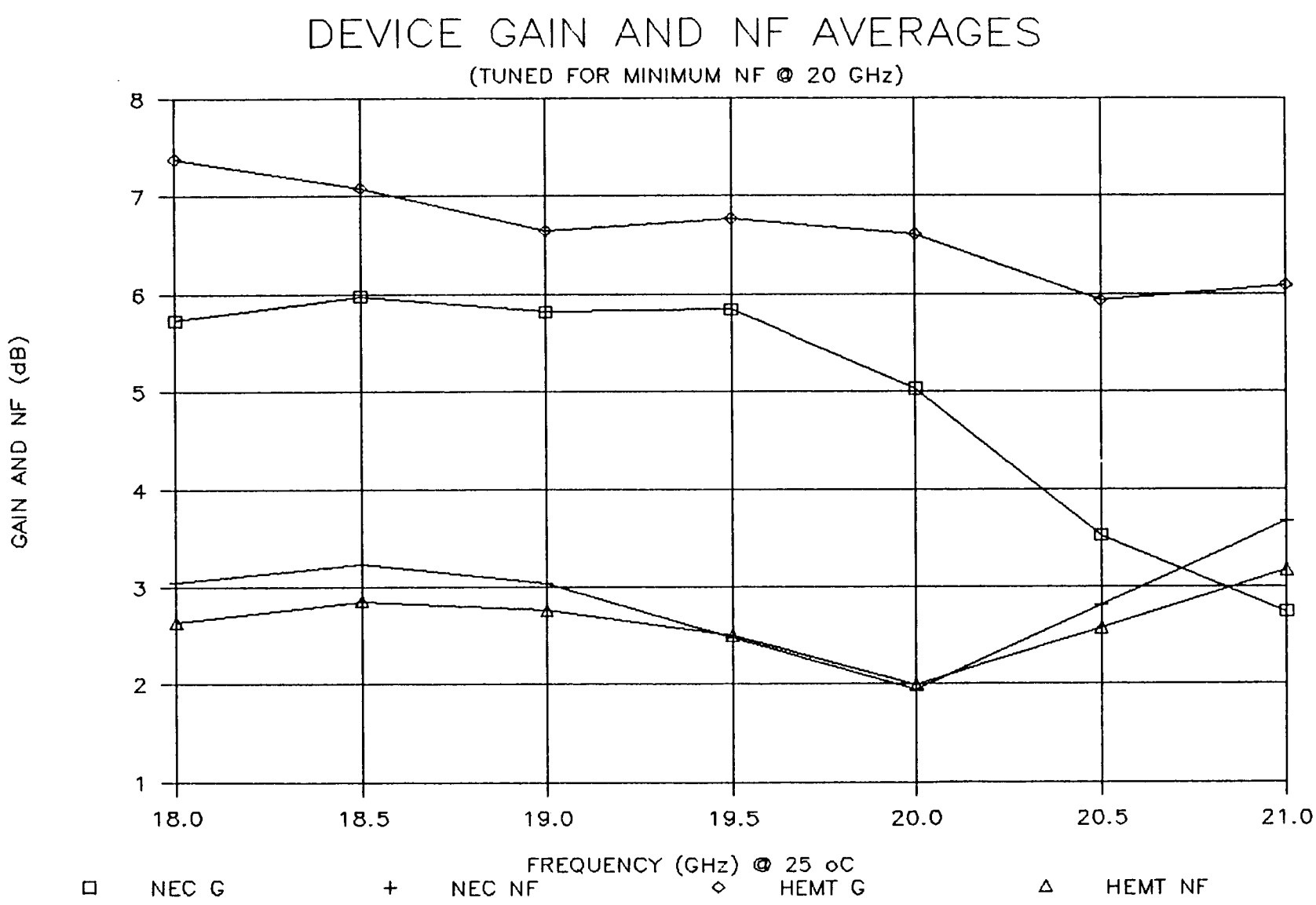
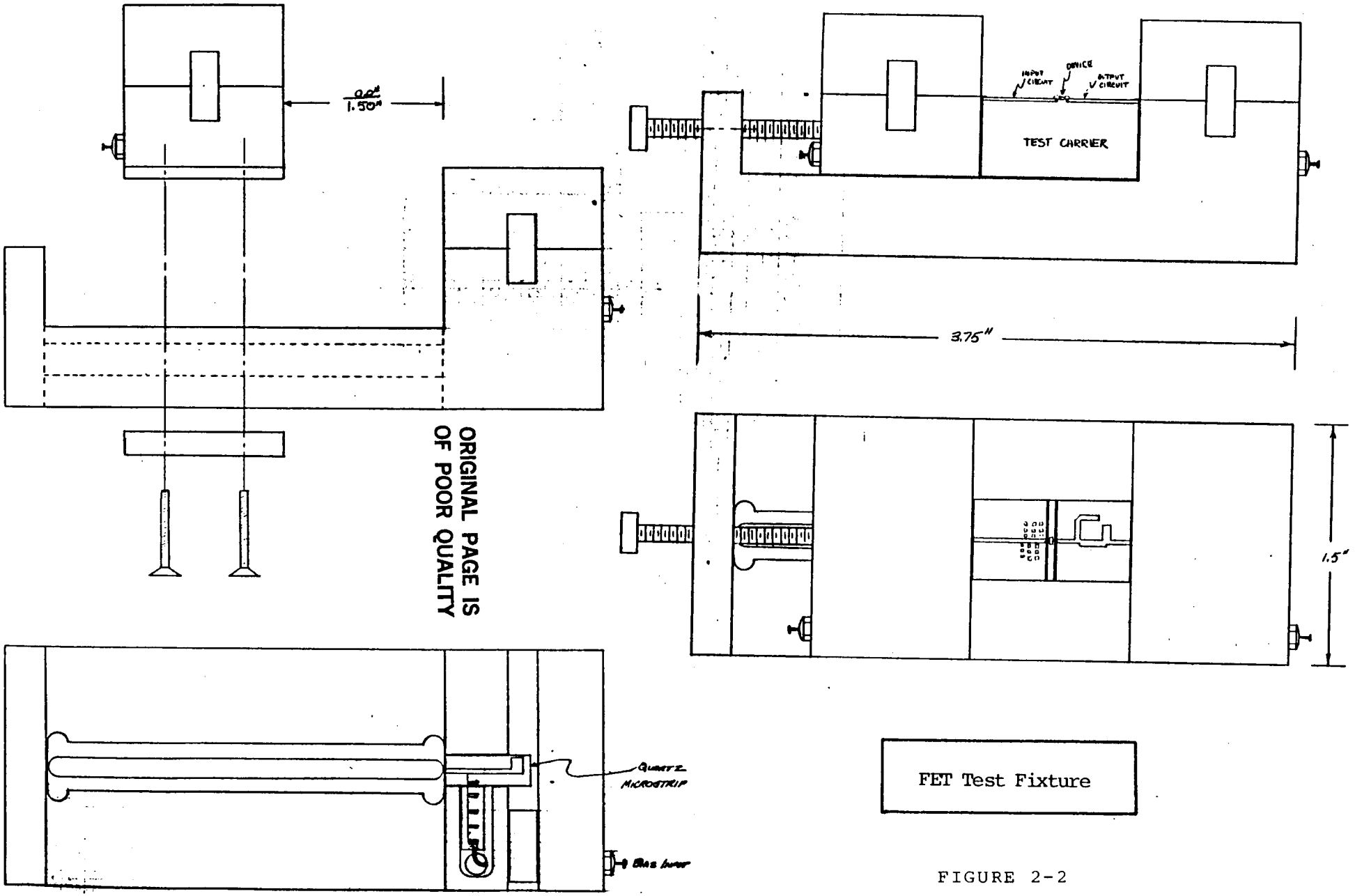

DEVICE GAIN AND NF AVERAGES
(TUNED FOR MINIMUM NF @ 20 GHz)
GAIN AND NF (dB)
8
7
6
5
4
3
2
1
18.0
18.5
19.0
19.5
20.0
20.5
21.0
FREQUENCY (GHz) @ 25 oC
NEC G
NEC NF
HEMT G
HEMT NF

FIGURE 2-1



FET Test Fixture

FIGURE 2-2

LNA & DEVICE TEST FIXTURE

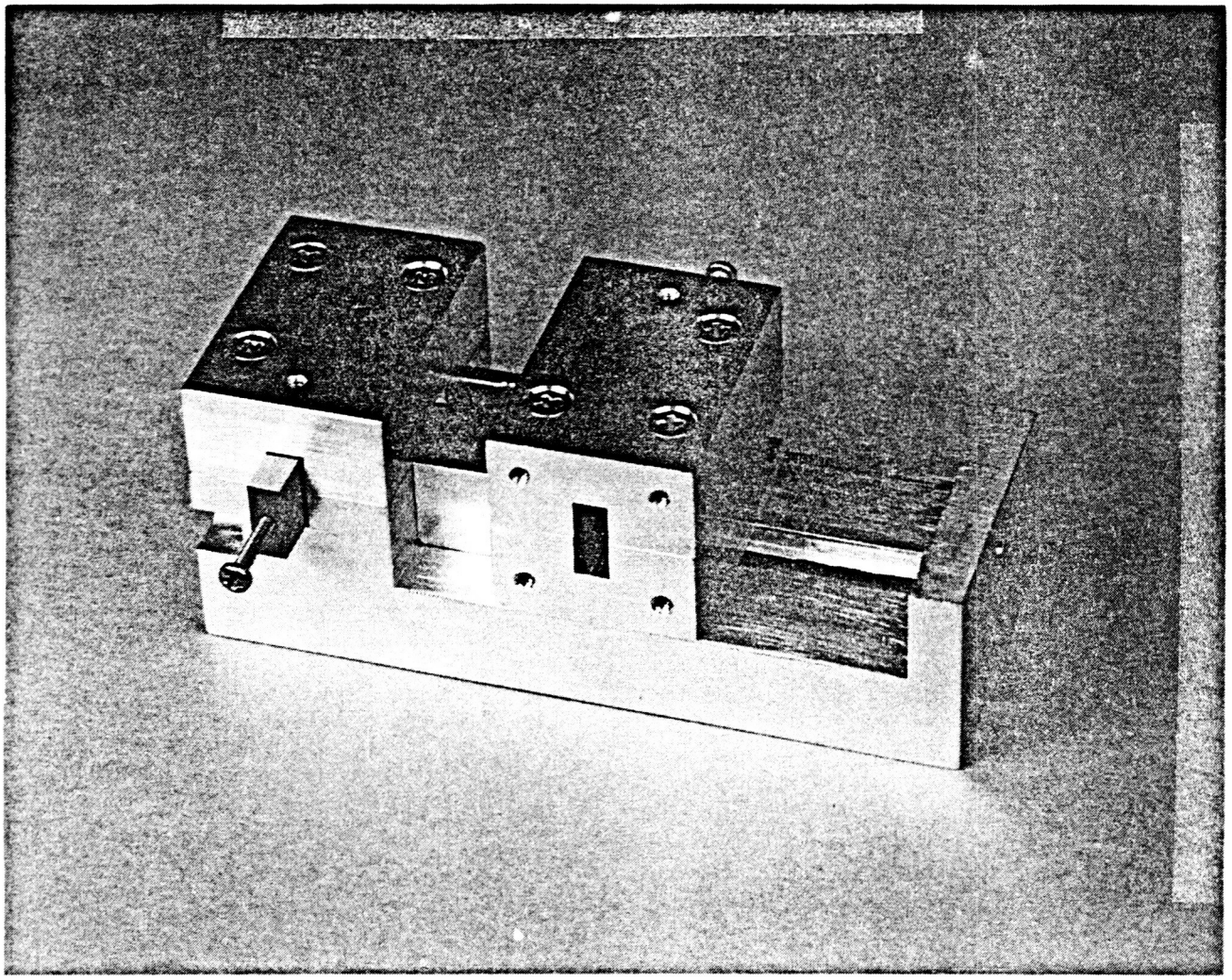


FIGURE 2-3

in impedances being presented to the FET's input as shown in Figure 2-4. Once a minimum of four data points have been measured, the noise figure equation shown below was solved yielding all four defining noise parameters.

$$F = F_m + r_n/g_s \left[(g_s-g_o)^2 + (b_s-b_o)^2 \right]$$

where:

F_m is the minimum device noise figure

r_n is the device noise resistance

g_o and b_o are the optimum matching impedance to obtain F_m

g_s and b_s are the source impedance presented to the device.

However, a much better fit was obtained by continuing these measurements until all stub lengths were connected (one at a time), and then performing a least squares best fit (LSBF) algorithm on the data to fit the noise figure equation. This method reduces most of the measurement error and allows an accurate LNA design to be performed. By expanding the noise figure equation above and regrouping the terms, a matrix problem can be set up to perform the LSBF as follows:

$$F_i = a_iX + b_iY + c_iZ + d_iT$$

where:

$a = 1$ $\qquad X = F_m - 2rng_o$

$b = g_s + b_s^2/g_s$ $\qquad Y = r_n$

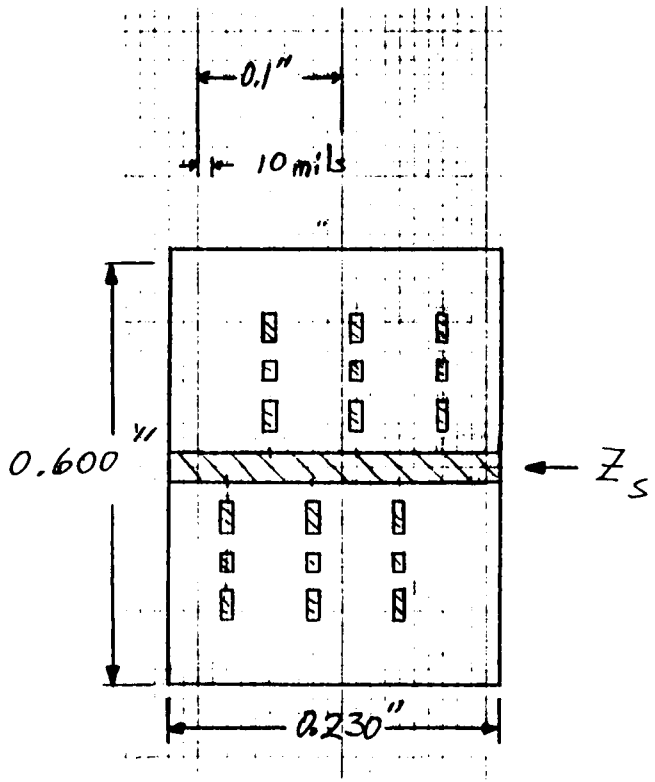
$c = 1/g_s$ $\qquad Z = r_n(g_o^2 + b_o^2)$

$d = b_s/g_s$ $\qquad T = -2r_nb_o$

(a_i through d_i represent the ith values of a through d determined from the ith source impedance presented to the device under test)

Then, the following matrix is solved for a LSBF of the solution vector to the measured noise figures obtained with various source impedances presented to the device under test.

Input Circuit



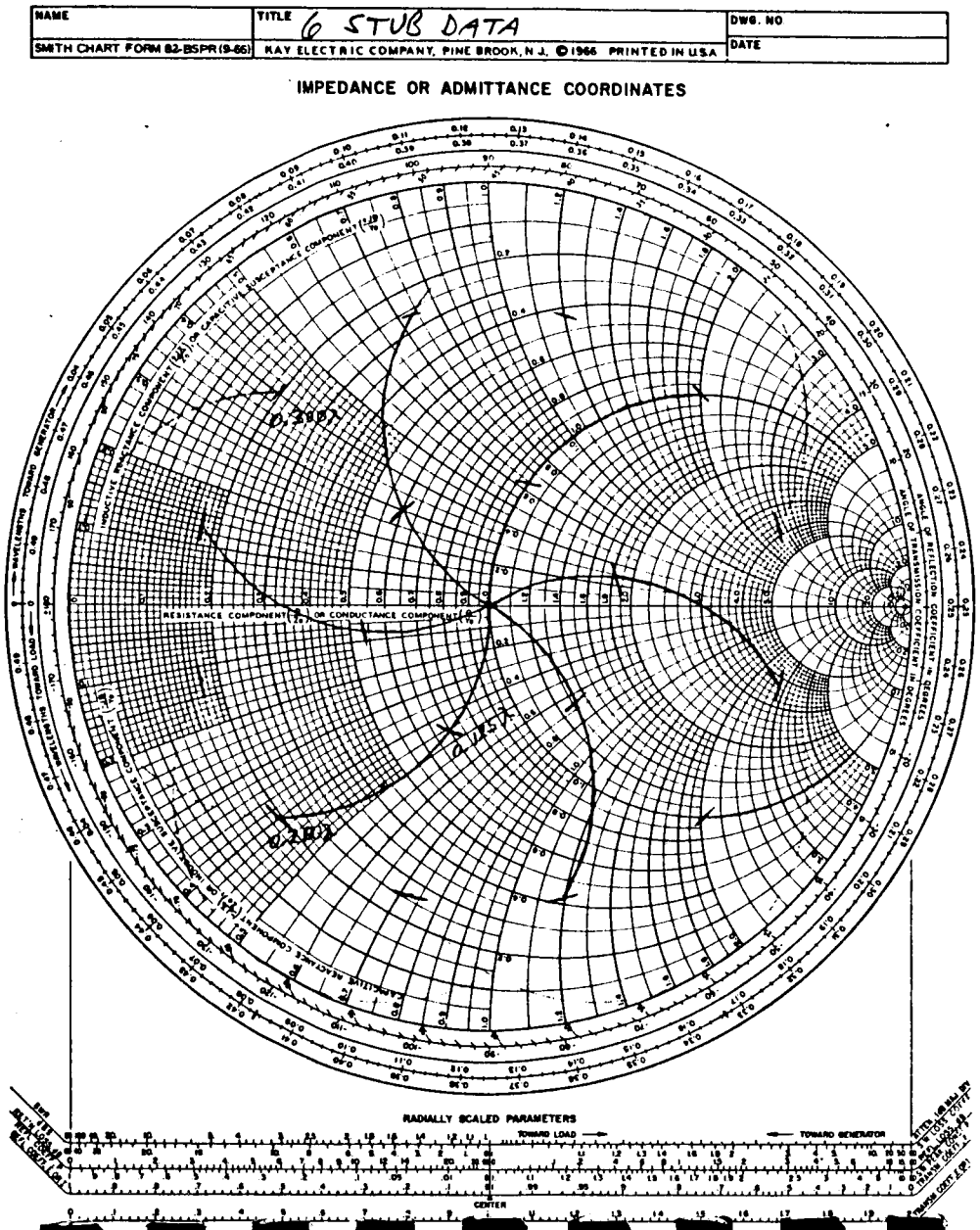
$$F = F_{min} + \frac{r_n}{g_s}\left[(g_s - g_o)^2 + (b_s - b_o)^2\right]$$

Noise Figure Equation

Input Matching to Calculate Noise Parameters

FIGURE 2-4

Input Circuit Source Impedance



$$
\begin{array}{lcl}
F_1 & & a_1\ b_1\ c_1\ d_1 \quad X \\
F_2 & & a_2\ b_2\ c_2\ d_2 \quad Y \\
\cdot & = & \cdot\ \cdot\ \cdot\ \cdot \quad Z \\
\cdot & & \cdot\ \cdot\ \cdot\ \cdot \quad T \\
\cdot & & \cdot\ \cdot\ \cdot\ \cdot \quad | \\
F_m & & a_m\ b_m\ c_m\ d_m \quad |
\end{array}
$$

| | Solution Vector

| Independent Variables

Dependent Variables

where:

$r_n = Y$

$b_o = -T/(2Y)$

$g_o = (4YZ - T^2)^{1/2}/(2Y)$

$F_m = X + (4YZ - T^2)^{1/2}$

One caution in using this approach is to ensure the model of the source impedance circuit is accurate. The computer prediction (Super-Compact software in this case) of source impedance is the value used - not a measurement of Zs. Super-Compact's model was sufficiently accurate as the breadboard data in following paragraphs indicate. Another potential problem area is FET bonding. For devices as small as these HEMTs, only thermal compression bonding should be used. The use of ultrasonic bonding can and will induce small micro-cracks in the FET structure. Figure 2-5 lists the LNA design as recorded in the Super-Compact program listing and shows the input/output substrate layouts.

A three stage breadboard LNA was designed, fabricated, and tested. Figure 2-6 shows the LI'A breadboard as built in the waveguide test fixture with the end piece covers removed, revealing the waveguide to microstrip transitions. Figure 2-7 details the LNA gain and noise figure measurement points. Note that a waveguide circulator is included in the data as one will be included in the final receiver. Also, only one waveguide to microstrip transition has been included because there will be

BREADBOARD LNA IN TEST FIXTURE

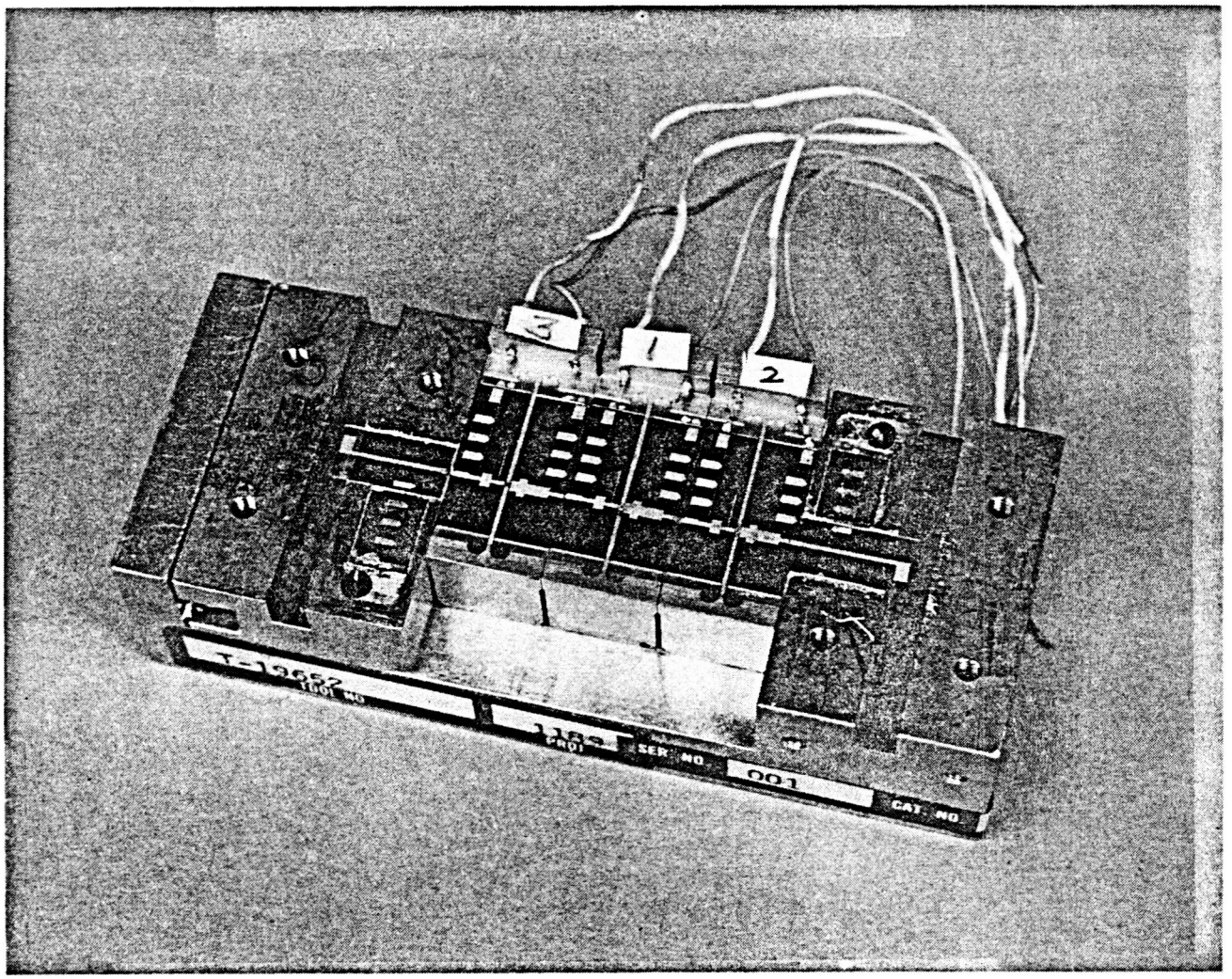


FIGURE 2-6

```
PT:230MIL
PB:131MIL
W1:?51.838MIL?                                    LNA DESIGN
W2:?38.01MIL?
P1:?99.542MIL?
P2:?30.403MIL?
P3:?45.692MIL?
BLK
JUMP 1 2 W=.7MIL T=.7MIL L=15MIL H=10MIL
JUMP 1 2 W=.7MIL T=.7MIL L=15MIL H=10MIL
JUMP 1 2 W=.7MIL T=.7MIL L=15MIL H=10MIL
JUMP 1 2 W=.7MIL T=.7MIL L=15MIL H=10MIL
JUM: 2POR 1 2
END
BLK
TRL 12 11 W=20.91MIL P=(PT-P1-P2-W2) SUB
TRL 11 1 W=W1 P=P1 SUB
TRL 1 3 W=?87.702MIL? P=W2 SUB
TRL 3 4 W=W1 P=P2 SUB
JUM 4 5
IN: 2POR 12 5
END
BLK
JUM 3 4
TRL 4 5  W=20.91MIL P=32.5MIL SUB
TRL 5 6 W=20.91MIL P=2.5MIL SUB
OST 5 W=5MIL P=?158.57MIL? SUB
TRL 6 9 W=19MIL P=24MIL SUB
TRL 9 11 W=?63.667MIL? P=P3 SUB
TRL 11 12 W=20.91MIL P=(PB-P3) SUB
IND 12 13 L=.003NH
CAP 13 14 C=10PF
TRL 14 15 W=20.91MIL P=40MIL SUB
OUT: 2POR 3 15
END
NOI
IN 1 2
TWO 2 3 Q1
OUT 3 4
IN 4 5
TWO 5 6 Q1
OUT 6 7
AMP: 2POR 1 7
END
FREQ
STEP 17.7GHZ 19.2GHZ .5GHZ
STEP 19.3GHZ 20.2GHZ .1GHZ
END
OUT
PRI AMP S
END
OPT
AMP
+ F=17.7GHZ 20.2GHZ MS22=0 MS21=13.0DB GT
```

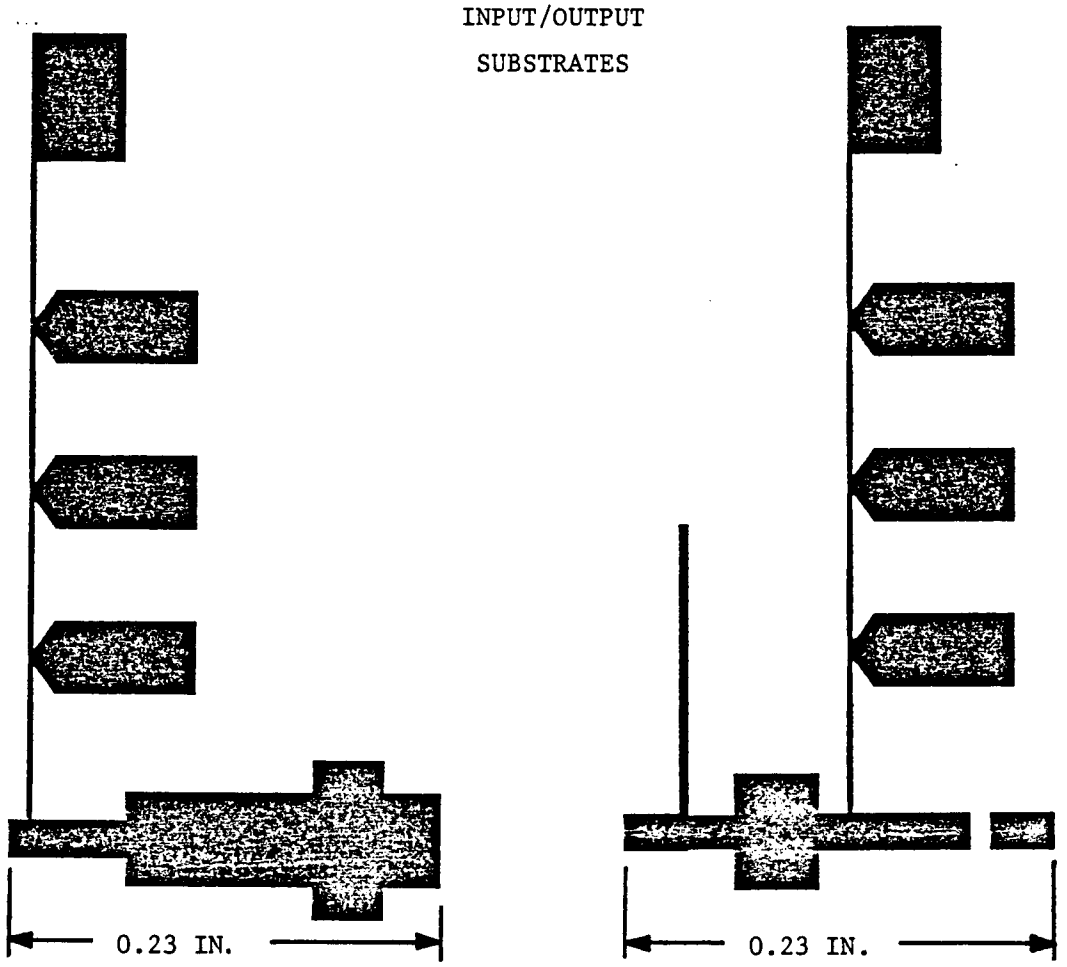
FIGURE 2-5

LNA DESIGN

```
+ F=19.3GHZ 20.1GHZ NF=2.3DB LT W=4
END
DATA
SUB: MS ER=3.82 H=10MIL MET1=CR 1UM MET2=AU .2MIL
Q1:S
17.5GHZ .738 -157.1 1.511 54.1 .078 25.3 .601 -68.3
18.0GHZ 0.737 -159.3   1.480   51.9   0.078   26.0   0.599  -70.2
18.5GHZ 0.736 -161.5   1.450   49.8   0.077   26.9   0.597  -72.0
19.0GHZ 0.735 -163.6   1.422   47.7   0.077   28.0   0.595  -73.9
19.5GHZ 0.734 -165.7   1.393   45.6   0.076   29.2   0.593  -75.8
20.0GHZ 0.734 -167.8   1.366   43.5   0.076   30.5   0.591  -77.7
20.5GHZ 0.734 -169.9   1.341   41.4   0.076   31.9   0.590  -79.7
NOI RN
17.5GHZ 1.70 .343 112.35 3
18.0GHZ  1.70 .343 112.35 3
18.5GHZ  1.75 .380 108.73 3
19.0GHZ  1.80 .332 132.26 3
19.5GHZ  1.85 .276 136.71 3.5
20.0GHZ  1.90 .300 152.33 3.5
20.5GHZ  1.95 .344 156.61 3.5
END
```

FIGURE 2-5 CONT.

LNA STAGE
INPUT/OUTPUT
SUBSTRATES



INPUT MATCH

OUTPUT MATCH

FIGURE 2-5 CONT.

NASA LNA BREADBOARD TEST DATA

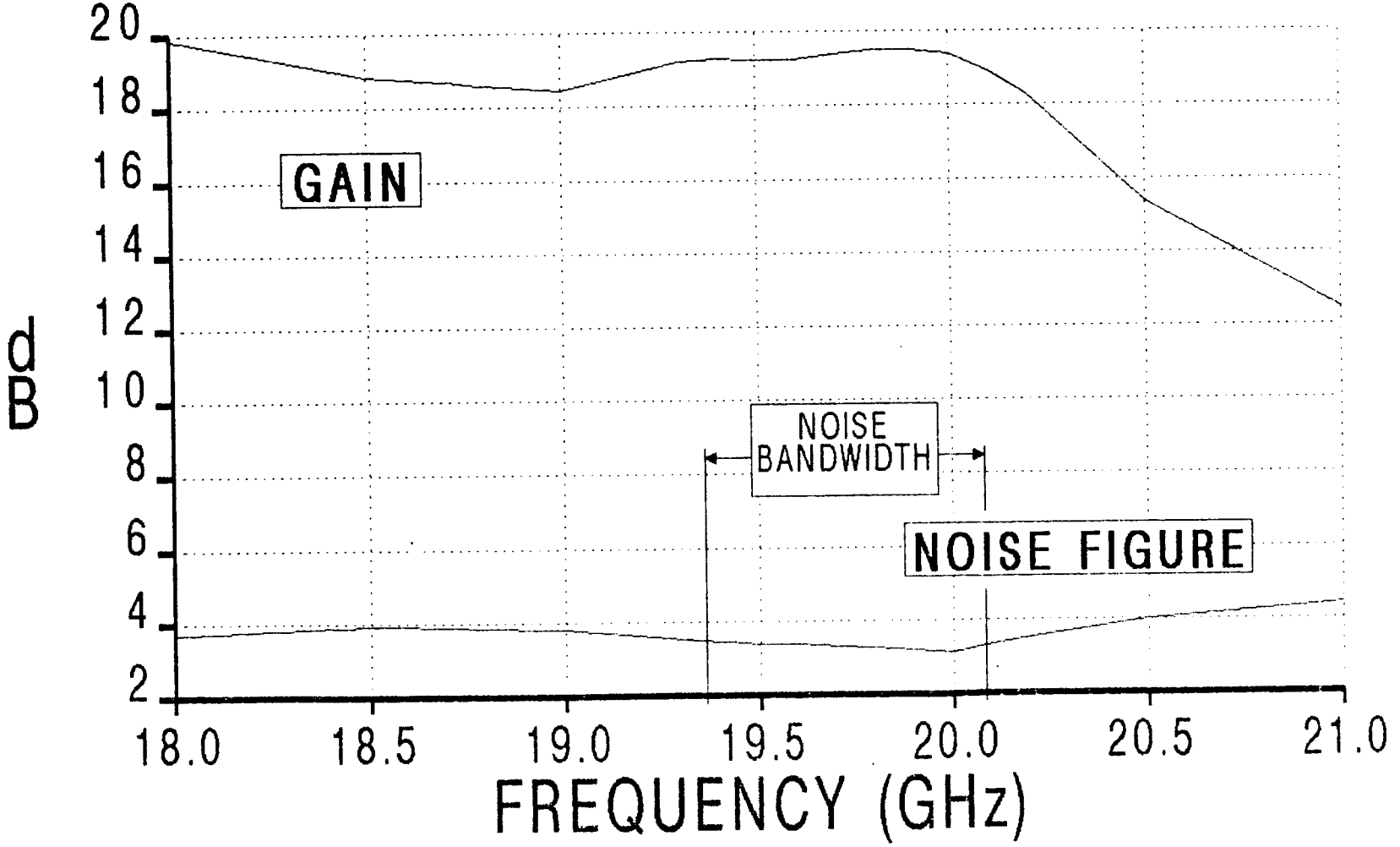


FIGURE 2-7

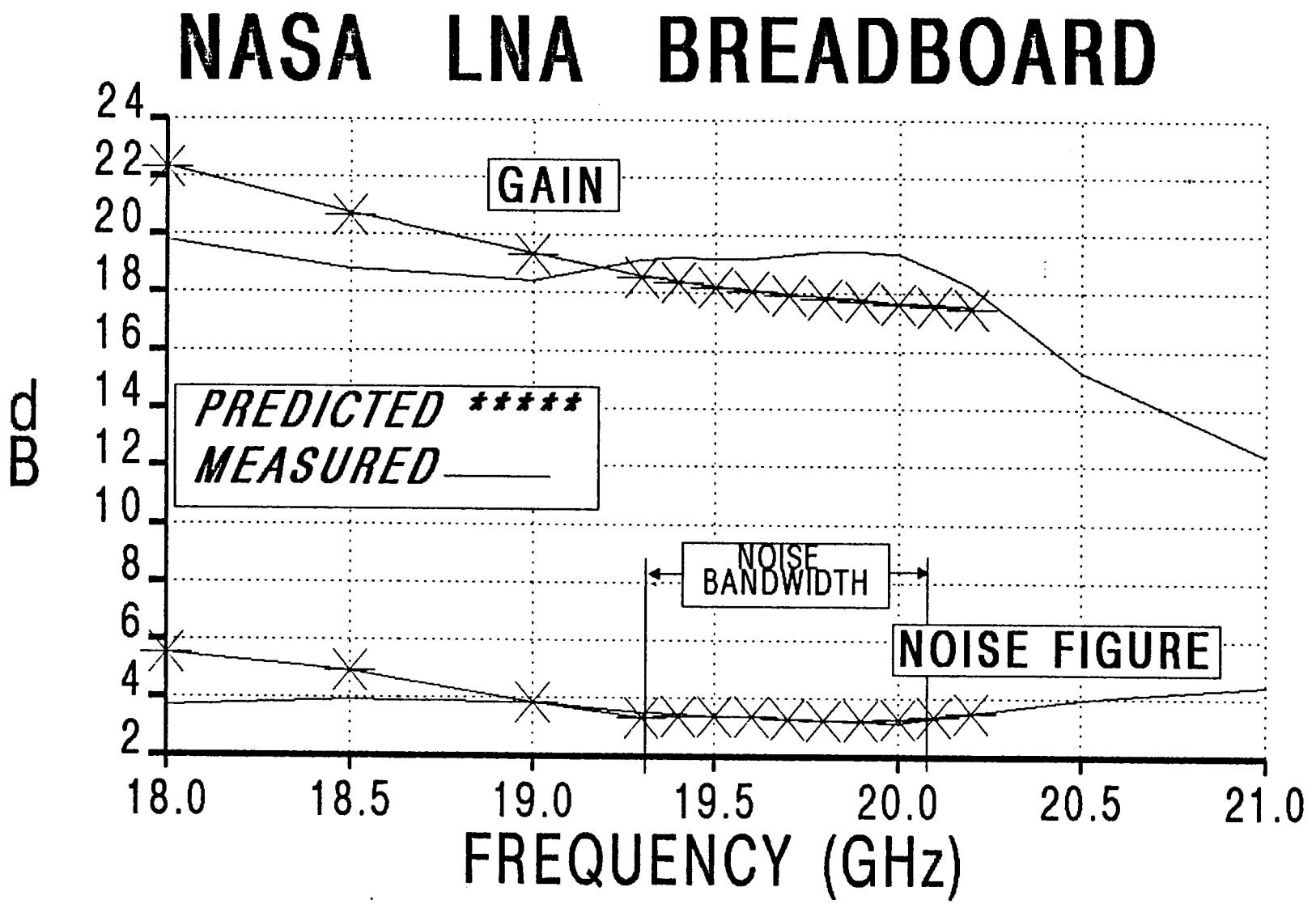

NASA LNA BREADBOARD
GAIN
PREDICTED *****
MEASURED
NOISE BANDWIDTH
NOISE FIGURE
dB
24
22
20
18
16
14
12
10
8
6
4
2
18.0
18.5
19.0
19.5
20.0
20.5
21.0
FREQUENCY (GHz)

FIGURE 2-8

only one transition in the LNA portion of the receiver. However, the insertion loss of the receiver's transition will be lower (by 0.1 to 0.2 dB due to a shorter microstrip portion than in the test fixture. Figure 2-8 compares the measured results of the breadboard to predicted performance at room temperature. Excellent agreement was obtained for noise figure over the noise bandwidth which covers the two NASA carriers while the gain slightly exceeded prediction over the same band. These results give a high degree of credibility to the noise parameter characterization procedure as described above.

After the LNA breadboard testing was completed and while we were waiting for additional Gould HEMT FETs to be received for the final receiver design, Gould informed us that they could no longer make these devices (or would not be able to deliver devices measuring up to the above demonstrated performance level for many months to come). As a result Harris again performed an industry survey of existing, available FETs. However, this time (more than one year after our first survey) several HEMT FET manufacturers were selling devices.

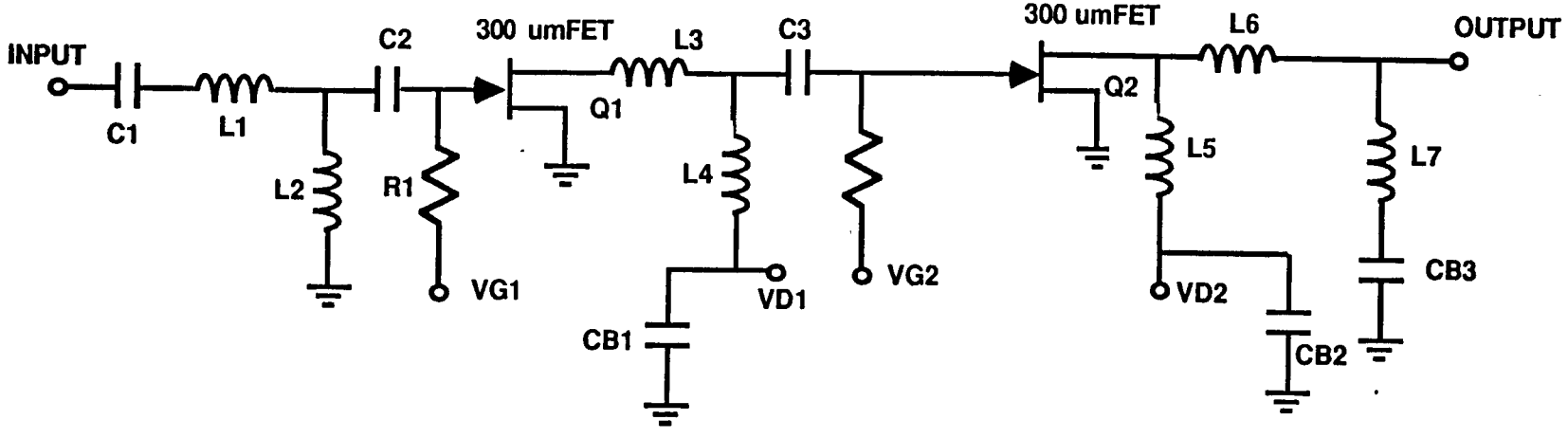
Harris has selected the NEC HEMT FET (NE 202) as the replacement for the Gould device. This new HEMT has both higher gain and lower noise figure than the Gould HEMT. It is available from stock and comes with a complete set of S and noise parameters through 30 GHz. Therefore, the long detailed process of noise parameter characterization will not have to be repeated for this FET, and an LNA with superior performance to that shown above will be delivered. The predicted LNA and receiver performance with this new HEMT FET is detailed at the end of this report.

3.0 MMIC RF AMPLIFIER

The RFA testing was completed with very good results obtained. A single-ended design was fabricated for NASA, and a balanced design was fabricated on our internal IR&D program which shared the same wafer. Figure 3-1 is a schematic of the single ended version and Figure 3-2 is a picture of the balanced amplifier. Figure 3-3 contains the Touchstone circuit file for the single-ended design. Both amplifier types exhibit the same gain response and reverse isolation qualities, however, the balanced amplifier shows a significant improvement in VSWR over the single ended design. VSWRs of 2.0:1 to 3.0:1 were encountered for the single-ended RFA where the balanced RFA did not exceed 1.4:1 on most amplifiers. Because of this improvement in VSWR performance, the balanced RFA has become the baseline MMIC amplifier.

NASA 17.7 TO 20.2 GHz AMP

(1/2 MICRON MMIC)



- o DESIGNED FOR 50% IDSS
- o MEASURED OUTPUT 1 dB COMPRESSION POINT OF 24 dBm FOR BALANCED CONFIGURATION
- o SPURS MEASURED $<$ -52 dBc (BELOW NOISE FLOOR)

FIGURE 3-1

BALANCED 20 GHz RF AMPLIFIER

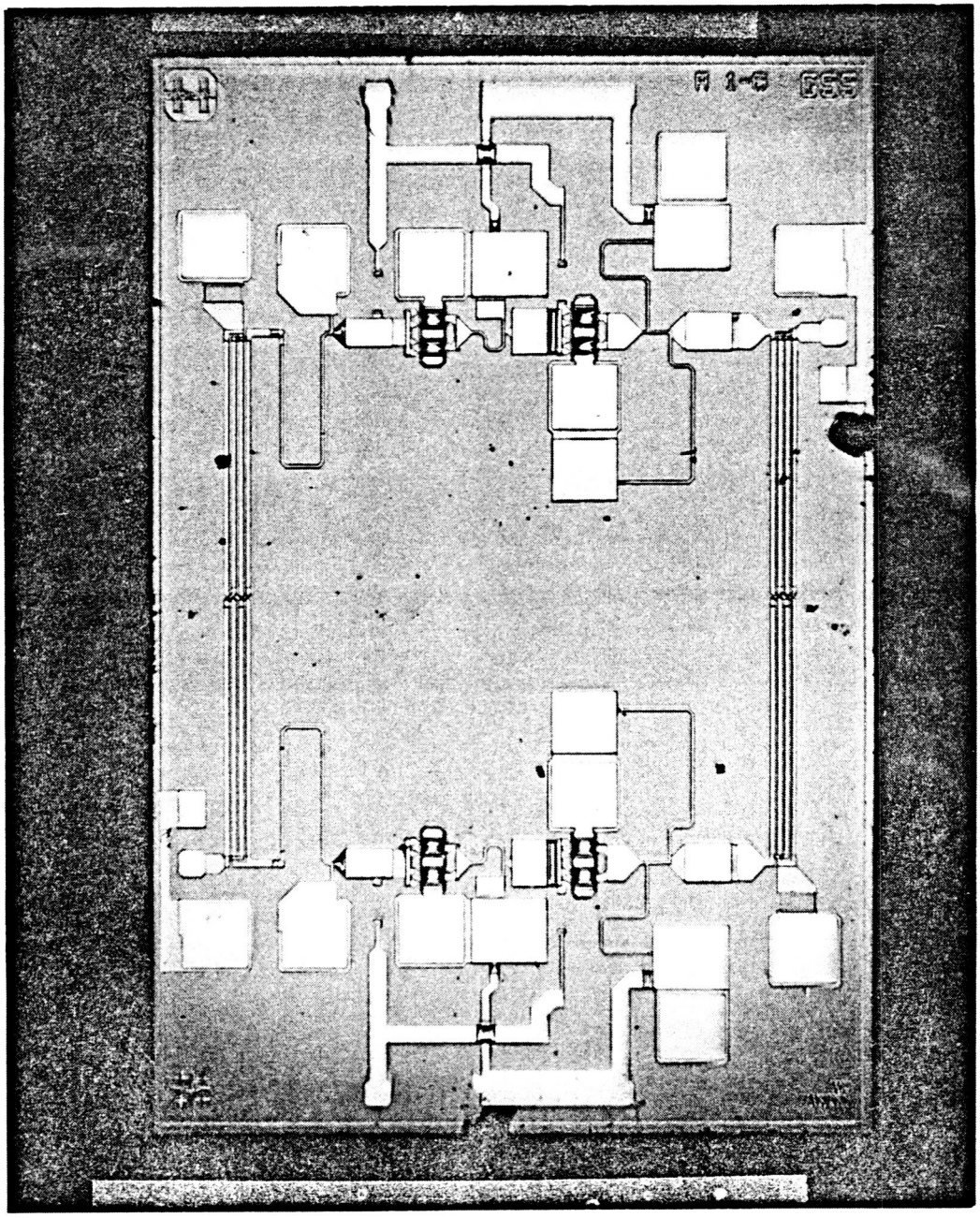


FIGURE 3-2

TOUCHSTONE CIRCUIT FILE FOR MMIC RFA

```
var
        x1=1.0
        x2=1.0
        c11 = 0.051
        c22 = 2.7
        c33 = 3.3
        h11 = 127
        x=.0001
eqn
        c1=c11*x1
        c2=c22*x1
        c3=c33*x1
        h1=h11*x2
!define dimensions to be used these override system default values
!this should take care of different system defaults that
!other people may have used on their TOUCHSTONE software
dim
        freq    ghz
        res     oh
        cond    /oh
        ind     nh
        cap     pf
        lng     um
        time    ps
        ang     deg
!define circuit configuration of amplifier
ckt
        msub er=12.5 h^h1 t=3.2 rho=1 rgh=.0001
        tand tand^x
!HOLE model - VIA MODEL BUT MUST CALL IT HOLE SINCE THERE IS AN ELEMENT
!IN TOUCHSTONE CALLED VIA
        mlin 1 2 w=200 l=100
        ind 2 0 l=.015
        mlef 2 w=200 l=100
        DEF1P 1 HOLE
!input/output for circuit
        wire 1 2 d=25.4 l=381 rho=1
        wire 1 2 d=25.4 l=381 rho=1
        mlin 2 3 w=75 l=37.5
        mlef 2 w=75 l=37.5
        def2p 1 3 IO
!8.6pf abrupt connection bypass capacitor
        mlin 1 3 w=150 l=200
        cap 3 4 c=8.6
        ribbon 4 5 w=200 l=10 rho=1
        HOLE 5
        def1p 1 bycap
!amplifier circuit layout
        io 1 2
        cap 2 3 c^c1
        ind 3 5 l=.007
        mlin 5 6 w=12 l=10
        mlin 6 7 w=8 l=855
        mlin 7 45 w=8 l=45
```

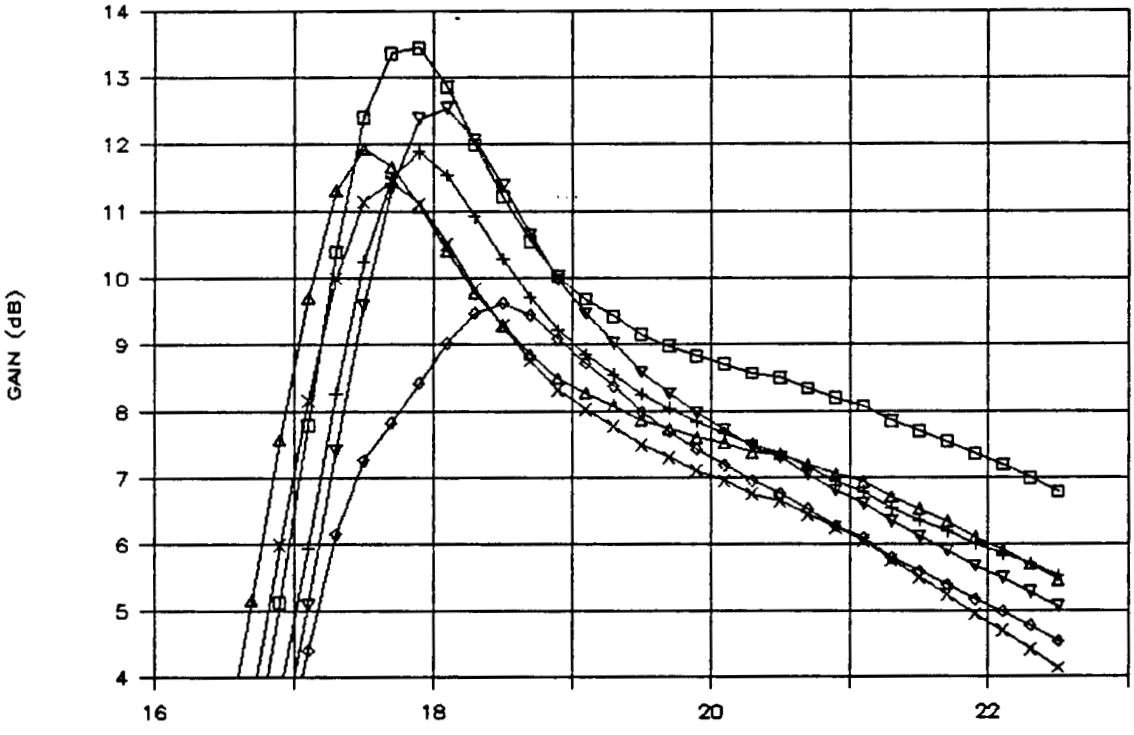
FIGURE 3-3

MMIC RFA CIRCUIT FILE
CONTINUED

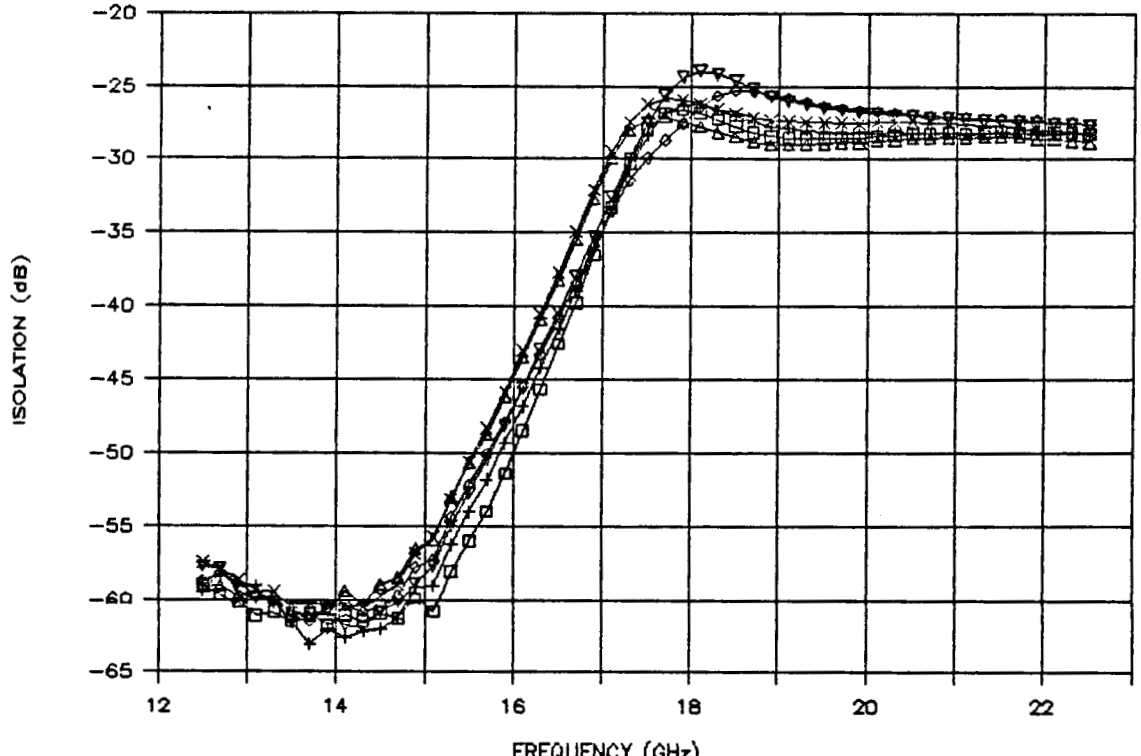
```
        HOLE 45
        cap 7 9 c^c2
        ind 9 10 l=.007
        mlin 10 12 w=77 l=95
        res 12 0 r=5000
        mlin 12 13 w=77 l=50
        s2pa 13 14 0 A:ASD300H.S2P      ! GASD MEAS. S-PARs BY D. COOK O
        mlin 14 15 w=8 l=200
        mlin 15 50 w=8 l=25
        MLIN 50 46 W=75 L=75
        bycap 46
        mlin 15 16 w=12 l=12.5
        cap 16 18 c^c3
        ind 18 19 l=.007
        mlin 19 20 w=95 l=100
        res 20 0 r=5000
        mlin 20 21 w=100 l=22
        s2pa 21 22 0
        mlin 22 23 w=100 l=50
        mlin 23 47 w=8 l=500
        bycap 47
        mlin 23 24 w=8 l=85
        mlin 24 48 w=8 l=700
        bycap 48
        mlin 24 41 w=100 l=325
        io 41 43
        def2p 1 43 amp
!define output block
out
        amp db[s21] gr1
        amp db[s11] gr2
        amp db[s22] gr3
!define frequencies to sweep circuit over
freq
        sweep 17.7 21.2 .5
!define limits of vertical axes on grid outputs
grid
        range 17.7 21.2 .5
        gr1 0 15 3
        gr2 -30 0 5
        gr3 -30 0 5
!define optimization variables and goals
opt
        range 17.7 21.2
        amp DB[s11] < -10 20
        amp DB[s22] < -10 20
        amp db[s21] > 11 20
        amp db[s21] < 11.5 20
 ! END NASAAMPF.CKT  26 AUGUST 1986 - CHRIS RICE
```

FIGURE 3-3 CONT.

BALANCED AMPLIFIER'S GAIN



BALANCED AMPLIFIER'S REVERSE ISOLATION



□ 84-6 + C8-1 ◇ D9-1 △ A9-6 X D5-4 ▽ D5-7

FIGURE 3-4, 3-5

The RF yield of the balanced amplifiers was found to be in excess of 25% on all three wafers fabricated. All amplifiers from the first wafer probed show a good grouping of performance data as shown in Figures 3-4 and 3-5. The second and third wafers have been probed giving similar mean values for the amplifier to those obtained off the first wafer. Also, we have probed the individual diagnostic FETs and analyzed the amplifier's performance with this data only inserted into the model. Very good agreement was shown between measured data and predicted performance under these conditions as shown in Figure 3-6 for the single-ended RFA from the first wafer. Figure 3-7 gives the balanced amplifier's noise figure versus bias for one MMIC balanced amplifier.

Figures 3-8 and 3-9 show the mean values of the balanced amplifiers from the first wafer as a function of the bias level. The gain graph shows that the gain peak moves in frequency as the bias is changed from a low of approximately 17 GHz at 100% IDSS to a high of approximately 18.75 GHz at 25% IDSS. All other parameters (isolation, input VSWR and output VSWR) remain good as bias is changed. This means that even though there is a significant peak in the gain response, it can be moved to lessen its impact on the overall receiver performance. The table below gives the input and output reflection coefficients at the different bias points for the single-ended RFA which is used within the balanced amplifier.

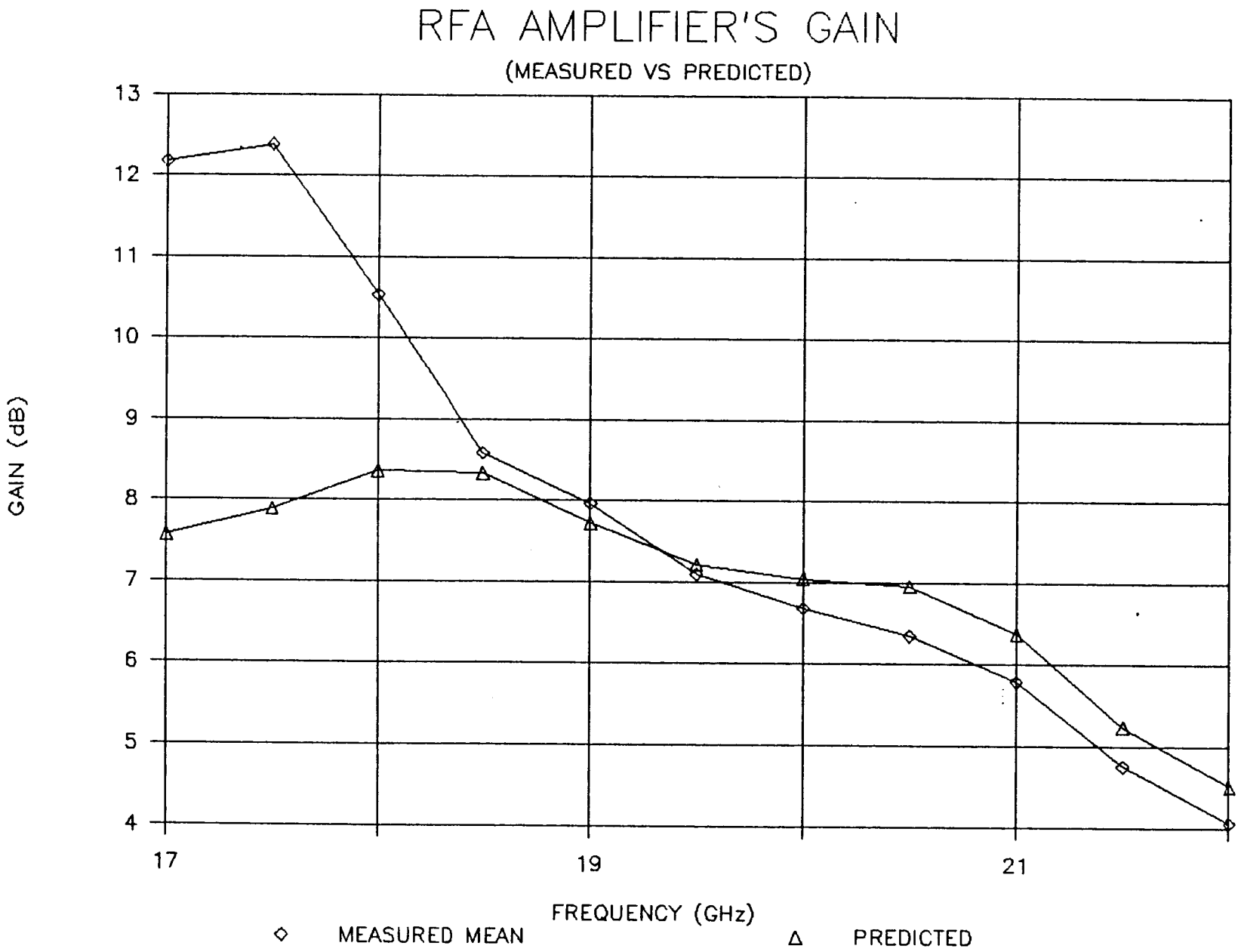

RFA AMPLIFIER'S GAIN
(MEASURED VS PREDICTED)
GAIN (dB)
13
12
11
10
9
8
7
6
5
4
17
19
21
FREQUENCY (GHz)
◇ MEASURED MEAN
Δ PREDICTED

FIGURE 3-6

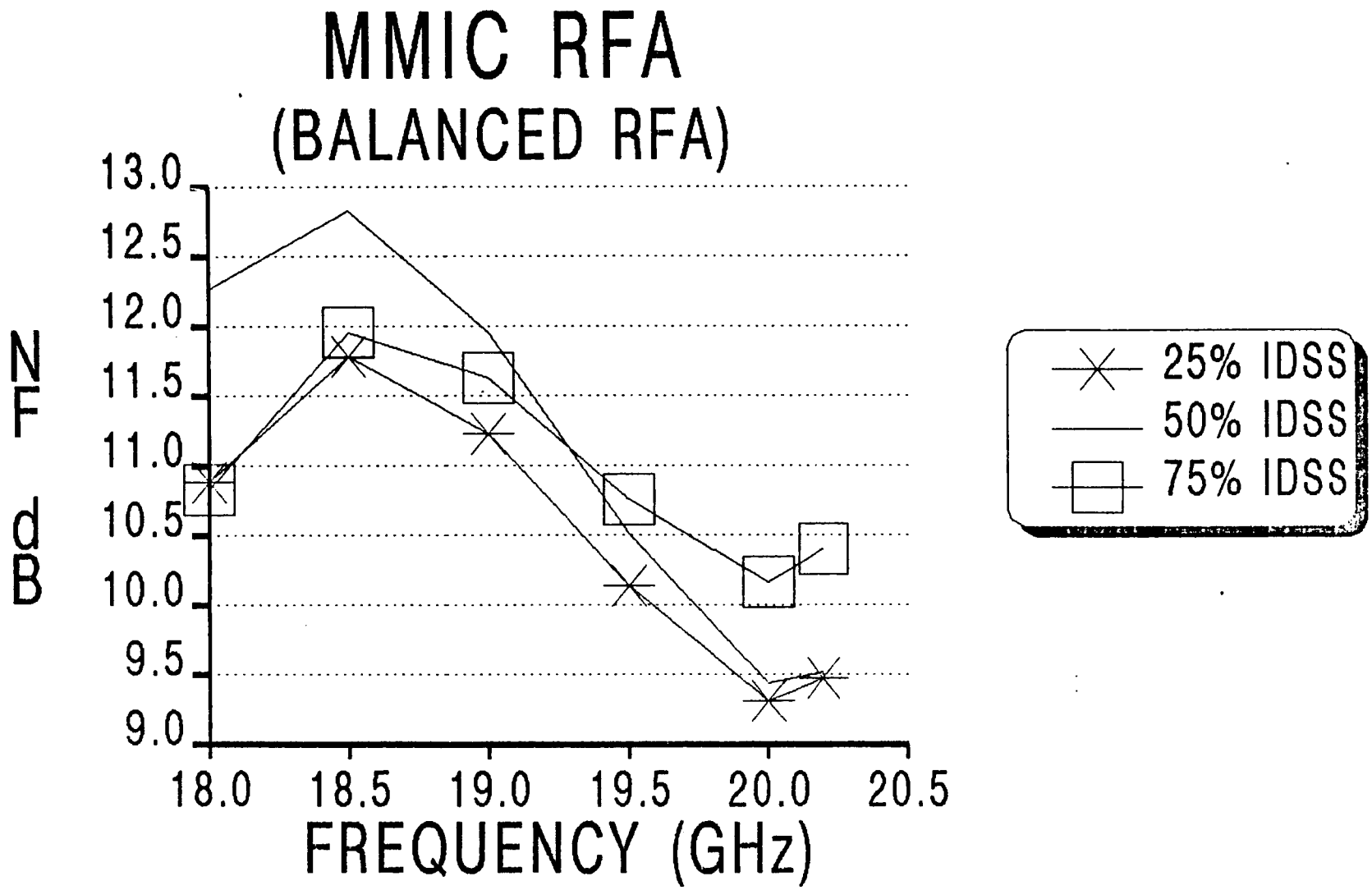
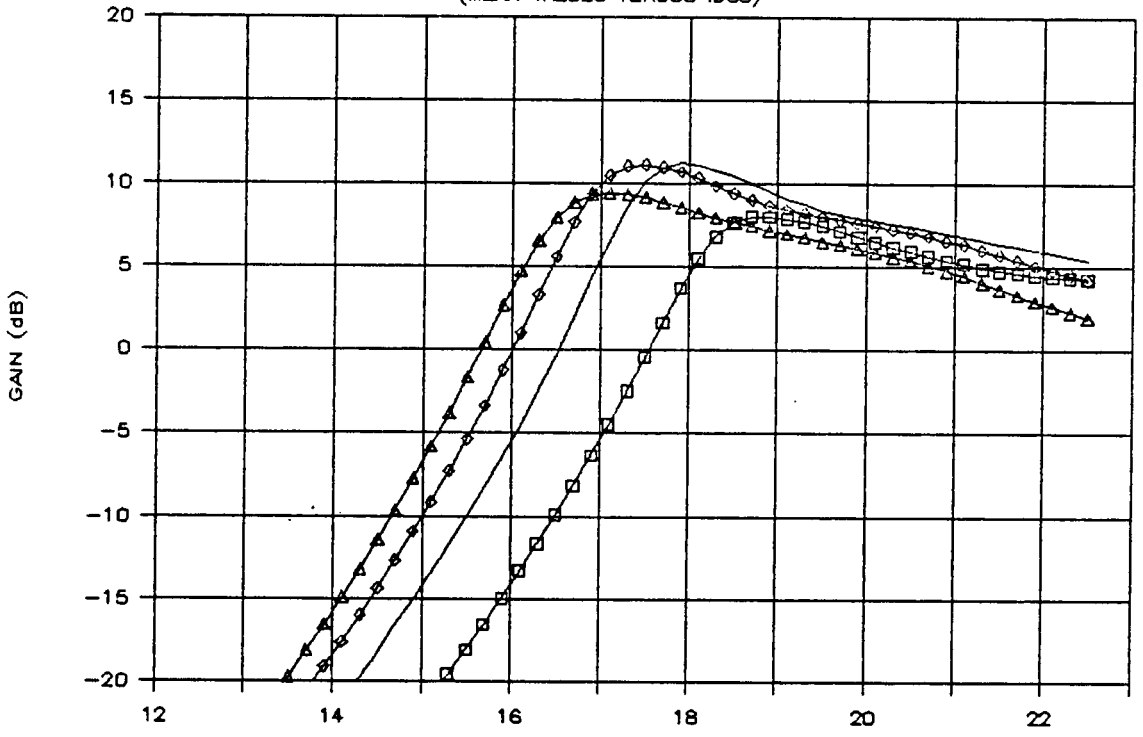

MMIC RFA
(BALANCED RFA)
NF dB
13.0
12.5
12.0
11.5
11.0
10.5
10.0
9.5
9.0
18.0
18.5
19.0
19.5
20.0
20.5
FREQUENCY (GHz)
25% IDSS
50% IDSS
75% IDSS

FIGURE 3-7

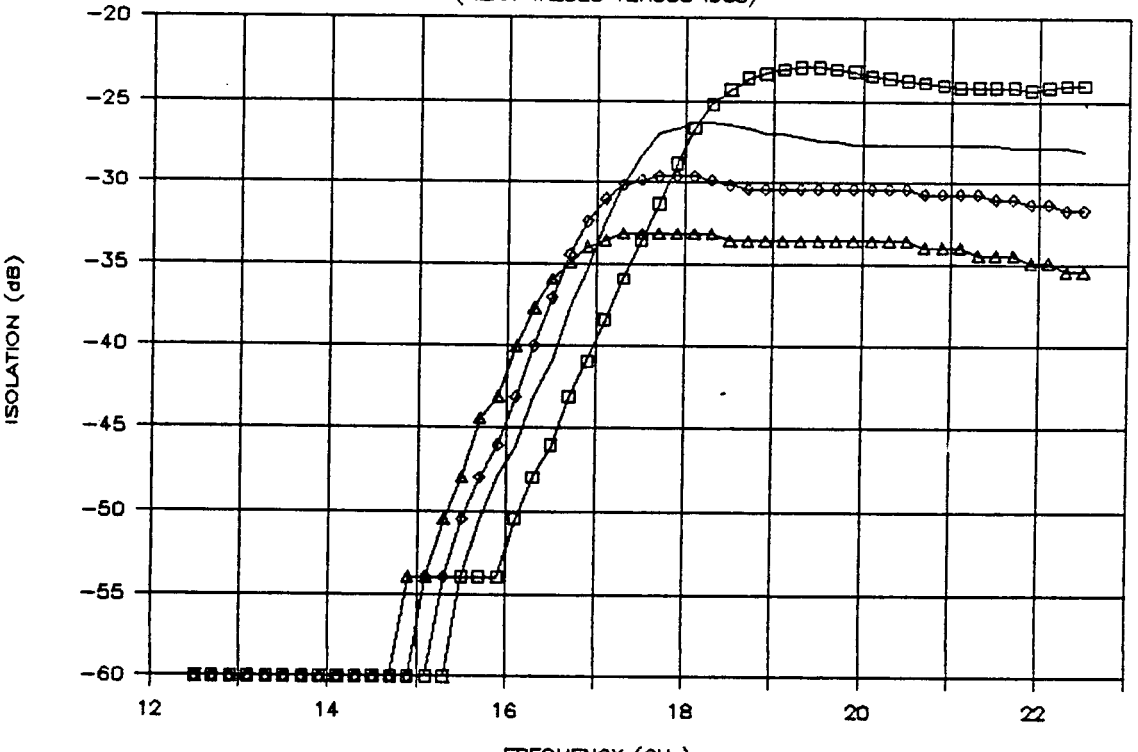
BALANCED AMPLIFIER'S GAIN

(MEAN VALUES VERSUS IDSS)



BALANCED AMPLIFIER'S ISOLATION

(MEAN VALUES VERSUS IDSS)



FIGURES 3-8, 3-9

FREQ (GHz)	IDSS (%)	S11 (NUMERIC)	/_S11 (DEG)	S22 (NUMERIC)	/_S22 (DEG)
17.9	25%	0.355	-152	0.626	246
17.9	50%	0.481	-111	0.252	73
17.9	75%	0.507	-115	0.323	20
17.9	100%	0.509	-114	0.453	8
18.9	25%	0.263	-144	0.261	81
18.9	50%	0.315	-143	0.27	23.3
18.9	75%	0.339	-132	0.275	9.9
18.9	100%	0.39	-126	0.372	4.5
19.9	25%	0.152	-185	0.233	29
19.9	50%	0.19	-152	0.224	20
19.9	75%	0.29	-142	0.24	21
19.9	100%	0.365	-146	0.34	5

4.0 RF BANDPASS FILTER

Test results for the breadboard RF filter show it to be within the allocated specifications on all but the VSWR and insertion loss requirements at the band edges. We believe these out-of-spec areas, which will have only a minor effect on the overall receiver's performance, to be due to the SMA connectors used on the test fixtures. These effects will not be present on the POC receivers.

The breadboard filter designed and fabricated was a five pole Chebychev filter. Figure 4-1 is a picture of the filter in

20 GHz RF BANDPASS FILTER

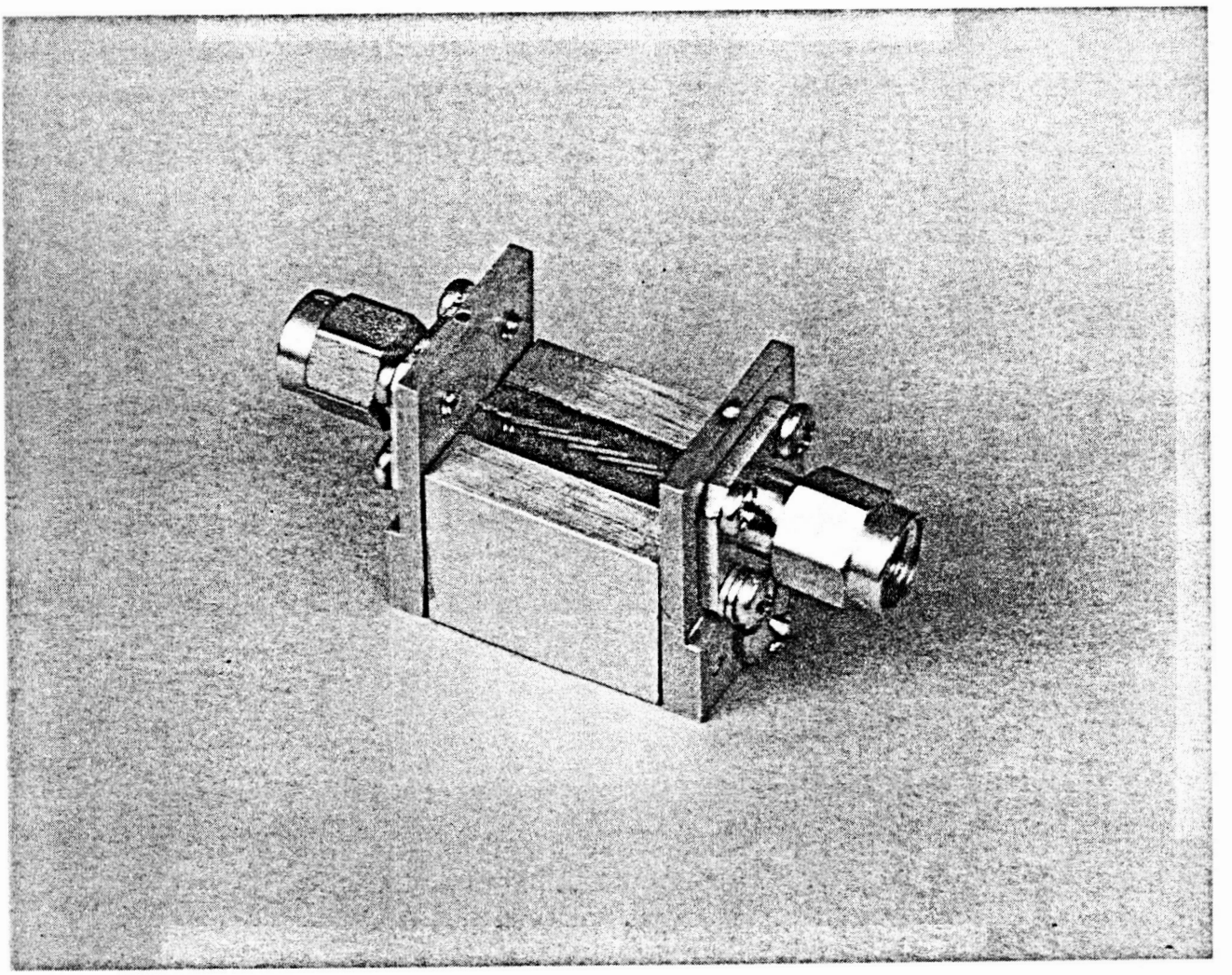


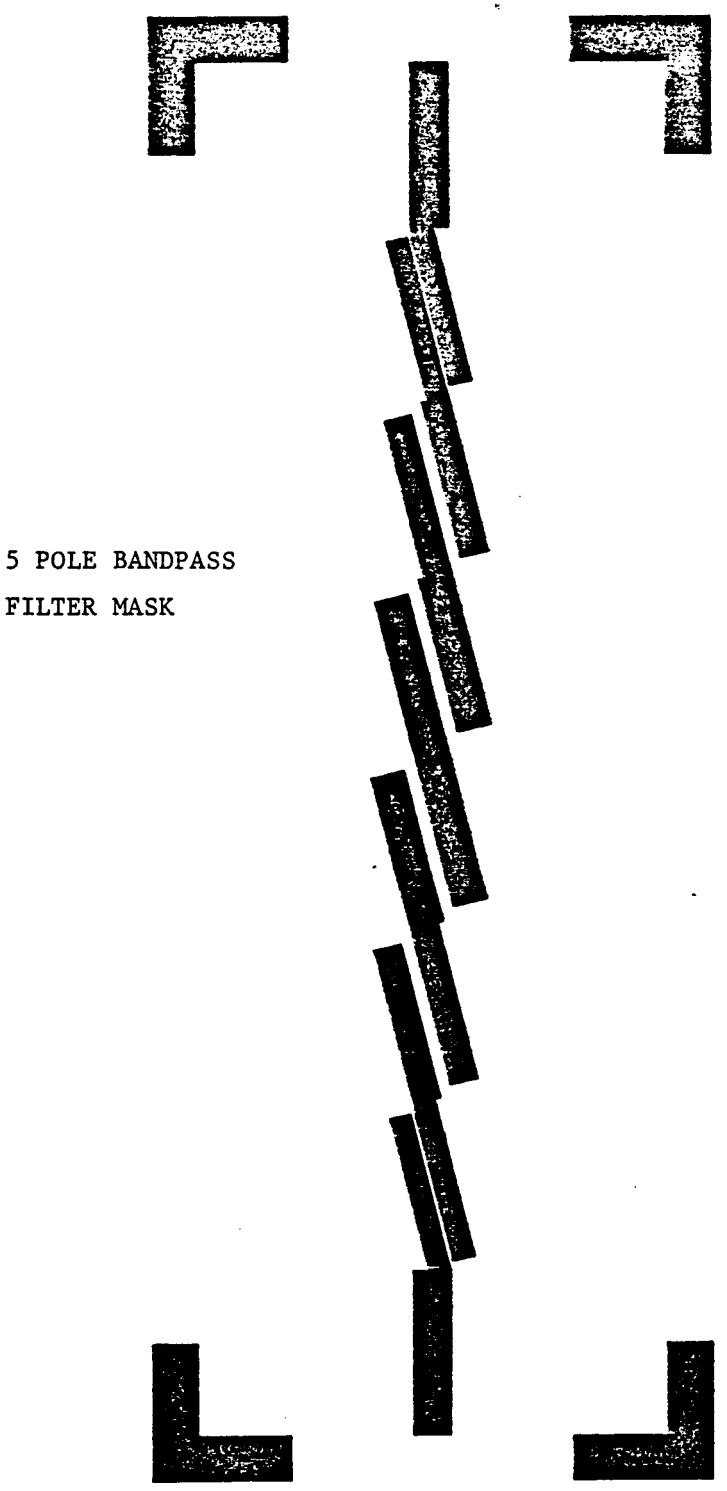
FIGURE 4-1

RF BPF DESIGN

```
**NASA 20 GHZ BPF***
W1:?12.665MIL?
S1:?1.3958MIL?
W2:?16.015MIL?
S2:?5.7093MIL?
W3:?19.153MIL?
S3:?6.2726MIL?
P1:?93.091MIL?
BLK
CPL 1 2 3 4 W=W1 S=S1 P=P1 SUB
CPL 3 5 6 7 W=W2 S=S2 P=P1 SUB
CPL 6 8 9 10 W=W3 S=S3 P=P1 SUB
CPL 9 11 12 13 W=W3 S=S3 P=P1 SUB
CPL 12 14 15 16 W=W2 S=S2 P=P1 SUB
CPL 15 17 18 19 W=W1 S=S1 P=P1 SUB
CAP 2 C=.0001PF
CAP 4 C=.0001PF
CAP 5 C=.0001PF
CAP 7 C=.0001PF
CAP 8 C=.0001PF
CAP 10 C=.0001PF
CAP 11 C=.0001PF
CAP 13 C=.0001PF
CAP 14 C=.0001PF
CAP 16 C=.0001PF
CAP 17 C=.0001PF
CAP 19 C=.0001PF
FLTR: 2POR 1 18
END
FREQ
STEP 13.2GHZ 17.2GHZ .5GHZ  STEP 17.7GHZ 20.2GHZ .25GHZ
STEP 20.7GHZ 23.2GHZ .5GHZ
END
OUT
PRI FLTR S
END
OPT
FLTR F 13.4GHZ MS21 -55DB LT
     F 17.7GHZ 20.GHZ MS21 -1.3DB GT W=300
     F 22.2GHZ MS21 -35DB LT
END
DATA
 SUB:MS H=10MIL ER=3.8 TAND=.0003 MET1=NI 1UM MET2=CR 1UM MET3=AU 15UM
END
```

FIGURE 4-2

RF BPF



5 POLE BANDPASS
FILTER MASK

FIGURE 4-2 CONT.

RF BPF PREDICTED INSERTION LOSS

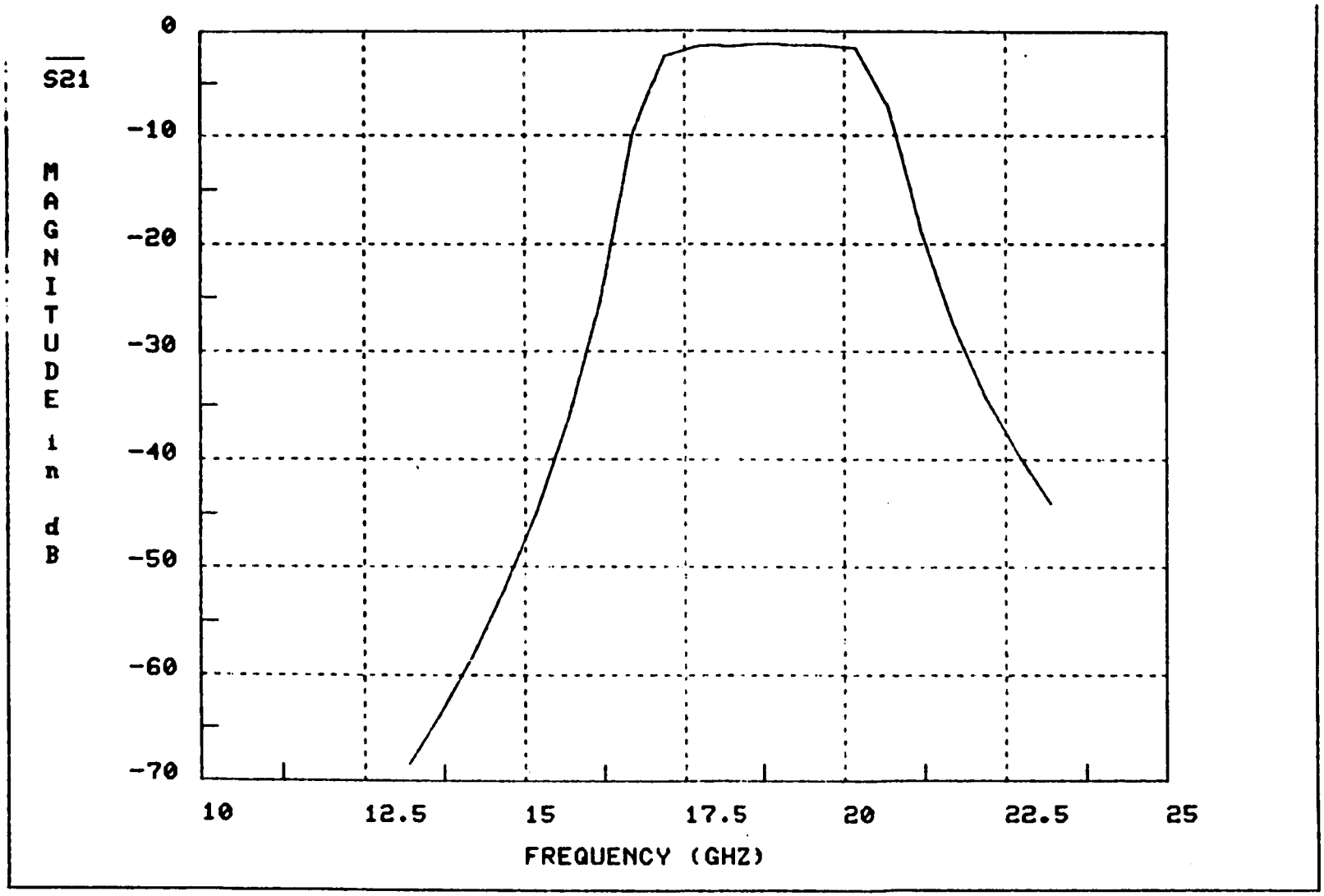
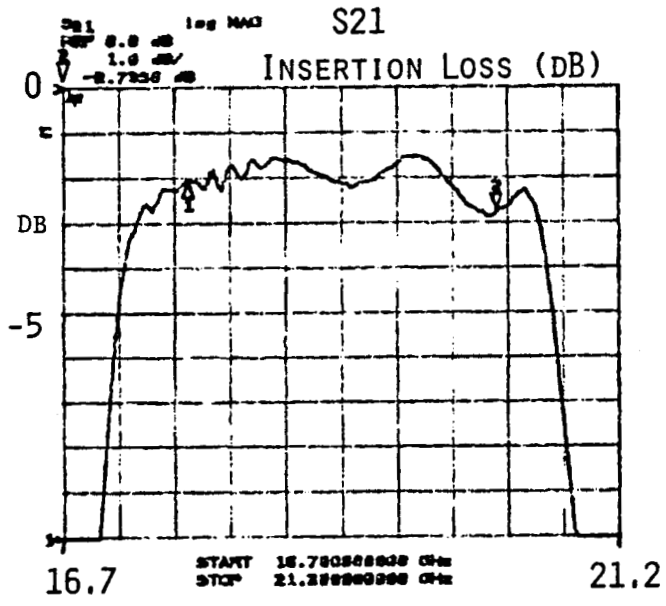
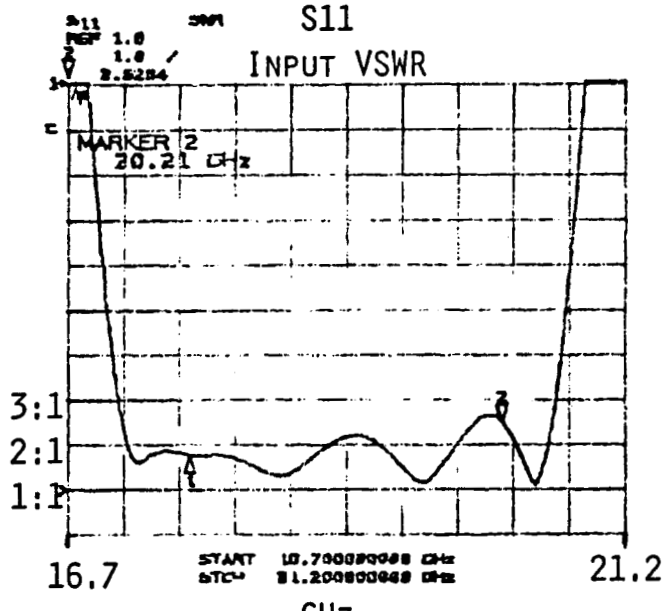
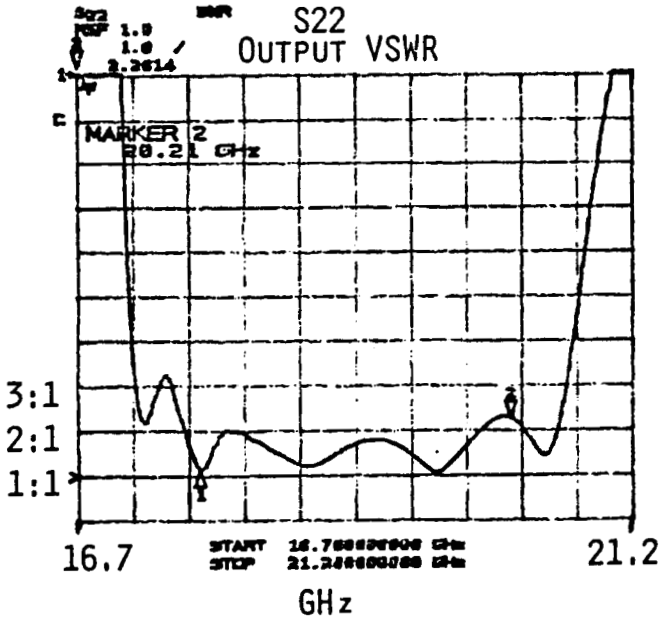


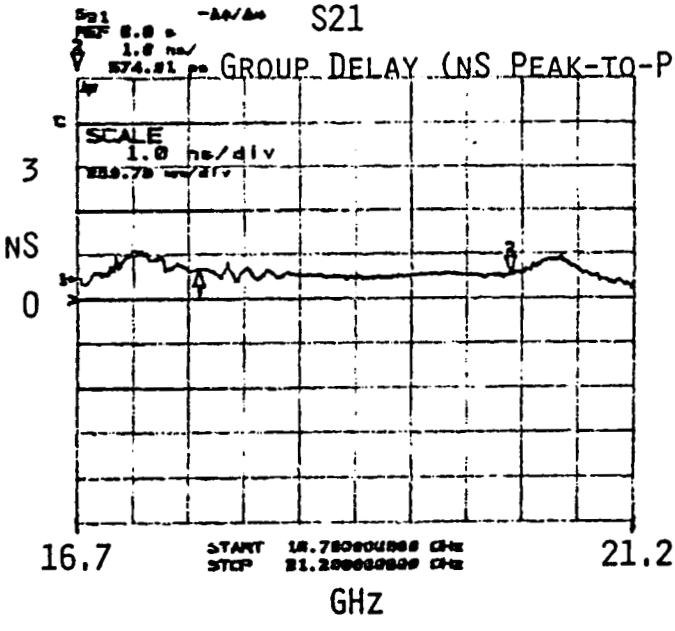
FIGURE 4-4

BREADBOARD RF FILTER W/LID





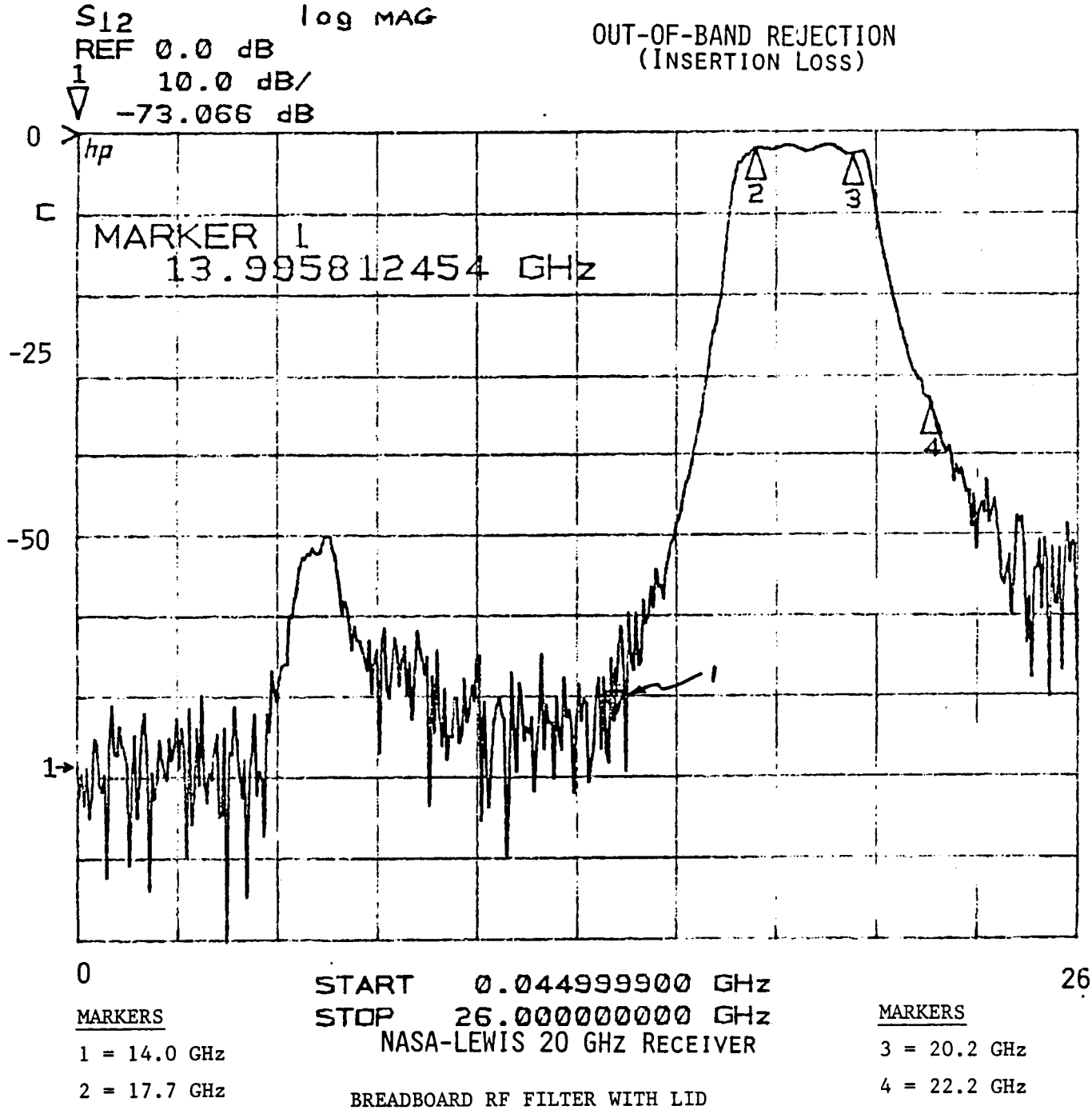




FOR EA. GRAPH
Δ_1=17.7 GHz ∇_2=20.2 GHz

ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE 4-5



MARKERS
1 = 14.0 GHz
2 = 17.7 GHz

MARKERS
3 = 20.2 GHz
4 = 22.2 GHz

FIGURE 4-6

RF BANDPASS FILTER AT 25°C
(IN BAND)

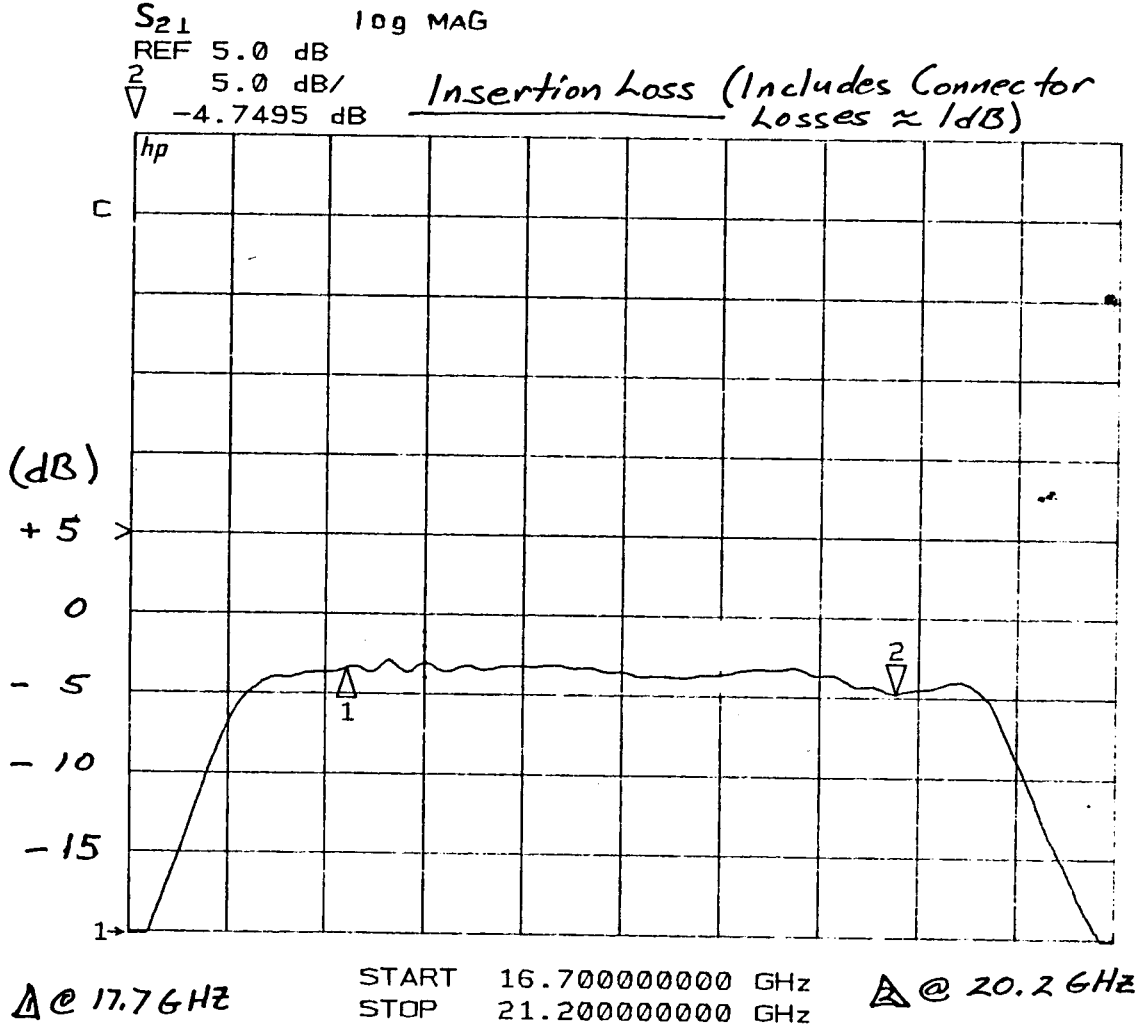


FIGURE 4-7

RF BANDPASS FILTER AT 75°C
(IN BAND)

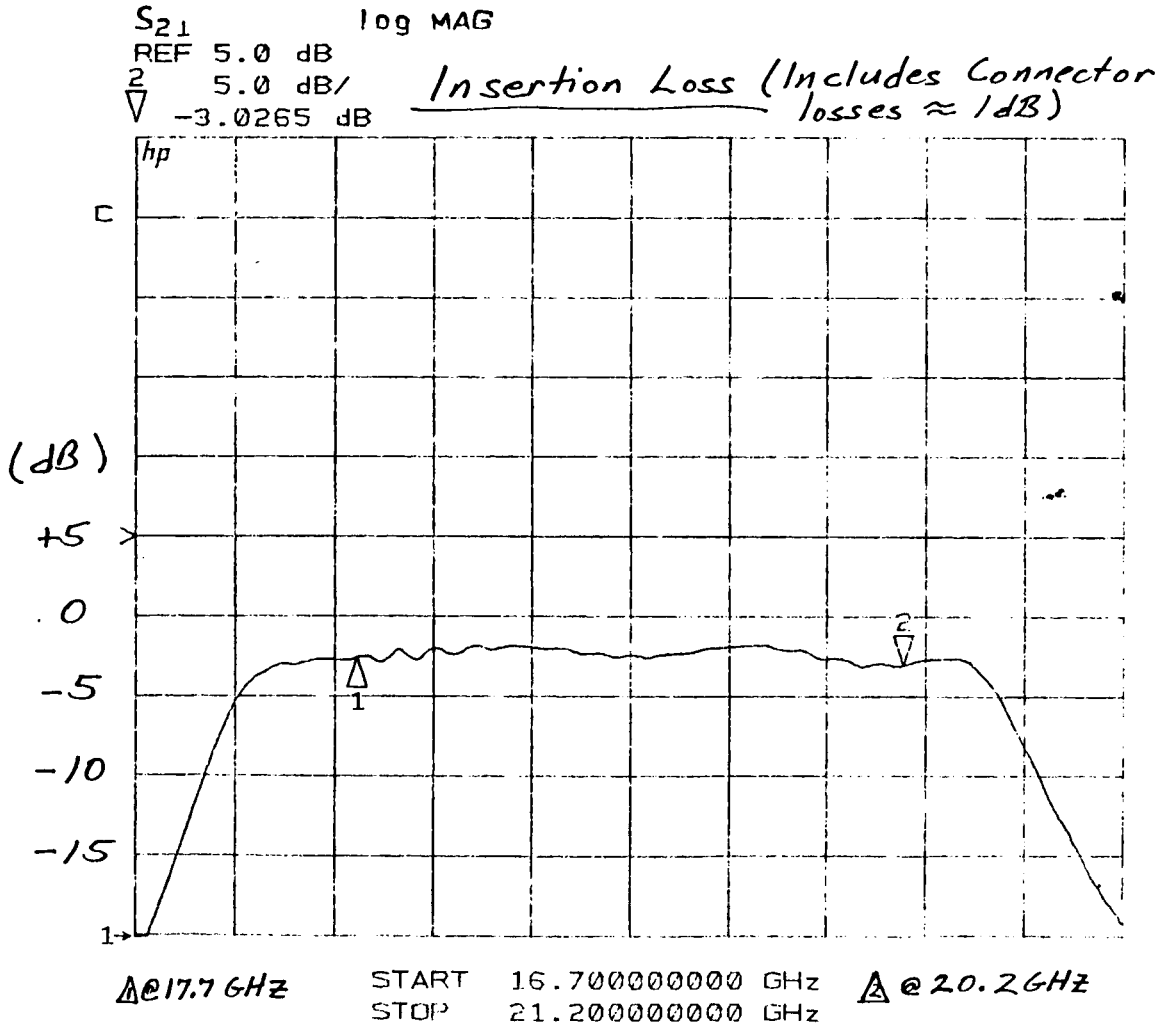


FIGURE 4-8

RF BANDPASS FILTER AT 25°C
(OUT OF BAND)

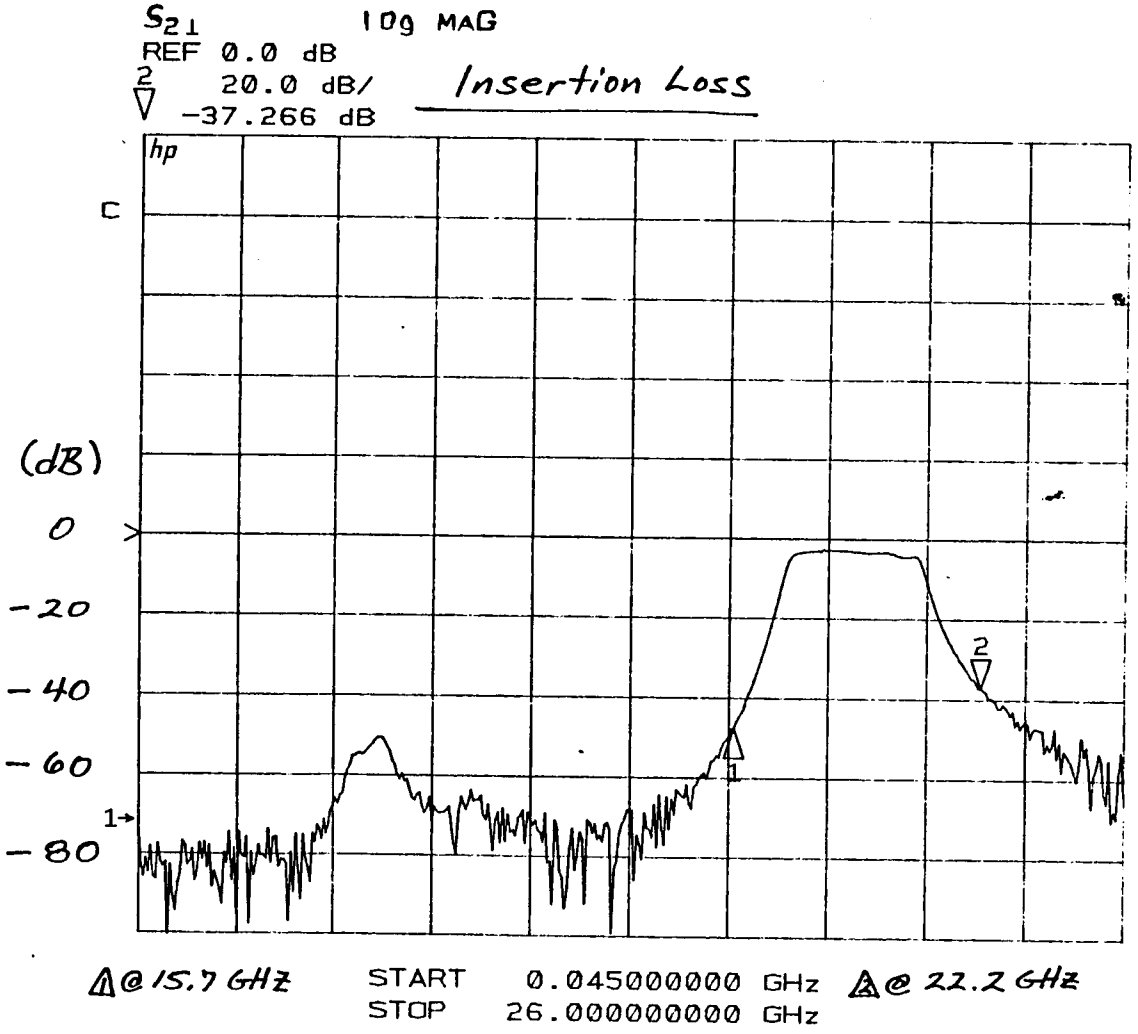


FIGURE 4-9

RF BANDPASS FILTER AT 75°C
(OUT OF BAND)

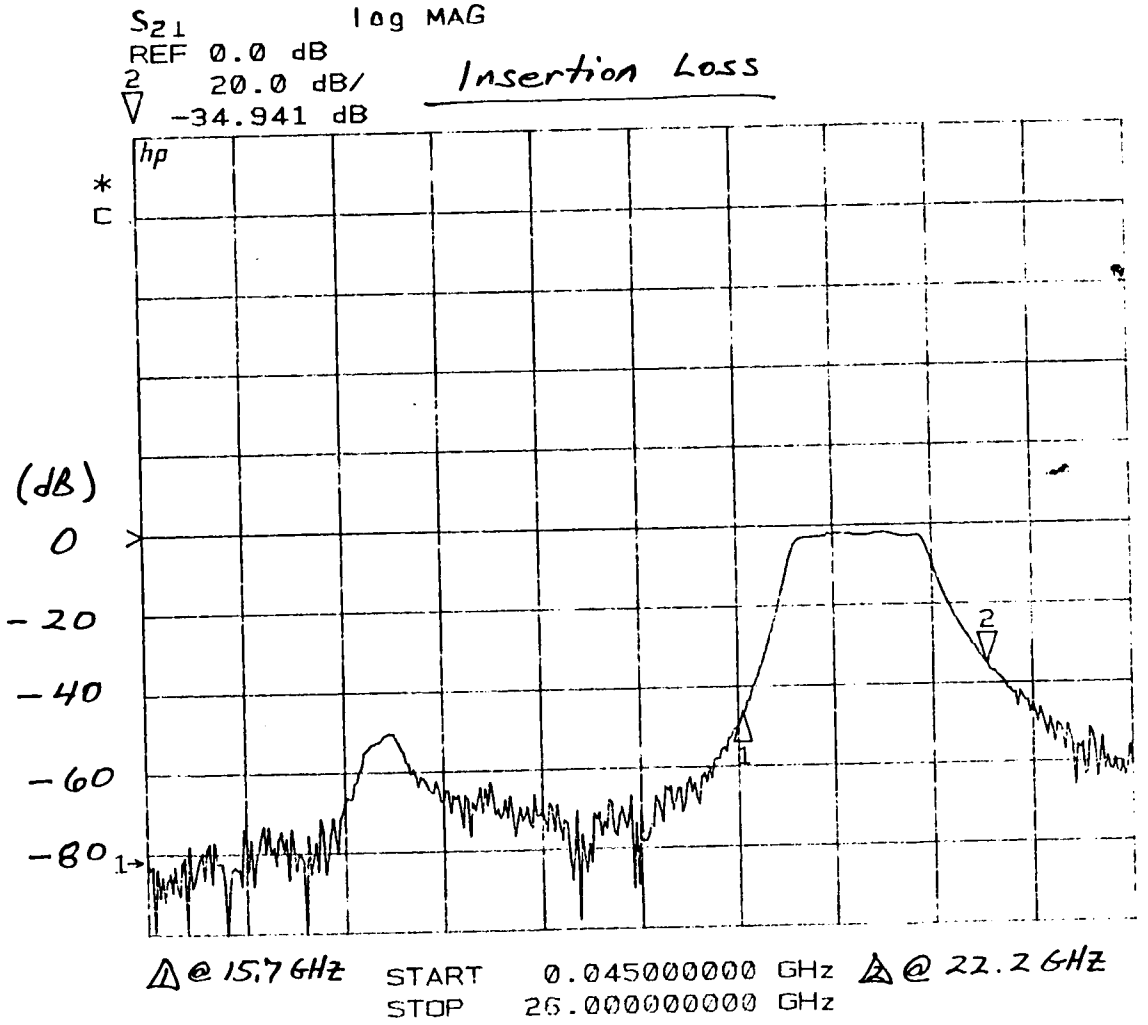


FIGURE 4-10

its test fixture, and Figure 4-2 lists the design as recorded in the Super-Compact program listing and shows the substrate layout.

Figures 4-3 and 4-4 show the filter's predicted insertion loss versus frequency for narrow and wide bandwidths, respectively. Figure 4-5 plots the in-band response of all four S parameters of the breadboard filter covered with a lid to suppress unwanted modes. The high input and output VSWRs (S11 and S22) are due mainly to the SMA test fixture connectors used and will not be present when the filter is ribbon bonded into the POC receiver. Figure 4-6 shows the out-of-band response for the same filter. The out-of-band frequencies of 14 GHz (Image) and 22.2 GHz are well within the requirements of 40 and 20 dB, respectively. The filter requirement could be met with a four pole filter since the balanced RFA has a steep low frequency roll-off and the mixer has good spur performance which reduces the required out-of-band rejection needed. Figures 4-7 and 8 and Figures 4-9 and 10 show the insertion loss versus frequency and temperature for in-band and out-of-band frequencies, respectively. The absolute insertion loss is not the same as in the previous figures because the connectors had been replaced and the filter not tuned for minimum loss. The point of these figures is the change in insertion loss as the temperature is varied Figures 4-7 and 4-8 show an increase in gain as temperature is raised and Figures 4-9 and 4-10 do not show any appreciable frequency shift versus temperature. The positive gain versus temperature characteristic partially offsets the gain decreases in the active stages and will reduce the overall gain variation versus temperature of the POC receiver. The unnoticeable frequency shift versus temperature means that practically no margin is required for temperature effects and helps keep the filter simple.

5.0 MMIC IMAGE REJECT MIXER

The test results for the MMIC IRM show good overall mixer performance such that an additional design iteration will not be necessary. The mixer block diagram is shown in Figure 5-1, and a picture of the fabricated MMIC is shown in Figure 5-2. The IRM uses three lange couplers in its design which is the same coupler used in the balanced RFA. Since the balanced RFA performed well, it was expected that the IRM would perform well, too. The following data taken on the IRM verify that it is basically a Class II mixer (higher conversion loss, intercept point and LO drive required) and that the balance and isolation qualities are acceptable for the NASA-Lewis 20 GHz POC receivers.

Figure 5-3 and 5-4 show conversion loss versus frequency for two different LO drive levels. Each of these graphs plot the mixer's conversion loss versus IF frequency for six

NASA IMAGE REJECT MIXER

(1/2 MICRON MMIC)

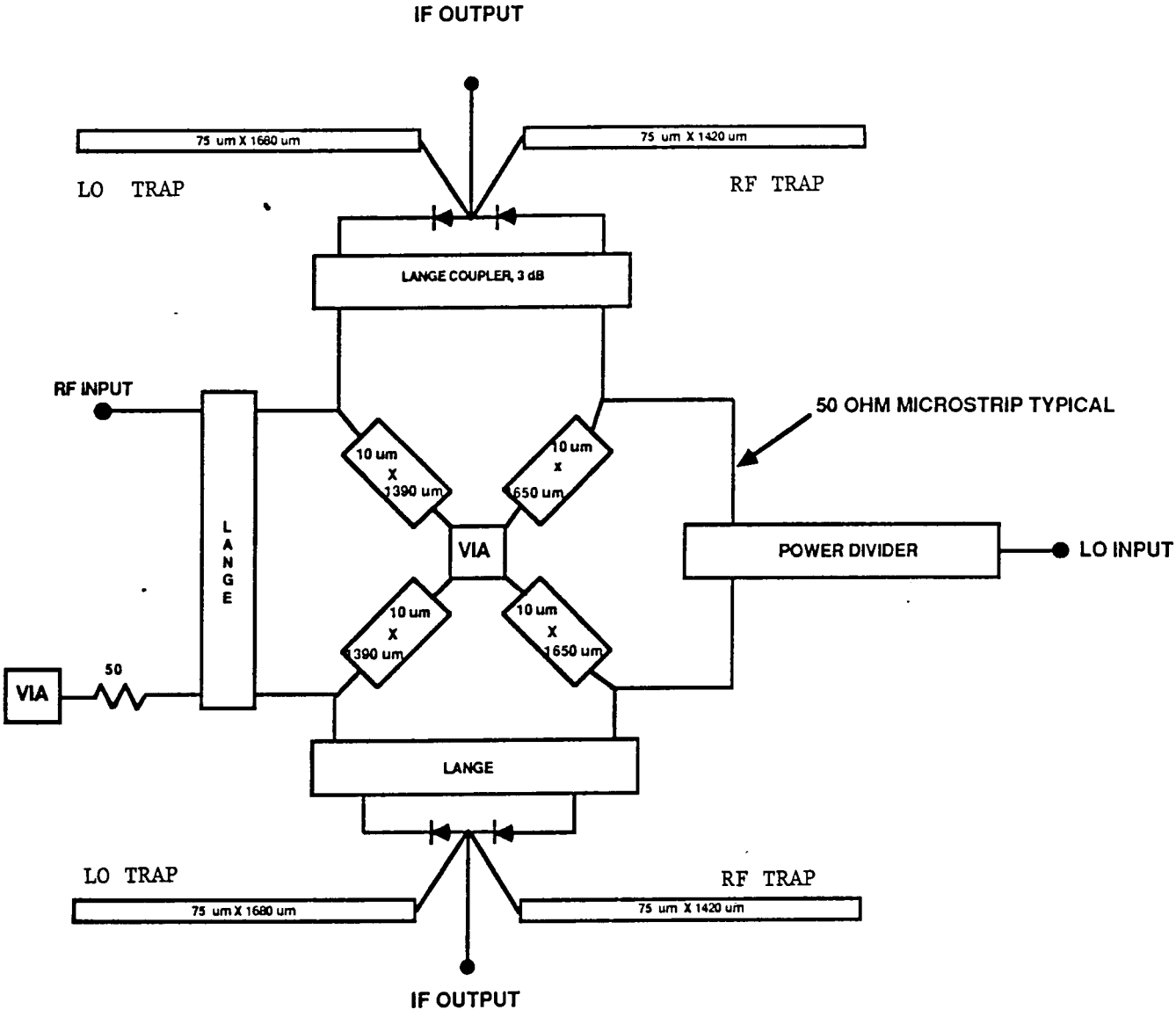


FIGURE 5-1

IMAGE REJECT MIXER

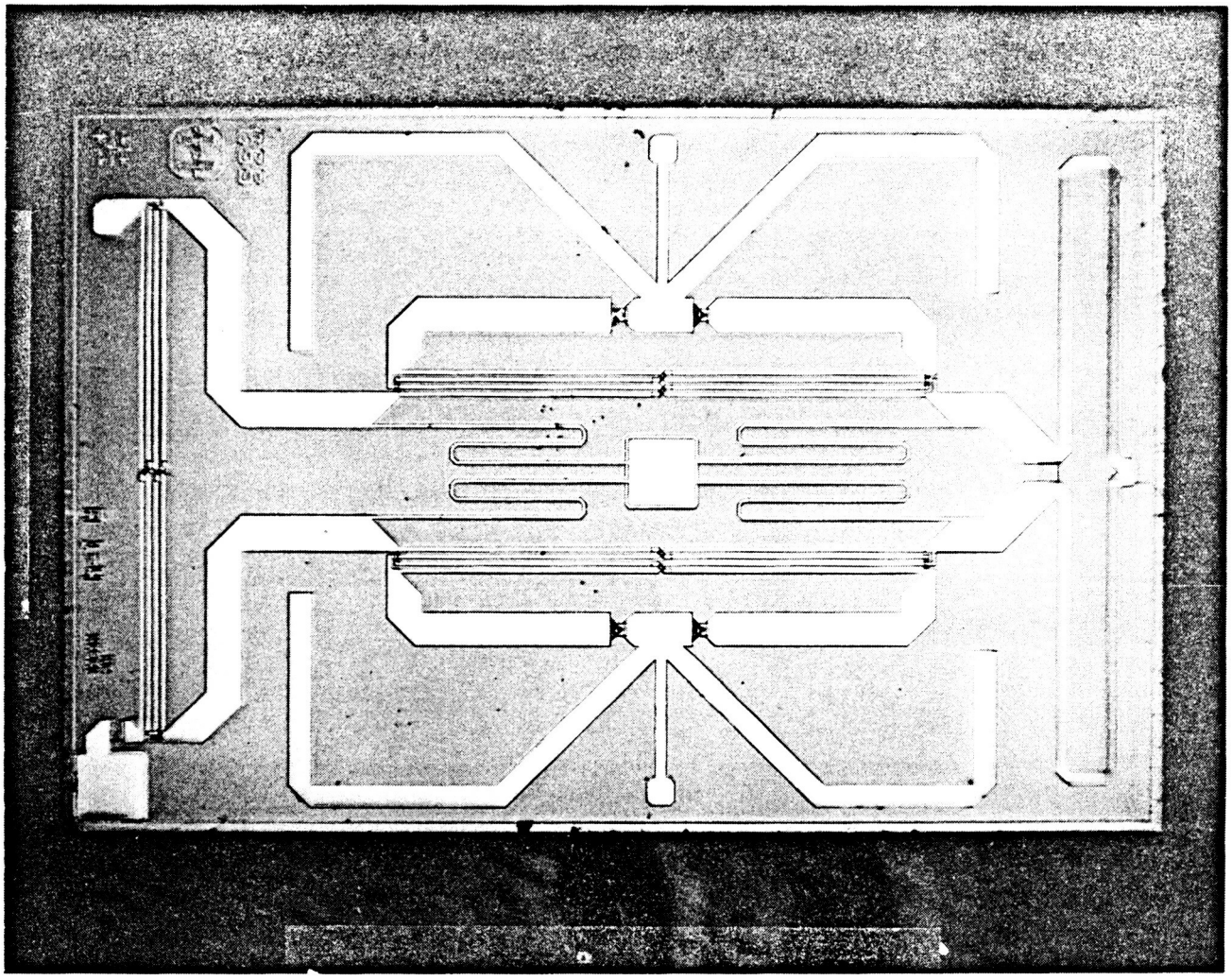


FIGURE 5-2

IMAGE REJECT MIXER CONVERSION LOSS

(+12 dBm LO)

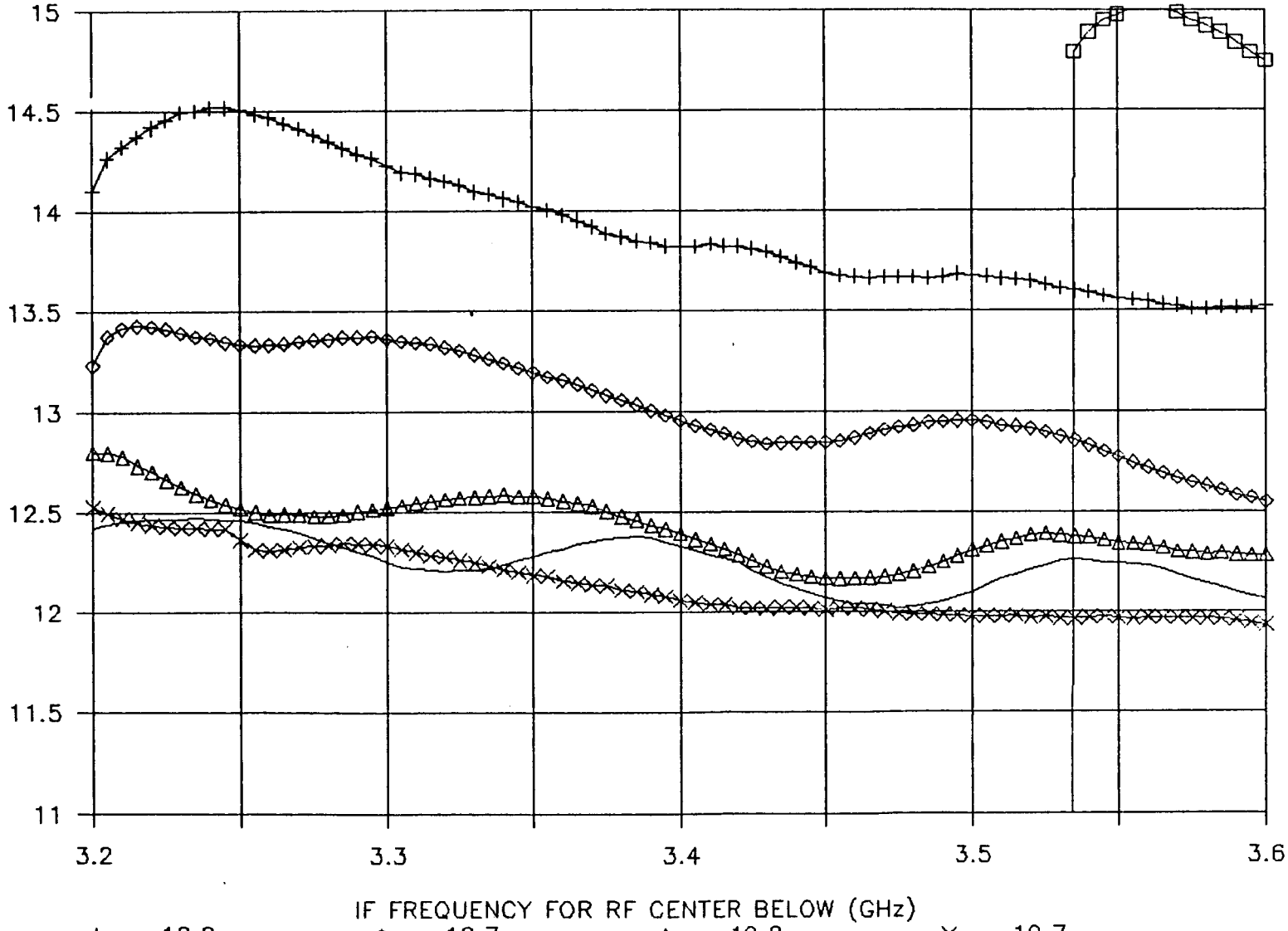


FIGURE 5-3

different fixed LO frequencies across the band. HP BASIC and Lotus spreadsheet programs were written to automatically take the data, correct for test fixture insertion losses and to minimize measurement errors. Each data point, signified by each symbol on the lines plotted, was measured four times and averaged to minimize the influence of noise and any oscillator power fluctuations, etc. The programs and methods used to gather the IRM data are directly applicable to testing the POC receivers in the same areas and will be used along with an updated receiver test procedure.

Actual measurements were made from the RF input to the I and Q IF outputs. However, the data displayed in Figures 5-3 and 5-4 is for the IRM with an ideal quadrature hybrid connected at its output. The impact of a non-ideal hybrid is shown in Figure 5-5 which was taken from the IRM connected to the breadboard hybrid/ bandstop filter. The null depth shown was measured at the image output port (as compared to the desired real output port) of the IRM/hybrid combination. As shown in the companion graph (insertion loss), no more than approximately 0.1 dB is added to the mixer's conversion loss due to the overall IRM/ hybrid amplitude and phase tracking qualities of the breadboard circuits at the upper NASA band edge of 20.2 GHz.

In the first graph (Figure 5-3) the maximum conversion loss is about 15 dB for a +12 dBm LO drive while in the second (Figure 5-4) the conversion loss is approximately 13 dB for a +17 dBm LO drive. However, the reduced conversion loss comes at the price of increased gain ripple. Part of the gain ripple in Figure 5-4 is due to VSWR ripple from the test fixture used measuring the IRM's performance. During the +17 dBm LO test a connector broke and was reconnected. The VSWR of the test fixture is not as good as the microstrip ribbon bonds which will be used in the integrated POC receivers.

Figure 5-6 shows the IRM input and output intercept point performance versus frequency at LO drive levels of +12 and +17dBm. Again improved performance is obtained at the higher LO drive of +17 dBm. Figure 5-7 gives the spur chart developed for the in-band and out-of-band spurs for the NASA-Lewis frequency plan. The IRM as used in the POC receivers will have a maximum input power level of -12 dBm, and therefore, the highest spur level will be -46 dBc (-44dBc from the 2x3 spur less 2 dB from being backed off 2 dB in drive from -10 dBm).

Finally, Figures 5-8 through 5-10 plot the mixer's return loss and isolation at/through various ports with the mixer diodes turned off. These diodes are turned off to allow the use of a network analyzer for the measurements. Under actual operation (diodes being driven) the return loss and isolation will improve above that shown in the figures as the inputs become properly terminated. Notice in Figure 5-8 the dip in return loss for the LO input within the LO band. This is due to the design bandwidth of the in phase LO power divider and the LO

IMAGE REJECT MIXER CONVERSION LOSS

(+17 dBm LO)

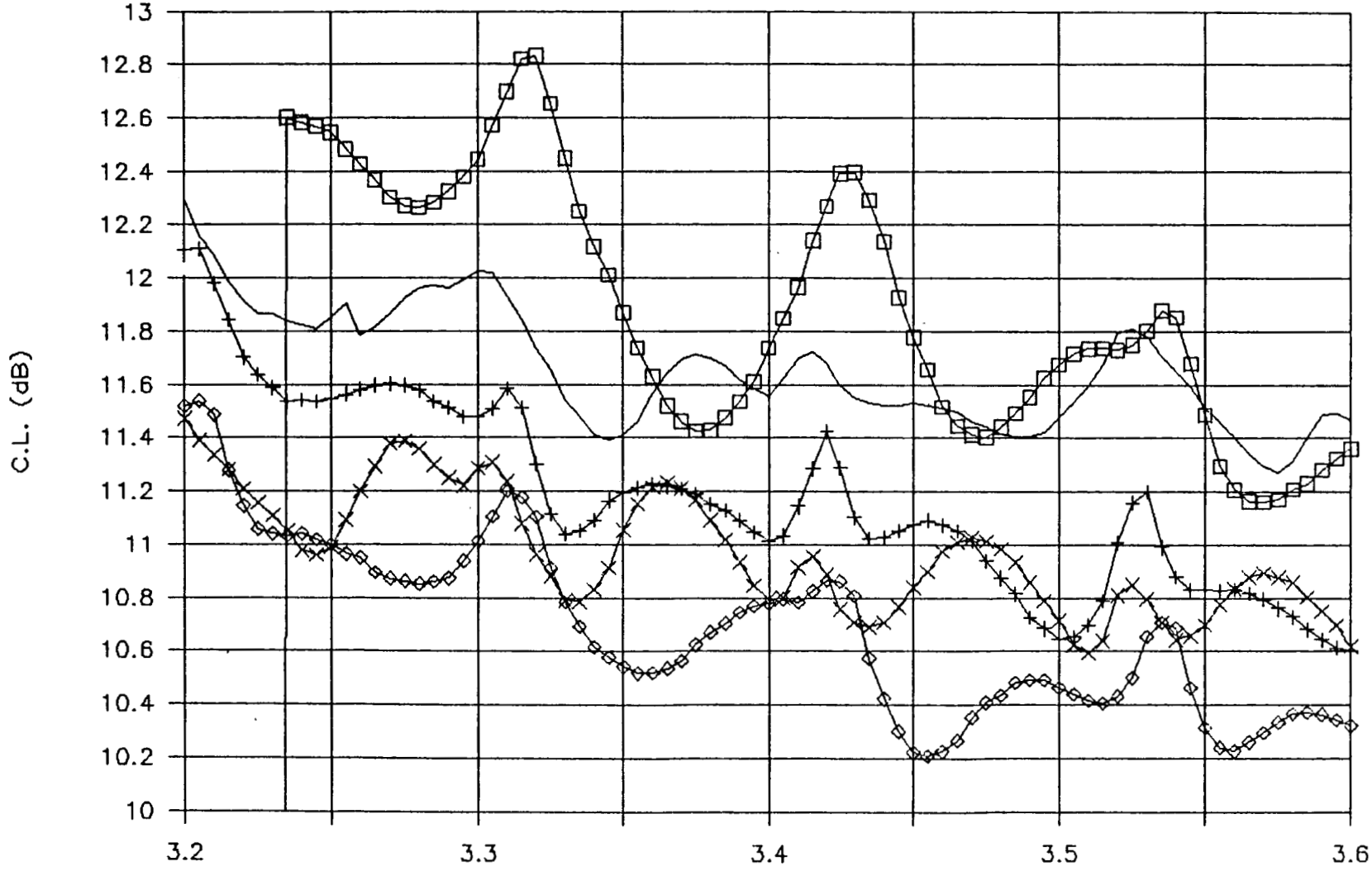


FIG. 5

IMAGE REJECT MIXER
AMPLITUDE & PHASE TRACKING

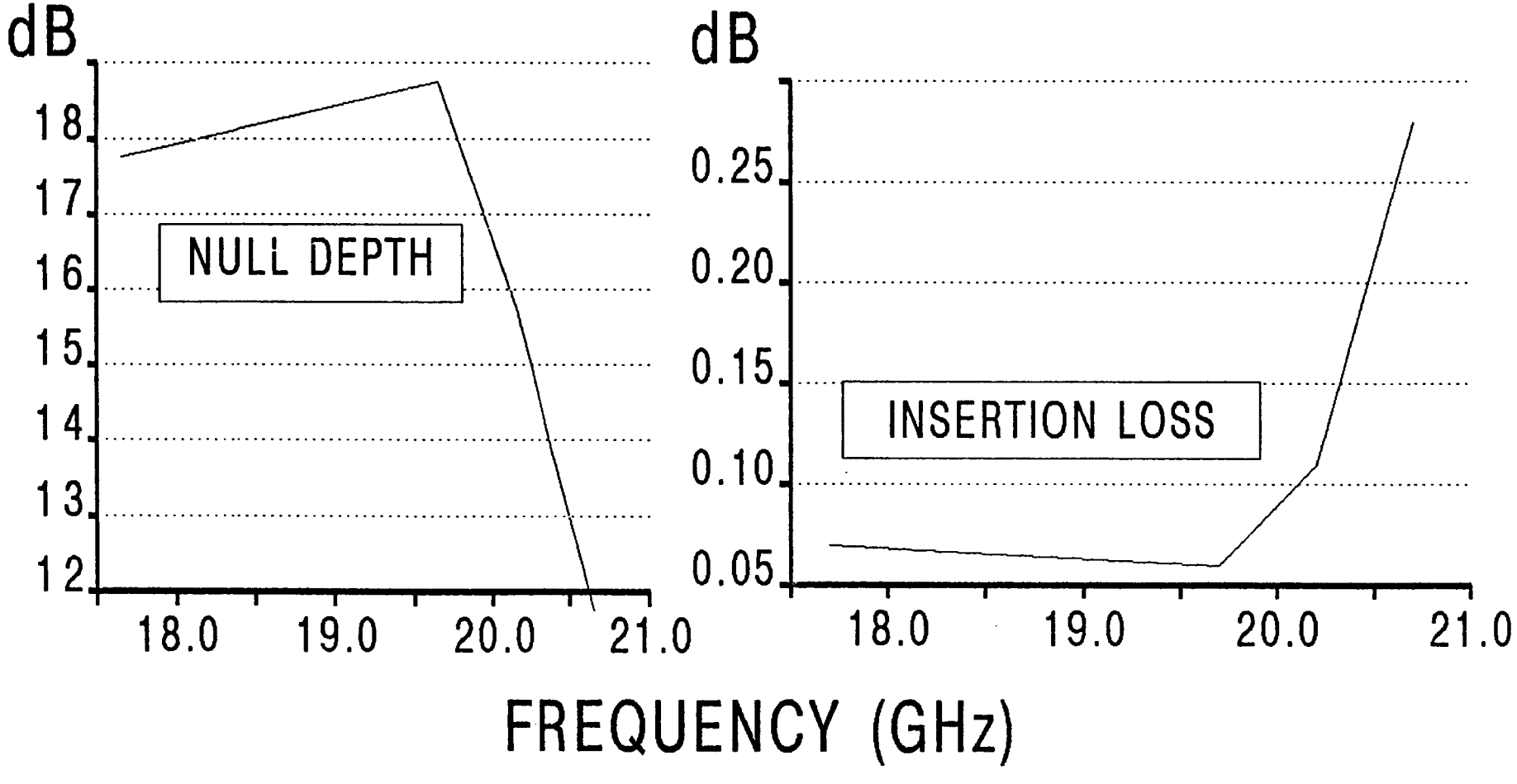
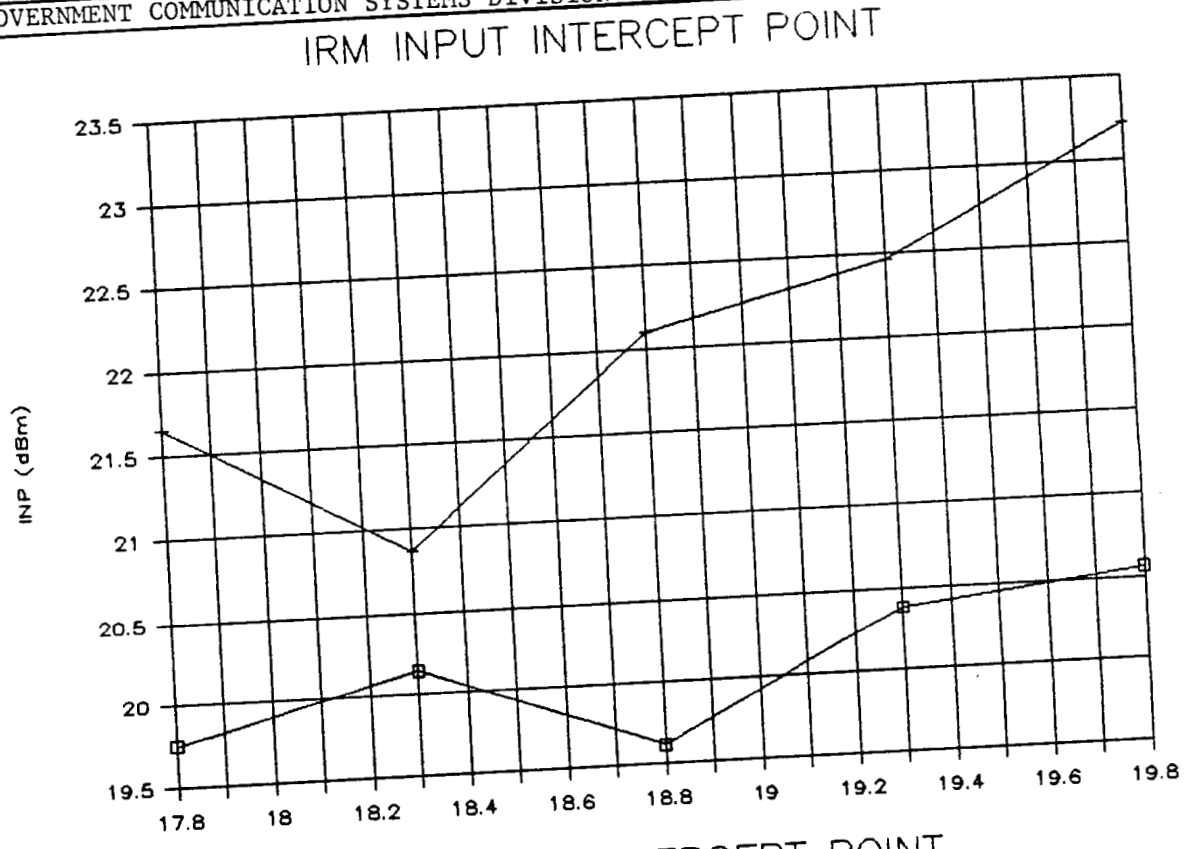


FIGURE 5-5


IRM INPUT INTERCEPT POINT
INP (dBm)
23.5
23
22.5
22
21.5
21
20.5
20
19.5
17.8
18
18.2
18.4
18.6
18.8
19
19.2
19.4
19.6
19.8

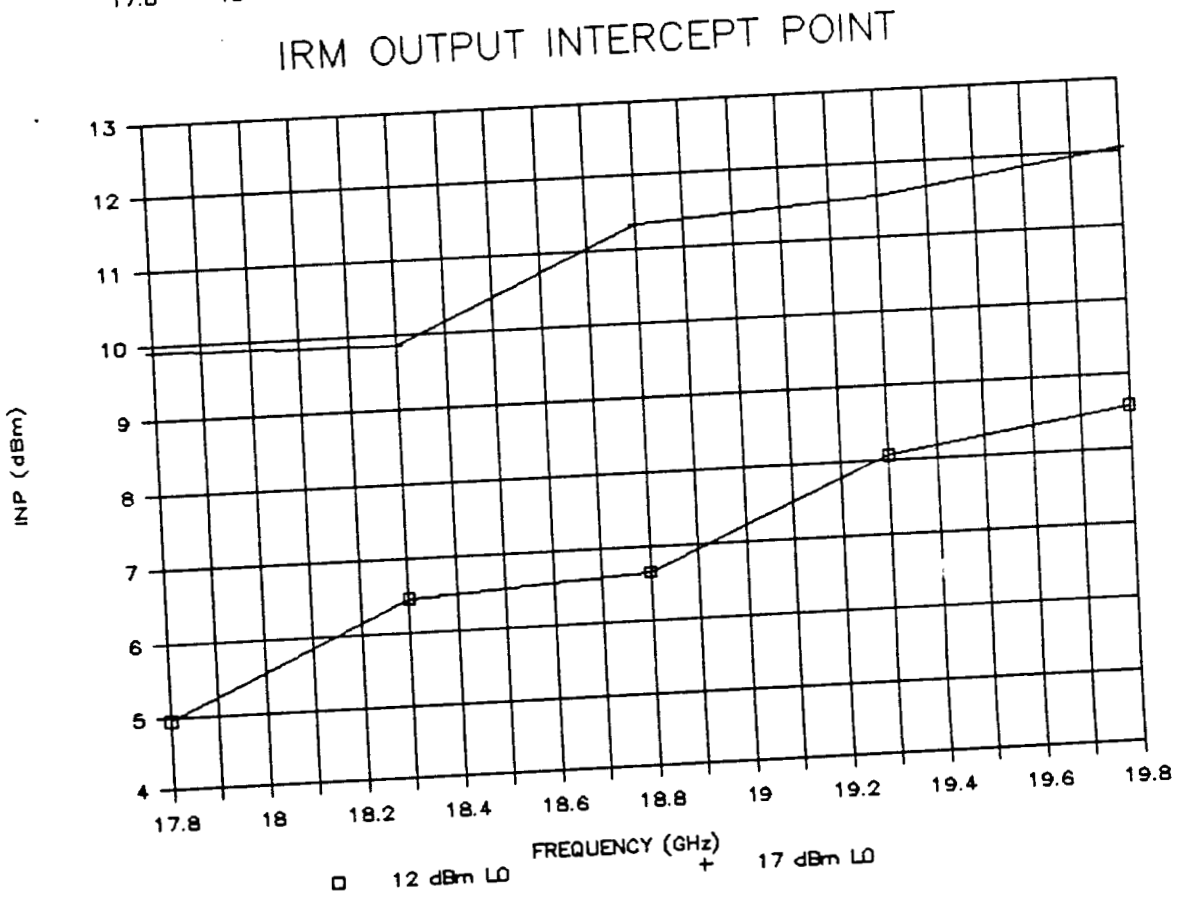

IRM OUTPUT INTERCEPT POINT
INP (dBm)
13
12
11
10
9
8
7
6
5
4
17.8
18
18.2
18.4
18.6
18.8
19
19.2
19.4
19.6
19.8
FREQUENCY (GHz)
12 dBm LO
17 dBm LO

FIGURE 5-6

IRM SPUR CHART

(dB BELOW CARRIER)

RF FREQUENCY MULTIPLE (M)	LO FREQUENCY MULTIPLE (N)				
	0	1	2	3	4	5
5						>56
4					>60	>60
3				>61	>59	
2			46 / 52	44 / 60		
1						
0						

LO @ +12 dBm
RF @ −10 dBm
/
LO @ +17 dBm
RF @ 0 dBm

LO @ +12 dBm
RF @ −10 dBm

FIGURE 5-7

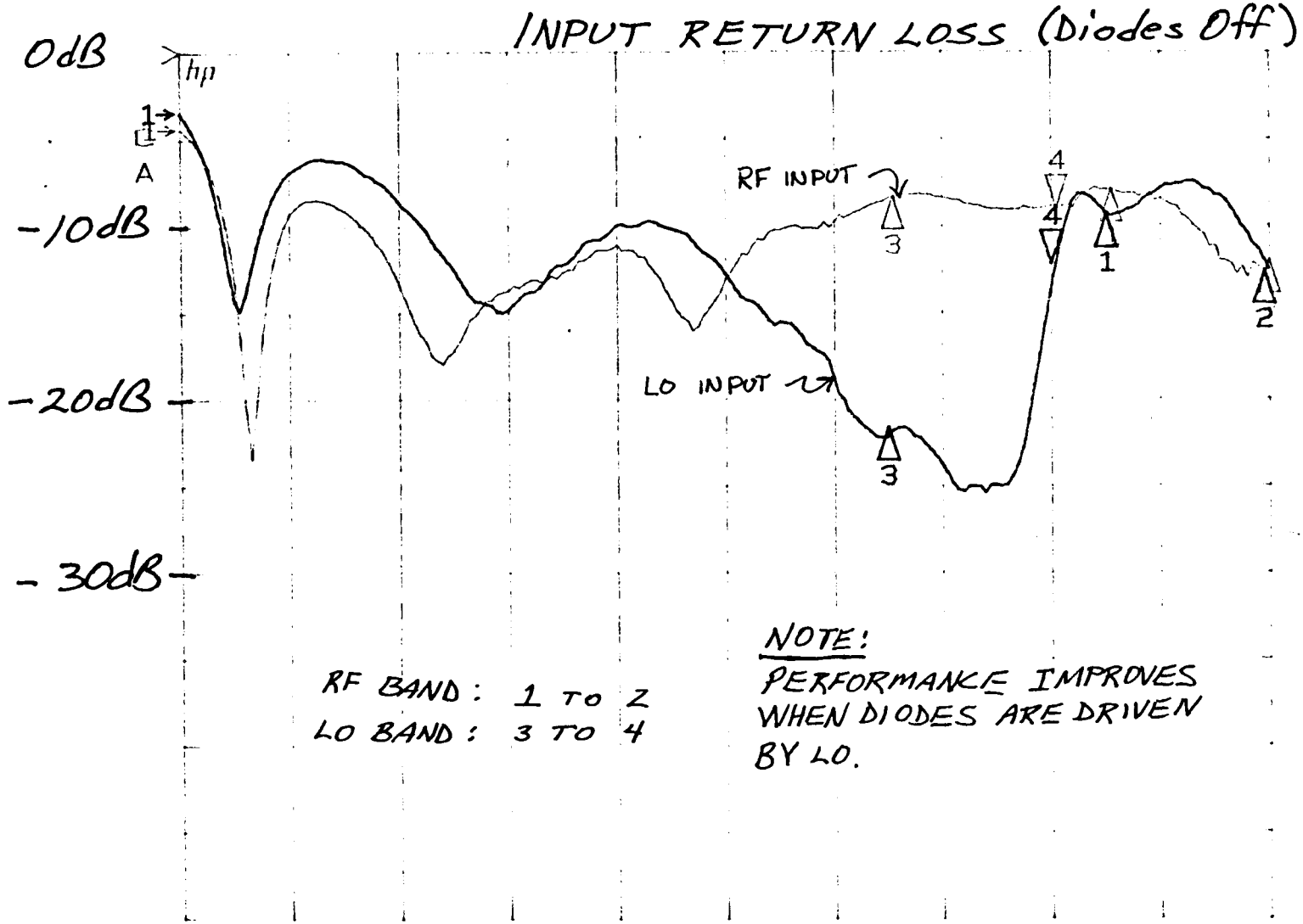
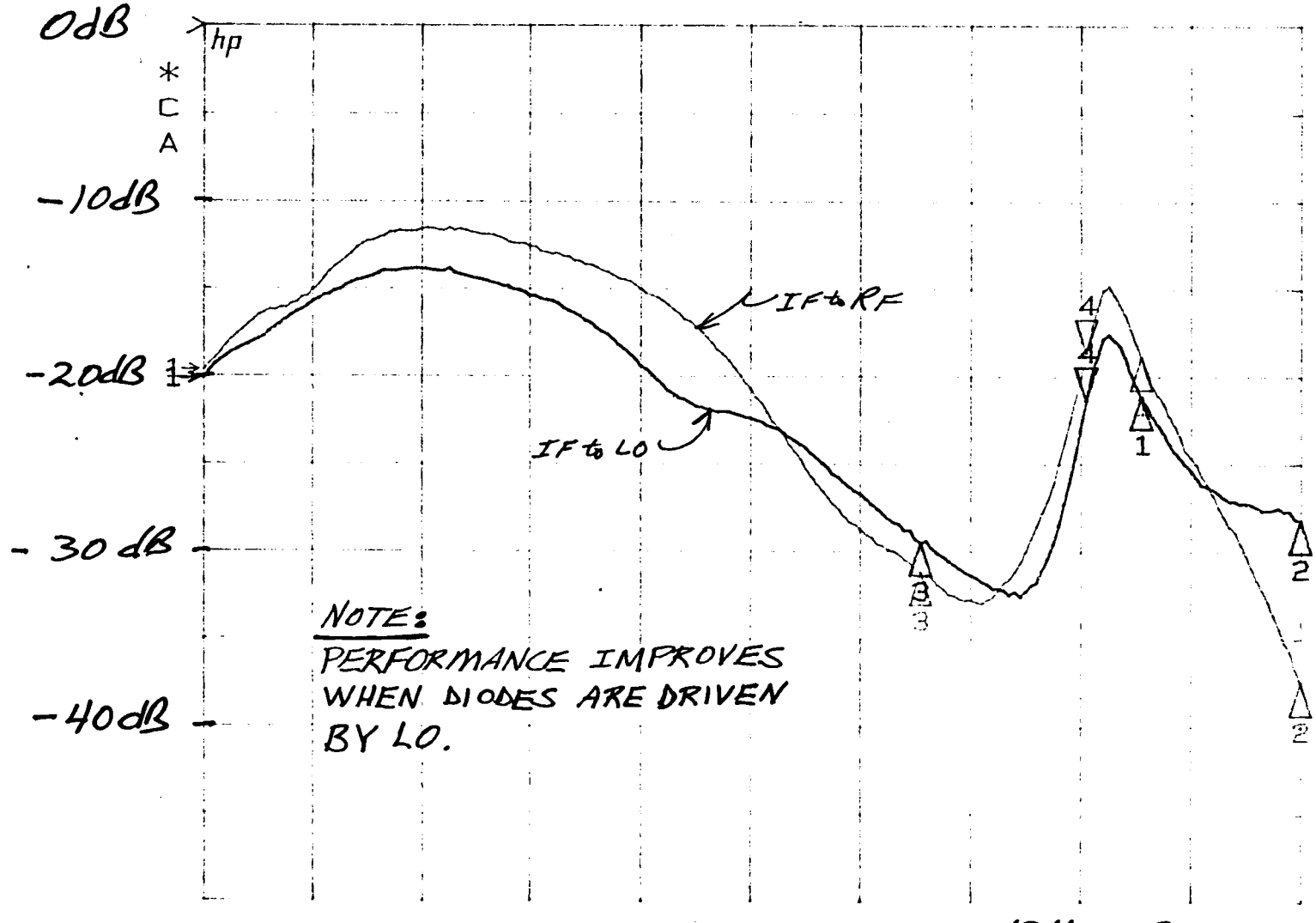


FIGURE 5-8

ISOLATION (DIODES OFF)

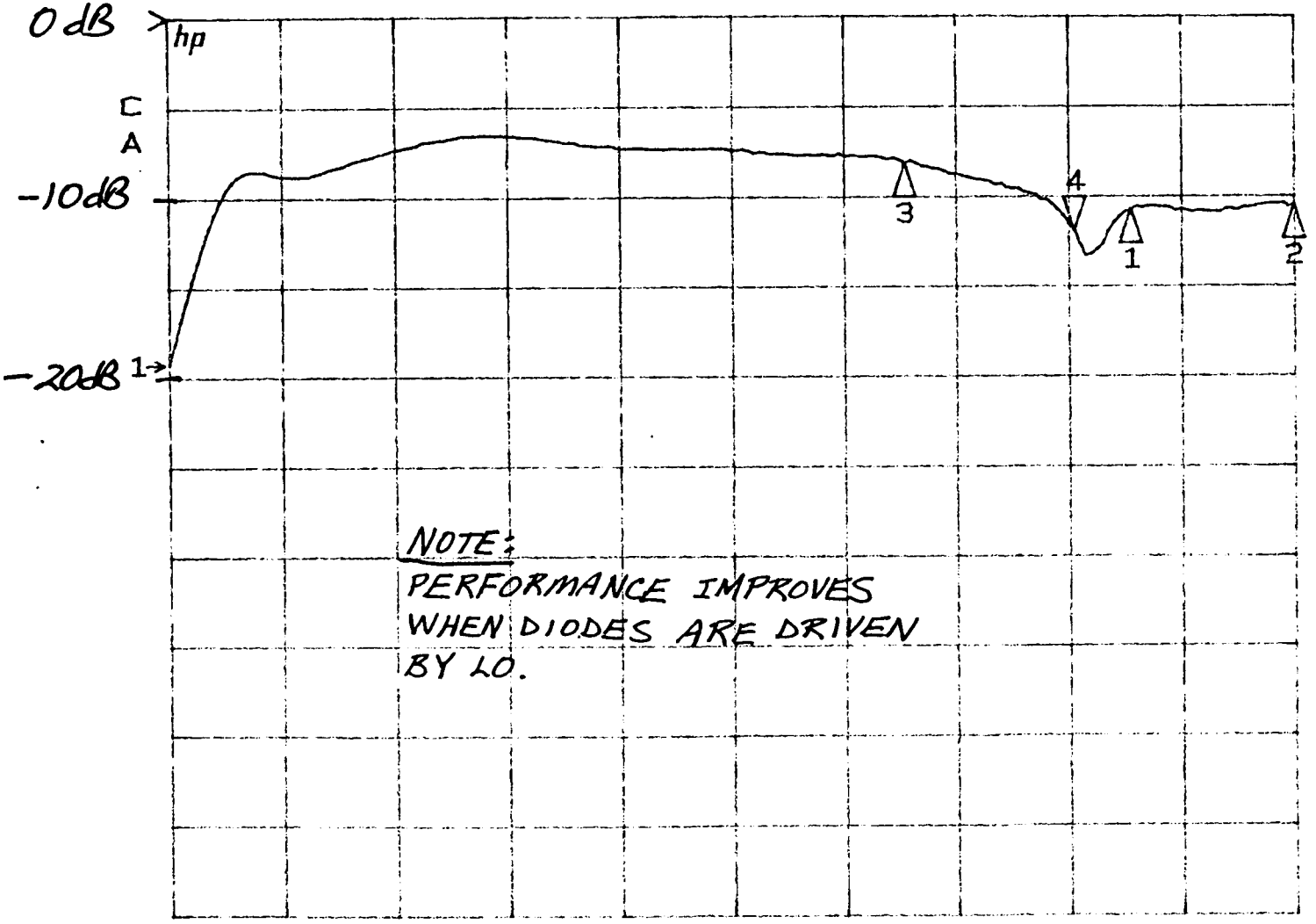


RF BAND: 1 to 2 START 3.200000000 GHz
LO BAND: 3 to 4 STOP 20.200000000 GHz

IRM 1285-1
A5-10

FIGURE 5-9

LO TO RF ISOLATION (DIODES OFF)



RF BAND: 1 TO 2 START 3.200000000 GHz
LO BAND: 3 TO 4 STOP 20.200000000 GHz

IRM 1285-1
A5-10

FIGURE 5-10

input signal reflecting off the two lange couplers at each IF section of the mixer into the RF input and being terminated. The isolation depicted in Figure 5-9 shows dips in the LO and RF bands for both IF to RF and IF to LO isolation. This is due to the RF and LO traps at each IF output. And in Figure 5-10 the LO to RF isolation is quite flat over both LO and RF bands and not very deep. This is caused in the same way as the dip in Figure 5-8 where the LO reflects through to the RF input in a low loss fashion because the mixer diodes are turned off (not being driven). When the diodes are driven by the LO, the LO signal will be terminated in the lange coupler instead of reflection off it, thereby greatly increasing the LO to RF isolation.

6.0 HYBRID/BANDSTOP FILTER

The IF Hybrid/Bandstop Filter is used to combine the quadrature outputs of the IRM. The Bandstop Filter rejects the LO frequencies and prevents over driving the IF amplifier which follows the hybrid. A bandpass filter is not required as one is contained within the modem which follows the POC receiver. Figure 6-1 is a picture of the breadboard IF Hybrid/Bandstop Filter, Figures 6-2 and 6-3 list the Super-Compact program circuit file, and Figure 6-4 depicts its substrate layout. This circuit operates from 3.1 to 3.6 GHz with low loss and rejects 14.3 to 16.8 GHz leakage signals from the local oscillator. Figure 6-5 shows the predicted frequency response from Super-Compact.

Figures 6-6 through 6-8 give the measured performance of the breadboard Hybrid/BSF. In Figure 6-6 it can be seen that the coupler is overcoupled by not obtaining balanced direct and coupled port insertion loss performance. This was caused from the circuit being slightly over etched during fabrication. This can be corrected be adjusting the coupler line widths and spacings to account for the overcoupling. Also, an additional BSF stub will be added to realize a flatter rejection of approximately 20 dB over the entire LO band. Figures 6-7 and 6-8 are plots of return loss and directivity, respectively. Both of these parameters are impacted slightly by the over etched circuit and will improve in the final design iteration.

7.0 DC REGULATOR

The DC regulators used in the receiver drop the input +/-15 volts from the outboard power supply to that required at each functional block within the receiver. Since the final designs were not available during the breadboard phase, only broad ranges of voltages and currents were known. Therefore, a general regulator design was derived and tested at various voltage and

IF HYBRID/BANDSTOP FILTER

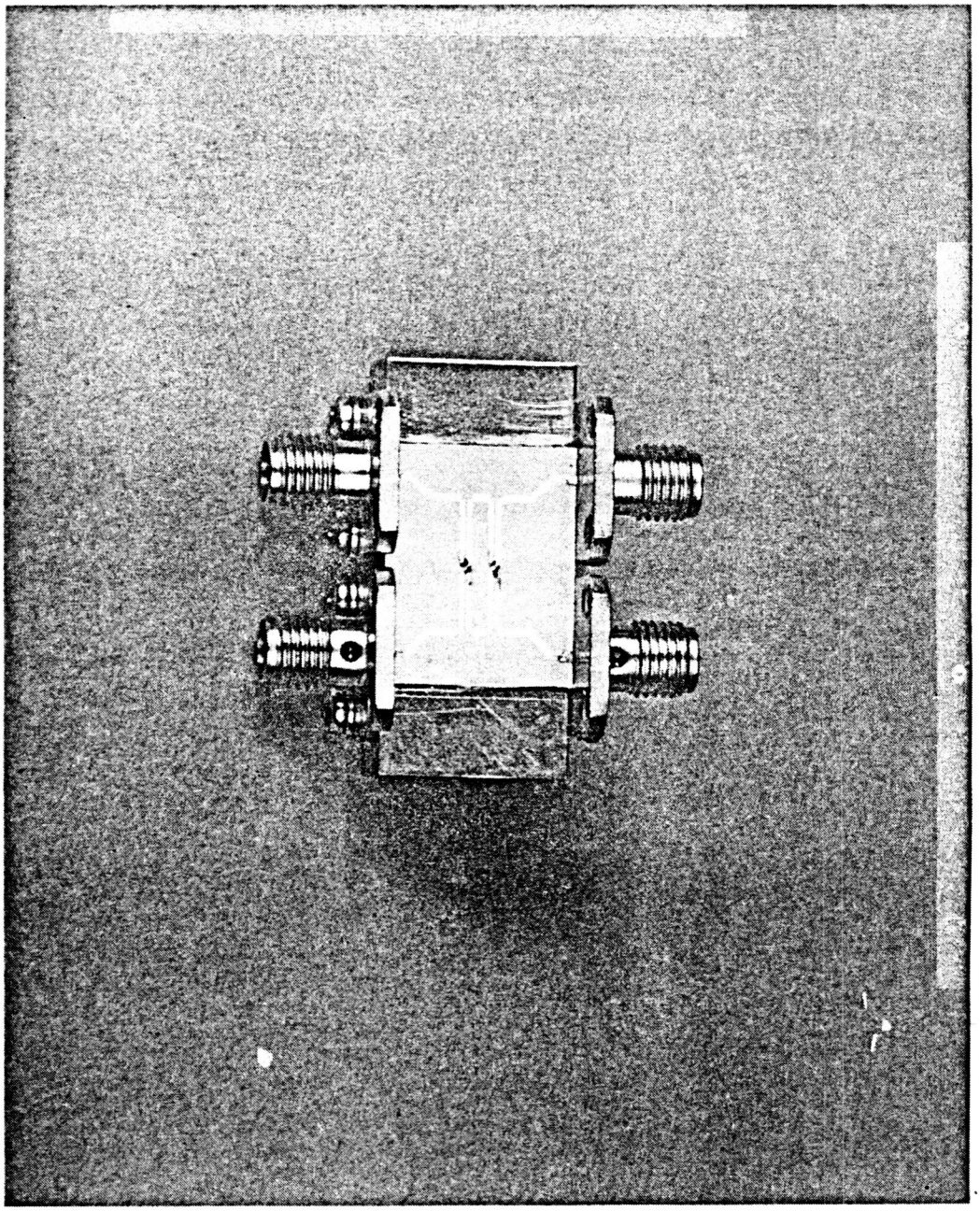


FIGURE 6-1

IMAGE REJECT MIXER COUPLER DESIGN

```
W1:18MIL
S1:5MIL
P1:172MIL
BLK
CPL 1 2 3 4 W=W1 S=S1 P=P1 SUB
CPL 3 4 5 6 W=W1 S=S1 P=P1 SUB
CPL3: 4POR 1 2 5 6
END
BLK
TRL 11 12 W=25MIL P=50MIL SUB
OST 12 W=5MIL P=69MIL SUB
OPEN 12 W=5MIL SUB
TRL 12 13 W=25MIL P=59MIL SUB
OST 13 W=5MIL P=78MIL SUB
OPEN 13 W=5MIL SUB
TRL 13 1 W=25MIL P=50MIL SUB
CPL3 1 2 3 4
CPL3 2 5 6 3
RES 4 0 R=50
HYB3: 3POR 11 5 6
END
LAD
TRL 1 2 W=?21.421MIL? P=1IN SUB
LINE: 2POR 1 2
END
FREQ
STEP 3.17GHZ 3.57GHZ .1GHZ
END
OUT
PRI HYB3 S
END
OPT
LINE MS11=0
END
DATA
SUB: MS H=25MIL ER=10.5 MET1=CU 1MIL MET2=AU 10UM
END
```

FIGURE 6-2

BAND STOP FILTER DESIGN

```
BLK
TRL 1 2 W=25MIL P=100MIL SUB
OST 2 W=5MIL P=?69.14MIL? SUB
OPEN 2 W=5MIL SUB
TRL 2 3 W=25MIL P=?59.1MIL? SUB
OST 3 W=5MIL P=?78.074MIL? SUB
OPEN 3 W=5MIL SUB
TRL 3 4 W=25MIL P=100MIL SUB
FILT: 2POR 1 4
END
FREQ
STEP 1GHZ 14GHZ 1GHZ STEP 14.3GHZ 16.9GHZ .2GHZ
END
OPT
FILT MS21=.03 LT
END
OUT
PRI FILT S
END
DATA
SUB; MS H=25MIL ER=10.2
END
```

FIGURE 6-3

IMAGE REJECT MIXER COUPLER AND BSF

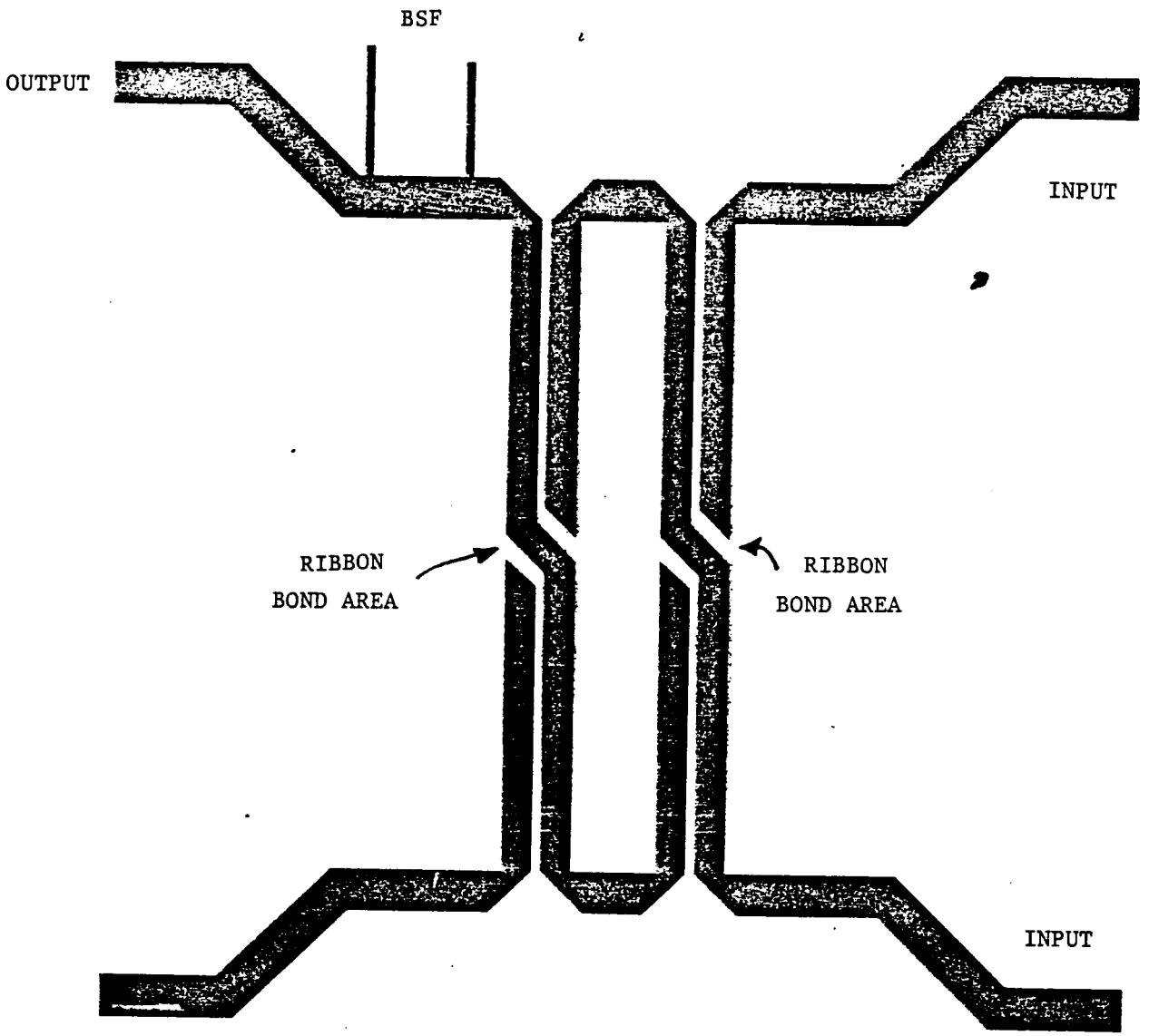


FIGURE 6-4

BANDSTOP FILTER PREDICTED INSERTION LOSS

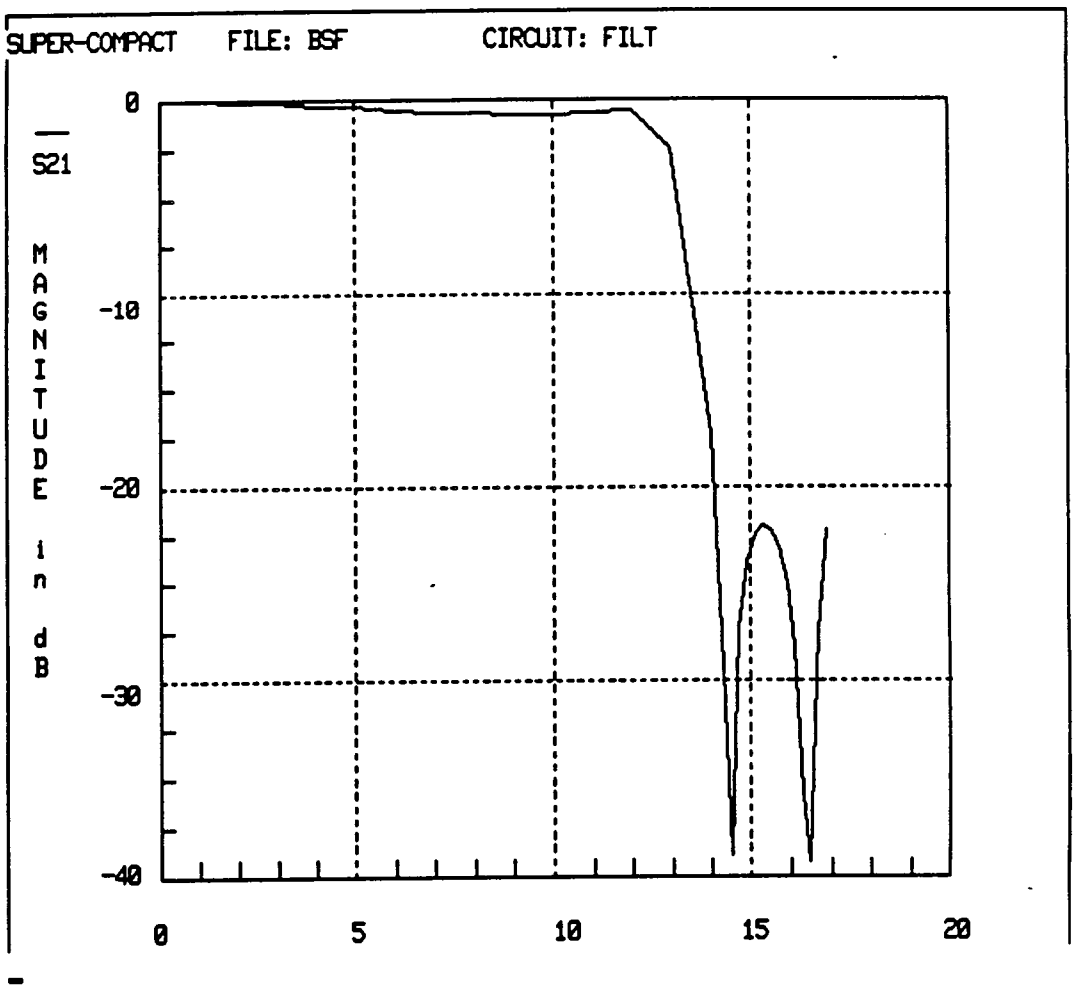


FIGURE 6-5

IF HYBRID AND BANDSTOP FILTER

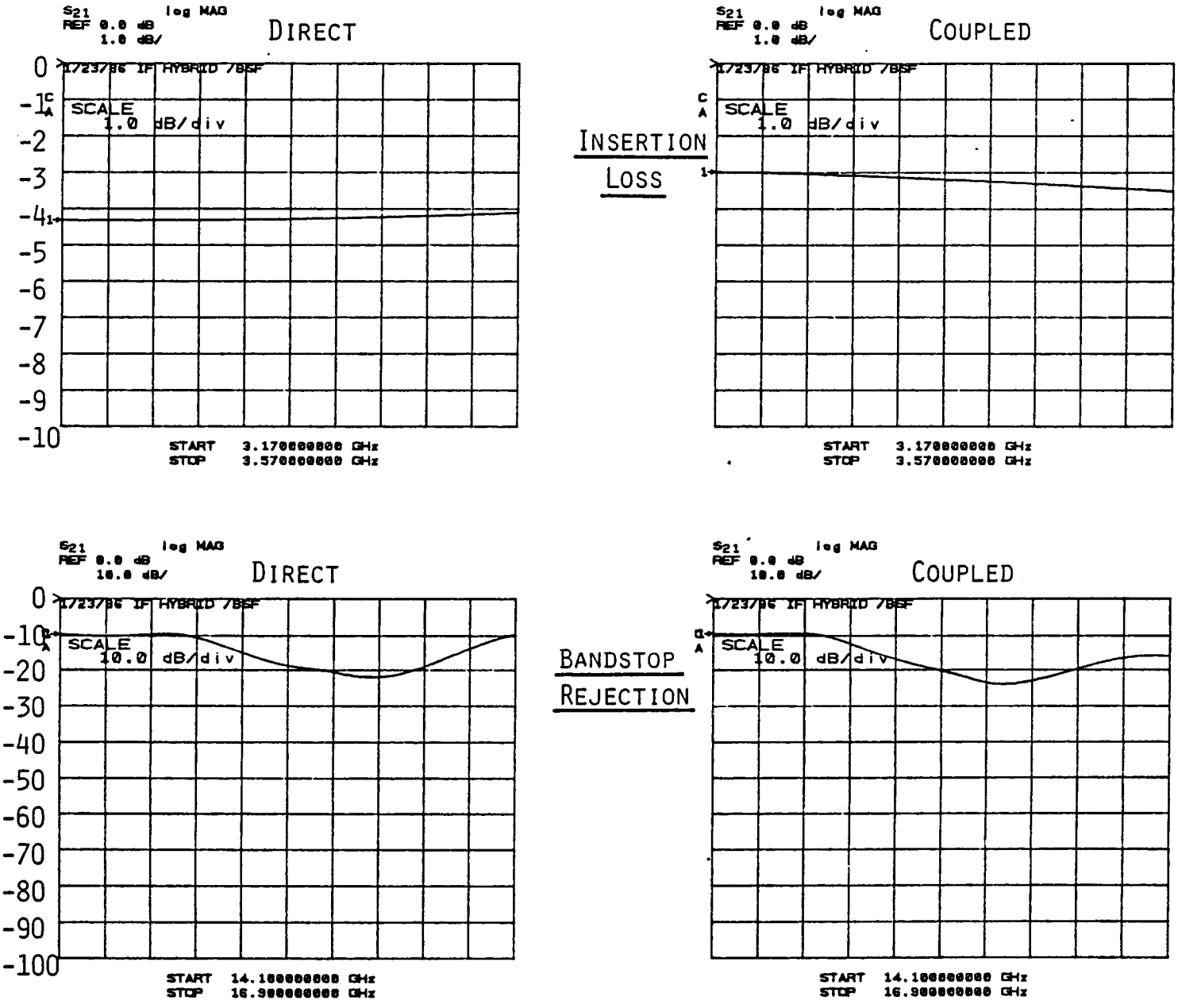
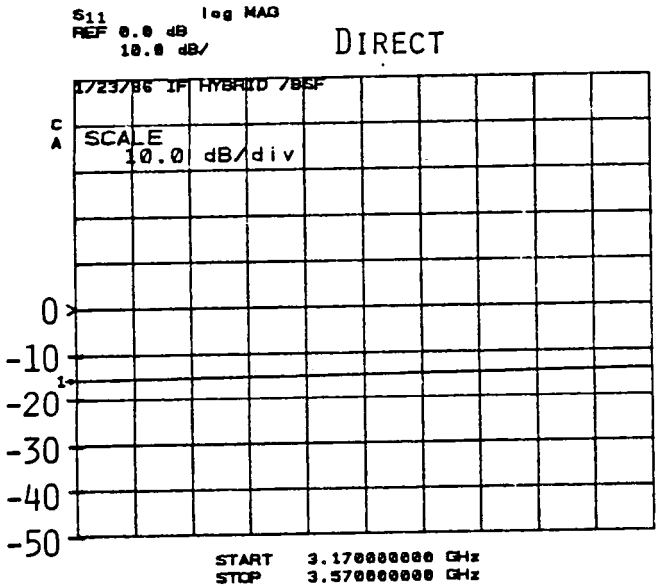
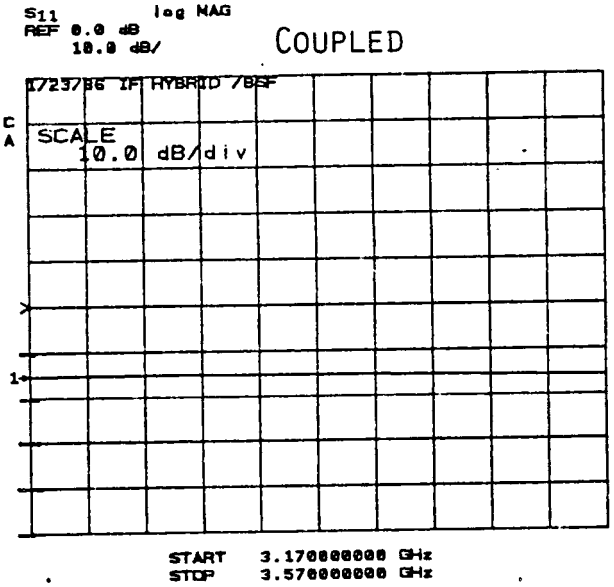


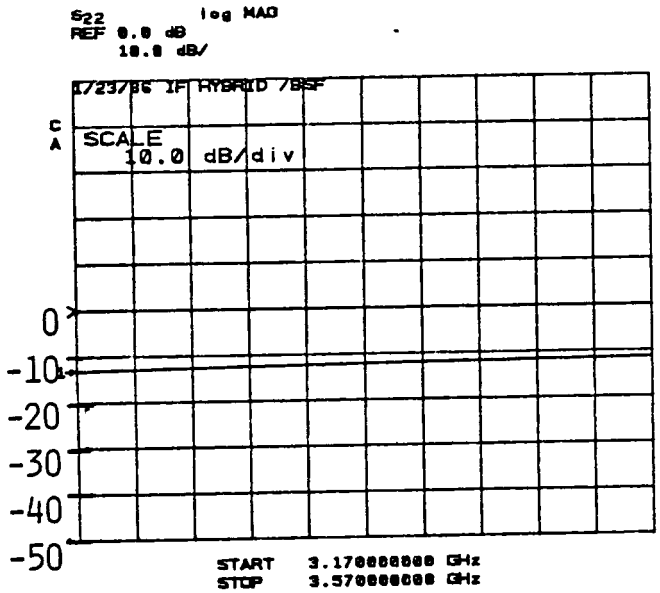
FIGURE 6-6

IF HYBRID AND BANDSTOP FILTER



INPUT RETURN LOSS



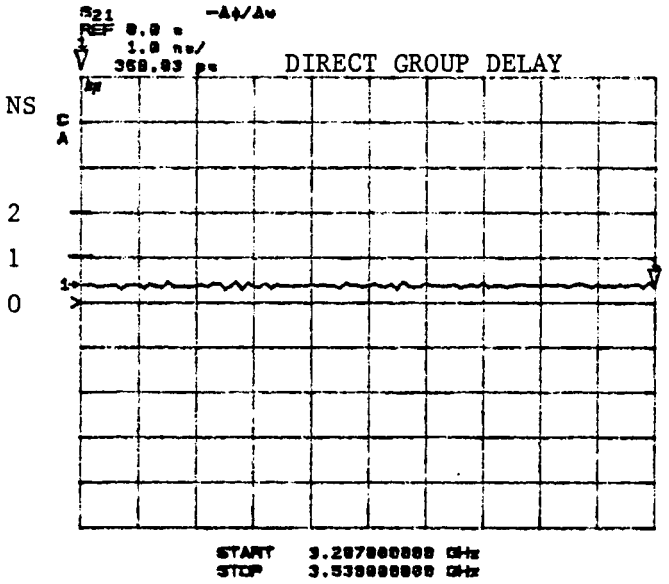


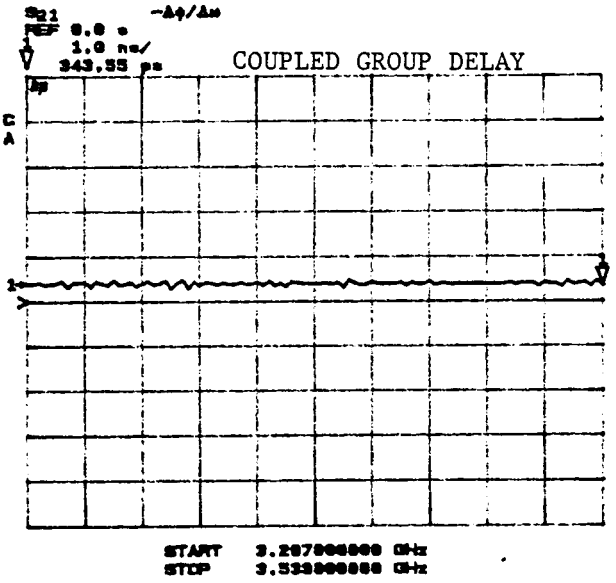
OUTPUT RETURN LOSS

ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE 6-7

IF HYBRID AND BANDSTOP FILTER





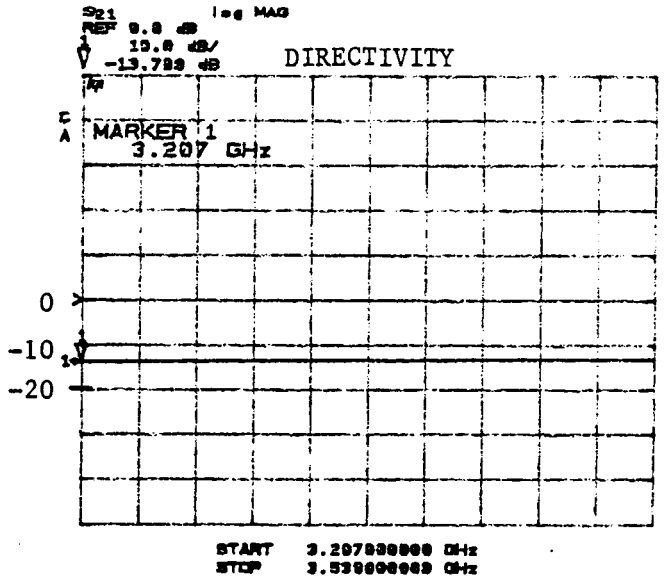


FIGURE 6-8

LOW POWER DC REGULATOR

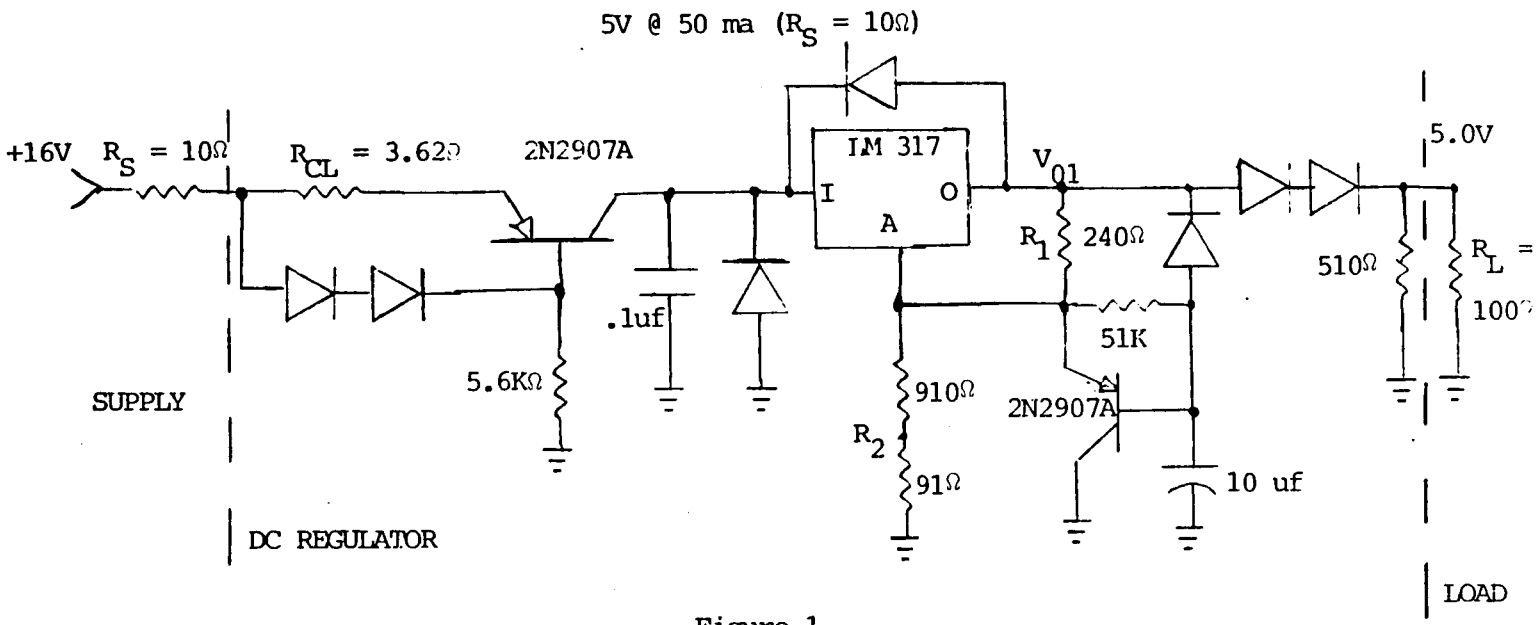


Figure 1

Pos. Regulator Equation = $V_{01} = 1.25\ (1 + R_2/R_1)$

All diodes 1n4001

MEDIUM POWER DC REGULATOR

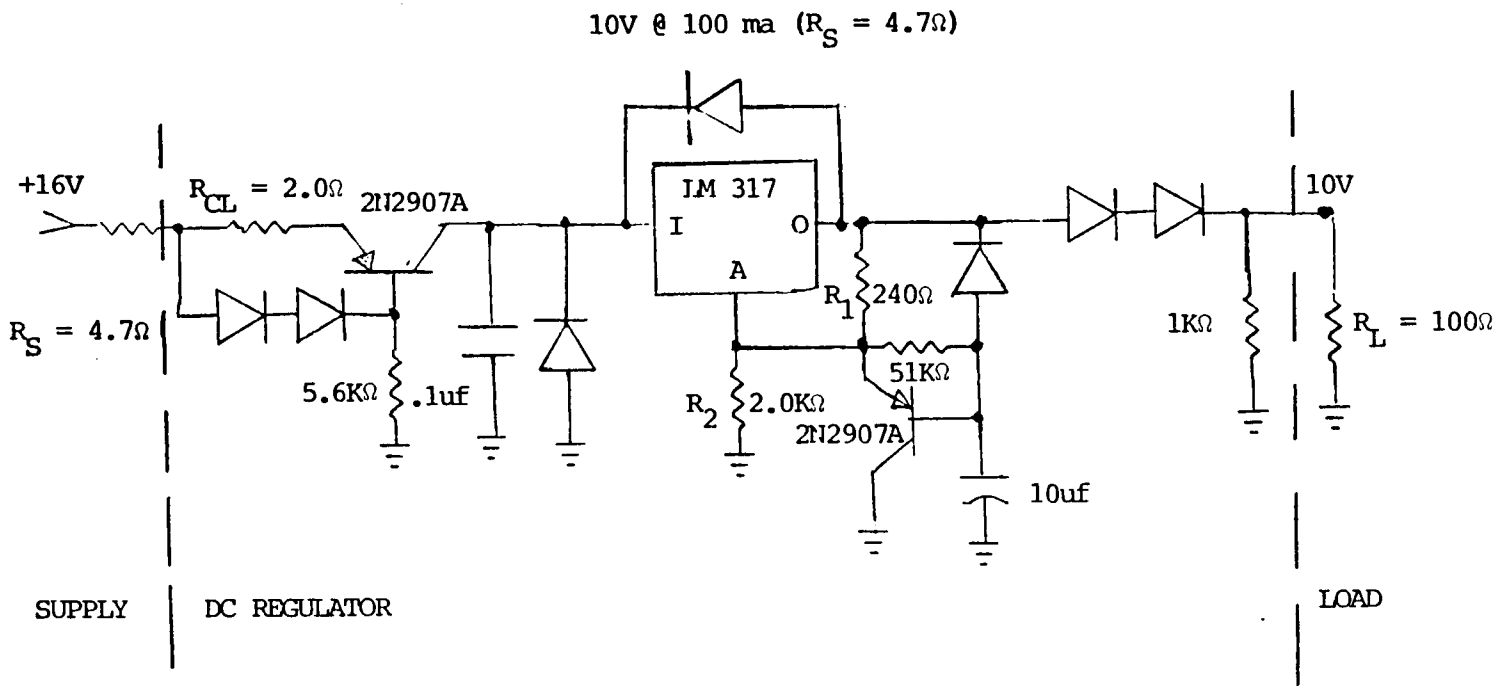


Figure 7-2

NEGATIVE VOLTAGE REGULATOR

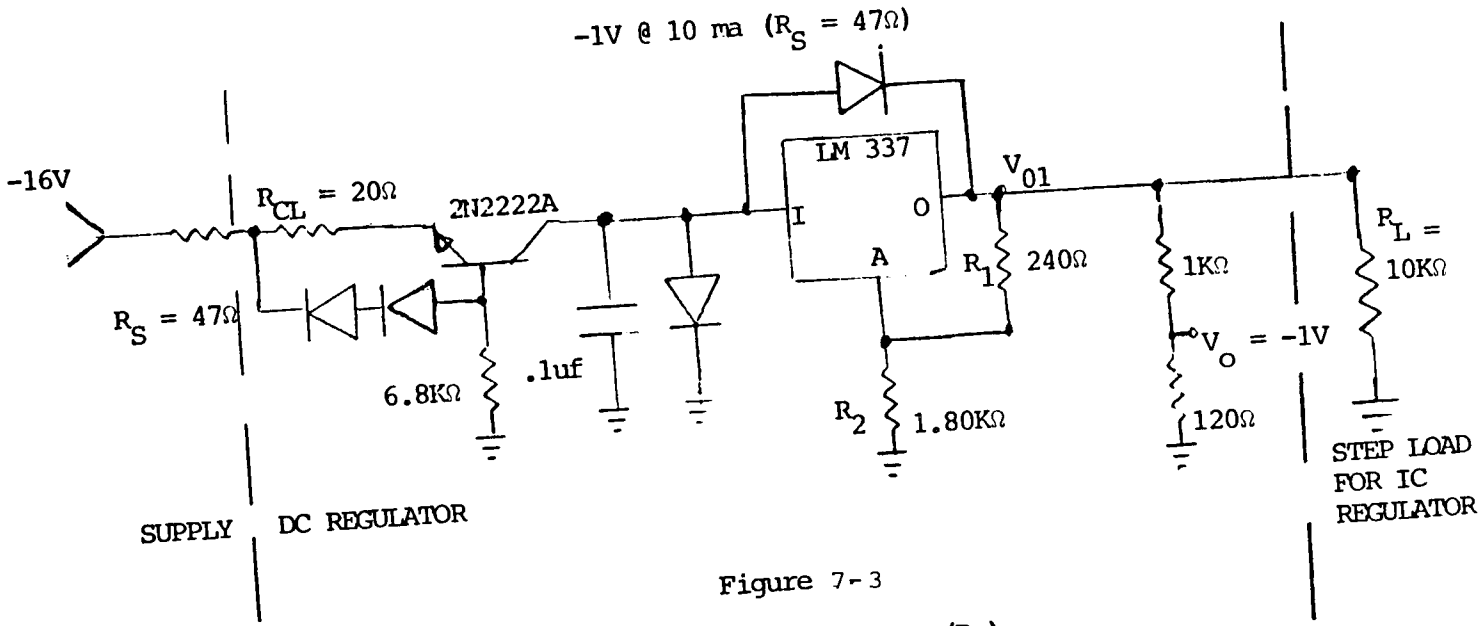


Figure 7-3

Negative Regulator Equation = $V_{01} = -1.25\ (1 + R_2/R_1)$

current levels. Figures 7-1 and 7-2 show the positive regulators and Figure 7-3 shows the negative regulator as they were breadboarded.

The positive regulators have a slow turn on circuit (the 2N2907 at the output side of the LM317 regulator) which allows the negative gate bias voltages to stabilize before the drain voltage powers up. The positive regulator ICs give approximately a one volt step output at turn on, independent of the slow turn on circuitry. The output diodes in the positive regulators insure that the overall regulator's output is kept at zero volts at turn on and then slowly rises to the desired value. This prevents any possible burn outs at turn on.

The transistor at the input side of each regulator IC (LM317/337) and the two diodes which are in parallel with the current limiting resistor, R_{cl}, limit the initial current surge at turn on to less than twice the nominal operating current. The diode immediately before the regulator IC provides reverse polarity protection in conjunction with the current limiting transistor.

A thermistor will be added to the negative regulator to provide gain stabilization over temperature. The thermistor network will be made out of R1 and R2. This gain stabilization will make it easier to meet the intercept and compression point requirements on the overall receiver. Each regulator was tested over temperature and performed nominally.

One resistor will be a select at test resistor. That resistor is R_{cl}, and its value depends on the I-V (current-voltage) relationships of the two input current limiting diodes. Its value is selected to give a turn on surge current to nominal current ratio of approximately 1.5:1. This leaves a +/- 0.5 margin for temperature variations. The thermistor (gain compensation) circuitry may require a select at test resistor, also. A potentiometer will be used for each unique FET drain voltage and for each FET gate bias.

8.0 IMPACTS ON POC RECEIVER DESIGN

The POC Receiver's performance using the measured breadboard data for all but the LNA was predicted and is shown in Figure 8-1. Data for the LNA's performance was taken from a Super-Compact prediction based on the replacement HEMT FET (NE 202) from NEC. The receiver analyzed consisted of an external (waveguide) input circulator, four stage HEMT LNA, one balanced RFA, RF filter, IRM, Hybrid/BSF, and an IF amplifier. The receiver's performance was analyzed at 18, 19 and 20 GHz. In all but the 18 GHz case, all specifications were met. The only

PREDICTED 20 GHz RECEIVER PERFORMANCE

BASED ON BREADBOARD DATA & NEW 1/3 um HEMT

PERFORMANCE OVER TEMPERATURE — 18 GHz DATA
****

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	SPECIFICATIONS (-30 oC < TA < +75 oC) GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	36.3	47.3	1.92	160.8	-32.9	30.0	3.5	-30.0
-25.0	35.7	46.7	2.21	192.0	-31.9	30.0	3.5	-30.0
0.0	35.1	46.1	2.50	226.0	-31.0	30.0	3.5	-30.0
25.0	34.5	45.5	2.81	263.3	-30.1	30.0	3.5	-30.0
50.0	33.9	44.9	3.11	304.0	-29.3	30.0	3.5	-30.0
75.0	33.3	44.3	3.43	348.6	-28.5	30.0	3.5	-30.0
100.0	32.7	43.7	3.75	397.5	-27.7	30.0	3.5	-30.0

PERFORMANCE OVER TEMPERATURE — 19 GHz DATA
****

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	SPECIFICATIONS (-30 oC < TA < +75 oC) GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	35.3	46.8	1.92	161.2	-31.3	30.0	3.5	-30.0
-25.0	34.7	46.2	2.21	192.5	-30.3	30.0	3.5	-30.0
0.0	34.1	45.6	2.51	226.6	-29.5	30.0	3.5	-30.0
25.0	33.5	45.0	2.81	264.0	-28.6	30.0	3.5	-30.0
50.0	32.9	44.4	3.12	304.8	-27.8	30.0	3.5	-30.0
75.0	32.3	43.8	3.43	349.4	-27.0	30.0	3.5	-30.0
100.0	31.7	43.2	3.75	398.3	-26.2	30.0	3.5	-30.0

PERFORMANCE OVER TEMPERATURE — 20 GHz DATA
****

TEMP (oC)	GMIN (dB)	GMAX (dB)	NF & Te NF (dB)	Te (oK)	IPI3 (dBm)	SPECIFICATIONS (-30 oC < TA < +75 oC) GAIN MIN (dB)	NF (dB)	IPI3 (dBm)
-50.0	33.3	43.8	1.94	162.8	-28.9	30.0	3.5	-30.0
-25.0	32.7	43.2	2.23	194.5	-27.9	30.0	3.5	-30.0
0.0	32.1	42.6	2.53	229.3	-26.9	30.0	3.5	-30.0
25.0	31.5	42.0	2.84	267.3	-26.0	30.0	3.5	-30.0
50.0	30.9	41.4	3.15	308.9	-25.1	30.0	3.5	-30.0
75.0	30.3	40.8	3.47	354.5	-24.2	30.0	3.5	-30.0
100.0	29.7	40.2	3.79	404.4	-23.4	30.0	3.5	-30.0

4 STAGE LNA AND BB MMICS MEET SPEC

FIGURE 8-1

exception was for intercept (compression) point at 18 GHz and then only at low temperatures. The analysis did not include the gain compensation circuit which is to be designed during the final receiver design, but as can be seen in the data of Figure 8-1, not much compensation will be required to be fully compliant.

Based on the predicted overall receiver performance being compliant with the NASA-Lewis specifications (when the gain compensation circuit is added), no additional MMIC design iterations will be required. The MMICs can be and have room to be improved, but their improvement is not required for successful POC receiver integration and test. It would, however, be prudent to pursue a design iteration of the MMICs as well as fabricate a few MMICs of the identical design to verify that high volume production (multiple wafers fabricated at different times) is a reality and to obtain optimum circuit performance.

NASA LEWIS RESEARCH CENTER

20 GHz RECEIVER

PROOF OF CONCEPT TEST

AND ANALYSIS REPORT

CONTRACT NAS3-24244

HARRIS CORPORATION GOVERNMENT COMMUNICATION SYSTEMS DIVISION
P.O. BOX 91000, MELBOURNE, FLORIDA 32902 (407) 729-2222

CONTENTS

1.0 INTRODUCTION

This report will present the work done on Task VI (Proof of Concept Test and Analysis) of the NASA 20 GHz Receiver Program sponsored by the NASA-Lewis Research Center in Cleveland, Ohio. The test procedure was generated during Task III (POC Plans and Specs),and updated during Task IV (POC Design) and Task V (POC Fab). Testing was done at -30°C, 25°C, and 75°C on the three receivers for many of the tests. The body of the report will present the data in graphical form and show diagrams of the test setups. The raw test data for the receivers is available in the appendix of this report, as is the test procedure used.

A model of the receiver was set up using data from the components as measured during Task V, and this model shows agreement with the measured performance. This model will be used for analysis that will show what changes can improve future receiver performance. POC receiver failures will be reported, as well as the modifications made to fix them. Recommendations for design modifications for production and follow-on technology development will be presented.

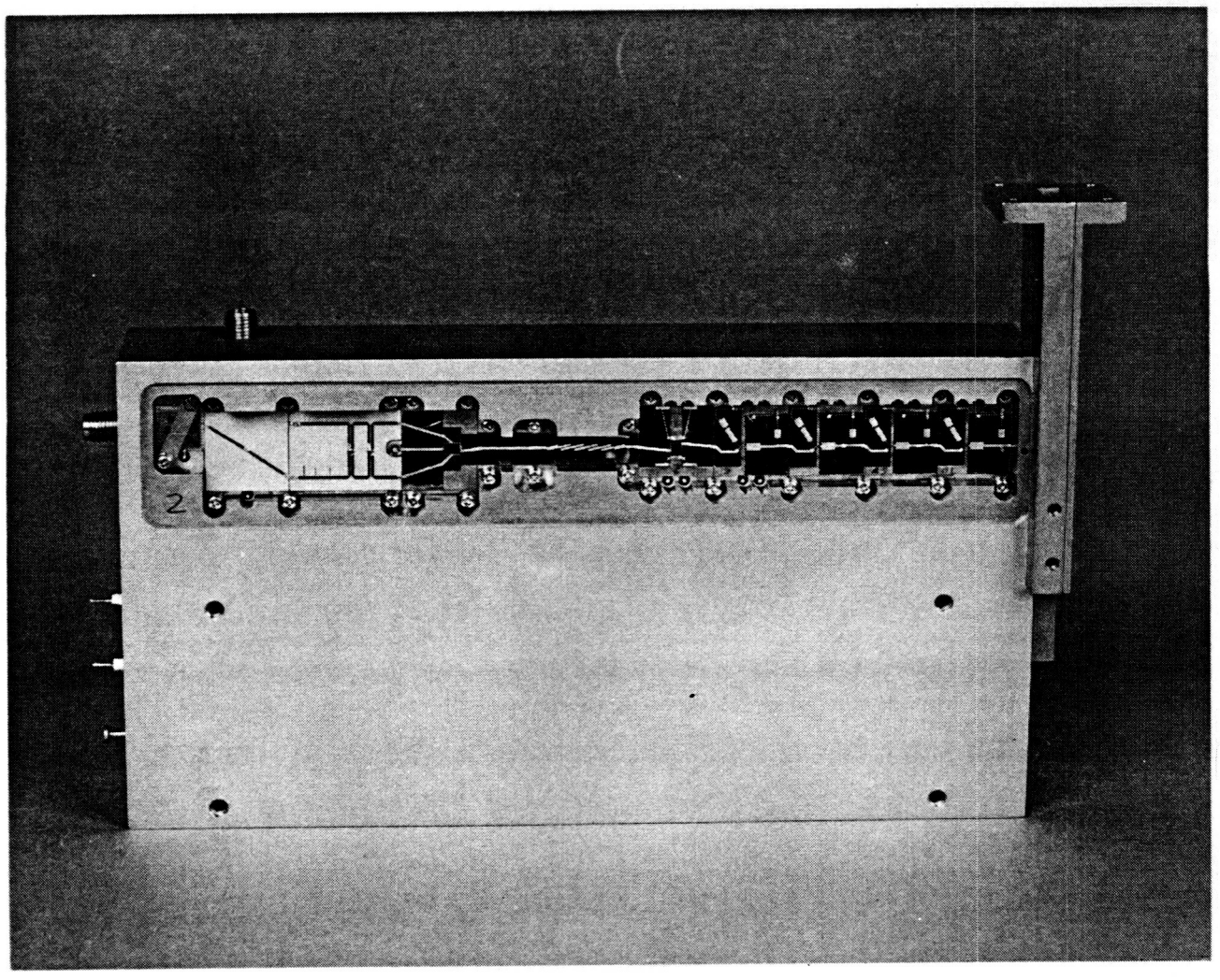


FIGURE 2-19 20 GHz RECEIVER MODULE WITH RF CAVITY EXPOSED

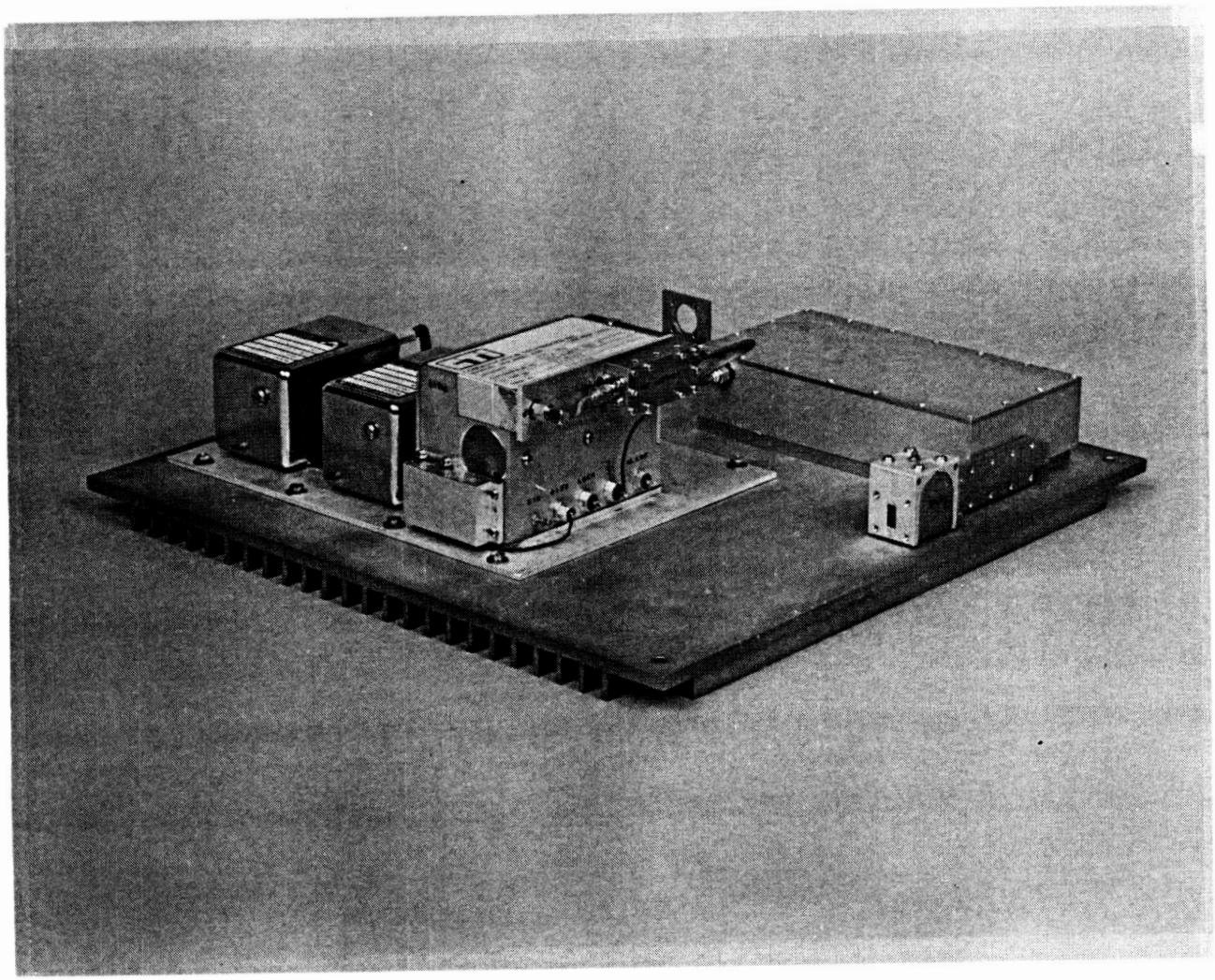


FIGURE 2-18 20 GHz RECEIVER TOP LEVEL ASSEMBLY

2.0 TEMPERATURE TEST DATA

This section contains POC receiver data over temperature for the following: Noise Figure, Gain, Gain Ripple (150 MHz), Gain Slope (10 MHz), and Input Third Order Intercept Point. The data is presented graphically on a parameter by parameter basis, with the specifications shown on the graphs. Data was taken at -30°C, 25°C, and 75°C.

Figure 2-1 shows the test setup used for noise figure measurements. The measurement system is calibrated at the IF frequencies of the measured subband, and the device is inserted. The spot ENR (Equivalent Noise Ratio) function of the HP8970A noise figure meter is used to enter the actual ENR of the noise source used in the measurement at the RF frequency. Special functions of the noise figure meter also allow compensation for the interconnect cables and waveguide required to send signals in and out of the temperature chamber.

Figure 2-2 shows the Noise Figure over temperature for the frequencies called out in the specification (19.385 to 20.081 GHz). Receiver one had the best high temperature noise figure (5.3 dB max). Receiver two offers the best ambient noise figure (4.2 dB max). Surprisingly, the noise figure for this receiver does not appreciably change at cold temperature. This may be due to a mechanical change due to package contraction, or by noise generated by an out of band oscillation. Receiver three offers the poorest overall noise figure performance (5.99 dB maximum).

Figure 2-3 shows the setup used for measuring gain, gain ripple (150 MHz), and gain slope (10 MHz). A Hewlett-Packard BASIC program was written to perform the calibration and measurement using 10 MHz frequency intervals, control the RF and LO sources, compute the worst case ripple and slope over each band segment, print out the results, and store the data on disk. The low pass filter is used to reject the wide band noise and local oscillator leakage that the power meter would measure. The set at test pad is used to keep the measured power within the range of the power head. The program allows compensation for this pad. It also allows compensation for measured inaccuracies of the local oscillator frequency. A hard copy of the BASIC program is provided in the appendix.

Figure 2-4 shows the data plots for the three receivers. On receiver one, the gain variation was about 10 dB different from ambient at the temperature extremes. There was an oscillation at 16.8 GHz in this receiver, which was cured by attaching absorber material to the sidewalls of the RF cavity. On receiver number two, the gain peaks at 18.5 and 19.1 GHz are especially prominent at cold temperature, where they almost reach 50 dB. These peaks are probably the result of high gain induced by a cavity resonance. The gain does not get high enough for the circuit to oscillate, so performance is not affected at other frequencies.

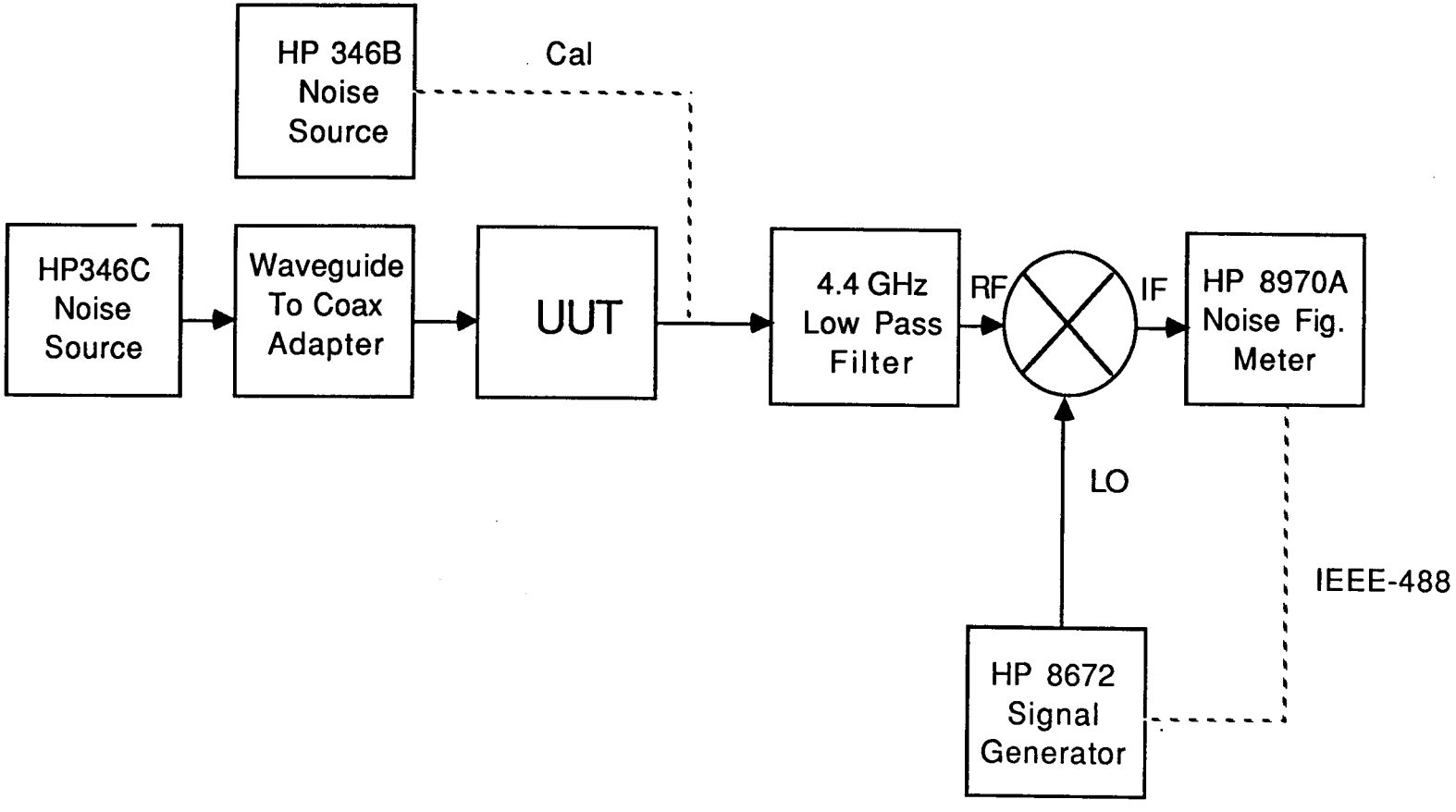


Figure 2-1 Noise Figure Test Setup

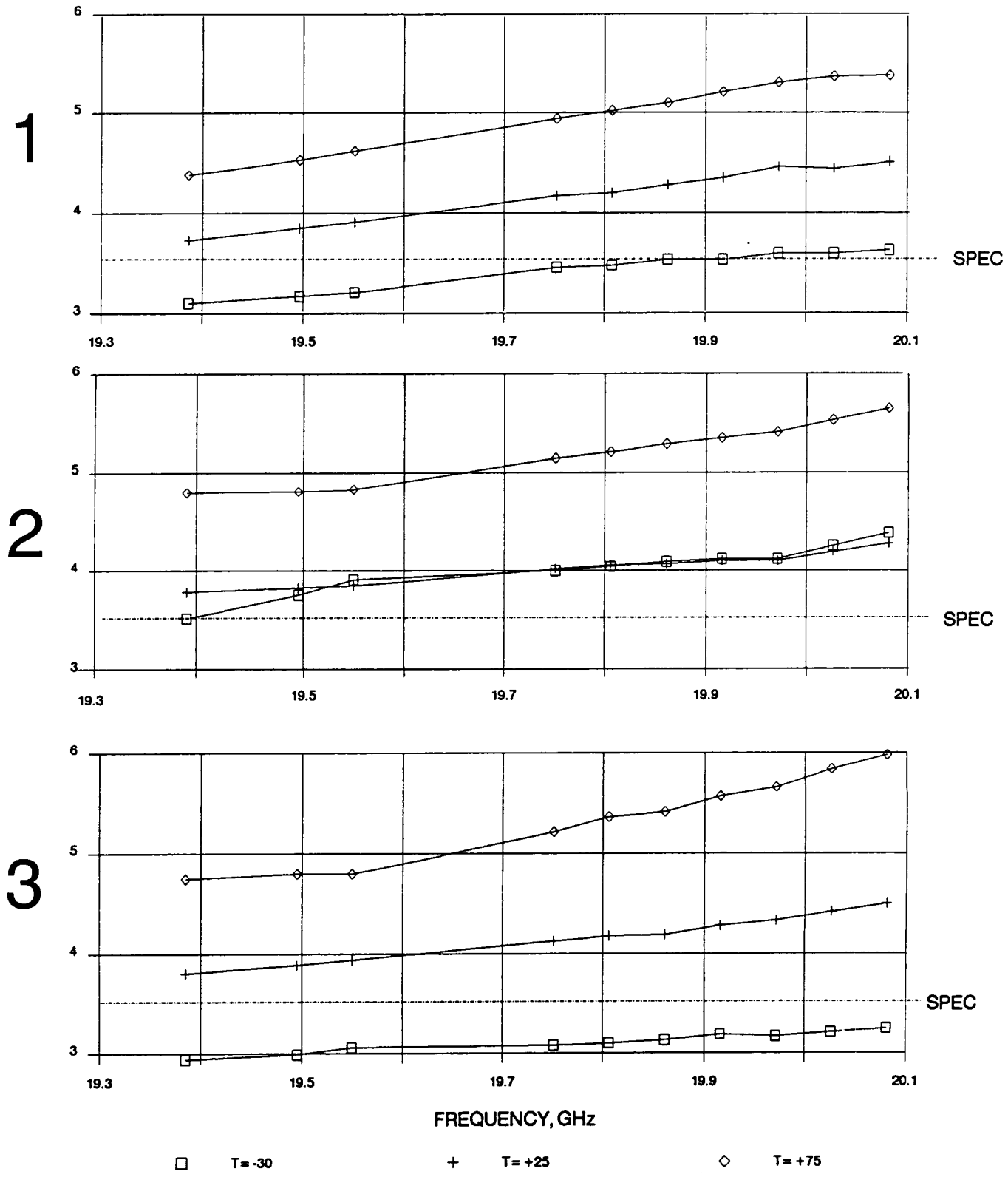


FIGURE 2-2 NOISE FIGURE OVER TEMPERATURE

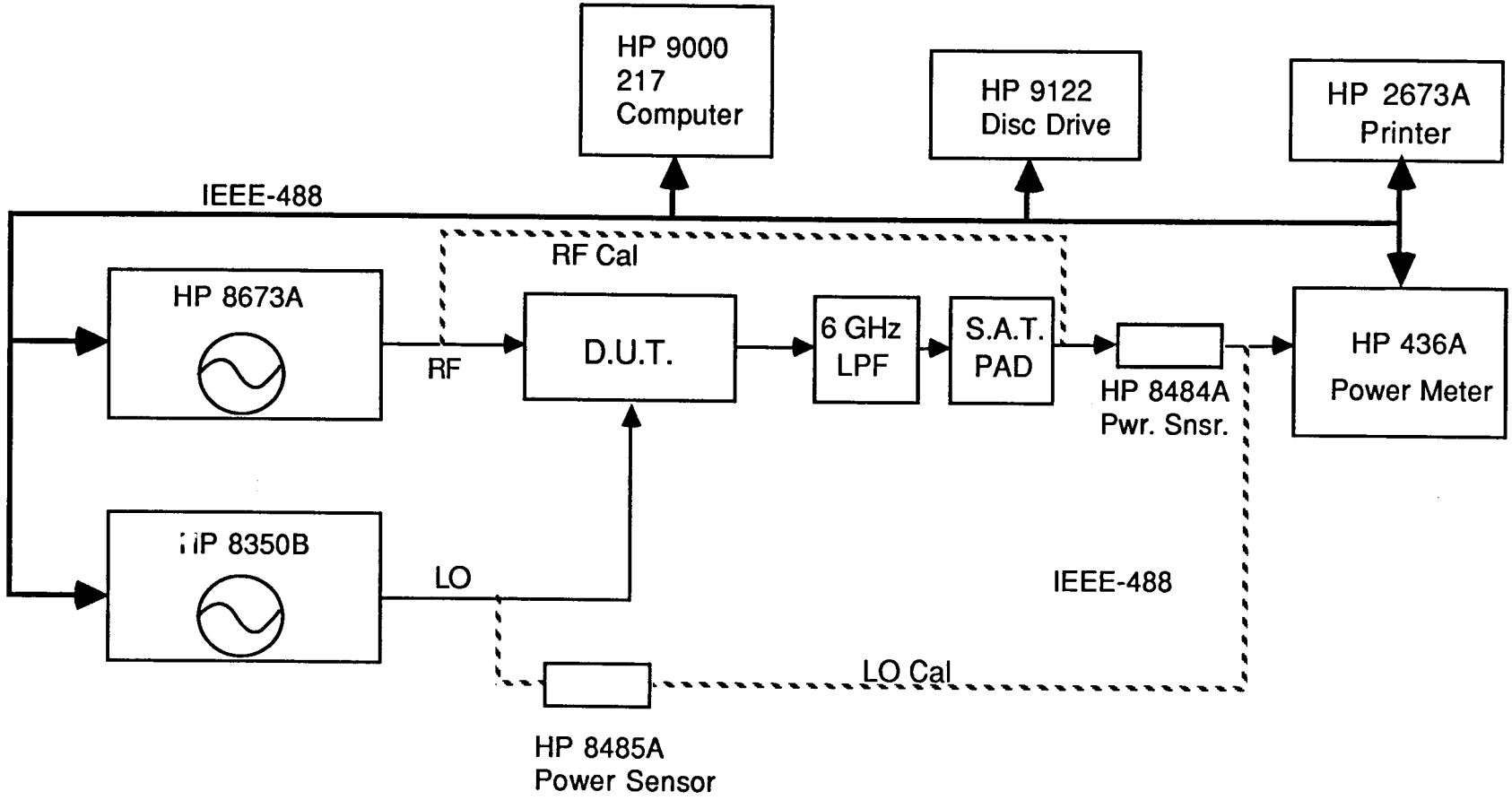


Figure 2-3 RF/IF Gain Test Setup

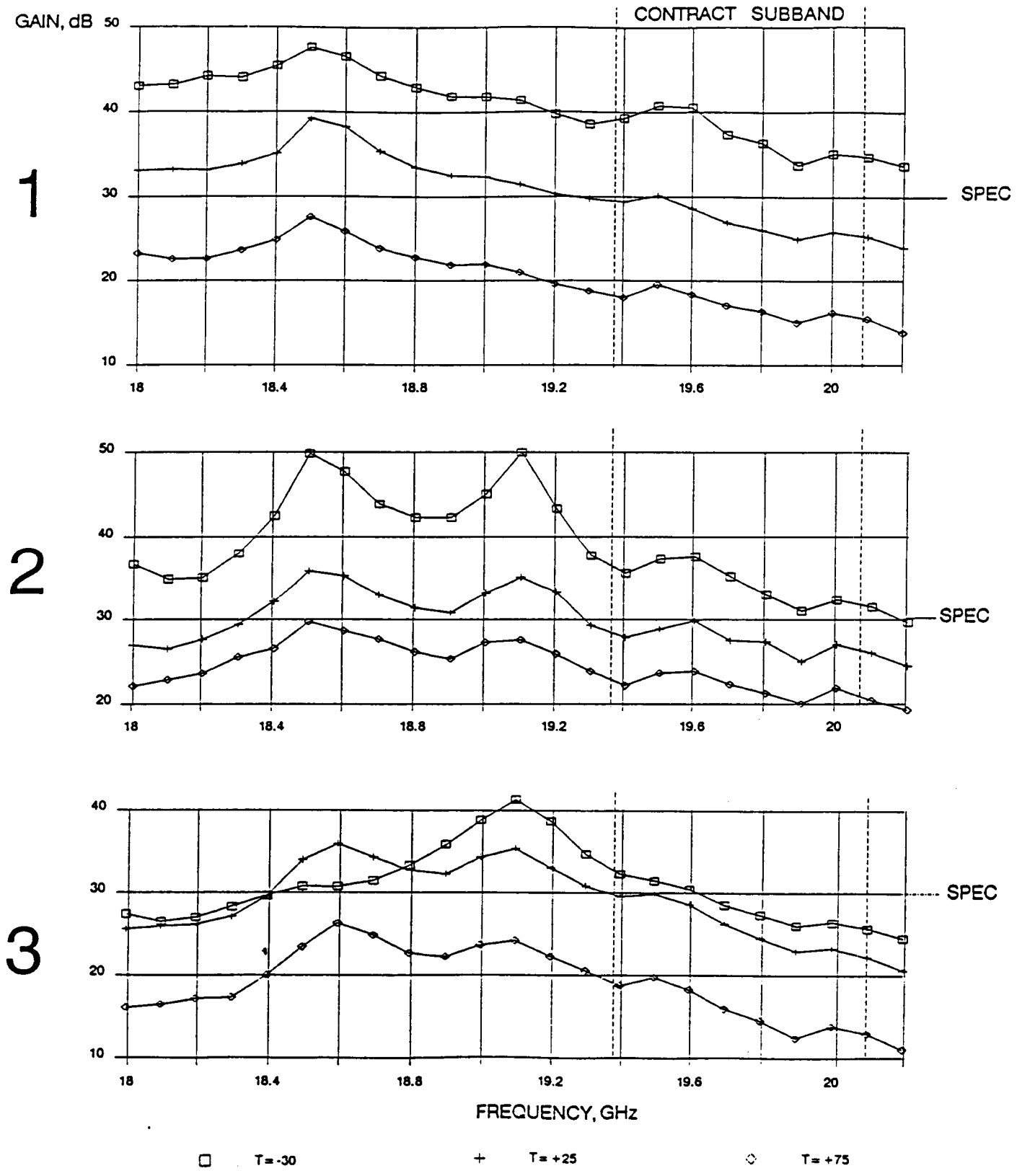


FIGURE 2-4 GAIN OVER TEMPERATURE

Receiver three offers the least performance of the three in terms of gain and has a gain peak at 19.1 GHz like receiver two.

Figure 2-5 shows the gain ripple for five subbands 500 MHz wide. The gain measurement system measures gain every 10 MHz, and computes the maximum change over 150 MHz. The worst case ripple is displayed on the bar chart. All three of the receivers have a gain peak around 18.5 GHz, and also have a good amount of ripple because of it. The highest frequency band, which is centered at 20.2 GHz, actually goes out of our spec band by 200 MHz, and thus has additional gain roll off. Receiver one has a slight gain peak at 19.5 GHz, causing it to exceed the spec at low temperature. Receiver two has the two high gain peaks described earlier that cause a great amount of ripple. Receiver three has gain peaks at 19.1 and 19.5 GHz that cause it to exceed spec slightly at all three temperatures. Figure 2-6 shows the receiver gains with a straight line plotted at a 1.5 dB per 150 MHz to graphically show the ripple in the contract subband of 19.385 to 20.081 GHz.

Figure 2-7 shows the gain slope for five subbands 500 MHz wide. The gain measurement system measures gain every 10 MHz, and computes the maximum change over 10 MHz for each subband. Receiver one slope exceeds the spec by 0.2 dB at cold temperature. Receiver two slope exceeds the spec in many instances due to the gain peaks at 18.5 and 19.1 GHz. It also has a roll off in the 500 MHZ subband that is out of our design band. Receiver three exceeds the spec mostly at high temperatures, where the gain rolls off significantly.

Figure 2-8 shows the setup used for measuring input third order intercept point. The setup actually shows the output spectrum from which the output intercept point can be calculated. The gain, which is previously measured, is subtracted from the output intercept point to determine the input intercept point.

Figure 2-9 shows the intercept point plotted over temperature. The only variance from the -30 dBm specification was on receiver two at 18.7 and 18.9 GHz at -30^{o}C. This is frequency where the large gain peak was observed at that temperature.

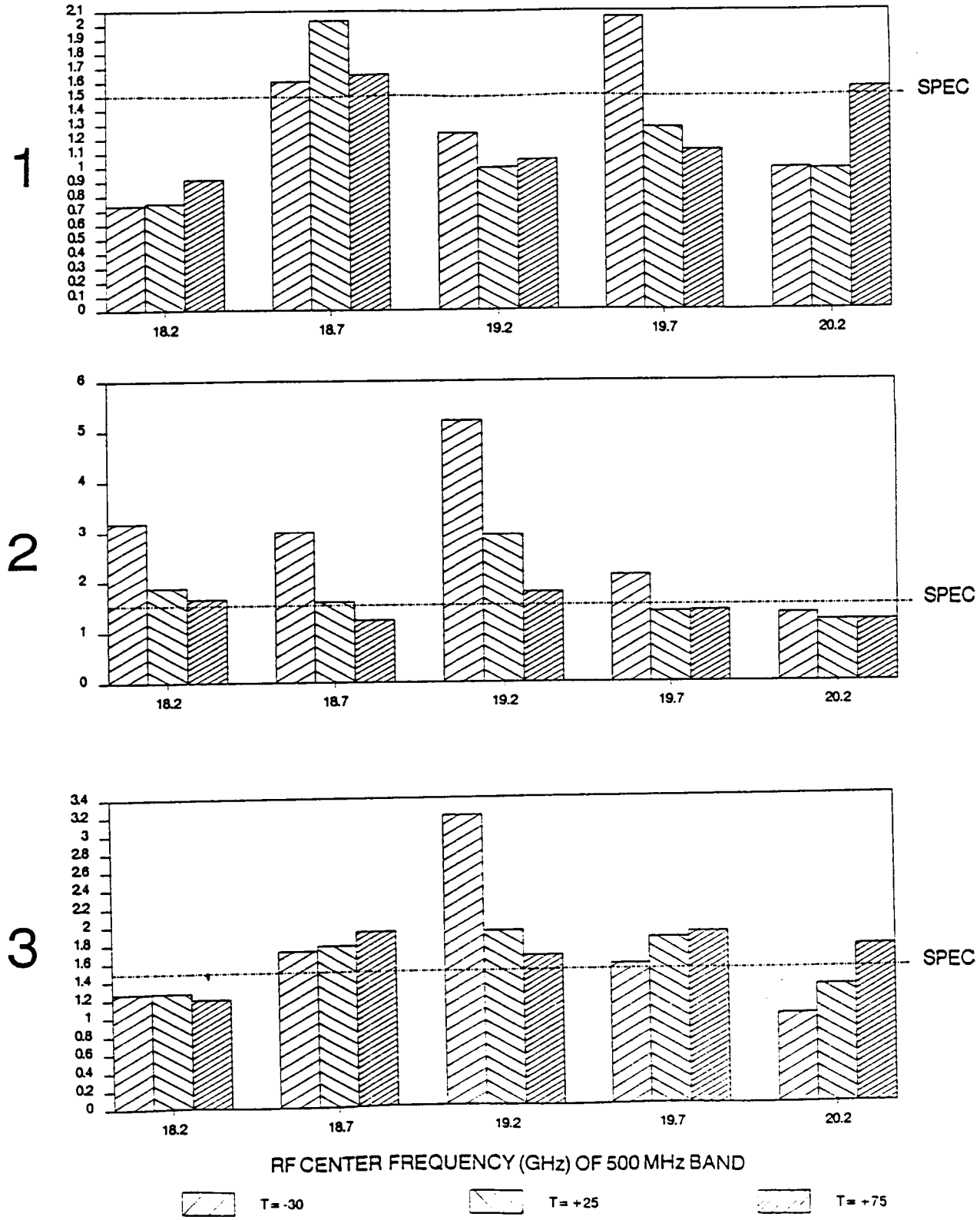


FIGURE 2-5 GAIN RIPPLE OVER TEMPERATURE

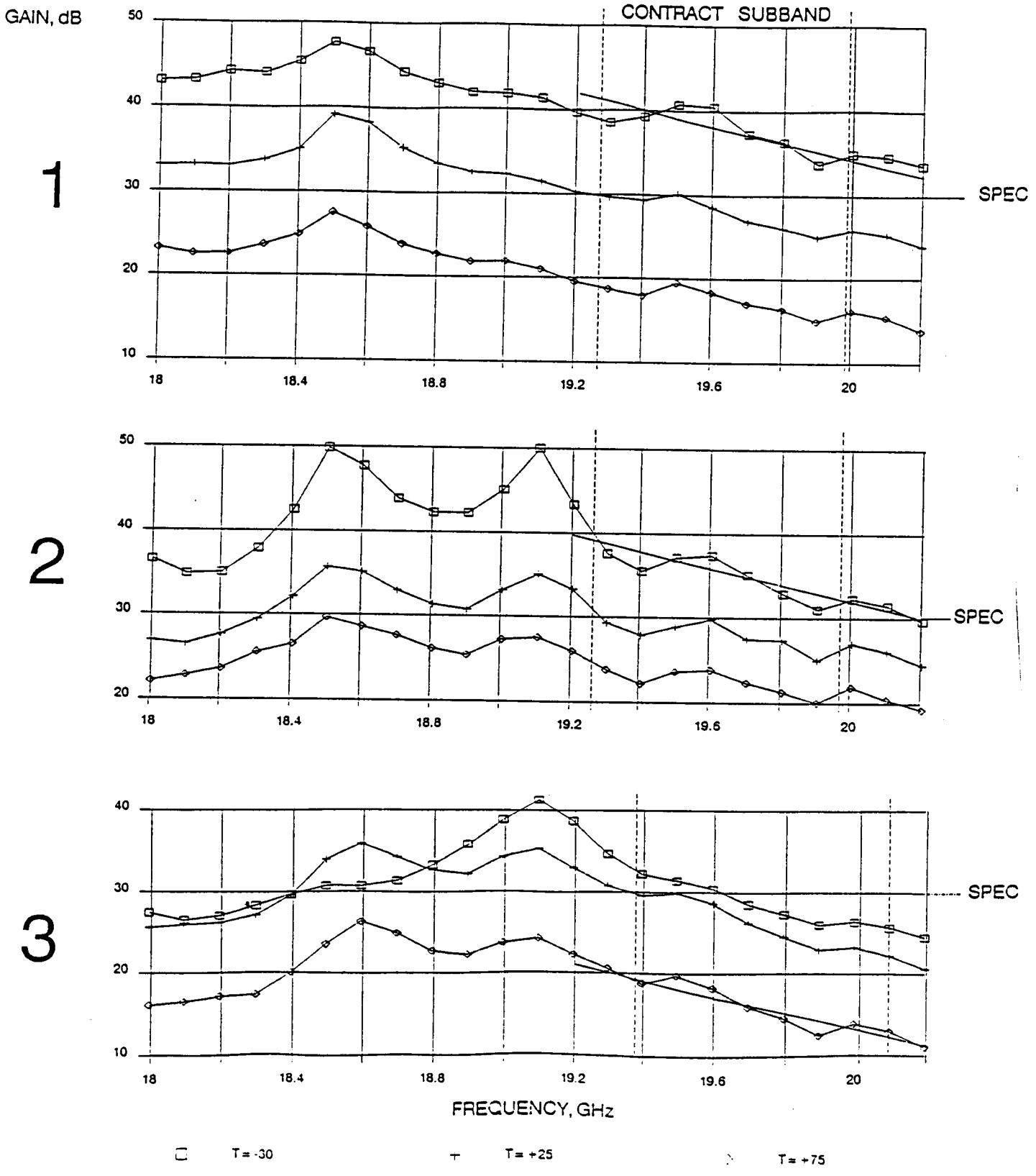


FIGURE 2-6 GAIN RIPPLE iN CONTRACT SUBBAND

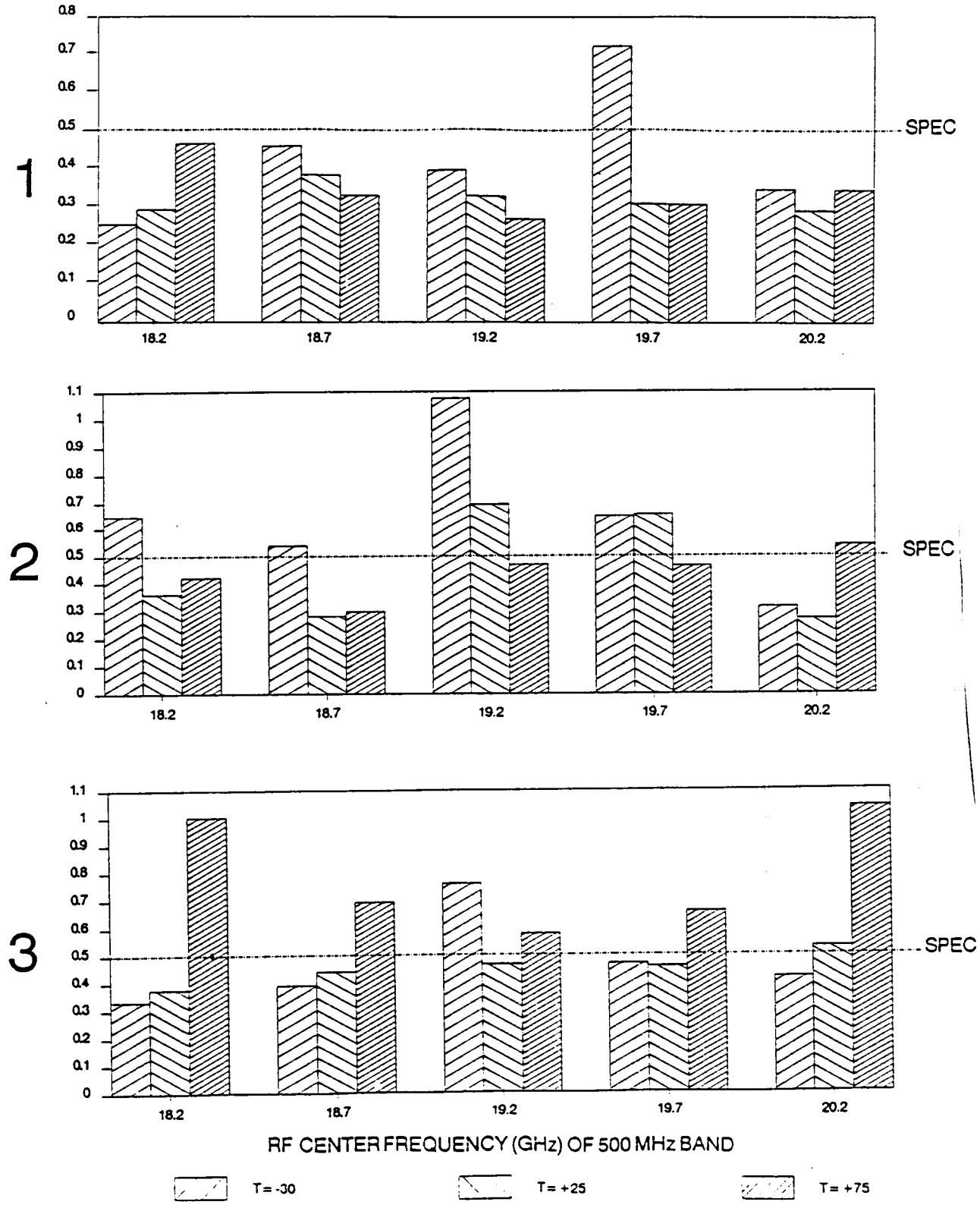


FIGURE 2-7 GAIN SLOPE OVER TEMPERATURE

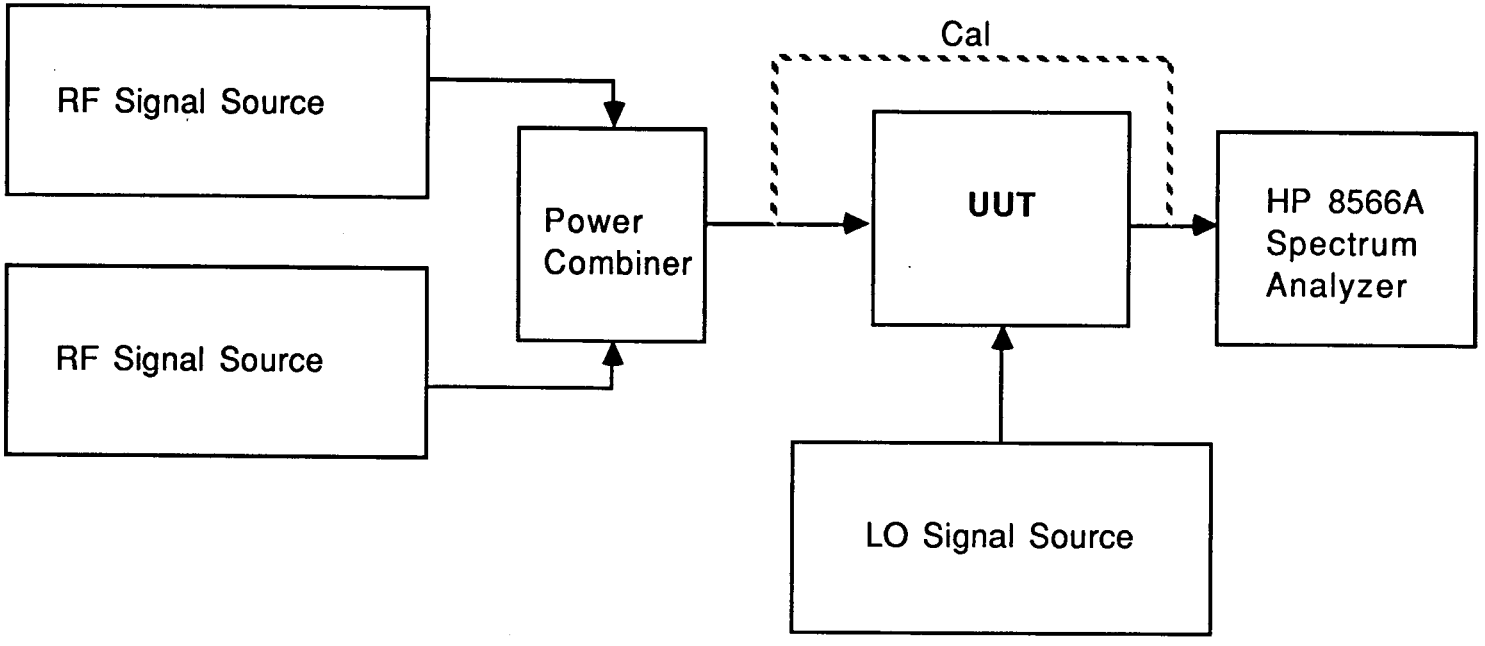


Figure 2-8 Third Order Intercept Point Test

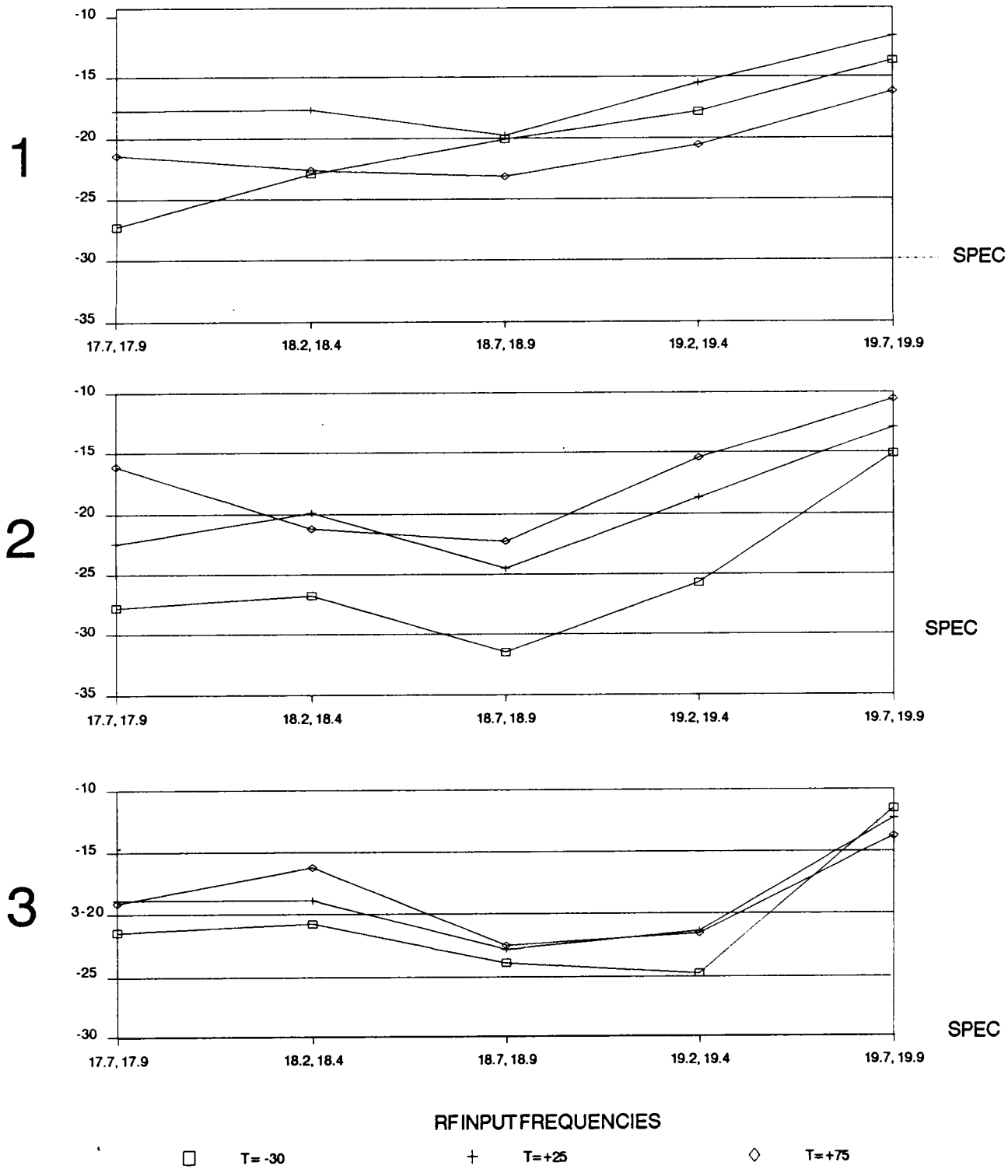


FIGURE 2-9 INPUT INTERCEPT POINT OVER TEMPERATURE

3.0 OTHER TEST DATA

In this section, the remainder of POC test data will be presented in a summary form, giving a general view of the receivers' performance. In most cases, worst case performance will be presented. The following tests will be reported:

1 dB Input Compression Point

Input and Output VSWR

Group Delay

AM/PM Conversion

Out of Band Rejection

Spurious Response

Image Rejection

Local Oscillator Phase Noise

Local Oscillator Frequency

Reverse Voltage

Inband Overdrive

Since an extensive third order intercept point test was conducted, and the 1 dB input compression point is generally 10 dB below the third order intercept, the compression point test was a spot check at 20 GHz at room temperature. The specification was -40 dBm minimum. The test setup was the same one use for the gain, gain ripple, and gain slope tests. The 1 dB compression points were:

Receiver 1: -19.6 dBm

Receiver 2: -18.6 dBm

Receiver 3: -17.6 dBm

Input and output VSWR was measured using the HP 8510 network analyzer. The input was measured with a WR-42 calibration. Because of the input circulator, the receivers meet the input VSWR specification always, including when the unit is turned off.

RF Input VSWR- 17.7- 20.2 GHz

Spec: 1.7:1
Max: 1.31:1

IF Output VSWR- 3.185- 3.540 GHz

Spec: 1.5:1
Max: 1.42:1

Figure 3-1 shows the setup used to measure group delay. The HP 8510 Port 1 signal is up converted, using the a sample of the receiver's LO, ensuring the signal will be down converted back to the same frequency. The 8510 is actually measuring the group delay of the up conversion and the receiver, but the up converter doesn't significantly affect the group delay because of its wide bandwidth. The specification was 5.0 nS peak-to-peak over 100 MHz. The maximum group delay measured was 2.61 nS peak-to-peak over 100 MHz. The group delay was measured over six segments of the RF band by varying the LO. When the LO was changed, the group delay changed very little, indicating the cause of it was in the IF portion of the receiver. The IF hybrid was probably the main factor because it had the least bandwidth of the IF components.

The AM/PM conversion test setup is shown in figure 3-2. A signal is AM modulated at the IF frequency and is up converted using a sample of the DUT LO. A second IF source is not modulated, and is locked to the same reference oscillator as the modulated source. The mixer after the receiver serves as a phase detector. To calibrate the phase detector, a CW signal is applied to the receiver. The oscilloscope display is a horizontal line, and the line stretcher in the LO path is varied until the DC voltage displayed is 0 VDC. This corresponds to a 90 degree phase difference between the mixer RF input (receiver output) and the mixer LO input. At this point, the mixer is a phase detector. The line stretcher is then changed 45 degrees, and the voltage change is divided by 45 to get the phase detector transfer function. the RF input source is AM modulated at 400 Hz with sidebands 25 dB down. This corresponds to a 1 dB change in amplitude. Our phase detector transfer function was quite low, and the output was generally 0.4 mV, which was about the width of the line on the oscilloscope display. The AM to PM conversion of the up converter is also included in the measurement, and its contribution is unknown. The receivers were measured at ambient temperature at 20 GHz with a power level of -60 dBm. The specification was 0.5 degrees/ dB. The measured AM to PM conversions were:

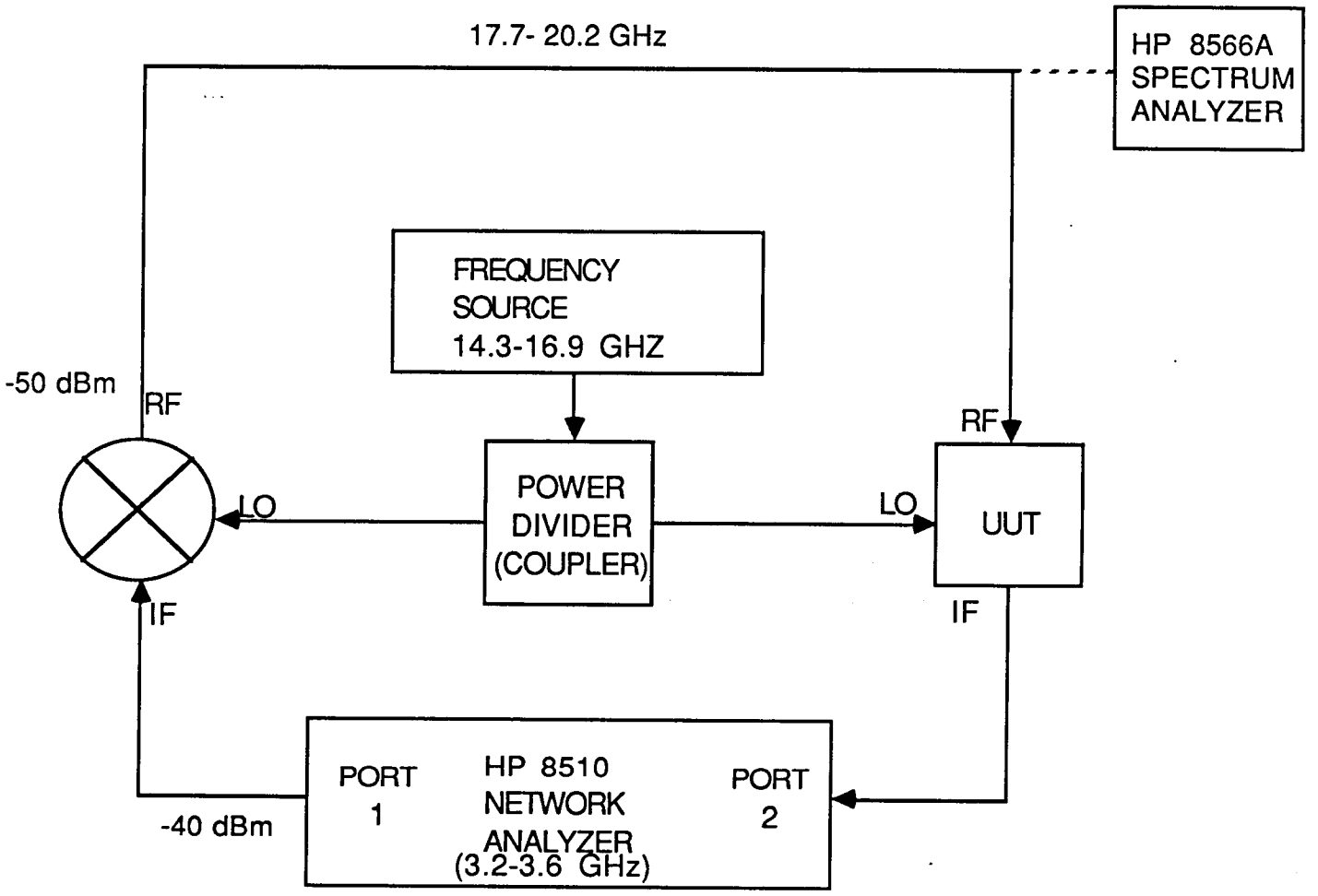


Figure 3-1 Group Delay Set-Up

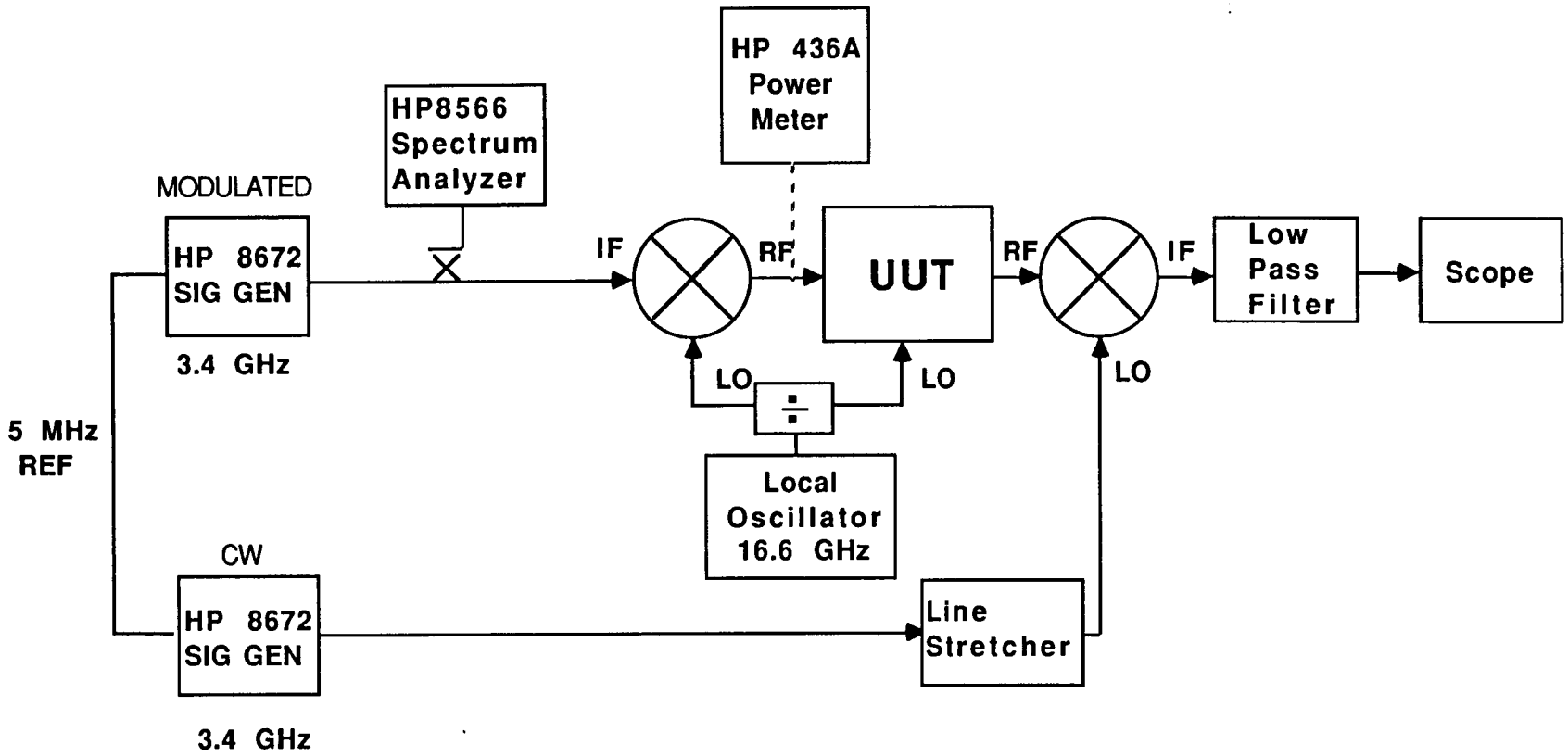


Figure 3-2 AM-PM Conversion Set-Up

Receiver 1: 1.7 degrees/ dB

Receiver 1: 2.0 degrees/ dB

Receiver 3: 1.6 degrees/ dB

Figure 3-3 shows the setup used for measurement of image rejection, in-band induced spurs, and out of band induced spurs. All of these were tested at -30°C, 25°C, and 75°C.

The image reject specification was 40 dB. No evidence of the image signal (13.5 GHz) was found in any of the receivers. The measurement was limited by the spectrum analyzer noise floor to 60 dB image rejection. The excellent image rejection can be attributed to the RF filter performance and the image frequency being below waveguide cutoff of 14.05 GHz.

Shown below are the worst case spurious response results for out of band signals. The M and N columns indicates the RF and LO multipliers, respectively. The specification for inband and out of band spurs is -45 dBc.

M	N	RF (GHz)	LO (GHz)	SPUR (dBc)
-2	2	15.1	16.8	-37.0
3	-2	12.4	16.8	-43.1
-3	3	15.7	16.8	-46.1
-1	2	25.0	14.3	-62.9
2	-3	23.1	14.3	-67.4
-2	3	22.2	15.9	-66.2

The worst case in-band spurious response is shown below.

M	N	RF (GHz)	LO (GHz)	SPUR (dBc)
2	-2	17.7	16.0	-31.3
3	-3	17.8	16.7	-52.8
-3	4	17.9	14.3	-67.4
4	-4	17.7	16.85	-61.0
4	-5	18.7	14.3	-67.4
5	-5	17.7	17.0	-64.0

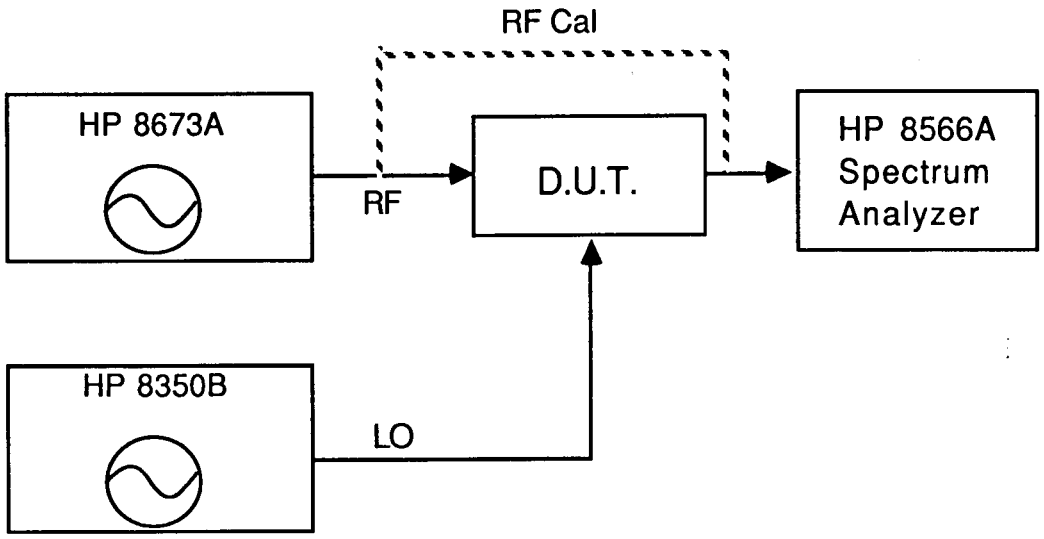


FIGURE 3-3 OUT OF BAND REJECTION AND SPURIOUS RESPONSE TEST

In general, the worst spurious response was observed at 75°C, indicating that the problem was in the mixer, and was caused by the LO. The three out of spec data spurs each involved the second harmonic of the LO. This out of spec spurious performance is probably caused by the high LO drive required to operate the mixer (20 dBm). As temperature rises the amplifier gain drops off, and the spurious response should improve by 1 dB for each 1 dB drop in the signal strength. Because the opposite happens, we can assume the problem is in the mixer.

The phase noise tests for the local oscillator were done by the vendor, Communications Techniques of Whippany, NJ. Shown below are the various offsets, specifications, and worst case phase noise performance.

OFFSET (FREQ)	SPEC. dBc	WORST CASE dBc
100 Hz	-56	-66
1 kHz	-78	-85
10 kHz	-80	-82
1 MHz	-100	-104

The local oscillator output frequency was measured over temperature. The specification calls for no more than 40 kHz deviation from the specified frequency. The maximum deviation was -7.84 kHz. The maximum change of any oscillator's frequency over temperature was 1.99 kHz.

The original local oscillator specification called for DC supply voltage of 15 V, +/- 1.5 V, which was consistent with the overall receiver specification. The vendor had problems with oscillator performance at -30oC with 13.5 VDC, and asked for relief in the form of the voltage tolerance changing to +/- 0.5 VDC. This relief was granted to avoid further program delay.

The three POC receivers did not suffer any degradation in performance after a 0 dBm 20 GHz CW input or a reverse DC voltage hookup. The receiver is provided with a non-reversible DC jack, the Burndy BT00E83P. The matching plug part number is BT06E83S.

4.0 ANALYSIS OF MEASURED DATA

In this section, the performance of one of the receivers (number two) will be analyzed by taking the data for the various components as taken during Task V (POC Fabrication) at room temperature at 20 GHz and doing a cascaded analysis using a LOTUS spread sheet to simulate receiver performance. The model has a reasonable correlation with the measured performance of the receiver. Some of the values used are estimates that seem to be held up by the model. These components are: input W/G transition, RF Attenuator, and DC block. The RF filter data was taken from the breadboard task, and the IFA data from the Harris internal IR&D project.

We had a problem with the noise sources used in our noise figure measurements of the receiver and the components. A noise source is imprinted with an ENR (Excess Noise Ratio) corresponding to some frequencies in the band. It is assumed that interpolation can be used for frequencies between those specified. Any error in the published ENR causes an identical error in the measured noise figure. During the breadboard and receiver fabrication phases of the contract, we used a waveguide noise source from MSC. We received a new HP 346C noise source at the end of Task V, after the receivers had been assembled. This new source showed higher measurements than the MSC. At the Task V review, we reported both results, stating that we thought the HP results accurate because of the newness of the source and its calibration. Since then, we rented another HP 346C source, and the results agreed with the other HP 346C, with a maximum deviation of .05 dB, which is well within the published accuracy of $\pm$ 0.2 dB.

Unfortunately, since the receivers were already assembled, we would have had to disassemble them to measure the components for noise figure with the new source. Therefore, the model of the performance is done using the data measured with the MSC noise source. It is assumed that the measurement errors are absolute. Despite the lack of accuracy in some of the data used in the analysis model, we will be able to show major factors in determining the receiver performance, and recommend changes that will enhance future iterations.

In Table 4-1, results are shown for measurements with both sources and the analysis model for room temperature at 20 GHz. The gain data shown here was taken by the noise figure meter, but the gain that was officially reported earlier was taken by the automated gain setup.

ROOM TEMPERATURE COMPARISON

	GAIN	NOISE FIGURE
HP MEASURED	27.84	4.2
MSC MEASURED	26.26	3.5
MODEL SIMULATION	25.8	3.5

TABLE 4-1

Table 4-2 displays the difference in gain and noise figure over temperature as measured, and as predicted by the analysis model. Receiver two had one unusual phenomenon- the noise figure did not go down at reduced temperature. This may be attributed to a change in HEMT noise parameters, S-parameters, or mechanical changes in the aluminum housing. The noise figure did go down in the other two receivers, and the lower temperature delta from receiver one is presented. As the noise figure changes were slightly more than predicted, it appears that the temperature coefficient used for HEMTs was slightly low.

DELTAS FROM ROOM TEMPERATURE

	GAIN	NOISE FIGURE
POC MEASURED -30°C	6.04	-1.2
MODEL SIMULATION -30°C	4.4	-1.0
POC MEASURED -75°C	-4.98	1.3
MODEL SIMULATION -75°C	-5.0	0.9

TABLE 4-2

Table 4-3 shows the analysis model at room temperature, and shows the sensitivity of the components' performance on the receiver performance noise figure and intercept point. The model shows the input waveguide to microstrip connection to have 0.7 dB of loss, which directly affects the noise figure. This loss should be 0.2 to 0.3 dB. This transition was not tested or optimized, so this would be a good future development activity.

A reduction of LNA noise figure in the first or second stages would of course be beneficial. The sensitivity analysis shows that the third and fourth LNA stages can have I_{DS} optimized for

gain instead of noise figure for best results. Experience with aligning the receivers confirms this. A future design might optimize the third and fourth stage input matching for gain. In the current design, the LNA stages are identical, individually fabricated and tested, and are selected so that the best noise figures are in the first stages.

The effects of changes on the front end of the receiver are not surprising- one would expect the changes in gain and noise figure to affect receiver performance. What is more interesting is the effects of the back of the receiver. In the cascaded analysis, the IFA contribution raises the system noise figure by 0.3 dB. One would not expect this, as the front end normally would swamp out this contribution. A combination of low LNA gain and a mixer with high insertion loss leaves only 13.8 dB gain in front of the IFA, which has a 6.0 dB noise figure. The sensitivity analysis shows that the IFA noise figure raises the receiver noise figure .08 dB/ dB. We must provide more gain before the IFA. The sensitivity analysis shows that lowering the mixer conversion loss would lower the noise figure on a .08 dB/ dB basis (assuming the mixer noise figure also is reduced). This is significant because of the high MMIC mixer conversion loss (16 dB), and the commercial availability of far superior mixers (CL of 8 dB). Also, recent work has produced MMIC mixers with superior performance to the MIC mixers. This will be discussed further in the recommendations section. Because we bought the best HEMTs commercially available, it is doubtful that we could make up 8 dB of gain with an LNA redesign. The analysis also shows that the mixer loss contributes very little (0.1 dB) to the noise figure, it just allows later contributions. Therefore, an increase in LNA gain would be little more beneficial than reduced mixer conversion loss.

Table 4-4 is another cascaded analysis of the receiver as built with temperature results included. Table 4-5 is a similar analysis with a mixer with a conversion loss of 8 dB. With the new mixer, the noise figure improves by 0.4 dB at 25^{o}C and 0.6 dB at 75^{o}C. The greater improvement at 75^{o}C is to be expected because the lowered LNA gain at elevated temperatures allows even greater later stage noise figure contributions in the current receiver. The noise figure improvement is 0.1 dB at -30^{o}C.

NASA 20 GHz RECEIVER SENSITIVITY ANALYSIS

P IN = -60.0 dBm

#	ELEMENT	GAIN (dB)	NF (dB)	IPO (dBm)	GCAS (dB)	NFCAS (dB)	IPICAS (dBm)	POUT (dBm)
1	ISOLATOR	-0.2	0.2	100.0	-0.2	0.2	100.2	-60.2
2	W/G TRANS.	-0.7	0.7	100.0	-0.9	0.9	97.5	-60.9
3	LNA 1	6.5	1.7	15.0	5.6	2.6	9.4	-54.4
4	LNA 2	6.4	1.9	15.0	12.0	3.0	2.1	-48.0
5	LNA 3	6.3	1.8	15.0	18.3	3.1	-4.4	-41.7
6	LNA 4	5.9	1.9	15.0	24.2	3.1	-10.4	-35.8
7	RFA	8.0	7.1	23.0	32.2	3.1	-12.9	-27.8
8	RF FILTER	-2.0	2.0	100.0	30.2	3.1	-12.9	-29.8
9	RF ATTEN	-0.2	0.2	100.0	30.0	3.1	-12.9	-30.0
10	MIXER/HYBRID	-16.0	16.0	8.5	14.0	3.2	-13.6	-46.0
11	DC BLOCK	-0.2	0.2	100.0	13.8	3.2	-13.6	-46.2
12	IFA	12.0	6.0	23.0	25.8	3.5	-14.0	-34.2

S E N S I T I V I T I E S / D E L T A S

CASCADED EQUIVALENTS		D E L T A S	
GAIN eq =	25.8 dB	GAIN i =	-10.00 dB
NF eq =	3.45 dB	NF i =	-10.00 dB
IP IN eq =	-13.95 dBm	IP i =	-10.00 dBm

		*** S L O P E S (dB/dB) ****					*** D E L T A S (dB) ***			
#	ELEMENT	NFeq/ Gi	NFeq/ NFi	IPeq/ Gi	IPeq/ IPi	*	NF eq f(Gi)	NF eq f(NFi)	IP eq f(Gi)	IP eq f(IPi)
1	ISOLATOR	-0.53	0.47	-1.00	0.00	*	7.59	-2.41	10.00	-0.00
2	W/G TRANS.	-0.44	0.56	-1.00	0.00	*	6.99	-3.01	10.00	-0.00
3	LNA 1	-0.17	0.83	-1.00	0.00	*	4.03	-5.97	10.00	-0.18
4	LNA 2	-0.10	0.19	-1.00	0.02	*	2.79	-0.84	9.82	-0.72
5	LNA 3	-0.09	0.04	-0.98	0.09	*	2.48	-0.17	9.13	-2.49
6	LNA 4	-0.08	0.01	-0.89	0.33	*	2.40	-0.04	6.99	-6.04
7	RFA	-0.07	0.01	-0.55	0.33	*	2.23	-0.03	3.00	-6.04
8	RF FILTER	-0.07	0.00	-0.22	0.00	*	2.23	-0.00	0.96	-0.00
9	RF ATTEN	-0.07	0.00	-0.22	0.00	*	2.23	-0.00	0.96	-0.00
10	MIXER/HYBRI	-0.06	0.02	-0.22	0.14	*	1.80	-0.07	0.96	-3.59
11	DC BLOCK	-0.06	0.02	-0.08	0.00	*	1.78	-0.07	0.31	-0.00
12	IFA	0.00	0.08	-0.08	0.08	*	0.00	-0.30	0.31	-2.28

TABLE 4-3

NASA 20 GHz RECEIVER CASCADED TEMPERATURE ANALYSIS WITH MMIC MIXER

		ELEMENT INPUT VALUES						CASCADED OUTPUT VALUES				
		G A I N		INTERCEPT PTS		NF, TEMP DATA		CASC. ELEMENT VALUES AT Ta				
	ELEMENT DESCRIPTION	GAIN (dB)	KG (dB/°C)	IPO3 (dBm)	KIPO (dB/°C)	NF (dB)	TA/T1 EXP	GAIN (dB)	IPO3 (dBm)	NF & (dB)	Te (°K)	IPI3 (dBm)
1	ISOLATOR	-0.2	0.000	100.0	0.000	0.2	1.0	-0.2	100.0	0.2	13.7	100.2
2	W/G TRANSITION	-0.7	0.000	100.0	0.000	0.7	1.0	-0.9	96.6	0.9	66.8	97.5
3	HEMT 1	6.5	-0.010	15.0	0.000	1.7	1.7	5.6	15.0	2.6	231.7	9.4
4	HEMT 2	6.4	-0.010	15.0	0.000	1.9	1.7	12.0	14.1	2.9	276.7	2.1
5	HEMT 3	6.3	-0.010	15.0	0.000	1.8	1.7	18.3	13.9	3.0	286.3	-4.4
6	HEMT 4	5.9	-0.010	15.0	0.000	1.9	1.7	24.2	13.8	3.0	288.7	-10.4
7	RFA	8.0	-0.020	23.0	0.000	7.1	1.5	32.2	19.3	3.0	293.3	-12.9
8	RF FILTER	-2.0	0.000	100.0	0.000	2.0	1.0	30.2	17.3	3.0	293.4	-12.9
9	RF ATTEN	-0.2	0.000	100.0	0.000	0.2	1.0	30.0	17.1	3.0	293.4	-12.9
10	MIXER/HYBRID	-16.0	0.000	8.5	0.000	16.0	1.0	14.0	0.4	3.1	304.6	-13.6
11	DC BLOCK	-0.2	0.000	100.0	0.000	0.2	1.0	13.8	0.2	3.1	305.2	-13.6
12	IFA	12.0	-0.020	23.0	0.000	6.0	1.5	25.8	11.8	3.4	341.2	-14.0

TEMPERATURE ANALYSIS

TEMP (°C)	GAIN (dB)	NF & (dB)	Te (°K)	IPI3 (dBm)
-50.0	31.8	2.2	191.1	-17.9
-30.0	30.2	2.5	223.6	-16.8
0.0	27.8	2.9	281.1	-15.2
25.0	25.8	3.4	339.8	-14.0
50.0	23.8	3.8	412.2	-12.7
75.0	21.8	4.4	504.0	-11.5
100.0	19.8	5.0	623.6	-10.2

CONDITIONS

MSC NOISE SOURCE
MEASURED DATA
20 GHz

TABLE 4-4

NASA 20 GHz RECEIVER CASCADED TEMPERATURE ANALYSIS WITH IMPROVED MIXER

	ELEMENT DESCRIPTION	ELEMENT INPUT VALUES: GAIN MIN (dB)	GAIN KG (dB/°C)	INTERCEPT PTS: IPO3 (dBm)	INTERCEPT PTS: KIPO (dB/°C)	NF, TEMP DATA: NF (dB)	NF, TEMP DATA: TA/T1 EXP	CASCADED OUTPUT VALUES: CASC. ELEMENT VALUES @TA GAIN (dB)	IPO3 (dBm)	NF & Te NF (dB)	NF & Te Te (°C)	IPI3 (dBm)
1	ISOLATOR	-0.2	0.000	100.0	0.000	0.2	1.0	-0.2	100.0	0.2	13.7	100.2
2	W/G TRANSITION	-0.7	0.000	100.0	0.000	0.7	1.0	-0.9	96.6	0.9	66.8	97.5
3	HEMT 1	6.5	-0.010	15.0	0.000	1.7	1.7	5.6	15.0	2.6	231.7	9.4
4	HEMT 2	6.4	-0.010	15.0	0.000	1.9	1.7	12.0	14.1	2.9	276.7	2.1
5	HEMT 3	6.3	-0.010	15.0	0.000	1.8	1.7	18.3	13.9	3.0	286.3	-4.4
6	HEMT 4	5.9	-0.010	15.0	0.000	1.9	1.7	24.2	13.8	3.0	288.7	-10.4
7	RFA	8.0	-0.020	23.0	0.000	7.1	1.5	32.2	19.3	3.0	293.3	-12.9
8	RF FILTER	-2.0	0.000	100.0	0.000	2.0	1.0	30.2	17.3	3.0	293.4	-12.9
9	RF ATTEN	-0.2	0.000	100.0	0.000	0.2	1.0	30.0	17.1	3.0	293.4	-12.9
10	MIXER/HYBRID	-8.0	0.000	8.5	0.000	8.0	1.0	22.0	5.8	3.0	294.9	-16.2
11	DC BLOCK	-0.2	0.000	100.0	0.000	0.2	1.0	21.8	5.6	3.0	295.0	-16.2
12	IFA	12.0	-0.020	23.0	0.000	6.0	1.5	33.8	16.5	3.1	300.8	-17.3

TEMPERATURE ANALYSIS

TEMP (°C)	GAIN (dB)	NF & NF (dB)	Te (°K)	IPI3 (dBm)
-50.0	39.8	2.1	181.4	-21.9
-30.0	38.2	2.4	209.3	-20.7
0.0	35.8	2.7	255.7	-18.8
25.0	33.8	3.1	299.3	-17.3
50.0	31.8	3.4	348.3	-15.8
75.0	29.8	3.8	403.9	-14.4
100.0	27.8	4.2	468.0	-13.0

CONDITIONS

MSC NOISE SOURCE
MEASURED DATA
20 GHz

TABLE 4-5

The most significant problems with receiver performance are of course the gain and noise figure. The LNA gain drives both of these problems. In general, the gain was about 2 dB low per LNA stage, which is 8 dB total. The analysis shows that this raises the ambient noise figure by at least 0.3 dB, and the high temperature noise figure by 0.5 dB. Our design used vendor data for S- parameters and noise figure optimum impedance, noise resistance, and minimum noise figure. This data is usually gathered from a small sample of devices, and many engineers complain that vendor data is usually not accurate in terms of gain. The input and output impedances (S11, S22) seemed accurate, as LNA VSWRs were as expected. The output VSWR was less than 1.5: 1, allowing cascadability of the single stages.

It is difficult to absolutely determine if the LNA noise figure is higher than originally projected, because it was measured using an inaccurate noise source. The measured noise figure was close to what we expected with the bad MSC diode source, and since the new source generally gives higher numbers, one would assume the LNA noise figure is higher than expected.

The effects of the input transition on gain and noise figure are obvious. The insertion loss is directly added to the noise figure. The effects of the mixer conversion loss on noise figure are detailed above.

Another shortcoming in the receiver performance is the high variation of gain over temperature. Our design analysis showed a variance of 10 dB over the stated temperature range. The data shows a typical range of 20 dB, with the deviation equally divided between hot and cold temperatures. It is generally thought that amplifier gain changes by -0.01 dB per degree centigrade per stage of amplification. This assumption was also carried to the mixer. We know from the spurious response tests that the mixers do not function well at high temperature, and may be the cause of some of the additional loss. No temperature measurements have been made on the individual components fabricated during Task V.

A provision for gain compensation was put in the receiver in the place of the component now known as the DC block. Since voltage controlled variable attenuators suitable for insertion in the receiver have an insertion loss of 2.5 dB minimum, it was decided not to include it because of the already low receiver gain would be made lower. As the sensitivity analysis shows, this loss would also further raise the noise figure in the range of 0.2 dB.

5.0 POC FAILURES AND REPAIRS

During the POC testing, two failure modes were found that required design modification. They were RF amplifier oscillation and voltage regulator thermal shut down.

The HEMT LNA stages are prone to both low and high frequency oscillations due to the high gain of the devices. The MMIC RFA is prone to low frequency oscillations only, due to the lower RF gain of the devices. Low frequency oscillations have symptoms such as low gain, high noise figure, varying RF measurements, and unusual and varying DC current draws. They are usually caused by a lack of bypassing in the DC bias circuitry. To eliminate this problem, 1 microfarad capacitors were attached to the feed through pins for positive drain bias. These pins are used to feed the bias from the printed wiring board to the RF/IF cavity.
High frequency oscillations were taken into account during the circuit design with low pass shunting networks being used to dampen RF signals below the design band. However, the RF channel could not be made small enough to cut off moding, and this caused oscillations. Absorber material was placed on the lid, making the circuit perform if there was no lid. In some cases, side to side modes caused isolations, and absorber was put on one side to eliminate this mode. It is recommended to do this on all future receivers.

The LM117 voltage regulator used for the MMIC RFA chip was required to drop about 10 volts with 150 ma of current. This caused the regulator to go into thermal shutdown, which is non-damaging to the receiver and the regulator. A heat sink was attached to the regulator, which cured the problem at room temperature. The VDS was raised and the IDS reduced on the RFA in order to drop the wattage dissipated by the regulator, but that degraded gain and noise figure performance. A 20 ohm, 2 watt resistor was placed in series with the power supply and the regulator circuits for the RFA and LNA. The typical current was 250 mA, causing a 5 V drop across the resistor and taking plenty of load off the regulators. The regulator for the MMIC IFA is still supplied with +15 VDC.

6.0 RECOMMENDATIONS

Recommendations for product development will focus on two primary concepts: improvement of the current design, and taking advantage of rising technology. No matter which of the two focuses are chosen, it is recommended that the ACTs terminals allow some margin for receiver performance, as opposed to pushing the state of the art for noise figure. This will allow production type cost instead of engineering model cost.

The development of C band TVRO terminals is a good example. In the 1970's, a low noise amplifier cost thousands of dollars for 120°K noise temperature (1.5 dB noise figure). After the GaAs FET technology matured, prices began to drop, but the amplifiers remained fairly costly due to the labor intensity. It was found that the same design yielded LNAs with noise temperatures from 70°K to 140°K. The lower temperature components obviously commanded a higher price, as they were used in high quality video terminals, while the high temperature LNAs were used for applications such as data transmission, where an exceptionally high signal to noise ratio is not needed. This single design allowed a manufacturing atmosphere to develop, which, along with competition drove the prices down further. After the assembly costs dropped, the device performance continued to rise, while the cost went down. The low cost allowed the consumer to enter the market, and those 120°K LNAs now cost under $100.00.

A wider performance margin can allow the use of cheaper and more workable components such as packaged HEMTs and soft substrates. It can also allow the integration of components such as the stages of the LNA. We built LNA stages on separate carriers so that we could better characterize their performance, and put the best ones in front. If the LNA, RFA, and bandpass filter were on one carrier, the number of substrates needed for those components would be dropped from thirteen to five.

A performance margin will allow a quarter micron MMIC front end to used in the receiver. The device technology has improved significantly since the initial design phase of this contract, and companies with quarter micron capability are starting to offer foundry service to outside companies. Alpha Industries offers this, and has an internal tenth micron process, which is reserved for their MIMIC program team.

As the analysis section of this report shows, any future product development should included improvement of the waveguide transition. The new transition should have a fixed short to improve mechanical stability. The transition should of course have better insertion loss.

The mixer should also be improved. Our MMIC Image Reject Mixer has 16 dB of loss, while many mixers are commercially available that have 8 dB of loss. The MMIC mixer requires a +20 dBm LO drive, while the commercially available mixers require only +10

dBm. The only advantage of our mixer is the image rejection capability, which is not needed due to the filtering already built into the receiver. Alpha Industries has developed a 35 GHz mixer with 4 dB conversion loss using Schottky diodes with a Mesa (vertical) topology. This diode technology is superior to the HMS FET MMIC technology, which suffers from high series resistance. A smaller local oscillator should be used. In the current receiver, the local oscillator is much larger than the receiver module, due to the two ovenized crystal reference sources. A future Harris IR&D will develop a dielectric resonator oscillator which will be locked to a 5 MHz crystal source.

If a smaller size is required for the current receiver, the two 100 Mhz crystal references can be moved away from the feed. This will also simplify any desired frequency control.

Casting the main portion of the receiver housing would facilitate production. The current housing takes four days of labor on a computerized mill. A cast housing would require about one day of machining. Using more integrated carriers would reduce this further. The use of a totally aluminum housing, without subcarriers, is discouraged because the high thermal coefficient of aluminum will cause the brittle GaAs devices to fracture. That is why Invar carriers are used in the receiver.

In the area of follow on technology development, HEMT MMIC is a promising rising technology. Single stage low noise amplifiers have been fabricated, and development work is being funded by DOD agencies such as RADC.

Future modifications in device periphery are also promising. Mitsubishi has developed a "mushroom" gate periphery that has demonstrated a 1.0 dB noise figure at 18 GHz. Future commercial release of devices with smaller gate widths will also allow lower noise figures.

20 GHz RECEIVER STUDY
CONTRACT NAS3-24244

PROOF OF CONCEPT TEST REPORT
FOR
SECOND BUILD OF THREE UNITS

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15 DECEMBER 1988

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CONTENTS

1.0 INTRODUCTION

This report presents the work done on the second build of three receivers performed on Task VI (Proof of Concept Test and Analysis) of the NASA 20 GHz Receiver Program sponsored by the NASA-Lewis Research Center in Cleveland, Ohio. The test procedure was generated during Task III (POC Plans and Specs),and updated during Task IV (POC Design) and Task V (POC Fab). Testing was done at -30°C, 25°C, and 75°C on the three receivers for many of the tests. The report will present the data in graphical, tabular, and worst case form. Diagrams of the test set-ups were shown in the previous Task VI report. Raw data is available in the individual logbooks. This report concludes with a comparison of the two builds of receivers, and an overall performance ranking of the six receivers.

2.0 TEMPERATURE TEST DATA

This section contains POC receiver data over temperature for the following: Noise Figure, Gain, Gain Ripple (150 MHz), Gain Slope (10 MHz), and Input Third Order Intercept Point. The data is presented graphically on a parameter by parameter basis, with the specifications shown on the graphs. Data was taken at -30°C, 25°C, and 75°C.

Figure 2-1 shows the noise figure over temperature for the frequencies called out in the specification (19.385 to 20.081 GHz). Due to circuit optimization, S/N 0006 has a declining noise figure with frequency and gives the best high band noise figure at ambient (4.25 dB max), but also demonstrated the worst high temperature noise figure (5.87 dB max). S/N 0005 has the highest ambient noise figure (4.63 dB max).

Figure 2-2 shows the gain data plots for the three additional receivers. S/N 0004 shows the greatest change in gain due to cold temperature, and a moderate change for high temperature. This receiver had the lowest overall gain. S/N 0005 had the greatest gain degradation due to high temperatures and gain increased only a few dB at cold temperatures. S/N 0006 has the highest overall gain, as well as smallest temperature deviation. In fact, gain measures slightly higher at high temperature at a couple of points. Overall, S/N 0006 is the best of the six receivers produced on this program.

Figure 2-3 shows the gain ripple for five subbands, each 500 MHz wide. The gain measurement system measures gain every 10 MHz, and computes the maximum change over 150 MHz. The worst case ripple is displayed on the bar chart. All three of the receivers met the specification of +/- 1.5 dB per 150 MHz. A gain roll off around 19.6 GHz is the most significant contributor to ripple.

Figure 2-4 shows the gain slope for five subbands, each 500 MHz wide. The gain measurement system measured gain every 10 MHz, and computed the maximum change over 10 MHz for each subband. The several instances of non-compliance with the spec of .5 dB per 10 MHz is unexpected, considering the gain ripple compliance. All but one of the discrepancies are less than 0.2 dB out of spec, and generally at cold temperature. S/N 0006 has a slope of 0.865 dB at 19.7 GHz at cold temperature.

Figure 2-5 shows the intercept point over temperature. The only variances from the -30 dBm specification is on S/N 0004 and 0005 at -30°C at the peak gain frequencies. The worst case is S/N 0005 at 17.7 GHz, where the intercept point was -33.03 dBm.

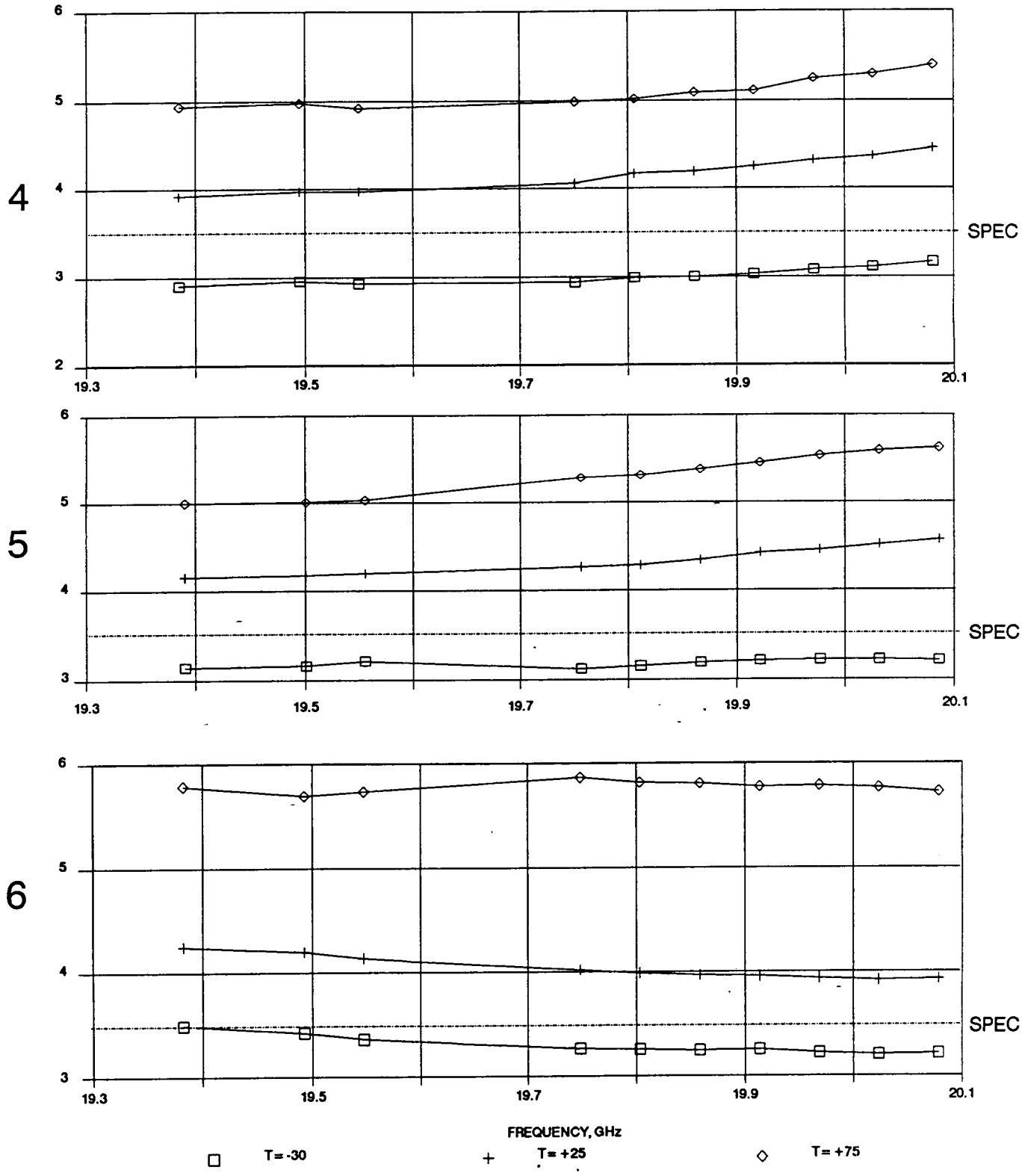

FIGURE 2-1 NASA 20 GHz RECEIVER NOISE FIGURE (dB)

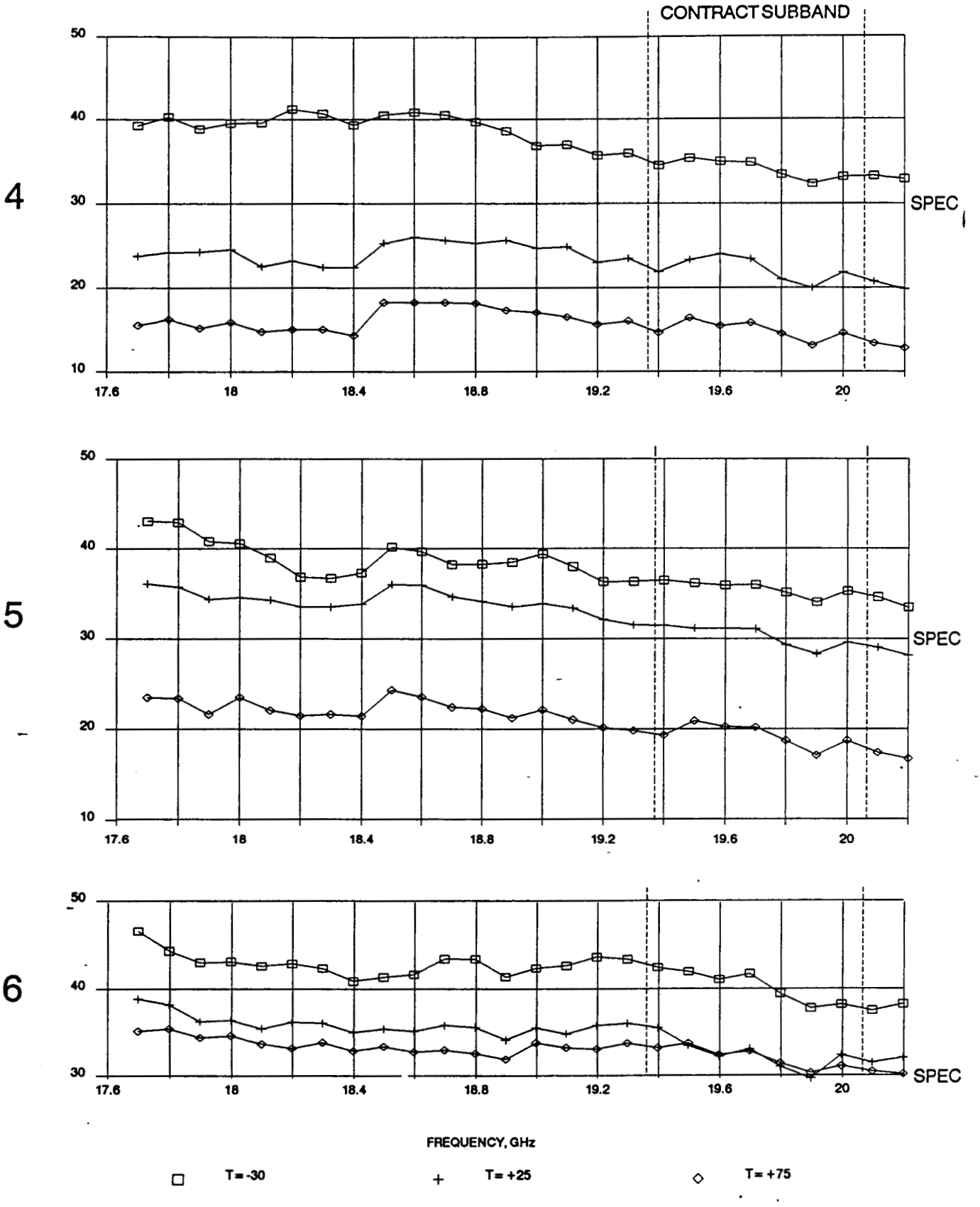

FIGURE 2-2 GAIN OVER TEMPERATURE (SPEC: >30 dB)

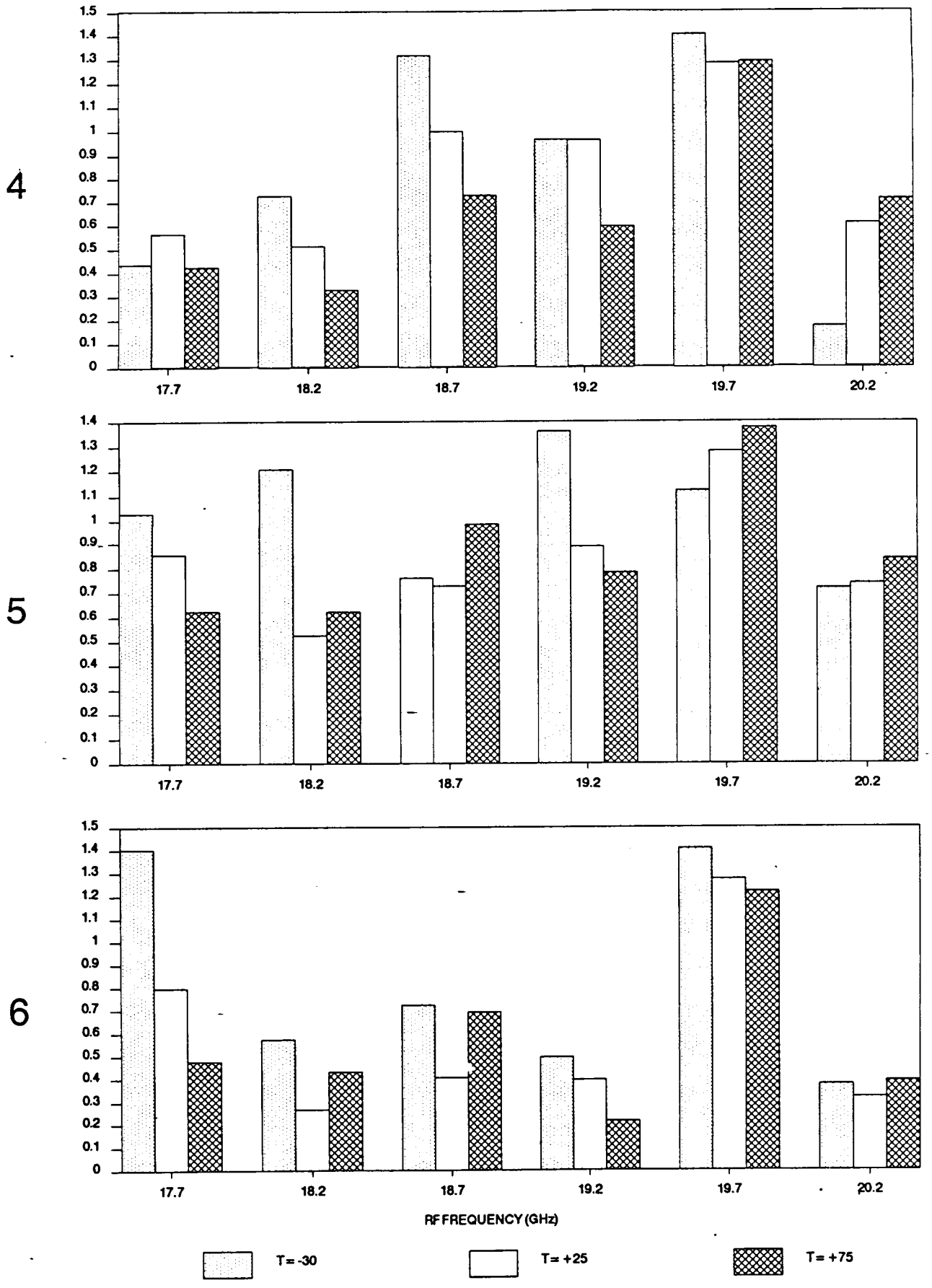

FIGURE 2-3 GAIN RIPPLE +/- dB / 150 MHz (SPEC: <1.5 dB)

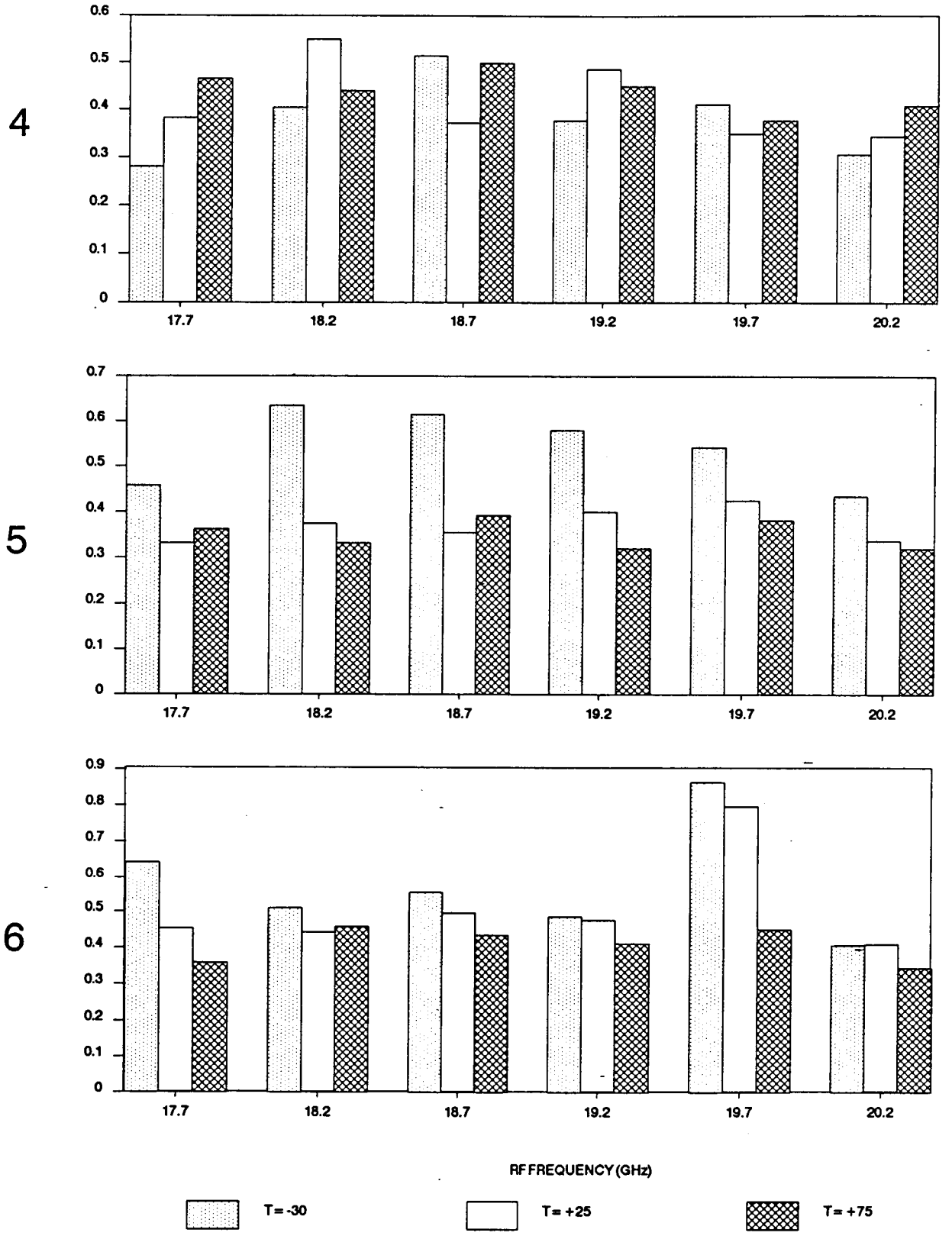

FIGURE 2-4 GAIN SLOPE dB / 10 MHz (SPEC: <.5 dB)

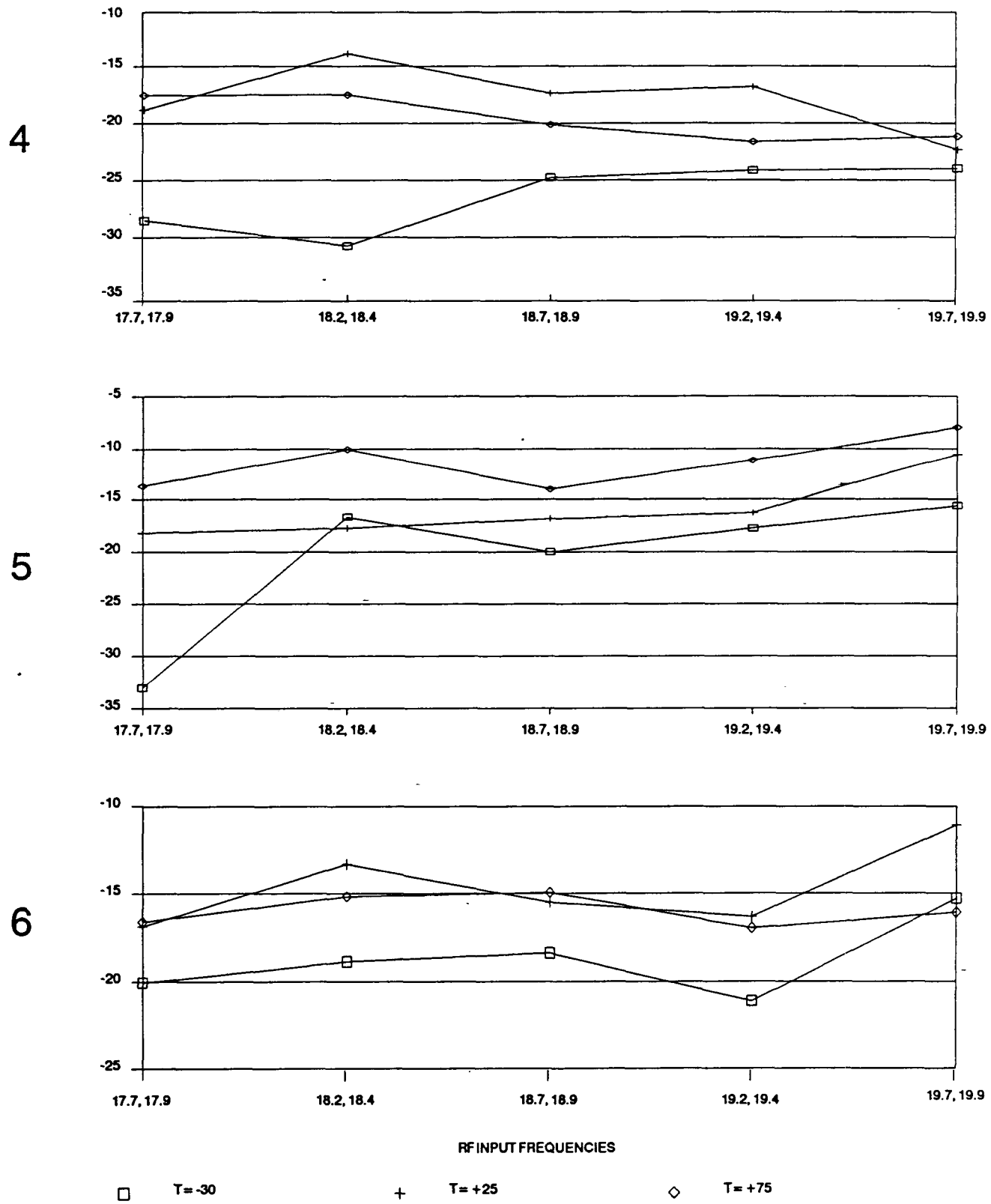

FIGURE 2-5 INPUT 3rd ORDER I.P. (SPEC > -30 dBm)

3.0 OTHER TEST DATA

In this section, the remainder of POC test data is presented in a summary form, giving a general view of the three additional receivers' performance. In most cases, worst case performance is presented. The following tests are included:

1 dB Input Compression Point

Input and Output VSWR

Group Delay

AM/PM Conversion

Out of Band Rejection

Spurious Response

Image Rejection

Local Oscillator Phase Noise

Local Oscillator Frequency

Reverse Voltage

Inband Overdrive

Input Gain Compression Point

The compression point test was a measured at 20 GHz at room temperature. The specification is -40 dBm minimum. The 1 dB compression points are:

S/N 0004: -23.76 dBm

S/N 0005: -23.9 dBm

S/N 0006: -18.7 dBm

VSWR

Input and output VSWRs were measured using the HP 8510 network analyzer. Because of the input circulator, the receivers meet the input VSWR specification always, including when the unit is turned off.

RF Input VSWR- 17.7- 20.2 GHz

Spec: 1.7:1

S/N 0004 Max: 1.19:1

S/N 0005 Max: 1.29:1

S/N 0006 Max: 1.19:1

IF Output VSWR- 3.185- 3.540 GHz

Spec: 1.5:1

S/N 0004 Max: 1.22:1

S/N 0005 Max: 1.53:1

S/N 0006 Max: 1.66:1

Group Delay

For group delay, the specification is 5.0 nS peak-to-peak over 100 MHz. The maximum group delay measured was 1.44 nS peak-to-peak over 100 MHz. The group delay was measured over six segments of the RF band by varying the LO.

AM/PM Conversion

The amplitude modulation to phase modulation conversion specification was 0.5 degrees/ dB. The measured AM to PM conversions are:

S/N 0004: 2.4 degrees/ dB

S/N 0005: 2.2 degrees/ dB

S/N 0006: 2.8 degrees/ dB

Image Rejection

The image reject specification is 40 dB. No evidence of the image signal (13.5 GHz) was found in any of the receivers. The measurement was limited by the spectrum analyzer noise floor to 58 dB image rejection. The excellent image rejection can be attributed to the RF filter performance and the image frequency being below waveguide cutoff of 14.05 GHz.

Spurious Response

Shown below are the worst case spurious response results for out of band signals. The M and N columns indicates the RF and LO multipliers, respectively. The specification for inband and out of band spurs is -45 dBc.

M	N	RF (GHz)	LO (GHz)	SPUR (dBc)
-2	2	15.1	16.8	-58.7
3	-2	12.4	16.8	-62.8
-3	3	15.7	16.8	-59.7
-1	2	25.0	14.3	-66.5
2	-3	23.1	14.3	-63.5
-2	3	22.2	15.9	-62.2

The worst case in-band spurious response is shown below.

M	N	RF (GHz)	LO (GHz)	SPUR (dBc)
2	-2	17.7	16.0	-31.9
3	-3	17.8	16.7	-55.7
-3	4	17.9	14.3	-63.5
4	-4	17.7	16.85	-61.7
4	-5	18.7	14.3	-63.5
5	-5	17.7	17.0	-61.7

The out of spec data spur (2 X -2) involved the second harmonic of the LO. This out of spec spurious performance is probably caused by the high LO drive required to operate the mixer (20 dBm). Also, an input level of -50 dBm was used to measure spurs, due to spectrum analyzer noise floor considerations. This is 10 dB higher than the specified range. For this spur, spurious response should improve by 1 dB for each 1 dB drop in the signal strength. This would make this spur only 3.1 dB too high at -60 dBm input.

Phase Noise

The phase noise tests for the local oscillator were done by the vendor, Communications Techniques of Whippany, NJ. Shown below are the various offsets, specifications, and worst case phase noise performance.

OFFSET (FREQ)	SPEC. dBc	WORST CASE dBc
100 Hz	-56	-75
1 kHz	-78	-88
10 kHz	-80	-93
1 MHz	-100	-115

Local Oscillator Stability

The local oscillator output frequency was measured over temperature. The specification calls for no more than 40 kHz deviation from the specified frequency. The maximum deviation is +36 kHz. The maximum change of any oscillator's frequency over temperature is 39 kHz.

Reverse Voltage Protection and Inband Overdrive

The three additional receivers did not suffer any degradation in performance after a 0 dBm 20 GHz CW input or a reverse DC voltage hookup. The receiver is provided with a non-reversible DC jack, the Burndy BT00E83P. The matching plug part number is BT06E83S.

4.0 OVERALL COMPARISON OF THE TWO GROUPS OF RECEIVERS

It is difficult to compare the two groups of receivers because of the number of parameters to be judged, and the variances between receivers. The two most important parameters are gain and noise figure. We will compare averages for the two builds of three receivers for these parameters over temperature.

Figure 4-1 shows the noise figures averaged for the two builds at all three temperatures. At cold temperatures, the second build has the advantage. At ambient, the second group is slightly better at high frequencies, but inferior in the low band. The group two noise figure is higher at high temperature, except at the very top of the band.

Figure 4-2 shows the gains averaged at the three temperatures. This plot shows the second group to be superior to the first, having higher gain at all temperatures. The first group has higher gain at some frequencies (18.3 and 18.8 GHz) but suffers from high gain ripple at these frequencies. The second group has much flatter gain.

The second group is far superior in terms of gain ripple, being specification compliant. The second group is slightly superior in terms of gain slope, with fewer and less serious deviations.

Intercept point performance for both groups is good, due to the low gain. Group two has two deviations, while group one has but one, and none of the deviations were significant.

Input VSWR is good for both groups because of the input isolator. Group two has a deviation (1.66:1 compared to 1.5:1) while group one is spec compliant.

Group two has higher AM to PM conversion, averaging 2.4 degrees/dB as opposed to 1.7 for group one. Because of the difficulties in making this measurement, the degree of confidence is somewhat lower than in any other parameter. Because of the high gain compression, the actual AM/PM conversion is probably significantly better than the measurement results indicate, and may in fact be within specification allowances.

All receivers have excellent image rejection. The second group has better out of band rejection in terms of spurious response, but both groups have equal trouble with the 2 X -2 in band spur (RF= 17.7 GHz, IF= 16.0 GHz). If the 16.541 GHz local oscillator is used, a signal around 18.2 GHz would produce this in band spur.

When all factors are considered, the second group is probably slightly better overall than the first. To rank the six receivers is very subjective, and is probably best done looking only at

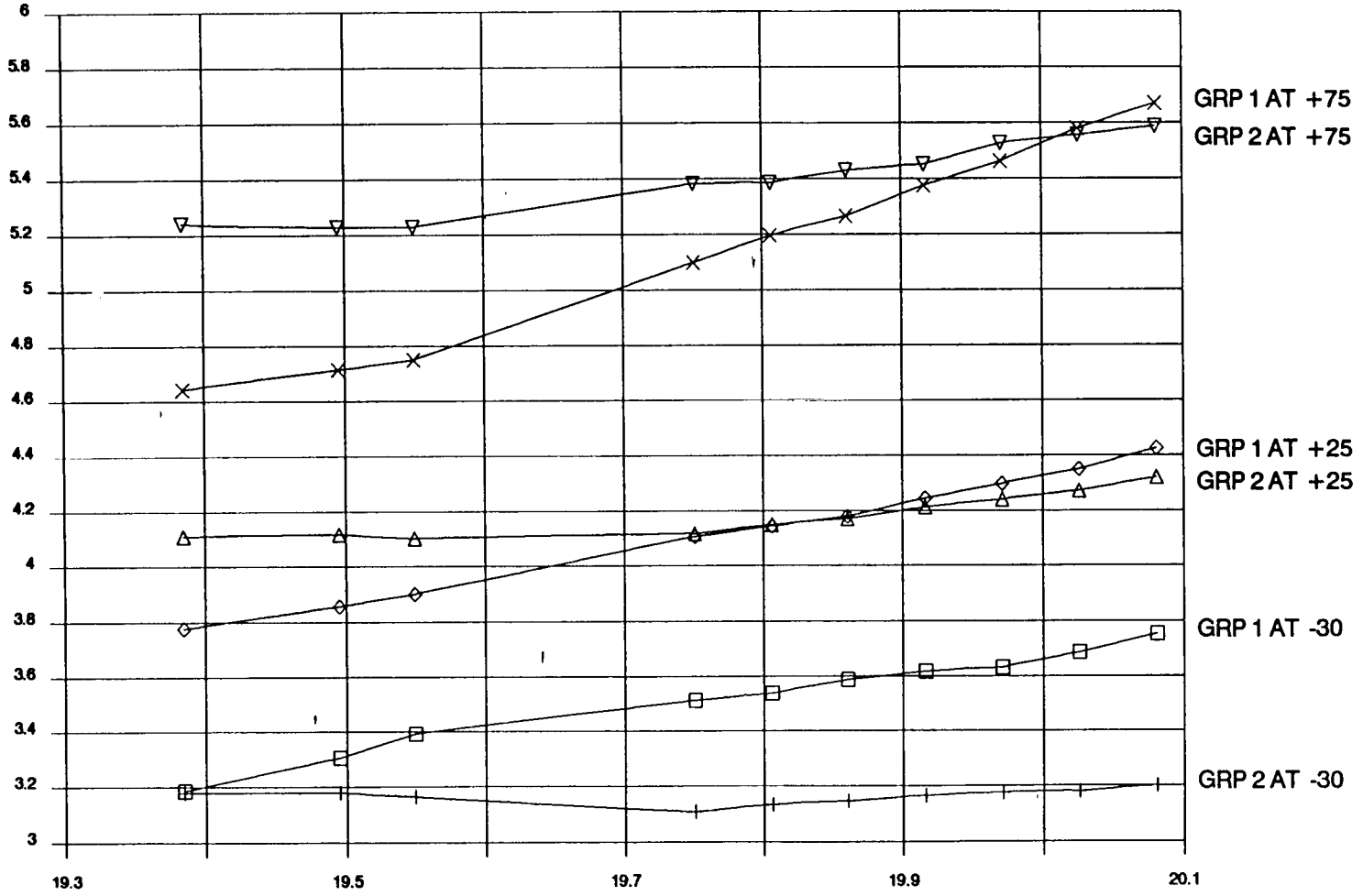

FIGURE 4-1 COMPARISON OF AVERAGE NOISE FIGURES OF THE TWO GROUPS OF RECEIVERS

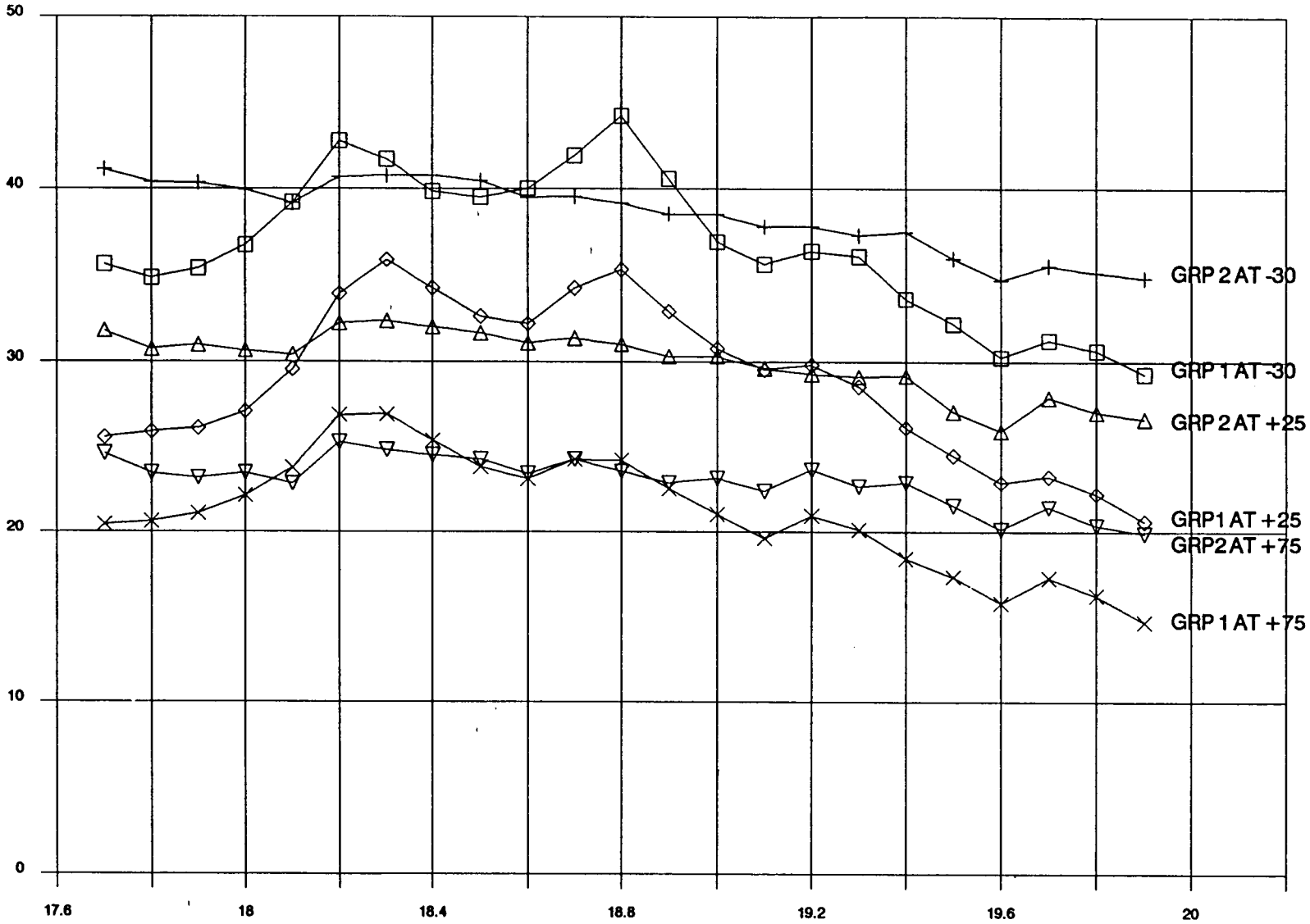

FIGURE 4-2 COMPARISON OF THE AVERAGE GAIN OF THE TWO GROUPS OF RECEIVERS

gain, noise figure, gain ripple, and the variations of these over temperature. Table 4-1 lists the six receivers in terms of quality of performance. The difference between units is slight, and the variation between the best and the worst is not great enough to warrant significant preference in individual applications.

Unit	Overall Performance
0006	Lowest Ambient NF, Best Gain
0002	Second Best Ambient NF, Lower Gain than 0005
0005	High Gain, NF Comparable to Remaining Units
0001	Lower Gain than 0005, Same NF as 0005
0004	Lower Gain than 0001, Same NF as 0005
0003	Lowest Gain, Same NF as 0005

TABLE 4-1 OVERALL RECEIVER PERFORMANCE RANKING