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IMAGE PROCESSING USING GALLIUM ARSENIDE (GaAs) TECHNOLOGY

Warner H. Miller
NASA/Goddard Space Flight Center

ABSTRACT

The need to increase the information return from space-borne imaging systems has increased in the past decade. The use of multi-spectral data has resulted in the need for finer spatial resolution and greater spectral coverage. Finer spatial resolution and a greater number of spectral bands has increased data rated and system bandwidth requirements. Although the telecommunication capability planned through the 1900's is relatively large, feasibility studies on solid state imaging instruments in support of AlOS have shown increased rates that exceed the telecommunication channel capacity. Onboard signal processing will be necessary in order to utilize the available Tracking and Data Relay Satellite System (TDRSS) communication channel at high efficiency.

A generally recognized approach to the increased efficiency of channel usage is through data compression techniques. The method selected must function in real time satisfying the requirements of both the high speed data instrument source and limited bandwidth of the telecommunication channel. The compression technique implemented is a differential pulse code modulation (DPCM) scheme with a non-uniform quantizer.

NASA has recognized the need to advance the state-of-the-art of onboard processing and has chosen for this purpose to develop GaAs integrated circuit technology. NASA's GaAs research effort has developed an Adaptive Programmable Processor (APP) chip set which is based on an 8-bit slice general processor. This 8-bit slice and a control chip which stores the DPCM algorithm has been fabricated. This chip set will provide a compression ratio of 2 and operate in

real time to reduce a data rate from an imaging instrument to a data rate which is compatible with TDRSS.

The presentation will describe the reason for choosing the compression technique for the Multi-spectral Linear Array (MLA) instrument. Also. the presentation will give a description of the GaAs integrated circuit chip set which will demonstrate that data compression can be performed onboard in real time at data rate in the order of 500 Mb/s.

REAL TIME PROCESSING OF IMAGING ARRAYS
RELATIONSHIP BETWEEN SPATIAL RESOLUTION AND DATA RATE FOR ONE SPECTURAL BAND ASSUMING 185K FOV AND AN EARTH VIEWING ALTITUDE OF 700KM

	IFOV (M)	# DET. PER FOV	INTEG. TIME (DWELL) (MSEC.)	PIXEL RATE	PIXEL PERIOD (MICRO SEC.)	SERIAL DATA RATE PER SPECTRAL BAND (B/SEC.)
	120	1542	17.7	87 KPPS	11.5	695.7 K
MSS	80	2313	11.8	196K	5.1	1.57M
	60	3083	8.9	347.7K	2.9	2.78M
	40	4625	5.9	782.4K	1.3	6.26M
TM	30	6167	4.4	1.39Mpps	0.72	11.13M
	20	9250	2.9	3.13M	0.32	25.0 M
	15	12334	2.2	5.56M	0.179	44.5 M
ALOS/MLA	10	18500	1.47	12.5M	0.080	100.0 M

REQUIREMENTS

1. COMPRESSION RATIO $>$ 1.8
2. BE FABRICABLE FROM SPACE QUALIFIABLE PARTS
3. CONSUME LOW POWER, IMPLYING LOW ON-BOARD STORAGE
4. ALLOW FOR BIT TRANSMISSION ERRORS OF THE ORDER OF 1 IN 10^5
5. MINIMIZE SPATIAL AND RADIOMETRIC DISTORTION
6. MINIMAL PROCESSING POWER

ENTROPY MEASUREMENTS AND MAXIMUM COMPRESSION RATIO WITH NO DISTORTION

	$H(Y/X)$	C_{MAX}
URBAN SCENE	3.283	2.44
NATURAL SCENE	3.051	2.62

THE INTERESTING RESULT OF THESE MEASUREMENTS IS THAT THE AVERAGE MAXIMUM COMPRESSION RATIO WITH NO DISTORTION IS LESS THAN 3:1 AND CLOSER TO ABOUT 2.5:1. IN AN ACTUAL SYSTEM, OF COURSE, THE COMPRESSION RATIO WOULD BE LOWER DUE TO THE "OVERHEAD" EFFECT OF SYNCHRONIZATION, ERROR CONTROL AND REFERENCE INFORMATION.

EVALUATION BASIS

COMPRESSION RATIO

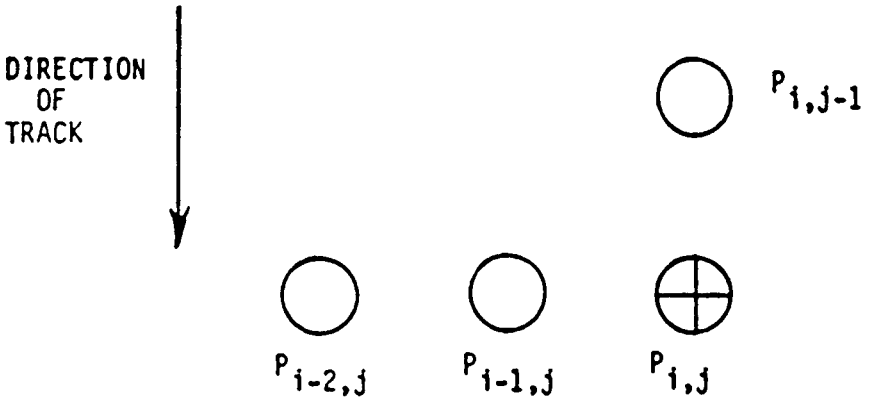
MEAN SQUARE ERROR

BUFFER REQUIREMENTS

SCHEMES CHOSEN:

DPCM FOLLOWED BY ENTROPY CODER

DPCM WITH A NON UNIFORM MAX QUANTIZER



a) NOTATION USED

b) PREDICTION SCHEMES

$$\hat{P}_{i,j} = P_{i-1,j} \qquad \text{ADJACENT}$$

$$\hat{P}_{i,j} = 2P_{i-1,j} - P_{i-2,j} \qquad \text{LINEAR EXTRAPOLATION}$$

$$\hat{P}_{i,j} = \frac{P_{i-1} + P_{i,j-1}}{2} \qquad \text{TWO DIMENSIONAL: TWO ADJACENT}$$

ACHIEVABLE COMPRESSION RATIO USING DPCM FOLLOWED BY HUFFMAN-TYPE ENTROPY CODE ASSUMING LAPLACIAN P.D.F.

PREDICTOR	URBAN	GEOLOGICAL
ONE DIMENSION	2.0	2.15
TWO DIMENSION	2.16	2.33
ADAPTIVE TWO DIMENSION	2.23	2.36
CALCULATED USING CONDITIONAL ENTROPY	2.44	2.62

NON-UNIFORM QUANTISER RESULTS

For Laplacian pdf

Design Sigma	Decision Levels	Reconstruction Levels	Projected D/Sigma^2	Absolute Mean Square Error/Pixel		Normalized* Mean Square Error/Pixel		Compression Ration
				Image 1	Image 2	Image 1	Image 2	
		3 Bit N = 7						
2.0	1,2,4	0,2,3,6	.102	4.17	3.66	.274	.335	2.7
2.5	1,2,4	0,2,3,6	.079	4.17	3.66	.274	.335	
3.0	1,3,6	0,2,5,8	.065	2.04	1.85	.134	.170	
3.5	1,3,7	0,2,5,8	.059	2.18	1.98	.143	.181	
4.0	1,4,8	0,3,6,11	.052	1.16	1.10	.076	.101	
4.5	1,4,8	0,3,6,11	.053	1.16	1.10	.076	.101	
5.0	1,4,9	0,3,6,13	.054	1.13	1.04	.074	.095	
5.5	1,5,11	0,3,8,15	.053	1.21	1.10	.079	.100	
		3 Bit N = 8						
2.0	0,1,2,4	1,2,3,6	.102	4.34	3.84	.285	.352	2.7
2.5	0,1,2,4	1,2,3,6	.073	4.03	3.50	.264	.321	
3.0	0,1,3,6	1,2,5,8	.059	1.91	1.72	.126	.157	
3.5	0,1,3,7	1,2,5,10	.053	1.23	1.11	.080	.101	
4.0	0,2,5,9	1,4,7,12	.046	.92	.89	.060	.081	
4.5	0,2,5,9	1,4,7,12	.045	.92	.89	.060	.081	
5.0	0,2,5,10	1,4,9,14	.045	1.18	1.04	.077	.095	
5.5	0,3,6,12	1,4,9,16	.044	.99	.87	.064	.081	
		4 Bit N = 15						
2.0	1,2,3,4,6,7,9	0,2,3,4,5,7,8,11	.086	.72	.72	.047	.065	2.0
2.5	1,2,3,4,6,8,11	0,2,3,4,5,7,10,13	.055	.51	.53	.033	.048	
3.0	1,2,3,4,7,9,13	0,2,3,4,6,8,11,16	.041	.45	.45	.029	.041	
3.5	1,2,3,4,7,10,14	0,2,3,4,6,9,12,17	.031	.44	.44	.028	.040	
4.0	1,2,3,5,8,11,15	0,2,3,4,7,10,13,18	.026	.44	.44	.029	.040	
4.5	1,2,3,5,8,11,15	0,2,3,4,7,10,13,18	.022	.44	.44	.029	.040	
5.0	1,2,3,5,8,11,15	0,2,3,4,7,10,13,18	.019	.44	.44	.029	.040	
5.5	1,2,3,5,8,11,15	0,2,3,4,7,10,13,19	.017	.45	.44	.029	.040	

PERFORMANCE SUMMARY

Method	Maximum Compression Ratio	Problems	Advantages
DPCM + Huffman Parameters: 2-adjacent prediction modified code adaptive by line segment	2-2.3	• Errors in Tx can cause loss of code sync • Requires Pre Proc. (ie Radiom. Corr.) • Potential buffer overflow • Large memory needed on board	• With error correcting code could produce very high fidelity
DPCM with Nonuniform Quantiser N = 7/8 N = 15	 2.67 2.0	• Distortion D/σ^2 ~ 0.09 ~ 0.04	• Simple to implement • Degrades gracefully as image gets "busier" • Fixed block structure

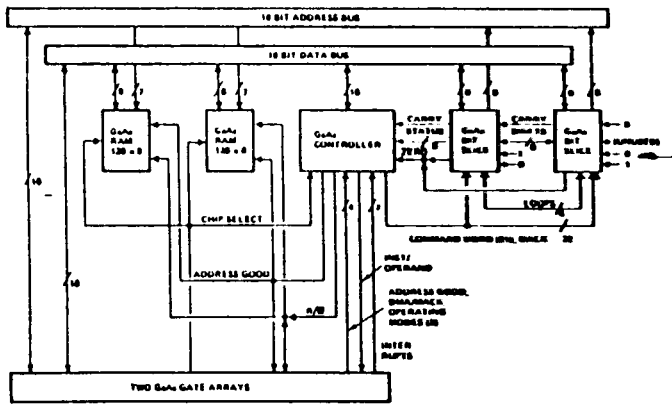
TECHNOLOGY TRADE OFF

PREDICTED SPEED-POWER CHARACTERISTIC OF HONEYWELL VHSIC CHIPS, ECL AND GaAs TECHNOLOGIES WHEN PERFORMING THE NON-UNIFORM QUANTIZING DPCM ALGORITHM (7 MICRO INSTRUCTIONS)

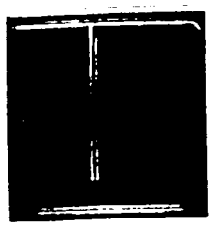
	DEDICATED DESIGN		PROGRAMMABLE PROCESSOR	
	ECL	GaAs	VHSIC (Si) (HONEYWELL)	APP (GaAs)
INSTRUCTION TIME (NSEC.)	-	-	40 NSEC.	5 NSEC.
PROCESSING TIME (NSEC.)	58.5	9.7	240	45
POWER, WATTS	14.0	2.7	4.7	4.5

GAAS ADAPTIVE PROGRAMMABLE PROCESSOR (APP)

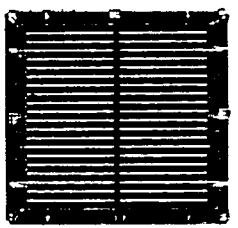
BLOCK DIAGRAM -GaAs 1750A COMPUTER



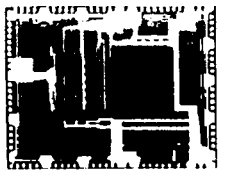
16K bit RAM
(DARPA)



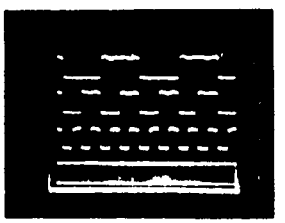
7K CONFIGURABLE GATE ARRAY
(DARPA)



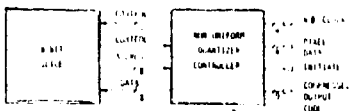
16-bit SLICE GENERAL PROCESSOR
(NASA)



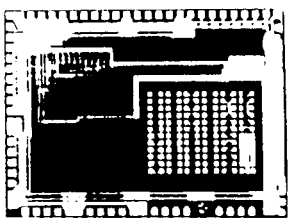
ALU Add, Incrementing
Register 0, 150 MHz Clock
Shows: bit 5
bit 4
bit 3
Clock



BLOCK DIAGRAM
GaAs DATA COMPRESSION PROCESSOR



NON-UNIFORM QUANTIZER CONTROLLER
(NASA)



Overview

8-Bit Slice Processor

- Original Architecture
- MIL-STD-1750A Computer Building Block
- Flexible Command Structure
- Signal Processing Applications, RISC

GaAs D-MESFET Technology

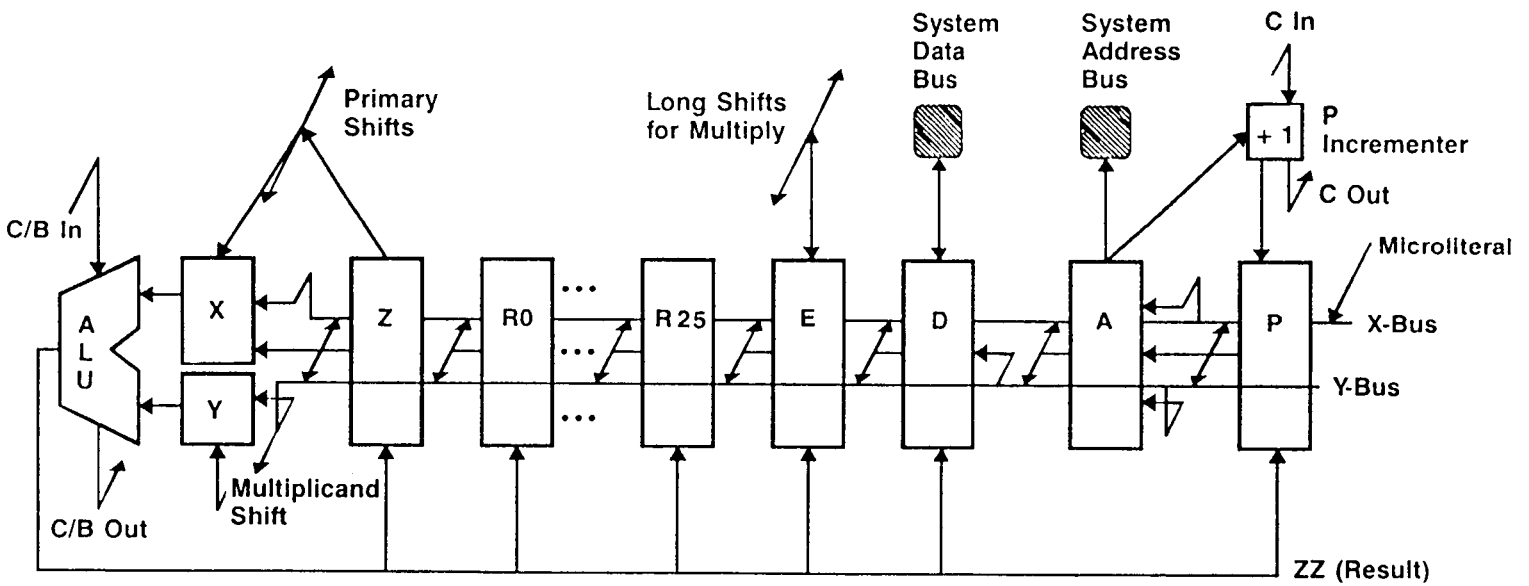
- Non S/A Ion Implanted
- Threshold Voltage $-1.0V$
- Gate Length 1.0 μm
- Conductor Pitch 4 μm (M1), 6 μm (M2)

6.6 ns Register–Register Add/Subtract

- 150 MHz Clock

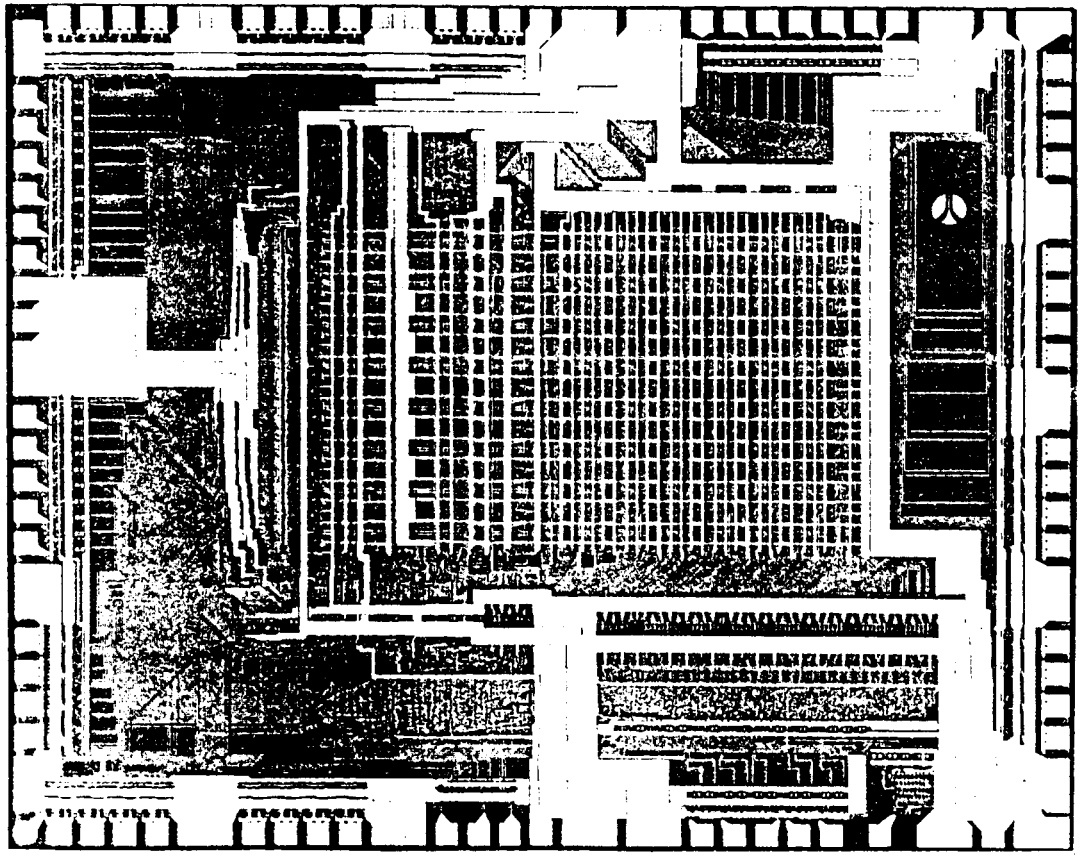
Power 4.2W (Low I_{DSS})
9.2W (High I_{DSS})

Data Path Functional Block Diagram



- 31 Word × 8-Bit 2 Port Register File
- 8 Function ALU
- 3 Internal Buses
- Program Counter Incrementer
- Shifts
- 8-Bit Address Port
- 8-Bit Bidirectional Data Port

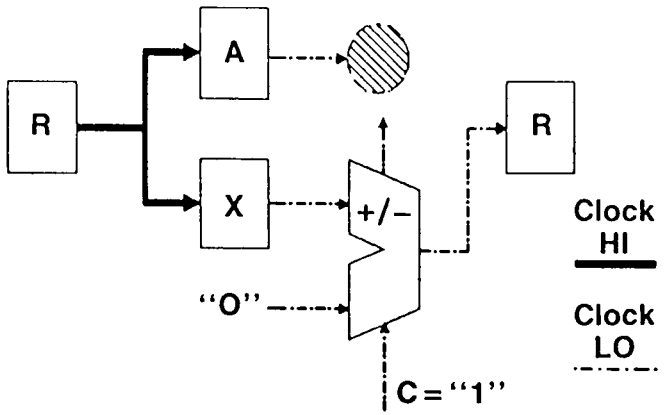
Die Photomicrograph



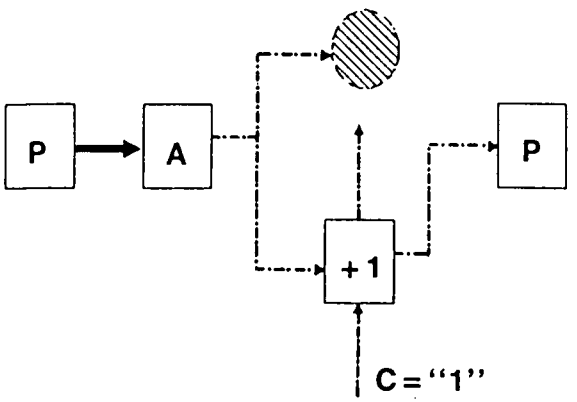
- Die Size
  - 4.9mm x 3.9mm
- Device Count
  - 9400 Transistors
  - 3010 Diodes
- Pads
  - 64 Signal
  - 29 Power/Ground

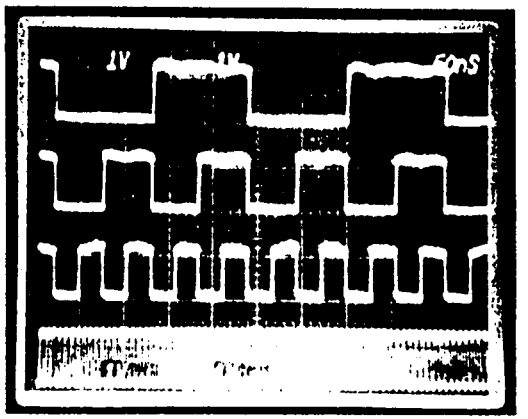
Performance Results

Register to Register Add/Subtract



Program Counter Increment





Bit 5

Bit 4

Bit 3

Clock

Memory Address Output Oscilloscope Waveforms

ALU Adds Incrementing Register 0, at 150 MHz Clock

- **Single Chip Worst-Case Delay Paths 6.6 ns**

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