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RADIATION EFFECTS IN SPACECRAFT ELECTRONICS*

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In this presentation effects on the internal spacecraft electronics due to exposure to the natural and enhanced space radiation environment will be reviewed. The emphasis will be placed on the description of the nature of both the exposure environment and failure mechanisms in semiconductors. Understanding both the system environment and device effects is critical in the use of laboratory simulation environments to obtain the data necessary to design and qualify components for successful application.

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Energy Deposition

For the internal electronics of a spacecraft the radiation exposure is characterized in terms of the energy deposited in critical regions of the piece parts. In modern electronic systems, the most sensitive pieceparts of the discrete semiconductor devices and microcircuits. It follows, therefore, the critical materials of interest are silicon and silicon-dioxide.

The absorbed energy is described in units of radiation absorbed dose for the material, or rad(Silicon) in this case, as shown in Figure 1. The energy can be absorbed in the semiconductor material by either ionizing or nonionizing means. For exposure by x- or gamma-rays (important principally in laboratory simulation environments) the energy deposition is almost exclusively by ionization. For the high energy electrons of the space radiation environment, energy deposition is principally by ionization. For the high energy electrons of the space radiation environment, energy is deposited by both ionization and nonionizing atomic displacements. For neutron exposure (important in laboratory simulation of displacement damage) the absorbed energy is almost exclusively in displacement damage, although the neutron exposure is always associated by concomitant ionizing gamma rays. It will be shown that ionizing radiation effects, both by accumulated effects and that of a single particle, are of principal concern to the internal spacecraft electronics.

- Absorbed Energy – rads(Silicon)
  - One rads(Si) = 100 ergs/gram(Silicon)
- X–/Gamma Rays: Ionization Exclusively
- Electrons: Principally Ionization
- Protons: Ionization and Atomic Displacement
- Neutrons: Principally Atomic Displacement

FIGURE 1

System/Simulator Exposure Environments

Space radiation environments can be initially scoped by the electron-induced accumulated ionizing radiation for both the natural environment and an environment enhanced (i.e., pumped-up) by the trapped electrons of a high-altitude nuclear weapon detonation, as shown in Figure 2. Also shown is the range of exposure levels typical for exposure using a laboratory Cobalt-60 source for the simulation of ionizing radiation effects.

The system environments represent the absorbed dose behind a 100 mil, semi-infinite slab of aluminum, for orbital altitudes ranging from 150 to 60,000 km, and for orbital inclinations of 0, 30, 60, and 90 degrees. System exposure to the natural environment was assumed over the range of one to thirty years. The enhanced environment is summarized for an exposure of 180 days [courtesy of Mr. S.C. Rogers, JAYCOR, and the Defense Nuclear Agency].

The lower ranges of exposure are representative of the environments at low earth or geosynchronous orbit, while the peak exposures are for environment roughly between 1,000 and 20,000 km in altitude. Additional shielding will further reduce the exposure levels, but shielding of the electron dose is limited by the production of gamma rays by bremsstrahlung.

It should be noted that the exposure rate for the natural environment is substantially lower than that typical of Cobalt-60 simulation exposures, and that the levels of exposure for the enhanced environment are both substantially greater and at a higher intensity than the natural environment exposure.

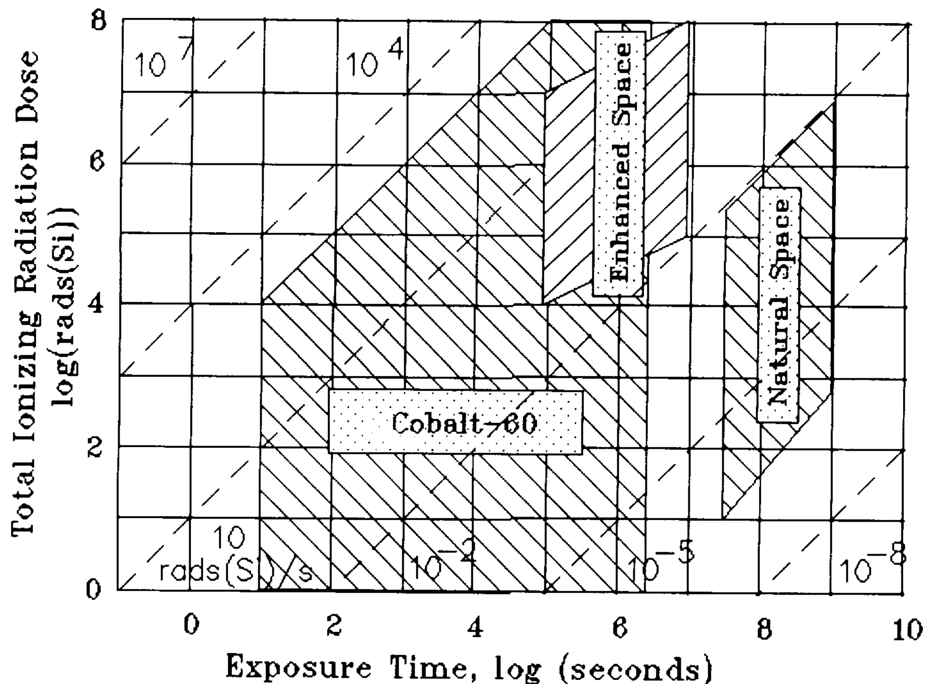

FIGURE 2

Summary of Semiconductor Device "Total Dose" Susceptibility

There has been extensive characterization of the permanent damage effects of ionizing radiation exposure of semiconductor microcircuits and devices for evaluation and qualification in systems required to survive space or nuclear weapon radiation exposure. The estimated ranges of observed hardness on a variety of semiconductor devices are shown in Figure 3 (Refs. 1,2).

In summary, the minimum level of concern for ionizing radiation exposure is on the order of 1,000 rads(Si) for the most sensitive devices; virtually all microcircuit technologies may be suspect at exposure levels of 10,000 rads(Si), and, with hardening and performance downscoping, an electronic system can be realized that can perform after exposure to greater than 1 Mrad(Si).

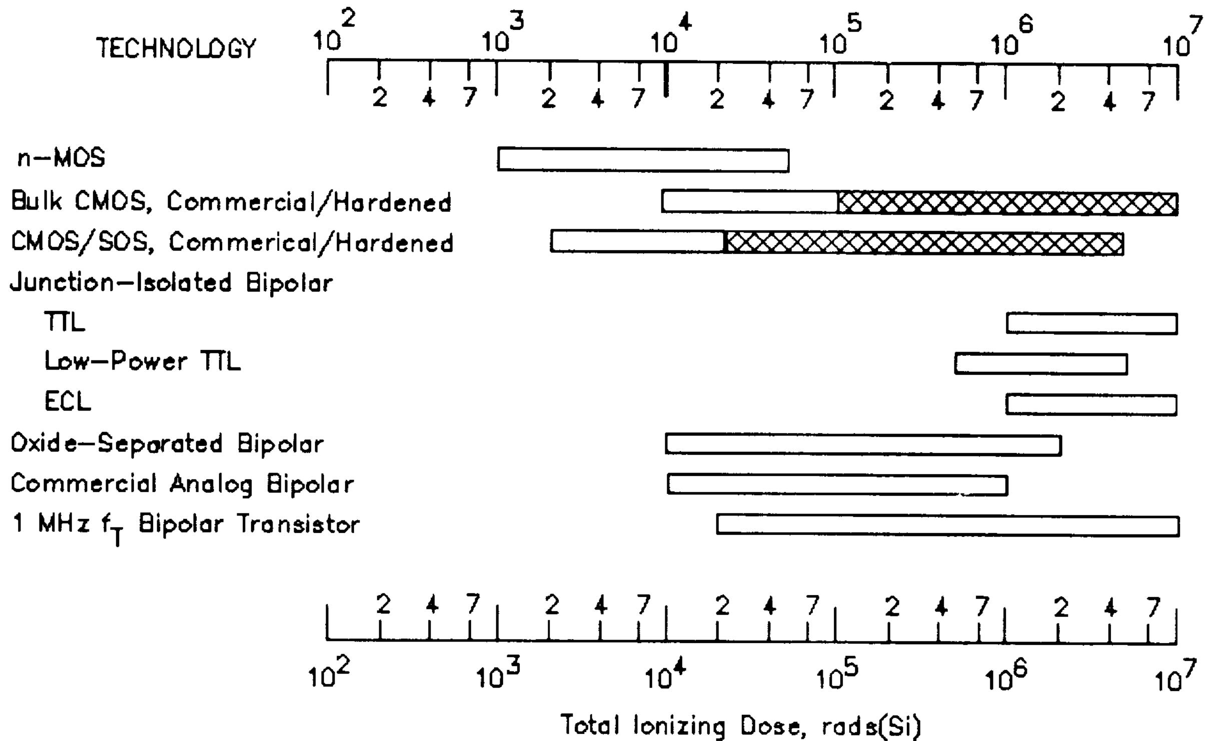

FIGURE 3

Accumulated Ionization Failure Mechanisms

The basic failure mechanisms of accumulated ionization damage in semiconductor devices, as summarized in Figure 4, are the result of hole-electron pair generation in critical silicon-dioxide isolation layers. The first failure mechanism is the result of holes being trapped in the oxide layer after the electrons are swept out by the applied electric field. The second failure mechanism is the result of an increased density of interface states formed at the active-silicon:silicon-dioxide interfaces. The manifestations of these basic failure mechanisms in the microcircuit elements include threshold voltage shift of the MOS transistors, gain degradation of the bipolar transistors, and a general increase in junction leakage currents (Ref. 3). At the overall circuit level, the result is degradation of overall performance such as drive capability and switching speed. Eventually, with sufficient exposure, the damage becomes sufficient to cause functional failure of the microcircuit.

- Accumulated Ionization
  - Oxide Trapped Charge
  - Interface States
    - Threshold Voltage Shift
    - Increased Leakage Current
- Parameter Degradation
- Functional Failure

FIGURE 4

CMOS Inverter Failure Modes

The nature of the observed failure of even simple microcircuits in application can be relatively complex. For example, considering a hypothetical illustration of the threshold voltage shift of the n-MOS and p-MOS transistors of an inverter pair, as shown in Figure 5, circuit failure can occur in at least three different ways depending on the circuit application. In the first case, if the application is very sensitive to power supply leakage current, failure will be observed as soon as the threshold voltage of the n-MOS transistor becomes less than zero. If the design is tolerant to power supply leakage current, at a higher exposure level (in this example) failure may be the result of an unacceptably large shift in the p-MOS transistor threshold voltage. Finally, if tolerant to the first two, functional failure in the inverter will inevitably result when the sum of the n-MOS and p-MOS threshold voltages exceeds the power supply voltage.

To further complicate the situation, the threshold voltage shifts of the MOS transistors are functions of the applied bias during radiation exposure as well as the intensity (or dose rate) of the exposure. The point here is that to interpret the observed effects in a complex microcircuit it is necessary to understand the basic nature of the effects in the individual element technology.

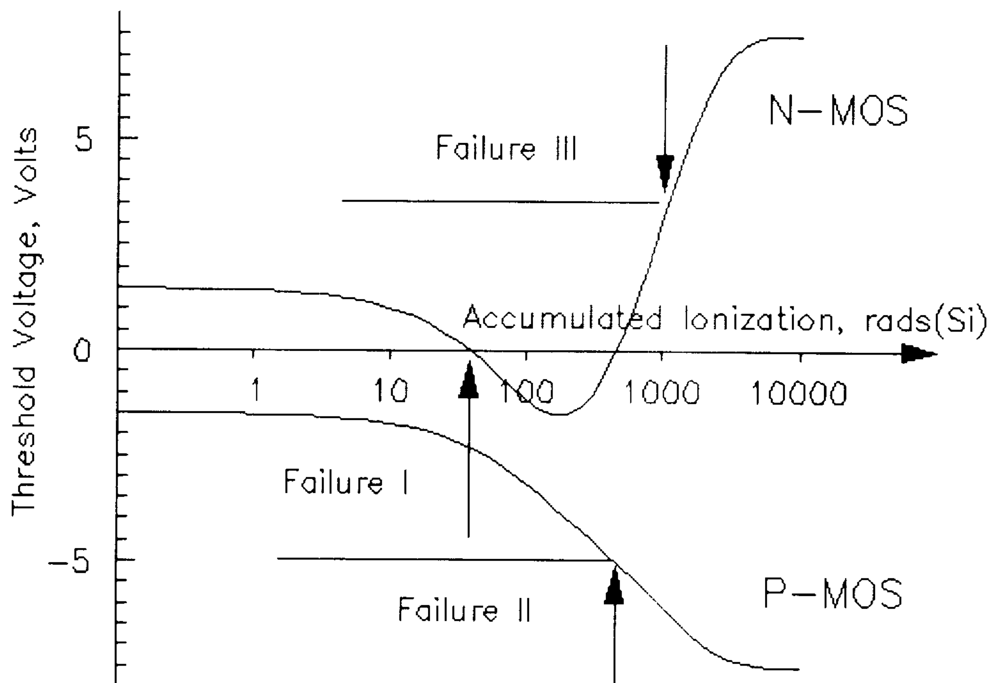

FIGURE 5

N-MOS Transistor Threshold Voltage Shift

To illustrate, consider the basic nature of variations in the threshold voltage shift of an n-MOS transistor, illustrated in Figure 6. As mentioned previously, the two basic failure mechanisms involved are trapped charge and interface states (Ref. 3). As it turns out, in an n-MOS transistor, the trapped charge results in a negative shift of the threshold voltage and the interface state buildup results in a positive shift of the threshold voltage. During ionizing radiation exposure, both trapped charge and interface states are created continuously. Also during a long exposure (e.g., greater than seconds) the trapped charge anneals and the interface state density tends to accumulate. As a result, the observed threshold voltage shift with exposure is a strong function of the time dependencies of trapped hole annealing and interface state buildup. As shown, only the relative rate of interface state buildup is varied. If the interface state buildup is rapid, the effects of trapped charge are nicely compensated and the minimum threshold voltage of the transistor remains greater than zero. Conversely, if the interface state buildup is slow, the negative excursion of the threshold voltage is substantial. It should be noted that, at least in this hypothetical example, for sufficiently long exposures, eventually the interface state buildup will dominate and the threshold voltage shift will increase above its initial value.

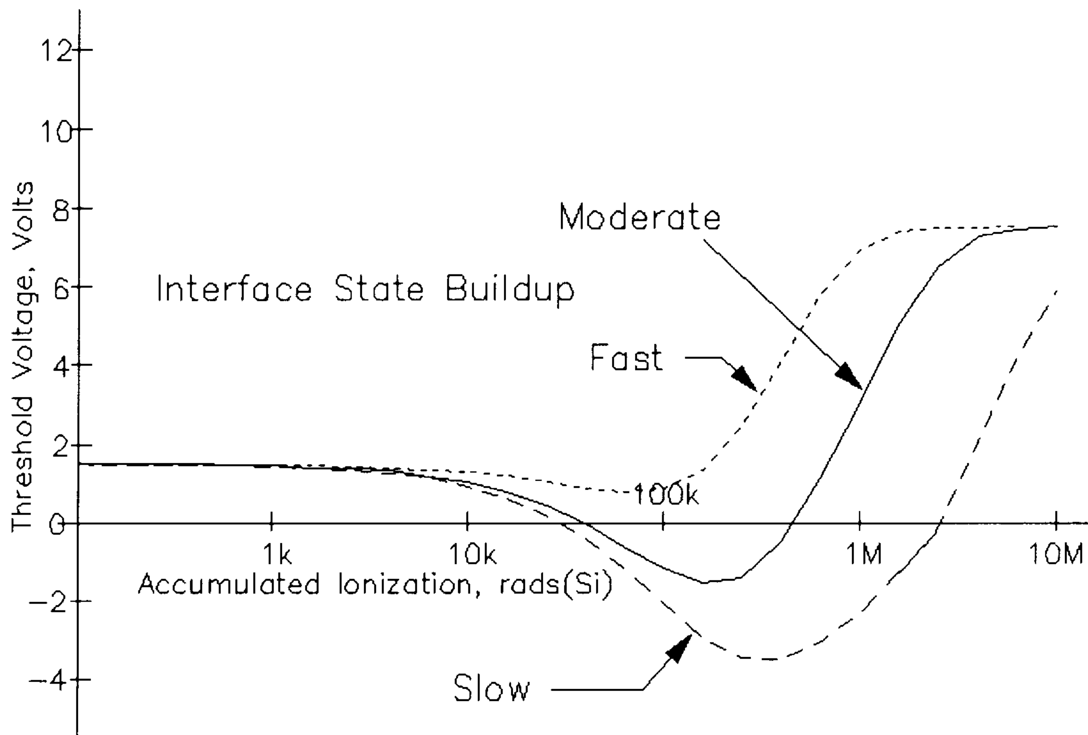

FIGURE 6

Variations in Microcircuit Hardness

As an example of the significance of the exposure environment on the effective microcircuit hardness, consider a hypothetical (and somewhat contrived) example of the effective failure level of three different microcircuits (Figure 7). It will be assumed that each of the three types was measured at an effective hardness of 100,000 rads(Si) for a 10,000 second exposure in a Cobalt-60 source. If the microcircuit hardness is essentially determined by interface states (as might be the case for some MOS microcircuits), the failure level will be highest for high-intensity exposures at short times following radiation exposure. As the exposure time increases, the effect of the interface states will increase and the effective hardness will

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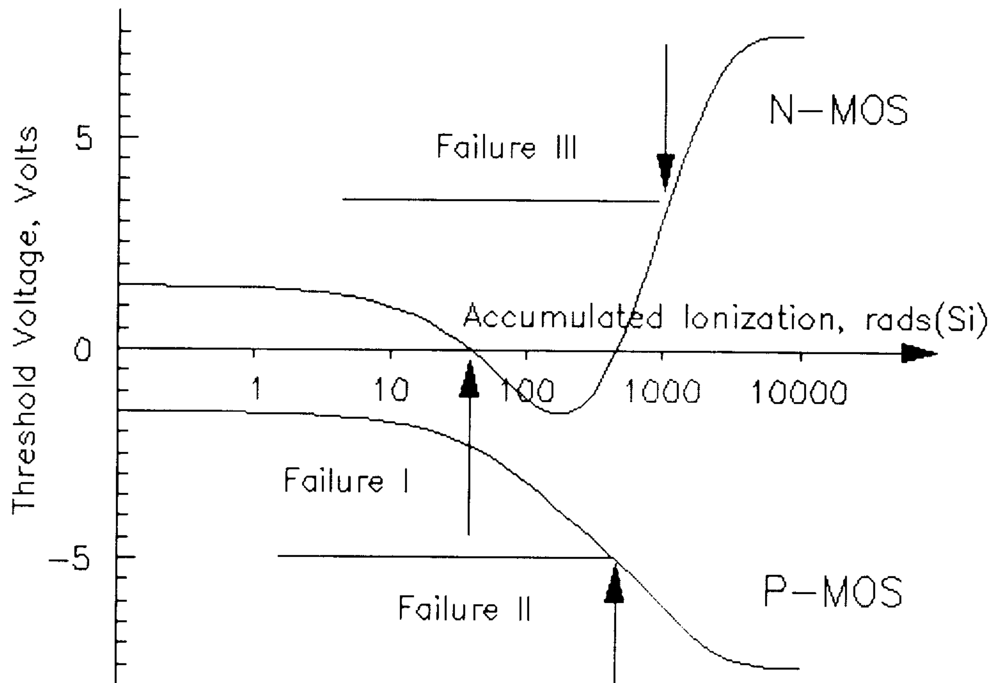

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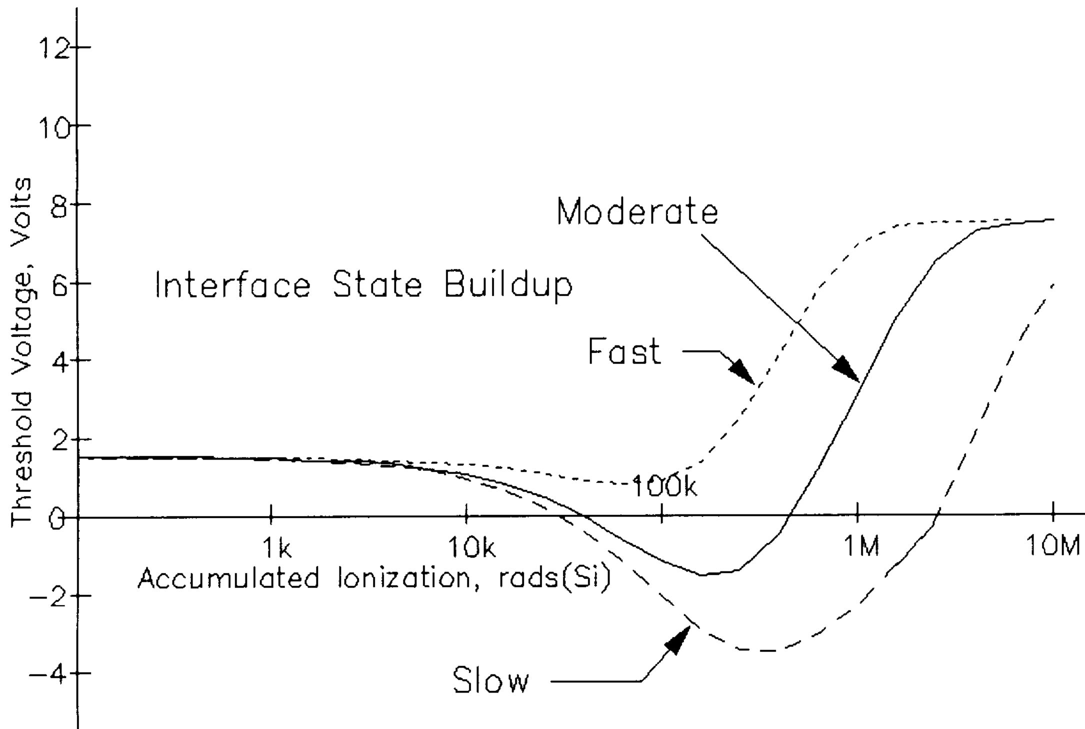

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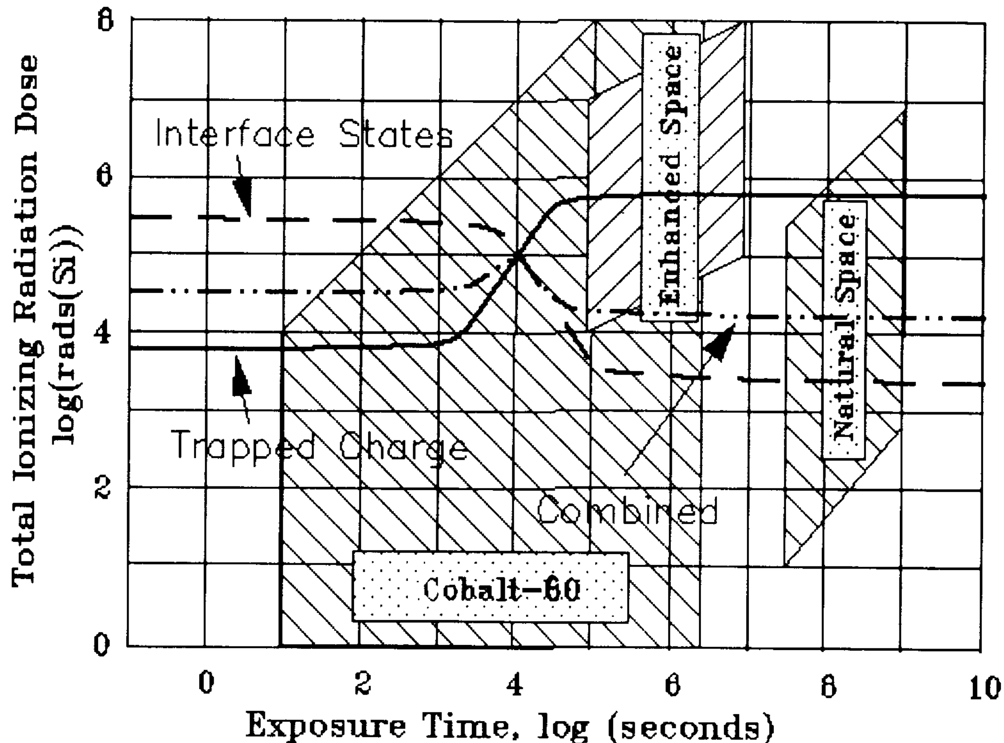


FIGURE 7

Displacement Damage Failure Mechanisms

In addition to accumulated ionizing radiation effects, exposure to the high-energy space proton environment causes atomic displacement damage in semiconductor devices and microcircuits, summarized in Figure 8. The basic failure mechanism of the atomic displacements is an accumulated reduction in the silicon minority carrier lifetime which, in turn, degrades the current gain of bipolar transistor elements and increases junction leakage currents (Ref. 3). The observed effects of the element degradation are accumulated performance degradation of the microcircuit and, eventually, functional failure.

- Displacement Damage
  - Minority Carrier Lifetime Degradation
    - Bipolar Gain Degradation
    - Increased Leakage Currents
- Parameter Degradation
- Functional Failure

FIGURE 8

Range of Neutron Damage Susceptibilities

Almost all the data on semiconductor device susceptibility to radiation-induced atomic displacement damage have been obtained by exposure to the neutron environment of nuclear reactors. This work has been done to support the hardened design of military systems that must survive a nuclear weapon radiation environment. Shown in Figure 9 are the estimated ranges of neutron damage susceptibility for the same semiconductor device technologies shown previously for accumulated ionization damage (Refs. 1,2). In terms of relative susceptibility, the MOS technologies, not critically dependent on high minority carrier lifetime for performance, are very tolerant to neutron exposure. Those technologies depending critically on high minority carrier lifetime such as the wide-base power transistor, commercial analog microcircuits using wide-base lateral pnp transistors, and older digital microcircuits are relatively susceptible to displacement damage. Modern digital microcircuits (and hardened analog microcircuits) use very fast bipolar transistor elements and are much less susceptible to displacement damage.

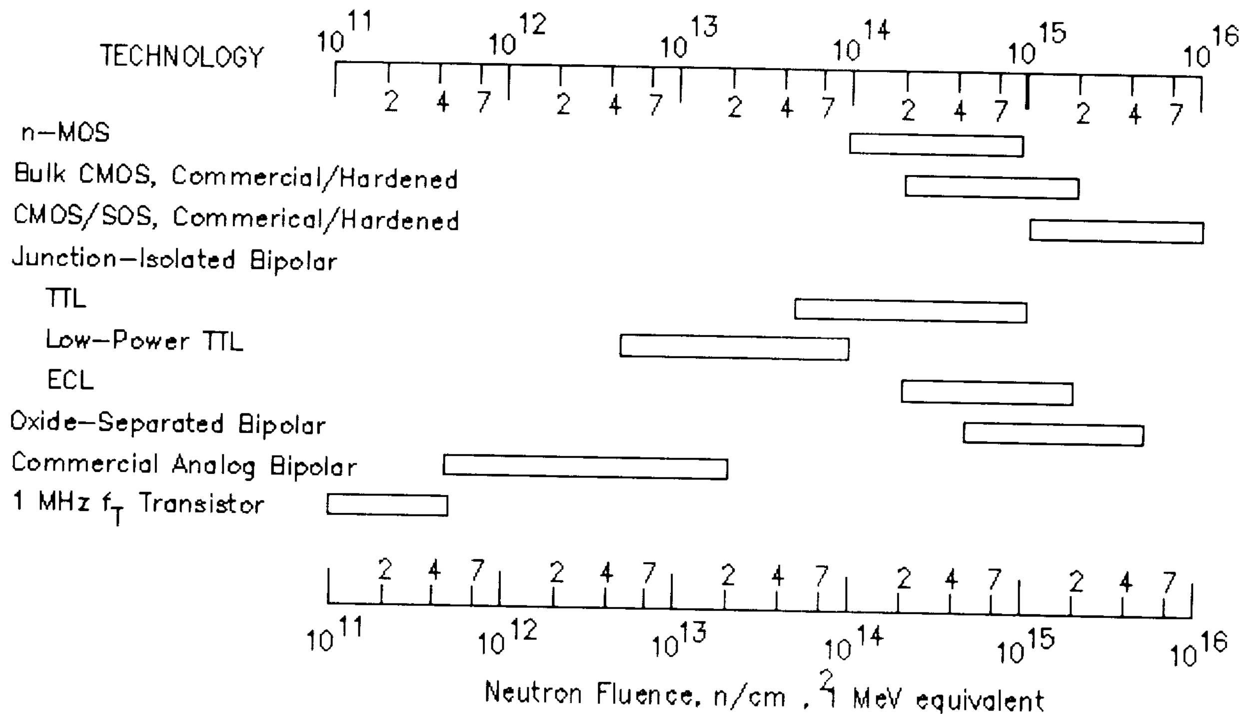


FIGURE 9

Schematic Representation of Device Susceptibility

Determination of the dominant failure mechanisms in electronics piece parts is important in the determination of the laboratory facilities required to evaluate and qualify candidates. Through careful analyses and experimental validation, the relative effects of ionization and displacement damage have been established for both the high-energy protons and electrons of the space radiation environment (Refs. 7,8). The ionizing contribution can then be related to device failure levels as observed in laboratory exposures such as with the use of a Cobalt-60 source. The displacement damage contribution can then be related to the device failure levels resulting from nuclear reactor exposure. Shown in Figure 10 are the device failure ranges. The lines represent the ratio of displacement damage and ionization damage for high energy protons and electrons. With a little reflection, it can be seen that if the device failure range falls above the particle equivalent line, the dominant failure mechanism is ionization (Ref. 2). Conversely, if the device failure range falls below the particle equivalent line, the dominant failure mechanism is displacement damage. As shown, ionization is the dominant failure mechanism for virtually all semiconductor technologies for high energy electron exposure. The exception is the susceptibility of the solar cells that are very sensitive to displacement damage and insensitive to ionization damage. For proton exposures, either displacement and ionization failure mechanisms can be dominant, but only for those technologies most susceptible to displacement damage. For virtually all modern digital microcircuit technologies, the dominant failure mechanism is ionization.

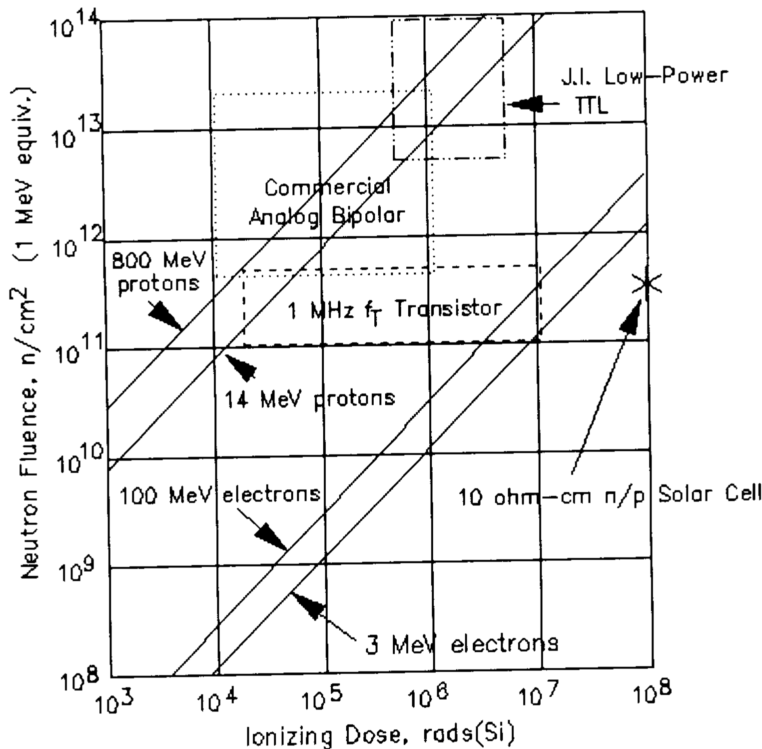


FIGURE 10

Single Particle Interactions in a P-N Junction (Ref. 9)

Single event effects in semiconductor devices, as shown in Figure 11, are the result of the intersection of the particle ionization path with a p-n junction. The result is a junction transient current that determines the overall device effect. The ionization track of the particle is characterized by its Linear Energy Deposition and range. For a high-energy cosmic ray (such as a 100 MeV lithium ion) the particle range is long compared to the semiconductor device dimensions. On the other hand, high energy proton effects are the result of energy deposition produced by the atomic product of a nuclear interaction between the proton and an atom of the semiconductor material such as a silicon recoil or product alpha particle.

Because the junction transient current is a very fast pulse (typically less than 1 ns) the circuit or device effect can be characterized in terms of a critical charge. The charge collected is determined by the particle LET and the effective collection volume of the junction. The overall susceptibility of the device or circuit is characterized by a cross section, typically in units of inverse square centimeters (i.e., cm^-2). The probability of observation of the effect is the product of the particle fluence and the cross section.

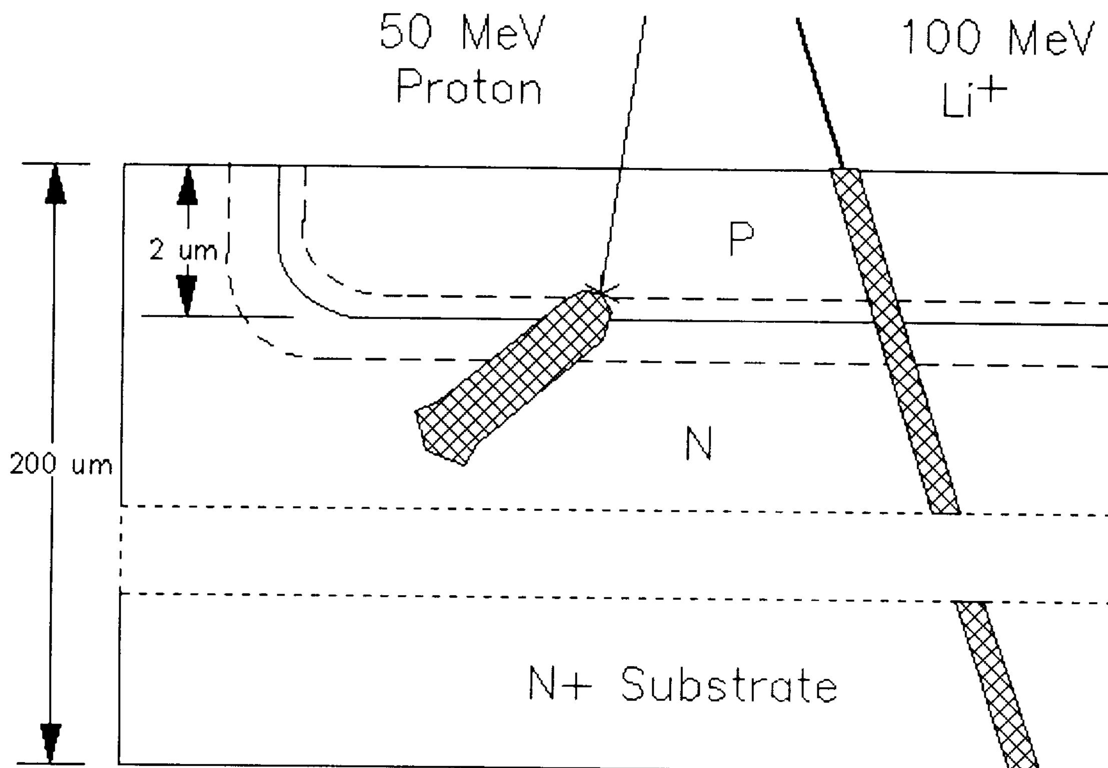


FIGURE 11

Single Particle Failure Mechanisms (Refs. 10-14)

The basic failure mechanisms of a single particle in a semiconductor device, summarized in Figure 12, are the ionization produced by the primary or secondary particles. The failure mechanisms observed in the overall device include the upset of stored data and potential damaging effects of latchup or device burnout. The data upset can be the result of a particle-induced change-of-state (i.e., flip) in a memory cell or flip-flop, or an electrical transient that can be interpreted as valid data by a latch. The most sensitive devices to bit upset effects are dynamic random-access memories, which are generally unacceptable for space applications. Bit upset rates for very sensitive semiconductor memories in space can be as great as 1E-4 upsets per bit-day, that is an average of one bit upset for every 10,000 bits of stored data in a single day, to less than 1E-8 upsets per bit-day in hardened semiconductor memories.

Latchup has been observed as a result of high-energy heavy-ion (i.e., cosmic ray) exposure in a number of junction-isolated CMOS memories. Dielectric-isolated memory technologies such as CMOS/SOS or CMOS/SOI can be designed to be latchup immune.

Single particle-induced burnout has been observed in n-channel power MOSFET transistors and electrically-alterable programmable read-only memories. The burnout susceptibility of the n-Power MOSFETs is a strong function of margin between the operating voltage and the d-c junction breakdown voltage. The burnout susceptibility of the EEPROMs has been observed only during the application of high-voltage during the write cycle when altering the stored data.

- Single Event Effects
  - Particle Ionization Track
  - High–LET Particle Production
- Memory Bit Upsets
- Latch Data Upsets
- Parasitic Latchup
- Burnout
  - Power MOSFET's
  - Elec. Er. PROM's

FIGURE 12

Bit Upset in a Read/Write Semiconductor Memory

The number of bit upsets in a read/write memory increases with particle exposure, as shown in Figure 13, until the memory is reset. Typically, the upset is that of a single memory cell. However, depending on the memory design, a single hit at specific locations can cause either clusters of upsets, or upsets along a row or column of the memory.

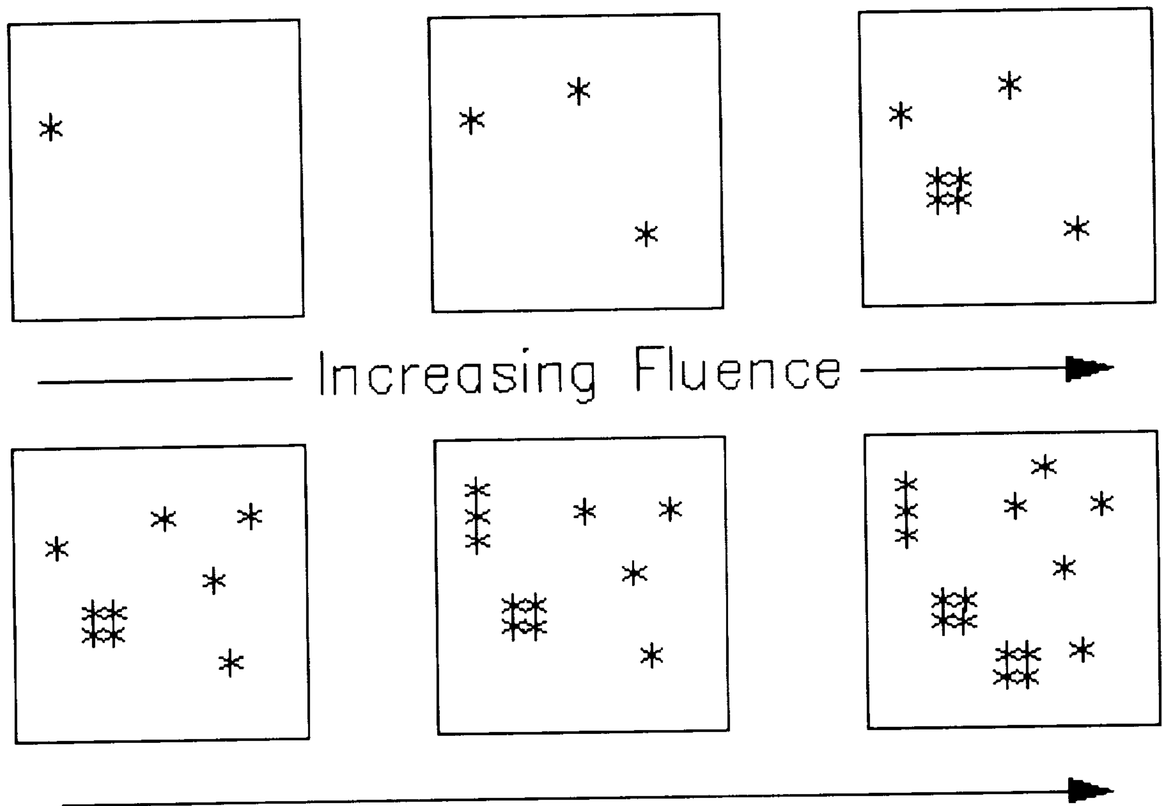


FIGURE 13

Bit Upset in a Complex Microcircuit

An important issue in the characterization of single-particle-induced upsets in complex microcircuits is that of the observability of the effect. Figure 14 illustrates cases where the induced upset can either be unobservable or can result in a large number of observed data errors.

The observed effects of an upset in the scratch-pad memory or data latches of a complex microcircuit are a strong function of the location of the upset and subsequent processing of the erroneous data. As the data is processed, the error can propagate down multiple paths. In some cases, these paths never reach an observable output and no upset is observed. The error was present, but under the test conditions used, was simply not observed.

On the other hand, the propagation of the original single upset can result in a multiplicity of paths, each of which, in the worst-case, produces errors at a number of microcircuit outputs. From the observable data, the determination of the actual number of internal upsets can be very challenging but is essential to determine the basic susceptibility of the microcircuit. In practice, careful modeling of the basic cells and a comprehensive selection of test conditions must be used.

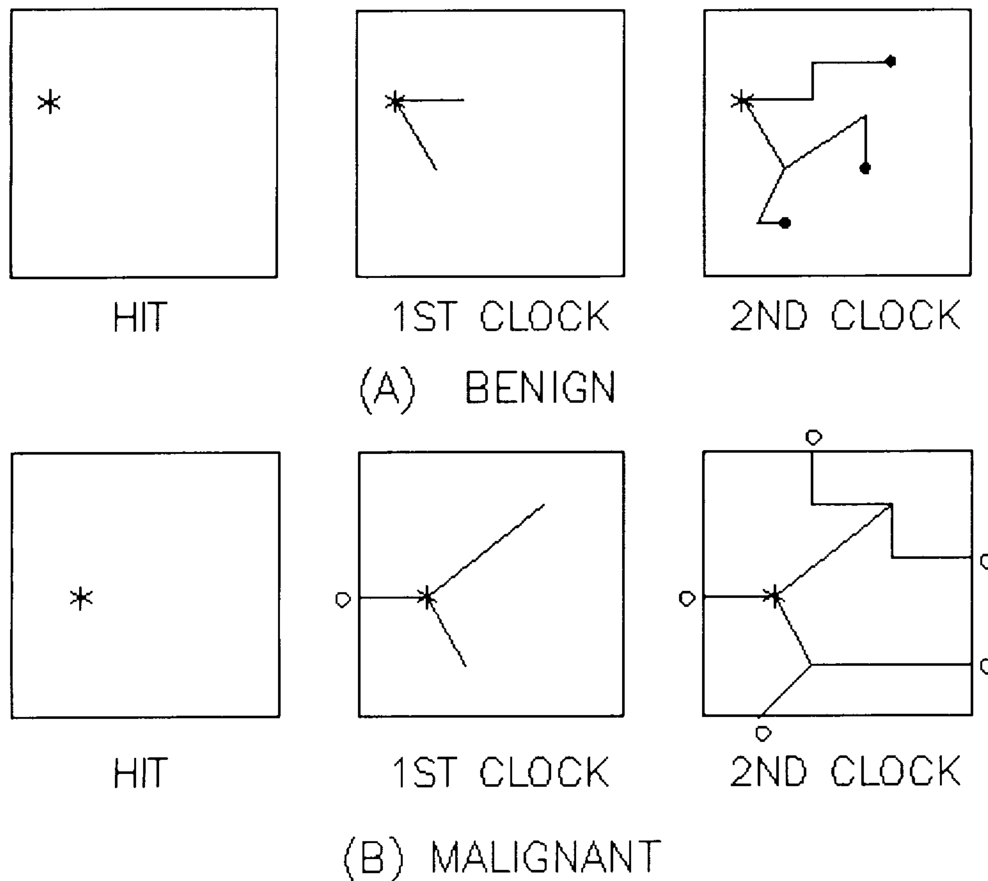


FIGURE 14

Single Event Upset Rate vs Altitude for Circular Orbits

The observed bit upset rate of microcircuits is a function of the satellite orbit as well as the microcircuit technology, as shown in Figure 15 (Ref. 9). At low and high altitudes, the bit upset rate is dominated by the cosmic ray environment. At altitudes from approximately 700 to 3,000 nautical miles, the bit upset rate is dominated by high-energy protons (for a circular orbit). The orbital dependence as shown, scales with the fundamental bit upset rate of a given microcircuit technology. A highly susceptible technology might have a bit upset rate on the order of 1E-4 upsets per bit-day. On the other hand, a less susceptible (or hardened) technology might have a bit upset rate on the order of 1E-8 upsets per bit-day or less.

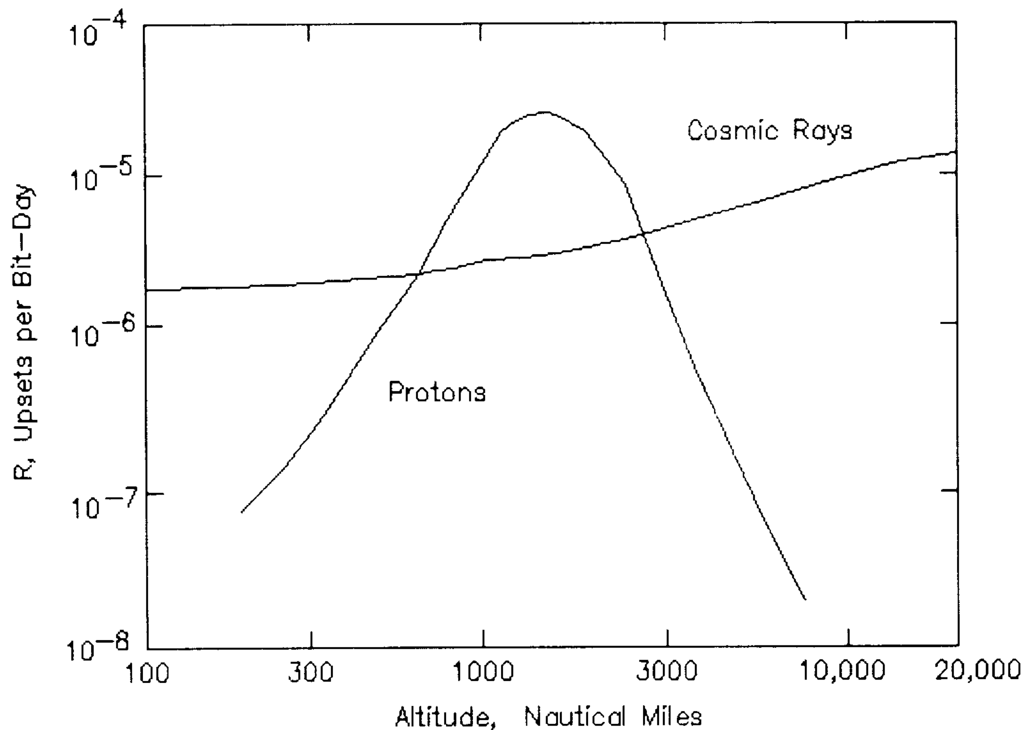


FIGURE 15

Microcircuit Parasitic PNPN Latchup Path

The mechanism of single-particle-induced latchup in a microcircuit is the regenerative action of an internal parasitic pnpn path when triggered by the particle-induced transient current pulse, as shown in Figure 16. Latchup will result when the transient current pulse is sufficiently large to initiate regenerative switching, and if there is an allowable current operating point at a dc current above the I-V characteristic holding current. The most susceptible microcircuit to single-particle-induced latchup is junction-isolated CMOS (Ref. 11). Latchup is also possible in junction-isolated bipolar, but has not yet been observed. Dielectric isolated technologies such as CMOS/SOS or CMOS/SOI are latchup-free.

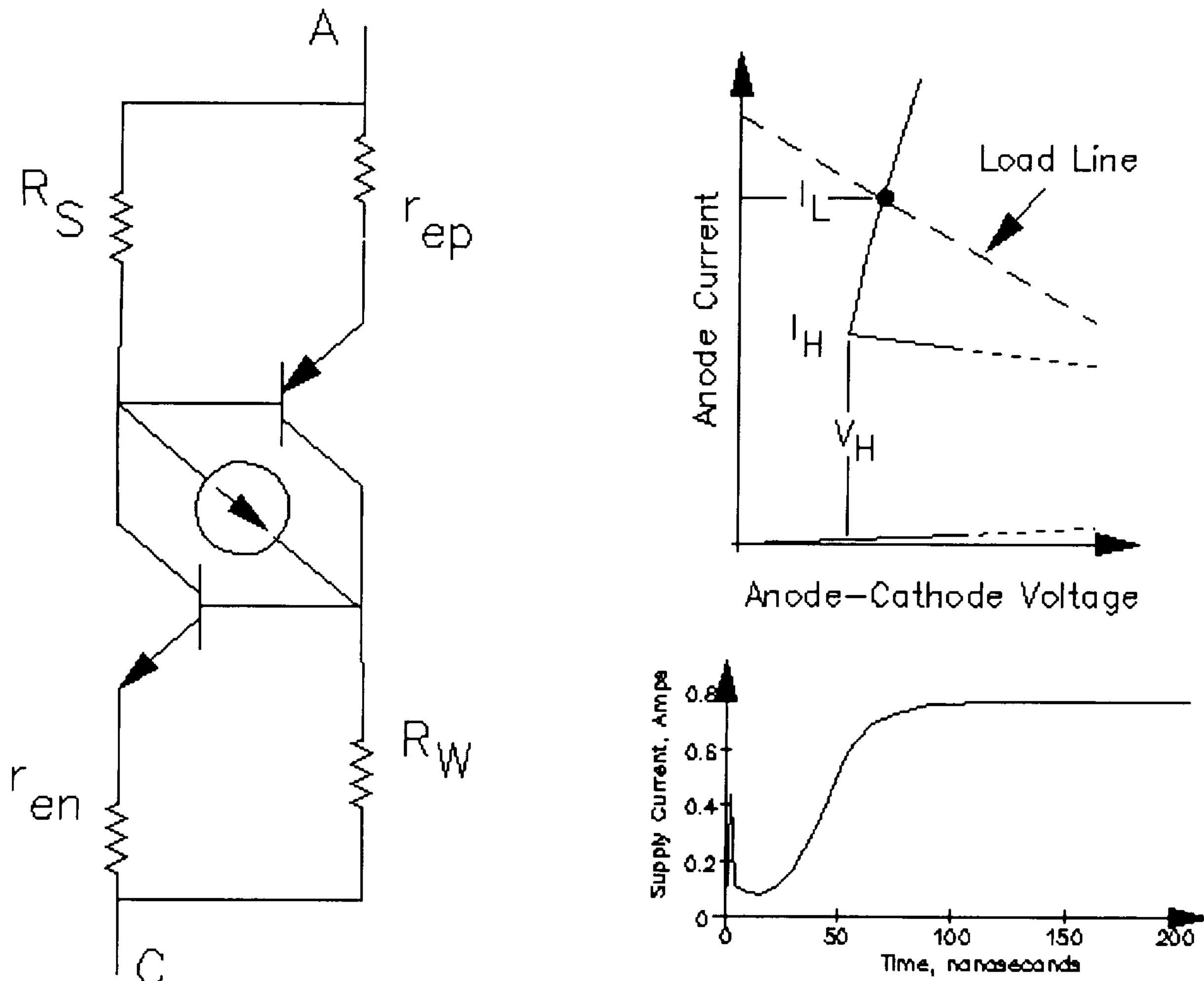


FIGURE 16

Power MOSFET Cross Section

The single-particle-induced burnout susceptibility of a Power MOSFET (shown in cross section in Figure 17, courtesy of John Adolphson, NASA Goddard) is the result of avalanche multiplication of carrier generated in the ionization track which results in current-mode second-breakdown (Ref. 12). Burnout will occur if the drain bias voltage is above the second-breakdown sustaining voltage (which can be substantially lower than the dc drain-source breakdown voltage).

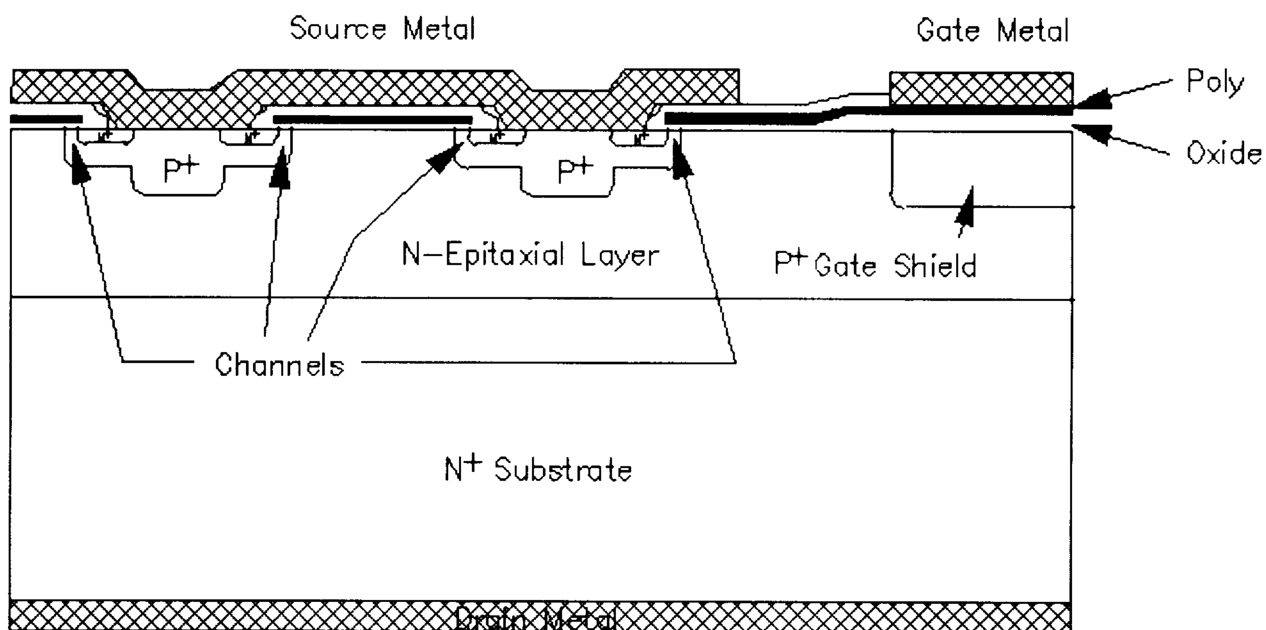
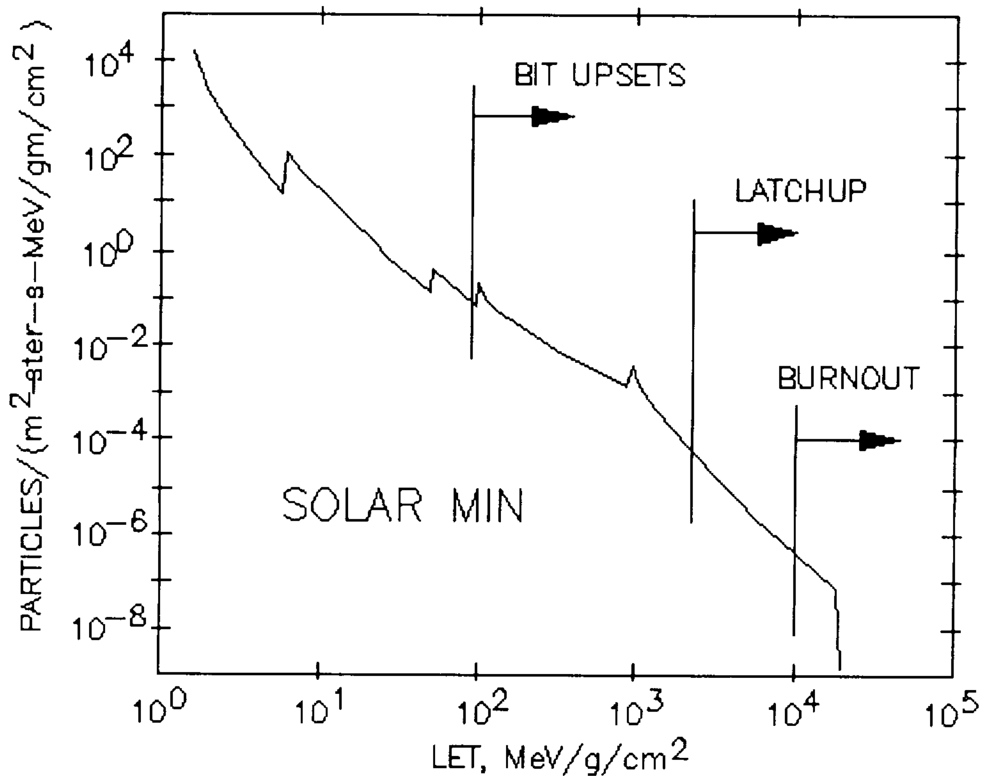


FIGURE 17

Cosmic Ray LET Spectra with Device Failure Mechanism Thresholds

Cosmic ray effects in semiconductor devices and microcircuits can be characterized by the energy deposition of the particle in the bulk semiconductor (i.e., Linear Energy Transfer or LET), and the cross section which is the probability of the effect normalized by particle fluence. Figure 18 shows the LET spectrum of cosmic rays (Ref. 15) with estimated thresholds for the various failure mechanisms presented. Clearly, bit upsets are quantitatively of greatest concern. The LET threshold for latchup is much greater than that for bit upset, and that for burnout is even greater than that of latchup. While latchup and burnout are much less likely that bit upset, it should be noted that the consequences of these effects on system performance can be much more severe.



*NRL Memorandum Report 4864, August 1982

FIGURE 18

Hardening Approaches

There are three basic hardening approaches that can be used for spacecraft electronics, as summarized in Figure 19. The first, of course, is the selection of components of minimum susceptibility. Unfortunately, however, it is very difficult to realize both very high hardness and very high electrical performance.

Shielding, for some aspects of the environment, can be very effective. Careful placement of the sensitive components can take advantage of the shielding of existing, less sensitive, spacecraft materials. Additional shielding can be added as necessary (until a fundamental limit is reached) at either the individual semiconductor device or the subsystem electronics box. It is important to note that while shielding is very effective for electrons and low-energy protons, the shielding to electrons is limited by the generation of bremsstrahlung gamma rays which are much more difficult to shield. Shielding is generally quite ineffective to reduce the effects of high-energy protons, and can be counter-effective for the shielding of cosmic rays. For the cosmic rays, shielding tends to be ineffective and even somewhat counter-productive.

Hardening techniques can be employed that include well known redundancy and error detection and correction techniques to reduce the effect of bit upsets. Hardening techniques for latchup and burnout effects on the system level can include current limiting, but hardened device selection is probably the preferred approach.

- Component Selection
- Shielding
  - Self-Shielding
  - Spot Shielding
  - Box Shielding
  - Note: Shielding Limitations
    - Electrons – Bremsstrahlung limit
    - High-energy Protons
    - Cosmic Rays
- System Hardening
  - Redundancy
  - Error Detection and Correction
  - Current Limiting (Latchup/Burnout)

FIGURE 19

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